Five-element circuit model using linear-regression method to correct the admittance measurement of metal-oxide-semiconductor capacitor

Chao-Ching Cheng, Chao-Hsin Chien, Guang-Li Luo, Jun-Cheng Liu, Yi-Cheng Chen, Yao-Feng Chang, Shin-Yuan Wang, Chi-Chung Kei, Chien-Nan Hsiao, and Chun-Yen Chang

Citation: Journal of Vacuum Science & Technology B **27**, 130 (2009); doi: 10.1116/1.3058724
View online: http://dx.doi.org/10.1116/1.3058724
View Table of Contents: http://scitation.aip.org/content/avs/journal/jvstb/27/1?ver=pdfcov
Published by the AVS: Science & Technology of Materials, Interfaces, and Processing

Five-element circuit model using linear-regression method to correct the admittance measurement of metal-oxide-semiconductor capacitor

Chao-Ching Cheng
Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan 300, Republic of China

Chao-Hsin Chien
Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan 300, Republic of China and National Nano Device Laboratory, Hsinchu, Taiwan 300, Republic of China

Guang-Li Luo
National Nano Device Laboratory, Hsinchu, Taiwan 300, Republic of China

Jun-Cheng Liu, Yi-Cheng Chen, Yao-Feng Chang, and Shin-Yuan Wang
Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan 300, Republic of China

Chi-Chung Kei and Chien-Nan Hsiao
Instrument Technology Research Center, National Applied Research Laboratories, Hsinchu, Taiwan 300, Republic of China

Chun-Yen Chang[a)]
Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan 300, Republic of China

(Received 25 June 2008; accepted 1 December 2008; published 12 January 2009)

The authors present a linear-regression method based on a five-element circuit model to correct measured capacitance-voltage and conductance-voltage curves. This model explains the effects of series resistance and parasitic capacitance/inductance on the frequency dispersion of measured capacitance and the magnification of measured conductance. These extracted parasitic components show significant dependencies on the geometry of capacitor structure, thereby causing different frequency-dependent capacitance characteristics in measurements. © *2009 American Vacuum Society.* [DOI: 10.1116/1.3058724]

I. INTRODUCTION

Currently, measurement of capacitance-voltage (C-V) and conductance-voltage (G-V) curves is a method commonly used to determine equivalent-oxide thickness (EOT), but also, to extract the interface trap density (D_{it}) in metal-oxide-semiconductor (MOS) capacitors.[1] However, this technique can no longer accurately obtain both EOT and D_{it} values in MOS capacitors with large gate leakage current and series resistance, especially when scaling the EOT below 1.8 nm.[2,3] An equivalent-circuit approach using distributed voltage-controlled resistor-capacitor (RC) networks has been proposed to explain these nonideal behaviors on the measured capacitance curves.[3] It was found that an increase in the measured frequency to the range of radio frequencies (RF), e.g., over 10 MHz, is a good approach to overcome these bottlenecks by reducing the overall impedance of the equivalent circuit of the dielectric film.[4,5] Accordingly, RF C-V probes to measure the leaky oxides catch more attention in recent years.[6,7] Another method in tackling the above issue is to introduce a dual-frequency correction using a three-element circuit model.[8,9] For better accuracy, four-element[10] and five-element[11] models were subsequently proposed and demonstrated by adding either parasitic inductance or capacitance. In practice, the validity and application limit of the dual-frequency correction method were found to depend strongly on the adopted frequencies and capacitor area.[11,12] In this study, we propose another five-element circuit model and linear regression of multifrequency admittance measurement targeting to recover the real electrical properties of MOS capacitors as the effects of leakage current and parasitic elements are involved. According to our analyses, the choice of which parasitic component to add, i.e., capacitance or inductance, is closely linked to the structural design of measured devices. In addition, we also evaluated the relative significance of these external components in the admittance correction.

II. EQUIVALENT-CIRCUIT MODEL OF FIVE ELEMENTS

Different to separately extract values of either R_S/L_S or R_S/C_S parasitic components in previously reported circuit models,[10,13] we consider the comprehensive influence of these parasitic components in our correction model and obtain the more reliable capacitance and conductance characteristics of MOS capacitors. Figure 1(a) shows the two-element parallel circuit model used for typical admittance characterization in an impedance meter, where C_m is the measured capacitance and $G_m(=1/R_m)$ is the measured conductance. Usually, this model cannot describe the real behavior of the small-signal frequency response of a MOS capacitor. Thus, we propose an integrated-circuit model with five elements, as shown in Fig. 1(b), to correct the measured raw data; C_C is the corrected dielectric capacitance in parallel

a)Electronic mail: cyc@mail.nctu.edu.tw

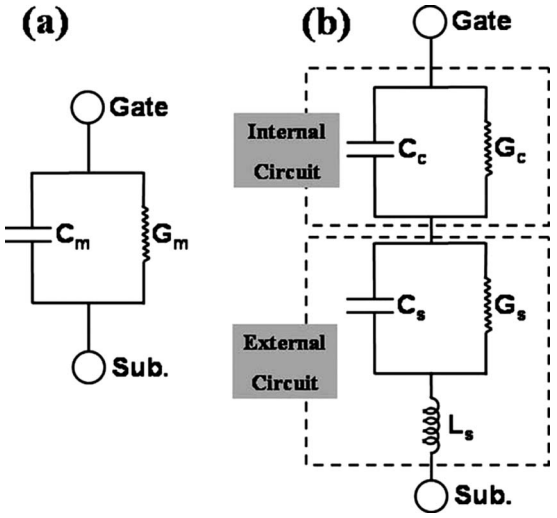

FIG. 1. Small-signal equivalent-circuit models of MOS capacitors: (a) simple parallel circuit model and (b) new five-element circuit model.

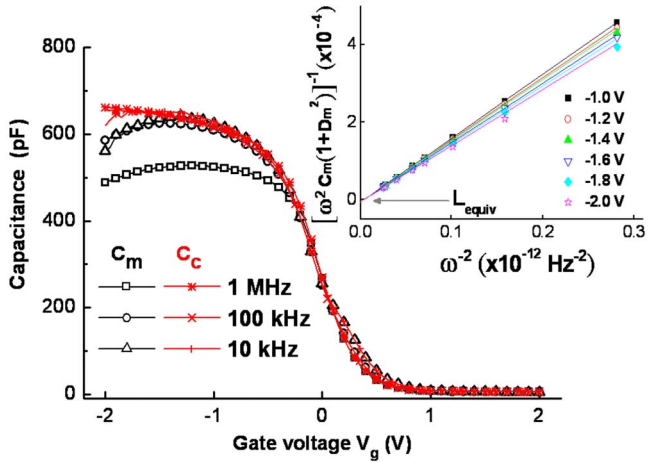

FIG. 2. (Color online) Measured and corrected *C-V* curves of the $Pt/Al_2O_3/p$-Si MOS capacitor with gate area $=3.85\times10^{-4}$ cm^2. The inset shows the extraction of L_{equiv}.

with a corrected conductance G_C, where G_C includes the effects of both the gate leakage current and the loss due to ac conductance arising from interface traps. In the part of external circuit, the conductance $G_S(=1/R_S)$ represents all series resistances, in parallel with parasitic capacitance C_S and in series with parasitic inductance L_S. Equating the real and imaginary parts of the total impedance in Figs. 1(a) and 1(b), we can obtain

$$\text{(Real)} \quad \frac{G_m}{G_m^2+(\omega C_m)^2}=\frac{G_C}{G_C^2+(\omega C_C)^2}+\frac{G_S}{G_S^2+(\omega C_S)^2}, \quad (1)$$

(Imaginary)

$$\frac{C_m}{G_m^2+(\omega C_m)^2}=\frac{C_C}{G_C^2+(\omega C_C)^2}+\frac{C_S}{G_S^2+(\omega C_S)^2}-L_s. \quad (2)$$

Here ω is the angular frequency. With the assumption of $(G_S)^2 \gg (\omega C_S)^2$, the above two equations can be simplified and rearranged as

$$\text{(Real)} \quad \frac{D_m}{\omega C_m(1+D_m^2)}=\frac{D_C}{C_C(1+D_C^2)}\left(\frac{1}{\omega}\right)+R_S, \quad (3)$$

(Imaginary)

$$\frac{1}{\omega^2 C_m(1+D_m^2)}=\frac{1}{C_C(1+D_C^2)}\left(\frac{1}{\omega^2}\right)+R_S^2 C_S-L_S, \quad (4)$$

where $D=G/\omega C$ is the dissipation factor. As seen, a linear-regression plot of $D_m/[\omega C_m(1+D_m^2)]$ vs $1/\omega$ evidently has an extrapolated value of R_S. Also, we further define an equivalent parasitic inductance L_{equiv}, which is equal to the intercept of $(R_S)^2C_S-L_S$, and whose value can be extracted from the inverse-square dependence on angular frequency ω, as given by Eq. (4). To make the above assumption hold, i.e., $(G_S)^2 \gg (\omega C_S)^2$, the measured parasitic capacitance C_S should be lower than 1000 pF at a frequency of 1 MHz for the typical G_S value of $\sim$0.01 mhos ($R_S \sim 100\ \Omega$ in most cases).

III. APPLICATION EXAMPLES AND DISCUSSION

MOS capacitors of the $Pt/Al_2O_3/p$-Si/Al-backside structure were fabricated, where Al_2O_3 was deposited by the atomic-layer deposition technique using trimethylaluminum and H_2O. The area of the Pt circular dot was estimated to be $\sim 3.85\times10^{-4}$ cm^2 using the optical microscopy. The *C-V* and *G-V* curves were measured using a HP4284 *LCR* meter, and the gate leakage (*I-V*) characteristics were measured using a Keithley 4200 semiconductor analyzer system. Figure 2 illustrates the measured multifrequency *C-V* curves before (open symbols) and after (crossover symbols) linear-regression correction; a series resistance R_S of $\sim$110 Ω can be extracted from Eq. (3). The inset shows the relationship of $1/[\omega^2 C_m(1+D_m^2)]$ vs $1/\omega^2$ at different accumulation biases for the extraction of L_{equiv}, where an extrapolated value of L_{equiv} is -5.5 μH, implying the dominance of the L_S term, rather than the $(R_S)^2C_S$ term, in our case. We clearly observe the frequency dispersion presented at the accumulation capacitance without the correction, accompanying the *C-V* roll-off behavior due to the high leakage current. Taking into account the effect of these parasitic components, all of the corrected *C-V* curves perfectly align with one another. The extracted capacitance equivalent thickness (CET) was 21 Å based on the accumulation capacitance at $V_g=-2$ V.

The corresponding variation of *G-V* curves as a function of measured frequency is shown in Fig. 3. The conductance curve at the accumulation region measured at 1 MHz significantly decreased after the correction, thereby revealing that a small peak existed at the depletion region due to the contribution of interface-state loss. The effect of the external R_S does dominate at higher frequencies, relative to the impedance of the overall capacitor. We may overcome this problem by performing the measurement at lower frequencies; so that

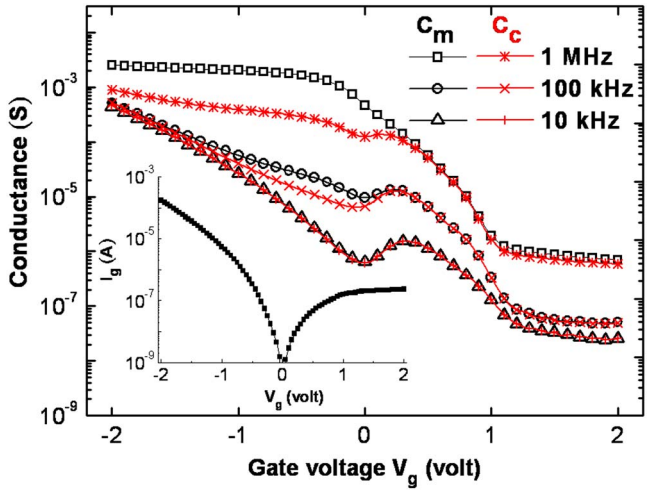

FIG. 3. (Color online) Measured and corrected G-V curves of the $Pt/Al_2O_3/p$-Si MOS capacitor with gate area$=3.85\times10^{-4}$ cm^2. The inset shows I-V characteristics.

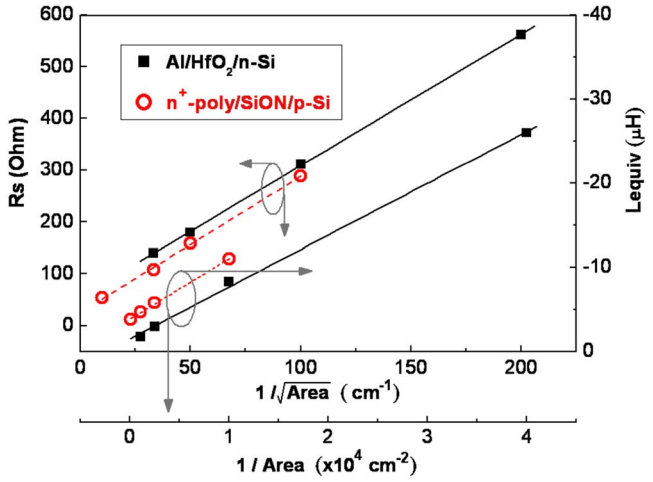

FIG. 4. (Color online) Gate-area dependence of the extracted R_S and L_{equiv} for $Al/HfO_2/n$-Si and n^+-poly/SiON/p-Si MOS capacitors. Note that the negative value of L_{equiv} presented here is due to the dominance of L_s term, as seen from the L_{equiv} definition, $L_{\text{equiv}}=(R_S)^2C_S-L_S$.

the effect of R_S can be omitted. However, the leakage-current issue becomes more severe at lower frequencies; this fact explains why the conductance at accumulation sharply increases with increasing negative gate voltage as the frequency is lowered to 10 kHz. We can further estimate the corresponding static shunt conductance G_{st} from the I-V characteristics shown in the inset of Fig. 3. A value of $\sim2\times10^{-4}$ for G_{st} can be obtained at $V_g=-2$ V, and it contributed the most energy loss in measured conductance curves at lower frequencies.

To clarify the dependence of extracted parasitic components on the capacitor structure, we also prepared two different MOS capacitors, $Al/HfO_2/n$-Si and n^+-poly/SiO_xN_y/p-Si, respectively, by standard photolithography to pattern various gate areas; the corresponding CET are $\sim$24 and $\sim$33 Å for the deposited HfO_2 and SiO_xN_y thin films, respectively. Figure 4 shows the dependence of extracted R_S and L_{equiv} on the gate-electrode area for two tested MOS structures, and they exhibit remarkable area dependences ($R_S\sim1/\text{area}^{1/2}$ and $L_{\text{equiv}}\sim1/\text{area}$). Both samples exhibit the same trend: the capacitor with a smaller area possesses higher absolute values of R_S and L_{equiv} than that with a larger area. These findings agree with the previously reported study.[14] It was also found that larger gate area enhanced the resultant frequency dispersion (not shown here). We note here that this area-induced dispersion behavior can be calibrated effectively by our proposed model.

In addition, we examined other MOS capacitors with different high-k dielectrics, e.g., Gd_2O_3, and found that the measured capacitances increase with respect to the frequency (not shown here); this anomalous phenomenon has been observed by other investigators[9] and can also be understood by our proposed model. Figures 5(a) and 5(b) show the simulated effect of the equivalent inductance L_{equiv} and series resistance R_S on the frequency dispersion of measured accumulation capacitance. All simulation cases illustrated here—after considering the respective parasitic components—will converge to the single corrected capacitance $C_C=920$ pF, i.e., without a frequency-dispersion effect. In Fig. 5(a), we observe that the measured capacitances exhibit a significant drop with respect to frequency as the value of L_{equiv} becomes positive. It implies that when either the C_S term dominates the contribution of the L_{equiv} or the L_S term decreases, we will likely measure a substantial decrease in accumulation

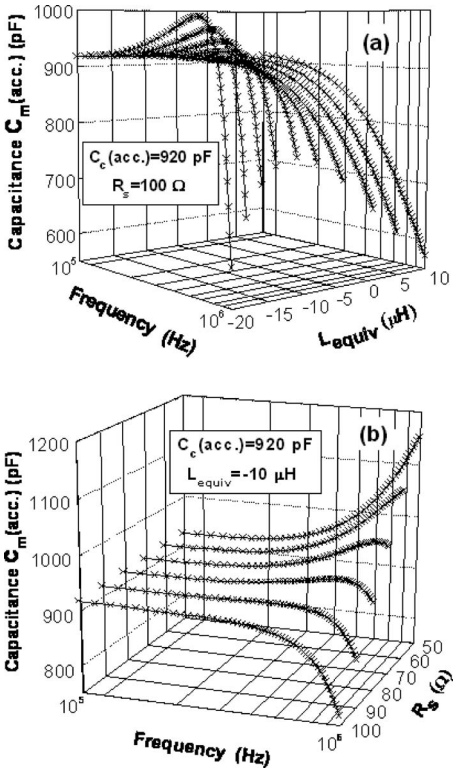

FIG. 5. Effects of the value of the L_{equiv} on the measured accumulation capacitance C_m as a function of frequency with the (a) fixed value of R_S (100 Ω) and (b) fixed value of L_{equiv} (-10 μH). The corrected accumulation capacitance $C_C=920$ pF is used in the simulation.

capacitances with increasing measured frequency. Together with the results from Fig. 4, we conclude that a positive value of the L_{equiv} may be extracted from a large-area capacitor; accordingly, shrinking the capacitor area causes a negative value of the L_{equiv} due to the external inductance L_S of concern. In addition, the measured capacitances are also sensitive to the variation of series resistance R_S, as seen in Fig. 5(b). Lower R_S led to the increasing capacitances with respect to measured frequency, whereas higher R_S caused the opposite behavior. We thus suggest that relative significance of either series resistance R_S or equivalent inductance L_{equiv} strongly correlates the geometry of device structure, measurements, cable-line connection, and other probing system setup, respectively.

IV. CONCLUSIONS

We proposed a five-element circuit model using a linear-regression method to correct the capacitance and conductance measurements of MOS capacitors with thin oxides and high-k dielectrics. This correction model is able to recover the real electrical properties of measured C-V and G-V curves by considering the presence of both the series resistance and equivalent inductance. These external parasitic components depend on measured capacitor area, and they resulted in different behavior of frequency dispersion in C-V characteristics. This method could be employed in calibrating electrical measurements for different MOS structures with thin-oxide and high-k gate dielectrics.

ACKNOWLEDGMENTS

This study was sponsored primarily by the National Science Council of the Republic of China under Contracts Nos. NSC96-2221-E-009-236 and NSC96-2221-E-009-202-MY3.

[1]E. M. Vogel, W. K. Henson, C. A. Richter, and J. S. Suehle, IEEE Trans. Electron Devices **47**, 601 (2000).
[2]W. K. Henson, K. Z. Ahmed, E. M. Vogel, J. R. Hauser, J. J. Wortman, R. D. Venables, M. Xu, and D. Venables, IEEE Electron Device Lett. **20**, 179 (1999).
[3]C.-H. Choi, Y. Wu, J.-S. Goo, Z. Yu, and R. W. Dutton, IEEE Trans. Electron Devices **47**, 1843 (2000).
[4]J. Schmitz, F. N. Cubaynes, R. J. Havens, R. D. Kort, A. J. Scholten, and L. F. Tiemeijer, IEEE Electron Device Lett. **24**, 37 (2003).
[5]Y. Okawa, H. Norimatsu, H. Suto, and M. Takayanagi, IEEE Proceedings of the International Conference on Microelectronic Test Structures (ICMTS), 2003 (unpublished), p. 197.
[6]G. A. Brown, IEEE Proceedings of the International Conference on Microelectronic Test Structures (ICMTS), 2005 (unpublished), 213.
[7]L. Pantisano, J. Ramos, E. S. A. Serrano, Ph. J. Roussel, W. Sansen, and G. Groeseneken, IEEE Proceedings of the International Conference on Microelectronic Test Structures (ICMTS), 2006 (unpublished), 222.
[8]D. K. Schroder, *Semiconductor Material and Device Characterization*, 2nd ed. (Wiley, New York, 1998).
[9]K. J. Yang and C. Hu, IEEE Trans. Electron Devices **46**, 1500 (1999).
[10]H. T. Lue, C. Y. Liu, and T. Y. Tseng, IEEE Electron Device Lett. **23**, 553 (2002).
[11]W. H. Wu, B. Y. Tsui, Y. P. Huang, F. C. Hsieh, M. C. Chen, Y. T. Hou, Y. Jin, H. J. Tao, S. C. Chen, and M. S. Liang, IEEE Electron Device Lett. **27**, 399 (2006).
[12]A. Nara, N. Yasuda, H. Satake, and A. Toriumi, IEEE Trans. Semicond. Manuf. **15**, 209 (2002).
[13]Z. Luo and T. P. Ma, IEEE Electron Device Lett. **25**, 655 (2004).
[14]S. H.-M. Jen, C. C. Enz, D. R. Pehlke, M. Schroter, and B. J. Sheu, IEEE Trans. Electron Devices **46**, 2217 (1999).