國立交通大學

電機資訊學院　電子與光電學程

碩　士　論　文

具高精確度 11 位元一階連續時間 Σ - Δ 類比至數位轉換器

The Design of a high-precision 11-bit 1st -order continuous-time Sigma-Delta Analog-to-Digital Converter

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碩士論文

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摘要

本論文中,將設計與分析一個十一位元, 46.08MHz 的取樣頻率, OSR= 256,高精確度度一階連續時間互補式金屬氧化物半導體 S-? 類比/數位轉換器.為了同時達到較好的效能和高速調變的目的,本設計採用了全差動式的電路架構並運用一個消耗 2.6 mW,高速的,兩級架構的運算放大器和高速比較器以及具有 1/4 時脈的歸零數位/類比轉換器形成回授路徑的技巧來完成此設計.

經過調變後,為了同時達到平均和降頻的目的,數位平均降頻的濾波器是不可或缺的,關於這部分是利用 MATLAB 套裝軟體中的 SIMULINK 來實現.

此轉換器使用台積電 0.25μm 1P5M n-well 互補式金氧半的製程製造. 整個晶片佈局的面積是 915 x 932 μm^2.輸入電壓範圍為 1V, 2.5V 的操作電壓. 量測的結果在 44KHz 的輸入訊號且取樣頻率在 46.08MHz 的情況下,信號對雜訊及諧波比值(SNDR)為 66dB (10.67 bits)以及信號對雜訊(SNR) 比值為 66.2dB (10.7 bits).

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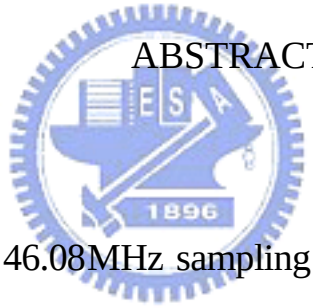


ABSTRACT

In this thesis, a 11-bit 46.08MHz sampling rate, OSR=256, high- precision first–order continuous-time CMOS sigma-delta analog-to-digital converter (ADC) is designed and analysis. In order to get better performance and high-speed modulation, using fully differential circuit architecture, including the high-speed two-stage opamp which dissipate 2.6mW, high-speed comparator and the feedback loop with 1/4 clock return-to-zero (RTZ) digital-to-analog converter (DAC) is implemented.

After the modulation, the digital decimation filter is needed to average filter function and rate reduction function simultaneously. The SIMULINK of the MATLAB implements the part of the digital decimation filter.

The ADC is fabricated with TSMC 0.25um 1P5M n-well CMOS technology. The total layout area is 915 x 932 μm^2. Input voltage range of the ADC is 1V with 2.5 V supply voltage. Measured performance includes 66dB (10.67 bits) of SNDR (Signal-to-Noise-plus-Distortion-Ratio) and 66.2dB (10.7 bits) of SNR (Signal-to-Noise-Ratio) for 44KHz input at 46.08MHz sampling rate.

誌謝

首先，要對我的指導教授吳重雨教授致上最高的敬意與謝意。沒有他，這本碩士論文不可能這麼順利完成。從碩士班一年級到現在這四年的時間裏，老師嚴謹的研究態度以及對人謙虛和善的態度，使我受益良多.此外，要感謝積體電路與系統實驗室諸多學長同學以及助理小姐的幫忙與照顧.不管是電路設計、layout、量測儀器使用，或是生活上瑣事。他們都盡心盡力的幫助我。特別要感謝廖以義學長、鄭秋宏學長、周忠昀學長、施育全學長、林俐如學姊、陳永宏學長、江政達學長、歐陽銘學長，感謝他們在電路設計,layout 以及量測上的幫助及建議。同時也要感謝公司的長官們讓我有再進修的機會。也感謝同時畢業的同學包括:謝致遠、丁彥、張秦豪、鄭建祥、鄭淑珍等人,在生活瑣事上的幫忙以及精神上的鼓勵.最後，最感謝的是我的父母以及家人，感謝他們長年以來的照顧，支持以及鼓勵，在我最失意時，給我關懷與鼓舞。

僅以此篇論文獻給所有關心我的人

CONTENTS

TABLE CAPTIONS

FIGURE CAPTIONS

SYMBOL DESCRIPTION

Σ : sigma

Δ : delta

SDM : Sigma-Delta Modulator

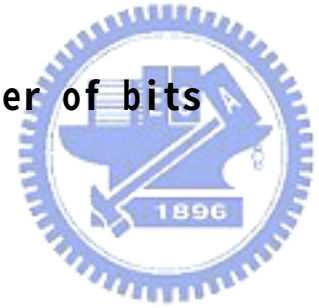
OSR : oversampling ratio

LSB : least significant bit

FFT : fast fourier transform

MIM : metal to metal

ENOB: effective number of bits



CHAPTER 1

INTRODUCTION

1.1 REVIEW

Many applications in the semiconductor industry including high quality digital audio systems and medium-to-low speed communication systems are driving the demands of 11-b high-precision ADCs. For lower cost, it is desirable to implement the ADC in a CMOS process. Moreover, a low-voltage supply is required due to technology scaling demands. Therefore, the low-power high-precision low-voltage 11-b CMOS ADCs is a major objective in the current market trend.

To achieve these requirements, the sigma-delta ADC architecture is fit to adapt. Because it has following advantages: high resolution and high dynamic range, less complexity of analog circuit design, relaxed the requirements on matching tolerances, reduced the complexity of the filter design. Many solutions have been developed such as those using current-steering [1] as shown in Fig1.1, the advantage of the structure is low power consumption but have 3 drawbacks: 1.the speed of the OTA is limited by the integrating capacitor C. 2.the linearity is decided by R1. 3. It is needed to operate 5V high voltage. And low-power high-speed structure [16] as shown in Fig1.2, have low-power and high-speed advantages. But, it has the current mirror mismatch problem as shown in Fig.1.3 and second-order sigma-delta modulator with 1/4 clock delayed return-to-zero (RTZ) feedback techniques [3] the advantage is all current-mode operation but it is needed a 26pF big capacitor for integrator constant as shown in Fig1.4. and the mismatch between Iref+ and Iref-, lead to an offset during RTZ in DAC circuit as shown in Fig1.5.

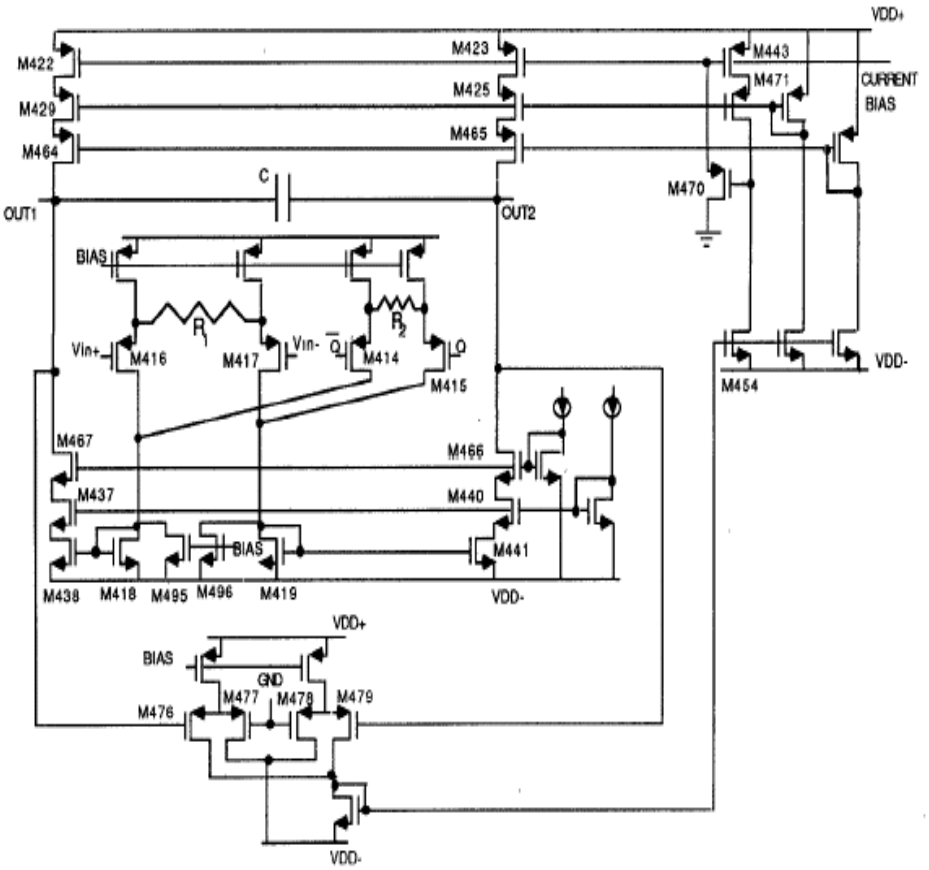


Fig.1.1 Integrator and D/A converter of [1]

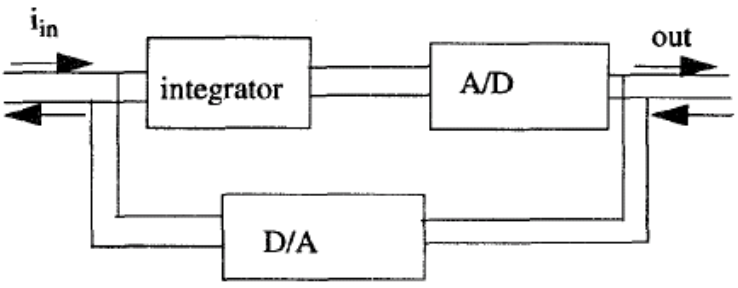


Fig1.2. System-level block diagram of the [16]

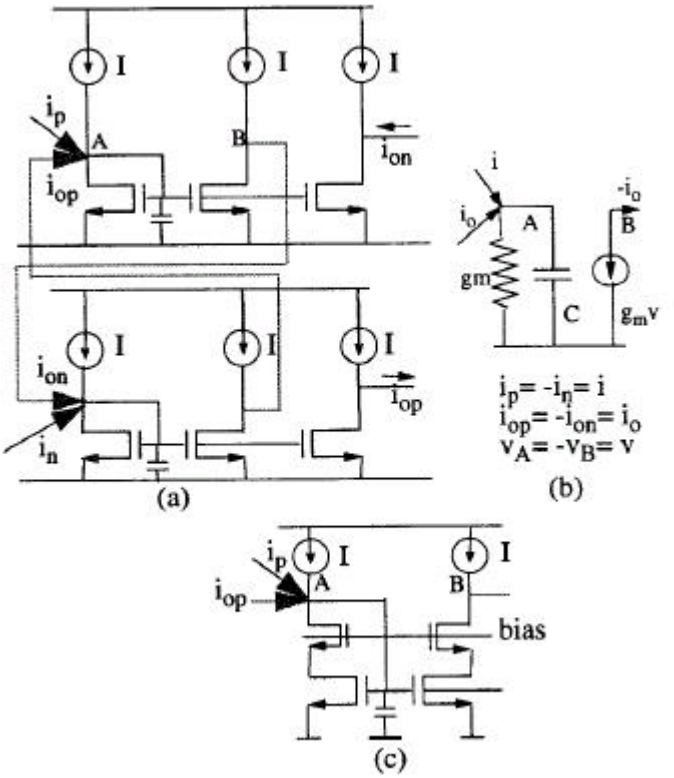


Fig1.3. The integrator of the [16]

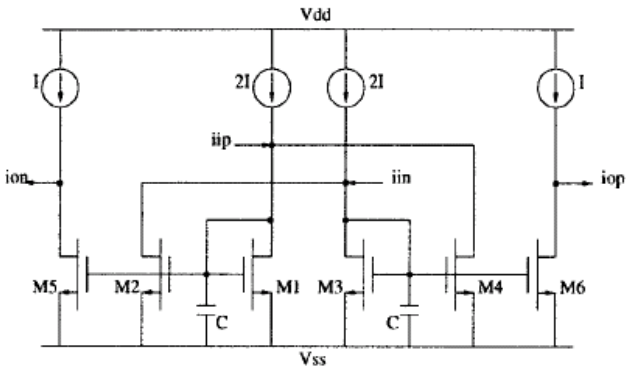


Fig1.4. A fully-balanced current-mode integrator of [3]

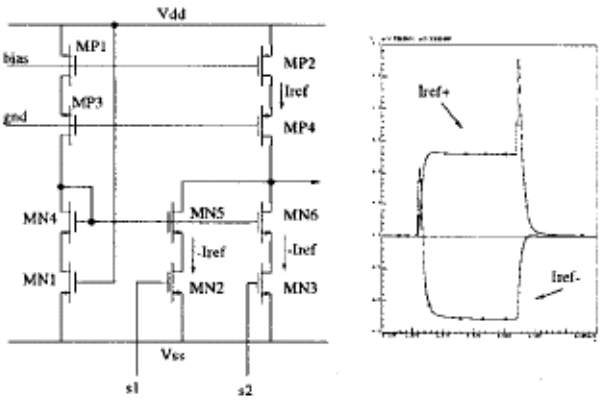


Fig1.5 Switched-current sources RTZ DAC of [3]

1.2 MOTIVATION

Currently, the popularity of continuous-time sigma-delta modulators is increasing due to some important advantages than discrete-time that. Recently, continuous-time modulators with higher sampling rate [8], low power consumption [9], and lower thermal noise [10] than discrete-time counterparts, has been reported. It is smaller glitches than discrete-time [19].

The objective of this thesis is to design a first-order 11-b high-precision ADC with power consumption under 8.34mW. The sigma-delta ADC architecture that just the simplest circuit---first-order architecture can achieve high resolution and high-precision conversion. Therefore, the sigma-delta architecture is adopted in this design. For the sigma-delta ADC architecture, the power dissipation is mainly due to the static current consumption in Gm-amp, 2-stage fully differential opamp, comparator, and DAC feedback circuit.

To design a first-order sigma-delta modulator architecture which can reach 11b resolution and high SNR with high OSR and high sampling frequency.

1.3 MAIN RESULTS

1. The total power consumption of the SDM is 8.39 mW when Vdd=Dvdd=Ovdd=2.5V.

2. The measured SNR is 62.5dB (ENOB=10.09b) when sampling frequency is 46.08MHz.

3. The measured SNDR is 62.3dB (ENOB=10.06b) when sampling frequency is 46.08MHz.

1.4 THESIS ORGANIZATION

In chapter 2, the first-order continuous-time sigma-delta ADC architecture design and operating principle is described. In chapter 3, the circuit design and software application is presented. In chapter 4, the layout descriptions, measurement setup and measurement results are presented. Finally, the conclusions and future works are given in chapter 5.

CHAPTER 2

ARCHITECTURE DESIGN AND OPERATING PRINCIPLE

A typical first-order Sigma-Delta A/D converter consists of two main building blocks, which are an analog first-order Sigma-Delta Modulator part and the digital decimation filter part that normally occupies most of the ADC chip area and consumes more power than the modulator part as shown in Fig.2.1. The former is simulated by HSPICE and the latter is simulated by MATLAB.

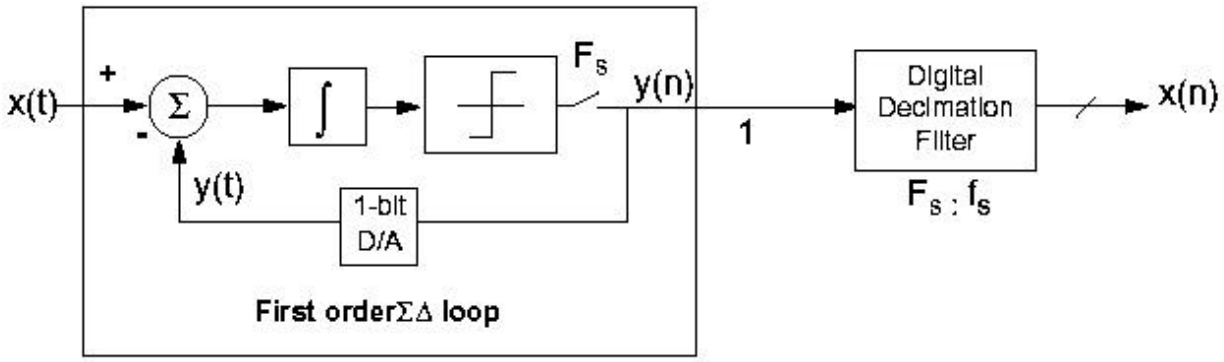


Fig.2.1. Block Diagram of First-Order Sigma-Delta ADC

2.1 FIRST-ORDER SIGMA-DELTA MODULATOR

The operation of Sigma-Delta Modulator can be explained by examining the simplest of these modulators, the first-order Sigma-Delta Modulator depicted in Fig.2.2.

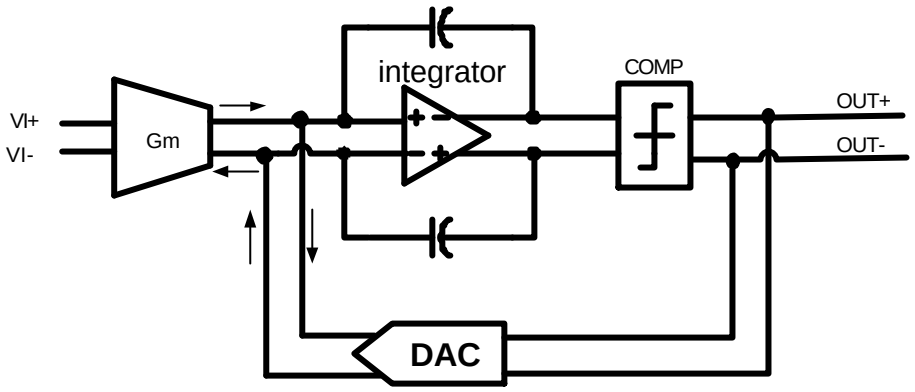


Fig.2.2 Block diagram of the first-order sigma-delta modulator

It consists of an integrator and a coarse quantizer (typically a two-level quantizer) place in the feedback loop.

When the integrator output is positive, the quantizer feedback a positive reference signal that is subtracted from the input signal, in order to move the integrator output in the negative direction. Similarly, when the integrator output is negative, the quantizer feedback a negative reference signal that is added to the input signal. The integrator therefore accumulates the difference between the input and quantized output signals and tries to maintain the integrator output around zero. A zero integrator output implies that the difference between the input signal and the quantized output is zero. The feedback around the integrator and quantizer forces the local average of quantizer output to track the local average value of

the input signal. The key point technology of the oversampling is quantization noise, noise shaping and decimation.

2.1.1 QUANTIZATION NOISE

The quantization noise power and Signal to Noise Ratio (SNR) of the oversampling are

$$SNR = 6.02b + 1.76 + 10\log OSR(dB) \quad \textbf{(1)}$$

$$OSR = \frac{f_S}{2 f_b} \quad \textbf{(2)}$$

b is the resolution of the ADC, OSR is oversampling ratio, fs is Sampling frequency, fb is signal bandwidth the **equation (1)** increases the 10logOSR term than Nyquist rate.
If the OSR increasing result in the power of the noise is decreasing then the SNR is increasing.

2.1.2 NOISE SHAPING

The SNR value after noise shaping is in Equation **(3)**. If the OSR double increasing 9dB in SNR and the resolution is increased 1.5bit.

$$SNR = 6.02b + 1.76 - 5.17 + 30\log(OSR)(dB) \quad \textbf{(3)}$$

2.2 DIGITAL DECIMATION FILTER

Filtering noise, which could be aliased back into the baseband, is the primary purpose of the digital filtering stage. Its secondary purpose is to take the 1-bit data stream that has a high sample rate and transforms it into an n-bit (n>>1) data stream at a lower sample rate. This process is known as decimation. Essentially, decimation is both an averaging filter function and a rate reduction function performed simultaneously.

Three basic tasks are performed in the digital filter sections:

1. Remove shaped quantization noise: The Sigma-Delta modulator is designed to suppress quantization noise in the baseband. Reducing the baseband quantization noise is equivalent to increasing the effective resolution of the digital output. The most of the quantization noise is at frequencies above the baseband. The main objective of the digital filter is to remove this out-of-band quantization noise.
2. Decimation (sample rate reduction): The output of the Sigma-Delta modulator is at a very high sampling rate. After the high frequency quantization noise is filtered out, it is desirable to bring the sampling rate down to the Nyquist rate, which minimizes the amount of information for subsequent transmission, storage, or digital signal processing.
3. Anti-aliasing: When the digital processor reduces the sampling rate down to the Nyquist rate, it needs to provide the necessary additional aliasing rejection for the input signal as

opposed to the internally generated quantization noise.

The simplest and most economical filter to reduce the input sampling rate is a "Comb-Filter", because such a filter does not require a multiplier. The remaining filtering is performed in three stages using half-band filters, which implement 2:1 decimation and have linear phase characteristic.

Because of the entirely different quantization process of Sigma-Delta ADCs, performances of theses ADCs can't be described in terms of integral and differential nonlinearity as in the case of Nyquist rate ADCs. Instead, performance measures such as signal-to-noise ratio (SNR) can be used to evaluate the effective number of bits (ENOB).

$$DR^2 = \frac{\left(\frac{LSB}{2\sqrt{2}}\right)^2}{\left(\frac{p^{2L}}{2L+1}\right)\left(\frac{1}{OSR^{2L+1}}\right)\left(\frac{LSB^2}{12}\right)} = \frac{3}{2}\frac{2L+1}{p^{2L}}OSR^{2L+1} \qquad \textbf{(4)[11]}$$

$$DR^2 = 3\times 2^{2B-1} \qquad \textbf{(5)}$$

DR is dynamic range; L is bit number of the quantizer, in the thesis is one. And the dynamic range of a B-bit Nyquist rate ADC is

How to trade-off the order number as shown in follow:

1. To decide the in-band frequency fb.
2. To decide the resolution of the ADC, the DR^2 can be calculated by equation **(5)** .
3. And from equation **(4)** if L (order)=1,can calculate OSR, then the fs is known.

4. If the higher fs is needed, the circuit is difficult to implement, can try L (order)=2, then the lower fs is got, the circuit is easier to implement.

In the thesis, OSR=256, from equation **(4) (5)** can obtain B is 11.1b resolution, DR(dB) =68.6dB**.**

CHAPTER 3

CIRCUIT IMPLEMENTATION

3.1 ANALOG CIRCUIT REALIZATION

The analog circuit of the first-order sigma-delta modulator is made up of fully differential Gm Amplifier, Integrator and 2-level Quantizer, is shown in Fig.3.1. Fully differential circuits achieve better power supply rejection and common mode noise rejection.

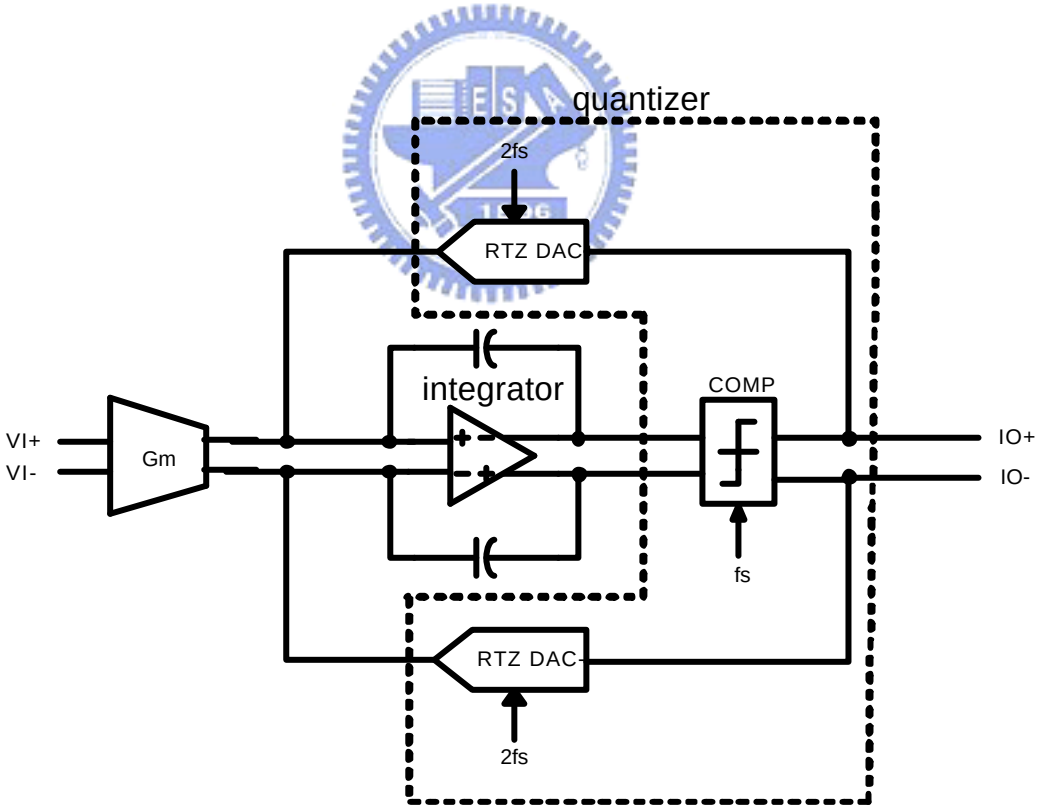


Fig.3.1. First-order sigma-delta modulator architecture

3.1.1 GM AMPLIFIER

In order to operating in high-speed operation the current-steering [1] and current-mode with 1/4 clock delayed 2-level return-to-zero (RTZ) feedback techniques [3] is adapted. Firstly, in order to designing a linear Gm amp is to use a triode-region transistor as shown in Fig.3.2 [4]. The cascade and gain boost structure provides large output impedance and high-swing cascade-current-source load to the Gm amp. The output cross-coupling connection reduces the common-mode gain of the Gm amplifier. Fig.3.3. show the circuit of the opamp used in the Gm amp, has 78 dB open loop gain and 114 MHz bandwidth [11]. The current of the triode-region transistor is shown in equation **(6)**. And the transconductance of the Gm amp is shown in equation **(7)**.

$$I_D = \mu_n C_{ox} \frac{W}{L}(V_{gs} - V_t)V_{ds} \quad \textbf{(6)}$$

$$g_m = \frac{\partial I_D}{\partial V_{gs}} = \mu_n C_{ox} \frac{W}{L} V_{ds} \quad \textbf{(7)}$$

Where μ_n is mobility of n-channel MOS, Cox is oxide capacitance, the g_m value is proportional to Vds.

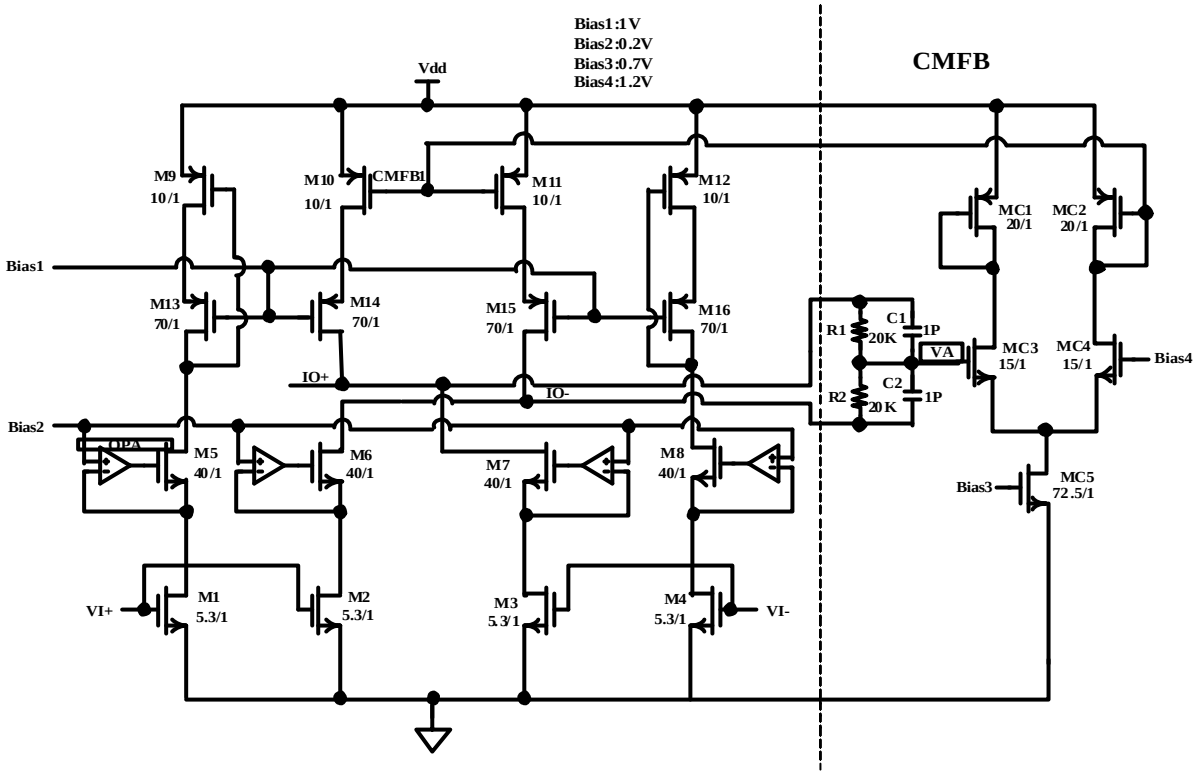


Fig.3.2. Fully differential triode-region Gm amp [4] [5]

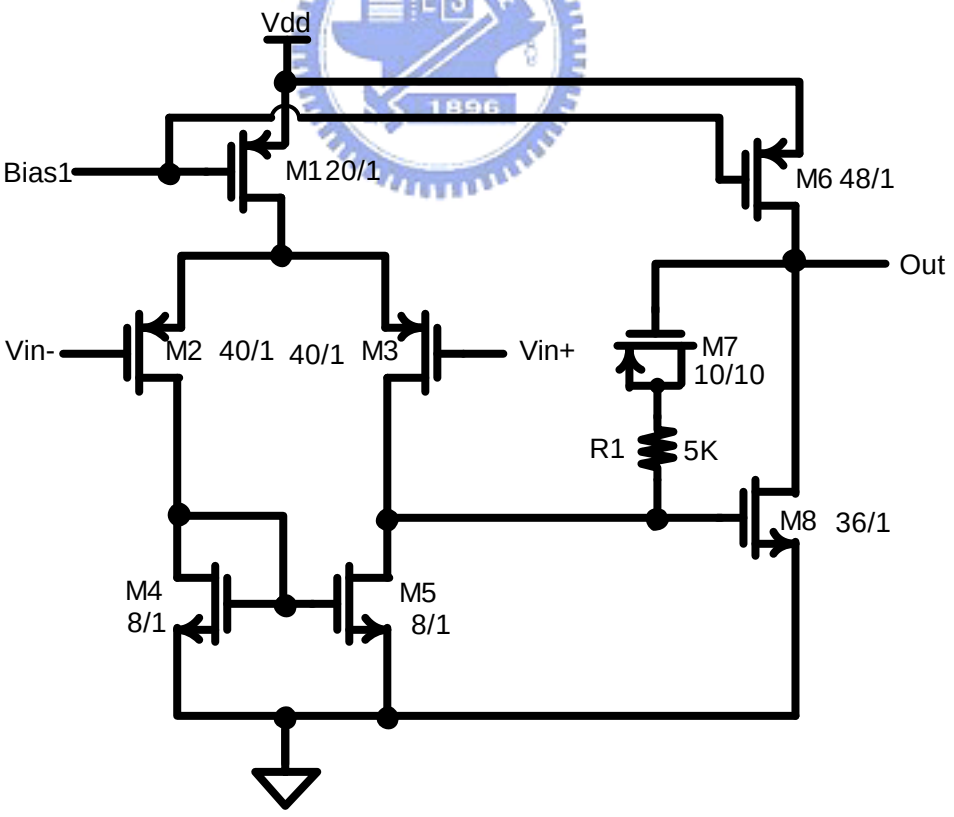


Fig.3.3. Opamp circuit used in the Gm amp

The opamp show in Fig.3.3 serves two functions. Firstly, it is used to control the Vds of the transistor (M1, M2, M3, M4) to be equal to bias2, so that the gm can be proportional to a constant voltage bias2. The reference voltage bias2 should smaller than (Vgs-Vt) of M1, M2, M3, M4 in order to enforce the transistor to operate in the triode-region. Secondly, it is used to enhance the output impedance of the Gm amp. The gain of the opamp should be reasonable large, so that the Vds of the triode-region transistor can follow the control bias2 as close as possible.

To create a negative feedback path is only for common-mode signals. For differential signals, CMFB has no effect on circuit performance.

An alternative approach for realizing common-mode feedback circuit is shown in Fig.3.4 [4] [7]. C1, C2 is compensation capacitor, to stable the differential loop. It is used in the Gm amp. This circuit generates common-mode voltage of the output signals at node VA. This voltage is compared to bias2 using a separate amplifier. The voltage at node CMFB1 is feedback to the Gm amp so that the common-mode voltage of the Gm amp output is the same. The voltage of the VA and Bias4 needed to satisfy the following equation:

$$Bias4 = VA = \frac{IO_+ + IO_-}{2} \qquad \textbf{(8)}$$

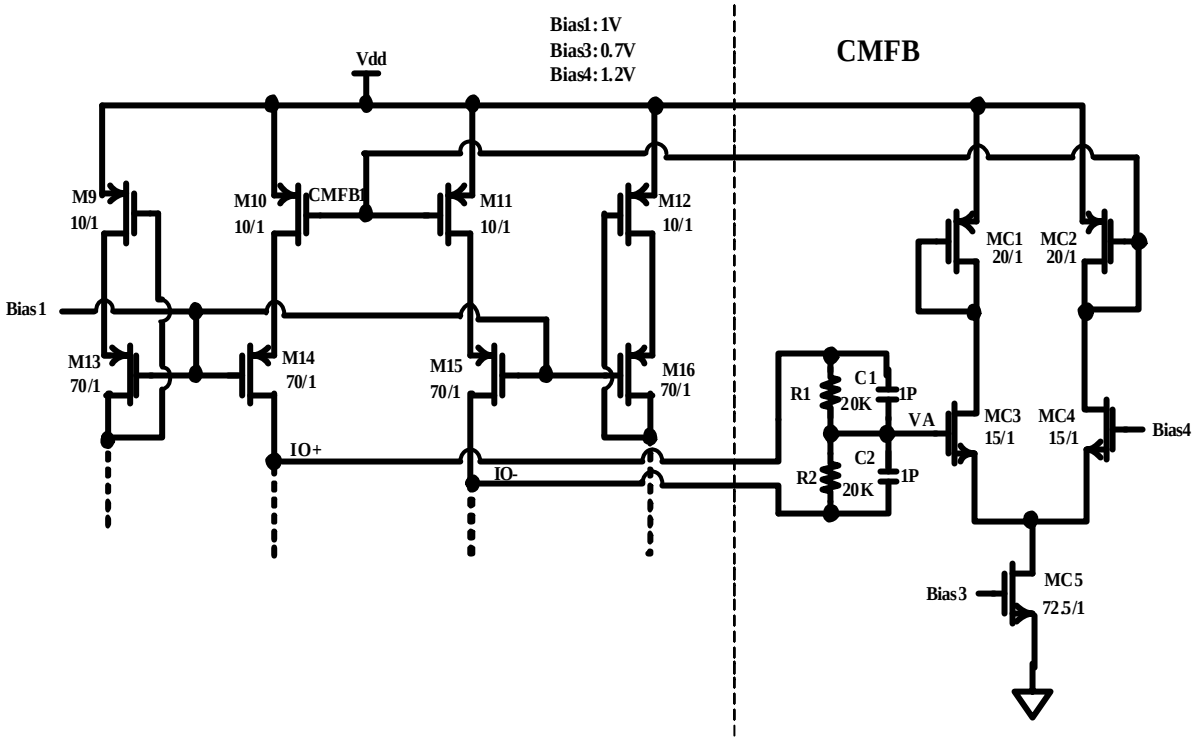


Fig.3.4. Common-mode feedback circuit used in the Gm amp [4] [7]

The first transconductor in the continuous-time SDM is most important for overall thermal noise and linearity. A mismatch in the input differential pair transistors leads to an offset which results in a dc term in the output spectrum; where dc is not removed by the decimation.

3.1.2 INTEGRATOR

An overall circuit of the integrator is shown in Fig.3.5. It is made up of fully differential opamp and common-mode feedback circuit.

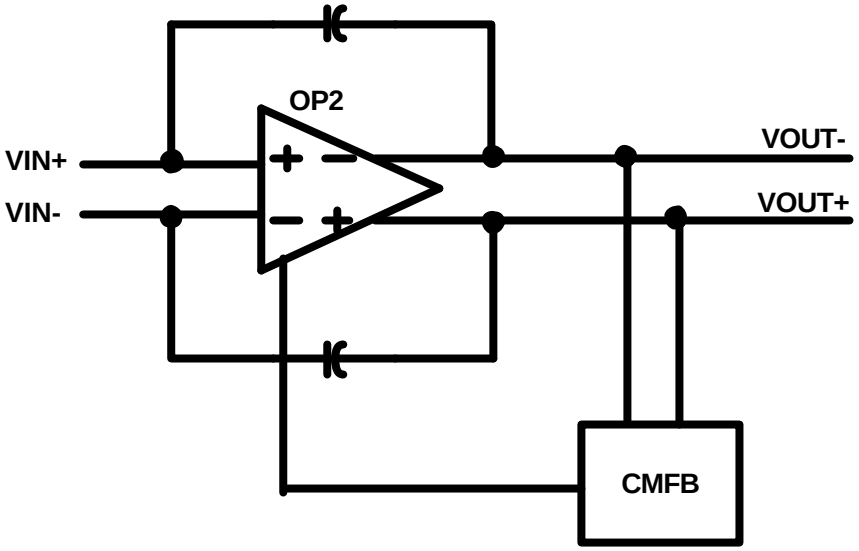


Fig.3.5. Integrator architecture

In order to operating in high-speed and obtaining noise-shaping benefit the opamp gain and bandwidth need to consider.

Finite op-amp gain causes the inverting op-amp terminal to reflect the output voltage rather than behave as a virtual ground. Not all of the charge will be transferred to the integrating capacitor, resulting in a "leaky" integration.

The output of the SDM, v(kT), is the sum of the previous output, v(kT-T), and the previous input, u(kT-T):

$$v(kT) = g_0 u(kT-T) + v(kT-T) \quad \textbf{(9)}$$

The constant $g_0$represents the gain preceding the input to the integrator. The above equation corresponds to the following transfer function for an ideal integrator:

$$H(z) = \frac{g_0 z^{-1}}{1-z^{-1}} \quad \textbf{(10)}$$

The dc gain of the ideal integrator is infinite. In practice, the gain is limited by

P_0

circuit constraints. The consequence of this "integrator leak" is that only a fraction of of the previous output of the integrator is added to each new input sample.

$$H(z) = \frac{g_0 z^{-1}}{1 - P_0 z^{-1}} \quad \textbf{(11)}$$

And the dc gain is $H_0(z) = \frac{g_0}{1 - P_0}$. The limited gain at low frequency reduces the attenuation of the quantization noise in the baseband, results in an increase of the in-band quantization noise S_B that is given by

$$\frac{\Delta S_B}{S_B} = \frac{5}{p^4}\left(\frac{M}{H_0}\right)^4 + \frac{10}{3p^2}\left(\frac{M}{H_0}\right)^2 \quad \textbf{(12)}$$

M is oversampling ratio, the performance penalty incurred is on the order of 1dB when the integrator dc gain is comparable to the oversampling ratio as shown in Fig.3.6.

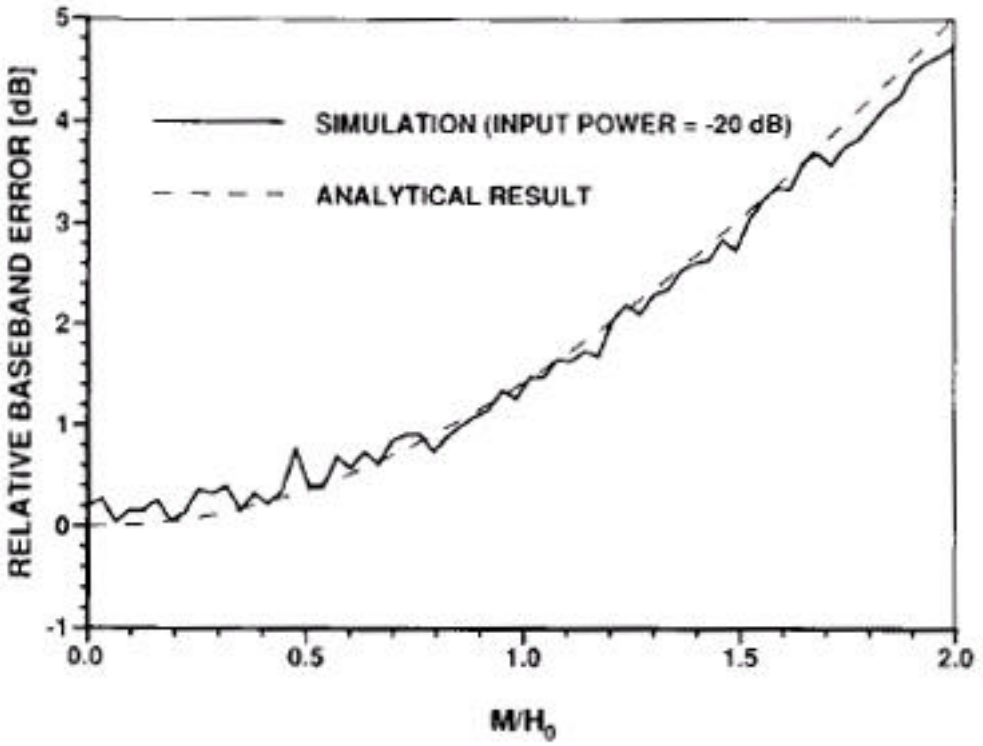


Fig.3.6. Influence of integrator leak on baseband quantization noise

Infinite a good rule of thumb, which applies to continuous-time SDM, is that the

integrators should have

$$A > OSR \qquad \textbf{(13)}\ [20]$$

Normally, the designers will typically ensure that the opamp gain is at least oversampling ratio, If this holds, the SNR will be only about 1dB worse than if the integrators had infinite gain. In the thesis the OSR=256, then the opamp DC gain is about 48dB.

For an amplifier with a single dominant pole and unity-gain frequency fu, the impulse response of the integrator output during sampling will be exponential with a time constant [22],[23]

$$t = \frac{1}{2pf_u} \qquad \textbf{(14)}$$

$t \le T$ must be met in order to guarantee stability of the modulator. This requirement corresponds to a lower limit for fu of

$$f_u \ge \frac{1}{pT} = \frac{f_s}{p} \qquad \textbf{(15)}$$

The fact that only one-half of the clock period T is available for the integration. And the opamp bandwidth could be as low as fs, the sampling frequency, give negligible performance loss [20].

The simulation results indicate a sharp increase in both quantization noise and harmonic distortion of the converter when the slew rate is less than $1.1\Delta/T$ as shown in Fig3.7. Δ is the difference between adjacent quantizer output levels. These simulations are based on the assumption that if the integrator response is not slew-rate limited, the impulse

response is exponential with time constant τ :

$$v(kT+t)=\frac{g_0}{1-e^{-T/t}}u(kT)[1-e^{t/t}]+v(kT) \qquad \textbf{(16)}$$

the term $1-e^{-T/t}$ has been included to separate the effects of finite slew rate from those due to variation in the equivalent gain. The peak rate of change in the impulse response occurs at t=0 and is given by

$$\frac{dv(kT+t)}{dt}=\frac{g_0}{1-e^{-T/t}}\frac{u(kT)}{t} \qquad \textbf{(17)}$$

Slewing distortion occurs when this rate exceeds the maximum slew rate the integrator can support [20].

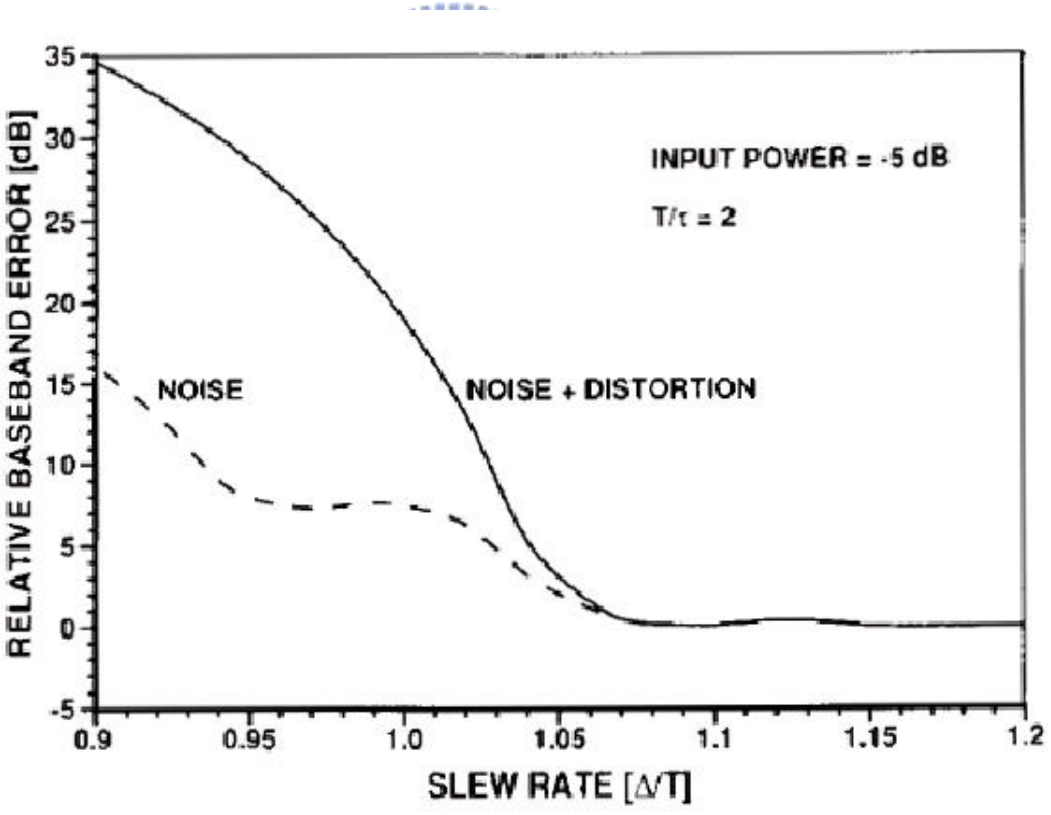


Fig.3.7. Simulated influence of integrator output slew rate on baseband quantization noise[20]

The Settling time of the opamp has 0.01% accuracy that is about 13.2b resolution accuracy. In the thesis, the accuracy is 0.04% needed. So the specification is met.

Fig.3.8 show the only one stage amplifier op-amp circuit, the open-loop gain is 26.4dB, bandwidth is 42MHz as shown in Fig.3.9, phase margin, gain margin is limited by R1 ,R2,C1,C2 in common-mode feedback circuit.

To achieve the specification requirement, the two stages structure is needed.

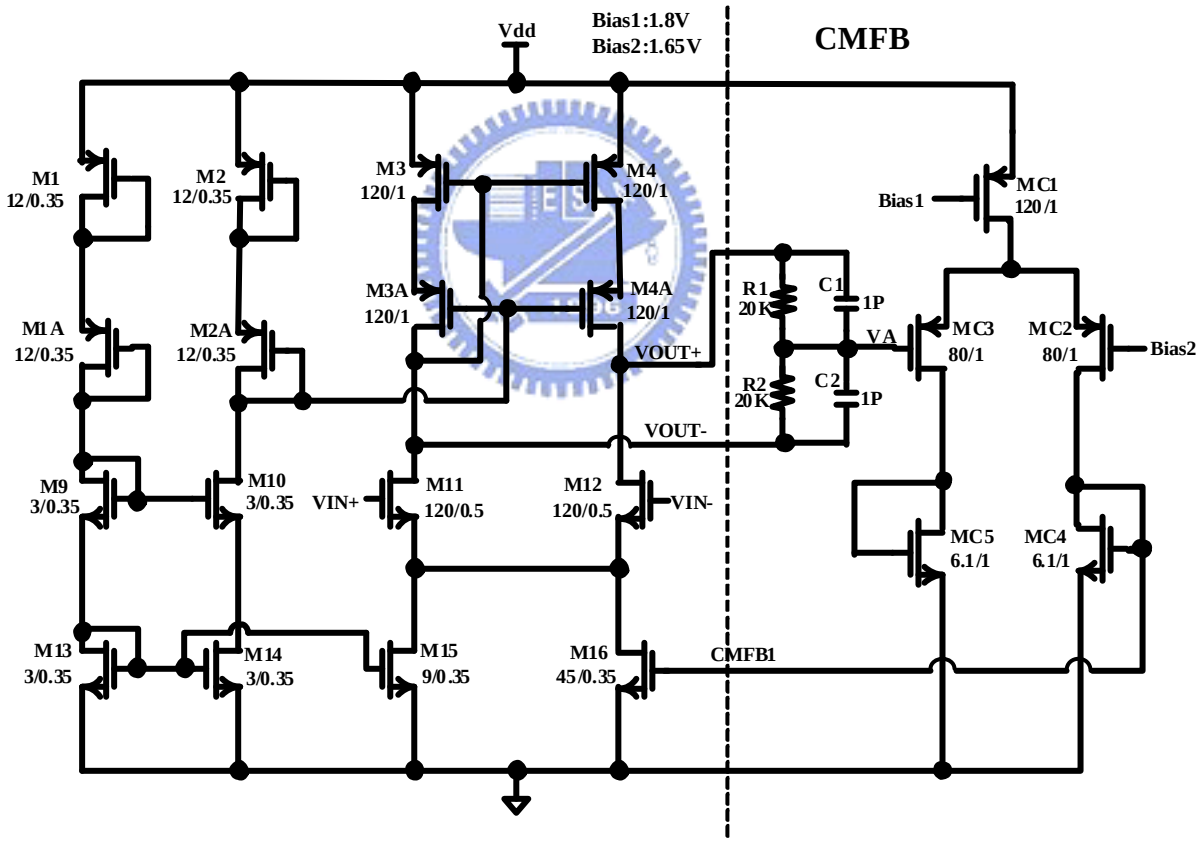


Fig.3.8. Fully differential opamp circuit only one stage amplifier

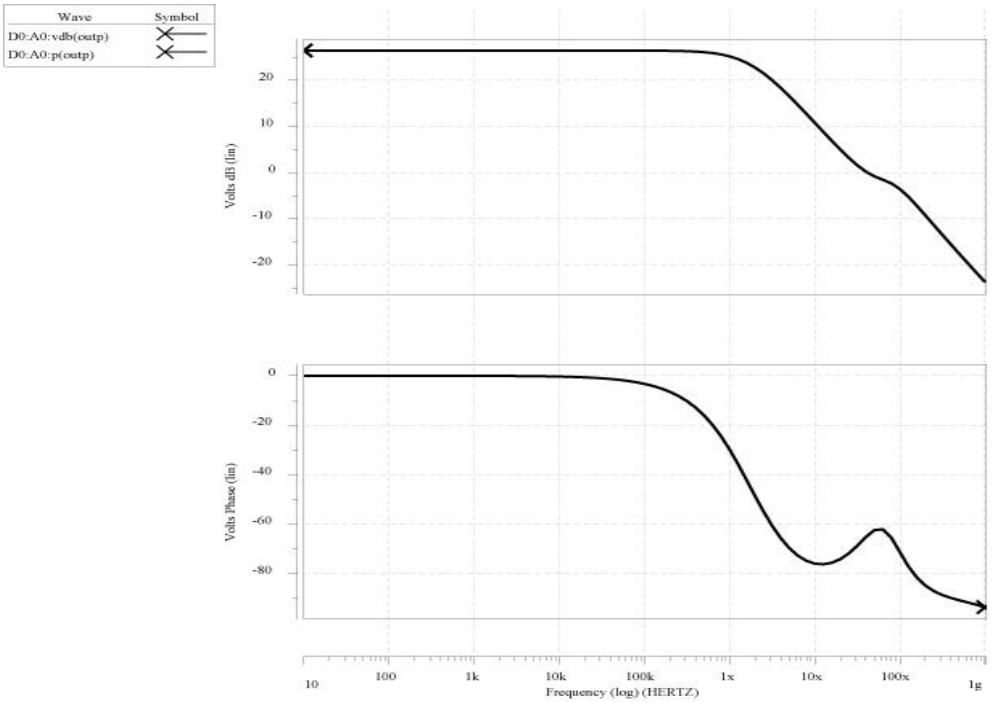


Fig.3.9. Only one stage opamp, the open-loop gain is 26.4dB, bandwidth is 42MHz

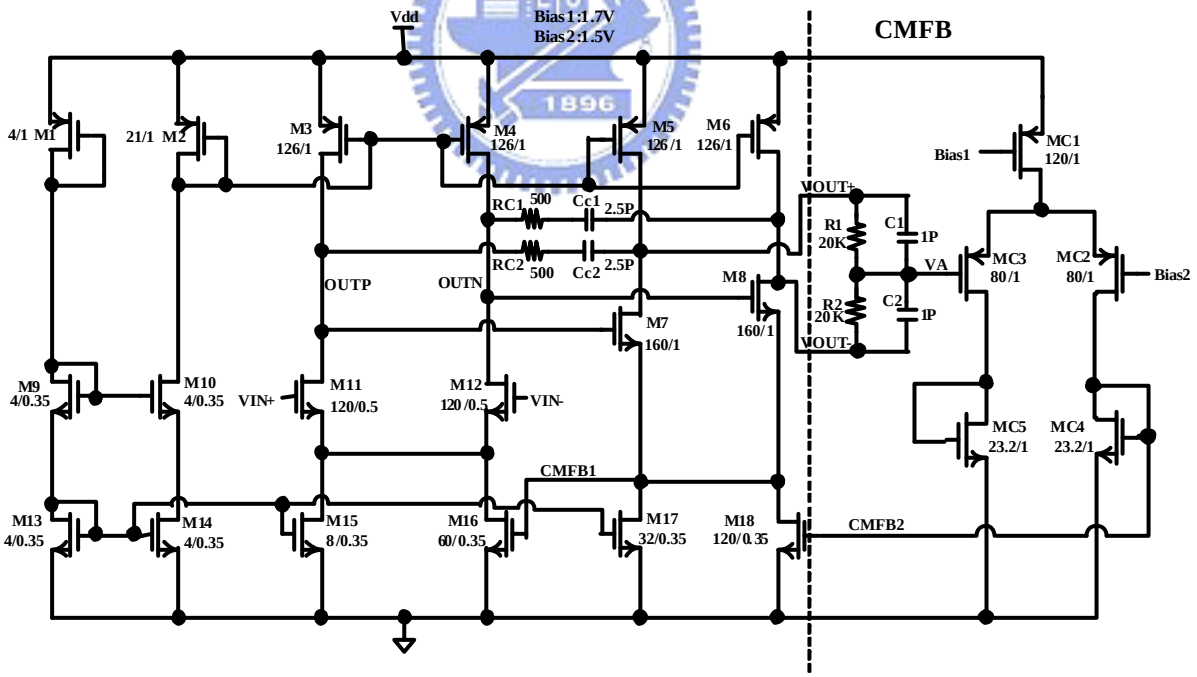


Fig.3.10. Fully differential opamp circuit used in integrator

The fully differential opamp, which has two-cascade-stage topology compensated by a series RC network, is shown in Fig.3.10. The dominant pole is located at the output of first

stage, and the second pole is located at the output of second stage as follows:

$$w_{p1} = \frac{1}{g_{m7}(r_{o7,8} // r_{o5,6}) \cdot (r_{o11,12} // r_{o3,4}) \cdot C_C} \quad \textbf{(18)}$$

$$w_{p2} = \frac{g_{m7}}{C_L} \quad \textbf{(19)}$$

The open-loop dc gain (A_v), the unity gain bandwidth (? $_u$) and the slew-rate are as follow,

$$A_V = g_{m11}(r_{o11} // r_{03}) g_{m7}(r_{o7} // r_{o5}) \approx g_m{}^2 r_o{}^2 \quad \textbf{(20)}$$

$$w_u = \frac{g_{m11,12}}{C_C} \quad \textbf{(21)}$$

$$SR = \min\left(\frac{I_{d15} + I_{d16}}{C_C}, \frac{I_{d17} + I_{d18}}{C_L}\right) \quad \textbf{(22)}$$

The second-pole is moved to higher frequency. Therefore the bandwidth of this opamp is increased and there is no other non-dominant pole to limit the bandwidth. Moreover, only a dominant pole and second pole exist in the signal path, the frequency compensation is easy to design and achieve. Also, the simple second-stage topology allows large output signal swings of 1.4V peak-to-peak differential from a 2.5V supply voltage without linearity degradation.

Though, the open-loop dc gain is about $g_m{}^2 r_o{}^2$. Only 48dB of open-loop dc gain is required for 11b resolution. From above analysis, therefore, the open-loop dc gain and reducing flicker noise can be achieved easily by using the long channel of MOS (M3~M6) and the larger parasitic capacitance combined to the dominant pole does not limit the bandwidth. Another drawback of the opamp is the common mode feedback circuits are

required on each stage.

Typically, when using fully differential opamps in a feedback application, the applied feedback determines the differential signal output voltages, but the output common mode voltages are not well-defined. It is necessary to add additional circuit to keep the output common mode voltage of opamp constant and to control it to be equal to some specified voltage. The additional circuit is referred to as the common-mode feedback circuit (CMFB).

The fully differential opamp, the output common-mode voltages of both stages are undefined. Therefore, the opamp uses two CMFB circuits, one for each stage. For the first-stage of the opamp, the CMFB circuit is done by simply connecting the node (CMFB1 node) at the drain of M17 and M18 to the gate of M16 as shown in Fig.3.10. The voltage on node CMFB1 is

$$V_{CMFB1} = \frac{OUTP + OUTN}{2} - \frac{V_{gs8} + V_{gs7}}{2} \qquad \textbf{(23)}$$

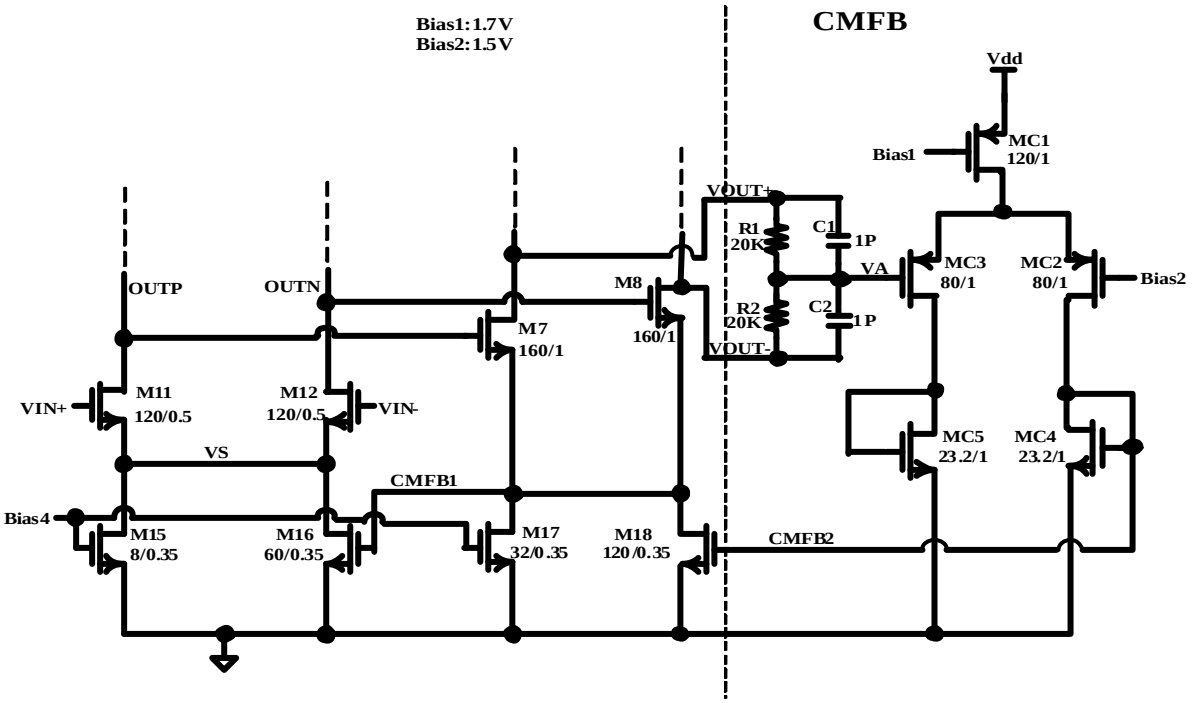


Fig.3.11. Common-mode feedback circuit used in integrator [4] [7]

where if the current in the second-stage of opamp is fixed, the voltage on node CMFB1 can sense the output common-mode voltage of first-stage of this opamp. When the common-mode voltage of V_{outp}, V_{outn} is too high so does the voltage on node CMFB1. By connecting the node CMFB1 to gate of M16, the gate voltage of M16 goes up and then decreases the common-mode voltage back to the desired output common-mode voltage (V_{ocm1}). The desired output common-mode voltage is ($V_{gs7,8}+V_{gs16}$).

For the second-stage of opamp, An alternative approach for realizing common-mode feedback circuit is shown in Fig.3.11 [4] [7]. This circuit generates common-mode voltage of the output signals at node VA. This voltage is compared to bias2 using a separate amplifier. The voltage at node CMFB2 is connected to gate of M18 of the fully differential opamp so that the common-mode voltage of the fully differential opamp output is the fixed. The voltage of the VA and Bias2 needed to satisfy the following equation:

$$Bias2 = VA = \frac{(VOUT+) + (VOUT-)}{2} \quad \textbf{(24)}$$

To ensure common-mode stability, the NMOS current sources (M15,M16) and (M17,M18) are split into two, the reduced g_m increases the phase margin of the CMFB loop and improves the common-mode stability.

The voltage of CMFB1 is 0.609V, CMFB2 is 0.643V. The current of the M15 is

45uA , M16 is 236uA, M17 is 184uA, M18 is 740uA. The current source is dominated by M16 and M18.

Table I. The fully differential opamp characteristic

VDD	**2.5V**
Open-loop gain	**74.5dB**
fu@6pF load	**110MHz**
Phase margin	**54 degree**
Gain margin	**35dB**
Slew rate	**17.5V/us**
Settling time	**29.3ns**
CMRR@44KHz	**131.2dB**
Input common-mode range	**0.7~2V**
Output swing	**1.4V**

3.1.3 QUANTIZER

In sigma-delta modulators, the comparator is required to work at high oversampling frequency but its resolution can be as small as 1-bit. Therefore, the comparator design in sigma-delta modulators focuses more on a high-speed operation instead of accuracy.

3.1.3.1 COMPARATOR DESIGN

To combine the sample-and-hold function and the comparator function in a quantizer, the latch-type comparator is adapted. Another reason is it operates in high-speed .The schematic of the latch-type comparator is shown in Fig.3.12. The operation of the comparator is described as follows:

During the pre-charge phase, i.e. when latch goes low, transistors M5 and M6 are turn off and the comparator does not respond to any input signal. The voltages Voc+ and Voc- will be pulled to Vdd, and the output of the inverters will be pulled to ground. At the same time, M1 and M4 discharge the voltages Vf+ and Vf- to ground.

During the evaluation phase, i.e. when latch goes high, both the voltages Voc+ and Voc- drop from Vdd and both the voltages Vf+ and Vf- rise from ground initially. If the voltage at Vi+ is higher than that at Vi-, M1 draws more current than M4. Thus, Voc+ drops faster than Voc- and Vf- rises faster than Vf+. As Voc+ drops to Vdd-Vtp, M9 turns on and charge Voc- to high level while Voc+ keeps going to ground. Also, as Vf- rises to Vtn, M2 turns on and discharge Vf+ to ground while Vf- keeps rising to Vdd.

The regenerative action of M8 and M9 together with that of M2 and M3 pulls Voc+ to ground and pulls Voc- to Vdd. Hence, following the inverters M11-M14, Vo+ is pulled to Vdd and Vo- is pulled to ground. The operation for the case when the voltage at Vi- is higher than that at Vi+ is similar.

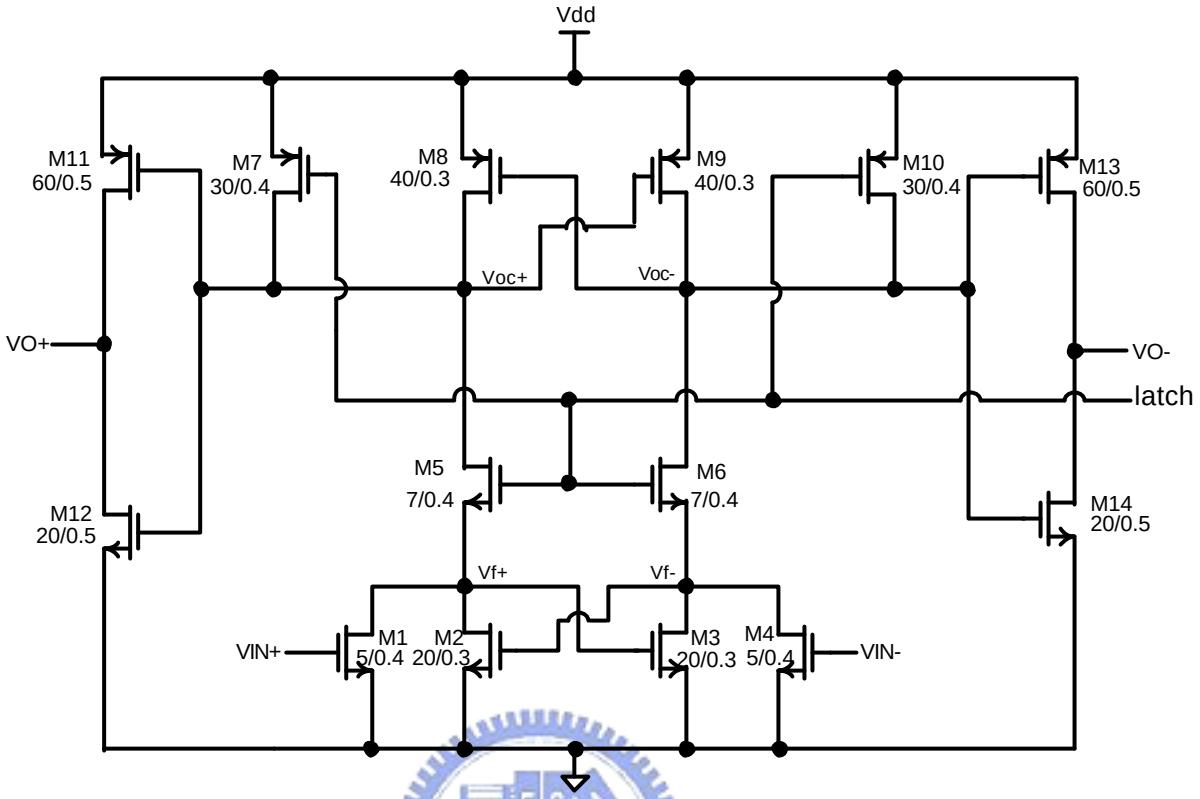


Fig.3.12. Latch-type comparator [5]

The digital circuit generating the DAC controls signals with high-crossing and low-crossing points, as shown in Fig.3.13, waveform is shown in Fig.3.14. In order to reduce the clock jitter on the control signals, the inverters driving the DAC switches are supplied from the analog Vdd. Fs is generated by 2Fs signal through the divided 2 circuit. The DAC control signals (RZP. RZN.P-.N+.P+.N-) with ¼duty RTZ are generated by 2Fs.

To reach the high-speed operation and 1/4 latch cycle RTZ, the dummy loop is made up by M2, M5, M8, M11. The signals controlling the NMOS switches (RZN, N+, and N-) have a high crossing point. In the same way, the PMOS switches control signals (RZP, P+ and P-) have a low crossing point. The DAC circuit is illustrated in Fig.3.15.

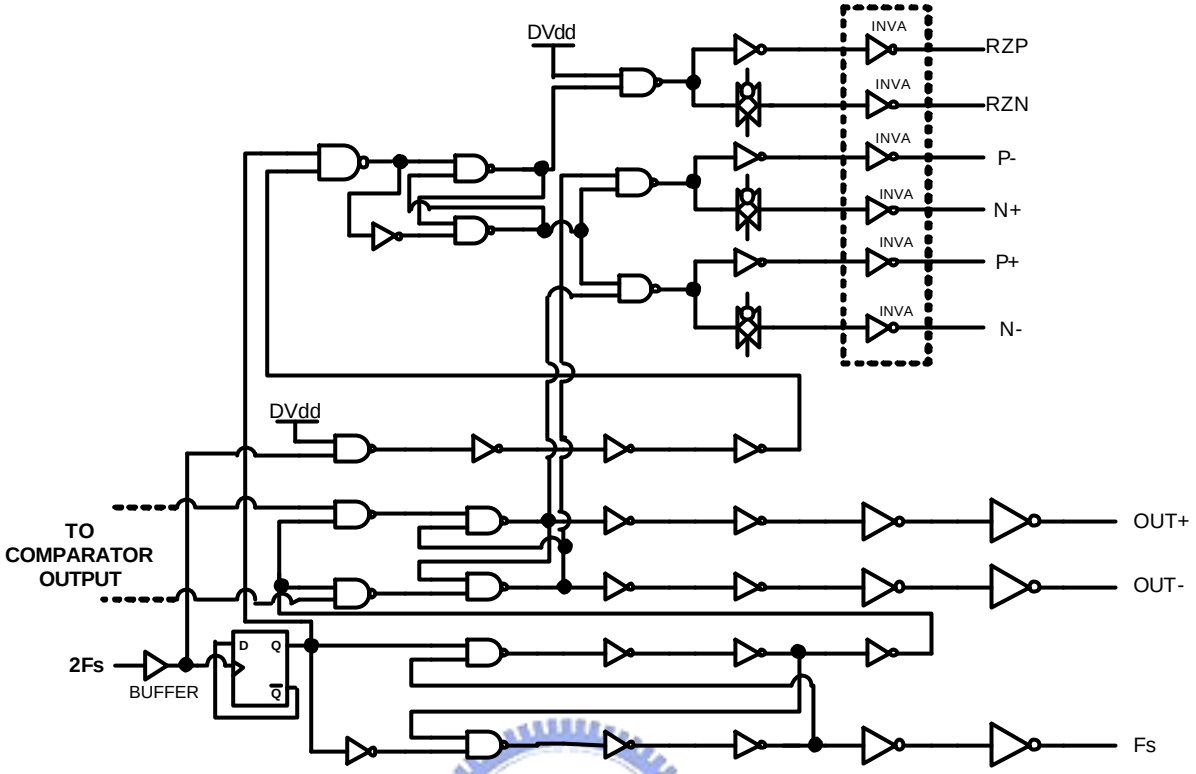


Fig.3.13. DAC control circuit [6]

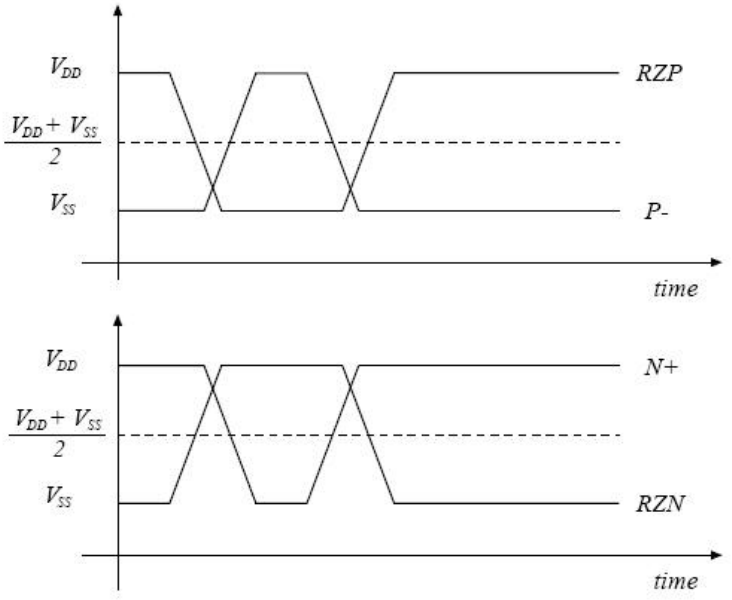


Fig.3.14. Timing diagram of high-crossing NMOS-switch control signals and low-crossing PMOS-switch control signals [6].

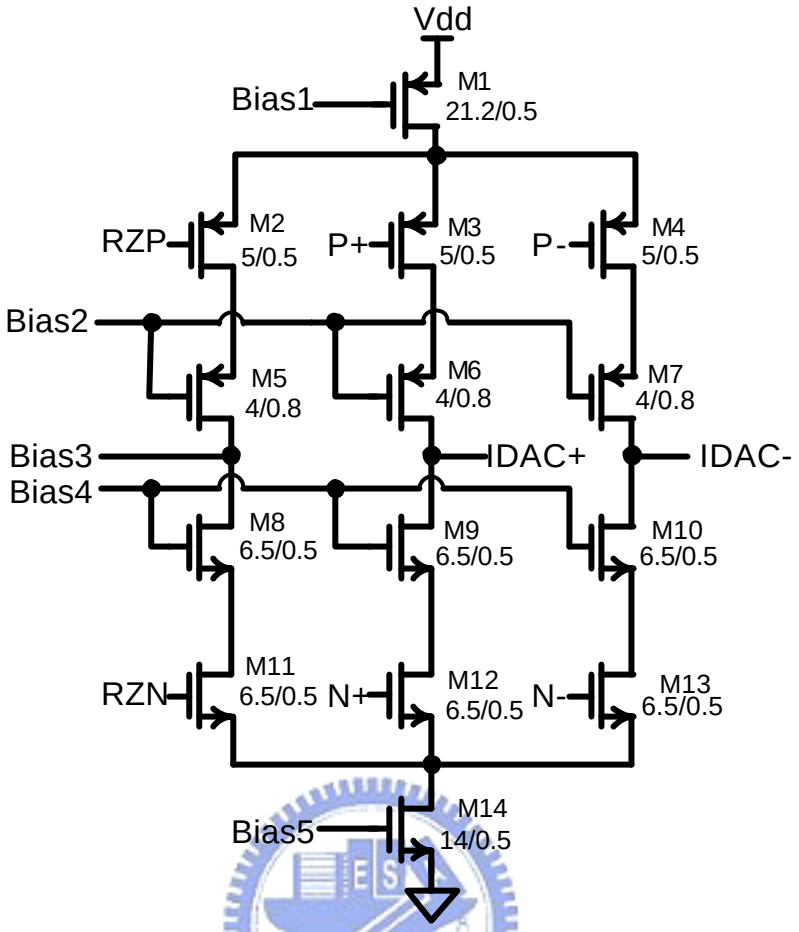


Fig.3.15. DAC circuit [6]

The mismatch of Iref+ and Iref- can result in lower Performance as shown in

Fig.3.16. The layout is needed to consider between Iref+ and Iref- relative mismatch.

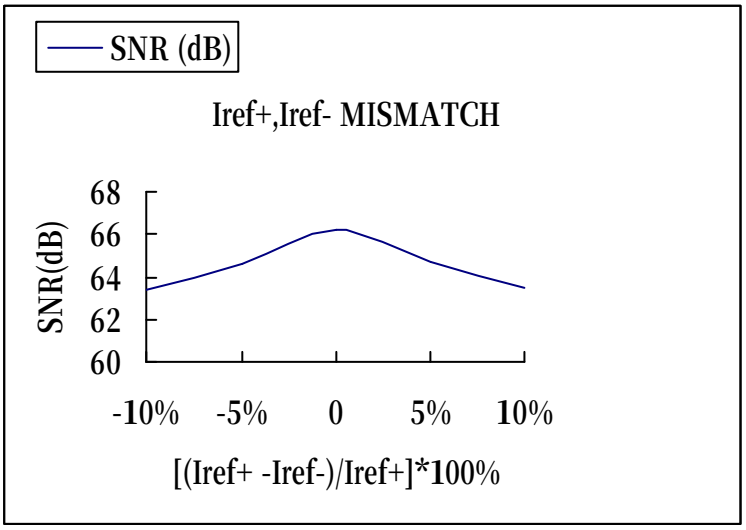


Fig.3.16. The effect of Iref+ and Iref- mismatch

3.1.3.2 RETURN-TO-ZERO (RTZ) FEEDBACK DAC CIRCUIT

When the RTZ is larger than 55%, it can reduce the performance in the thesis as shown in Fig.3.17. The RTZ time is needed to larger than loop delay, but cannot too long. Otherwise, it can affect the modulation result.

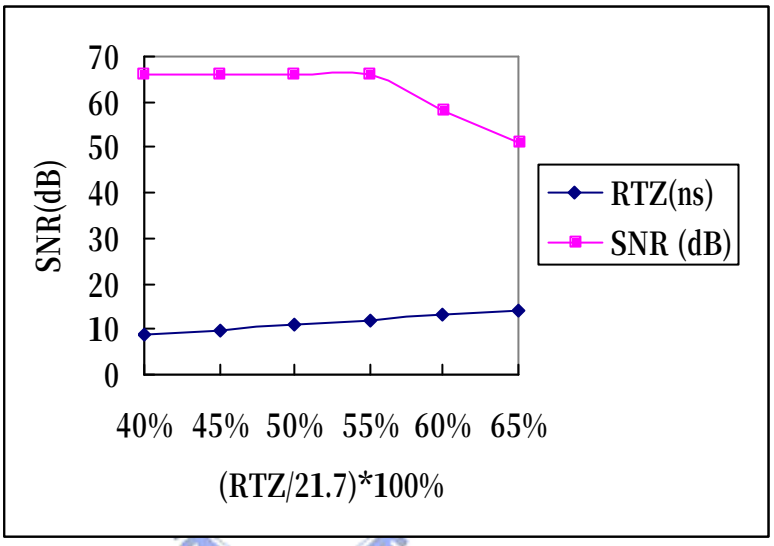


Fig.3.17. The effect of RTZ duty

An external clock frequency equal to twice the sampling frequency is required in order to get a T/4 RTZ phase at the beginning of each cycle as shown in Fig.3.18. The output current is directed either to IDAC+ or IDAC- depending on the comparator output DATA.

During RTZ phase, the positive and negative current sources are connected together through the Bias3 node. IDAC+ and IDAC- are voltage-control-current-source, P+=P-=Vdd, N+=N-=0, its current is zero Amp. It has no offset occurred during the return-to-zero (RTZ) interval.

In addition to reducing errors due to comparator delay and DAC output waveform asymmetry.

The purpose of cascading the switch transistor is to:

1. Reduce the capacitance seen by the output node (the input of the integrator and the output of the Gm amp). This reduces error current due to charging of the drain of the current source transistor to the potential of the output node.
2. Prevent any voltage variations at the output from reaching the drain of the current source transistor.
3. Increase the output resistance of the current source.
4. Prevent glitches that occur during switching from reaching the output through of the switch transistor.

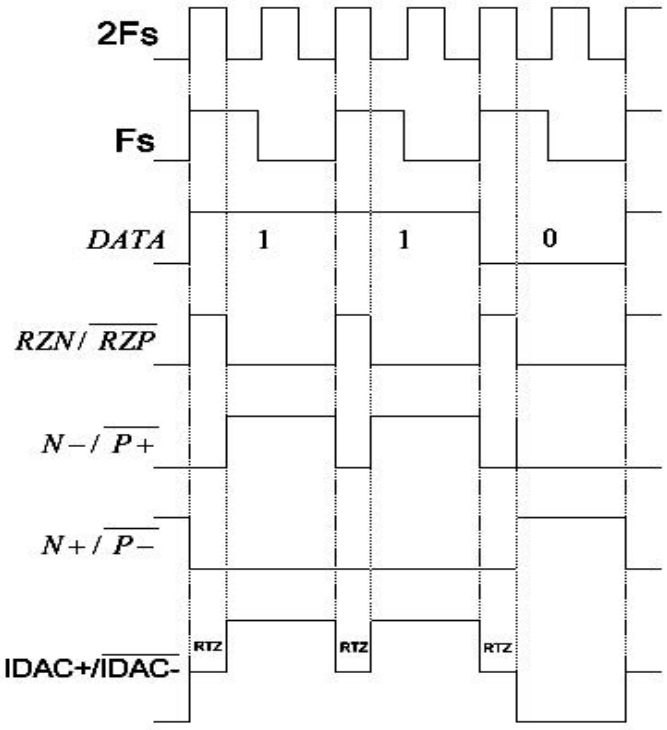


Fig.3.18. DAC control signal [6]

Circuit noise is usually the performance-limiting factor; include KT/C noise in capacitors, thermal noise in the resistors and switches, 1/f noise in the MOSFETS.

3.2 DIGITAL DECIMATION FILTER SIMULATION BY MATLAB

Filtering noise, which could be aliased back into the baseband, is the primary purpose of the digital filtering stage. Its secondary purpose is to take the 1-bit data stream that has a high sample rate and transform it into an n-bit data stream at a lower sample rate. This process is known as decimation. Essentially, decimation is both an averaging filter function and a rate reduction function performed simultaneously.

A multistage decimation filter is shown in Fig.3.19. It is made up second order comb-filter and three stages half-band filter. Comb filters are suitable for reducing the sampling rate to eight times the Nyquist rate. The remaining filtering is performed in three stages FIR filters.

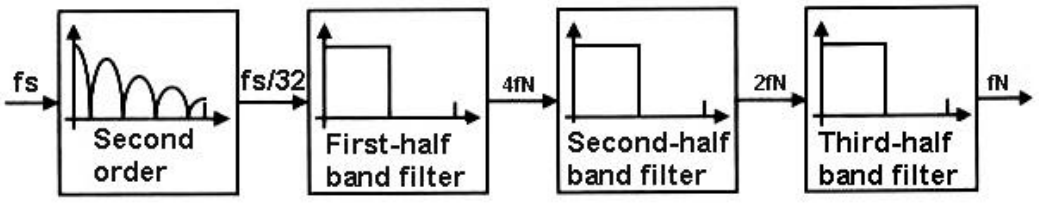


Fig.3.19. A multistage decimation filter

3.2.1 COMB FILTER

The simplest and most economical filter to reduce the input sampling rate is a "Comb-Filter", because such a filter does not require a multiplier. Because of the comb-filter coefficients are all unity. This comb-filter operation is equivalent to a rectangular window finite impulse response (FIR) filter.

The transfer function H (z) of a Comb Filter of order k for a decimation ratio N is defined by

$$H(z) = \left(\frac{1-z^{-N}}{1-z^{-1}}\right)^{M} \quad \textbf{(25)}$$

in the thesis, the order M=1 and decimation ratio N=32.

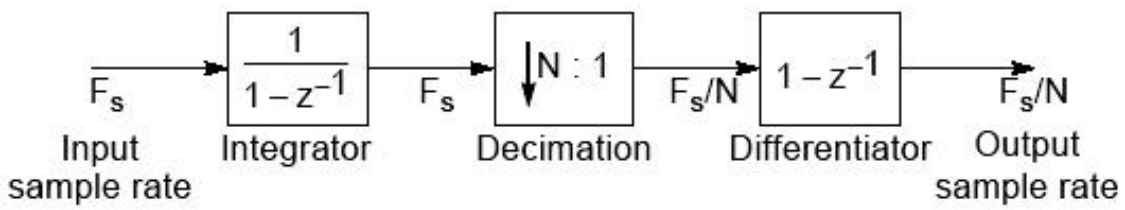


Fig.3.20. Block diagram of one-stage Comb Filtering process

Fig.3.20. Show the one-stage, N decimation ratio comb-filter process. In summary the magnitude response of a cascaded comb-filter with 32:1 decimation process is shown in Fig.3.21. In the thesis, is a 1st-order modulator, the required cascade number of the comb filter is K=M+1=2.

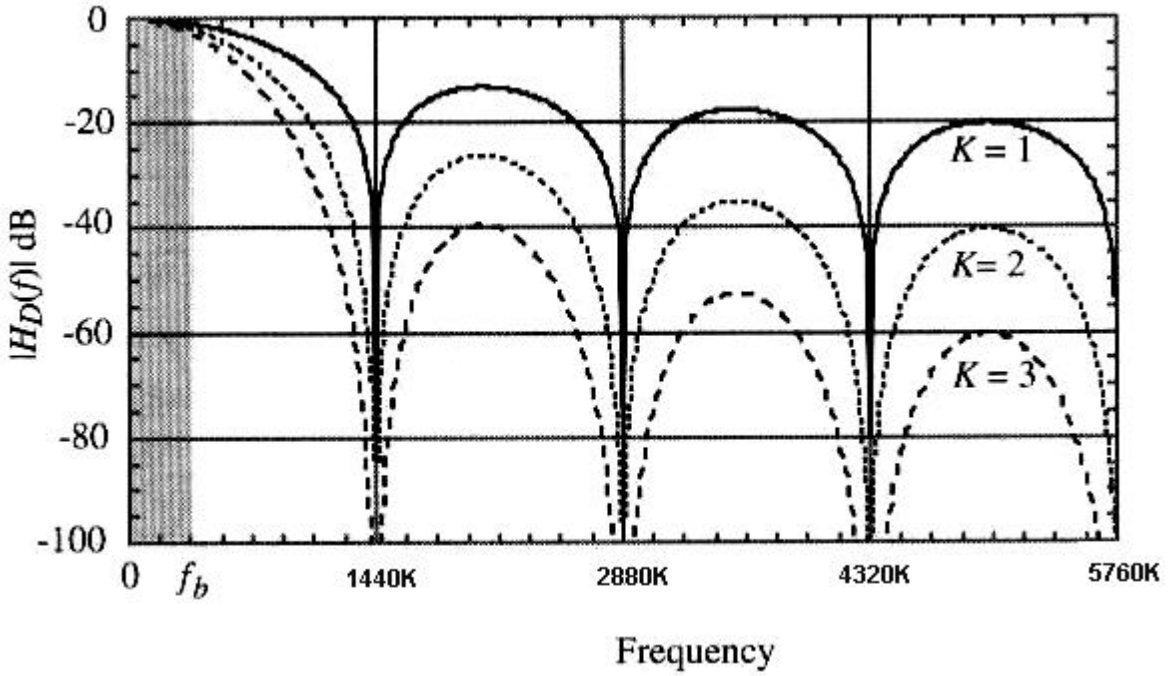


Fig.3.21. Magnitude response of a cascaded comb-filter for K=1, 2 and 3

3.2.2 HALF-BAND FILTER

Since a half-band filter can only implement a 2:1 decimation, a series of such filters may be cascaded to perform a higher decimation filter process.Fig.3.22 illustrates the 3 stages cascaded half-band filter design specification for a 8:1 decimation process.

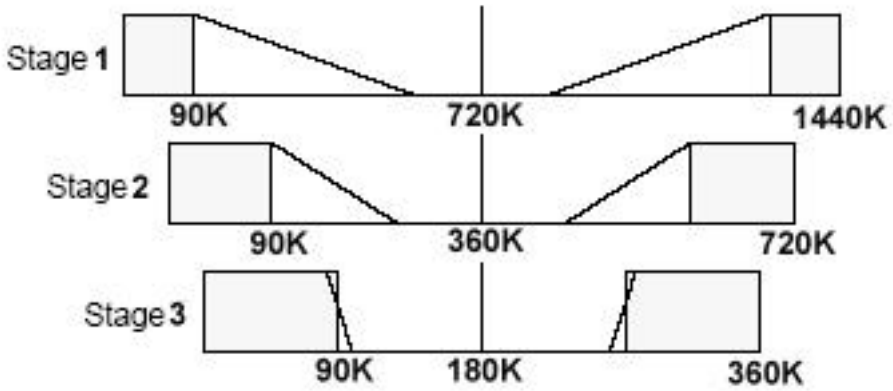


Fig.3.22. Decimation process using a series of Half-Band Filters

3.3 SIMULATION RESULTS

3.3.1 SIMULATION RESULTS OF GM AMPLIFIER

Fig.3.23. show the gm curve of the Gm-amp, the range that the thesis used from –250 mV to 250 mV is linearity; the current is about –18uA to 18uA, the gm value is 72uA / V.

Fig.3.24 show the FFT of the Gm amp, the SNR is 48.7dB, the SNDR is 47.2dB, about 7.5b resolution in-band signal.

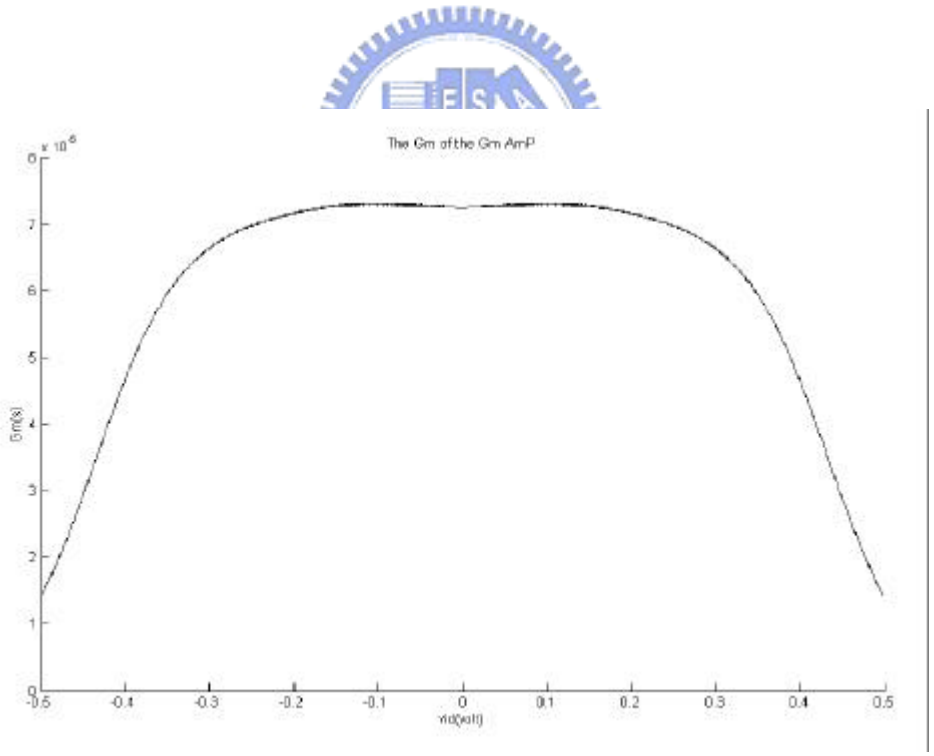


Fig.3.23. The gm curve of the Gm-amp

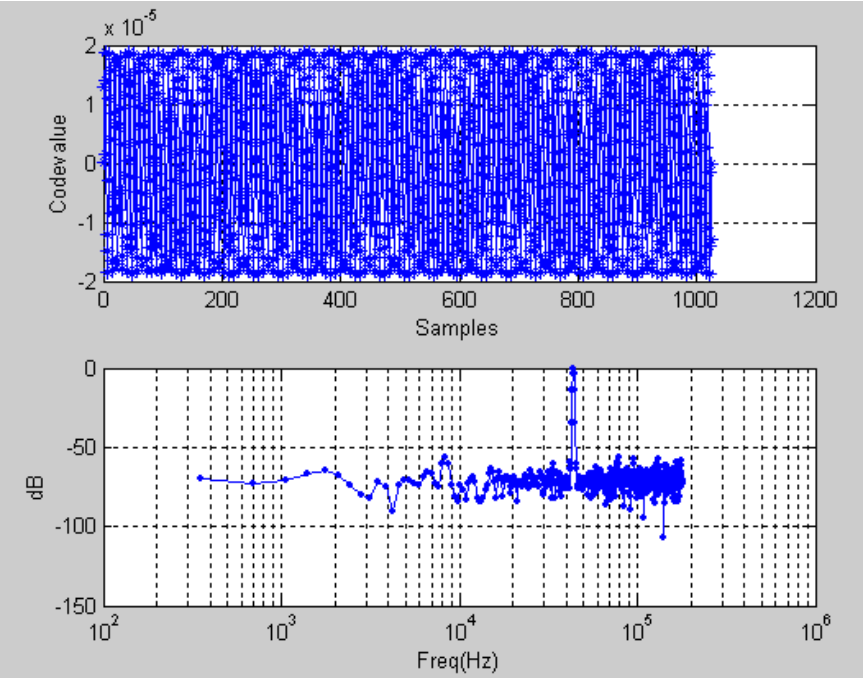
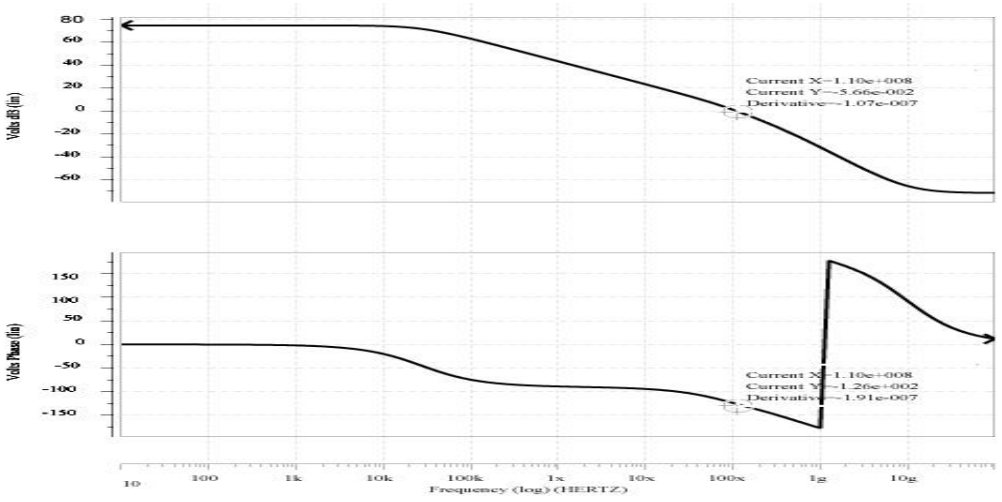


Fig.3.24. The FFT of the Gm amp

3.3.2 SIMULATION RESULTS OF INTEGRATOR

Fig.3.25.show the open-loop gain is 74.5dB, and phase margin is 54 degree and with 110MHz bandwidth, slew rate is 17.5V/us, settling time is 29.3 ns characteristics of fully differential opamp with practical Common-Mode FeedBack (CMFB) circuit.



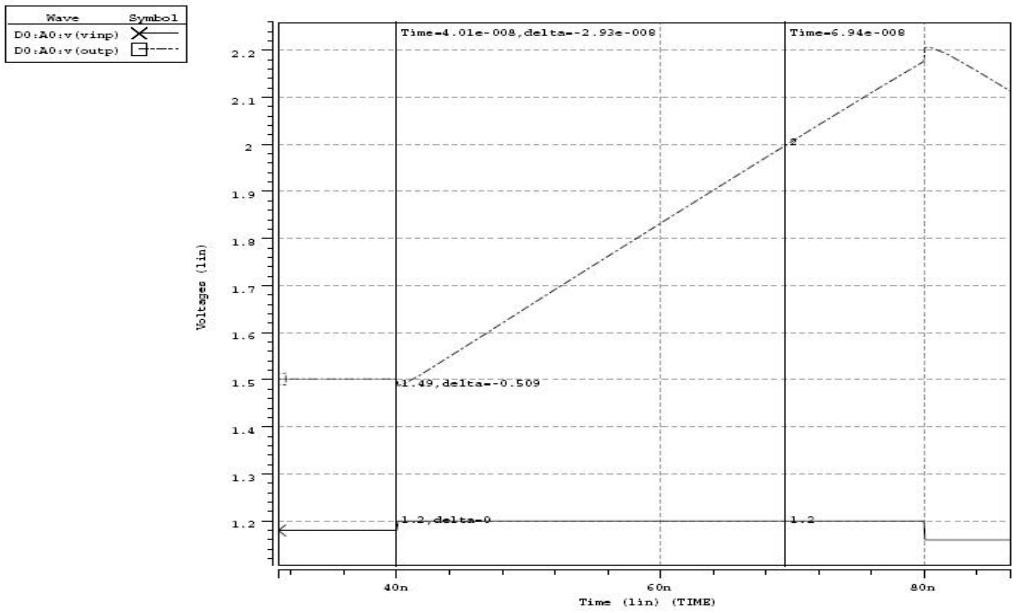


Fig.3.25. The characteristics of the fully differential opamp with practical Common-Mode FeedBack (CMFB) circuit

3.3.3 SIMULATION RESULTS OF QUANTIZER

Fig.3.26. show the regeneration action of the latch-type comparator includes precharge phase and evaluation phase. When the precharge phase, Voc+ and Voc- is pulled to Vdd. When the evaluation phase, Vin+ and Vin- working in comparing action.

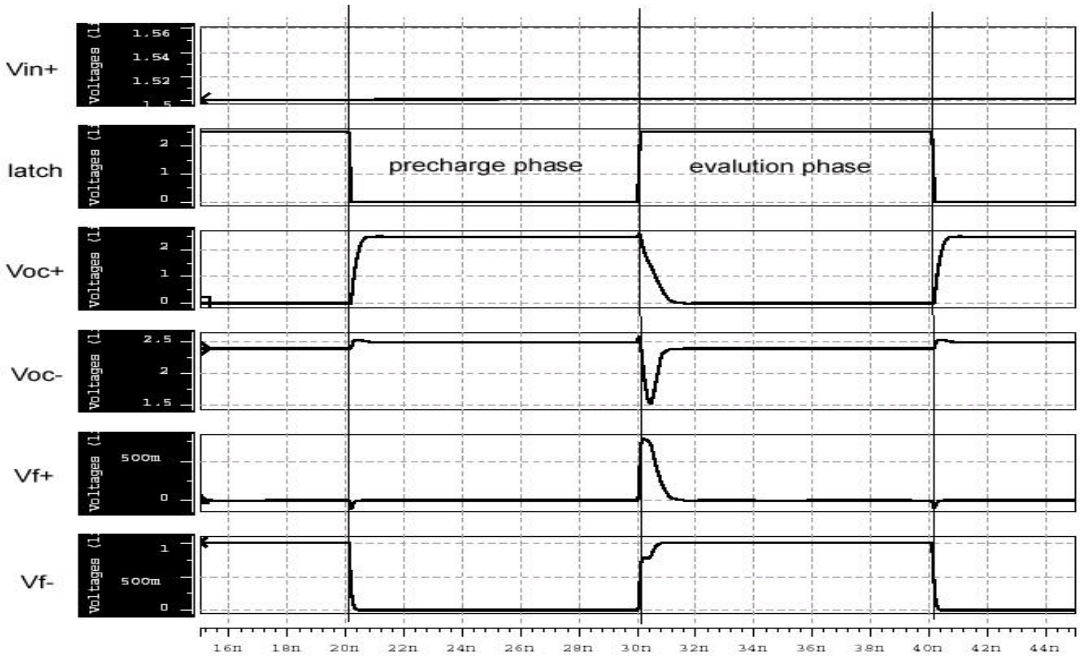


Fig.3.26. Regeneration action of the latch-type comparator

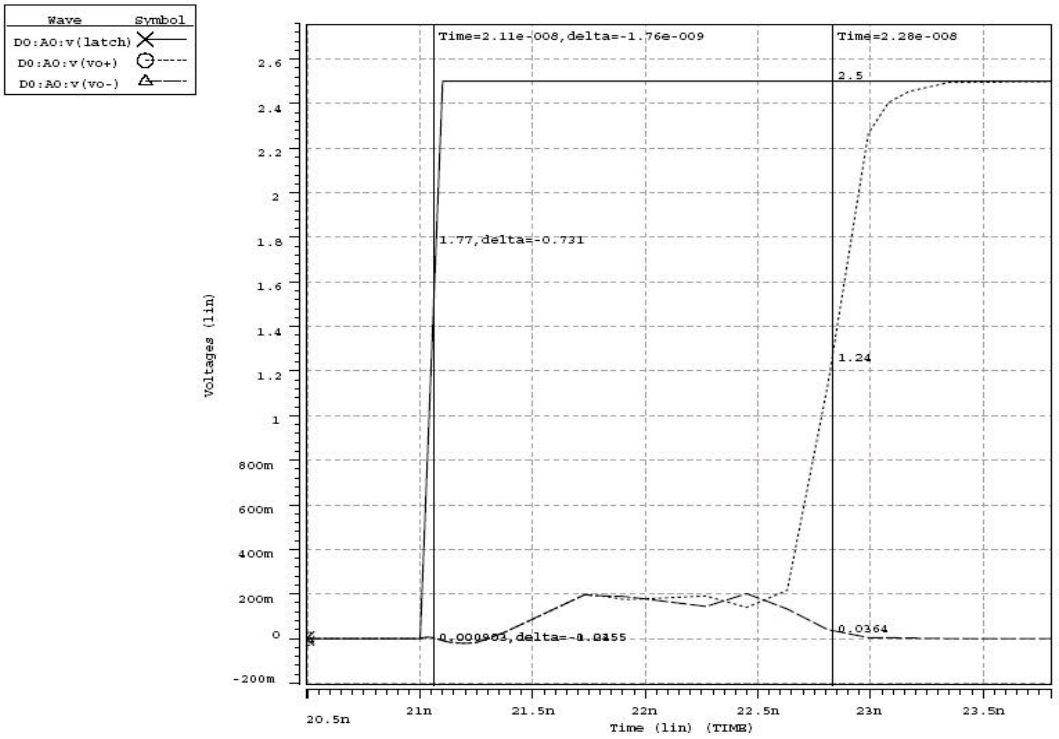


Fig.3.27. Simulation result of the latch-type comparator with 46.08MHz latch, 16uV differential input voltage

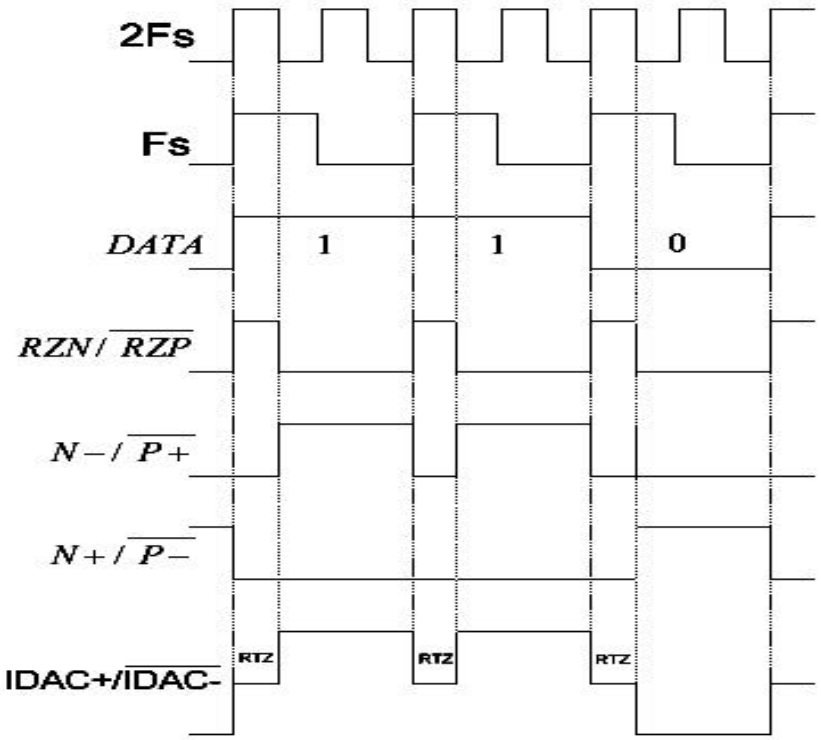


Fig.3.28. Simulation results of the control signal for DAC circuit

Fig.3.27. show the simulation result of the latch-type comparator with 46.08MHz latch signal and 16uV input differential voltage, the comparison time is about 1.76ns. The value is much less than $\frac{1}{2f_s}$. But the drawback of the design is that the separated-point needed to move to 1.25V to get the shortest compare time.

Fig.3.28. show the simulation results of the control signal for DAC circuit. To reduce the clock jitter come from quantizer to DAC delay, with 1/4 latch cycle Return-to-Zero (RTZ) is used.

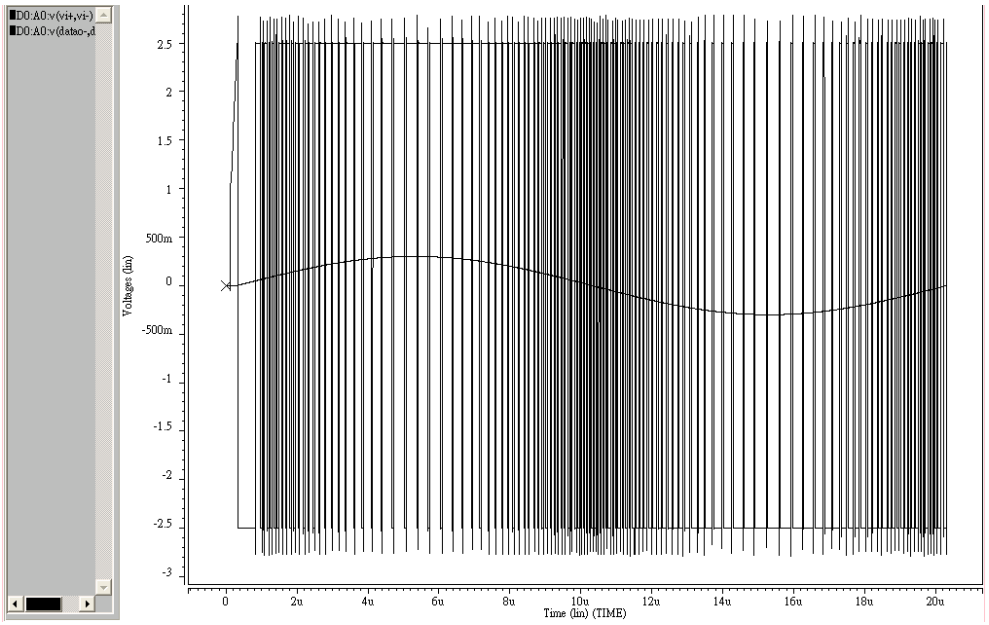


Fig.3.29. Overall simulation result of the sigma-delta modulator with HSPICE tool

Fig.3.29. show the overall simulation result of the sigma-delta modulator. The input signal is 1Vp-p and the output signal is +/-2.5Vp-p.

3.3.4 SIMULATION RESULTS OF DIGITAL DECIMATION FILTER

Fig.3.29.is sigma-delta modulator output waveform then using logic analyzer collects the data, using SIMULINK of MATLAB to verify as showed in Fig.3.30. The decimation filter is made of comb-filter and 3-stage cascade half-band filter. The comb-filter is made of 2 stages cascade integrator and 32:1 decimation and 2 stages cascade differentiator. The output frequency of the Fig.3.30 has been downed to Nyquist rate. Fig.3.31 is Digital filter design1, Fig.3.32 is Digital filter design2, Fig.3.33 is Digital filter design3. The decimation ratio can be downed to 256. The parameters of the design filter are listed in Table

II. Then put the output file to calculate for FFT analysis. Fig.3.34. show the simulation results for FFT plot for 1Vp-p, 44KHz sinusoidal input signal, after HSPICE simulation the SDM, then the MATLAB software can be used to run the decimation filter and to analysis FFT. SNR is 66.2dB (10.7 bits), SNDR=66dB (10.67 bits) within 90KHz. All the characteristics of the prototype ADC are summary in Table III.

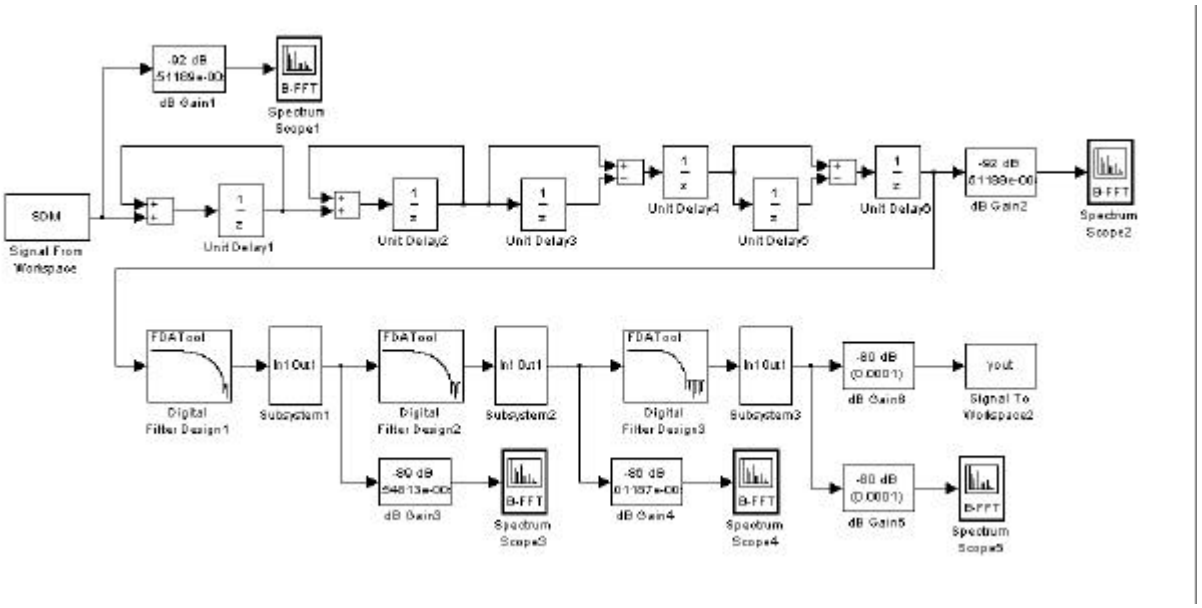


Fig.3.30. Decimation filter by SIMULINK of MATLAB software

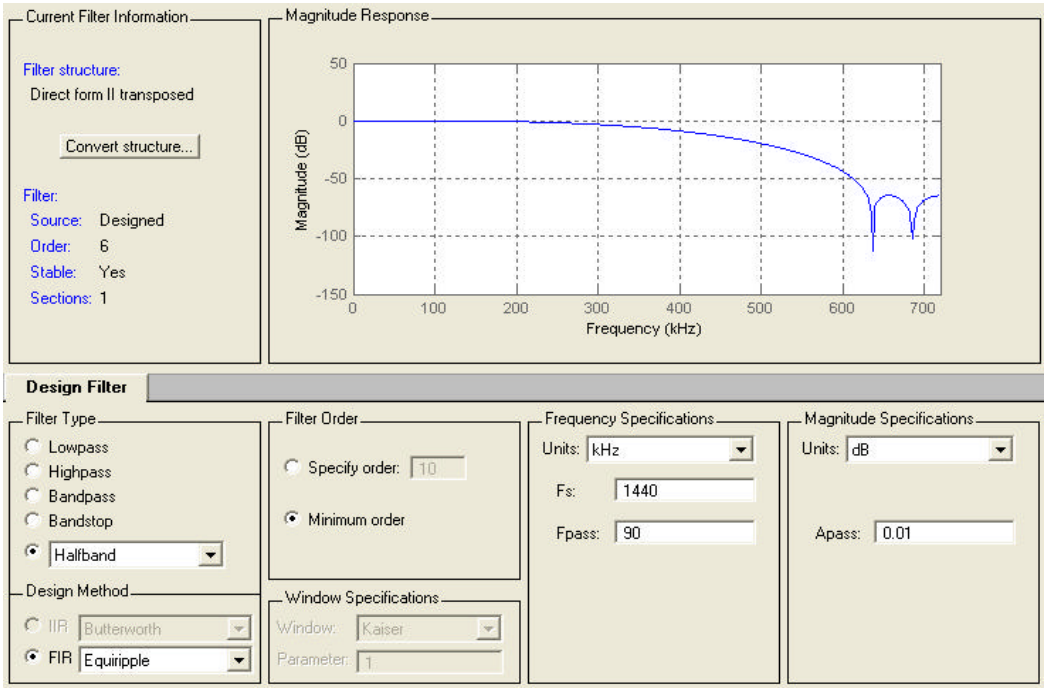


Fig.3.31. Digital filter design1

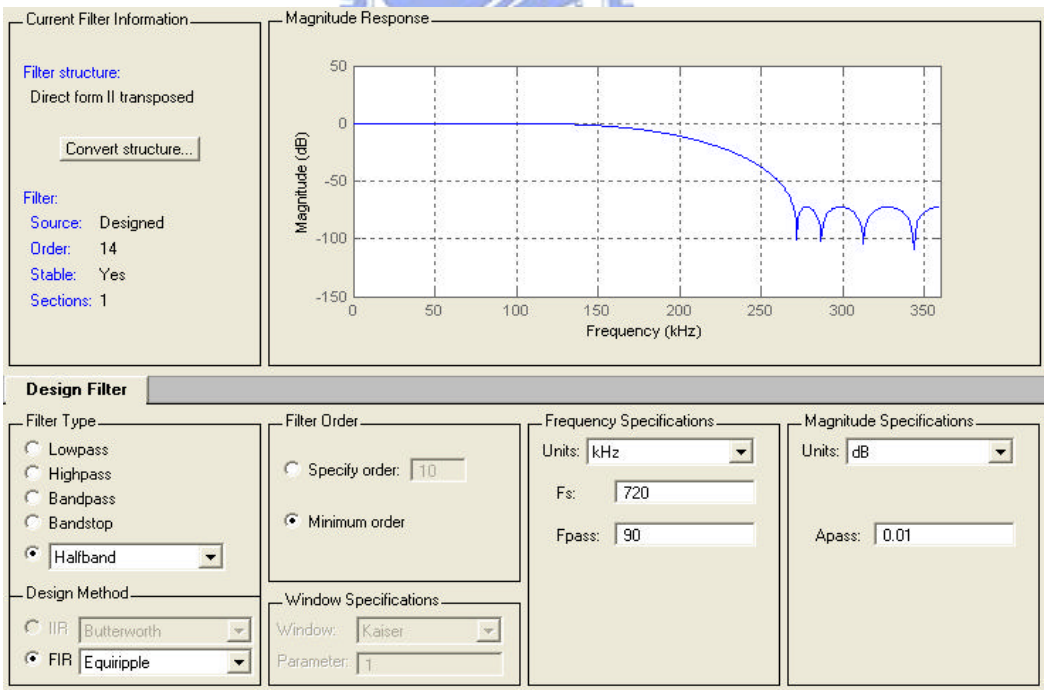


Fig.3.32. Digital filter design2

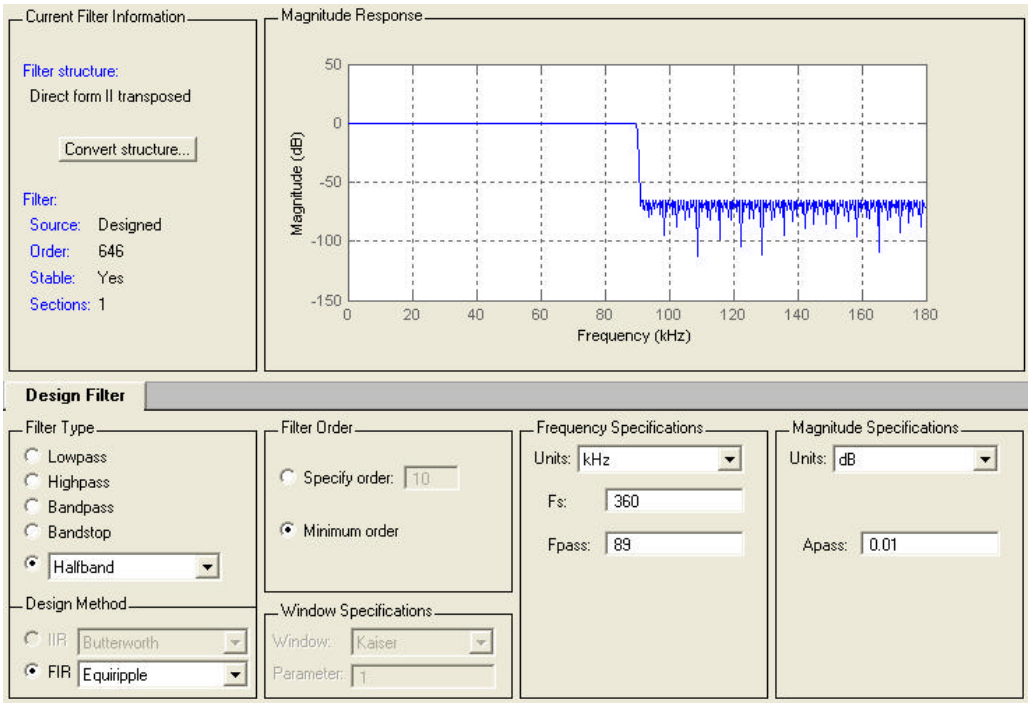


Fig.3.33. Digital filter design3

Table II. Parameters for designing filters

Stage	Output sample rate	Passband	Stopband
SIGMA-DELTA MODULATOR	46.08MHz	90KHz	–
COMB-FILTER (32:1)	1.44MHz	90KHz	–
1. HALF-BAND FILTER (2:1)	720KHz	90KHz	630KHz
2. HALF-BAND FILTER (2:1)	360KHz	90KHz	270KHz
3. HALF-BAND FILTER (2:1)	180KHz	89KHz	91KHz

The original sampling frequency is 46.08MHz, the input signal frequency is 44KHz, the OSR is 522. Through the comb-filter and 3 stages half-band filter, the final sampling frequency is 180KHz, the passband is 89KHz by sample theory. The software is limited by sampling frequency larger than four times input frequency. The real OSR is 256.

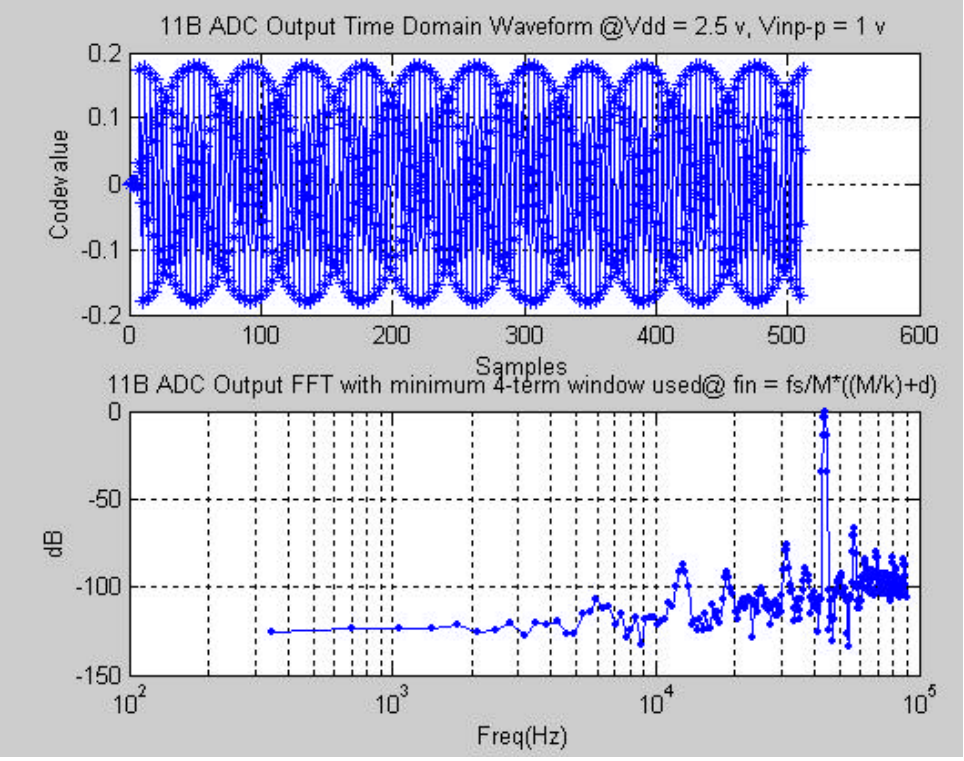


Fig.3.34. FFT plot for 44KHz input sinusoidal signal, SNR is 66.2dB, SNDR=66 dB

Table III. Summary of post-simulation results

	Post-Simulation
Technology	0.25μm 1P5M
Supply Voltage	Vdd=DVdd=OVdd=2.5V
Baseband limit	89KHz
Input differential range	1V
Power dissipation	8.34mW
Chip size	915 x 932 μm^2
Oversampling Ratio (OSR)	256
SNR@ Fs=46.08MHz	66.2dB (ENOB=10.7 bit)
SNDR @ Fs=46.08MHz	66 dB (ENOB=10.67 bit)

CHAPTER 4

EXPERIMENTAL RESULTS AND DISCUSSIONS

4.1 LAYOUT DESCRIPTIONS

The prototype ADC was fabricated using TSMC 0.25um 1P5M CMOS process. The linear capacitors were implemented by using MIM capacitor structure. The chip size of the converter was 913 x 932 um^2. Fig. 4.1 and Fig.4.2 shows the chip microphotograph and a floor plan of the sigma-delta A/D converter.

To reduce the digital noise coupling, the digital blocks and the analog blocks were separated by double guard rings and larger than 50um spacing. Moreover, the digital and analog power supplies are using different pads (Vdd, Vss and DVdd, DVss) and the output buffers are using OVdd, OVss pads. To avoid the power noise occurred the decoupling capacitor is implemented in idling area.

To avoid body effect occurred the NMOS p-substrate of the analog block is shorted to source terminal, the NMOS p-substrate of the digital block are separated with source terminal, and then shorted to p-substrate of the analog block. The NMOS p-substrate of the output buffers is independent of pad.

The fully differential opamp, gm amplifier was laid out carefully using a common-centroid arrangement to overcome variation in process. The capacitor arrays were laid out in common-centroid structures with dummy capacitors surrounded, which were placed inside N-well guard rings.

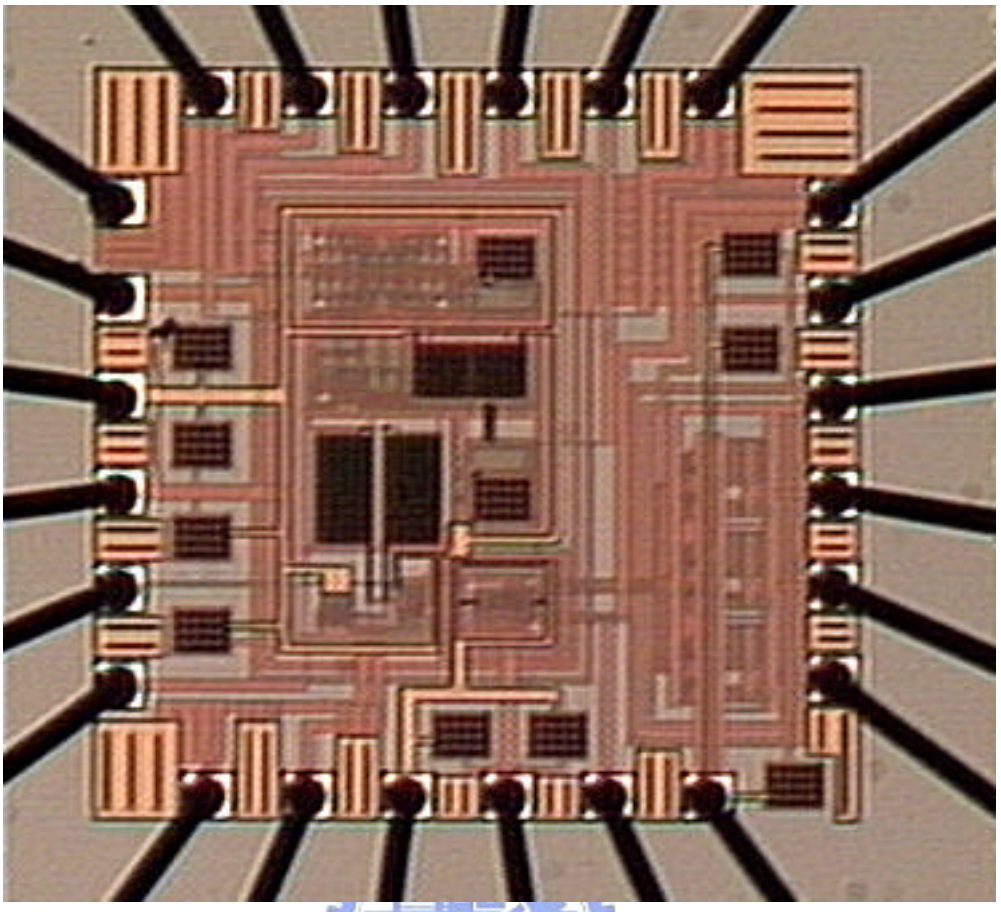


Fig.4.1. Chip photograph

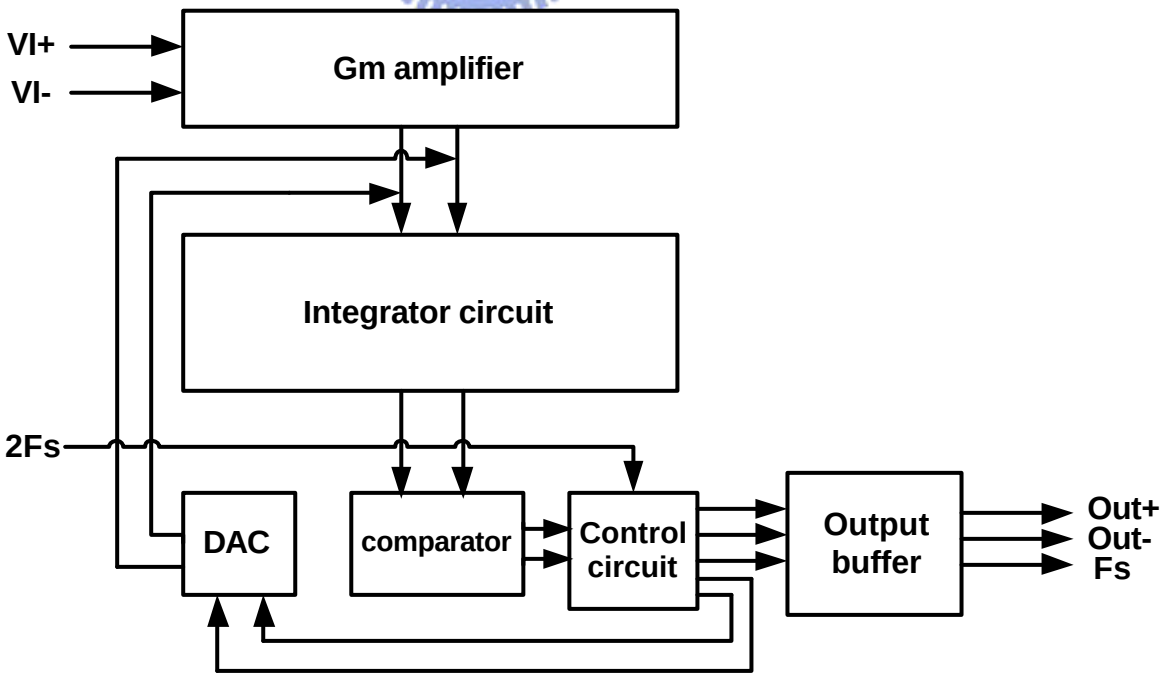


Fig.4.2. Floor plan of this ADC

The output buffer circuit is shown in Fig.4.3. To reduce the ground bounce, the driver of MP4 and MN7 is separated into two paths.

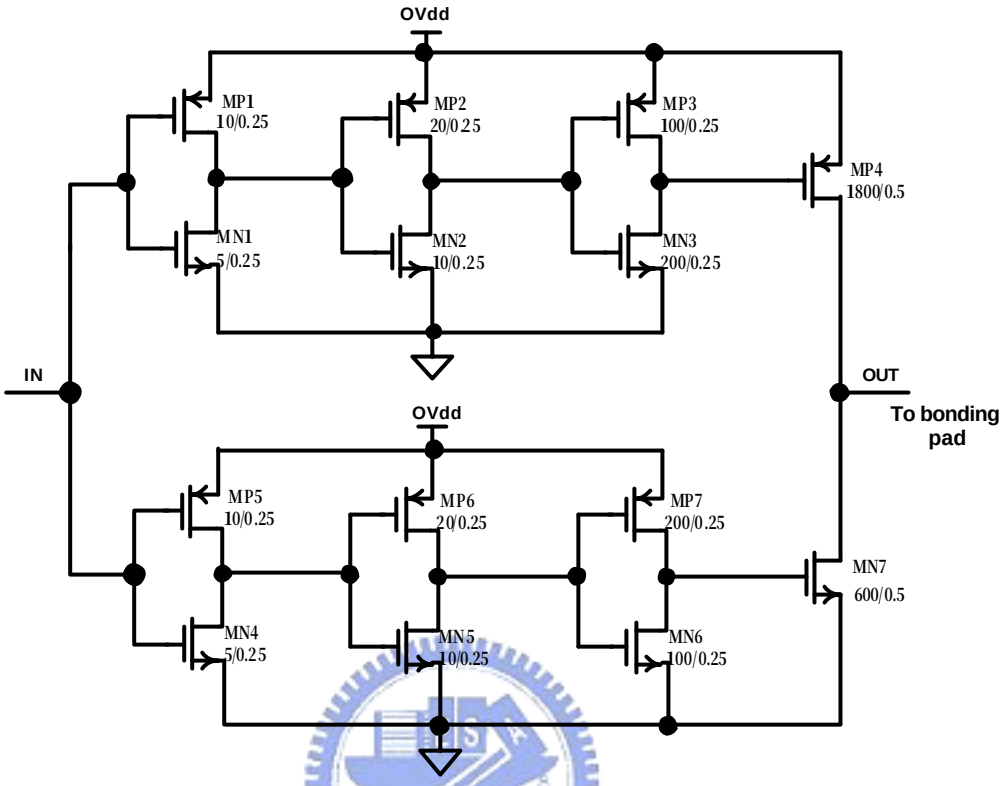


Fig.4.3 Output buffer circuit

4.2 TESTING ENVIRONMENT

The measurement setup is shown in Fig.4.4. Tektronix AWG420 that has 16-bit vertical resolution generates the sinusoidal input signal to parallel inverting and non-inverting opamp. Then the high-resolution differential sinusoidal signals are sent to the chip. Tektronix AWG520 that has 8 digits waveform resolution work as double sampling frequency source. The maximum amplitude is 2 volts supplied. Then the square signal is sent to the chip. The photograph of the PC test board is shown in Fig.4.5. The batteries (+9V, -9V) and regulators

generate the bias of the chip in order to avoid interference of the noise. To achieve highest level of performance, surface-mount components are used wherever possible. This reduces the trace length and minimizes the effects of parasitic capacitance and inductance. On the test board, the single-ended input sinusoidal signal is converted to a differential signal by using two positive and negative phase opamp. The model of high bandwidth and low offset opamps are ICL7650 that are manufactured by MAXIM. The logic analyzer HP16702 stores all the digital output data. All digital data can be collected and analysis by PC. Then the MATLAB software can be used to run the decimation filter and to analysis FFT.

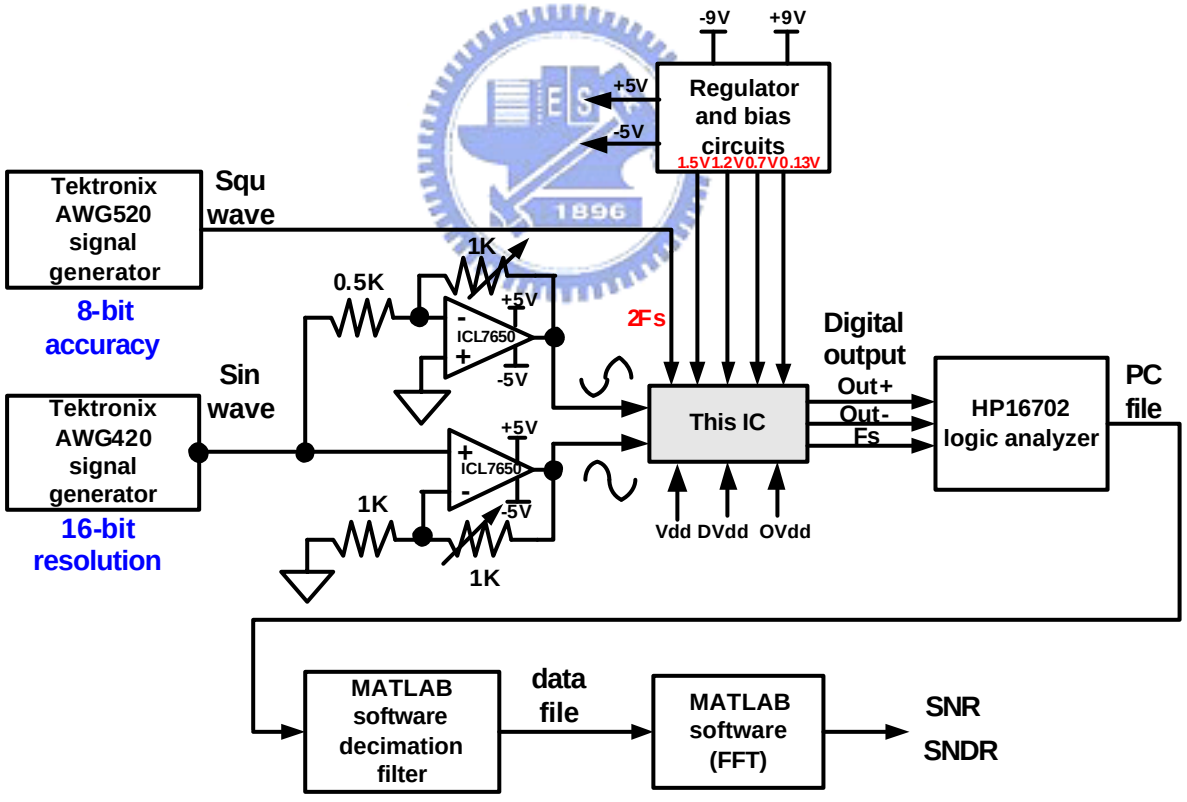
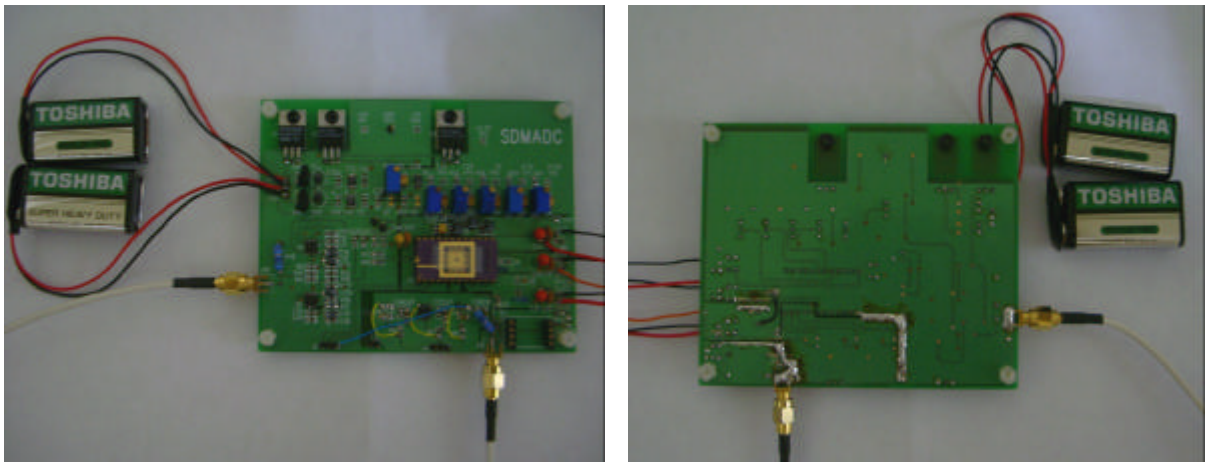


Fig.4.4 Measurement setup



(a) Top plate (b) Bottom plate

Fig.4.5 (a) (b) Photograph of the PC test board

4.3 EXPERIMENTAL RESULTS AND DISCUSSIONS

Fig 4.6 shows the waveform from logic analyzer, and then collects the logic data named to SDM of the Fig 4.7.

A SDM ADC verification flow chart is shown in Fig 4.7. A 131072-point samples is collected in SDM file for a 44KHz input sine wave, sampled at 46.08MHz is shown in Fig 4.7. And 131072-point FFT plot in spectrum scope1 is shown in Fig 4.8. Then through the 32:1 comb-filter get 4096-point FFT plot in spectrum scope2 is shown in Fig 4.9, the sampling rate is down to 1.44MHz. Then through the 2:1 1st stage half-band filter get 2048-point FFT plot in spectrum scope3 is shown in Fig 4.10, the sampling rate is down to 720KHz. Then through the 2:1 2nd stage half-band filter get 1024-point FFT plot in spectrum scope4 is shown in Fig 4.11, the sampling rate is down to 360KHz. Then through the 2:1 3rd stage half-band filter get 512-point FFT plot in spectrum scope5 is shown in Fig 4.12, the sampling rate is down to 180KHz. The yout file has

512-point send to analysis the SNR, SNDR by the program of the MATLAB. The results of the 512-point samples and FFT plot for 44 KHz input are shown in Fig 4.13 within 90KHz. The SNR is 62.5 dB and SNDR is 62.3dB. Table IV summarizes the simulated and measured characteristics of the prototype A/D converter.

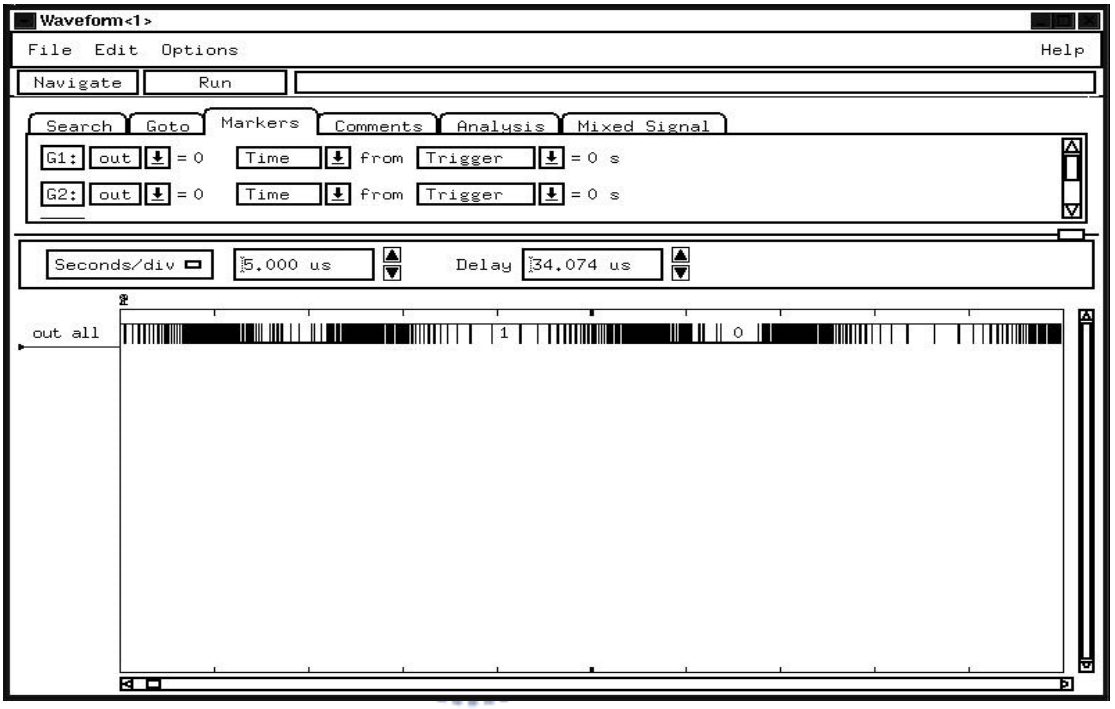


Fig4.6 Logic analyzer waveform

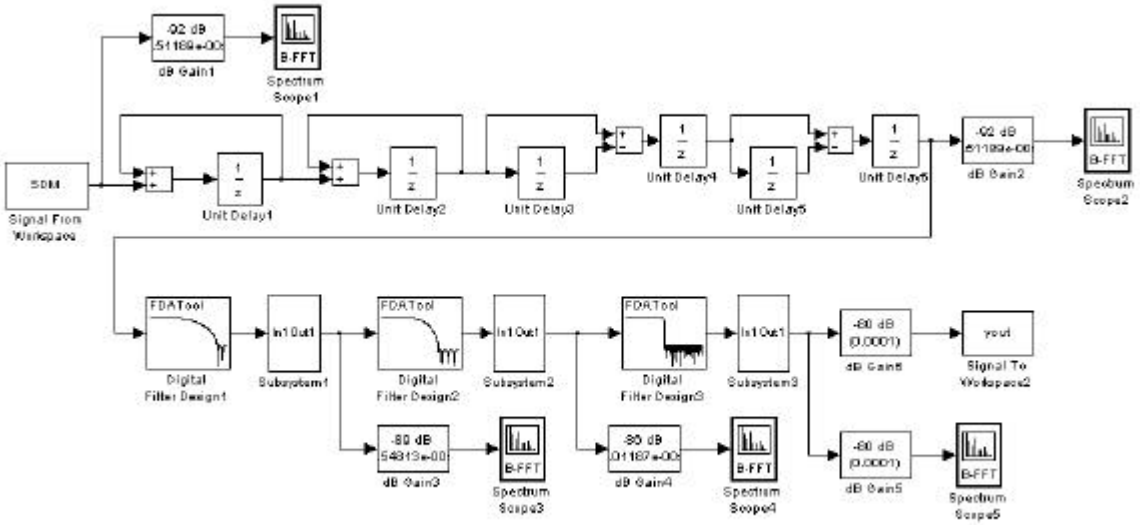


Fig4.7. A Sigma-Delta ADC verification flowchart

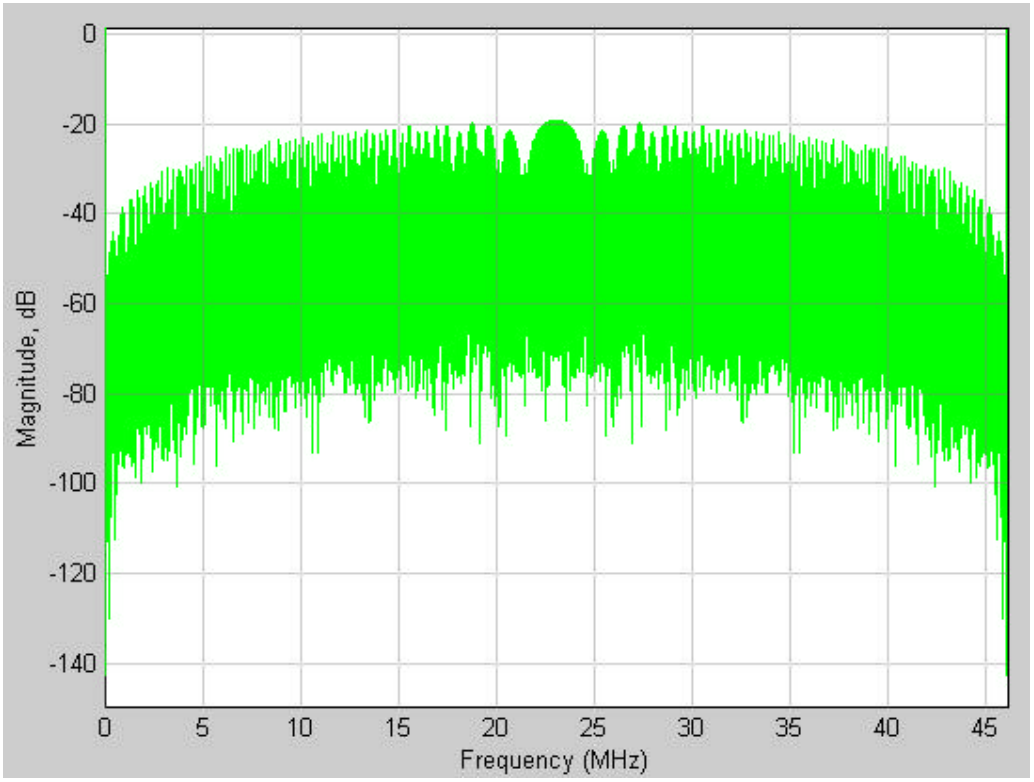


Fig4.8. 131072-point FFT plot in spectrum scope1

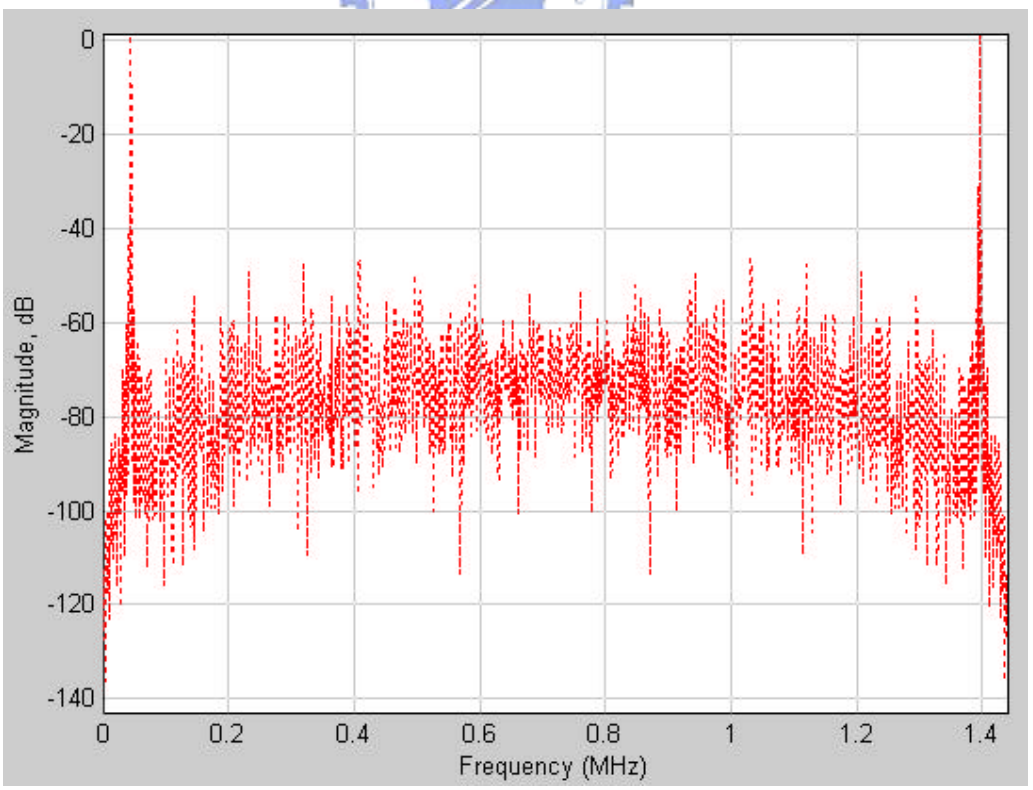


Fig4.9. 4096-point FFT plot in spectrum scope2

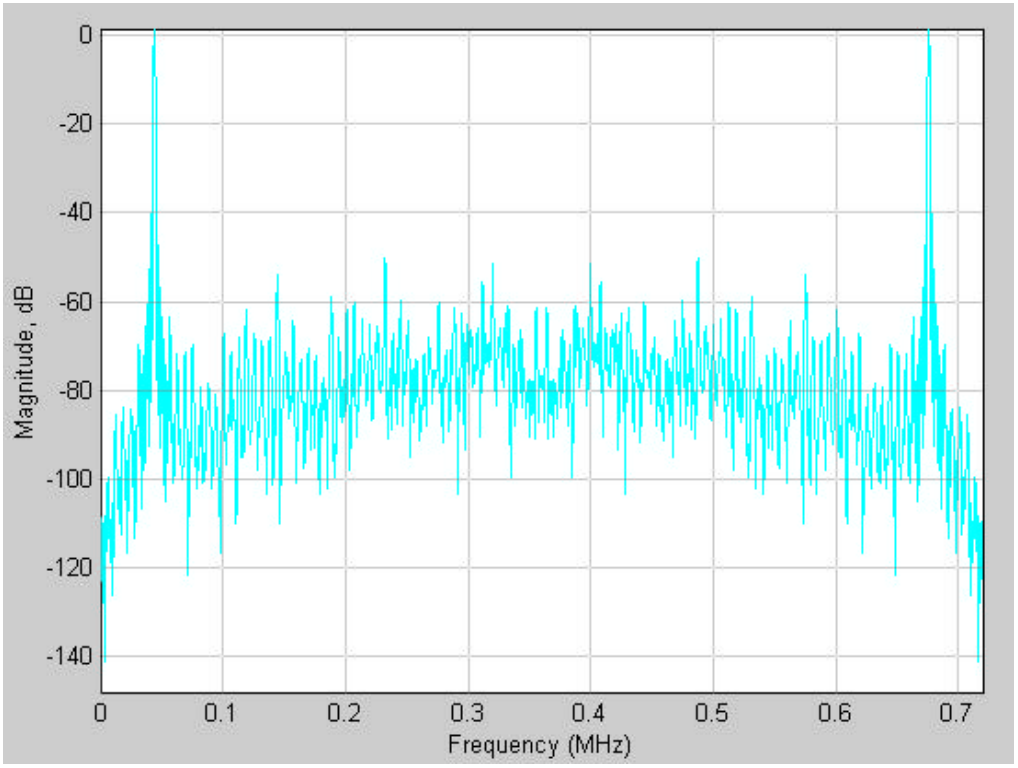


Fig4.10. 2048-point FFT plot in spectrum scope3

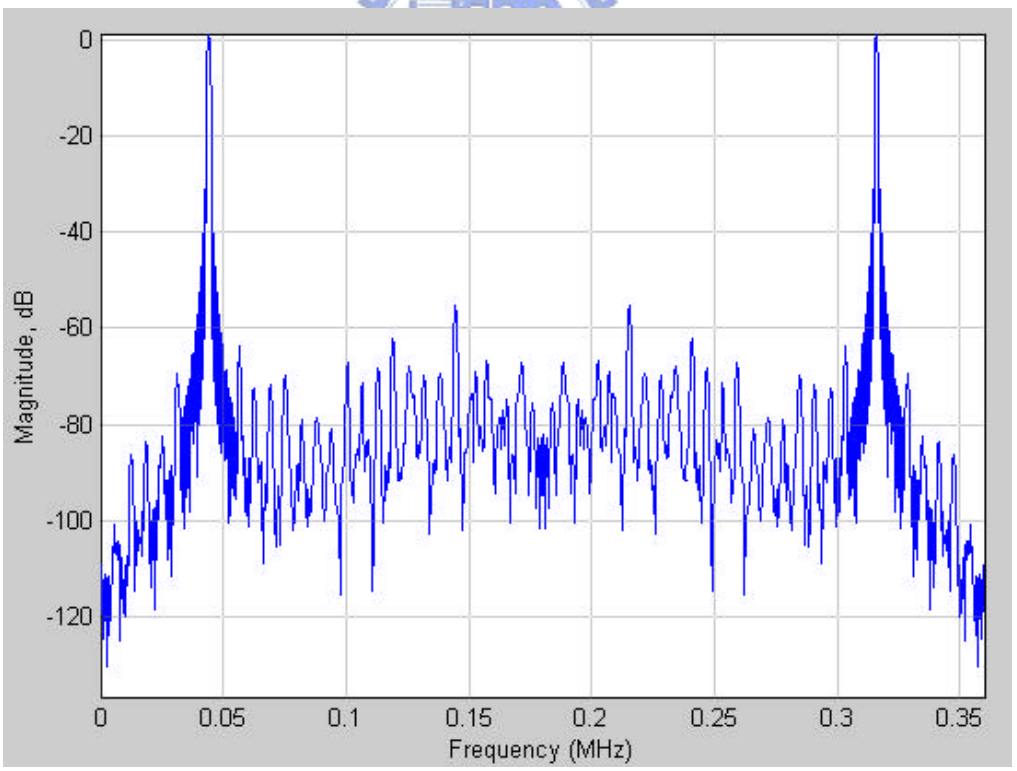


Fig4.11. 1024-point FFT plot in spectrum scope4

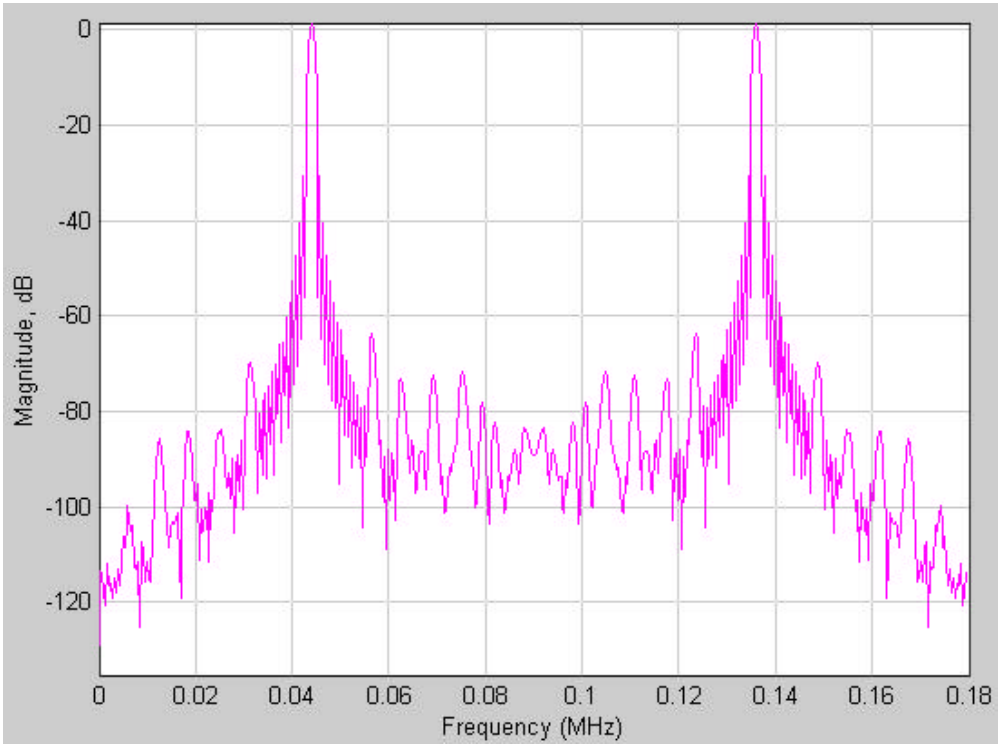


Fig4.12. 512-point FFT plot in spectrum scope5

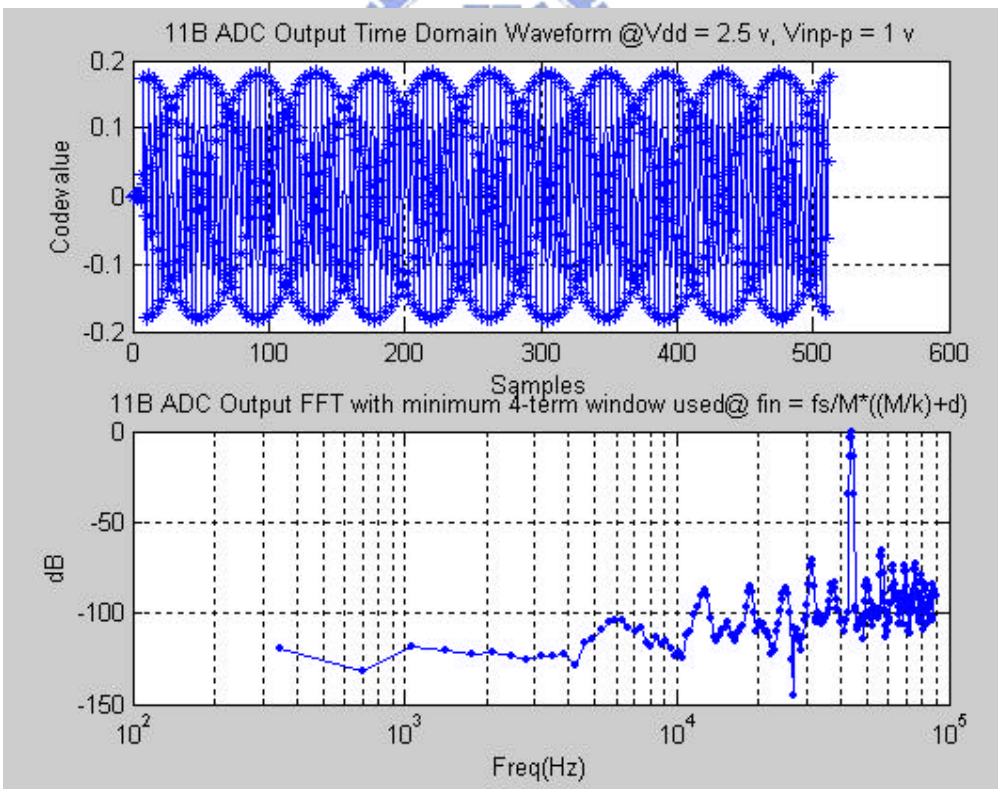


Fig4.13. 512-point output and FFT plot for 44 KHz input, SNR=62.5 dB

SNDR=62.3 Db

Table IV. The simulated and measured characteristics

	Post-Simulation	Measurement
Technology	0.25μm 1P5M	
Supply Voltage	Vdd=DVdd=OVdd=2.5V	
Chip size	915 x 932 μm^2	
Baseband limit	89KHz	89KHz
Input differential range	1V	1V
Power dissipation	8.34 mW	8.39mW
Oversampling ratio (OSR)	256	256
SNR @Fs= 46.08MHz	66.2dB(ENOB=10.7 bit)	62.5dB(ENOB=10.09 bit)
SNDR @Fs= 46.08MHz	66dB (ENOB=10.67bit)	62.3dB (ENOB=10.06bit)

Table V. Compare the measured results with surveyed paper

	This work experimental	[1] experimental	[16] simulation	[3] simulation
Order	1	1	1	2
Sampling frequency	46.08MHz	18.5 MHz	128 MHz	26 MHz
VDD	Vdd=DVdd=OVdd=2.5V	+/- 2.5 V	3.3 V	3.3 V
Technology	0.25 um	2 um	1.2 um	0.6 um
SNR	62.5dB(10.09b)	53.9dB(8.7b)	56.9dB(9.1b)	82dB(13.3b)
Power dissipation	8.39 mW	3 mW	1 mW	9.1 mW
Baseband limit	89KHz	72 KHz	1MHz	100 KHz
Oversampling rate	256	128	128	128

Table V compare the measured results with [1] [16] [3]. In this work, the OSR is larger than them, so the SNR is larger than [1] [16], is smaller than [3]. The power dissipation of [3] is the highest.

The measured SNDR is 62.3dB and the corresponding ENOB is 10.06-bit when input frequency is 44 KHz. There is 0.61-b resolution degraded compared with post-simulation result. The reason is that the sampling clock as shown in Fig 4.14. Sampling clock jitter results in non-uniform sampling and increases the total error power in the quantizer output. The amplitude of the sampling clock is 2.5V in the post-simulation. But the instrument maximum amplitude is 2V. DVdd and OVdd is supplied to 2.5V. The jitter value of the sampling clock is 44ps PkPk shown in Fig 4.15.

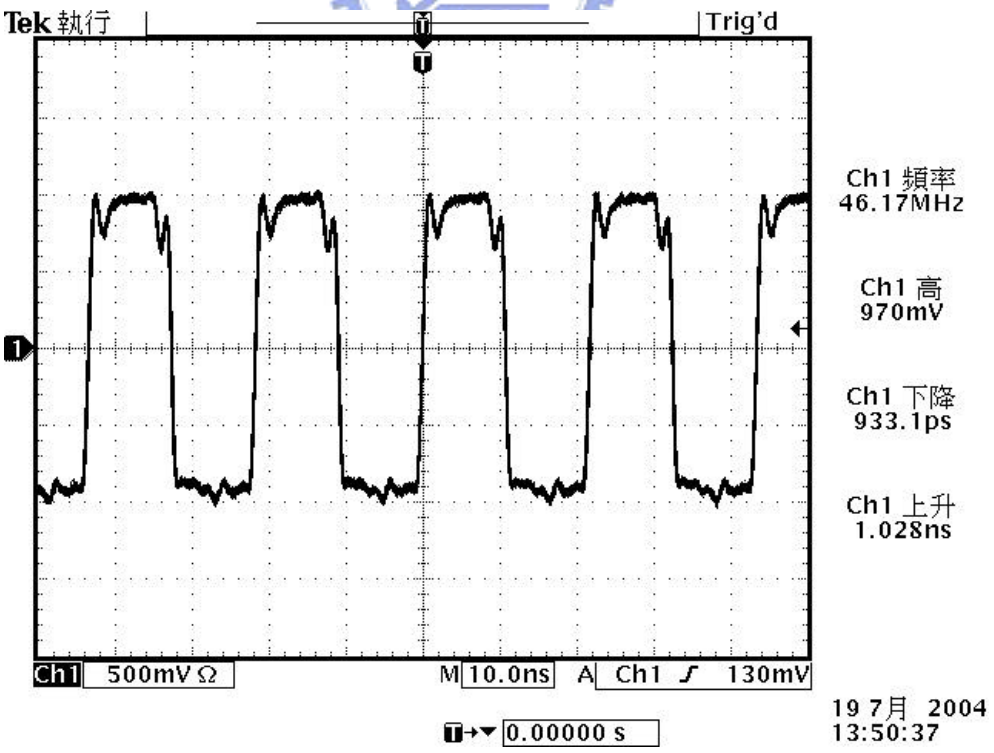


Fig 4.14 Sampling clock waveform

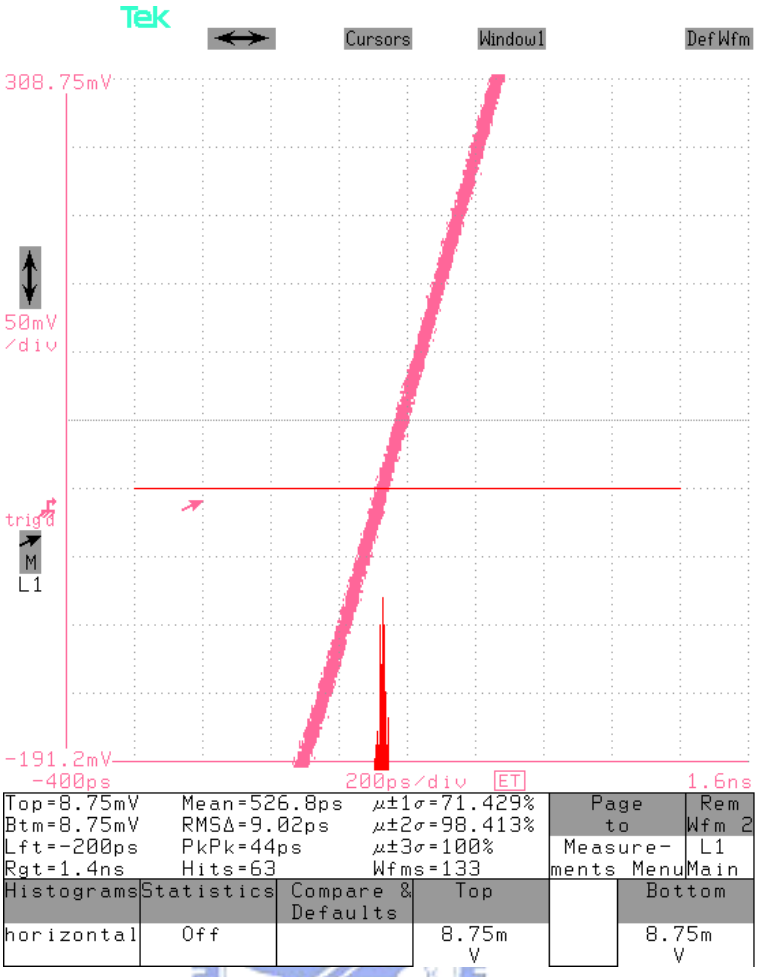


Fig 4.15 Sampling clock jitter

In the switched-current case this amount of charge varies linearly with the variation in timing. Consequently, the switched-current D/A converter are sensitive to clock jitter. If the clock jitter causes timing errors ?t with variance s_j^2, and the DAC output current levels are ±IDAC, the variance of the charge transferred per clock cycle T is

$$s_q^2 = s_j^2 \bullet I_{DAC}^2 \qquad \textbf{(26)}$$

The maximum signal amplitude is -3dB compared to the DAC current levels, so the maximum variance of signal charge is

$$s_{signal}^2 = \frac{T^2}{4} \bullet I_{DAC}^2 \qquad \textbf{(27)}$$

The maximum signal-to-noise ratio is the maximum signal power divided by the noise power in the signal band. Assuming that the noise power that is introduced by the jitter is white, the maximum signal-to-noise ratio due to the clock jitter is

$$\frac{S}{N} = 10\log\left(\frac{\boldsymbol{S}_{signal}^{2}}{\boldsymbol{S}_{q}^{2}} \cdot \frac{mf_s}{2f_b}\right) = 10\log\left(\frac{1}{8\boldsymbol{S}_{j}^{2} f_b m f_s}\right) \quad \textbf{(28)}$$

Where m is the oversampling ratio and fs is the sampling rate. The maximum jitter can be accepted is 482ps.

CHAPTER 5

CONCLUSIONS AND FUTURE WORKS

In this thesis, a 12-b high-precision high OSR 46.08MHz sampling rate 1st-order continuous-time sigma-delta ADC is realized with a 0.25um CMOS technology. The summary is as follows:

1. The measured maximum SNDR is 62.3dB (ENOB=10.06 bit) and SNR is 62.5 dB (ENOB=10.09 bit).
2. The total power consumption of the SDM is 8.39mW @Vdd=DVdd=OVdd= 2.5V.

Based on the analysis and experimental results mentioned above, the following practical issues can be further made:

1. In order to reject noise interference the four-layer testing PC board is needed, the second-layer for ground plane and the third-layer for power plane for better shielding.

2. In order to reach higher resolution, the higher-order structure is needed to achieve better noise shaping as shown in Fig.5.1 and Fig.5.2, but must consider the circuit stability.

3. When operating higher sampling rate that the signal source need low-jitter, high accuracy.

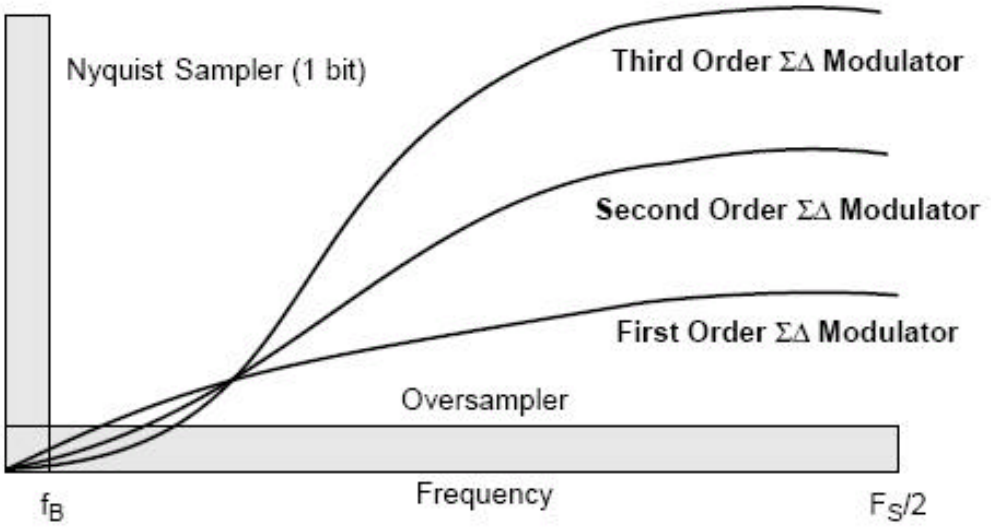


Fig.5.1 Multi-order Sigma-Delta noise shapers

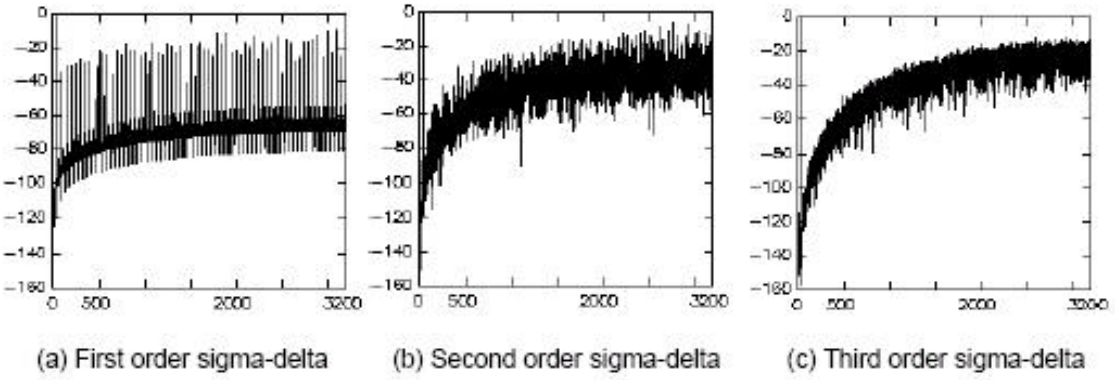


Fig.5.2 Spectra of three Sigma-Delta noise shapers

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