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碩 士 論 文

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A Study on Simulations of Single-Electron Memories

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摘　　要

單電子元件是目前相當受重視的一個研究領域，並被認為極有可能取代傳統的元件，尤其是應用在記憶體這個龐大的市場上。本篇研究使用 MOSES—根據蒙地卡羅模擬方法所設計的模擬軟體—來模擬多種單電子記憶體。包括 flip-flop 單電子記憶體、電子阱記憶體、背景電荷不相依記憶體以及旋轉門式架構的單電子記憶體。

除了上述元件的基本操作上的模擬外，在特性上也做了一番討論。對於 flip-flop 單電子記憶體的負載阻抗與記憶維持時間的關係曾做一番探討。電子阱記憶體在這篇論文裡是討論得比較多的，特別是在將之應用在單電子隨機存取記憶體上的相關問題。原始設計所存在的一些缺點，像是動作上的穩定性以及功率的消耗上，都有獲得改善。位元線、字線和 Vg 的電壓被調整到較省電，且又可正常運作的準位。接面數、溫度和 Vg 之間的關係在此也有分析。對於旋轉門式架構的單電子記憶體，clock wave 的寬度會影響到元件的穩定性，最大波長藉由模擬定出，因此也可以知道此元件的最小工作頻率。

A Study on Simulations of Single-Electron Memories

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ABSTRACT

Single-electron device is currently an important field of study and is supposed to replace the conventional devices, especially in the huge market of memory. In this thesis, a simulation tool MOSES which is based on Monte Carlo simulation method is used to simulate several types of single-electron memories including single-electron flip-flop memory, electron trap memory, background-charge-independent memory and turnstile based single-electron memory.

Besides the simulation of basic operation, the characterizations are also discussed in this work. The load resistance is discussed to improve the retention problem of single-electron flip-flop memory. The electron trap memory is discussed more detail in this thesis, especially for the application in the single-electron random-access memory. Several disadvantages of the original design like operation stability and power consumption have been improved. The voltages used for bit-lines, word-lines and Vg are modifies to have lower power consumption for all memory array. The correlations between junction number, temperature and Vg are also discussed. For the turnstile based single-electron memory, the width of clock wave correlates to the stability of this device. It is simulated to define the longest clock width. Therefore the restriction about working frequency of the turnstile based single-electron memory is obtained.

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Chapter 1 Introduction

1-1 Single-Electronics

Single-electronics is the field to study how to control the movement and position of a single electron or few electrons. The control over the movement and position of a single electron is based on a phenomenon described below.

Assume a small metallic sphere (traditionally called an island) initially electroneutral. It has exactly as many electrons as it has protons in its crystal lattice. In this state the island does not generate large enough electric field beyond its borders. A weak external force $\boldsymbol{F}$ may bring in an additional electron from outside. After the additional electron is in this island, the net charge $\boldsymbol{Q}$ of this island is $-e$. The resulting electric field $\mathcal{E}$ repulses the following electrons from outside. Even the charge $e \approx 1.6 \times 10^{-19}$ Coulomb is very small, the field $\mathcal{E}$ is inversely proportional to the square of the island size and becomes very strong if the island size is small. According to Likharev, the field is $\approx$ 140kV/cm on the surface of a 10-nm sphere in vacuum [1]. It's easily larger than the external force $\boldsymbol{F}$, as shown in Fig. 1-1. This phenomenon is the foundation of single-electronics.

Accurately, the single electron is not isolated because there are still many electrons in this island but the key point of single-electronics is to manipulate electrons with single-electron precision.

Because of the improvements on semiconductor process integrations, we have better opportunities to study this field. The limitations of conventional semiconductor devices like scale, power consumption and

speed also push us to think about other possible and promising methods. That's why single-electronics is going to play an important role in the future.

1-2 History of Single-Electronics

The fact that charge is discrete and single valued was found by Millikan from his famous oil drop experiment and he received the Nobel prize in 1923. However, it took several decades for the field of single-electronics to progress further until the late 1980s because of the big improvement in semiconductor integration and process. But for the theories which help us to understand single-electronics, the research in quantum mechanics played an important role and filled the emptiness caused by poor semiconductor integration techniques in the last several decades, especially quantum mechanical tunneling since single-electronics is a field of nanoscale.

A totally new fundamental concept that particles may also have the characteristics of waves was introduced by Broglie in 1926. Schrodinger expressed this idea in 1926 with a form which is known as the Schrodinger wave equation. Because of the usage of wavefunction to represent an electron or particle, it implies an ability to penetrate the regions which is impossible from classical point of view and a probability of tunneling from one classically allowed region to another. Conclusive experimental evidence for tunneling was found by Esaki [2] in 1957 and by Giaever in 1960. Esaki's tunnel diode had a large impact on the physics of semiconductors.

A current suppression at low bias voltage as the cause of Coulomb repulsion was explained correctly by Gorter [3] in 1951. This phenomenon is known today as Coulomb blockade. About ten years later, the same current suppression at low bias voltages was observed from granular films by Neugebauer and Webb [4]. In 1985, Dimitri Averin and Konstantin Likharev [5] formulated the “orthodox” theory of single-electron tunneling, which quantitatively describes important charging effects such as the Coubomb blockade and single-electron tunneling oscillations.

About fabrication of single-electronics, Dolan [6] developed the double shadow evaporation process and Fulton and Dolan [7] built the first single-electron transistor (SET) and observed single-electron charging effects. This technique and its variations are still the most prevalent ones to manufacture single-electron devices in metallic material systems today.

Once the fundamental physical understanding was achieved and practical manufacturing methods were known, single-electron devices and circuits were the next step to go. To start the research, analysis and simulation tools are necessary for no matter digital or analog devices or circuits. The Monte Carlo method proves its potential to simulate single-electron devices because it traces the evolution of individual electrons and shows a clear image of the movements of the electrons based on the calculation results of interaction to other parts in the circuit. Especially for today’s computer technology, with powerful CPU and large enough memory, Monte Carlo takes much less time than it was in the past and gains significant importance.

Bakhvalov [8] was the first one to use a Monte Carlo approach to simulate single-electron devices. A master equation method introduced by Ben-Jacob [9] is also an appropriate technique applicable to single-electron devices. The Monte Carlo method and the direct solution of the master equation are today the mainstay of simulation for single-electron devices and circuits. A third method, the macro-modeling of single-electron devices in SPICE, is employed more frequently in the last years [10]. It was first suggested and applies by Fujishima [11]. The group at New York University in Stony Brook, headed by Likharev, developed two very influential and publicly available programs, MOSES and SENECA. SIMON developed by Christoph Wasshuber [12] is also proved as a powerful simulation tool and used in some research documents.

1-3 Coulomb Blockade

The Coulomb energy $E_C = \frac{e^2}{2C}$ must be overcome before an electron is transferred to an island. Consider a simple circuit which is generally called a single-electron box as shown in Fig. 1-2. The voltage source is the only energy used to overcome the Coulomb energy if we neglect the thermal fluctuation. As long as the voltage source is smaller than the threshold $V_{th} = \frac{e}{C}$, not even an electron can be transferred through the tunnel junction to the island. This is called Coulomb blockade. Increasing

the voltage bias will make the electrons transferred to the island one by one. A staircase charge-voltage characteristic can be easily observed.

1-4 Simulation of Single-Electronics

Kirchhoff's fundamental laws can be used only on conventional circuits since their electronic charge is assumed to be continuous. In single electronic circuits, the charge transfer due to tunneling is discrete and the event of the electron tunneling has stochastic nature. Conventional simulation is not suitable for single-electron devices and therefore a simulation method, Monte Carlo method, is used for single-electron devices. It showed that Monte Carlo is suitable for the simulation of such kind of stochastic physical events [13].

In Monte Carlo simulation, the tunneling rate Γ is the most important parameter to describe the frequency of electron tunneling events through tunnel junctions. Based on this Γ, we can judge whether the tunneling occurs or not. Since the tunneling events determine the charge status of each node, the happening of tunneling also correlates to the voltage conditions. The new charge and voltage conditions affect the tunneling rate Γ again. Finally we'll have a clear picture of the evolution of this single-electron circuit.

A random number r plays an important role in Monte Carlo simulation. The tunnel interval $t_{tunneling}$ is evaluated for all tunnel junctions by using this random number in the range of $0 \le r \le 1$ given by

$$t_{tunneling} = -\frac{1}{\Gamma_i}\ln(r)$$

The minimum time interval for electron tunneling is chosen and compared with a time duration in which the change of external voltage exceeds a given threshold value in the case of AC voltage source. If the minimum $t_{tunneling}$ is smaller than this time duration, the tunneling happens at the tunnel junction then the minimum $t_{tunneling}$ is added to total simulation time. If the minimum $t_{tunneling}$ is larger than this time duration, no tunneling event happens and new potential because of this voltage source is used for tunneling rate consideration. Simulation time proceeds this duration without updating the charge condition. The above processes are repeated until the time exceeds a specific maximum time then we have the final state of this single-electron circuit. The flow chart is shown as Fig. 1-3.

1-5 Applications of Single-Electronics

The advantages of the single-electron devices are ultralarge scale [14], ultralow power consumption and fast operation [15]. Good scalability is the strong incentive to explore the possibility of this device. Because the operating principle relies simply on the Coulomb repulsion among electrons, single-electron devices are anticipated to operate with very small physical dimensions, such as atomic scale. This makes ultralarge scale integration possible. Another advantage is its ultralow power operation because they use very small number of electrons to accomplish basic operation. Another advantage is the faster operation. In

conventional devices, hundreds of thousands of electrons are charged or discharged for a digital operation. But in single-electron devices, only a few electrons are transferred. This makes the process faster than those of conventional devices.

For the applications of single-electronics, some concepts including analog, logic fields and single-electron memories were suggested and mentioned [1] [16].

A supersensitive electrometer was suggested by K. K. Likharev [17]. It uses the property that if the source-drain voltage V applied to a single-electron transistor is slightly above its Coulomb blockade threshold V_t, source-drain current I of the device is very sensitive to the gate voltage U. Another spin off of this single-electron electrometer is the usage for measuring the electron additional energies in quantum dots and other nanoscale objects (single-electron spectroscopy).

The standard of DC current is also a promising application. The suggestion of this application is to phase lock SET oscillations in a simple oscillator. With a well-characterized frequency f, the phase locking provides the transfer of certain number m of electrons per period. This generates DC current as $I = mef$. The research for using single-electronics as a standard of absolute temperature developed by Pekola [18] also showed a possible application. Other applications like resistance standards and detection of infrared radiation are also possible fields in which single-electronics are useful [1].

For logic applications, there are more constraints. Uniformity and interconnection are especially stringent. Compared to logic circuits, memories have a very symmetric layout. Amplifiers can be used by

several cells at different time and this can be treated easily in single-electronics. For logic, the situation is different. For example, the longest interconnections of a processor are as long as the edge of the die and the same repeater can rarely be used by several signals. Although there are some challenges for logic applications, several ideas were developed. The concept which uses single-electron transistors as inverters was suggested by Tucker [19]. Further research which implemented this concept in an A/D converter was developed by C. H. Hu [20].

One of the most promising applications is the single-electron memory. More introduction of single-electron memory is included in the following section.

1-6 Single-Electron Memories

One reason why single-electron memory is important is that single-electron devices are not suitable for logical functional units because single-electron devices have poor current-drive capability and this is necessary to communicate with another distantly placed logic unit for a logic device. This gives single-electron memory more chance than logic devices. Another reason is that since the memory cell technology changes continuously to become smaller and smaller and the requirement of memory keeps going high because of huge applications of digital products like camera, PC, PDA…etc, single-electron memory seems to be a good solution.

Memory cell technology changes continuously to become smaller and smaller. Single-electron memories provide a totally new aspect to

store information and are ultimate devices which can store one-bit information by charging a single electron. This device is one of promising candidates for basic elements of future electronics because its power dissipation is expected to be very small compared to a conventional semiconductor memory, like DRAM, which needs to charge hundreds of thousands of electrons for one-bit information. The conventional DRAM operates by storing charges in individual storage capacitors with a capacitance of C_{cell}. The leakage of the access transistor should be low in order to have a long retention time so the transistors have a relatively high threshold voltage (0.5~0.7 V). When a DRAM cell is selected, a higher word line voltage is used to turn on the transistor then the charges stored in the cell are dumped onto the bit line for charge sharing. This causes a voltage variation and is detected by the sense amplifier. C_{cell} has to be as large as possible to store enough charges to make the signal of the bit line detectable by the sense amplifier. Typical C_{cell} is in the range of 25~35 fF. Fig. 1-4 shows the structure of a trench type memory cell of the conventional DRAM. Over 100000 electrons flow in or out the cell for each read or write not like the single-electron memory which uses only 1 or few electrons for operation.

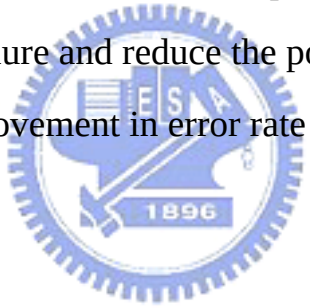
1-7 Objective

Since single-electron memories shows so much potential, this thesis focuses on the simulation of single-electron memories. Several types of single-electron memories including single-electron flip-flop memory,

electron trap memory, background-charge-independent memory and turnstile based single-electron memory are simulated and discussed.

MOSES, a single-electron simulator, developed by Ruby H. Chen is used for simulation. This is a tool based on Monte Carlo simulation. SIMON, developed by Christoph Wasshuber, is a better choice because of its friendly interface. It is used largely in the field of single-electron simulation but since the free version is not available for me, MOSES is the only choice.

During the simulation of the devices mentioned above, some weak points of a single-electron random-access memory are observed. Some modifications of the circuit and fine-tune of potential are made to overcome the function failure and reduce the power consumption. The simulation results of improvement in error rate and compromise in write speed are also compared.



Chapter 2 Basic Theories

2-1 Tunneling Rate

The total internal energy E_{internal} of a close system consisting of capacitors, tunnel junctions and voltage sources is conserved. The decrease in electrostatic energy for a tunnel event is dissipated as heat:

$$E_{\text{internal}} = U + Q_{\text{thermal}}$$

where Q_{thermal} is the thermal energy. The internal energy of a closed system can be expressed in terms of all extensive variables. For the case here, we can choose node charges and entropy as the extensive variables and the total differential of the internal energy becomes

$$\mathrm{d}E_{\text{internal}} = \sum_{i=1}^{N} \frac{\partial E_{\text{internal}}}{\partial q_i} dq_i + \frac{\partial E_{\text{internal}}}{\partial S} dS$$

where S is the entropy of the system. Since

$$\upsilon_i = \frac{\partial E_{\text{internal}}}{\partial q_i} = \frac{\partial U}{\partial q_i}, \quad T = \frac{\partial E_{\text{internal}}}{\partial S}$$

we can express the total differential of the internal energy as

$$\mathrm{d}E_{\text{internal}} = \sum_{i=1}^{N} \upsilon_i dq_i + TdS = \mathbf{v}^T \mathrm{d}\mathbf{q} + T\mathrm{d}S$$

The internal energy is conserved even an electron tunnels so $\mathrm{d}E_{\text{internal}} = 0$. It's convenient to use the form of Helmholtz free energy because the practical cases are performed at fixed temperature, not fixed entropy.

$$F_{\mathrm{H}} = E_{\text{internal}} - TS$$

Then

$$\mathrm{d}F_{\mathrm{H}} = \mathrm{d}E_{\text{internal}} - T\mathrm{d}S - S\mathrm{d}T = \mathbf{v}^T \mathrm{d}\mathbf{q} + T\mathrm{d}S - T\mathrm{d}S - S\mathrm{d}T = \mathbf{v}^T \mathrm{d}\mathbf{q} - S\mathrm{d}T$$

When the temperature is constant, changes in the Helmholtz free energy are equal to changes in the electrostatic energy of the system,

$$\Delta U = \Delta F_H = \int \mathbf{v}^T \mathrm{d}\mathbf{q}.$$

If we include voltage sources in the system, it's convenient to use Gibbs free energy

$$F = F_{\mathrm{H}} - \mathbf{v_v}^T \mathbf{q_v} = E_{\mathrm{internal}} - TS - \mathbf{v_v}^T \mathbf{q_v} = U + Q_{\mathrm{thermal}} - TS - W,$$

where W is the work done by the voltage sources. The work done by voltage sources also can be written as

$$W = \sum_{sources} \int V(t) I(t) dt$$

where $V(t)$ and $I(t)$ are the voltages and currents of the voltage sources. Generally voltage sources are constant so $\mathbf{v_v}^T \mathbf{q_v}$ is recovered. The differential of Gibbs free energy is

$$\mathrm{d}F = \mathrm{d}U + T\mathrm{d}S - T\mathrm{d}S - S\mathrm{d}T - \mathrm{d}W = \mathrm{d}U - S\mathrm{d}T - \mathrm{d}W.$$

For constant temperature,

$$\mathrm{d}F = \mathrm{d}U - \mathrm{d}W$$

and the change in free energy is defined as

$$\Delta F = F_f - F_i$$

where F_{f} is the free energy after tunnel event and F_{i} is before.

Using Fermi's golden rule to describe the tunneling rate from an initial state i to a final state f, also considering the change in free energy, the tunneling rate can be expressed as [21]

$$\Gamma_{i \to f}(\Delta F) = \frac{2\pi}{\eta} \left| T_{if} \right|^2 \delta(E_i - E_f - \Delta F)$$

where T_{if} is the tunnel transmission coefficient from state i with a certain momentum k_i to a state f with momentum k_f. The total tunnel rate from occupied states on one side of the barrier to unoccupied states on the other side is expressed by summation of all moments k_i and k_f.

$$\Gamma(\Delta F) = \frac{2\pi}{\eta} \sum_i \sum_f \left|T_{if}\right|^2 f(E_i)(1 - f(E_f))\delta(E_i - E_f - \Delta F)$$

where $f(E)$ is the Fermi-Dirac distribution describing the occupation probability of energy levels in equilibrium and $1 - f(E)$ is the probability of finding an empty state an electron can tunnel to.

$$f(E) = \frac{1}{1 + e^{\frac{E - E_F}{k_B T}}}$$

$$1 - f(E) = \frac{e^{\frac{E - E_F}{k_B T}}}{1 + e^{\frac{E - E_F}{k_B T}}} = \frac{1}{1 + e^{\frac{-E + E_F}{k_B T}}}$$

As long as T = 0, $f(E)$ = 1 if $E < E_F$ and $f(E)$ = 0 if $E > E_F$. Generally the variation of the tunnel transmission coefficient with energy and momentum is neglected and then $\left|T_{if}\right|^2$ is treated as a constant.

$$\Gamma(\Delta F) = \frac{2\pi}{\eta} \left|T_{if}\right|^2 \sum_i \sum_f f(E_i)(1 - f(E_f))\delta(E_i - E_f - \Delta F)$$

$D(E)\mathrm{d}E$ where $D(E)$ is the density of states means the number of electron states in a small energy interval dE and can be implemented.

$$\Gamma(\Delta F) = \frac{2\pi}{\eta} \left|T_{if}\right|^2 \int_{E_{c,i}}^{\infty} dE_i \int_{E_{c,f}}^{\infty} dE_f D_i(E_i) D_f(E_f) \cdot f(E_i)(1 - f(E_f))\delta(E_i - E_f - \Delta F)$$

where $E_{c,i}$ is the conduction band edge at the side where the electron exists initially, $E_{c,f}$ is the conduction band edge at the side where the electron tunnels to, $D_i(E)$ is the density of states at the initial side and $D_f(E)$ is at the final side. The product of these two Fermi functions defines a rectangular-like shape around the Fermi energies of initial and final side.

Since the main contribution of the integral comes from the narrow window, the densities of states appearing in the integral may be treated as constants and taken out the integral. The expression becomes

$$\Gamma(\Delta F) = \frac{2\pi}{\eta}|T|^2 D_i D_f \int_{E_c}^{\infty} f(E)(1 - f(E - \Delta F))dE ,$$

where the lower limit of the integration E_c is max($E_{c,i}$, $E_{c,f}$). Neglecting charging effect, a tunnel junction has an Ohmic *I-V* characteristic which means the current through the junction is proportional to the applied voltage across the junction. Now we can introduce the concept, tunnel resistance, which can be expressed as $I = \frac{V}{R_T}$. The tunnel resistance is defined as

$$R_T = \frac{\eta}{2\pi e^2 |T|^2 D_i D_f} .$$

Then

$$\Gamma(\Delta F) = \frac{1}{e^2 R_T} \int_{E_c}^{\infty} f(E)(1 - f(E - \Delta F))dE .$$

Since the Fermi level of metal lies into the conduction band, E_c is extended to $-\infty$. Integrating over the Fermi functions, we get the expression of orthodox single-electron tunnel rate which depends on the change in free energy,

$$\Gamma(\Delta F) = \frac{\Delta F}{e^2 R_T (e^{\frac{\Delta F}{k_B T}} - 1)}.$$

For zero temperature,

$$\Gamma(\Delta F) = \begin{cases} 0 & \Delta F \geq 0 \\ -\dfrac{\Delta F}{e^2 R_T} & \Delta F < 0 \end{cases}.$$

Tunnel events take place only if they reduce the free energy.

2-2 Electrostatic Energy

The charge configuration of a system determines the electrostatic energy so a tunneling event can change the overall energy condition. When the charge configuration changes, node voltages change. This change further affects the electrostatic energy. A tunneling event happens from a state of higher electrostatic energy to a state of lower electrostatic energy. The difference in energy is dissipated as heat. Assuming node charges as the independent variables, the total differential of the electrostatic energy is

$$\mathrm{d}U(\mathbf{q}) = \sum_{i=1}^{N} \frac{\partial U}{\partial q_i} dq_i = \sum_{i=1}^{N} v_i dq_i .$$

If a very small quantity of charge is added to node *j*, the differential change in electrostatic energy is

$$\mathrm{d}U = v_j dq_j = \sum_{i=1}^{N} C_{ji}^{-1} q_i dq_j \quad .$$

The energy needed to add charge *e* to node *j* is

$$ev_j + C_{jj}^{-1} \frac{e^2}{2}.$$

Assuming an electron tunneling from node *i* to node *f*, we can consider the situation from two stages. First, we remove an electron from node *i* and second, we add an electron to node *f*. The change of electrostatic energy to remove an electron from node *i* is

$$ev_i + C_{ii}^{-1}\frac{e^2}{2}.$$

After the electron is removed from node *i*, the node voltages also are changed. Assuming v_i' and v_f' the voltages of node *i* and *f* after the electron is removed from node *i* respectively,

$$v_i' = v_i + eC_{ii}^{-1},\ \ v_f' = v_f + eC_{if}^{-1}.$$

Thus, adding an electron on node *f* causes a change

$$-ev_f' + C_{ff}^{-1}\frac{e^2}{2} = -ev_f + (C_{ff}^{-1} - 2C_{if}^{-1})\frac{e^2}{2}.$$

Now we have the total energy change for an electron tunneling from node *i* to *f*. It can be expressed as

$$-e(v_f - v_i) + (C_{ii}^{-1} - 2C_{if}^{-1} + C_{ff}^{-1})\frac{e^2}{2}.$$

From this expression, we can notice that the change in electrostatic energy depends only on the voltage difference between the two nodes related to the tunneling event plus a term which is independent of the charge state of the system.

Chapter 3 Simulated Results and Discussion

3-1 Single-Electron Flip-Flop Memory

3-1-1 The First Design

The flip-flop design is very common for conventional SRAM. Two designs of single-electron flip-flop memory were proposed by Korotkov [22]. These designs are similar to the conventional circuits. The first is shown as Fig. 3-1. Like the conventional application, J_1 and J_2 are used as load. J_3, J_5 and C_1 form a single-electron transistor. J_4, J_6 and C_2 form another. The operation of the single-electron flip-flop memory is described in Table 1. The potential of SET and RESET determine the potential of OUT and OUT'.

3-1-1-1 Simulation of Basic Operations

MOSES developed by Ruby H. Chen was used for simulation. For the configuration of the circuit shown in Fig. 3-1, the tunnel resistances of J_1 to J_6 are 1 G_0 and the capacitance 1 C_0 where C_0 and G_0 are normalizing units. Capacitances of C_1 and C_2 are 3 C_0 and 20 C_0 for C_L. C_0 = 1 aF and G_0 = 1 uS are assumed. Temperature is 0.001 $e \times e /(k \times C_0)$ ($\cong 1.856^{\circ}K$) since $0^{\circ}K$ is not practical but $1.856^{\circ}K$ is reasonable if some cryo technologies are used. The dependency between actual and normalization value is expressed in Table 2.

The simulation sequences of operation are as below. First, the SET and RESET are both 0. Background charges of all islands are also 0. V_b always keeps at 5 e/C_0. Then SET is set to 5 e/C_0 and RESET keeps 0. V_{out} jumps to a higher potential than V_{out}' as described in the operation

table. After 350 C_0/G_0, SET and RESET are both set to 0. After 30 C_0/G_0, RESET is set to 5 e/C_0 and SET 0. Potential of V_{out} and V_{out}' switches and V_{out}' has a higher potential than V_{out}. After 350 C_0/G_0, SET and RESET are both set to 0. After 30 C_0/G_0, SET is set to 5 e/C_0 and RESET 0. The time variations of SET, RESET, V_{out} and V_{out}' are shown in Fig. 3-2.

3-1-1-2 Evaluation for Different Load

From the simulation above, we know the device works as the operation table but it shows some weak performances. First, it has poor retention performance. When SET and RESET are both set to 0, the potential difference between V_{out} and V_{out}' becomes smaller and smaller rapidly. This means it can't hold the correct information for a long time. Second, from the output waveform of V_{out} and V_{out}', we can observe the potential difference between "high" and "low" level is not obvious. This implies sense amplifiers should be used if this design is chosen as a memory device. From Fig. 3-2, it is suspected that V_b pulls V_{out} and V_{out}' to a similar level when SET and RESET are 0. Therefore the potential difference between V_{out} and V_{out}' is not anymore. Since J_1 and J_2 are used as load, some investigations for the tunnel resistances of J_1 and J_2 can be made to check the influence.

The simulation sequences of operation are as below. First, the SET and RESET are both 0. Background charges of all islands are also 0. V_b always keeps at 5 e/C_0. Then SET is set to 5 e/C_0 and RESET keeps 0. After 350 C_0/G_0, SET and RESET are both set to 0 to check the retention performance. The tunnel resistances of J_3 to J_6 are 1 G_0 and the

capacitance of J_1 to J_6 are 1 C_0 where C_0 and G_0 are normalizing units. Capacitances of C_1 and C_2 are 3 C_0 and 20 C_0 for C_L. C_0 = 1 aF and G_0 = 1 uS are assumed. Temperature is 0.001 e×e /(k×C_0). The tunnel resistances of J_1 to J_2 are set as 1, 0.5, 0.1, 0.05, 0.01 and 0 G_0 so total 6 times of simulation are done . The time variations of SET, RESET, V_{out} and V_{out}' are shown in Fig. 3-3.

The simulation results show the potential difference between V_{out} and V_{out}' is getting larger and larger when the tunnel conductance of J_1 to J_2 is getting smaller. This implies the information stored can be distinguished more easily if the tunnel conductance of J_1 to J_2 is small enough. With the tunnel conductance of J_1 to J_2 getting smaller, potential of V_{out} decreases because more potential drops on the tunnel of J_1 to J_2. Since the potential difference between V_{out} and V_{out}' is larger if the tunnel conductance of J_1 to J_2 is smaller, the information stored can last longer then potentials of V_{out} and V_{out}' are the same and stored information is destroyed. This shows better retention performance. Fig. 3-4 shows the relation between retention time and tunnel conductance of J_1 to J_2 where retention time is defined as the period the potential of V_{out} is larger than V_{out}'. In conventional SRAM cell, the impedance should be high to reduce the power consumption. From the assessment of different load here, larger load causes less tunneling. Therefore the data stored lasts for a longer time. Like the conventional flip-flop circuits, we hope the impedance of load is larger.

3-1-2 Another Complementary Design

The second design proposed by Korotkov is similar to the first but it's complementary. The complementary design uses single-electron transistors to replace the load tunnel junctions as shown in Fig. 3-5.

3-1-2-1 Simulation of Basic Operations

The operation also follows Table 1. The tunnel resistance of J1 to J8 is 1 G_0 and the capacitance 1 C_0 where C_0 and G_0 are normalizing units. Capacitance of C_1 to C_4 is 3 C_0 and 20 C_0 for C_L. C_0 = 1 aF and G_0 = 1 uS are assumed. Temperature is 0.001 $e \times e /(k \times C_0)$. Like the design in Fig. 3-1, the dependency between actual and normalized value is expressed in Table 2.

The simulation sequences of operation are as below. First, the SET and RESET are both 0. Background charges of all islands are also 0. Then SET is set to 5 e /C_0 and RESET keeps 0. V_{out} jumps to a higher potential. After a period of time, RESET is set to 5 e /C_0 and SET 0. Potential of V_{out} and V_{out}' switches and V_{out}' has a higher potential than V_{out}. From the output waveform of V_{out} and V_{out}' shown in Fig. 3-6, the difference between "high" and "low" is much improved compared to the design of Fig. 3-1. This means the information stored in the memory device can be read out correctly more easily. From this point of view, the characteristic of complementary design is better than the one shown in Fig. 3-1.

3-1-2-2 Evaluation for Different Load

Even the complementary design has better characteristic, it also has the same weak point like the previous design: poor retention performance.

The potential difference between V_{out} and V_{out}' is getting smaller when SET and RESET are both set to 0. Therefore can't keep the information for a long time. Some investigations for the tunnel resistances of J_1, J_2, J_3 and J_4 can be made to check the influence.

The simulation sequences of operation are as below. First, the SET and RESET are both 0. Background charges of all islands are also 0. V_b always keeps at 5 e/C_0. After 10 C_0/G_0, SET is set to 5 e/C_0 and RESET keeps 0 for 350 C_0/G_0. After that, SET and RESET are both set to 0 to check the retention performance. The tunnel resistances of J_5 to J_8 are 1 G_0 and the capacitance of J_1 to J_8 are 1 C_0 where C_0 and G_0 are normalizing units. Capacitances of C_1 to C_4 are 3 C_0 and 20 C_0 for C_L. C_0 = 1 aF and G_0 = 1 uS are assumed. Temperature is 0.001 e×e /(k×C_0). The tunnel resistances of J_1 to J_4 are set as 1, 0.5, 0.1, 0.05, 0.01 and 0 G_0 so total 6 times of simulation are done. The time variations of SET, RESET, V_{out} and V_{out}' are shown in Fig. 3-7.

The simulation results show the potential difference between V_{out} and V_{out}' is getting larger and larger when the tunnel conductance of J_1 to J_4 is getting smaller. This implies the information stored can be distinguished more easily if the tunnel conductance of J_1 to J_4 is small enough. With the tunnel conductance of J_1 to J_4 getting smaller, potential of V_{out} decreases because more potential drops on the tunnel of J_1 to J_4. Since the potential difference between V_{out} and V_{out}' is larger if the tunnel conductance of J_1 to J_4 is smaller, the information stored can last longer then potentials of V_{out} and V_{out}' are the same and stored information is destroyed. This shows better retention performance. Fig. 3-8 shows the relation between retention time and tunnel conductance of J_1 to J_4 where retention time is

defined as the period the potential of V_{out} is larger than V_{out}'. Like the conventional flip-flop circuits, we hope the impedance of load is larger.

3-2 Electron Trap Memory

3-2-1 An Electron Box

In chapter 1, the electron box is introduced but actually an electron box can't be used as a memory device. Here is the result of simulation for further understanding. The circuit of an electron box shown in Fig. 1-2 can be expressed as Fig. 3-9. Fig. 3-10 shows the charge vs. bias voltage characteristic. The tunnel resistance of J_1 is 1 G_0 and the capacitance 1 C_0 where C_0 and G_0 are normalizing units. Capacitance of C_1 is 1 C_0. C_0 = 1 aF and G_0 = 1 uS are assumed. Temperature is 0.001 $e \times e /(k \times C_0)$. We can observe the characteristic shows a staircase property and the island charge depends on the bias voltage. This is not the behavior of a memory device since the contents of the cell are completely controlled by the external voltage. That is, it lacks internal memory.

3-2-2 Simulation of An Electron Trap Memory

The simplest way to improve the structure of the electron box is to use two tunnel junctions connected in series to show the property of a memory device. However, using more tunnel junctions is beneficial for the control of information storage. An idea was proposed by Nakazato and Ahmed [23] like Fig. 3-11. Since it traps electrons to present "0" and "1", it's called "electron trap memory".

The characteristic of charge vs. bias voltage is shown in Fig. 3-12. The tunnel resistance of J_1 to J_4 is 1 G_0 and the capacitance 1 C_0 where C_0

and G_0 are normalizing units. Capacitance of C_1 is 1 C_0. C_0 = 1 aF and G_0 = 1 uS are assumed. Temperature is 0.001 e×e /(k×C_0). We can observe the characteristic shows a hysteresis property therefore we can store information. For example, if we increase Vg from 0 to 2.5 e/C_0, the charge stored in I_1 (island 1) becomes 1. If we decrease V_g from 2.5 to 0 e/C_0, the charge stored in I_1 (island 1) keeps 1. Obviously this shows the property of a memory device.

3-2-3 A Single-Electron Random-Access Memory

This structure of Fig. 3-11 is often used for further improvements because of its simplicity for fabrication. A single-electron random-access memory array proposed by Ioannis Karafyllidis [24] uses this structure and simulates the read write operation as a random-access memory. The circuit of electron trap he used is a 6-island structure like Fig. 3-13. It has more tunnel junctions compared to Fig. 3-11 therefore has better control to the electrons stored.

3-2-3-1 Simulation of the 6-Island Structure

MOSES, not SIMON used by Ioannis Karafyllidis, was used for the simulation this time. The parameters are set like what Ioannis Karafyllidis used. The tunnel resistance of J_1 to J_6 is 10 G_0 and the capacitance 1 C_0 where C_0 and G_0 are normalizing units. Capacitance of C_1 is 1 C_0. C_0 = 1 aF and G_0 = 1 uS are assumed. Temperature is 0.001 e×e /(k×C_0). When a positive V_g is applied, electrons are transported to the island I_1. How many electrons are transported depends on V_g and the parameters of the tunnel junctions. In this case, 3.75 e/C_0 is used for V_g to attract an electron to I_1 (write ‘1’) and –2.5 e/C_0 for rejecting the electron out I_1

(write ‘0’) as shown in Fig. 3-14. If V_g keeps 0 after writing ‘1’, the information keeps storing in I_1.

Ioannis Karafyllidis extends the application of this design to a random-access memory [24]. In conventional random-access memory, a cell which stores information is selected by activating the word line and bit line specified to this cell. Fig. 3-15 shows a typical array of conventional random-access memory. The design proposed by Ioannis Karafyllidis is like the conventional random-access memory. It uses two signals to activate the specified cell as shown in Fig. 3-16 so we can treat V_x and V_y as word line and bit line.

3-2-3-2 Simulation of the Single-Electron Random-Access Memory

The results simulated by MOSES are shown in Fig. 3-17. The tunnel resistance of J_1 to J_8, J_x and J_y is 10 G_0 and the capacitance 1 C_0 where C_0 and G_0 are normalizing units. Capacitance of C_1 is 1 C_0. C_0 = 1 aF and G_0 = 1 uS are assumed. Temperature is 0.001 $e \times e /(k \times C_0)$. The circuit is assumed to store an electron when V_g, V_x and V_y are activated but from the simulation results, it doesn’t always act like what we hope. From Fig. 3-17 we can observe something wrong when V_g = 10, V_x = –2.5 and V_y = 0 e/C_0. This is different from the result got from SIMON and this means the voltage setting should be fine-tuned further to make the circuit more stable.

3-2-3-3 To Improve the Original Design

To solve this problem, V_x and V_y are tuned to find the proper voltages to have a stable state. A statistical tool “Jump” is used for this evaluation.

Many times of simulation were done to have enough data to find the correlations of $V(7)$, V_g, V_x and V_y. The relationship is found that $V(7) = 0.03 + 0.203 \times V_g + 0.6 \times V_x + 0.201 \times V_y$ where $V(7)$ is the potential at I_7 (island 7). The F ratio shown in Fig. 3-18 means the influence on $V(7)$. Larger F ratio, bigger influence on $V(7)$.

From Fig. 3-18, Vg and V_x have much larger influence than V_y. That's why the device is written "1" when V_g and V_x are "high" but V_y is "low" in Fig. 3-17. The strong effect from V_x makes it necessary to set a much lower level than -2.5 e/C_0 as "low" of V_y. Table 3 shows the estimation for $V(7)$, V_g, V_x and V_y. The $V(7)$ when V_x is activated is much higher than when V_y is activated. From Table 3, $V_y = -7.5$ e/C_0 is a proper value to suppress the influence when Vx is "high". This is very different from the original setting -2.5 e/C_0. A modified design of this random-access memory is shown in Fig. 3-19. There is one additional tunnel junction for V_x to suppress the influence from V_x.

The statistical tool "Jump" is used again for this evaluation. The relationship between $V(7)$, V_g, V_x and V_y of this new circuit is found that $V(7) = 0.0488 + 0.294 \times V_g + 0.4224 \times V_x + 0.2876 \times V_y$ where $V(7)$ is the potential at I_7 (island 7). From the F ratio shown in Fig. 3-20 we can observe that V_x and V_y have closer weighting than the original circuit. This means we can set the voltages at a more reasonable level now.

The original design has another disadvantage. V_x and V_y have to keep at negative voltages when not activated. In a memory array, only the cell selected needs to be activated so most part of this array is not activated. For a 1 Giga-memory, let's assume there are 10^5 word lines and 10^4 bit lines. The original design has to supply voltages to so many word lines

and bit lines since the huge part of them are not activated. This causes very severe power consumption.

Table 4 shows the new setting of voltages for the modified circuit. 0 is chosen as “low”, 2 e/C_0 as “high” for V_x and V_y, 3 e/C_0 as “high” for V_g. When V_x and V_y are not activated, the voltage keeps 0. This helps much about power consumption.

Table 5 is a comparison of different designs for specified conditions. The parameters of the circuits used in simulation follow those used in Fig. 3-16 and 3-19. Simulation duration is 5000 C_0/G_0 to guarantee it’s long enough to test the stability. Temperature is 0.001 e×e /(k×C_0) where C_0 = 1 aF and G_0 = 1 uS. 50 times of simulation have been done for each condition. For the original design, because of the influence from V_x, errors occur when V_x = “high” and V_y = “low”. Fig. 3-21 shows the modified circuit works like we hope. Writing “1” only when V_g, V_x and V_y are “high”.

3-2-3-4 Function and Speed Comparison

The modified design can operate more stable than the original but we may sacrifice the writing speed since the potential of V_g, V_x and V_y are chosen to work stably. Fig. 3-22 shows the speed comparison of different designs for writing “1”. The upper figure is original design and lower one is the modified. The parameters of the circuits used in simulation follow those used in Fig. 3-16 and 3-19. Temperature is 0.001 e×e /(k×C_0). 30 times of simulation have been done for each design. Since “1” is written in this simulation, voltages are set as V_g = 7.5 e/C_0, V_x = V_y = 0 for the original design and V_g = 3 e/C_0, V_x = V_y = 2 e/C_0 for the improved one. C_0

= 1 aF and G_0 = 1 uS are assumed. From this comparison, the writing time of the original design is roughly 20 ~ 100 C_0/G_0 and 200 ~ 1000 C_0/G_0 for the modified one. The modified circuit is slower than the original for an order. This is a compromise since the original design has function problems. When V_g and V_x are "high" but V_y is "low", original design writes wrong information and in the field of memory testing, function failures are always important than speed failures so the sacrifice of speed for correct function is acceptable.

For writing "0", V_g = –5 e/C_0 is selected to eject the electron stored in I_1. Fig. 3-23 shows the time variation of V_g and $Q(1)$ which means the charges stored in island 1. V_x and V_y are 2 e/C_0 to select this cell and V_g is 3 e/C_0 to write "1" into this cell. After the "1" is stored, V_g = 3 e/C_0 again doesn't change the information. Then V_g is set to –5 e/C_0 to write "0" into this cell. After the "0" is stored, V_g = –5 e/C_0 again doesn't change the data stored.

3-2-4 Correlations between Junction, Temperature and V_g of an Electron Trap Memory

Christoph Wasshuber did some comparative studies for several types of single-electron memories [25] including flip-flop, electron trap, ring memory, background-charge-independent memory, single island memory, multiple island memory and T-memory. The maximum operation temperature of each single-electron memories is mentioned there. Here the further correlations between number of junctions, temperature and V_g are discussed for the electron trap memory.

For electron trap memory as Fig. 3-13, if the capacitance is 1 C_0, tunnel conductance 10 G_0 and the potential of V_g used for writing "1" is 3.75 e/C_0 (like Fig. 3-14) where C_0 = 1 aF and G_0 = 1 uS are assumed, the maximum operation temperature is 0.004 e×e /(k×C_0) ($\cong$ 7.5°K). This is different from the simulation results mentioned by Christoph Wasshuber which show the maximum operation temperature of electron trap memory is 74°K. That's because the capacitances are assumed as 0.35 aF. If the capacitances are set as his evaluation, the same maximum temperature can be observed but the potential of V_g for writing "1" has to be pulled up to 9 e/C_0. This is reasonable because the coulomb blockade is much stronger. The number of tunnel junctions also is a factor affecting the maximum operation temperature because more tunnel junctions imply higher tunneling barrier. After inserting a tunnel junction to form a 7-junction electron trap, if the capacitance, tunnel conductance and the potential of V_g follow the settings before, the maximum operation temperature is 0.011 e×e /(k×C_0) ($\cong$ 20.4°K) but the potential of V_g has to be increased further since the number of tunnel junctions increase.

If the potential of V_g, temperature of operation and the number of tunnel junctions are all considered together, it becomes more complicated. Fig. 3-24 shows the relationships between temperature of operation, potential of V_g and number of tunnel junctions. All of the simulations are based on electron trap memory like Fig. 3-13. The capacitances are 1 C_0 and tunnel conductance 10 G_0 where C_0 = 1 aF and G_0 = 1 uS are assumed. The simulation time is chosen as 1000 C_0/G_0. 20 times of simulations are done for each dot in Fig. 3-24 to make sure the device can

work correctly at this setting. The lowest temperature for simulation is 0.001 e×e /(k×C_0). The V_g has to be set properly to let the device work correctly. If V_g is too small, no electrons can be trapped in I_1, like Fig. 3-25. If V_g is too large, more than one electron can be trapped in I_1, like Fig. 3-26. If the temperature is out of the proper range of the device, it becomes very difficult to set a proper potential of V_g, like Fig. 3-27 because thermal fluctuation makes the electrons in I_1 unstable. These results are all considered as failures.

For 6-tunnel-junction electron trap memory, the device can work well if the potential of V_g is among 3 to 3.9 e/C_0 when the temperature is 0.001 e×e /(k×C_0). If the temperature is raised to 0.005 e×e /(k×C_0), the proper range of V_g is from 2.9 to 3.6 e/C_0 because the thermal fluctuation reduces the effect of coulomb blockade. The V_g goes down further when the temperature is increased. Finally, if the temperature is higher than 0.009 e×e /(k×C_0), it's very difficult to set a good V_g to let the device work correctly because thermal fluctuation makes the electrons in I_1 unstable. Therefore the maximum temperature of operation for 6-tunnel-junction electron trap memory is 0.009 e×e /(k×C_0) (16.7°K) if V_g is considered.

Comparing 6 and 7-tunnel-junction electron trap memories, 7-tunnel-junction electron trap memory can work at higher temperature because of better immunity to thermal fluctuation. But it needs higher potential of V_g compared to 6-tunnel-junction devices if at the same temperature because there is one more junction to overcome to store an electron in I_1. At higher temperature, the working range of V_g decreases

because the thermal fluctuation makes the device unstable. Some electrons may be in I_1 even the V_g is small but this is not controlled by V_g but thermal fluctuation. Therefore the device is not functional under this situation. Fig. 3-24 shows the relationships between potential of V_g and temperature for 6, 7 and 8-tunnel-junction electron trap memories. The area encircled by the dots of each plots indicates the working area of 3 different kinds of electron trap memories if V_g and temperature are considered at the same time.

3-3 Background-Charge-Independent Memory

The background-charge-independent memory was proposed by Likharev and Korotkov [26]. The circuit is shown in Fig. 3-28. C_1, J_2 and J_3 construct a single-electron transistor [27]. The reason why this design is background-charge-independent is because it doesn't detect the present of charges but check the relative change of charges. When the charges stored in I_1 change, current oscillations occur and are amplified by an *FET*. The *FET* which is used as an amplifier can be shared by several memory cells.

3-3-1 Simulation of Basic Operations

To write "1" into the cell, a positive voltage V_d is applied to the word line and similar negative voltage $-V_d$ to both bit lines. Then some fraction of the applied control voltage $2V_d$ drops between the floating gate and the word line and exceeds the threshold voltage. The charge on the floating gate increases because the electrons tunnel to the word line as shown in Fig. 3-29. Writing "0" is similar but the voltage polarity is different. A negative voltage $-V_d$ is applied to the word line and a positive voltage V_d

to both bit lines. The results of simulation are shown in Fig. 3-30. In the simulation, the tunnel resistance of J_1 to J_3 is 1 G_0 and the capacitance 1 C_0 where C_0 and G_0 are normalizing units. Capacitance of C_1 is 1 C_0. C_0 = 1 aF and G_0 = 1 uS are assumed. Temperature is 0.001 $e \times e /(k \times C_0)$. Word line and bit line voltages are shown in Fig. 3-29 and 3-30 for writing "1" and "0" respectively.

To read "1" or "0", a negative voltage $-V_d$ is applied to the word line and a positive voltage V_d to both bit lines. A small difference of voltage also exists between bit line+ and bit line–. The parameters of capacitance, tunnel conductance and temperature for simulation are as mentioned above. The word line voltage used for reading is –2 e/C_0, 2.1 e/C_0 for bit line+ and 1.9 e/C_0 for bit line–. The results of simulation for reading "1" are shown in Fig. 3-31. The current oscillation can be observed. The results of simulation for reading "0" are shown in Fig. 3-32 and show no current oscillation.

3-4 Turnstile Based Single-Electron Memory

Geerligs suggested the design of single-electron turnstile [28]. This design is shown in Fig. 3-34. When V_b is zero, electrons can be transferred to the central island by increasing the gate voltage. The electrons can be from either right or left side of this circuit. Contrarily, electrons can be ejected from the central island to either right or left side of the circuit by lowering the gate voltage. With a bias voltage V_b applied, the direction where the electrons are from can be controlled. What Fig. 3-33 shows is a symmetric turnstile circuit since the capacitance of each tunnel junction is the same.

Casper Lageweg uses the turnstile circuit as a basis and modifies this circuit. His main idea is to perform the logic operations by transporting electrons depending on different control signals like enable, clock and data. The modified design is shown in Fig. 3-34. When “enable” is high, the circuit is activated and can operate normally. “data” means the data will be stored in this memory element. “clock” can be used to synchronize with other devices since V_{out} also depends on “clock”.

3-4-1 Simulation of Basic Operations

The simulation results are shown in Fig. 3-35. For writing “0”, when “enable” is “high”, “clock” is “high” and “data” is “low”, V_{out} is “low”. After the information is stored, “clock” goes “low” but “enable” keeps “high” to keep the device activated so V_{out} is still “low”. For writing “1”, when “enable” is “high”, “clock” is “high” and “data” is “high”, V_{out} is “high”. After the information is stored, “clock” goes “low” but “enable” keeps “high” to keep the device activated so V_{out} is still “high”. These results show the properties of a memory device. In the simulation, the tunnel resistance of J_1 to J_3 is 10 G_0 and the capacitance is 2.5 C_0 for J_1, 3 C_0 for J_2 and J_3 where C_0 and G_0 are normalizing units. Capacitance of C_1 is 1.5 C_0, 1 C_0 for C_2 and 2.5 C_0 for C_3. C_0 = 1 aF and G_0 = 1 uS are assumed. Temperature is 0.001 $e \times e / (k \times C_0)$. “low” is 0 for “enable”, “clock” and “data”. “high” is 0.1 e/C_0 for “data” and 0.4125 e/C_0 for “enable” and “clock”.

3-4-2 Further Study

From the simulation of basic operations, it is observed that V_{out} may be incorrect when “enable” is “high”, “clock” is “high” and “data” is

“low”. The input is supposed to write “0” but sometimes it becomes writing “0”. This indicates the inputs of “enable” and “clock” need to be controlled and shouldn’t last at “high” too long. “clock” is of course a better choice than “enable” to control its width since “enable” should keep at “high” whenever the device is selected. An evaluation is done to check the width of “clock”. At first, “enable”, “clock” and “data” keep “low” then “enable” goes “high” after 10 C_0/G_0. “clock” also goes “high” after 10 C_0/G_0 then V_{out} is checked when to change from “low” to “high”. From Fig. 3-36, the “clock” shouldn’t keep at “high” longer than 0.4 C_0/G_0. Because C_0 = 1 aF and G_0 = 1 uS are assumed, the “clock” shouldn’t keep at “high” longer than 0.4ps. Therefore the frequency of “clock” should be higher than 1/0.8ps = 1.25 THz. This guarantees the correct function of the turnstile based single-electron memory.

Chapter 4 Conclusions and Outlook

4-1 Conclusions

In this thesis, a simulation tool MOSES which is based on Monte Carlo simulation method is used for simulating several types of single-electron memories including single-electron flip-flop memory, electron trap memory, background-charge-independent memory and turnstile based single-electron memory.

Besides the simulation of basic operation, the characterizations are also discussed. For the single-electron flip-flop memory, the complementary type shows better characterization than another. V_{out} and V_{out}' can be distinguished more easily. The load resistance is discussed to improve the retention problem. Larger load resistance shows better performance.

A single-electron random-access memory array using the improved design of the electron trap memory as its elements has been presented in this thesis. MOSES using Monte Carlo simulation method shows that selective writing can be done and selective reading also can be operated by sensing the charge at memory island using an electrometer. The most important is the new design improves several disadvantages of the original design including operation stability and power consumption. Based on the same comparison level, the error rate is improved from 78% to 0%. The voltages used for bit-lines, word-lines and V_g are modifies to have lower power consumption for all memory array. The correlations between junction number, temperature and V_g are also discussed.

For the turnstile based single-electron memory, the width of clock wave correlates to the stability of this device. It is simulated to define the longest clock width. Therefore the restriction about minimum working frequency of the turnstile based single-electron memory is known. Only under this condition, this device can work without functional failures.

4-2 Future Work

Because the compiler used by Ruby H. Chen, the developer of MOSES, is different (WATCOM) from the one I used (Lahey), the original source code is modified to run correctly on Lahey but the functions used for graph drawing have being taken out during compiling. Further improvements of the program to draw graphs can be studied.

Room temperature single-electron memory is an important topic for the application of this future technology [29] [30]. Further characteristic study of the device focusing on the field is also a topic for future work. This correlates directly to the size of “island” so the problems about fabrication can also be discussed.

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Table 1. Operation of single-electron flip-flop memory

Reset	*Set*	*Vout (n+1)*
0	0	*Vout (n)*
0	1	1
1	0	0
1	1	Not used

Table 2. Normalization table

Normalized Quantity		Normalization Factor		
Description	Symbol	Symbol	Value	Units
Capacitance	C	C_0	1.0	aF
Conductance	G	G_0	1.0	μS
Charge	Q	q	1.0	e
Energy	E	$e \times e / C_0$	0.16	eV
Potential	U	e / C_0	0.16	V
Temperature	T	$e \times e / (k \times C_0)$	1856.15	°K
Time	t	C_0/G_0	1.0	psec
Physical Parameters				
Description		Symbol	Value	Units
Boltzmann's constant		k	8.62×10-5	eV/°K
Electronic charge		e	1.6×10-19	coul.

Table 3. Correlation of V(7), Vg, Vx and Vy

V(7)	Vg	Vx	Vy	remark
1.5513699	7.5	0	0	Vx and Vy activated
-0.450431	7.5	-2.5	-2.5	Vx and Vy not activated
1.0488249	7.5	0	-2.5	Vx activated
0.0521141	7.5	-2.5	0	Vy activated
0.9483159	7.5	0	-3	
0.8478069	7.5	0	-3.5	
0.7472979	7.5	0	-4	
0.6467889	7.5	0	-4.5	
0.5462799	7.5	0	-5	
0.4457709	7.5	0	-5.5	
0.3452619	7.5	0	-6	
0.2447529	7.5	0	-6.5	
0.1442439	7.5	0	-7	
0.0437349	7.5	0	-7.5	

Table 4. Voltage setting for the modified circuit

Vg	Vx	Vy	definition
3	2	2	Vx and Vy activated
3	0	0	Vx and Vy not activated
3	2	0	Vx activated
3	0	2	Vy activated

Table 5. The comparison of different designs for specified conditions

original design (fig. 3-12)			
conditions			error rate
Vg = "high"	Vx = "low"	Vy = "low"	0
	Vx = "low"	Vy = "high"	0
	Vx = "high"	Vy = "low"	78%
	Vx = "high"	Vy = "high"	0
modified design (fig. 3-15)			
conditions			error rate
Vg = "high"	Vx = "low"	Vy = "low"	0
	Vx = "low"	Vy = "high"	0
	Vx = "high"	Vy = "low"	0
	Vx = "high"	Vy = "high"	0

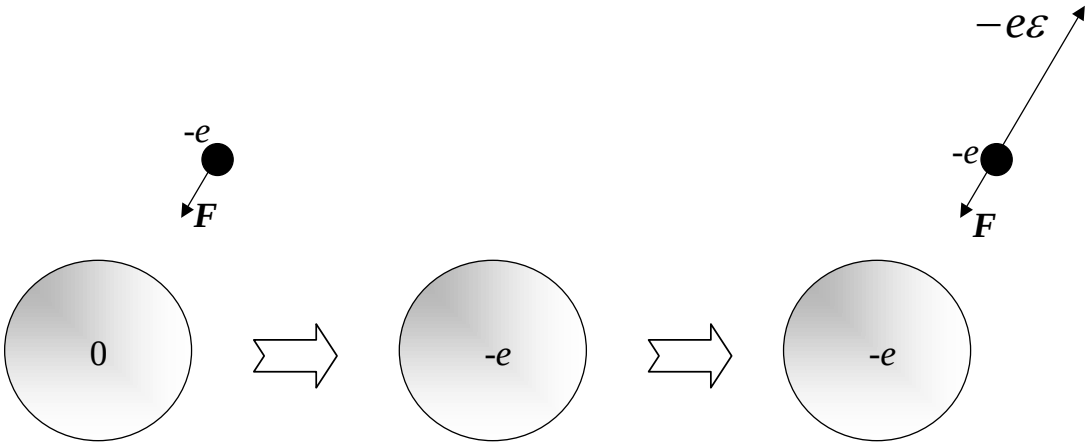


Fig. 1-1. The concept of single-electron control. After adding a electron from outside, the electric field ε may prevent the following electrons.

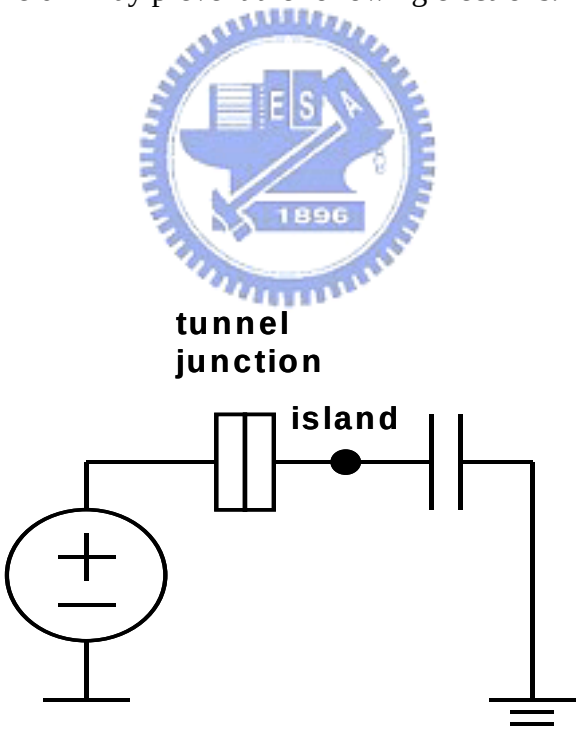


Fig. 1-2. A single-electron box.

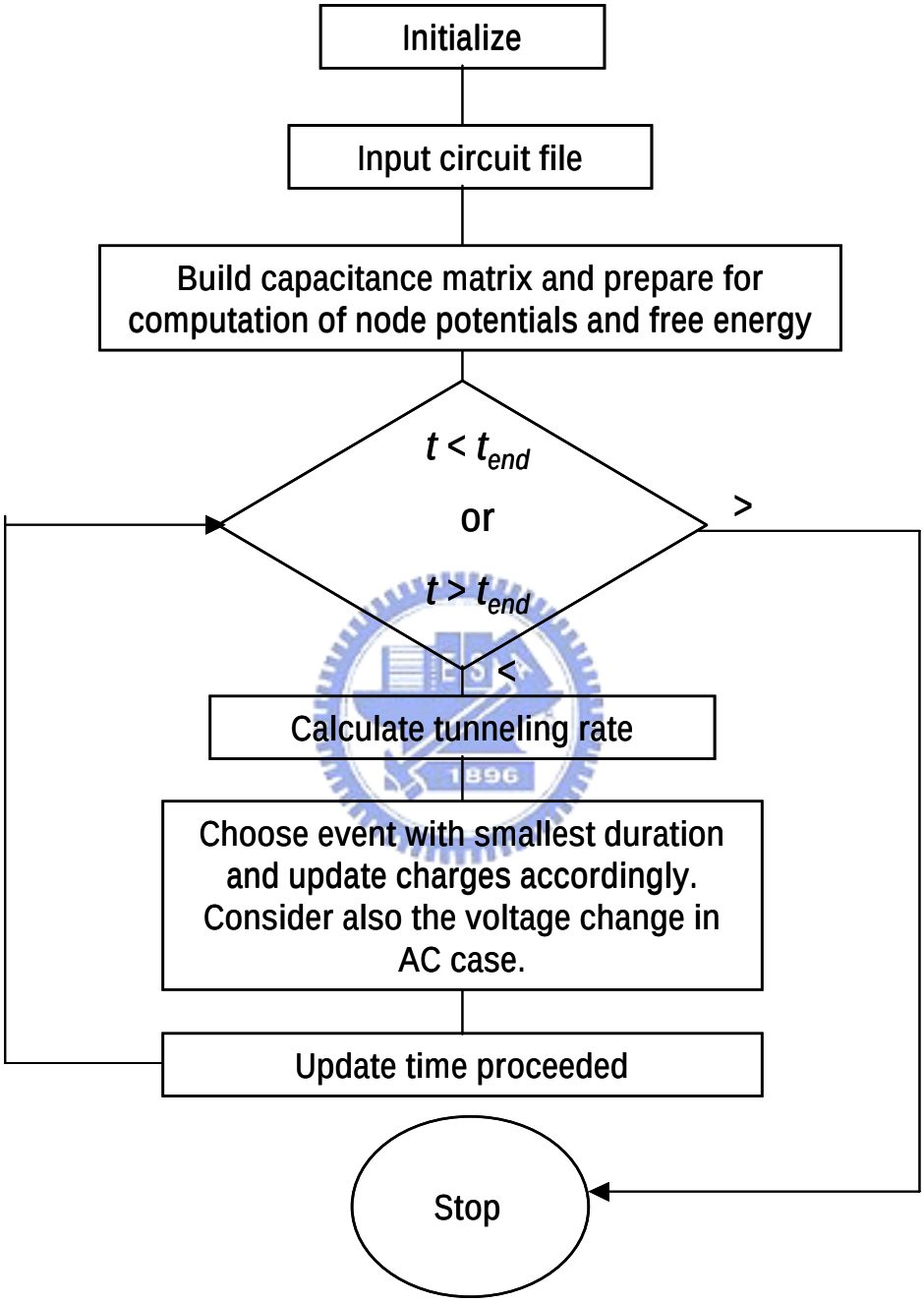


Fig. 1-3. Flow chart of Monte Carlo method for single-electron simulation

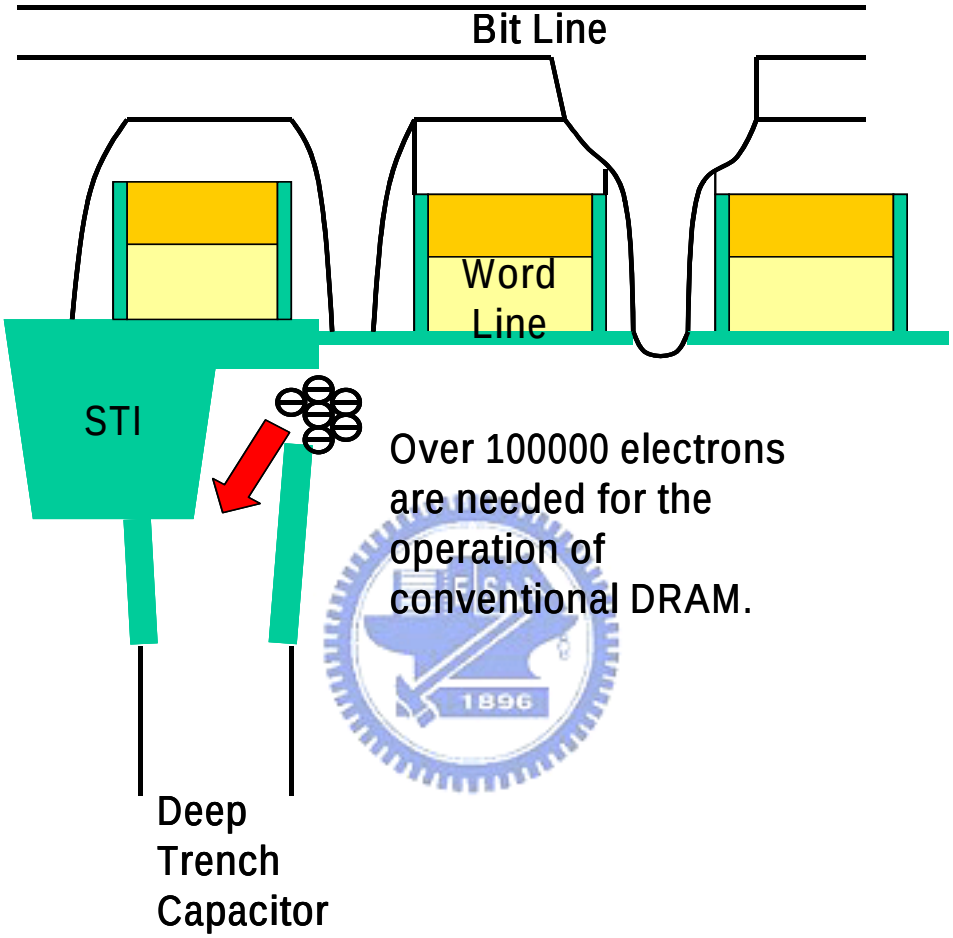


Fig. 1-4. A trench type memory cell of the conventional DRAM. Hundred thousands of electrons flowing in and out the deep trench are necessary for the normal operations.

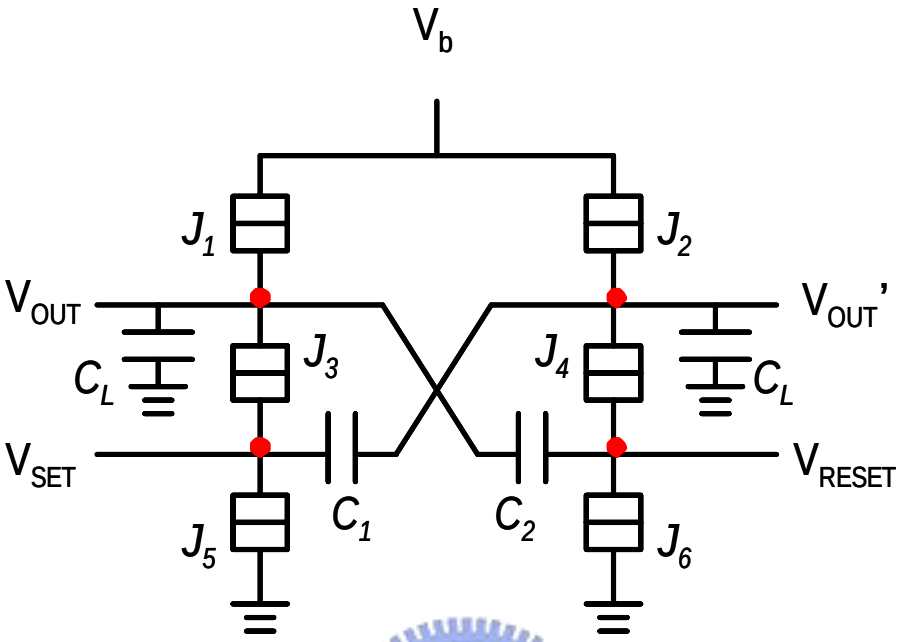


Fig. 3-1. Single-electron flip-flop memory

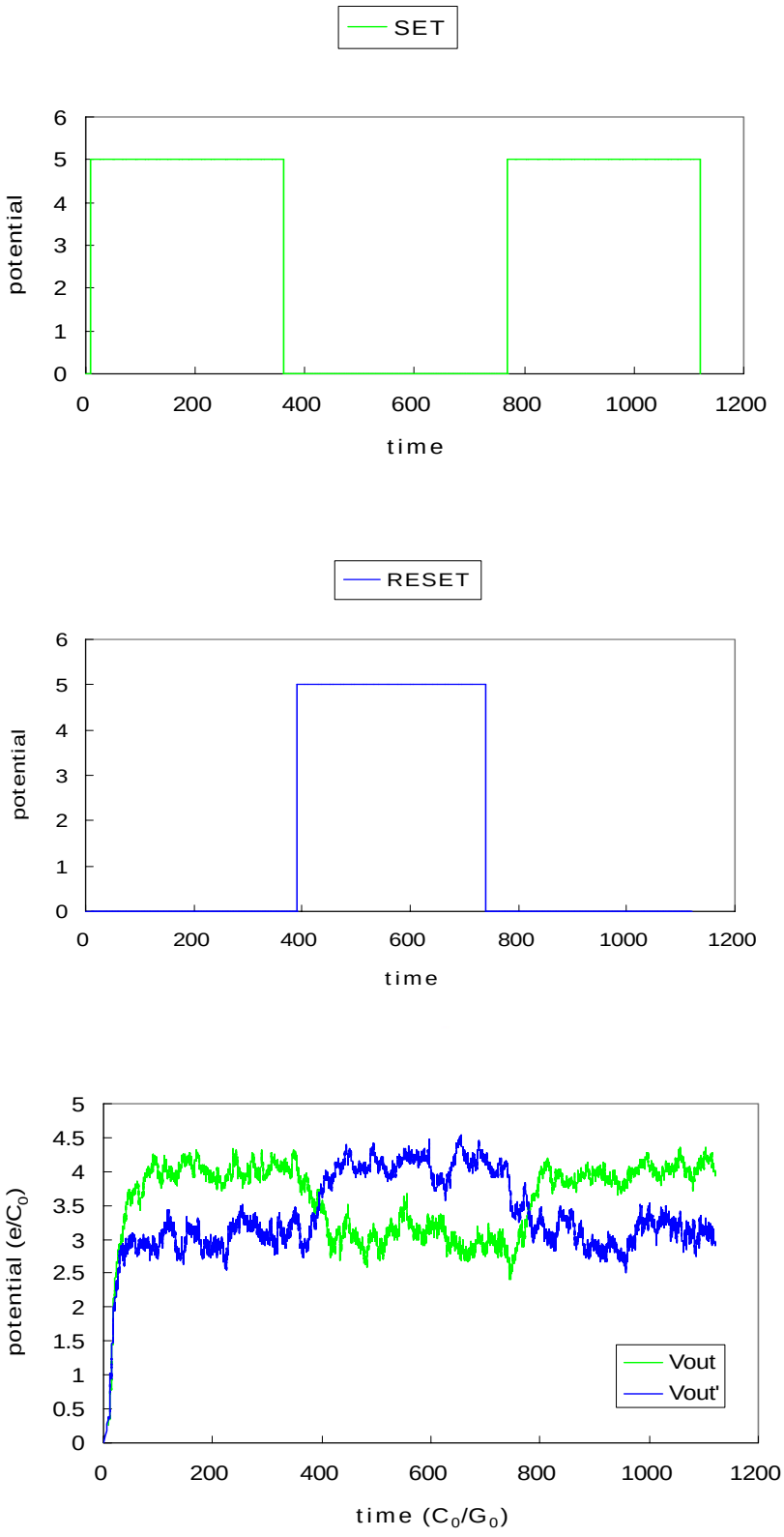
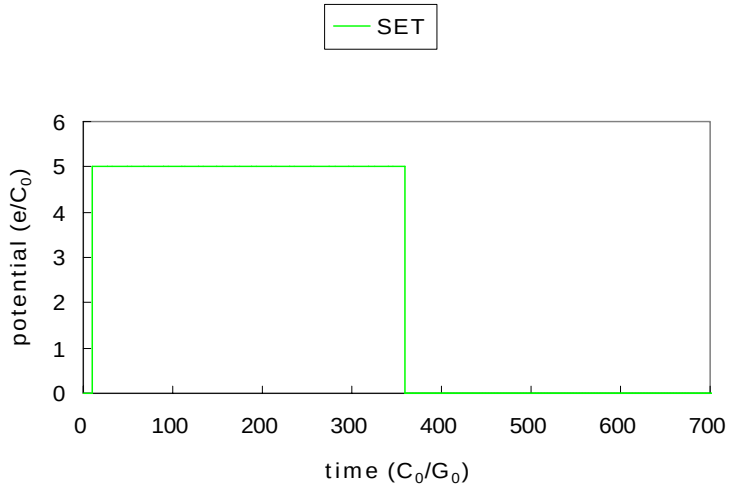
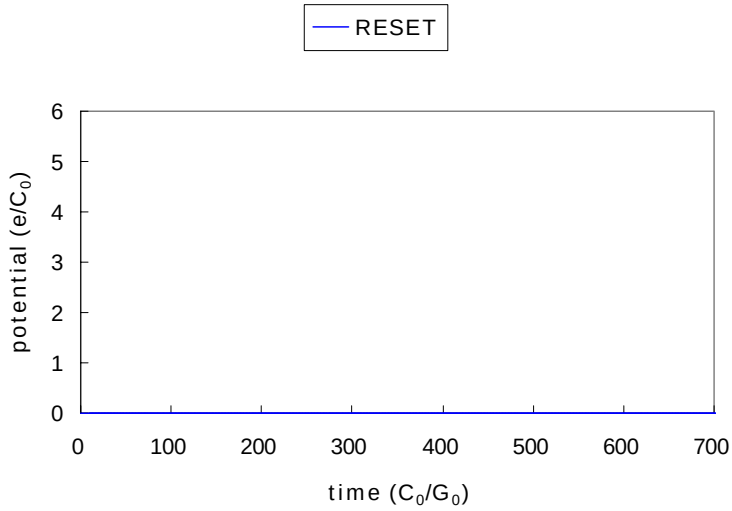
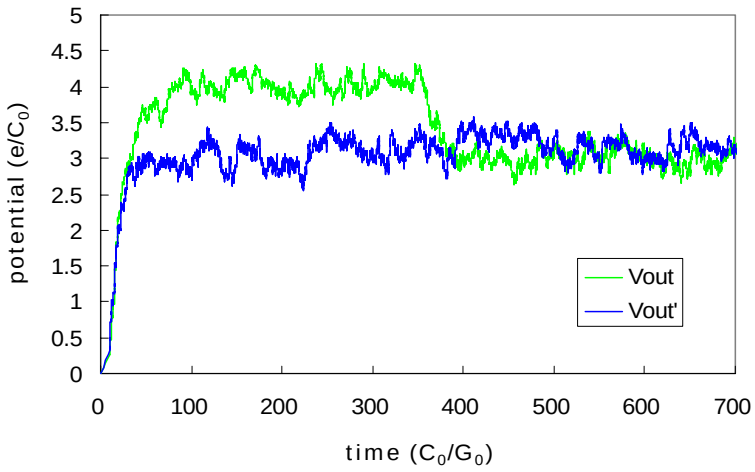


Fig. 3-2. Input and output conditions of a single-electron flip-flop memory (time unit: ps)





Tunnel conductance of J_1 & J_2: $1G_0$



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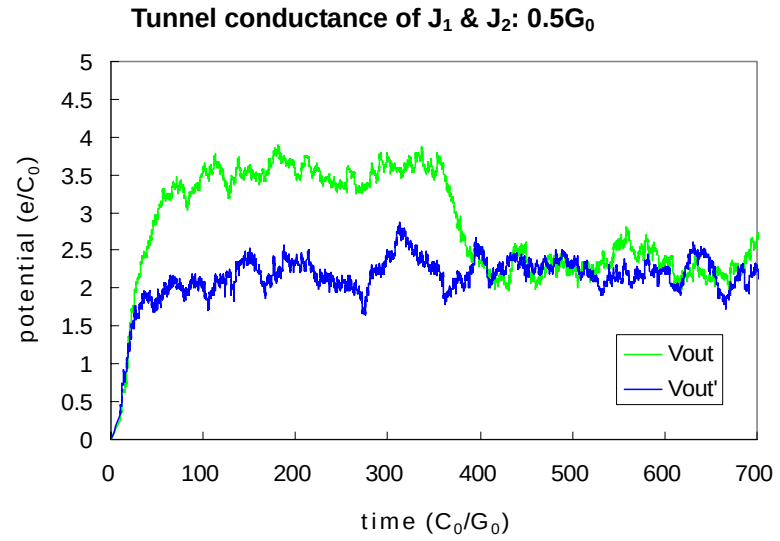

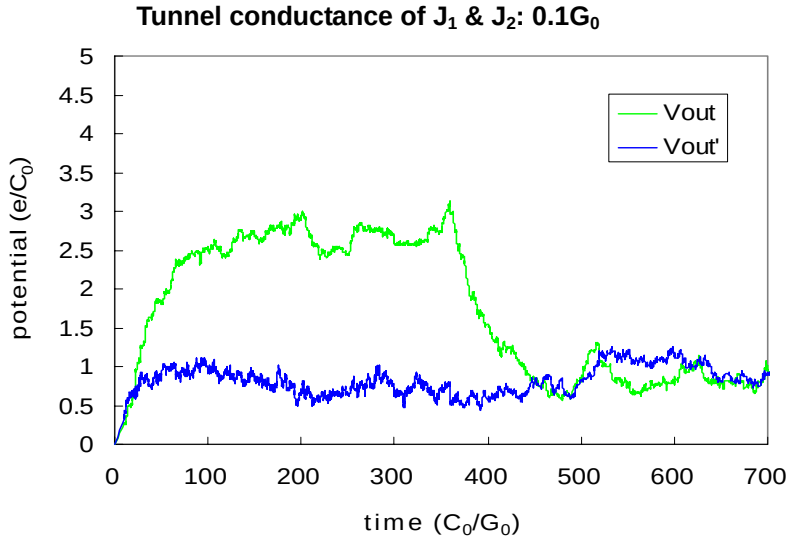

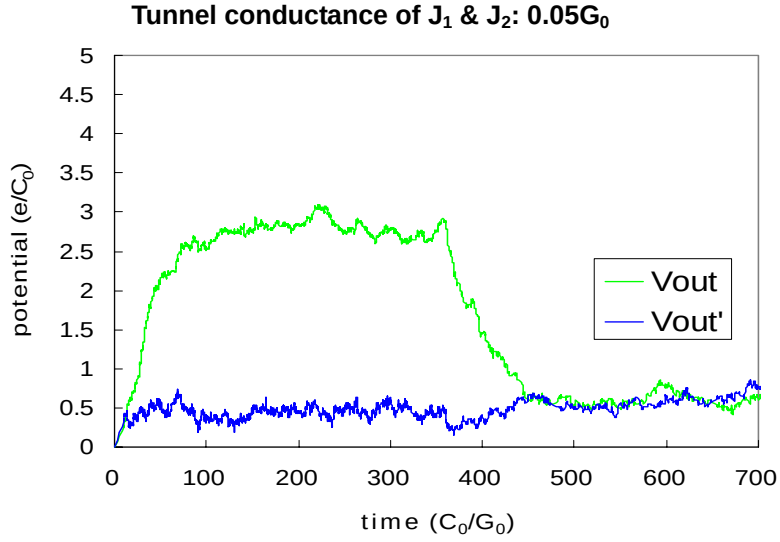

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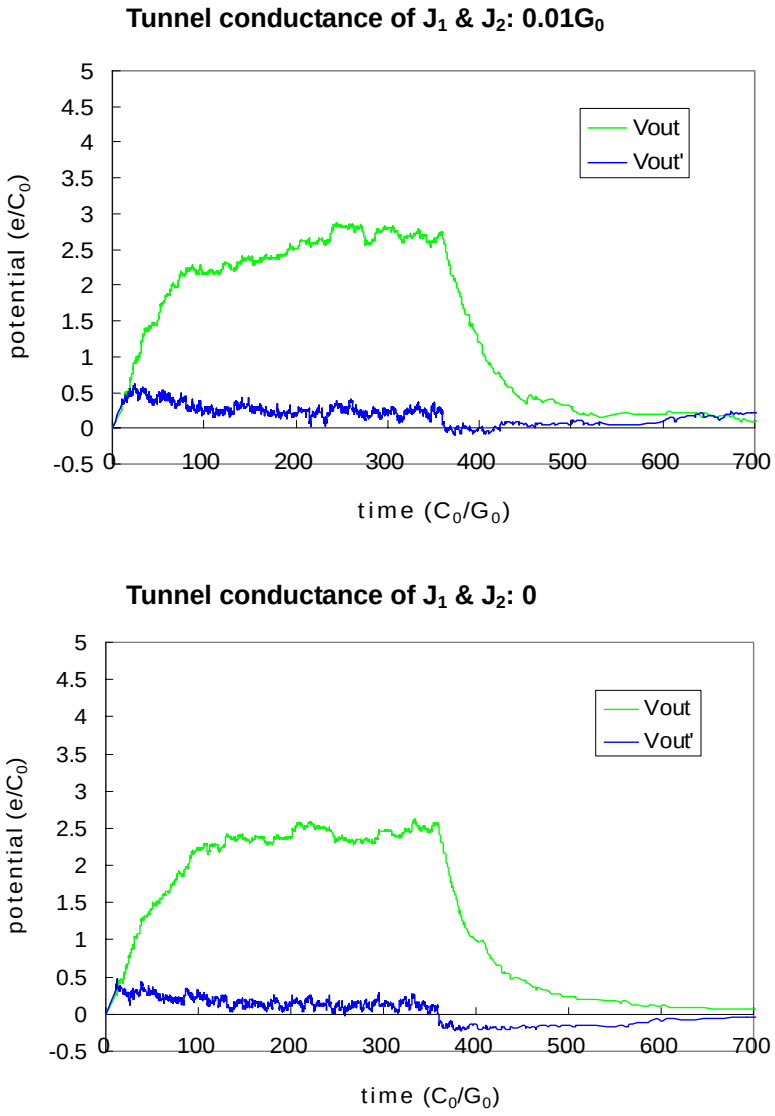


Fig. 3-3. V_{out} and V_{out}' of various tunnel conductance of J_1 & J_2 (time unit: ps)

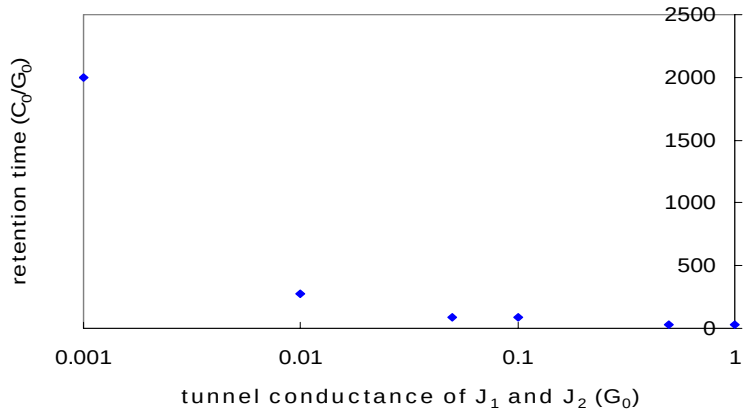


Fig. 3-4. Relation of retention time and tunnel conductance of J_1 & J_2 (time unit: ps)

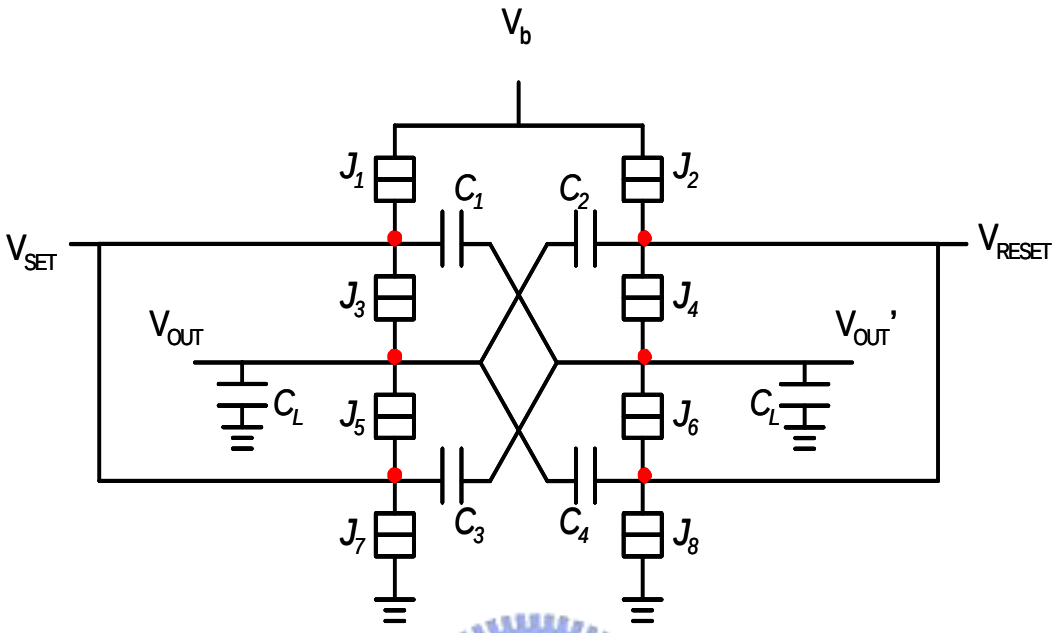


Fig. 3-5. Complementary design of a single-electron flip-flop memory

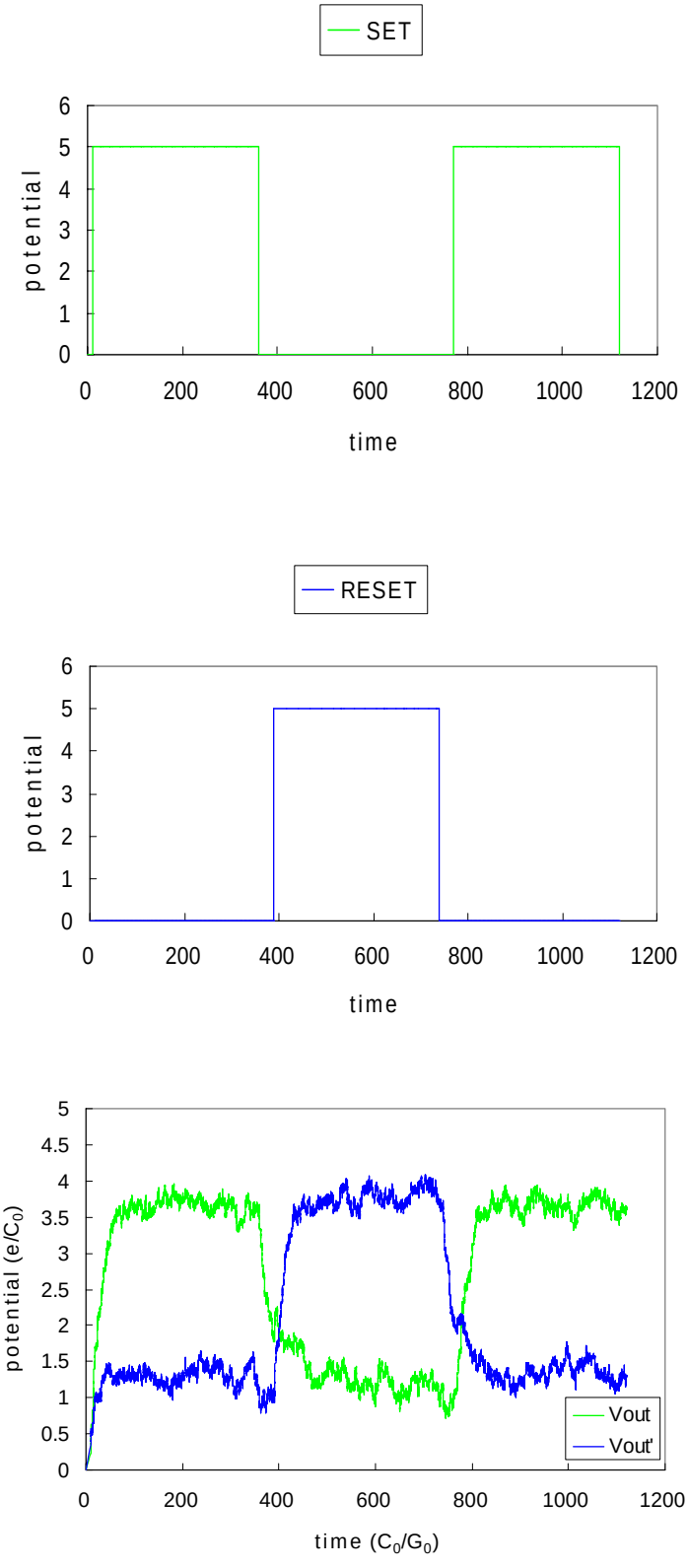
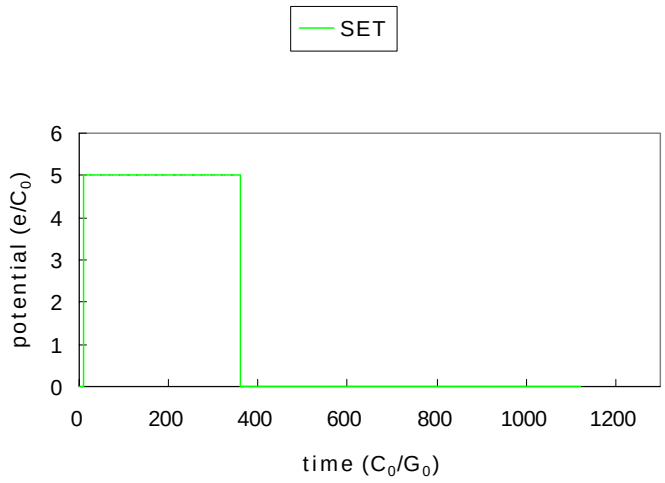
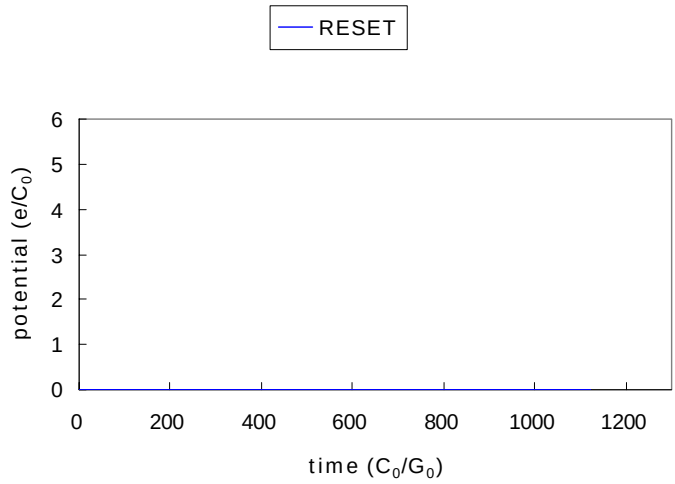
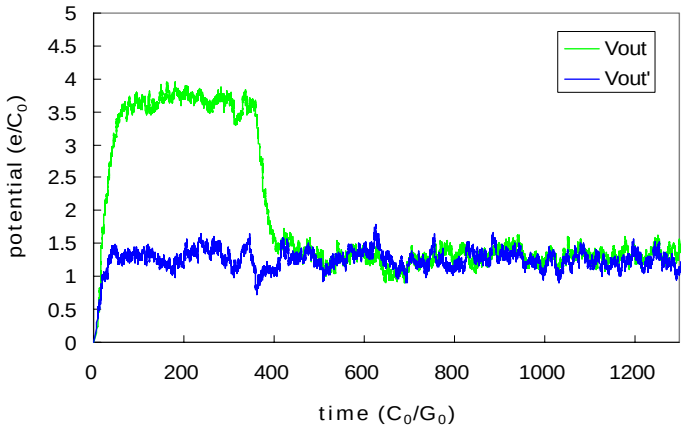


Fig. 3-6. Input and output conditions of a complementary single-electron flip-flop memory (time unit: ps)





Tunnel conductance of J_1, J_2, J_3 & J_4: $1G_0$



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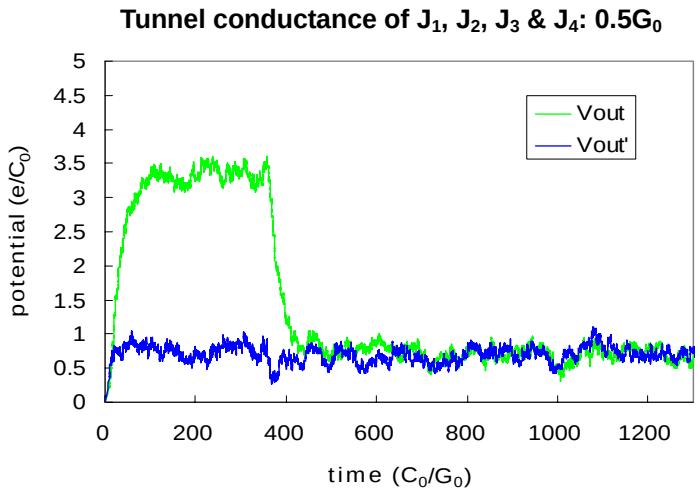

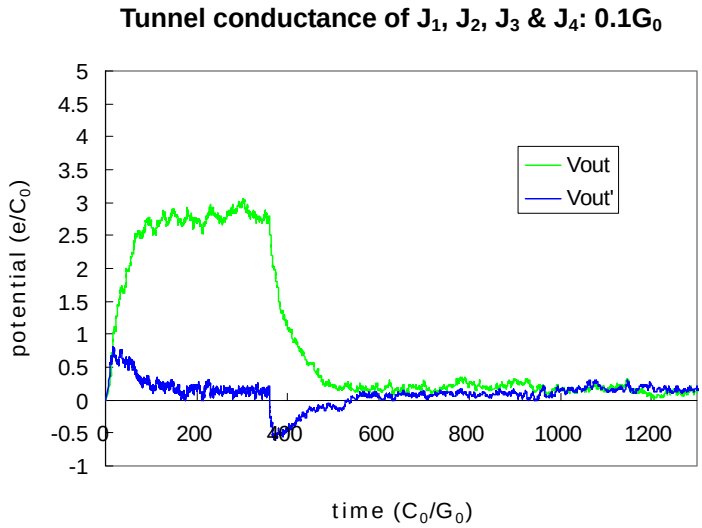

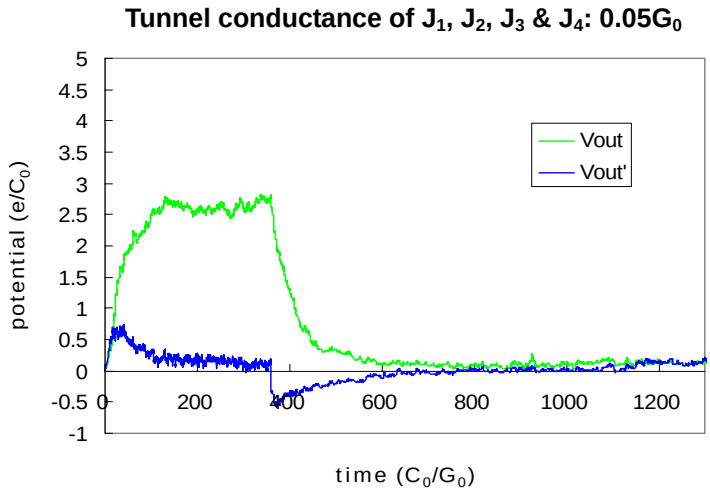

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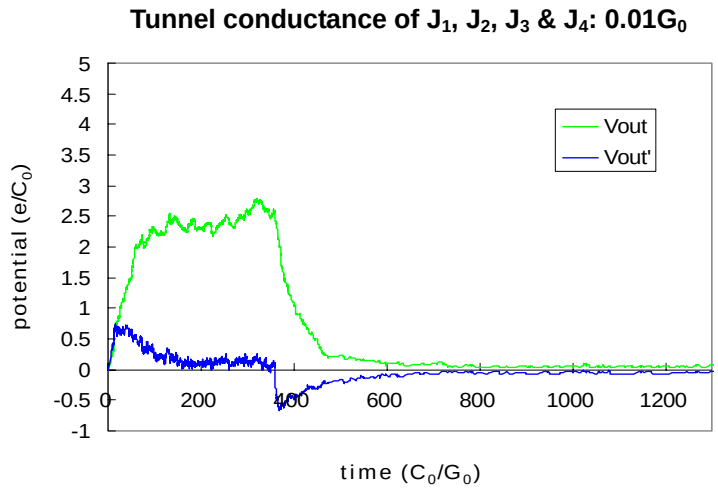

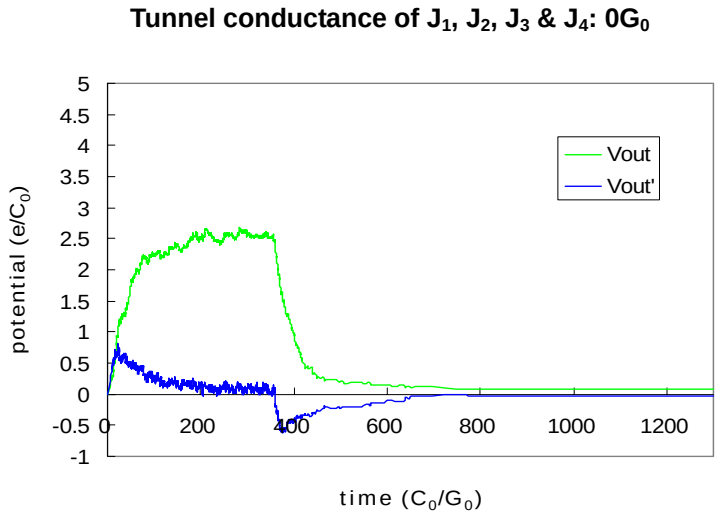

Fig. 3-7. V_{out} and V_{out}' of various tunnel conductance of J_1, J_2, J_3 & J_4 (time unit: ps)

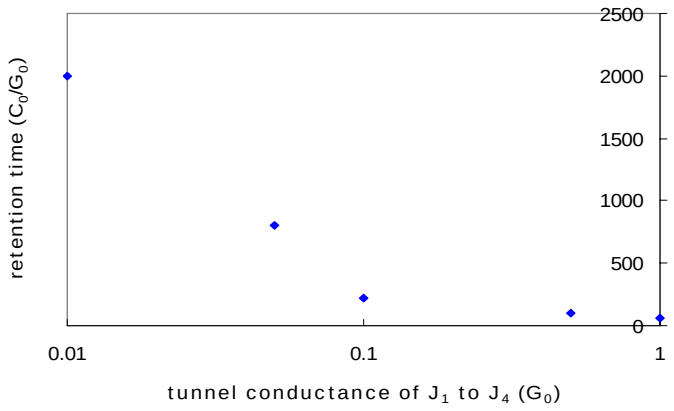

Fig. 3-8. Relation of retention time and tunnel conductance of J_1 to J_4 (time unit: ps)

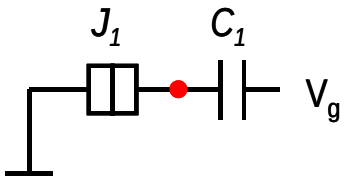

Fig. 3-9. An electron box

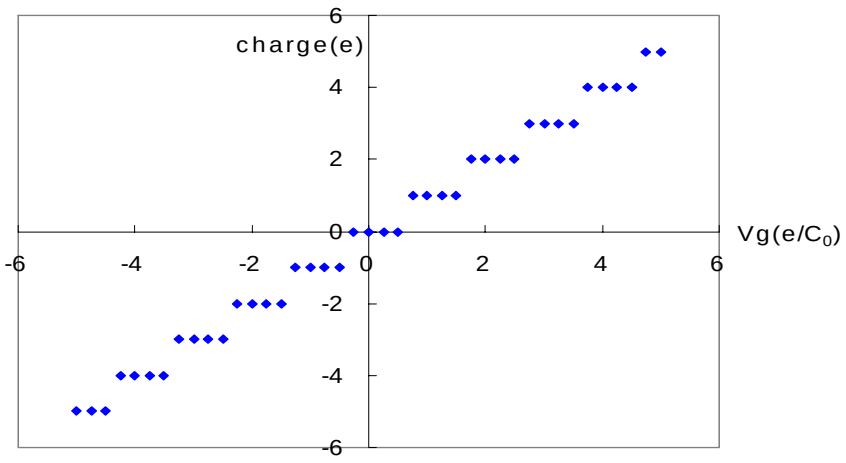

Fig. 3-10. The charge vs. bias voltage characteristic of a single-electron box.

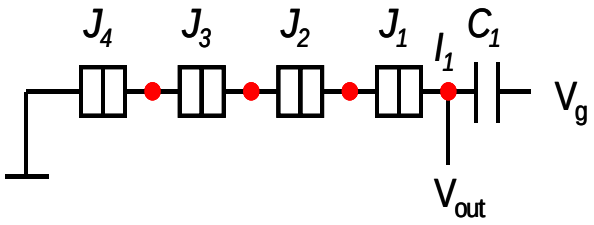

Fig. 3-11. An electron trap memory.

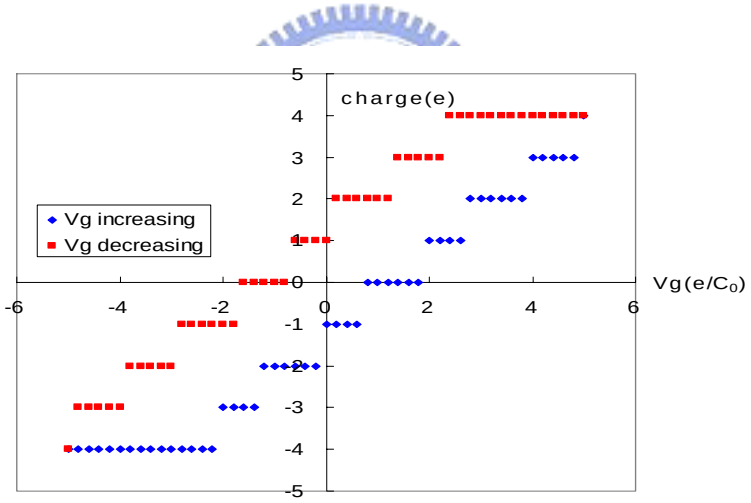

Fig. 3-12. The charge vs. bias voltage characteristic of an electron trap memory shown in Fig. 3-11.

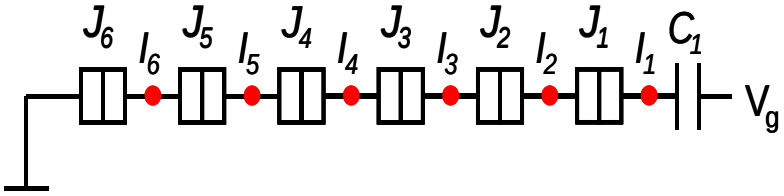

Fig. 3-13. The circuit of electron trap memory.

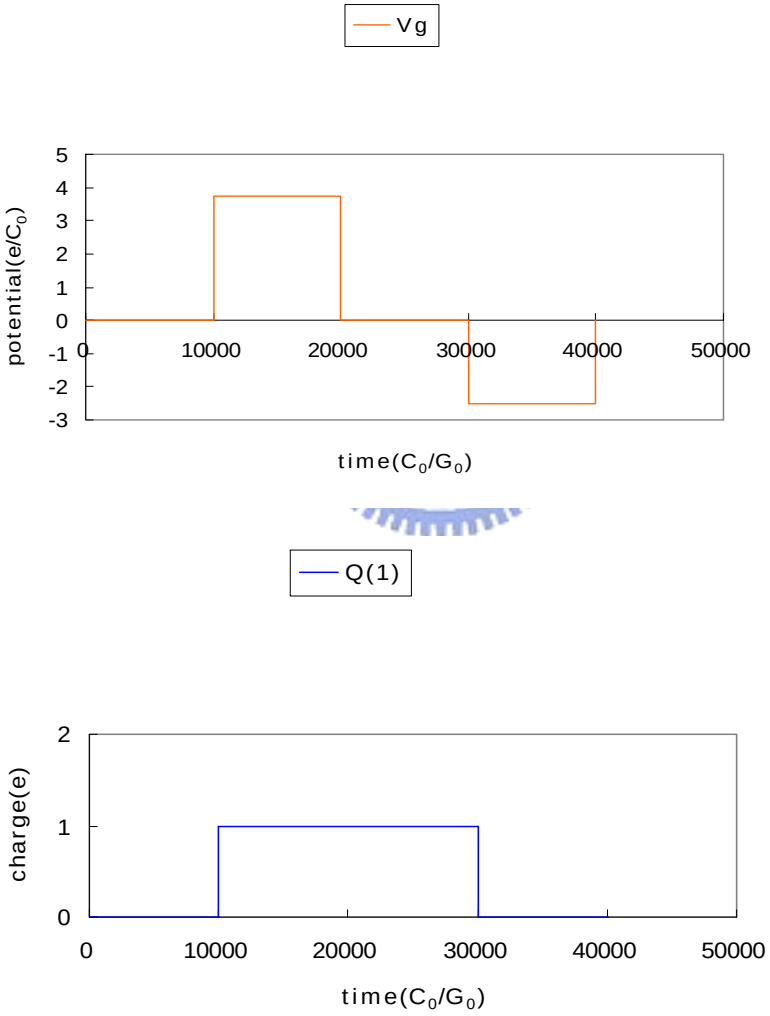

Fig. 3-14. Time variation of Vg and Q(1) which means the charge of island 1 (I1) (time unit: ps).

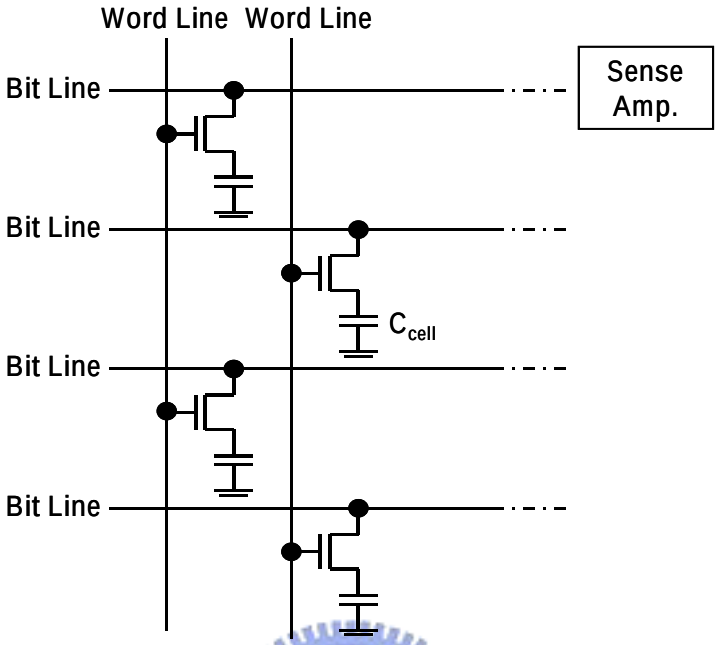

Fig. 3-15. The array of a conventional random-access memory.

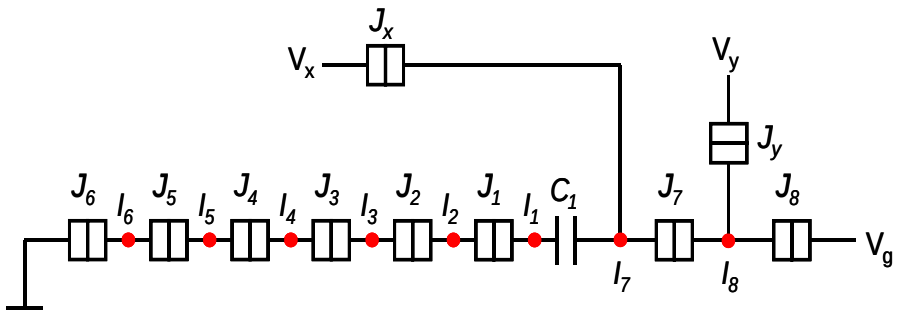

Fig. 3-16. A random-access electron trap memory.

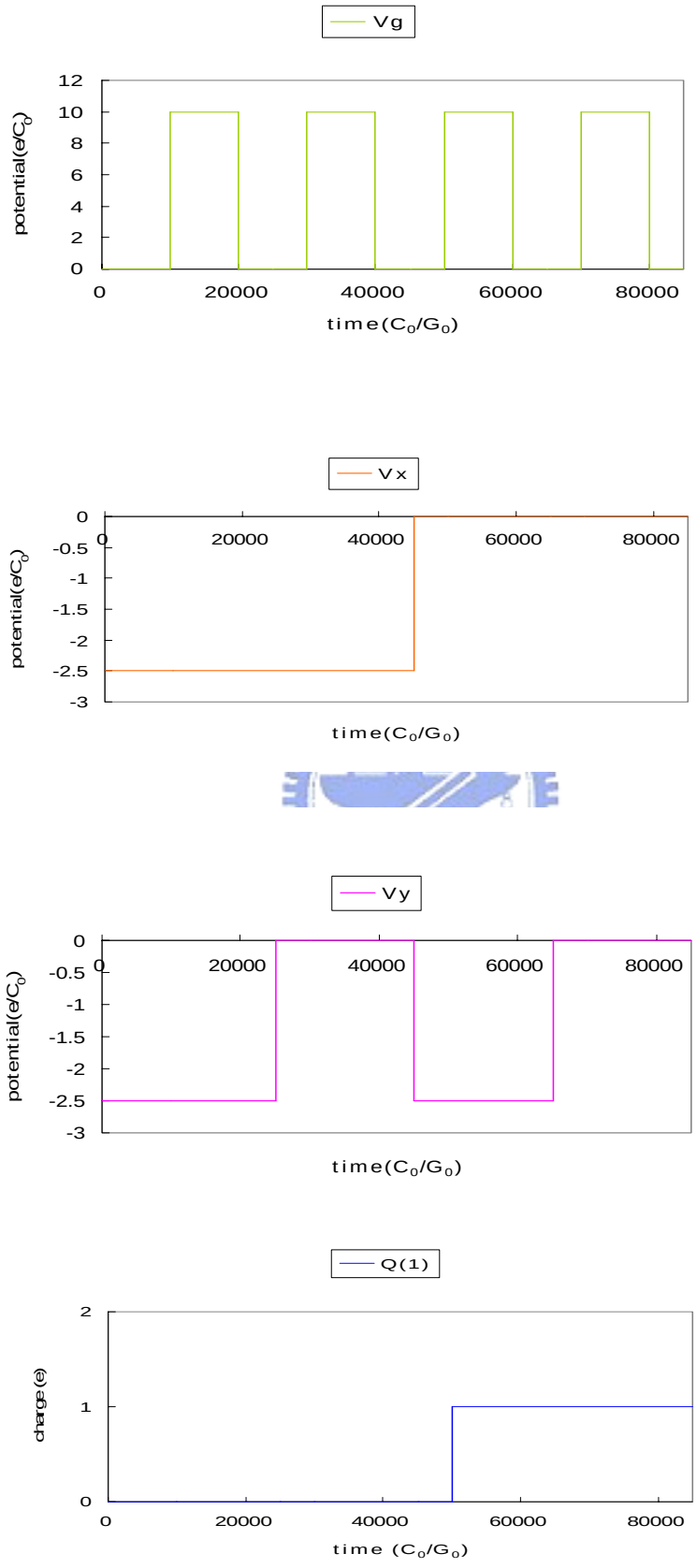

Fig. 3-17. Time variation of Vg, Vx, Vy and Q(1) (time unit: ps).

Effect Test

Source	Nparm	DF	Sum of Squares	F Ratio	Prob>F
Vg	1	1	192.83474	224386.2	0.0000
Vx	1	1	169.74196	197515	0.0000
Vy	1	1	19.07163	22192.11	0.0000

Fig. 3-18. The correlation of Vg, Vx and Vy

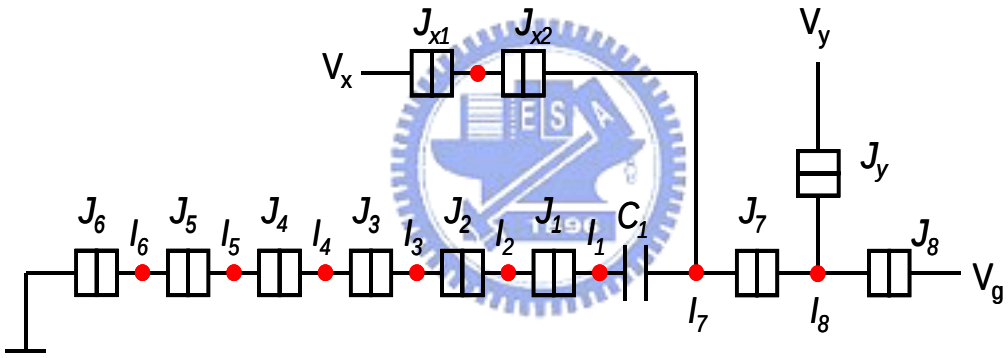

Fig. 3-19. The modified random-access memory

Effect Test

Source	Nparm	DF	Sum of Squares	F Ratio	Prob>F
Vg	1	1	288.20982	292330.6	0.0000
Vx	1	1	86.86303	88104.97	0.0000
Vy	1	1	40.26124	40836.88	0.0000

Fig. 3-20. The correlation of Vg, Vx and Vy of the modified circuit

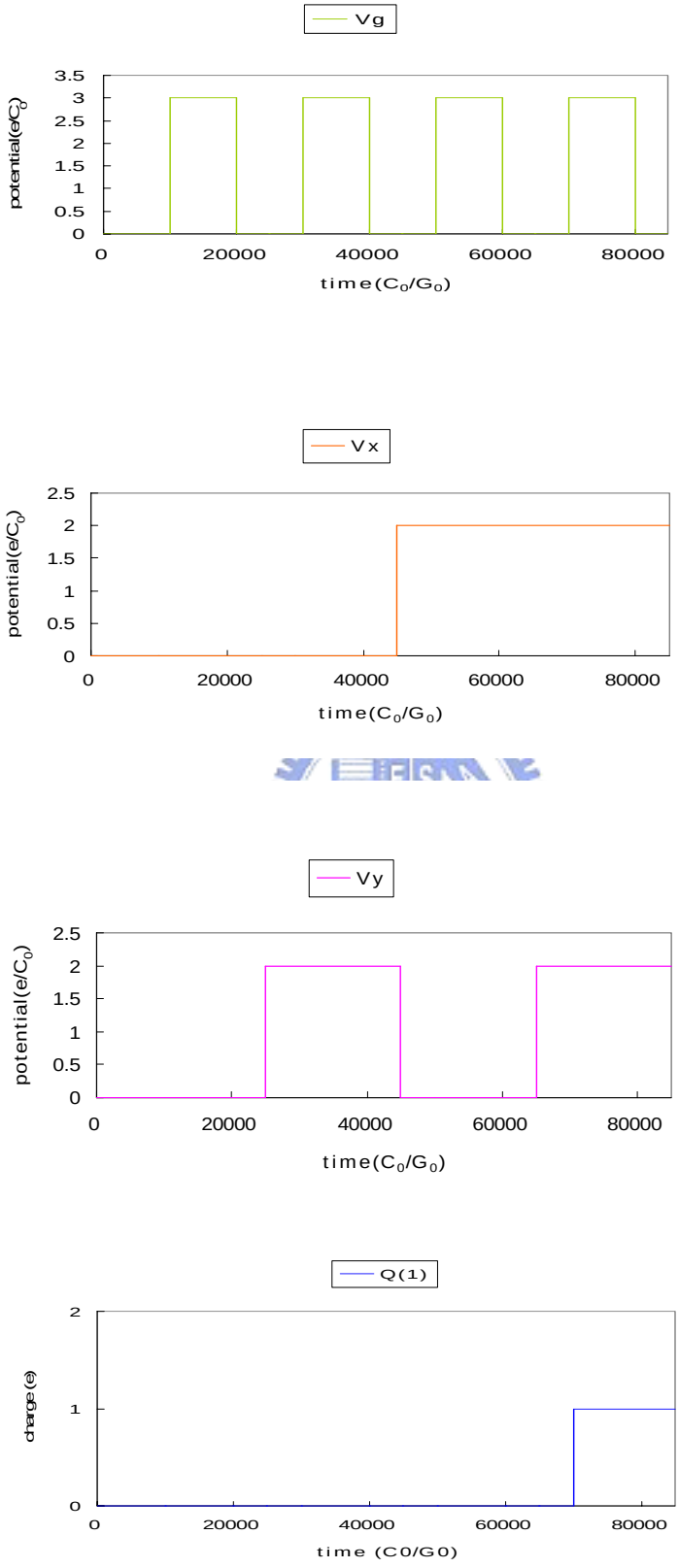

Fig. 3-21. Time variation of Q(1) (time unit: ps)

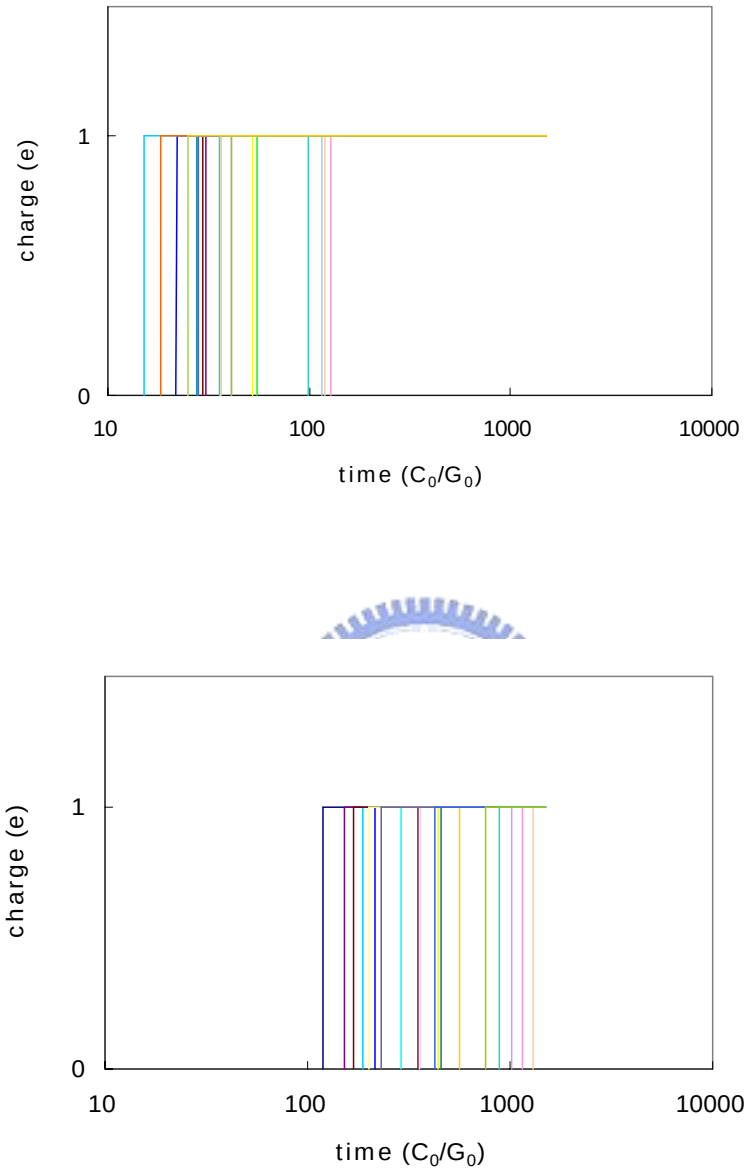

Figure 3-22. The speed comparison of different designs for writing “1”. The upper is original design and lower is the modified (time unit: ps).

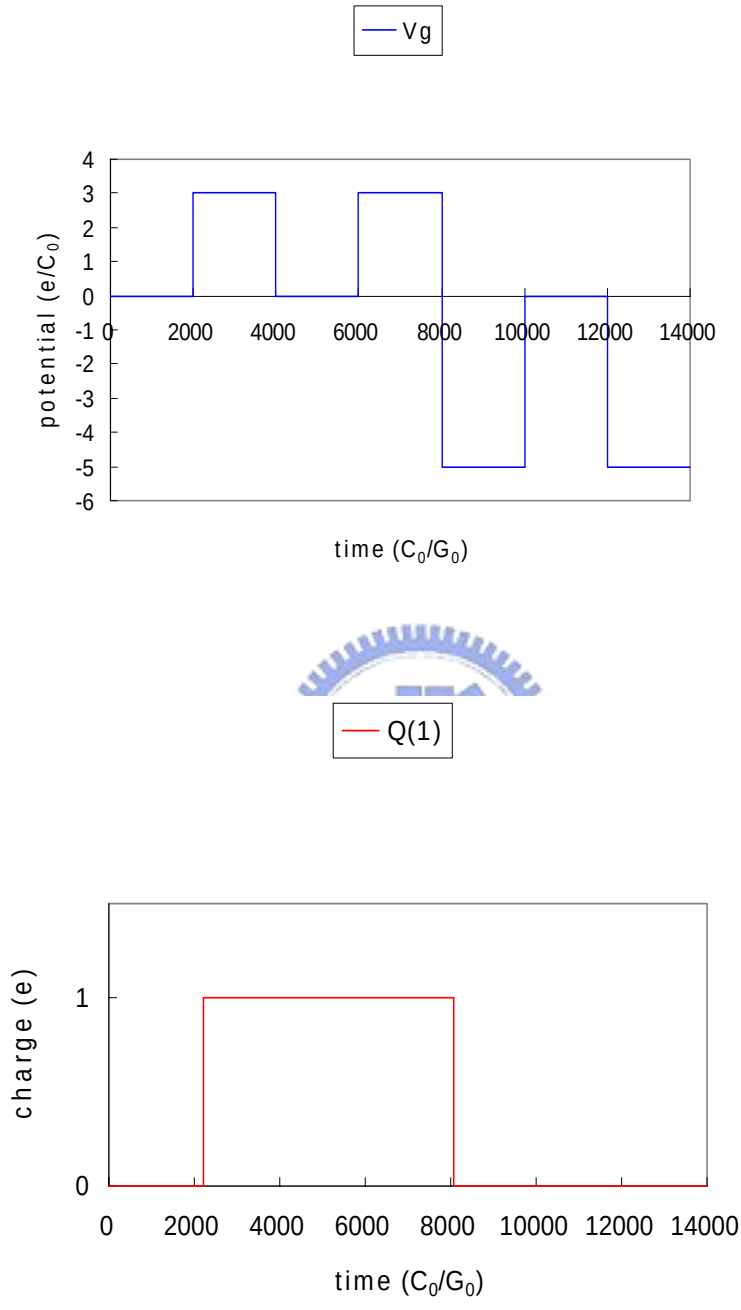

Figure 3-23. Time variation of Vg to write “1” and “0” (time unit: ps)

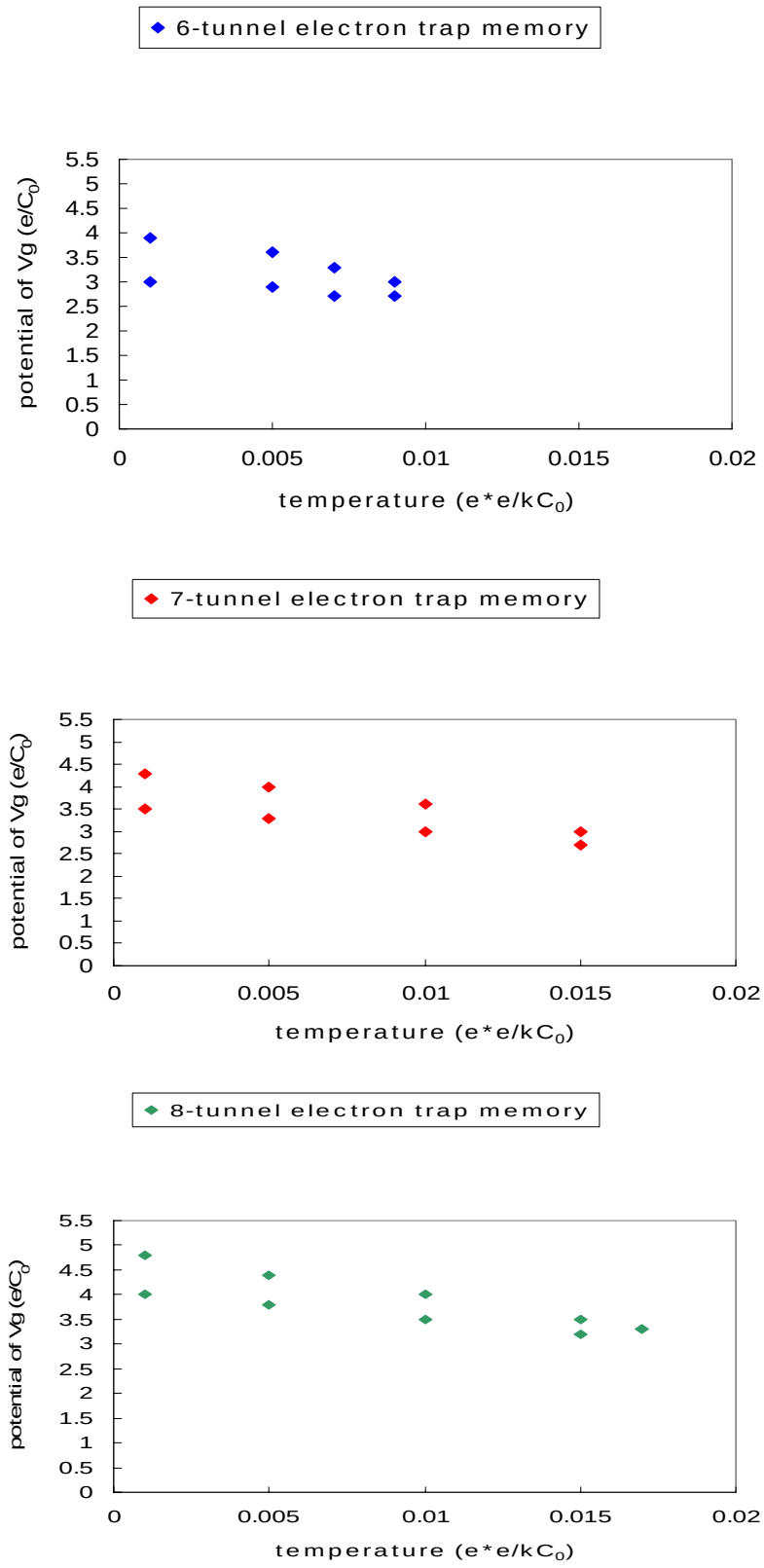

Fig. 3-24. The relationships of temperature, potential of Vg and number of tunnel junctions

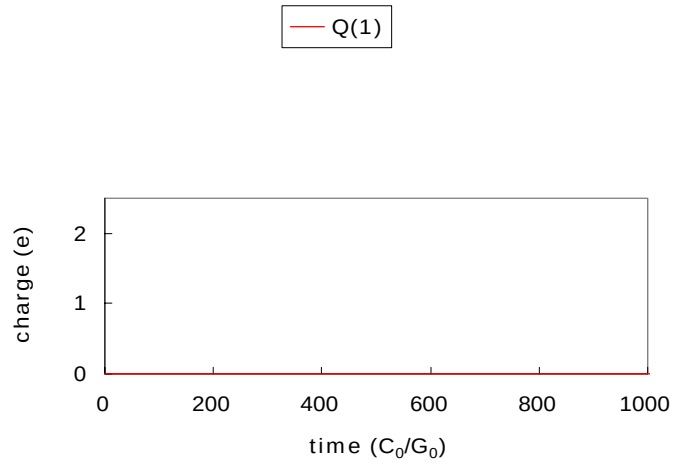

Fig. 3-25. Charge at I_1 keeps zero if the potential of V_g is too small.

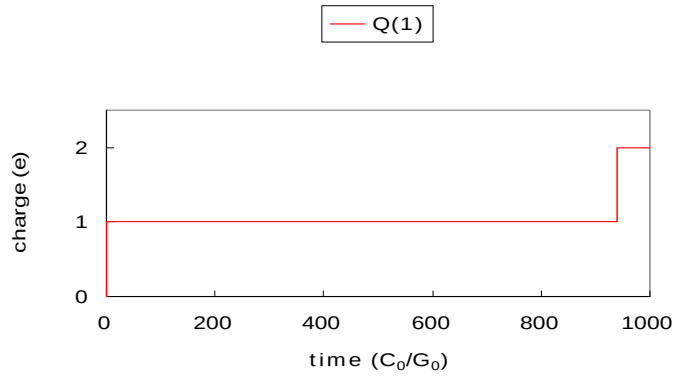

Fig. 3-26. Too many electrons are trapped at I_1 if the potential of V_g is too large.

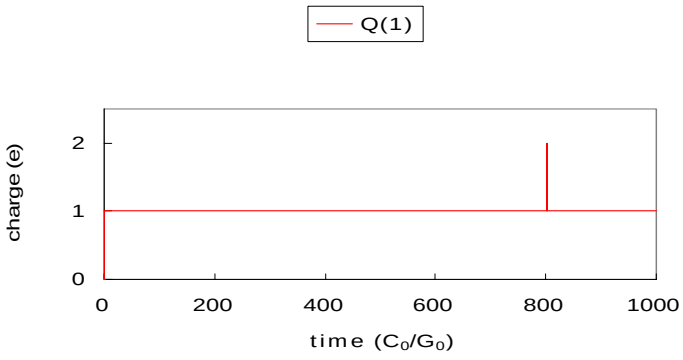

Fig. 3-27. Too large temperature makes the electrons in I_1 unstable.

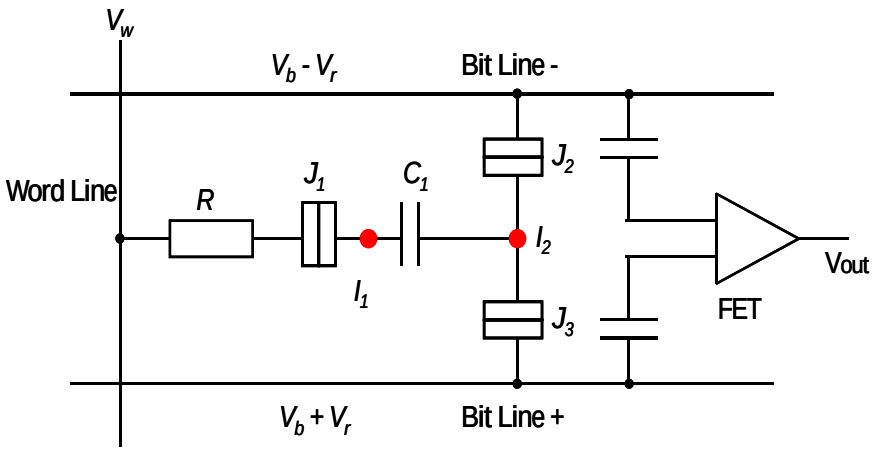

Fig. 3-28. A background-charge-independent memory

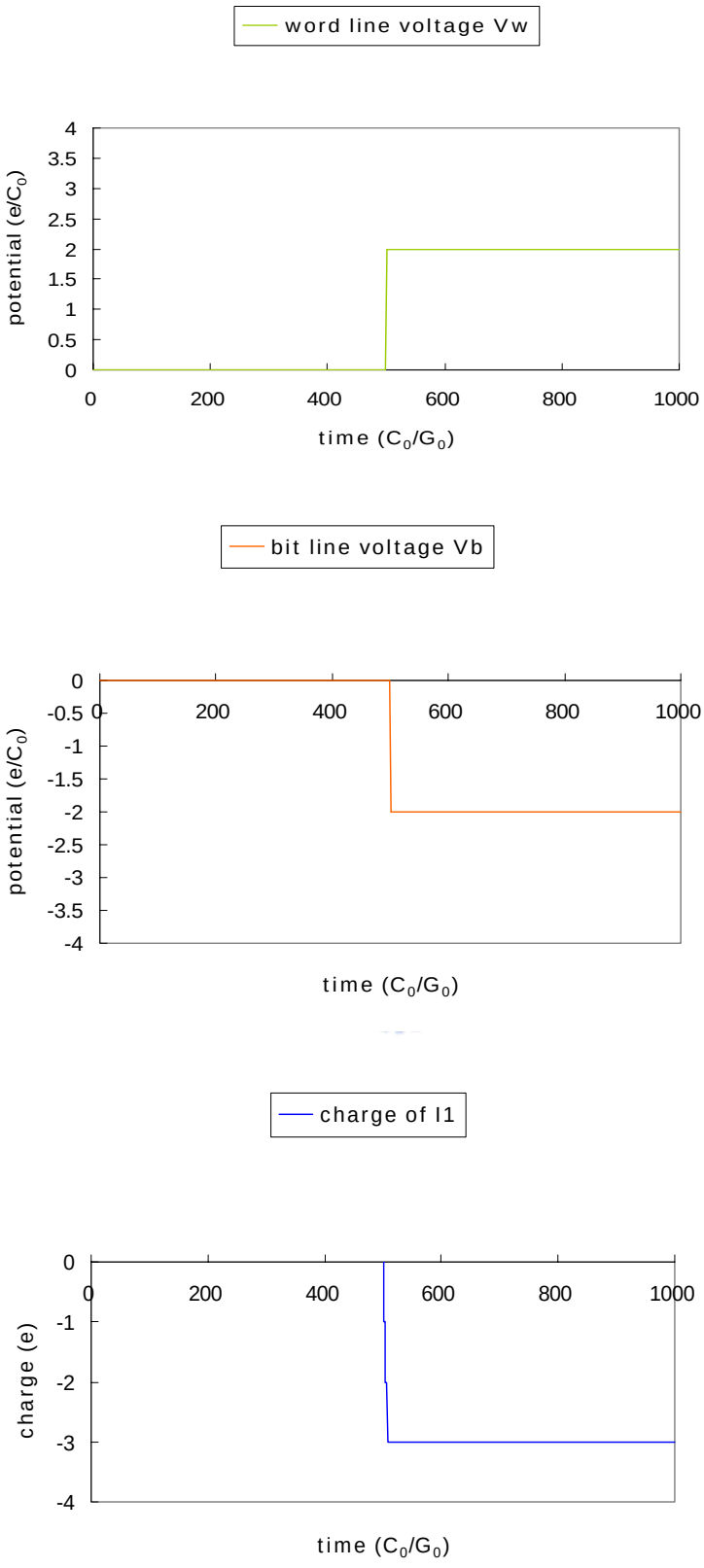

Fig. 3-29. Time variation of writing “1” (time unit: ps)

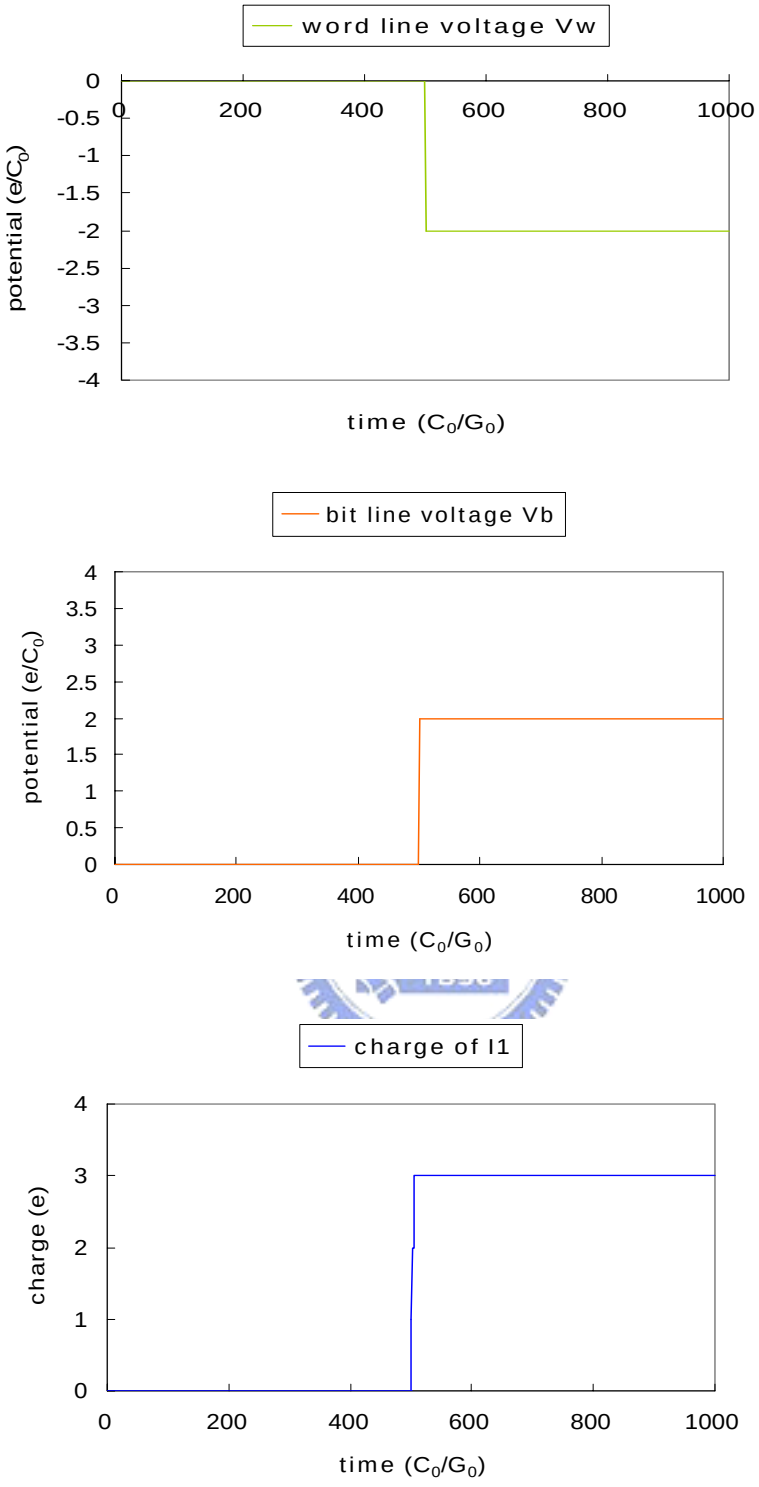

Fig. 3-30. Time variation of writing “0” (time unit: ps)

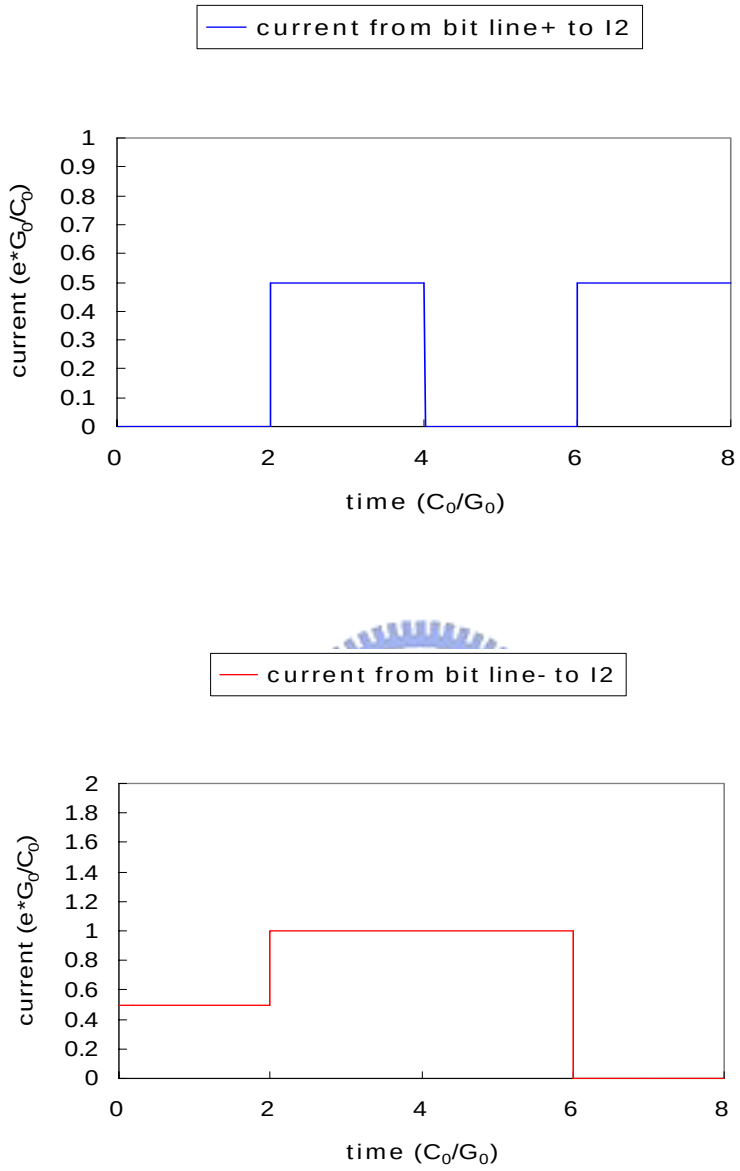

Fig. 3-31. Current oscillation when reading “1” (time unit: ps)

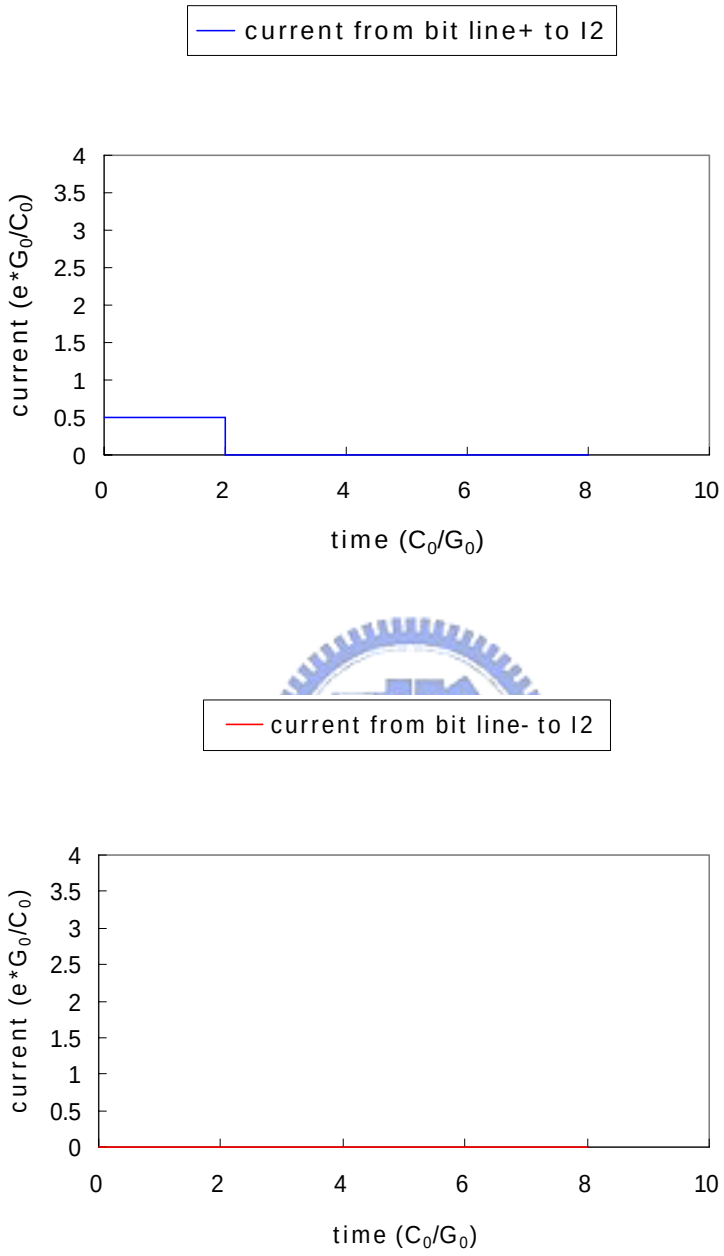

Fig. 3-32. No current oscillation when reading “0” (time unit: ps)

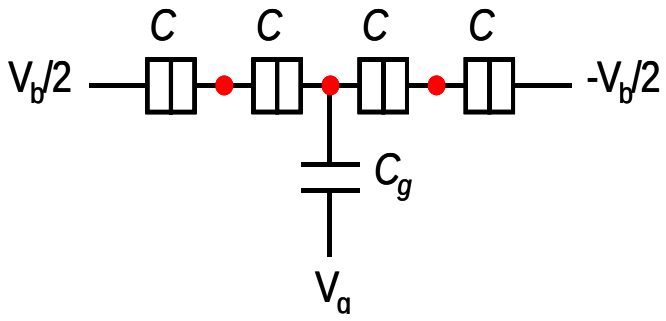

Fig. 3-33. The structure of single-electron turnstile

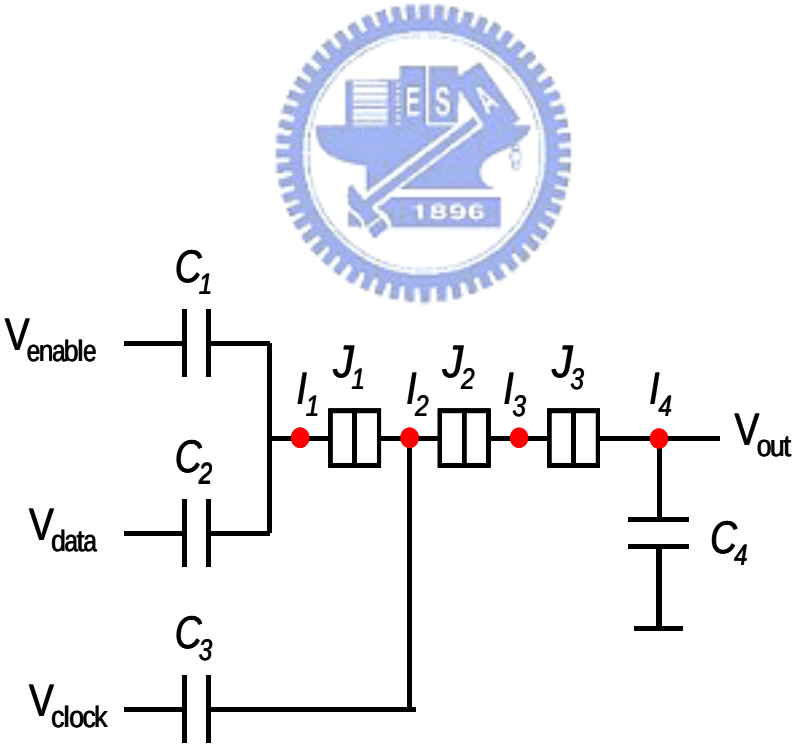

Fig. 3-34. The single-electron turnstile memory

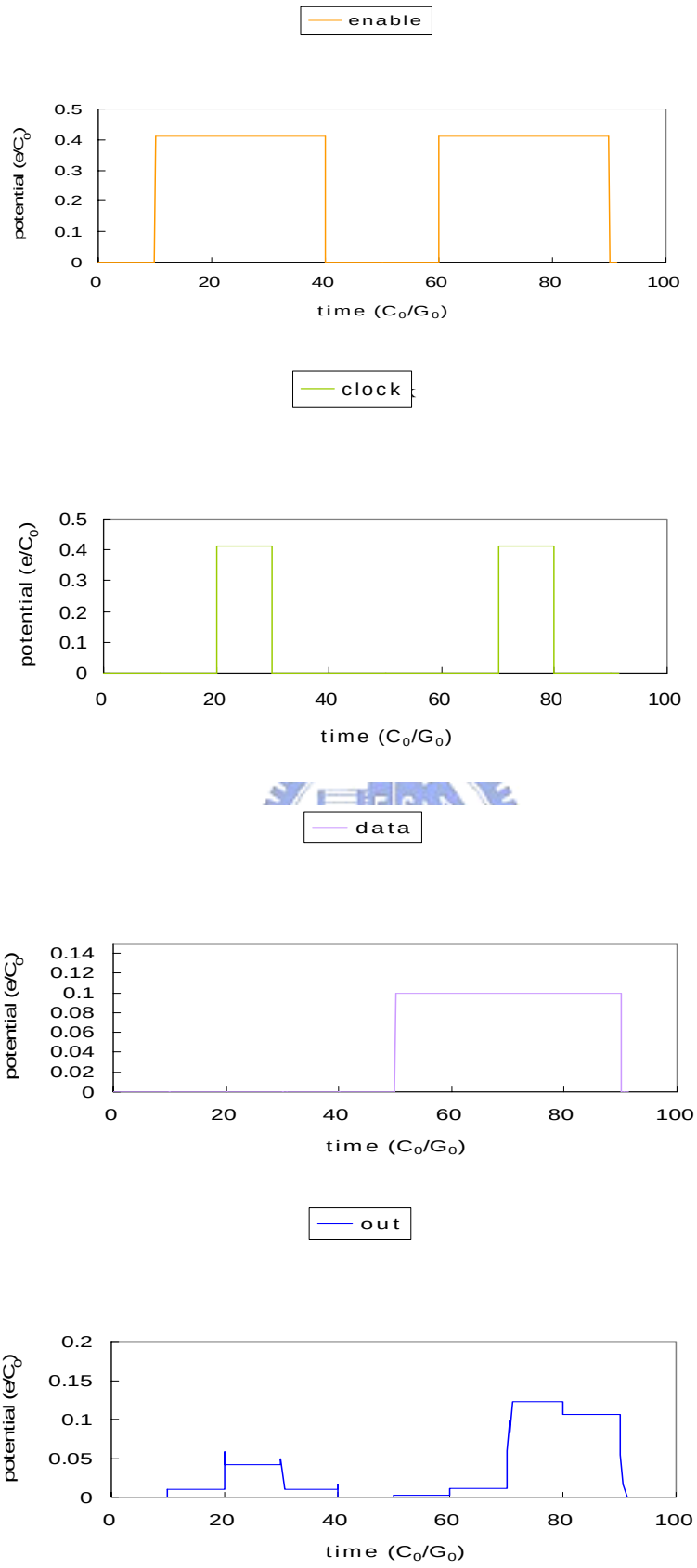

Fig. 3-35. Time variation of different enable, clock and data (time unit: ps)

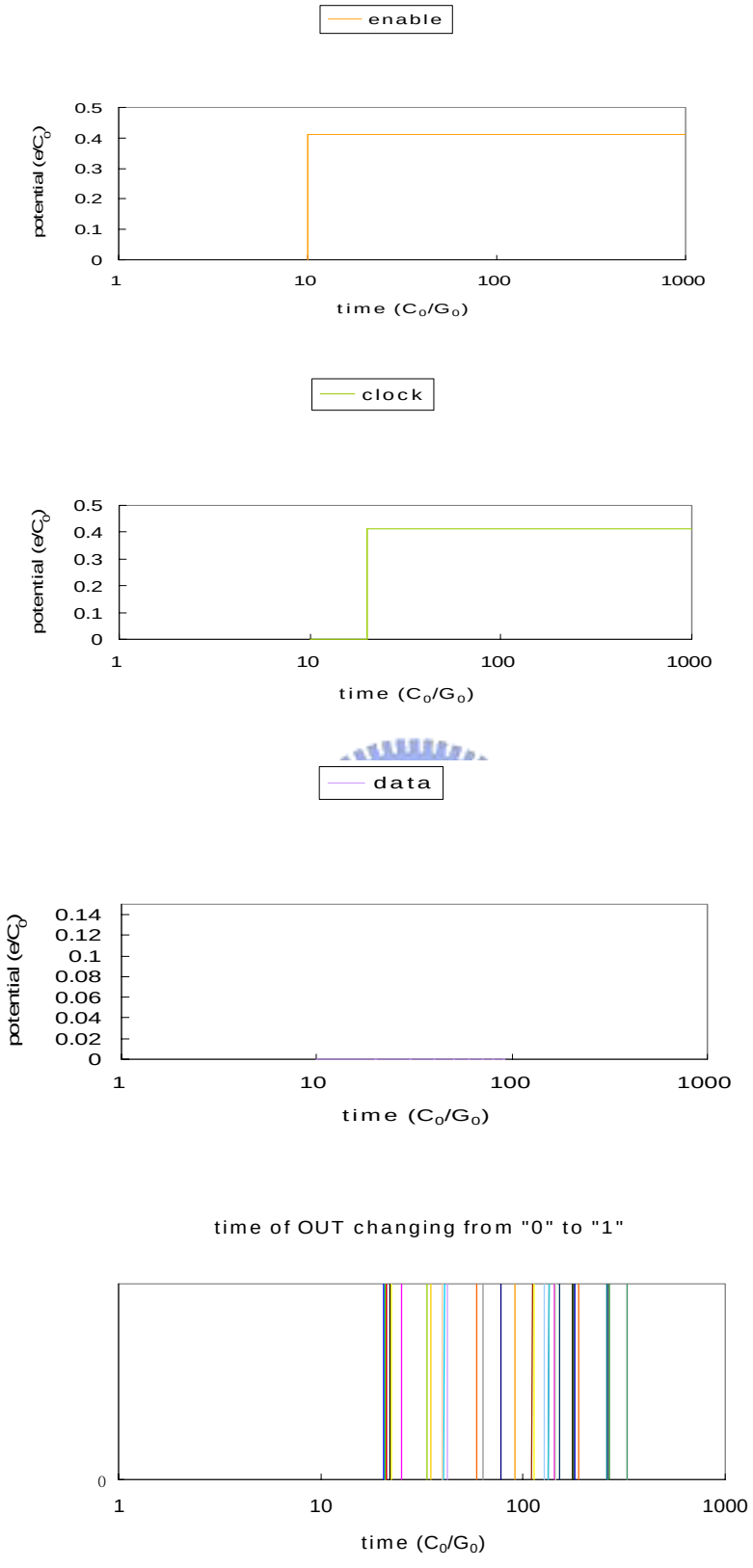

Fig. 3-36. Voltage setting of enable, clock and data to check the changing from “0” to “1” of out (time unit: ps)