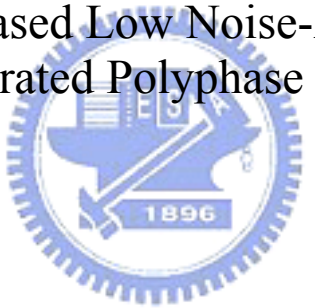
# 國立交通大學

## 電機資訊學院 電子與光電學程

## 碩士論文

具有基體偏壓之低雜訊放大器及整合型多相位濾波器
之 1-V 2.4-GHz 低中頻架構前端接收器電路設計

The Design of 1-V 2.4-GHz Low-IF Receiver Front-End
With Body-biased Low Noise-Amplifier And
Integrated Polyphase Filter



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指導教授：吳重雨　教授

中華民國九十三年十二月

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# The Design of 1-V 2.4-GHz Low-IF Receiver Front-End With Body-biased Low Noise-Amplifier and Integrated Polyphase Filter


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# 國立交通大學

## 論文口試委員會審定書

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所提論文

（中文） 具有基體偏壓之低雜訊放大器及整合型多相位濾波器之 1-V 2.4-GHz 低中頻架構前端接收器電路設計

（英文） The design of 1-V 2.4-GHz Low-IF Receiver front-end with body-biased low noise- amplifier and integrated polyphase filter

合於碩士資格水準、業經本委員會評審認可。

口試委員： 吳重雨 、 洪崇智

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班主任：

中 華 民 國 93 年 12 月 28 日

# 具有基體偏壓之低雜訊放大器及整合型多相位濾波器之 1-V 2.4-GHz 低中頻架構前端接收器電路設計

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## 摘　　要

此論文提出一個能操作在 1-V 電源電壓，射頻頻率為 2.4-GHz 之低中頻架構之前端接收器電路，所完成的晶片是一個適用於電池供電的通訊器或藍芽無線傳輸的應用。目的是能夠實現一個簡單，低成本，低電壓，低功率消耗，且能有最少的額外元件，而能夠很容易的使用在可攜式裝備上。

這個晶片的製作是透過國家晶片系統設計中心，以台灣積體電路製造股份有限公司提供的 0.25-um 互補式金氧半導體製程技術實現。整個晶片包含一個基體偏壓型低雜訊放大器，正交壓控振盪器，降頻混波器及一個主動型多相位濾波器。

量測結果顯示，接收器可以正確的操作在 1-V 電源電壓。它並能提供 15-dB 增益，17-dB 的雜訊指數，41-dB 的鏡像拒斥比，-15-dBm 輸入三階截點值。在 1-V 電源電壓下有 18.575mW 的功率消耗。

# The Design of 1-V 2.4-GHz Low-IF Receiver Front-End With Body-biased Low-Noise Amplifier and Integrated Polyphase Filter

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## ABSTRACT

This thesis proposed a design of 1-V 2.4-GHz low-IF architecture receiver front-end circuit. It is suitable for battery-based communication equipments or bluetooth application. The goal of this design is to realize a simple, low cost, low voltage, low power consumption and with fewer external components receiver architecture and it can be easy to use for portable equipments.

This chip was fabricated using 0.25-um CMOS technology provided by Taiwan semiconductor manufacturing company via national chip implementation center. Whole chip includes a body-biased low noise amplifier, quadrature voltage control oscillator, downconvert mixer and an active polyphase filter.

The measured results show that the receiver can be correctly operated at 1-V power supply. The receiver provides gain 15-dB, 17-dB noise figure, 41-dB image rejection ratio, and -15-dBm input third intercept point. The power dissipation is 18.575mW with 1-V power supply.

# ACKNOWLEDGMENTS

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In this chip's implementation, I want to say thank to National chip implementation center (CIC), Taiwan semiconductor manufacturing company (TSMC) for their help and support in the chip fabrication.

I thank my parents, who gave me the courage to get my education, supported me in all achievements. In addition, I give my dearly thanks to my wife, Yu-Pin Huang. We married last year-end. But I sacrificed a lot of time for my job and my research. Especially she born my daughter during my education, she must tolerate many pressures and take cares our baby lonely.

Finally, I would like to say thank to all the people who have ever helped me in the past years.

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# CHAPTER 1

# INTRODUCTION

## 1.1 BACKGROUND

Before, RF CMOS process could not be widely used, due to its complexity and instability. RF front-end circuit are usually designed and fabricated with GaAs or BiCMOS technology due to its better characteristics in the RF band. However, in recent years advances in the development of CMOS processes continues to spread. CMOS processing technology have continued to reduce the minimum channel length of MOS device, thereby increasing the transistor cut-off frequency *ft*. In the case of RF circuits, higher *ft* transistor means it can be operated at higher frequency. This parameter moves up the carrier frequency of RF system.

RF CMOS processing has the benefits of low cost. The wireless communication system designer attempts to integrate RF and baseband components for cost-sensitive applications. A great amount of researches continues to improve the power efficiency and to reduce the supply voltage in RF circuit used in the present generation of wireless products. Otherwise, RF system is still needed to meet the desired gain, linearity and noise figure. These are always a challenge for a RF circuit designer.

Low-IF receiver is one of popular architecture in the RF receiver front-end circuit, where off-chip IF filter is easy to implement in a single chip so that the additional power dissipation can be saved and complexity can be reduced. Otherwise, low-IF receiver architecture has fewer external components. It is the benefit of integration. Monolithic image cancellation has been always a challenge in receiver design. A low-IF receiver will suffer from an in-band image signal.

That's a challenging to separate the desired channel from undesired ones and from interference. The complex polyphase filter presented in this paper is the low-IF filtering section of the bluetooth in the short-range radio receiver. We used an active complex polyphase filter to restrain the image signal. This design of IF filters focus on cost, size and manufacturing point of view.

Although the development of CMOS process is push to 90nm process, Fig. 1.1 is a process trend of Taiwan semiconductor manufacturing company. 0.25um CMOS process is ripe and cheaper than newer generation. 0.25um CMOS processing enhanced the *ft* up about to 25GHz and operating voltage is down to 2.5V(refer to TSMC's RF IC technology). This frequency range can be easily used in bluetooth 2.4GHz. But the 2.5V operating voltage is still high for battery-based applications. But its threshold voltage is still suitable for 1V applications.

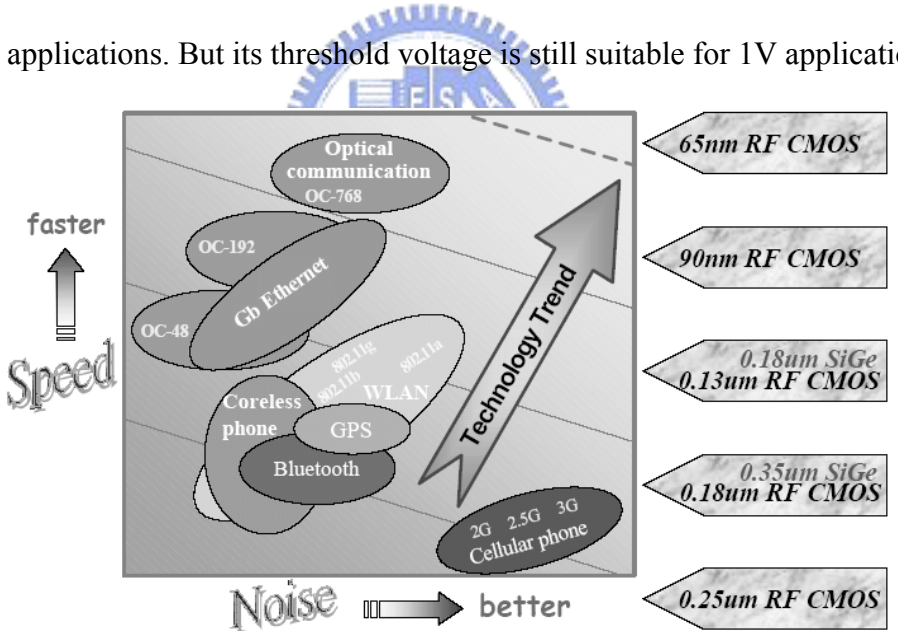



Fig. 1.1 RF technology trend (TSMC).

The mail application of this thesis is used for bluetooth system. Bluetooth is an industry standard for short-range wireless voice and data communication in 2.4GHz ISM band. It regulates operating band from 2.4GHz to 2.48GHz. The channel bandwidth is about 1-MHz. In order to empower low power and highly

integration implementations, the Bluetooth system specifications were made quite relaxed.

The specification of this design is based on bluetooth. Bluetooth specifies an operating frequency range 2.40~2.48-GHz with 79 channel of 1-MHz bandwidth per channel. The basic access is based on 1-Mbps GFSK modulations. The input-power-level range is -70~-20dBm.

In this paper, the receiver was fabricated using a low cost 0.25um standard CMOS process provided by TSMC. This design used operating voltage 1V and applied in 2.4GHz bluetooth frequency band. The architecture of receiver uses a low-IF architecture with 5~10MHz intermediate frequency (IF).

## 1.2 REVIEW CMOS RF RECEIVER ARCHITECTURES

A typical block diagram of transceiver system is shown in Fig. 1.2. The upper side represents the receiver part of the transceiver, while the lower side represent the transmit part of transceiver. The system also includes a frequency synthesizer (RF local oscillator) to apply a clear and stable frequency. The local oscillator is responsible for the correct frequency selection in the up- and down-converters.

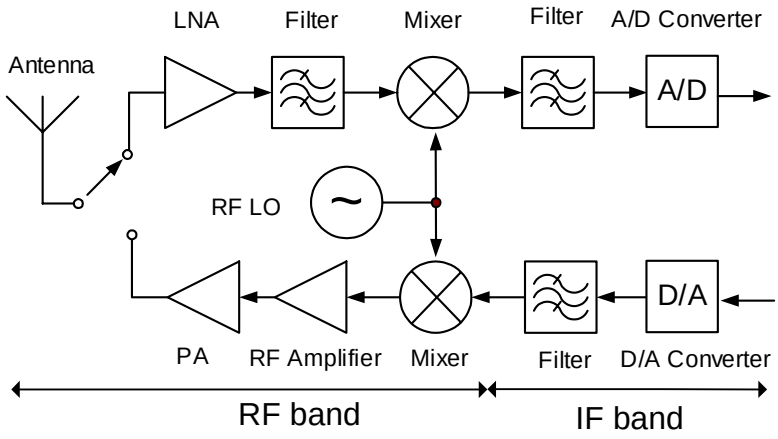



Fig. 1.2 transceiver system architecture

The frequency domain can be separated to RF band and IF band in the transceiver system. In the receive path, the receiver must be able to reject signals outside the band. The receiver must without loss and it also meet its performance. In the first stage of receiver system, the received signal amplified by the low noise amplifier (LNA). Because noise added by the LNA corrupt the received signal significantly and degrades the overall system performance, the amplifier must have the ability to detect weak signals and to reject the noise interference. Hence, noise figure is always an important consideration in the design of LNA. The received signal usually has a carrier frequency of a few 100's MHz, or even a few GHz. The frequency down-conversion stage locks to the frequency of the received signal and down converts the received signal to the IF band.

Next to the low noise amplifier, the down converter operation is done by mixing the received signal and LO signals. The LO signal is generated by a frequency synthesizer. The LO signal must be clear and stable.

In the last stage of receiver, The IF band signal pass to A/D converter processing to digitize by a digital signal processor (DSP) or any application in integrated circuit.

In the part of transmitter, the information signal can be speech, video or data is digitized and organized into frames. Finally, it will be transmitted by transmission path. A baseband signal is up-converted to the desired transmit carrier frequency by mixing the LO signal and IF frequency. The power amplifier transmits enough power to antenna in the last stage of transmission path. The transmitter must efficiently produce enough output power. But the harmonics will be generated in an efficient power amplifier. These usually must be filtered out before they reach the antenna.

The performance of receiver system can be issued in selectivity, noise figure, and intermodulation. High selectivity means it can receive a low magnitude signal in a high noise environment. In addition to noise consideration, a receiver system also needs enough BER (bit error rate) requirements. In order to meet this requirement, the signal must be enhanced and the noise and image signal from antenna must be degraded.

The main purpose of receiver system is to translate the input RF spectrum to a much lower frequency. The primary criteria of selecting receiver architecture are their complexity, cost, integration, power dissipation and the number of external components. The designer selects receiver architecture according to their applications.

The following reviews three kinds of popular receiver architectures. They are heterodyne receivers, direct-conversion receivers and Low-IF receivers.

**A. Heterodyne Receivers**

This is probably the most commonly employed architecture in current wireless communication. Heterodyne receiver down-converts the received signal to an intermediate frequency (IF). The Heterdyne receiver is illustrated in Fig. 1.3.

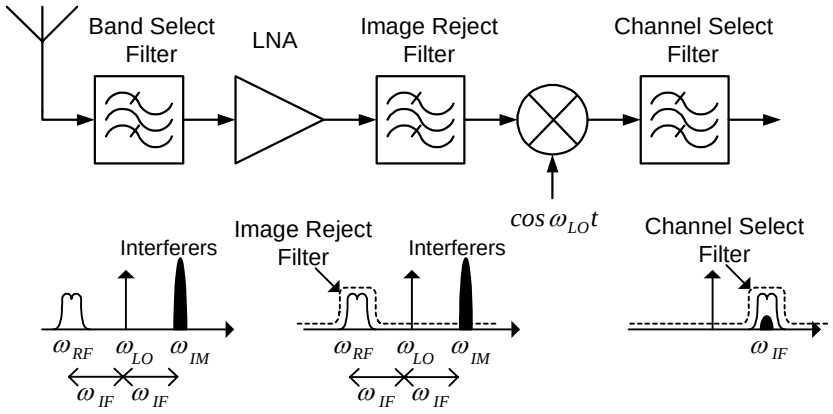



Fig. 1.3 Heterodyne architecture

The mixer mixes the RF signal and LO signals to generate IF. The RF frequency and LO frequency is different, and therefore the mixer output frequency is $\omega_{IF} = \omega_{RF} - \omega_{LO}$. If it exist an image signal $\omega_{IM}$ to satisfy $\omega_{IF} = \omega_{LO} - \omega_{IM}$, they are down-convert to an identical IF. The desired signal is interfered by image signal. The receiver architecture must consider image signal $\omega_{IM}$ and desired signal $\omega_{RF}$ are received at the same time. For this reason, the receiver needs an image reject filter to remove the image signal. The image reject filter is usually implemented with off-chip because the filter is passive and consumes large area. Because it is off-chip implementation, the low noise amplifier must drive a 50Ω load. This intensifies a trade-off among the noise, linearity, gain and power dissipation of the low noise amplifier. Furthermore, due to it need several discrete components; the large power consumption is not suitable for low power application. There is a trade-off between the selective of IF frequency and image rejection filter. If the chosen of IF frequency is lower, the filter must have good performance reject the image frequency but the cost will be increased. If the choice of IF frequency is higher, the filter performance is relaxed.

Although the heterodyne receivers widely used in most application and offer best selectivity, a number of drawbacks cause that it is difficult to implement in high-Q filter, and high power dissipation is usually not suitable for single-chip and low power application.

**B. Direct-Conversion Receivers**

Illustrate in Fig. 1.4, direct-Conversion receiver architectures translate the received signal directly to zero frequency ($\omega_{IF} = 0$); it also called zero-IF receiver or homodyne conversion receiver.

Compared with heterodyne architecture, direct-conversion doesn't have the problem of image signal interference. As a result, no external image reject filter is required and the LNA need not drive a 50Ω load. Otherwise, a LPF and baseband amplifiers can replace the IF-filter in heterodyne receivers. These architectures can be easily realized to monolithic integration. Because of its simplicity, appears to offer the best opportunity for integrated systems.

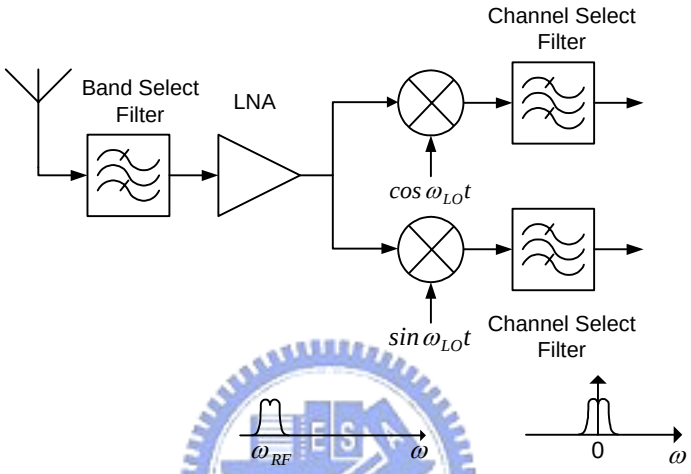



Fig. 1.4 Direct conversion architecture

The RF frequency mixes the LO frequency into baseband frequency. Image signal is shifted to negative frequency domain. The desired signal is selected by baseband LPF, therefore image signal is out of baseband domain and image signal is fully rejected.

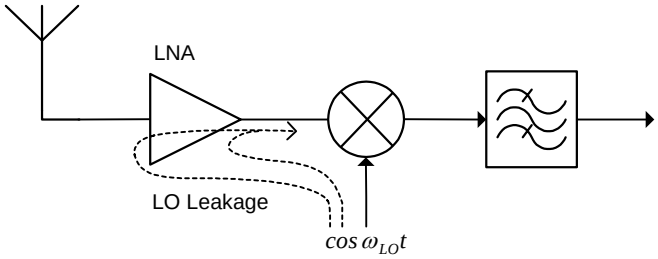



Fig. 1.5 DC offset due to self-mixing of LO

Direct-conversion receiver offers many advantages to realize in monolithic integration, but it comes with a number of design issues. As shown in Fig. 1.5, DC

offset is a design trouble in this architecture. The source of DC offset comes from two reasons. First, LO signal is a usually large signal and high power. LO frequency is the same as RF frequency. For this reason, LO signal is easily leak to LNA and mixer input port. The leakage effect usually arises from capacitive and subtract coupling. This leakage signal is mixed with the LO signal and produce a DC component. This DC component corrupts the baseband signal. Second, if a large interferers leaks from the LNA and mixer input to the LO port. The interferers similarly produce the DC offset variation.

Another important trouble of design issue is second order distortion. As depicted in Fig. 1.6, because the transfer function of circuit is not linear, the non-linear effect causes the even-order distortion in RF signal path. Second order distortion appears to the mixer output. If the frequency is within the pass band of the filter, the distortion will interfere with the base band.

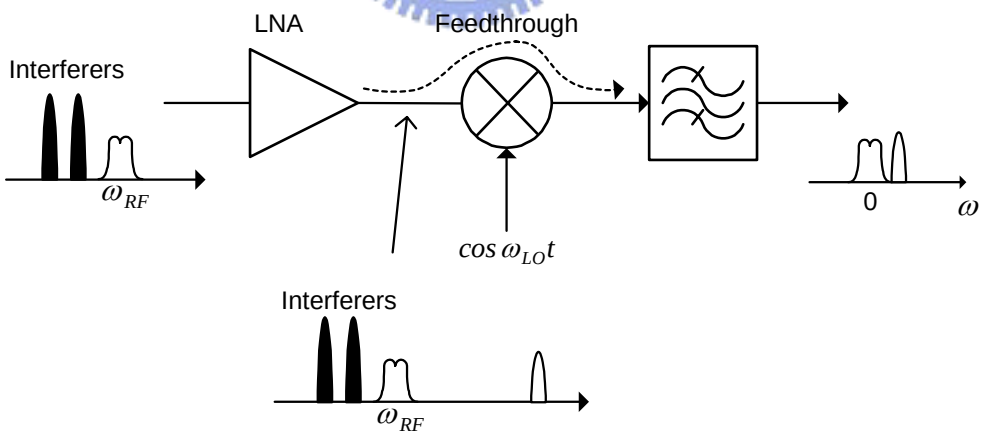



Fig. 1.6 Effect of second-order distortion

### *1.2.1 Low-IF receiver with image reject filter*

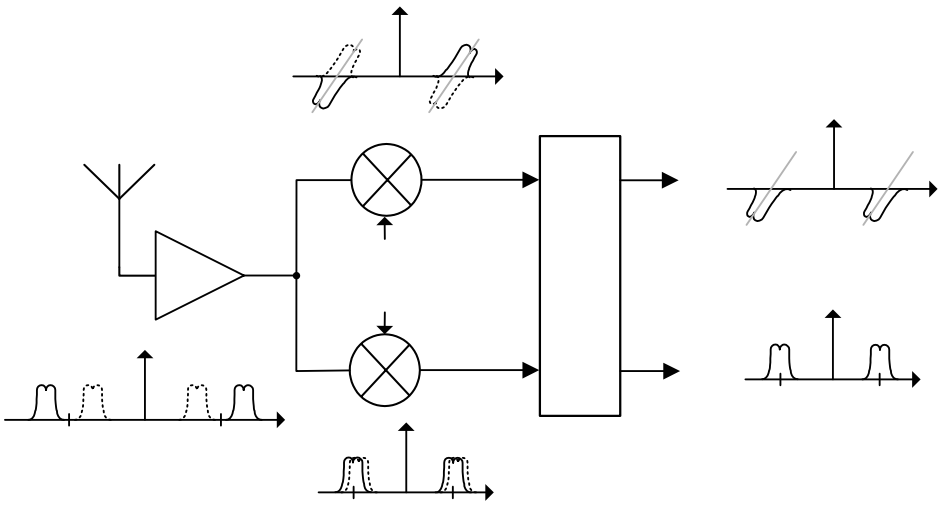


Fig. 1.7 Low-IF architecture with polyphase filter

Low-IF receiver is usually used in wireless communication because it's high integrality, low cost and easy to implement filter at low frequency. The low-IF architecture resolve the trade-off between image-reject filter and channel select for IF choice. I-Q mismatch is a disadvantage of low-IF receiver. I-Q mismatch cause s the receiver unable to reject image signal entirely. Asymmetry on layout, process variation or parasitic degrades the image rejection capability. Layout and design strategies are proposed to achieve high performance of image rejection for mismatch consideration.

Low-IF architecture with polyphase filter is shown in Fig 1.7, RF desired signal is amplified by low-noise amplifier and transfer to the mixer to mix with RF and LO signal. The LO signal is generated and it is I/Q signal with 90 degree phase difference. The quadrature mixer mixes the LO signal and down-convert the signal to I/Q low intermediate frequency band. This operation will be further discussion in chapter.2.

Relative to direct-conversion receiver, the main advantage of the Low-IF receiver is that it doesn't have DC offset problem. In order to solve the DC offset and to achieve higher monolithic integration, Low-IF receiver down converts the RF signal to IF.

Although this architecture solves the troubles of DC offset, the existed image signal degrades the performance of the receiver. Fortunately, the RF signal down-converts to very low frequency and image reject filter is easy to implement at low frequency. This architecture can use many kinds of methods to reduce the image signal. For example, Hartley architecture, Weaver architecture and polyphase filter architecture.

In this case of low-IF receiver, it uses a polyphase filter as the image reject filter. The basic function is used to pass the desired IF signal and to reject the image signal.

The bluetooth specification is developed in favor of high-IF or low-IF architecture. However, A high IF receiver, which uses an IF much larger than the signal bandwidth, needs off-chip filters due to required high Q components. Hence the system integration level is reduced and extra power on the I/O driving circuit is demanded. In addition, the high IF also increases the complexity and cause more power dissipation in the IF stage. For this reasons, a low-IF architecture is preferred in this proposed design. Fig. 1.6 shows the block diagram of the low-IF receiver. Low-IF receiver architectures translate the received signal to very low frequency. It via a polyphase filters to reject the image signal.

### *1.2.2 Body-biased low-noise amplifier design*

This thesis tries to realize a low-IF receiver with polyphase image reject architecture operated at 1-V supply voltage by TSMC 0.25um technology. The

high threshold voltage in 0.25um process is a challenge when it operates at low supply voltage.

To provide body-bias control is an effective method to reduce the threshold voltage for low voltage design. This is often seen in SOI technology low-noise amplifier design. The SOI technology has many advantages for low voltage and high frequency design due to its bulk isolation scheme [11]. But SOI process is not a standard process and it is not ripe and popular than CMOS bulk process.

The body of transistor is connecting to a bias voltage. The threshold voltage of the transistor becomes smaller due to body effect so that a large drain current is obtained which keeps the gain high even at a lower supply voltage. By using body-bias control, it can operate at below 1.0V with a higher gain and higher 1dB-compression point.

The body-bias method is applied to LNA circuit. The measurement results have proved the body-bias method can improve the performance at low voltage operation.

| | **This work Simulation results** | | **Reference paper Experimental results** | |
|---|---|---|---|---|
| | **with body bias** | w/o bulk bias (same device size*) | Active body type LNA[11] | Body effect feedback[14] |
| Technology | **0.25um bulk** | 0.25um bulk | 0.35um SOI | 0.18 bulk |
| Frequency | **2.4GHz** | 2.4GHz | 1.9GHz | 1.65~2.5GHz |
| Bulk voltage | **0.5V** | VBS=0V | 0.5V | 0.6V |
| Supply Voltage | **1V** | 1V | 1V | 0.9V |
| Power Consumption | **3.17mA** | 3.5mA | 5mA | 2.5mA |
| S11 | **-20dB** | -20dB | - | - |
| Gain | **20.2dB** | 16dB | 7dB | 10dB |
| NF | **2.02dB** | 3dB | 5.6dB | 1.34dB |
| P-1dB | **-10dBm** | -13dBm | -4.5dBm | -16dBm |

## 1.3 Motivation

TSMC 0.25-um 1P5M 2.5V process is ripe, cheaper and stable in today's application. Its standard supply voltage is 2.5V. Most of portable system consuming low power has become a new trend in circuit design. This thesis tries to realize a 1-V low voltage receiver circuit fabricated by TSMC 0.25-um for low voltage and low power application. Besides, the headroom of design circuit will be degraded because of its threshold voltage too high. The gain and linearity are limited by its intrinsic performance. Using body-bias in LNA can solves the drawback of voltage drop down but the performance of MOS device is improved.

## 1.4 Thesis organization

In this chapter, the thesis discussed about the principle of different receiver architecture and their advantages and disadvantages. In the next chapter, chapter 2, it presents the design of receiver components in detail and their design considerations. Each component is divided to several sub sections and discussed the features and design considerations separately. The algorithm of image-reject process is also analyzed in this chapter. The implementation method and post-simulation results is completed. Chapter 3 contains experimental results and discussions. The measurement setup and environment is also introduced. Finally, conclusions and future works are described in chapter 4.

# CHAPTER 2

# CIRCUIT ARCHITECTURE AND SIMULATION RESULTS

## 2.1 SYSTEM ARCHITECTURE

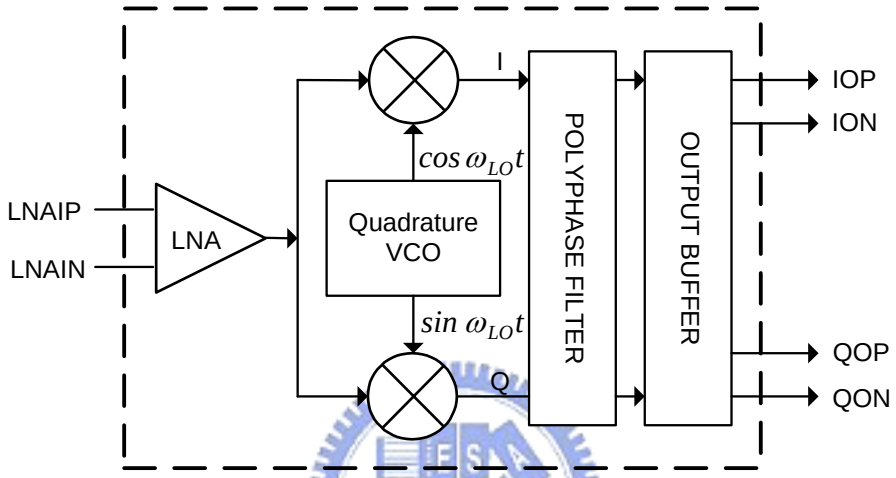



Fig. 2.1 System architecture

The block diagram of Low-IF receiver system architecture is shown in Fig. 2.1. The receiver architecture includes a low noise amplifier, quadrature VCO, quadrature mixer, polyphase filter, and an output buffer in the last stage.

LNA provides a high gain but low noise figure to amplify the RF signal. It amplifies the desired signal and suppresses noise interference. LNA also provides a 50Ω input matching for antenna and transmission line. The LNA is the frist stage of receiver system. It plays an important role on noise figure for whole receiver system. The LNA output transfers RF signal to next stage. The quadratuere mixer used to down-converts the RF signal to IF signal.

A quadrature VCO generates LO signals with 90-phase difference. As shown in Fig. 2.2, the quadrature LO signal is used to mixes with RF signal to generate IF I/Q signal.

The quadrature mixer stage follows the LNA. The quadrature mixer mixes RF signal and quadrature LO signals. The quadrature mixer is used to down-converts RF band to IF band and splits the IF band to I/Q phase difference. The mismatch of VCO and mixer can degrade the image rejection ratio.

Polyphase filter and output buffer is a complex filter in the last stage, which follows the RF mixer, used to suppress the image signal and employ a common source buffer to transfer the desired signal in IF band. The desired and image signals can be distinguished in phase relation and double-ended spectrum. The polyphase filter generally can be easily realized by passive R-C polyphase network. The main disadvantage is the signal loose. The receiver in this design used an active polyphase filter to solve the image signal and improve the linearity.

The common source output buffer must consider the linearity and used to drive the output load. It provides enough output power to drive the output capacitance and eliminate output loss as far as possible.

Layout and design strategies are considered to achieve high performance and image rejection ratio in this architecture. The whole chip floorplan, mismatch, The symmetry of differential circuit, robust power line, and signal transmission line are the key points to eliminate the ill effect in layout.

## 2.2 OPERATIONAL PRINCIPLE

This section describes the principle of the receiver, it presents how the receiver down-converts RF band signal to IF band signal. It also shows the image cancellation methodology.

The typical function of downcoversion is to do a multiplication operation. It assumes the RF signal is $e^{j\omega_{RF}t}$ and the LO signal is $e^{j\omega_{LO}t}$. To multiply these two signal and input to an analog multiplier. Then the mixer generates an IF frequency

$\omega_{RF} - \omega_{LO}$. i.e. $\omega_{IF} = \omega_{RF} - \omega_{LO}$. The following are the mathematical representations with an assumption of $\omega_{RF} > \omega_{LO}$, to multiply the RF and LO signal with exponential equation (1).

$$e^{j\omega_{RF}t} \times e^{-j\omega_{LO}t} \rightarrow e^{j\omega_{IF}t} \tag{1}$$

It is an easy way to expand the equation by Eulers's formula, exponential function and Euler's formula act as an important role on the discussion of complex signal. After the Eulers's formula transformation, the operation of mixer operation can be rewritten as follow.

$$\begin{aligned} &(\cos\omega_{RF}t + j\sin\omega_{RF}t)\bullet(\cos\omega_{LO}t - j\sin\omega_{LO}t) \\ &= (\cos\omega_{RF}t\bullet\cos\omega_{LO}t + \sin\omega_{RF}t\bullet\sin\omega_{LO}t) \\ &\quad + j(\sin\omega_{RF}t\bullet\cos\omega_{LO}t - \cos\omega_{RF}t\bullet\sin\omega_{LO}t) \\ &= \cos(\omega_{RF} - \omega_{LO}) + j\sin(\omega_{RF} - \omega_{LO})t \\ &\rightarrow \cos\omega_{IF}t + j\sin\omega_{IF}t \end{aligned} \tag{2}$$

From the equation (2), Quadrature RF signal is multiplied with quadrature LO signal. The procedure generates quadrature IF signal on the output terminal of I-channel and Q-channel. I-channel corresponds to the real part of complex signal and Q-channel corresponds to the imaginary one. I-channel and Q-channel are always with 90-degree phase difference in an identical frequency.

The operation of signal multiplication in frequency domain depicts on Fig. 2.2. The equation (1) and (2) can be described and signify in block function diagram, which is shown in Fig. 2.3.

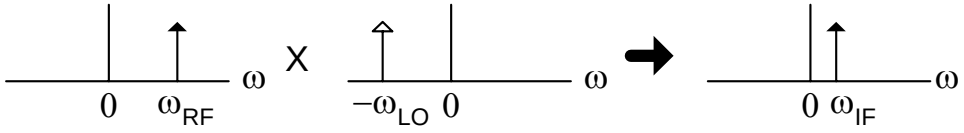



Fig. 2.2 Operation of downconversion

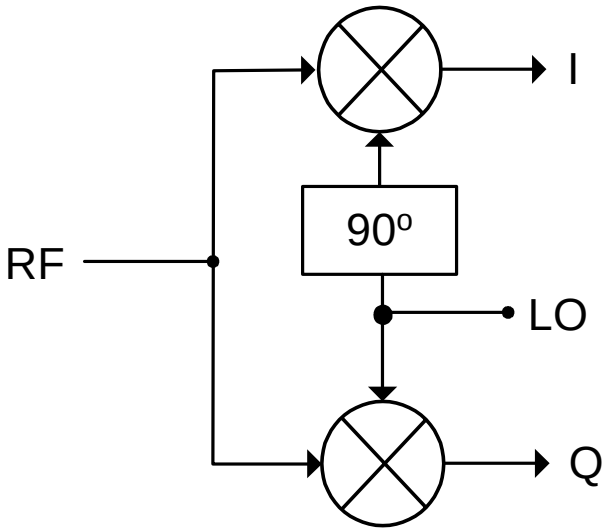



Fig. 2.3 IF quadrature I/Q signal generator

It presented how the equation (2) to be implemented in frequency domain. The quadrature VCO applies I/Q quadrature LO signal with 90-degree phase difference and multiplied with RF input signal. The LO quadrature signal can be denoted to $\cos\omega_{LO}t$ and $\sin\omega_{LO}t$. The operation of Low-IF block diagram is shown in Fig. 2.4.

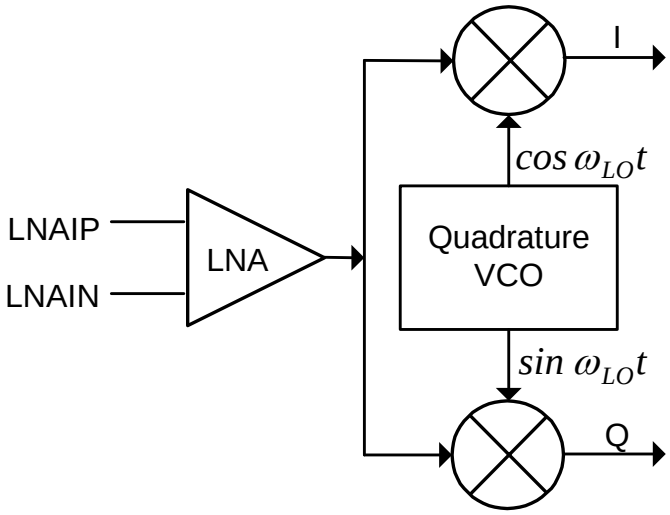



Fig. 2.4 Low-IF quadrature downconverter

**Image-reject process.**

If there exist an image signal $e^{j\omega_{IM}t}$, the image frequency has the same frequency. After down-conversion processing, it can be denoted by $\omega_{IF} = \omega_{RF} - \omega_{LO}$ and $\omega_{IF} = \omega_{LO} - \omega_{IM}$ separately, where the $\omega_{IM}$ is the image frequency. The below mathematical equation representations the image signal mixes the LO signal with an assumption of $\omega_{IM} < \omega_{LO}$,

$$e^{j\omega_{IM}t} \times e^{-j\omega_{LO}t} \rightarrow e^{-j\omega_{IF}t} \tag{3}$$

By Euler's formula, the down-conversion procedure can be rewritten as.

$$\begin{aligned} &(\cos\omega_{IM}t + j\sin\omega_{IM}t) \bullet (\cos\omega_{LO}t - j\sin\omega_{LO}t) \\ &= (\cos\omega_{IM}t \bullet \cos\omega_{LO}t + \sin\omega_{IM}t \bullet \sin\omega_{LO}t) \\ &\quad + j(\sin\omega_{IM}t \bullet \cos\omega_{LO}t - \cos\omega_{IM}t \bullet \sin\omega_{LO}t) \\ &= \cos(\omega_{IM} - \omega_{LO}) + j\sin(\omega_{IM} - \omega_{LO})t \\ &\rightarrow \cos\omega_{IF}t - j\sin\omega_{IF}t \end{aligned} \tag{4}$$

The signal mixing procedure generates quadrature IF signal on the output terminal of I-channel and Q-channel. The output IF frequency is $\omega_{IF}$. The frequency is similar to $\omega_{RF}$ signal mixes with LO signal, which is represented in previous equation (2). Image IF signal contains negative sine function on Q-channel. It should be known that a quadrature image rejection filter must distinguish the desired signal $\omega_{RF}$ and undesired image signal $\omega_{IM}$ by complex filter. The polyphase filter is usually implement to act as the complex filter to reject the image signal.

## 2.3 CIRCUIT DESIGN

### *2.3.1 Body-biased low noise amplifier (LNA)*

Low noise amplifier (LNA) is the first stage of the receiver system. The architecture of LNA proposed in this thesis is inductive source degeneration with body-bias scheme. In order to operate at 1-V power supply, the body-bias is applied in cascode input stage. The body-bias is used to improve the voltage headroom, linearity and noise factor.

The performance of the LNA is optimized by properly choosing the size of the input and cascade transistors. This strategy can also minimizes noise as possible as for the system.

There are several common goals in design of LNA. These include input impedance matching, higher power gain, minimizing the noise figure, sufficient linearity, and small power consumption. Otherwise, it also provides 50Ω input matching for antenna input.

**A. Body-biased design**

In order to decrease the threshold voltage of cascade input devices and improve the operation headroom, body-bias voltage is implemented in the LNA design. The body-bias must be supplied in terminal of NMOS bulk that is separated from other NMOS devices. TSMC 0.25um provides an effective method to separate the NMOS substrate that is deep N-well process. The P-well in DEEP NWELL is called RW. It isolates the P-well from other NMOS devices. That not only cancels the NMOS body effect but also the body-bias supplied to the terminal of NMOS bulk independently. The Fig. 2.11 illustrates how the single end cascode NMOS place on deep N-well with body-bias circuit. Fig. 2.5 illustrates the cross section of the LNA input cascade stage. The junction model of MOS device is not

well defined. We must pay attention to the design guard band and sensitive to process variation.

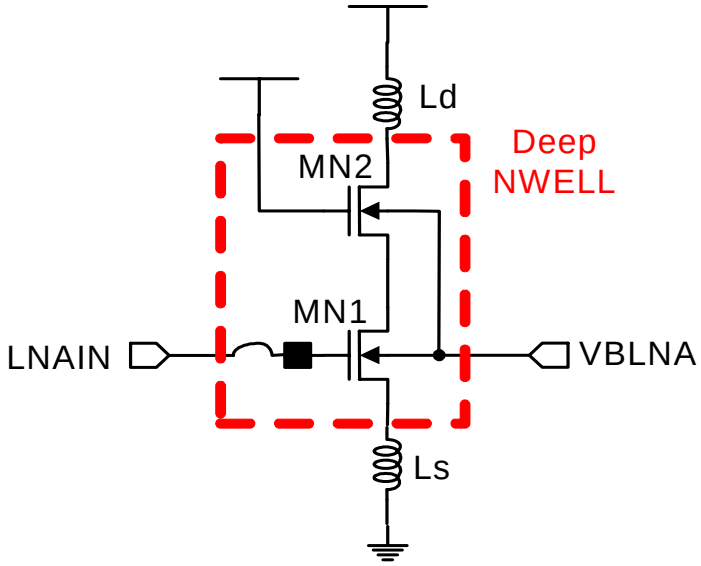



Fig. 2.5 Single end cascode NMOS place on Deep N-well with body-bias

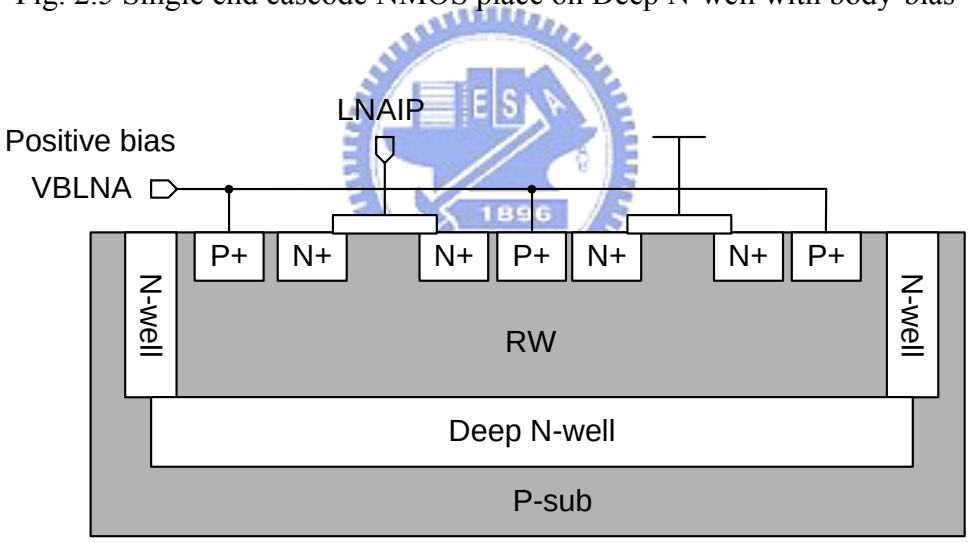



Fig. 2.6 Cross section of cascode NMOS place on deep N-well

Shown in Fig. 2.6, it provides a positive body-bias (VBLNA) voltage to the terminal of NMOS bulk. Then a forward parasitic PN junction will be created. It generates a forward current when the body-bias (VBLNA) greater than the PN junction on voltage. A forward current induced into source or drain of the NMOS. This causes the NMOS input stage operation point shift. For this reason, the gain of LNA will be degraded. The top curve of Fig. 2.7 shows the threshold voltage

decrease if VBLNA increase. The bottom curve of Fig. 2.7 shows the $I_{BS}$ forward current is created if the forward VBS voltage VBLNA greater than about 0.7V.

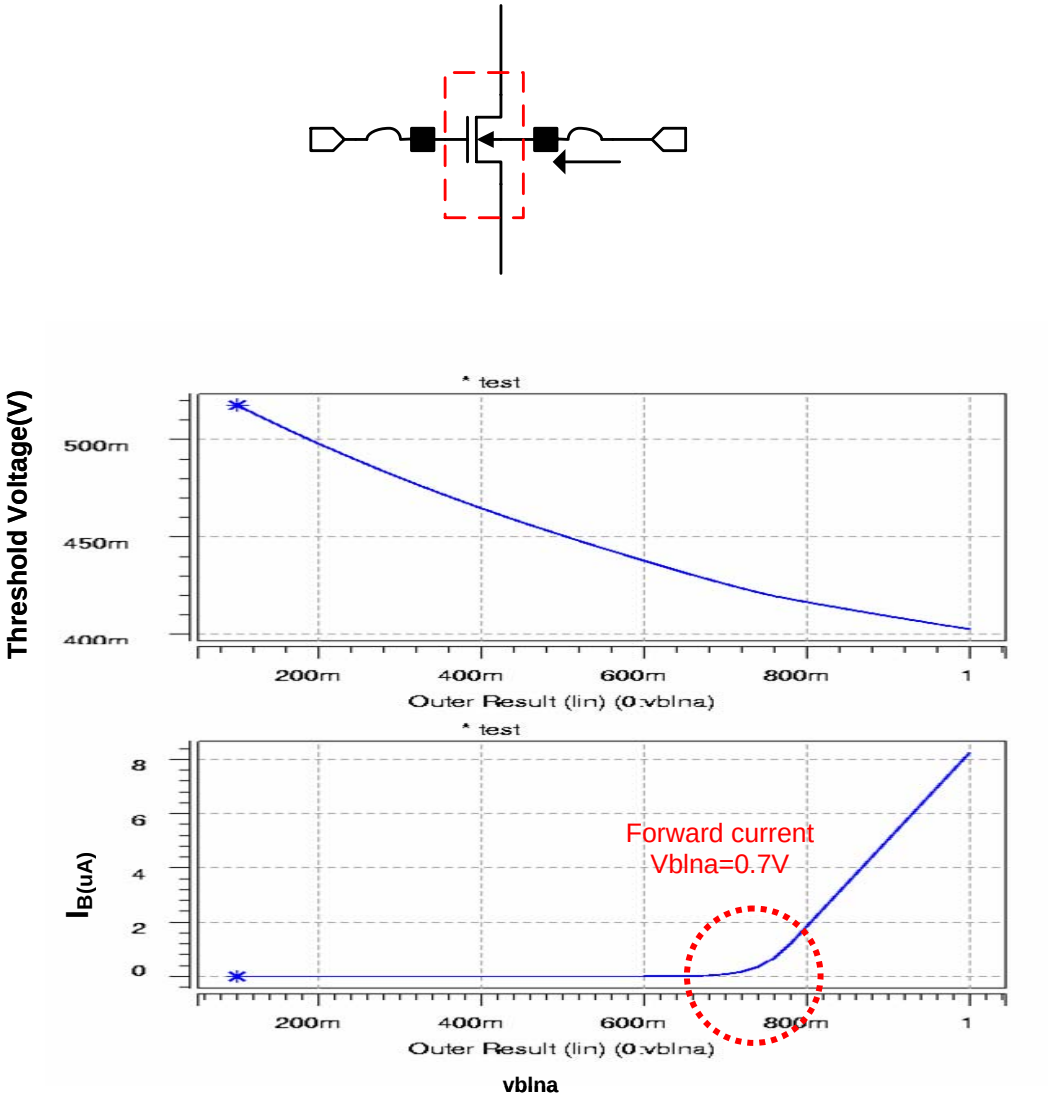



Fig. 2.7 The deviation of threshold voltage and forward current

The drain current $Id$ of MOSFET is $Id = K(V_{GS} - Vth)^2$ where K and Vth ater the gain factor and the threshold voltage, respectively. In order to obtain a large gain, the current increased. However, the supply voltage is lowered, the drain current is limited. The body of the transistor is connected to the bias voltage. The Vth of the transistor is $Vth = Vtho + \gamma\left[\sqrt{|2\phi_F - V_{BS}|} - \sqrt{|2\phi_F|}\right]$, where $Vtho$ is

the threshold voltage for body-source voltage, VBS=0V, $\gamma$ is body-effect coefficient, $\phi_F$ is the bulk potential. As the gate-source voltage (VGS) must be not less than 0V. The threshold voltage becomes smaller due to the body biased effect and this leads to a larger drain current. The transconductance factor (gm) of the body-biased LNA is larger than conventional LNA. The ratio of the gm to gm0, which is the transconductance factor when the body biased at the source, is

$$\frac{gm}{gm0} = \frac{\left(V_{GS} - Vth0 - \gamma\left[\sqrt{\left|2\phi_F - V_{BS}\right|} - \sqrt{\left|2\phi_F\right|}\right]\right)\cdot\left(1 + \frac{\gamma}{\sqrt{\left|2\phi_F - V_{BS}\right|}}\right)}{\left(V_{GS} - Vth0\right)}$$

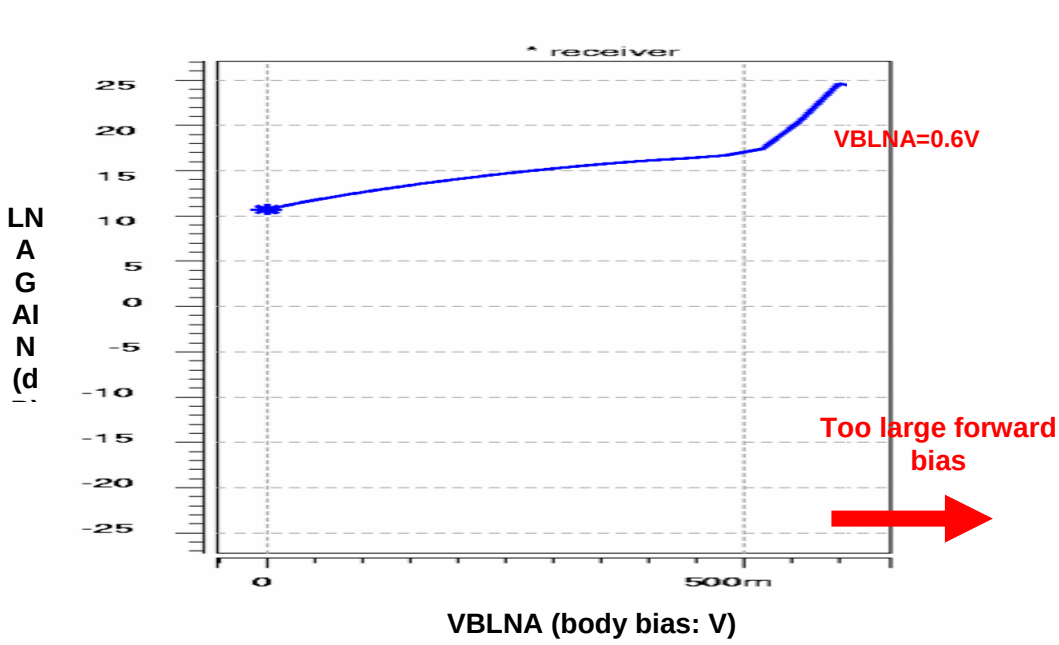



Fig. 2.8 body-bias voltage vs. LNA gain

Fig. 2.8 shows the gain of LNA increase if VBLNA increase. The junction forward current destroys the DC operating point of input stage devices and it further decrease the gain of LNA. From the transfer curve of LNA gain with sweep the bias voltage, the best body-bias (VBLNA) is about the range from 0.4V to 0.6V. If The VBLNA greater than 0.6-V will cause the gain of LNA decrease.

Fig. 2.9 illustrates the frequency response of LNA with difference body-bias voltage.

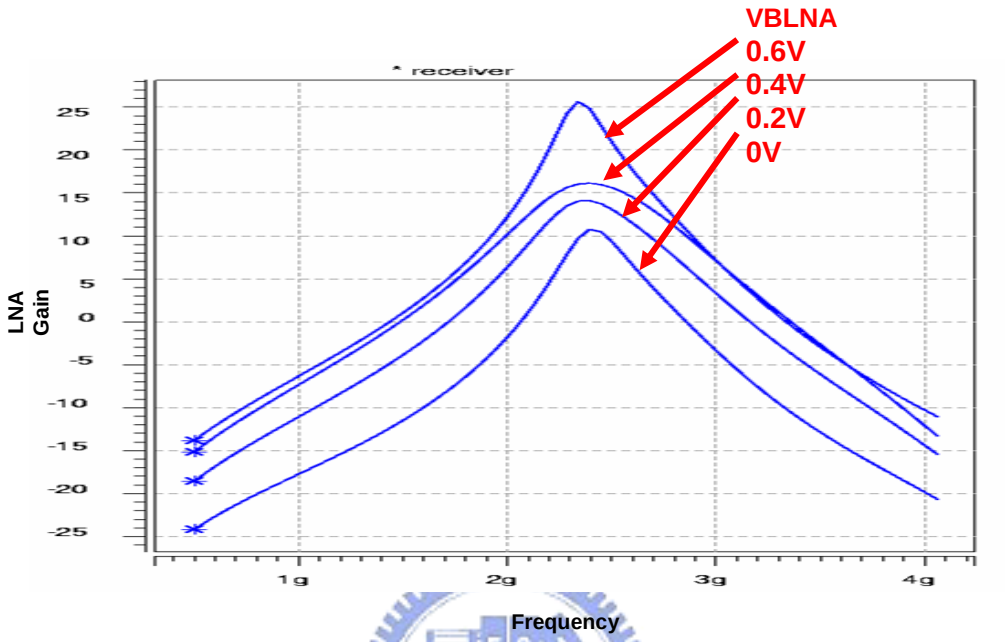



Fig. 2.9 LNA gain with difference body-bias

**B. Input matching**

There are four kinds of common architectures used in input matching of LNA. Fig.2.2 illustrates four kinds of input matching circuit. They are resistive termination, 1/gm termination, shunt-series feedback and inductive degeneration.

Illustrate in Fig. 2.10(a), The resistance termination shunt with input port to provide a 50Ω resistance. The use of real resistor has a poor noise figure. The resistor in this fashion has a deleterious effect on LNA's noise figure. A second The NF of 1/gm termination is usually larger than 3dB. Shunt-series feedback needs on-chip resistors of reasonable quality. It also often has higher power to provide high gain. The shunt-series feedback approach is not suitable for this work. The inductive degeneration usually has best quality and small noise in this LNA design.

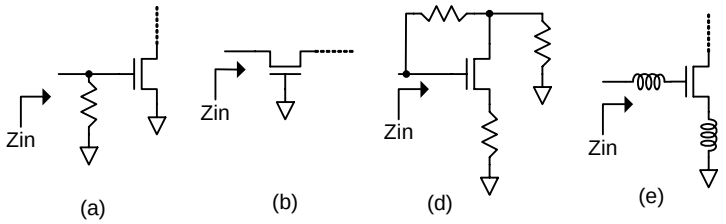



Fig. 2.10 (a) Resistive termination (b) 1/gm termination
(c) shunt-series feedback (d) inductive degeneration

Fig. 2.11 is the input stage equivalent circuit of source degeneration cascode low noise amplifier.

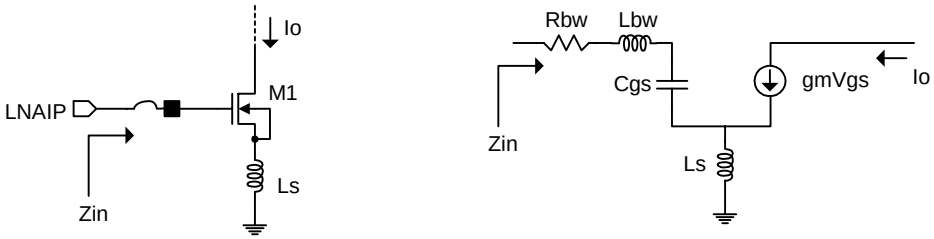



Fig. 2.11 The small signal model of Input impendence matching

To simplify the analysis, we consider the device model that expands to the equivalent circuit of small signal. It is illustrated in right side of the fig. 2.2. It can be show that the input impedance of the circuit is shown as follow:

$$Zin(s) = \frac{Vs}{Is} = \frac{sCgs(R_G + sLg)\cdot Vgs + (gmVgs + sCgsVgs)\cdot sLs}{sCgsVgs}$$

$$= R_G + sLg + \frac{1}{sCgs} + \left(\frac{gm}{Cgs}\right)\cdot Ls + sLs$$

$$= s(Lg + Ls) + \frac{1}{sCgs} + \left(\frac{gm}{Cgs}\right)\cdot Ls + R_G \qquad (5)$$

At the resonate frequency, that is Zin(i)=0 then

$$s(Lg + Ls) + \frac{1}{sCgs} = 0 \qquad (6)$$

Alternately,

$$\omega_o = 2\pi f_o = \frac{1}{\sqrt{(Ls + Lg)Cgs}} \tag{7}$$

From this equation, to evaluate can get the Lg value.

in the real part of Zin, Zin(r)=50Ω

$$Zin = \left(\frac{gm}{Cgs}\right) \cdot Ls = \omega_t Ls = 50\Omega \tag{8}$$

Ls value can be evaluated from this equation.

Replace the gm/Cgs with mos cut-off frequency, i.e. $ft = \frac{gm}{Cgs}$

$$Cgs = K' \cdot W \tag{9}$$

From this equation, we can see the Zin=50 are related to the mos cut-off frequency.

The parasitic of a output pad and bond-wire loading are modeled by a resistance series an inductor and parallel a PAD capacitance; the PAD capacitance is connected to substrate. This model is illustrated in Fig. 2.12. The bond-wire impendence also compensates the input impedance to fit the 50Ω matching. After adjust the bond-wire inductance and capacitance, The low-noise amplifier has best S11 performance.

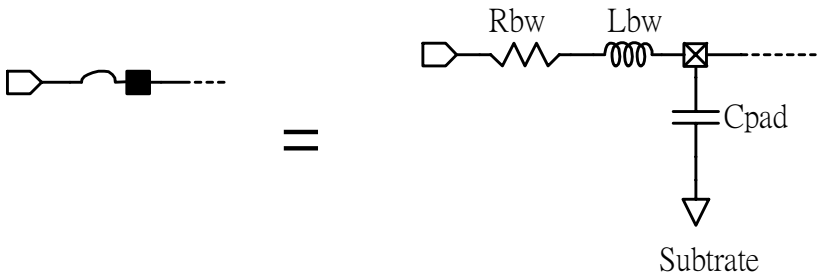



Fig. 2.12 Parasitic circuit model of a pad capacitance and bond-wire

**C. Voltage gain and linearity**

For LNA design, Linearity and gain are usually tradeoffs in general condition. The gain generally designed in appropriate range of 15~20dB in a conventional LNA for wireless communication. Fig 2.13 shows the model of LNA small signal analysis equivalent circuit.

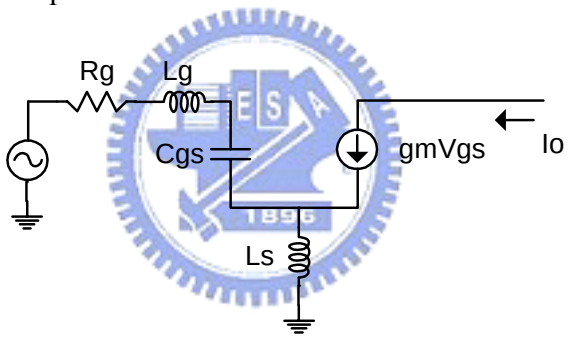



Fig. 2.13 LNA Gmeff small signal analysis equivalent circuit

$$i_o = gm \cdot Vgs$$

$$Ve = (sCgsVgs + gmVgs) \cdot sLs$$

$$Vin = sCgsVgs(Rs + sLg + \frac{1}{sCgs}) + sLs(Vgs \cdot sCgs + gmVgs)$$

$$= Vgs\left[s^2 Cgs(Ls + Lg) + s(CgsRs + gmLs) + 1\right]$$

$$G_{meff} = \frac{io}{Vs} = \frac{gm}{s^2 Cgs(Ls + Lg) + s(CgsRs + gmLs) + 1} \qquad (10)$$

At the resonate frequency, we can get the effect transconductance in equ. (11)

$$\omega_o = \frac{1}{\sqrt{Cgs(Ls+Lg)}}$$

$$|Gmeff| = \frac{gm}{\omega(CgsRs+gmLs)} = \frac{\omega_t}{\omega Rs\left(1+\frac{\omega_t Ls}{Rs}\right)} = \frac{\omega_t}{2\omega R_s} \qquad (11)$$

**D. Noise Optimization.**

This subsection describes noise performance on the inductor-degeneration configuration and designing an optimal dimension of the MOS devices for minimal noise contribution. Noise figure is an important specification in LNA design. In the cascade network of multi-stage, first stage plays an important role to reduce the total noise figure of the receiver system. The LNA is the first stage of the receiver system. In general, LNA noise figure determine the receiver sensitivity.

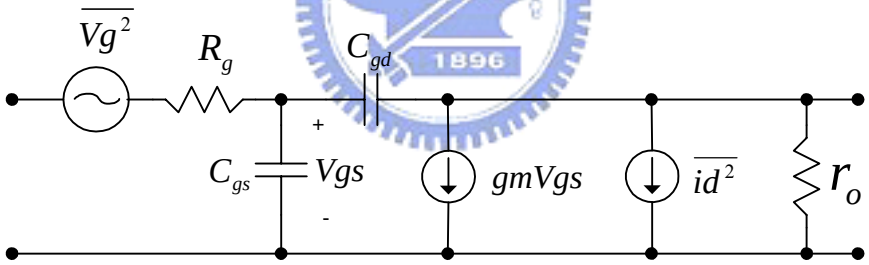



Fig. 2.14 small signal noise model of MOS device

Fig. 2.14 shows a small signal noise model of the input stage, Rg is gate resistance and Rs is voltage source resistance; Rg can be minimized by good layout. Where $\overline{Vg^2}$ and $\overline{id^2}$ are induced by Rs and channel resistance respectively. Thermal noise and gate current noise are main source in LNA design. Especially the channel thermal noise is dominant. The equation $\overline{id^2}$ is listed in (9).

$$\overline{id^2} = 4kTB\gamma g_{d0} \qquad (12)$$

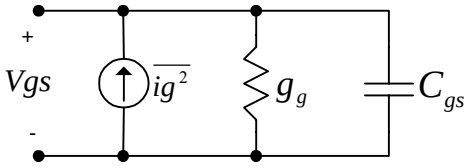



Fig. 2.15 Equivalent gate circuit

A equivalent gate circuit model is shown in Fig.2.15. A shunt noise current $\overline{ig^2}$ and a shunt conductance $g_g$ have been added. At resonance frequency, the small signal revised noise model is shown in Fig. 2.16.

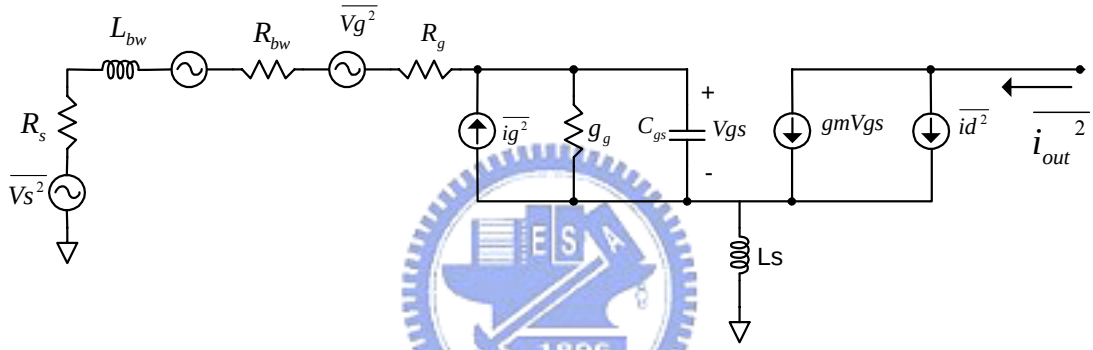



Fig. 2.16 Revised Noise model

$$F = 1 + \frac{R_{bw}}{R_s} + \frac{R_g}{R_s} + \frac{\gamma g_{d0} R_s \omega^2 C_{gs}^2}{g_m^2} \tag{13}$$

$$F = 1 + \frac{R_{bw}}{R_s} + \frac{R_g}{R_s} + \gamma g_{d0} R_s \left(\frac{\omega}{\omega_T}\right)^2 \tag{14}$$

A common form of the noise factor is listed in equ. (13). It is re-arranged to equ. (14). It is observed that It can further decrease noise factor by to reduce $g_{d0}$. To achieve low noise factor involves linearity tradeoff. Besides, the technology scaling is a key.

$$F = 1 + \frac{R_{bw}}{R_s} + \frac{R_g}{R_s} + \gamma g_{d0} R_s \left(\frac{\omega}{\omega_T}\right)^2 \left\{1 + 2\sqrt{\frac{\delta\alpha^2}{5\gamma}} Q_L |c| + \frac{\delta\alpha^2}{5\gamma}\left[1 + Q_L^2\right]\right\} \tag{15}$$

## E. Low-Noise Amplifier Circuit Implementation

The new LNA with body-bias circuit is proposed in this thesis. The LNA uses common-source degeneration cascode with fully differential configuration. Shown in Fig. 2.17, its device size is listed in table I. MN1, MN2 provide the enough gain and noise optimization. MN1, MN2, LS1 and LS2 are designed to optimize the input matching. MN3, MN4 isolate the input RF signal input and LNA output. LD1, LD2 and CC1, CC2 provides impedance for voltage gain in resonate frequency.

The body-bias is applied for MN1, MN2, MN3 and MN4. For this reason, these devices are placed in a deep-NWELL structure to isolate with other NMOS P-substrate. The body-bias scheme can further decrease the threshold voltage and improve the gain and linearity.

All inductors are spiral inductor supplied by TSMC 0.25-um technology. A sub-circuit in HSPICE simulation models the behavior of inductor, MIM capacitance.

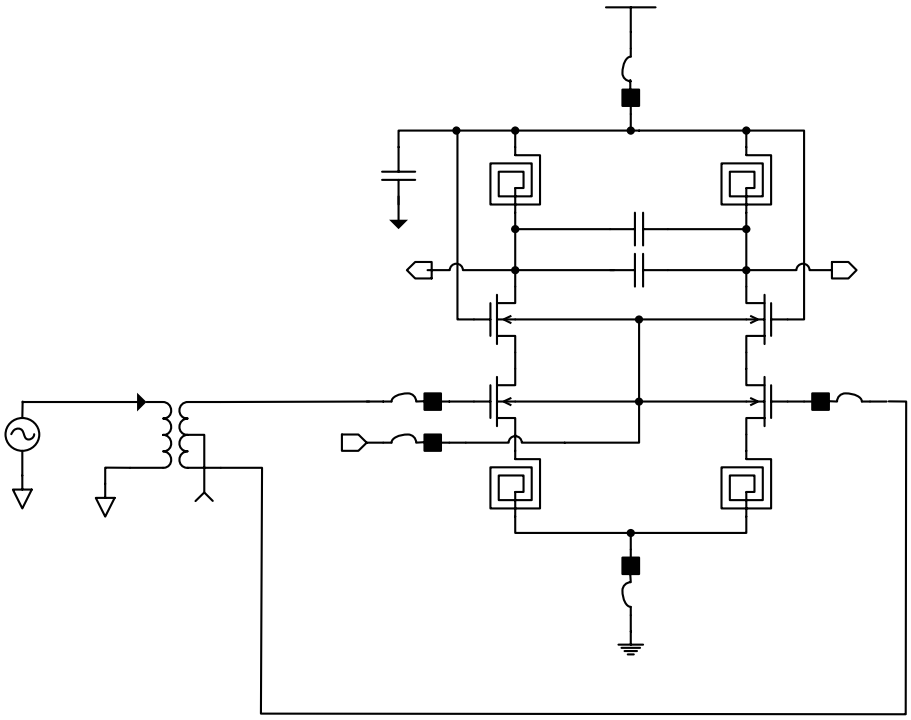


Fig. 2.17 LNA circuit

| Device Name | W/L(um/um) |
|---|---|
| MN1,MN2 | 120/0.24 |
| MN3,MN4 | 10/0.24 |
| XLS1,XLS2 | 2.5n |
| XLD1,XLD2 | 4.7n |
| CC1,CC2 | 0.1p |

Table 2.1 LNA device parameter

### *2.3.2 Quadrature voltage control oscillator*

This receiver involves the design of circuit to generate a quadrature LO signal with 90-phase difference. The most popular method is to use a voltage-controlled oscillator (VCO), which is usually in the form of the LC-tank. High frequency oscillator usually comprises a resonator, which includes inductor, capacitor, and negative resistor. Fig. 2.18 illustrates the standard circuit of typical resonator. In order to generate quadrature LO signal, a structure of VCO based on even-stage ring oscillator usually be used.

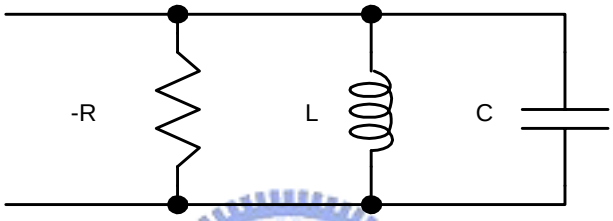



Fig. 2.18 Typical RLC tank

Fig. 2.9 is the conceptual block diagram of the quadrature VCO. This structure is like as a two-stage ring oscillator. INV1 and INV2 are identical fully differential inverter. The ring oscillator was combined with two fully differential inverters. Finally, The inverters connect to LC-tank load and a negative resistor respectively.

Fig. 2.19 further depicts the fully differential inverter with LC-tank and negative resistor. MN5 and MN6 act as the negative resistor to cancel the parasitic resistor. Two spiral inductor and varactor decide the frequency of oscillator. MN1 and MN2 act as fully differential inverter. The inverter output terminal is VO1 and VO2. Two identical inverters are combined together for two-stage ring-oscillator. To observe the output DC level can bias at VDD.

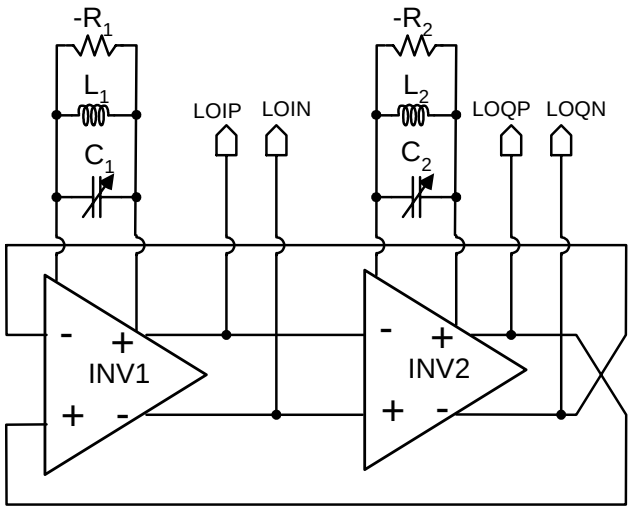



Fig. 2.19 Conceptual block diagram of the quadrature VCO

The fully circuit of quadrature voltage-controlled oscillator in this thesis is shown in Fig. 2.21. The output terminal of VCO connected to next stage(mixer) directly.

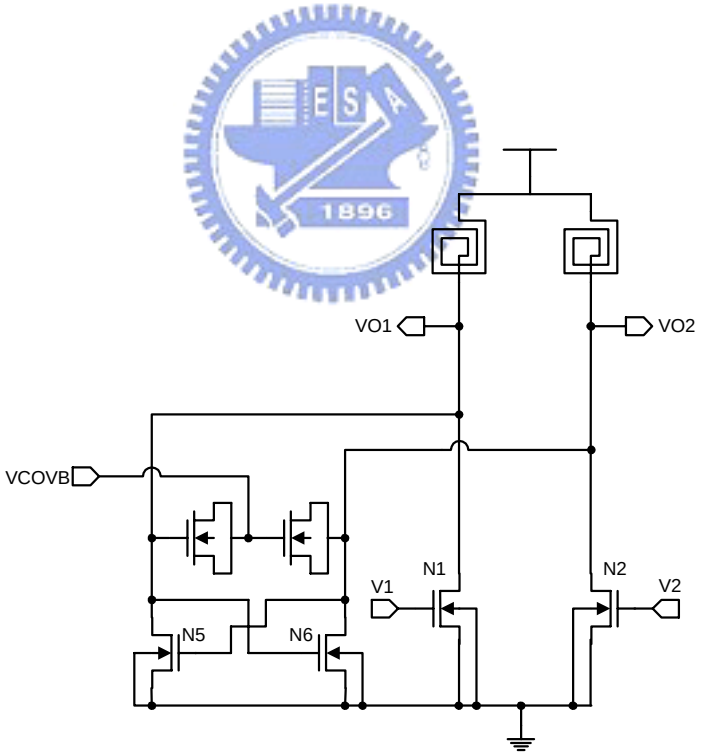



Fig. 2.20 Fully differential inverter with LC-tuned in the quadrature VCO

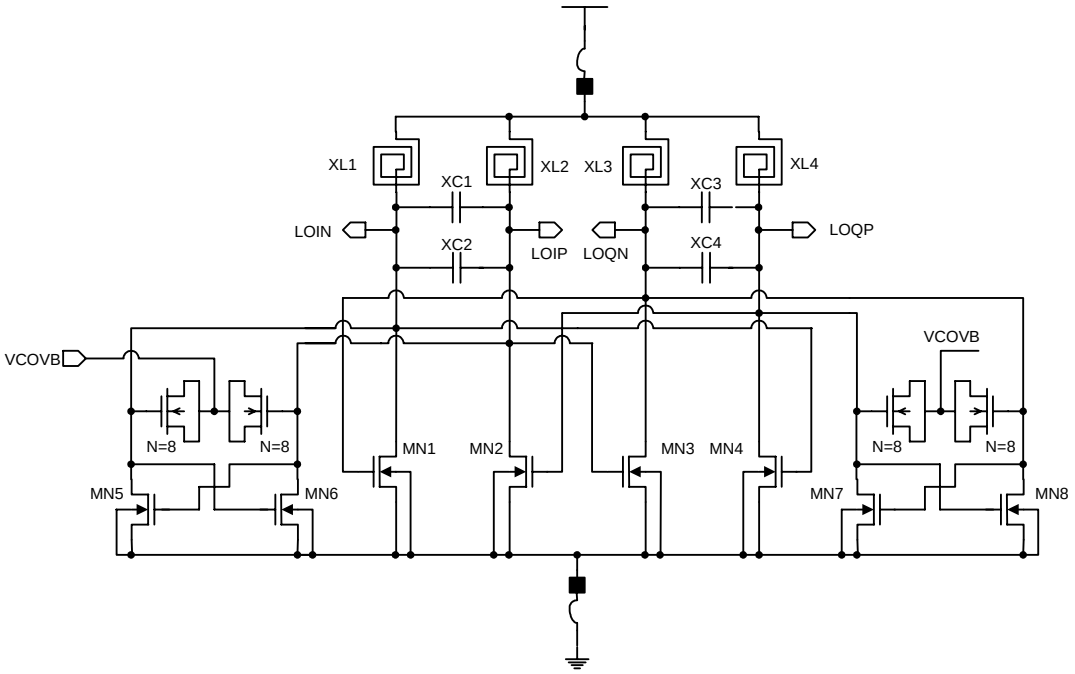



Fig. 2.21 The whole circuit of quadeature voltage-controlled oscillator circuit

| Device Name | W/L(um/um) |
|---|---|
| MN1,MN2,MN3,MN4 | 10/0.36 |
| MN5,MN6,MN7,MN8 | 40/0.24 |
| XL1,XL2,XL3,XL4 | 2.5n |
| XLD1,XLD2 | 1.05n |
| XC1,XC2,XC3,XC4 | 0.049p |

Table 2.2 QVCO device parameter

### *2.3.3 Quadrature mixer*

This section discussed the principle and design methodology of the downconverter mixer. Consider the Fig. 2.22, refer the drain current of basic unit PMOS cell. By means of the PMOS drain current operating equation in saturation, the mixer can achieve the mixing operation.

PMOS is a basic unit cell in this mixer design. First, we can observe that the PMOS current is the function of gate to drain voltage in saturation region.

$$I_d = K(Vgs - Vt)^2 \tag{16}$$

Where the constant K is

$$K = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right) \tag{17}$$

In order to simplify the following analysis and to make it clearly, replace the gate and drain terminal to ‘Va’ and ‘Vb’ respectively. The drain current of the PMOS device can be written as

$$I_d = K(Vgs - Vt)^2 = K[(Va^2 - 2Va \cdot Vb + Vb^2 - 2(Va - Vb) \cdot Vt + Vt^2] \tag{18}$$

Thus, the voltage of Vmx1 shown in Fig. 2.22 will become (Vt is replaced by constant value C )

$$Vmx1 = I_d \times Z_L = KZ_L[(Va^2 - 2Va \cdot Vb + Vb^2 - 2(Va - Vb) \cdot C_1 + C_2] \tag{19}$$

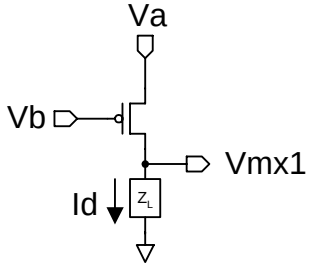



Fig. 2.22 Basic PMOS unit cell of mixer

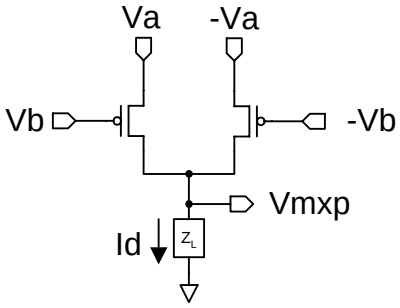



Fig. 2.23 Mix Va and Vb operation constructed by two basic PMOS device

Illustrate in Fig. 2.23, merge two basic PMOS unit cells as and summation the Id current flow through the $Z_L$. The Id current can be deriving as.

$$\begin{aligned} I_d &= K[(Va^2 - 2Va \cdot Vb + Vb^2 - 2(Va - Vb) \cdot C_1 + C_2] \\ &+ K[(Va^2 - 2Va \cdot Vb + Vb^2 - 2(-Va + Vb) \cdot C_1 + C_2] \\ &= 2(Va^2 + Vb^2) - 4Va \cdot Vb + 2C_2 \end{aligned} \tag{20}$$

$$Vmx2 = I_d \times Z_L = [2(Va^2 + Vb^2) - 4Va \cdot Vb + 2C_2]Z_L \tag{21}$$

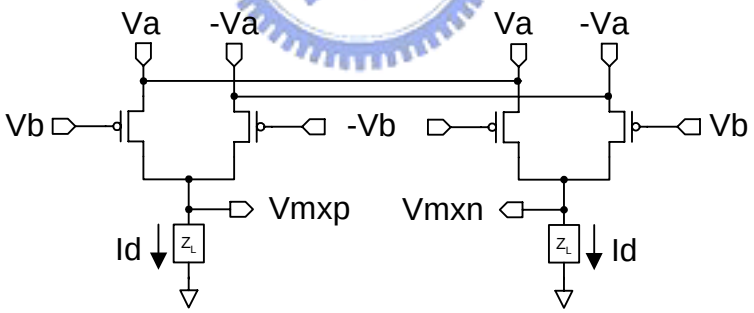



Fig. 2.24 double-balanced mixer structure

The Fig. 2.24 shows the double-balanced mixer structure.

$$\begin{aligned} Vmxp - Vmxn &= [2(Va^2 + Vb^2) - 4Va \cdot Vb + 2C] \cdot Z_L \\ &- [2(Va^2 + Vb^2) + 4Va \cdot Vb + 2C] \cdot Z_L \\ &= 8 \cdot Va \cdot Vb \end{aligned} \tag{22}$$

To replace the sign of equations. It can be Va=LOIP, -Va=LOIN, Vb=MXIP, -Vb=MXIN

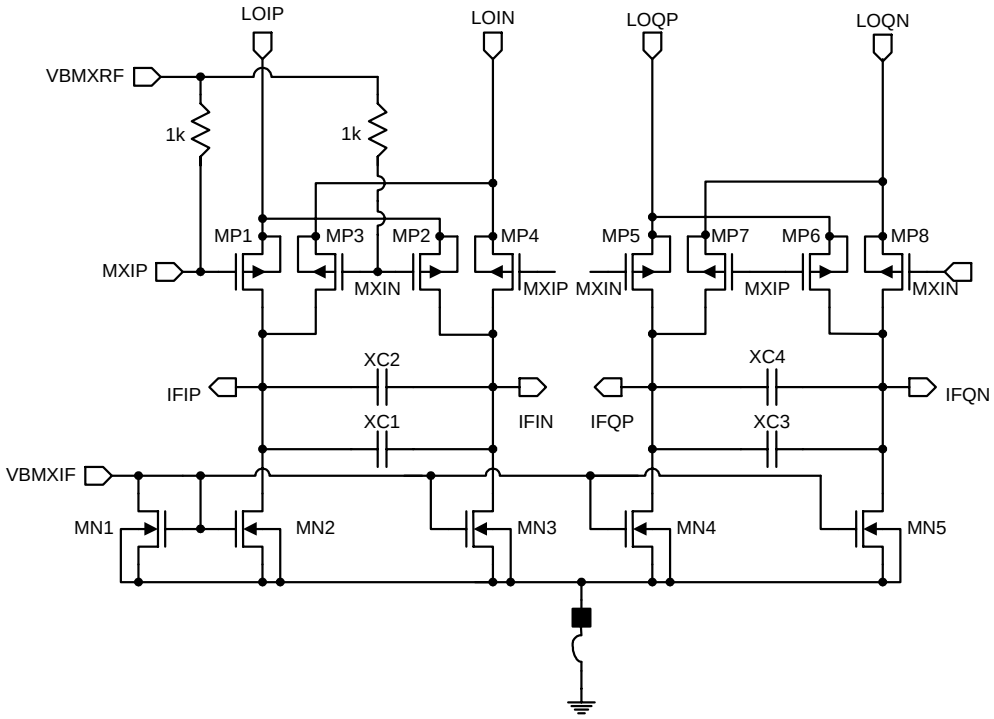



Fig. 2.25 Quadrature downconversion mixer schematic

| Device Name | W/L(um/um) |
|---|---|
| MP1,MP2,MP3,MP4, MP5,MP6,MP7,MP8 | 5/0.3 |
| MN1,MN2,MN3,MN4 | 10/0.24 |
| XC1,XC2,XC3,XC4 | 0.9p |

Table 2.3 Mixer device parameter

### *2.3.4 Active polyphase filter*

The polyphase filter and output buffer are the last stage of receiver front-end system. The polyphase filter stage that follows the mixer and selected the desired signal to output. The polyphase filter is used to reject image interference in a receiver front-end system. It must have the features with high image rejection ratio, low sensitivity to mismatching components, sufficient linearity, and low power consumption in the design of integrated RF front-end receiver. When the input signal is clockwise or positive frequency, the RF signal down converted IF signal passes to output. Contrary, the signal is anti-clockwise or negative frequency; the

filter should reject the image IF signal. In the application of monolithic integration, the polyphase filter design must be easily integrated in a receiver chip.

The polyphase filter is a complex filter; most of popular of polyphase filter is RC sequence network. It is comprise of two passive components, which are resistor and capacitance to do the filter operation. The center frequency of one-stage RC polyphase filter can be determined by $\omega = 1/RC$ for narrow band design. The amplitude of the output will be equal only at the input frequency. The transfer function of RC network depends on phase order of the input sequence. In order to prevent process variation and increase variation guard band, a multi-stage RC network can be used to achieve a broadband design. M-stage network can be constructed by cascading M-stage to expand the bandwidth of the filter. The 4-stage RC polyphase filter network is shown in fig. 2.26.

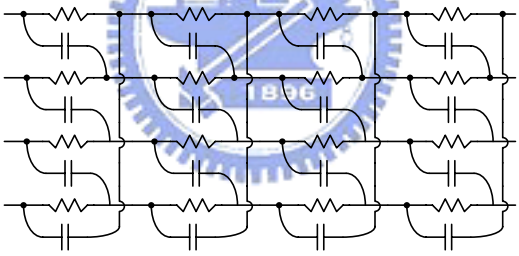


Fig. 2.26 4-stages RC network polyphase filter

The main disadvantage of the multi-stage RC polyphase filter is its signal loose. This will cause received signal decay and decrease the noise figure (NF) performance of the receiver system.

In this thesis, we use an active polyphase filter for the Low-IF receiver application. The advantages of the active polyphase filter are its high input impendence in each stage and provide enough gain to amplify the IF desired signal. It prevent the degradation of the gain lose. Besides, it eliminates the extra

power dissipation. Simultaneously, the high gain is assigned to the first stage to improve the better noise performance.

The main consideration of polyphase filter is its image rejection ratio (IRR), tolerance in process variation, bandwidth, linearity and power consumption.

As the transfer function of complex filter, this is similar to RC network polyphase filter to perform the positive or negative frequency filter. The filter must distinguish positive frequency and negative frequency. In the point of view in filter transfer function, it is combination of 1st order low-pass and high pass transfer function. The transfer function of a complex filter can be represented as.

$$H(\omega) = H_1(\omega) + jH_2(\omega) \tag{23}$$

Where $H_1(\omega)$ and $H_2(\omega)$ are real transfer function. If a complex signal $I(\omega) + jQ(\omega)$ is applied to this complex filter, the output signal $R(\omega)$ can be rewritten as

$$R(\omega) = I(\omega)H_1(\omega) - Q(\omega)H_2(\omega) + j(I(\omega)H_2(\omega) + Q(\omega)H_1(\omega)) \tag{24}$$

The block diagram of simple complex filter was presented in Fig. 2.27.

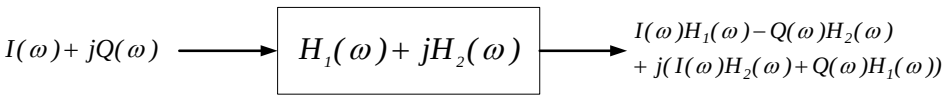



Fig. 2.27 The principle of complex filter

To expand the equation to first order high pass and low pass filter with single pole. The transfer function $H(s)$ can be represented as follow.

$$H(s) = H_1(s) + jH_2(s) = A \cdot \left( \frac{1}{s + \omega_p} + \frac{s}{s + \omega_p} \right) \tag{25}$$

Where A is the gain of the transfer function and $\omega_p$ is the position of single pole. $H_1(s)$ and $H_2(s)$ are the first order low pass and high pass equation. The image signal can be rejected by this equation at the frequency $\omega_p$. A 1-stage polyphase filter can be implemented by combination of first order low-pass and high-pass filter circuit.

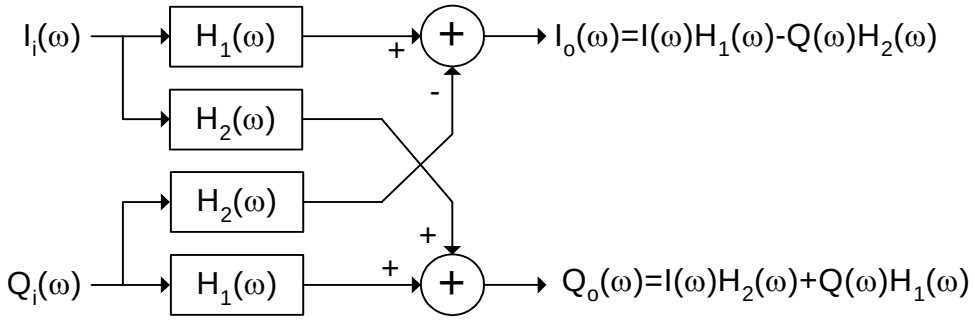



Fig. 2.28 Using real filter realize complex filter

In order to increase the tolerance of process variation, the bandwidth of filter must be expanded. Wide bandwidth can be achieved by cascade multi-stage.

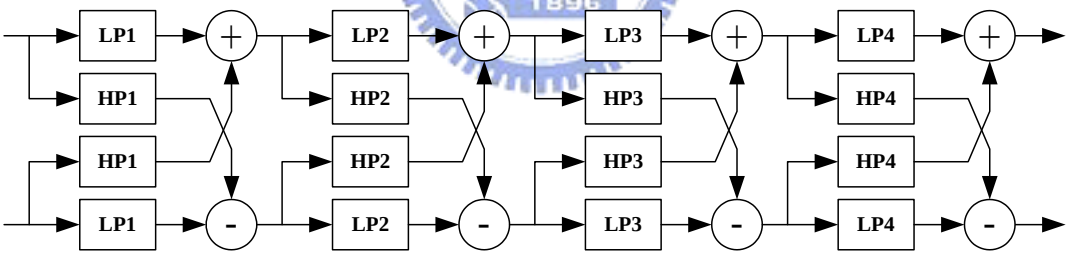



Fig. 2.29 The four-stage polyphase filter

This design implements a four-stage polyphase filter to expand the bandwidth and enhance the tolerances of process variation. Fig. 2.29 illustrates the four-stage polyphase filter design in this chip. The poles of each stage are difference to fine-tune the bandwidth and operating frequency. The poles are determined by changing CH for each one-stage polyphase filter.

The polyphase filter also provides enough gain to amplify the IF signal and prevent the best performance of linearity.

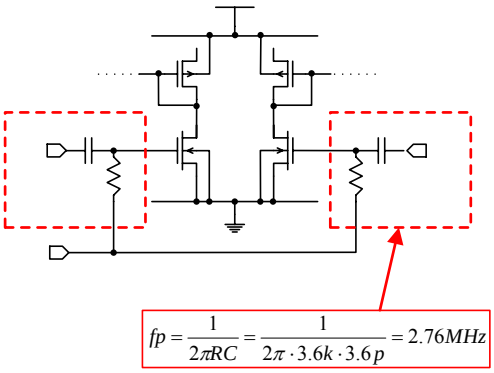



Fig. 2.30 Polyphase filter input bias.

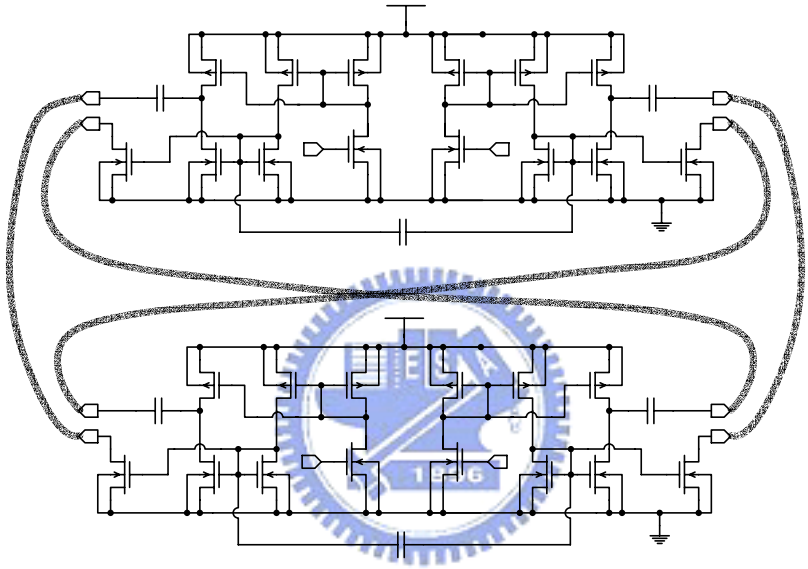


Fig. 2.31 1-stage polyphase filter

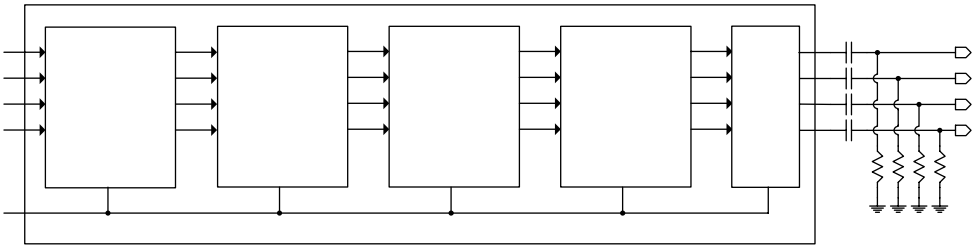


Fig. 2.32 4-stage polyphase filter

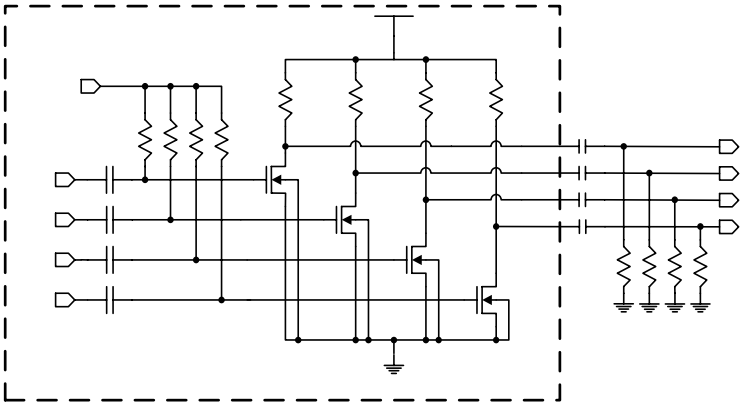


Fig. 2.33 output buffer

| Type | Passive Polyphase filter | Active Polyphase filter |
|---|---|---|
| pole | Decided by $\frac{1}{RC}$ | Decided by gm and C<br>HP:<br>$\frac{Vol}{Vp}=\frac{r\cdot\alpha\cdot gm_1\cdot(\frac{gm_1}{Ch})}{s+(\frac{gm_1}{Ch})}$<br>LP:<br>$\frac{Voh}{Vp}=\frac{r\cdot\alpha\cdot gm_1\cdot s}{s+(\frac{gm_1}{Ch})}$<br>(W/L)mp3=(W/L)mp4=$\alpha$ (W/L)mp1 |
| Device | RC | MOS, C |
| Area | Large area | Small area |
| Input impedance | Low input impedance | High input impedance |
| Gain | Lossy | Provide gain |
| Extra amplifier | Additional buffer | no need of extra amplifier |
| Power | More power for buffer | Smaller than passive filter |

Table 2.4 Compare with passive and active polyphase filter.

The mirrored current I3 is then divided into IL and IH by a diode-connected transistor MI, and a capacitor, CH, respectively. IL and IH can be derived as.

$$\frac{Vol}{Vp}=\frac{r\cdot\alpha\cdot gm_1\cdot(\frac{gm_1}{Ch})}{s+(\frac{gm_1}{Ch})} \qquad (26)$$

$$\frac{Voh}{Vp} = \frac{r \cdot \alpha \cdot gm_1 \cdot s}{s + (\frac{gm_1}{Ch})} \tag{27}$$

Where $\alpha$ is the value of (W/L)3/(W/L)1, and gml and gmh are the transcoductances of Ml and ML, respectively.

(W/L)mp3=(W/L)mp4= $\alpha$ (W/L)mp1

The bias voltage of each stage must adjust to gain a best performance of receiver. It is observed the positive frequency gain loss in lower frequency. It is because of the input stage HP filter. It is shown in Fig.2.30. The pole of the HP filter is about 2.76MHz. Lower pole frequency is best but it is trade-off between area and low pole. The Fig. 2.31 presents the circuit of 1-stage polyphase filter. Fig. 2.32 presents the circuit of 4-stage polyphase filter. The output buffer is shown in Fig.2.33.

Table 2.4 shows the comparison between passive and active polyphase filter. The main disadvantage of the multi-stage passive polyphse filter is that it is lossy, and thus received signal decays and the overall noise figure (NF) of the receiver is degraded. Additional buffer should be inserted among stage to overcome this drawback. However, additional buffer means it consumes extra power. Furthermore, a larger area is required to implementation numbers of passive resistors and capacitors in the RC polyphase filter.

## 2.4 RECEIVER REALIZATION

The designed receiver has been implemented on a single testchip; it comprises a body-biased LNA, a quadrature VCO, a quadrature mixer, polyphase filter and an output buffer. 1-V power supply design is a challenge on TSMC 0.25-um technology in many conventional circuit structure. The body bias VBLNA for LNA to gain the headroom of LNA.

All inductors employed are spiral inductors made of top thick metal; varactors are N-well structure; resistors are polysilicon with P-type implant. To avoid the body-effect, all N-mos device contain deep N-well for equal voltage between VBS. The model including spiral inductor, MIM capacitor, varactor and deep NWELL NMOS devices is supported by TSMC. The design is checked by LPE parasitic RC extraction based on TSMC's spice model document to evaluate the simulation results.

In order To avoid body effect of NMOS, all NMOS devices contain deep N-WELL to make VSB voltage is zero. All spiral inductors made of top thick metal; Varactors are N-WELL structure; resistors are made of polysilicon with p-type implant.

The buffer circuit as output stage follows the polyphase filter for measurement. The circuit comprises four common-source stage, following the four terminals of the polyphase filter respectively. The Fig.2.30 in next page presents the complete schematic of proposed Low-IF receiver.

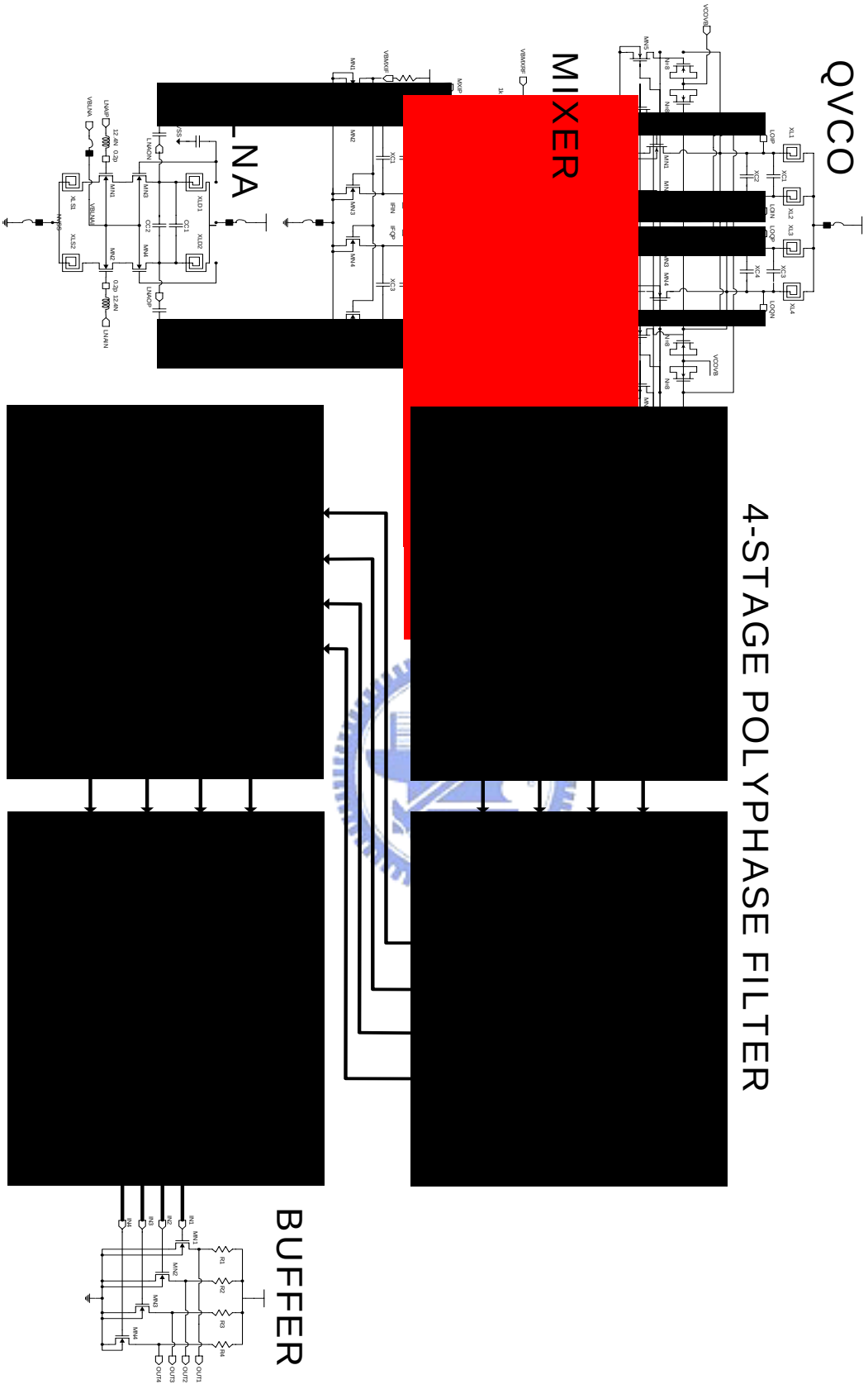



Fig. 2.34 whole chip of receiver schematic

## 2.5 SIMULATION RESULT

The receiver chip is simulated by HSPICE. Post-simulation is completed by HSPICE with spice model of TSMC .25-um 1P5M process. This section presents the post-simulation results of all circuit constructing the receiver.

**A. Low noise amplifier**

LNA is the first stage of the receiver; it provides input matching, voltage gain and low noise contribution for the receiver. Fig. 2.31 and Fig. 2.32 show the simulated input matching (S11) lower than –20dB and voltage gain higher than 20dB, respectively.

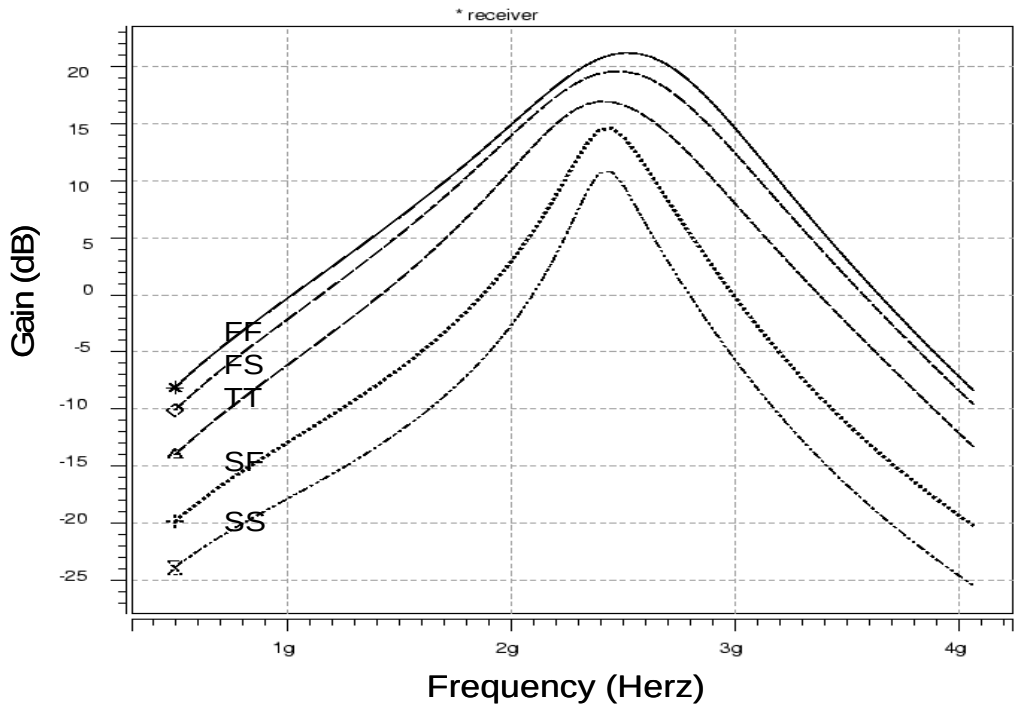



Fig. 2.35 simulated voltage gain of the LNA

This fig.2.35 shows the dependence of gain due to process variation. The gain is about 12dB in worst case SS corner simulation. The gain of LNA can guarantee at least larger than 10dB for five corner simulation and meet the specification.

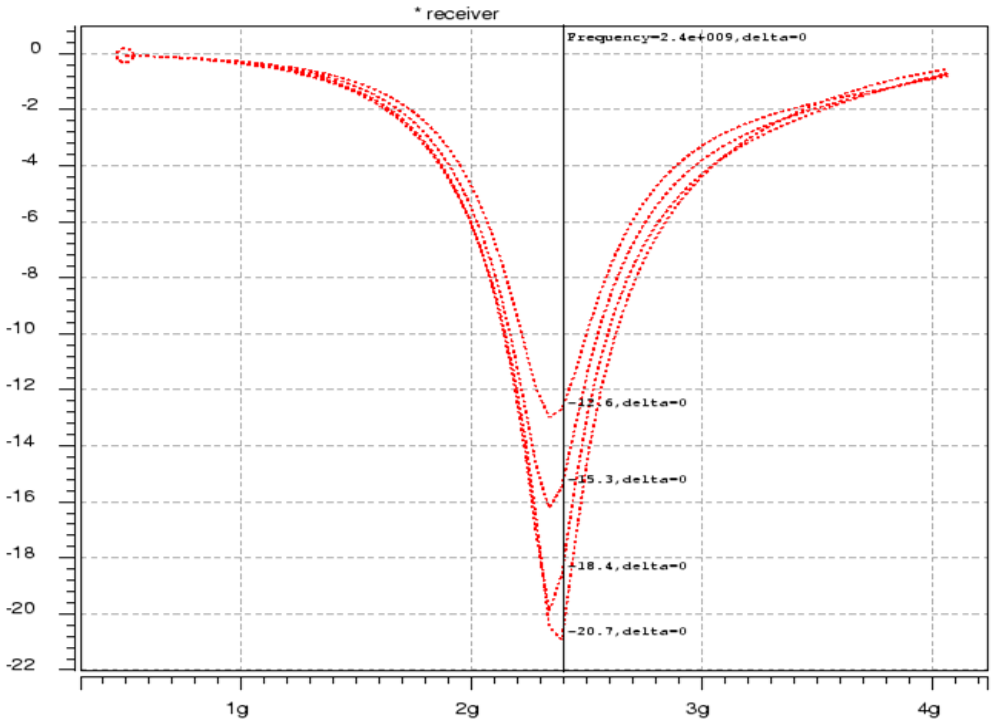
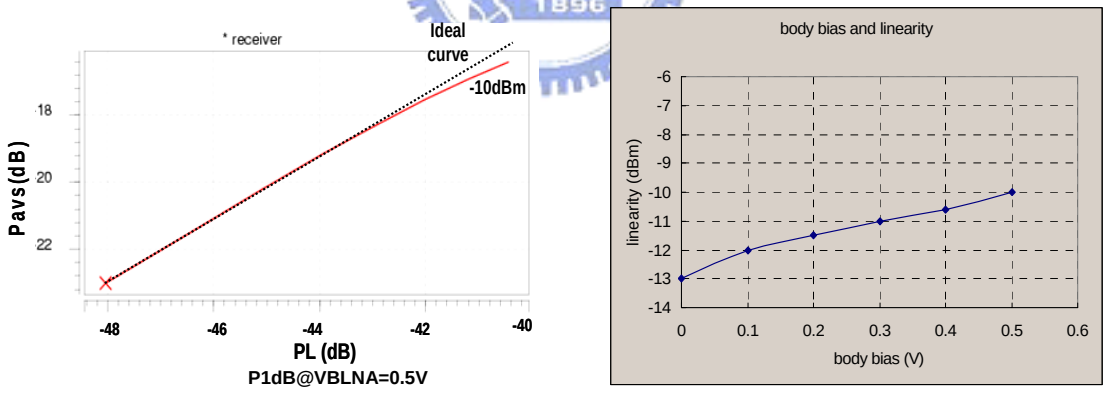
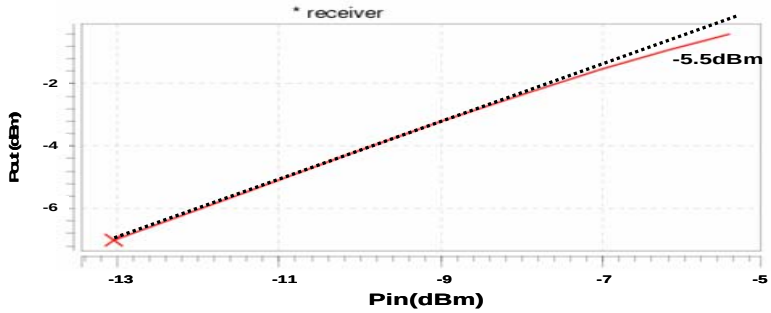



Fig. 2.36 The simulated input matching (S11) of the receiver

The Fig.2.36 shows the body bias sweep from 0.3V to 0.6V, the input matching (S11) of LNA can guarantee smaller than -12-dB.




(a)




(b)

Fig. 2.37 (a) LNA P-1dB HSPICE simulation result.
(b) redesign the LNA gain to 6dB, P-1dB can be improved to -5.5dBm

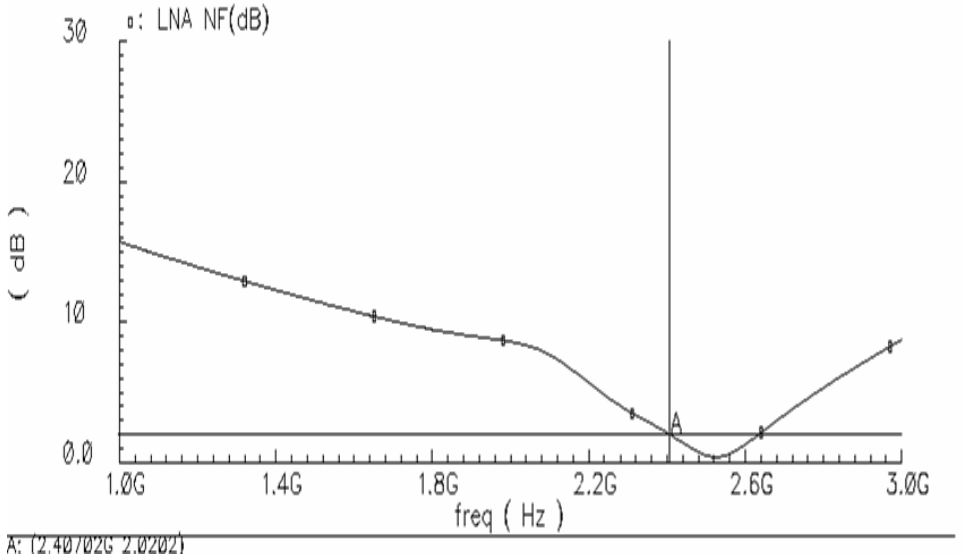



Fig. 2.38 LNA noise figure SpectreRF simulation
NF=2.02dB@2.4GHz

| | This work Simulation results | | Reference paper Experimental results | |
|---|---|---|---|---|
| | with body bias | w/o bulk bias (same device size*) | Active body type LNA[11] | Body effect feedback[14] |
| Technology | 0.25um bulk | 0.25um bulk | 0.35um SOI | 0.18 bulk |
| Frequency | 2.4GHz | 2.4GHz | 1.9GHz | 1.65~2.5GHz |
| Bulk voltage | 0.5V | VBS=0V | 0.5V | 0.6V |
| Supply Voltage | 1V | 1V | 1V | 0.9V |
| Power Consumption | 3.17mA | 3.5mA | 5mA | 2.5mA |
| S11 | -20dB | -20dB | - | - |
| Gain | 20.2dB | 16dB | 7dB | 10dB |
| NF | 2.02dB | 3dB | 5.6dB | 1.34dB |
| P-1dB | -10dBm | -13dBm | -4.5dBm | -16dBm |

Table 2.5 The comparison between w/o body bias, w/i body bias.and reference paper

The comparison between w/o body bias, w/i body bias.and reference paper is listed in table 2.5. The main advantages of body biased LNA are gain and linearity for low power supply design [11].

1. Gain improvement
2. 1-dB compression point improvement

The body of the transistor is connected to its gate. The threshold voltage of the transistor becomes smaller due to body effect so that a large drain current is obtained which keeps the gain high even at a low supply voltage. An added feature of connection between the body and the gate is the high 1-dB compression point. This is because the transistor can drive large load capacitance with a larger RFsignal input due to the active threshold voltage of the body control.

**B. Quadrature Voltage control oscillator**

The tuning range of VCO is shown in Fig. 2.33. The quadrature VCO oscillates 2376MHz~2639MHz by control voltage (VCOBIAS) from 0V to 1V

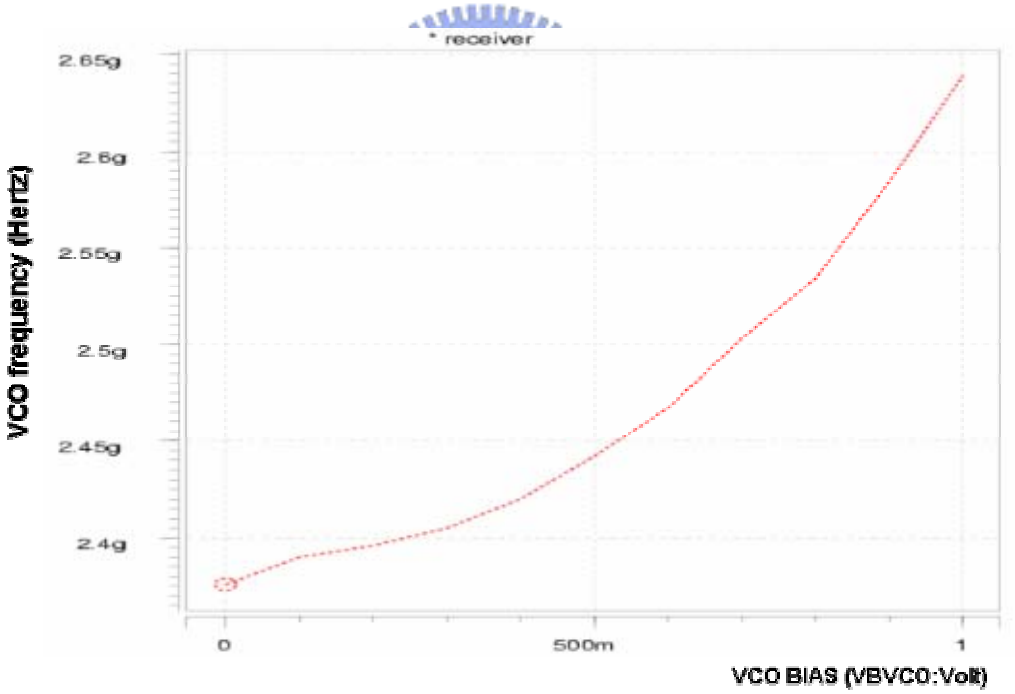



Fig. 2.39 The simulated tuning range of VCO

**B. Quadrature downconverter mixer**

The RF input, LNA output, quadrature VCO output , mixer I/Q IF output waveform are shown in Fig. 2.34. Low noise amplifier amplifies the input signal to the receiver. The voltage gain of LNA is about 20-dB. The simulated waveform is shown in Fig. 2.34(a). The quadrature voltage-controlled oscillator provides I/Q signal and mixes with LNA output. The quadrature VCO I/Q signal is shown in Fig. 2.34(b). The quadrature downconverter mixer down converts the RF signal to I/Q IF signal. The terminal of mixer output is IP, IN, QP, QN, separately.

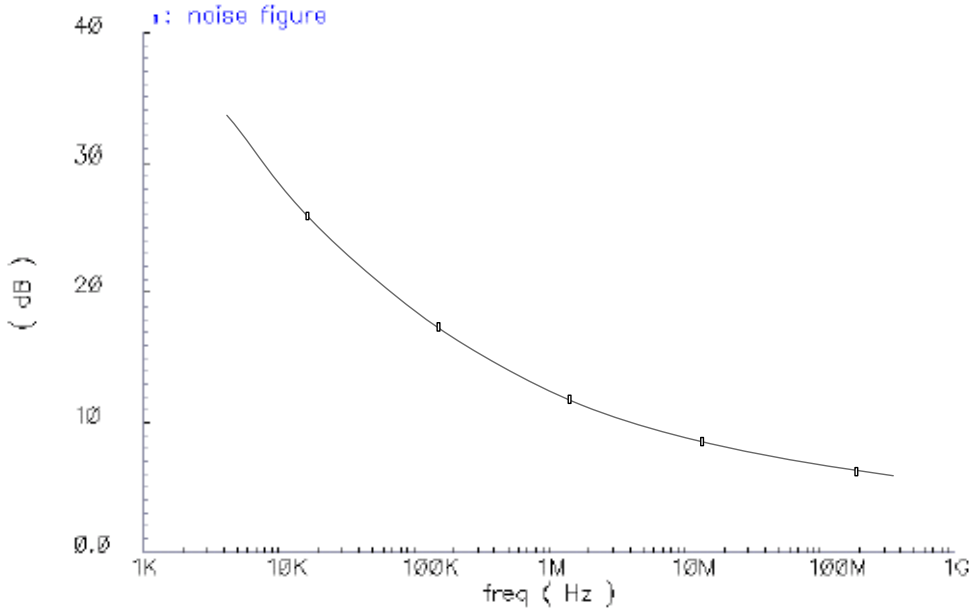



Fig. 2.40 Mixer noise figure SpectreRF simulation
NF=8dB@10MHz

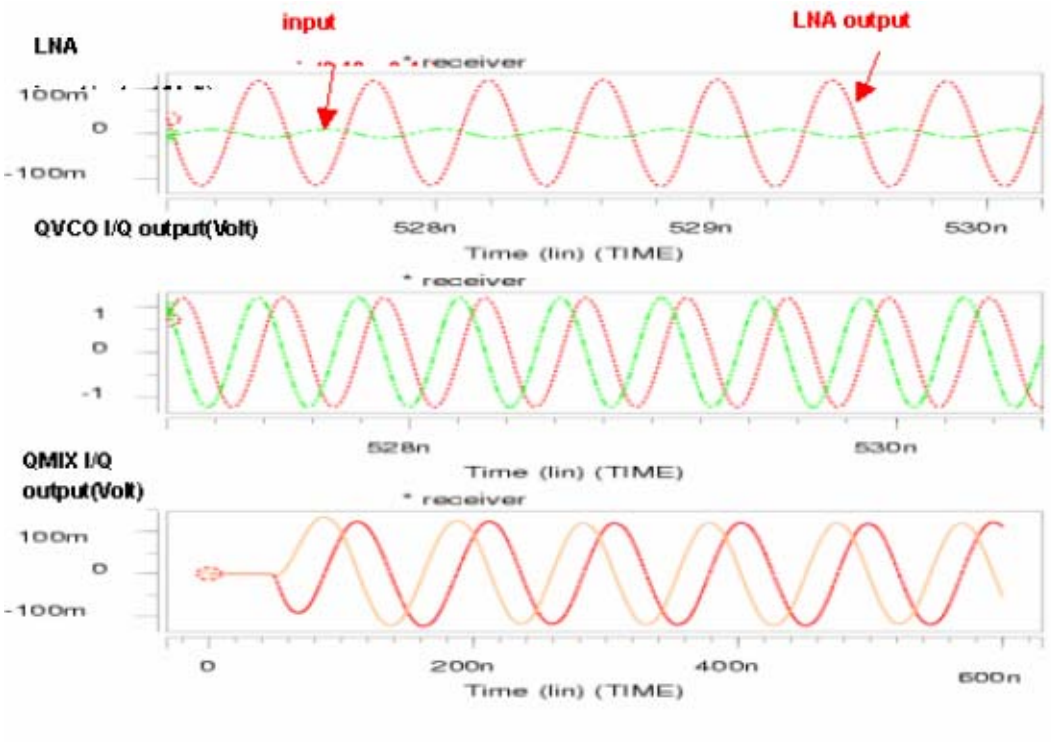



Fig. 2.41 The transient analysis of downconverter (a) input and output of LNA (b) I/Q signal of quadrature VCO (c) output waveform of downconverter

### C. Active polyphase filter

The polyphase filter is used to buffer the desired signal and reject the image signal. The simulated frequency response of polyphase filter is shown in Fig. 2.35. The image rejection ratio is greater than 60-dB. In order to expand the frequency band, the four-stage polyphase filter is used. The required band is about 5MHz~10MHz. For 1-stage polyphase filter, the ideal equation are

$$IOP = IP\frac{1}{s+\omega_o} + QN\frac{s}{s+\omega_o}$$

$$QOP = QP\frac{1}{s+\omega_o} + IP\frac{s}{s+\omega_o}$$

$$ION = IN\frac{1}{s+\omega_o} + QP\frac{s}{s+\omega_o}$$

$$QON = QN\frac{1}{s+\omega_o} + IN\frac{s}{s+\omega_o}$$

Four poles is located at 13.26MHz, 10.62MHz, 8.85MHz, 7.07MHz. To map the ideal transfer curve and simulation results.

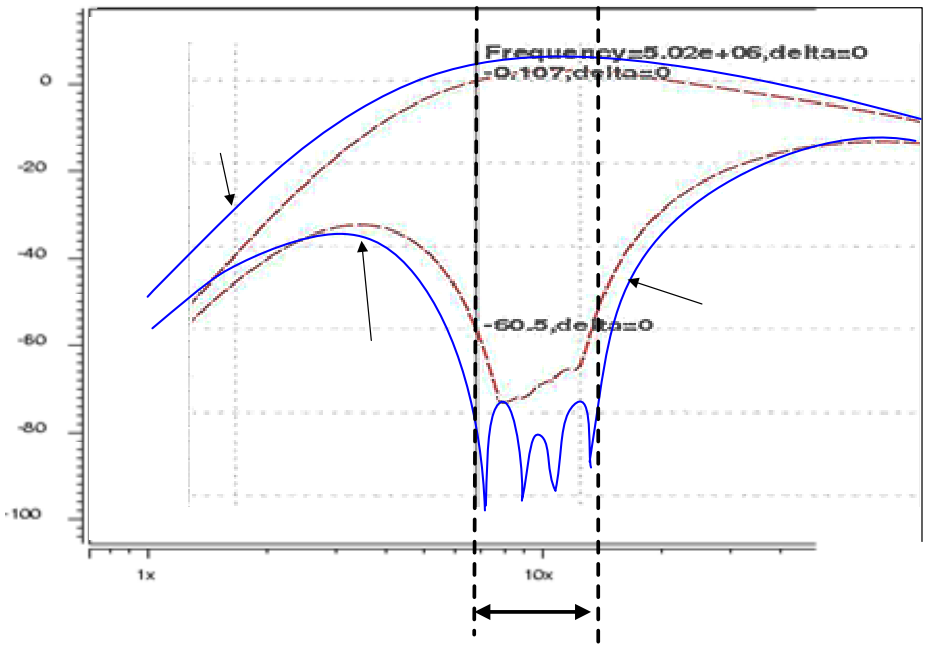



Fig. 2.42 The frequency response of polyphase filter

The frequency response of polyphase filter can be shown in Fig. 2.42.

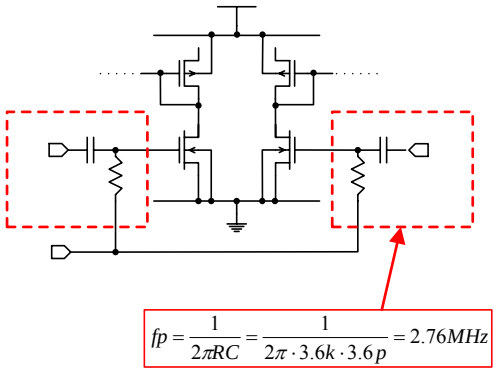



Fig. 2.43 The input stage HP filter

| | |
|---|---|
| Technology | 0.25um |
| Power supply | 1V |
| Gain in Bandwidth | 6dB (5MHz~13MHz) |
| THD | -40dB |
| IRR | >60dB |
| Power consumption | 1.6344mW |

Table 2.6 The performance summary of polyphse filter

Fig. 2.42 illustrates the input bias stage. It becomes a HP filter in each stage input. The gain degrade can be observed in Fig.2.42 at low frequency.

Table 2.6 summarizes the results of the simulation results of the polyphase filter. The image rejection exceeds 60dB over the range 5MHz to 13MHz. The THD (Total harmonic distortion) is -40dB when 10MHz, 100mV signal is applied. The power consumption of polyphase filter is 1.6344mW.

**C. The receiver analysis**

The bluetooth required the gain greater than 10-dB in this receiver front-end. The design of receiver must assigned to get enough noise figure and gain. Table 2.7 listed the gain and noise figure assignments in this receiver front-end system.

The spectrum of receiver is shown in Fig. 2.36. The following example is a 2.4-GHz input and 10-MHz output frequency spectrum. The output is split to two signals I/Q with 90-degree difference phase.

| Stage | LNA | Mixer | Polyphase filter | Output buffer | all |
|---|---|---|---|---|---|
| Gain | 18dB | -4dB | 6dB | -6dB | 12dB |
| NF | 2.03dB | 8dB | 8dB | 6dB | 8.2dB |

Table 2.7 The gain and noise figure assignment

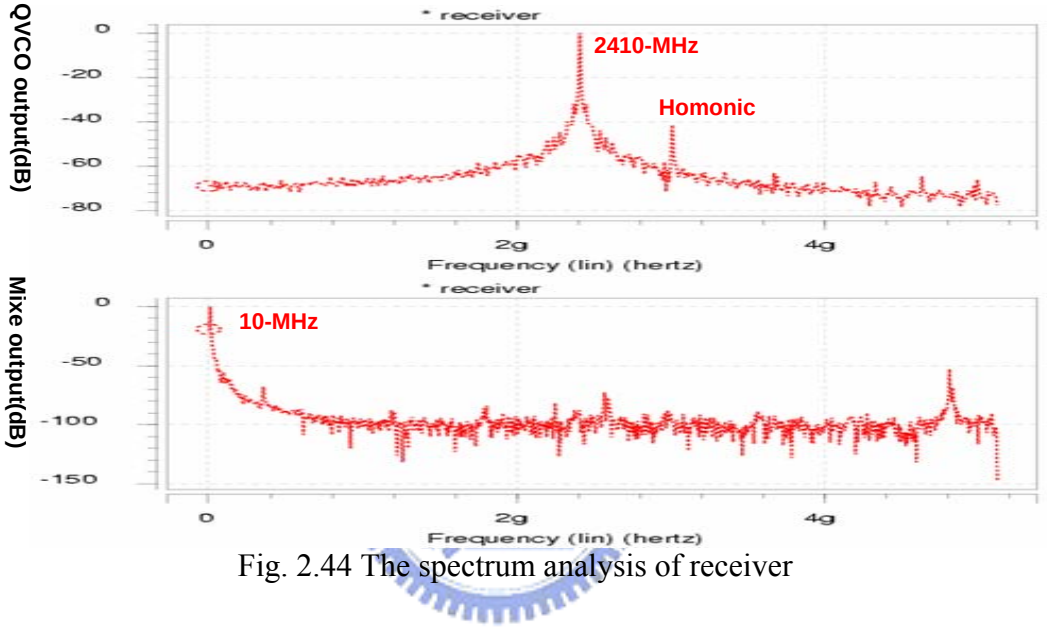



Fig. 2.44 The spectrum analysis of receiver

The noise figure of receiver is simulated by SpectreRF and shown in Fig. 2.45. The NF is equal to 8.8dB at 10MHz IF freqneycy.

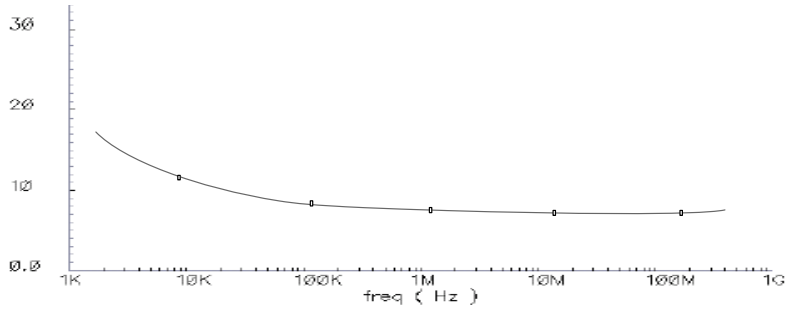



Fig. 2.45 Output noise spectral density for receiver NF=8.2dB@10MHz

# CHAPTER 3

# EXPERIMENT RESULTS

This chapter presents the chip layout, testing environment setting and experimental results. It also discussed and compared with post-simulation results regarding the measurement results

## 3.1 Layout Description

This receiver testchip can be divided in four parts. They are a Low-Noise amplifier, a quadrature VCO, a quadrature mixer, a polyphase filter with output buffer. The receiver layout and chip floorplan is shown in Fig. 3.1. The die photograph is shown in Fig. 3.2.

All the NMOS devices are placed on deep N-WELL (DNW), which is called R-WELL (RW) supported by TSMC 0.25-um technology. The external DNW drawing layer and mask must be used in this layout to define the RW region. The deep N-WELL isolates the NMOS to other device within the R-WELL. It can reduce the NMOS body-effect. For body-bias LNA, the NMOS bulk terminal can be biased to an independent power.

The guard ring surrounds each MOS device to avoid the substrate noise and signal couple. It also used to prevent the latch-up issue caused by parasitic SCR circuit for large MOS devices. The dummy POLY and dummy OD is usually inserted to reduce the side effect of process etching. The dummy metal is added in the top of layout, the dummy metal occupies large area. It is used to improve the metal density and to overcome the DRC density violation. To improve the metal

CMP process window, it must fill the dummy metal uniformly even if the originally drawn has already met the density rule. The dummy metal can be also worked as power line simultaneously.

The widely used on-chip inductor is spiral inductor. All spiral inductor must keep proper distance with the others and core circuit to prevent mutual inductance and disturbance on circuit. The source of spiral inductor layout cell is from TSMC's RF design library. The cell library is silicon proven and the measurement data is collected in SPICE model document for our reference.

The input resistance is an important key to contribute for noise figure. In order to reduce the input resistance, the LNA block is close to RF input to minimize input resistance. The LNA circuit is fully differential configuration, four-inductor belong to LNA are located surround with the NMOS devices and made them symmetrically as far as possible. Dummy gate and dummy resistors are equipped with every MOS device and resistor respectively to cope with process variation. The body of LNA NMOS input stage is connected to a bias voltage used to control its body bias voltage.

The chip floorplan must consider the optimum signal flow path. It should be as short as possible in metal routing and alleviate transmission line effect especially for high frequency. The mixer places on the middle of the receiver chip. It accepts LO signal from left side and LNA amplified RF signal from the bottom side of the chip. The mixer output transfer to right side and input into polyphase filter then to the output buffer. It can be observed that MIM capacitances occupy large area in polyphase region.

The fully receiver chip layout is shown in Fig 3.1 in the next page.

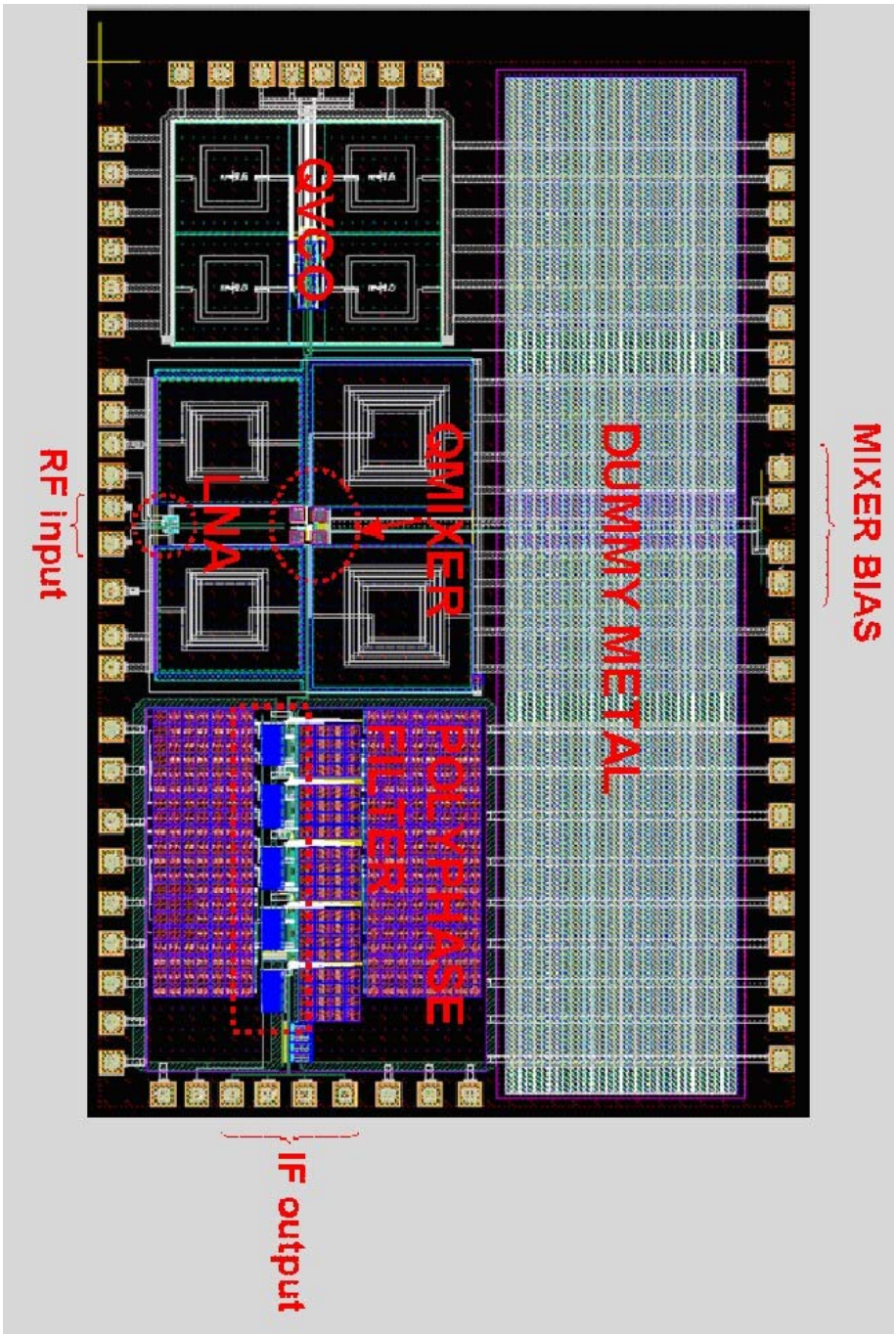



Fig. 3.1 The receiver chip layout

## 3.2 Testing Description

The receiver chip is a bare dies and needs to bond on a bonding board because it is more complicated for parasitic RC and inductance to place the chip on package. The purpose of testing board is to route the die pad to the testing equipments. The routing must be as short as possible to eliminate the parasitic RLC effect. The photograph of receiver chip and the bonding boards are shown in Fig. 3.2 and Fig. 3.3.

The input and output terminal are differential so that it needs external components like as balun and transformers for RF input and IF output in the measurement. The RF input signal flows into a balun and split the single-end RF signal to differential RF signal into receiver testchip. The receiver IF outputs are IP, IN, QP, QN, separately. Their DC signal is blocked by a 3uf block capacitance and drive to output by transformer.

The baluns with part number BL2012-10B2450 are made by Advanced Ceramic X Corporation. The transformers with module number ADT2-1T are made by Minicircuits. Signal attenuation caused by the baluns and transformers are measured for compensating back to relative apparent performance.The signal attenuation caused by transmission line should be considered and need to compensate back according to the measurement results.

The inductance variation of bond-wire and parasitic capacitance may affect the performance of input matching (S11). It is compensated by an off-chip parallel capacitance and fine-tunes the transmission line inductance. The bias voltage is fed by an external pin and can be flexible adjustment.

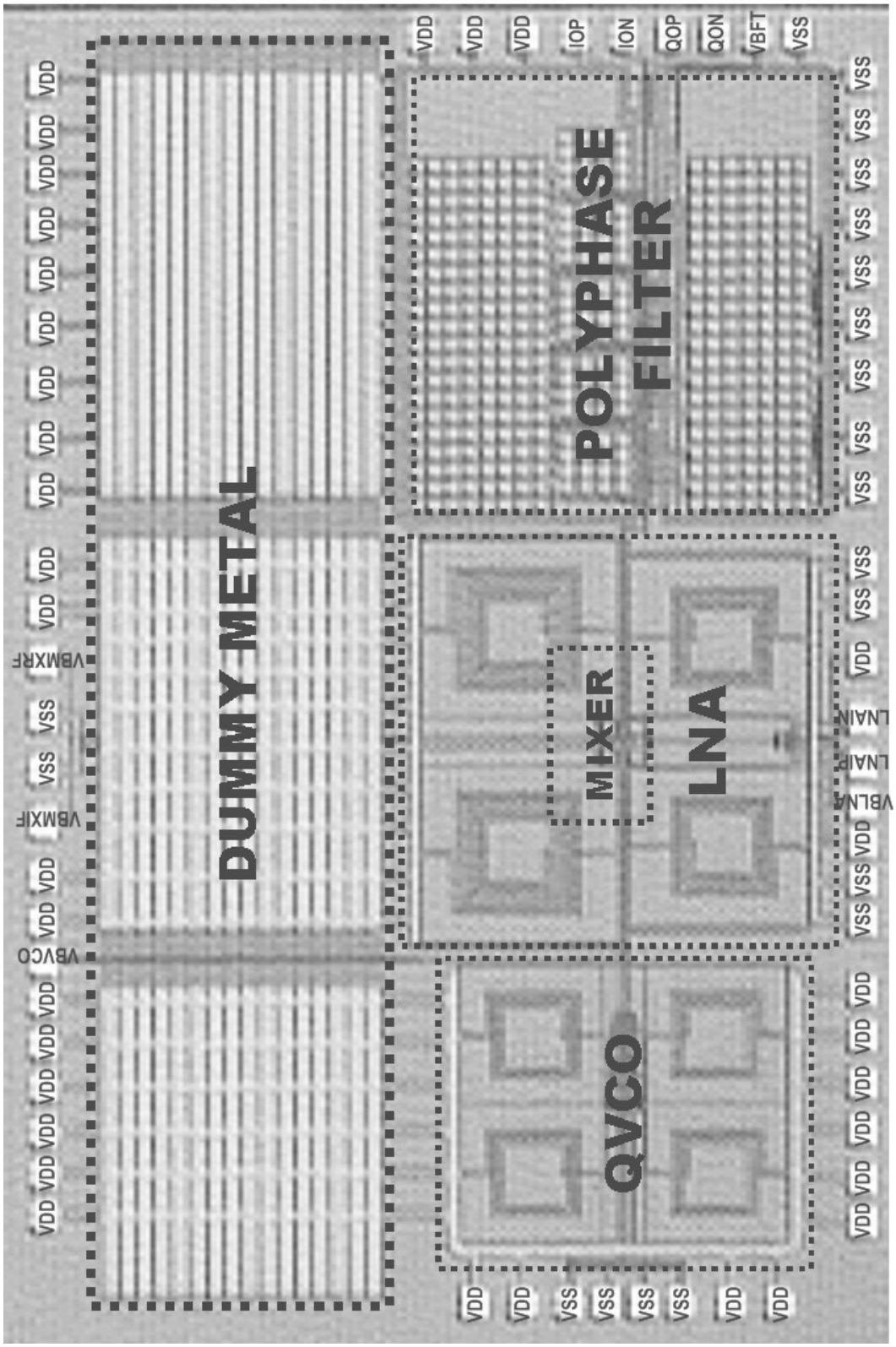



Fig. 3.2. Die photograph and receiver chip floorplan

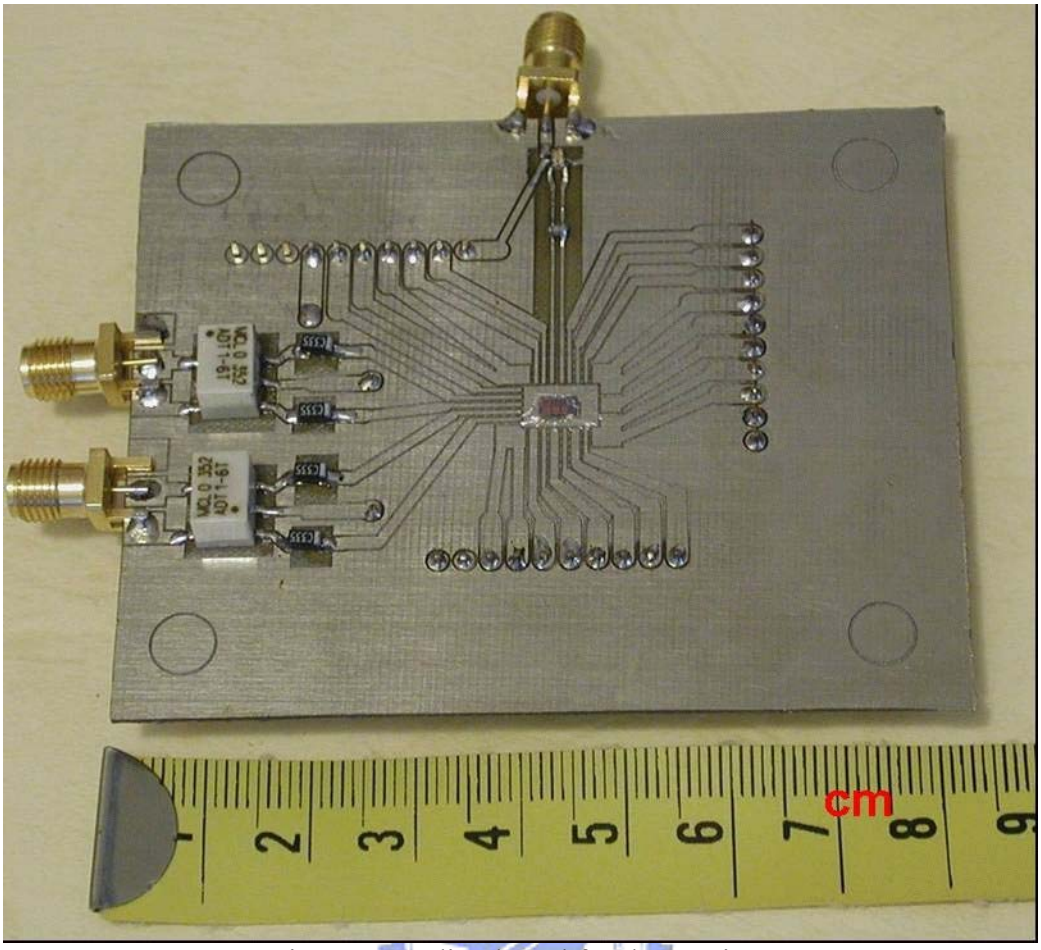



Fig. 3.3 Bonding board for the receiver

## 3.3 Measurement Setup

As shown in Fig. 3.4, the testing board is integrated in an individual DC boards for the testchip measurement. All the supply and bias voltage should parallel a large capacitor to provide a stable power voltage.

The test platform for receiver is shown in Fig. 3.4. The bonding board plugs in the DC board for testing. The DC board drag out pin of bonding board and it connect to power supply and bias voltage.

The standard measurement setup of receiver chip is shown in Fig. 3.5. A signal generator generates RF input to the balun, which split the RF single-end input to differential input to receiver chip of LNA. There are many power bias can be applied to the receiver chip. The power bias fed to the receiver chip and can be adjusted according to circuit's operating point. The input bias of balun can set the input DC bias to bias the LNA input stage. The terminal of LNA input parallels a 1pf capacitance to fine-tune the performance of input matching.

The testing items need various instruments for measurement, for example, S-parameter analysis requires a network analyzer, spectrum analysis requires a signal generator and spectrum analyzer; noise analysis requires a noise source and a noise analyzer; linearity analysis (two-tone test) require two signal generator, a power splitter, a spectrum analyzer, and a waveform analysis, etc. This section introduces the measurement setup and the methodology.

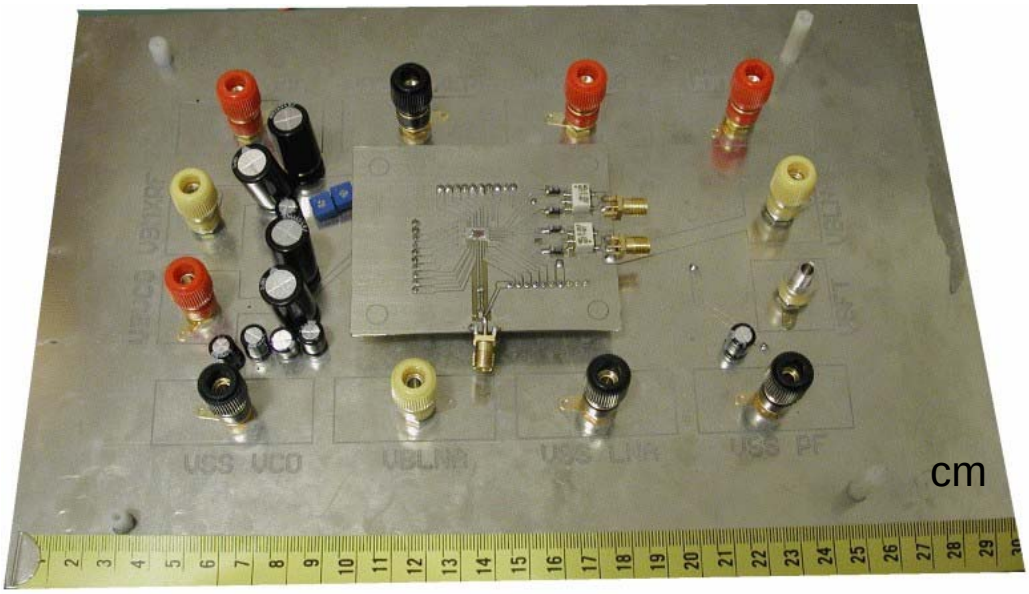



Fig. 3.4 test platform for receiver

A measurement environments setup of receiver chip is shown in Fig. 3.5. The signal generator provides the desired signal input to the receiver. The spectrum analyzer used to measure down converted IF spectrum to analyze the performance of conversion gains and the potential regarding the internal leakage.

The linearity of a receiver system is a important parameter. The linearity analysis (two tone test) measurement setup is shown in Fig. 3.6. Two signal generators applied to generate two signals with different frequency to input into power splitter. The power splitter combines two tones and transfers into the receiver chip. The receiver down converts and generate first and third order output spectrum to be measured.

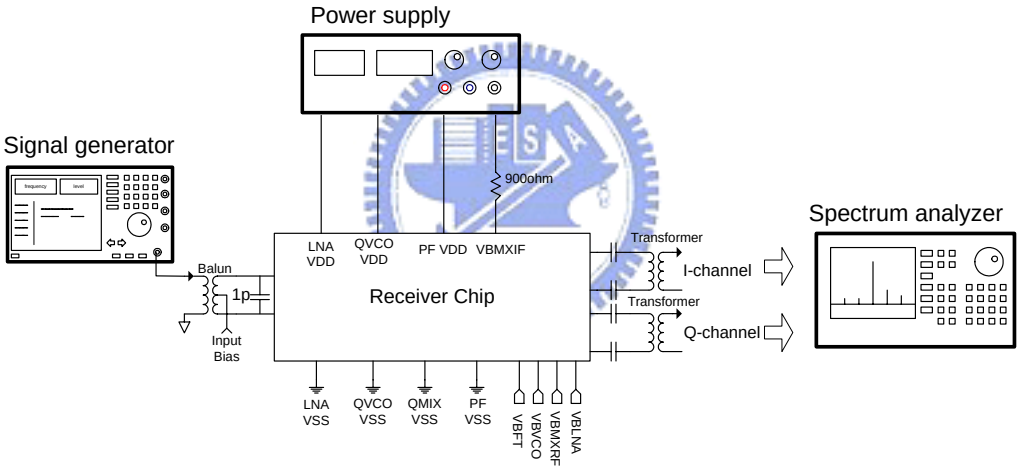



Fig. 3.5 The measurement setup of receiver chip

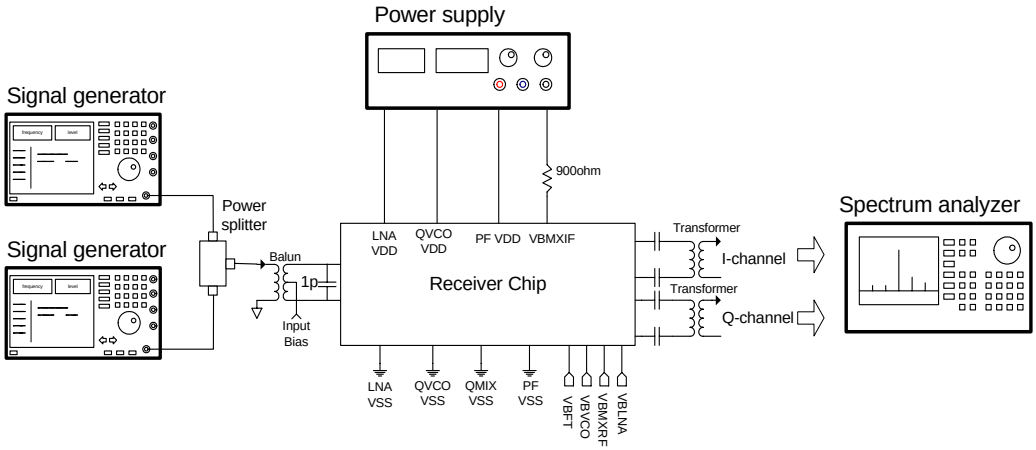



Fig. 3.6 IIP3 and conversion gain measurement setup

## 3.4 Experimental results

The receiver testchip has several components totally consumes about 18.575-mW DC power. The measurement data is slightly greater than the post-simulation results. The root cause is inferred that process corner variation. The supply voltage is 1-V to affect an inaccurate power consumption simulation results. The device current and power consumption can be evaluated by corner simulation.

The measurement DC bias condition is adjusted and it does the effort to get the best performance for the receiver testchip. After adjusts the bias DC operation point, the performance of receiver can be further close to the target of specification. The DC bias conditions are listed in table 3.1.

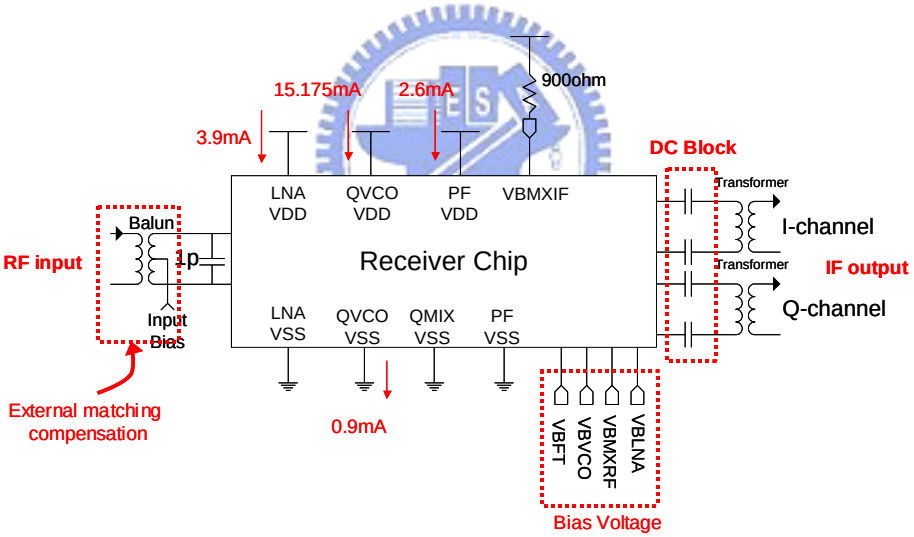



Fig. 3.7 bias conditions

| BIAS CONDITION | DESCRIPTION | Volt |
|---|---|---|
| RFBIAS | RF input bias | 0.6 |
| VBLNA | LNA body-bias | 0.4 |
| VBMXRF | MIXER input bias | 0.6 |
| VBVCO | VCO frequency control bias | 0~1 |
| VBFT | Polyphase filter input bias | 0.6 |

Table 3.1 DC bias tables

The input terminal parallels 1pF capacitance and adjusted the transmission line to compensate the performance of input matching (S11). The bond-wire inductance is estimated to have approximately maximum 3.2-nH variation. The input matching is compensated with 2.7-GHz, because the VCO frequency is shift up to 2.7-GHz. The input measurement of receiver input matching results is shown in Fig. 3.8. The receiver performs S11 better than –20-dB in band.

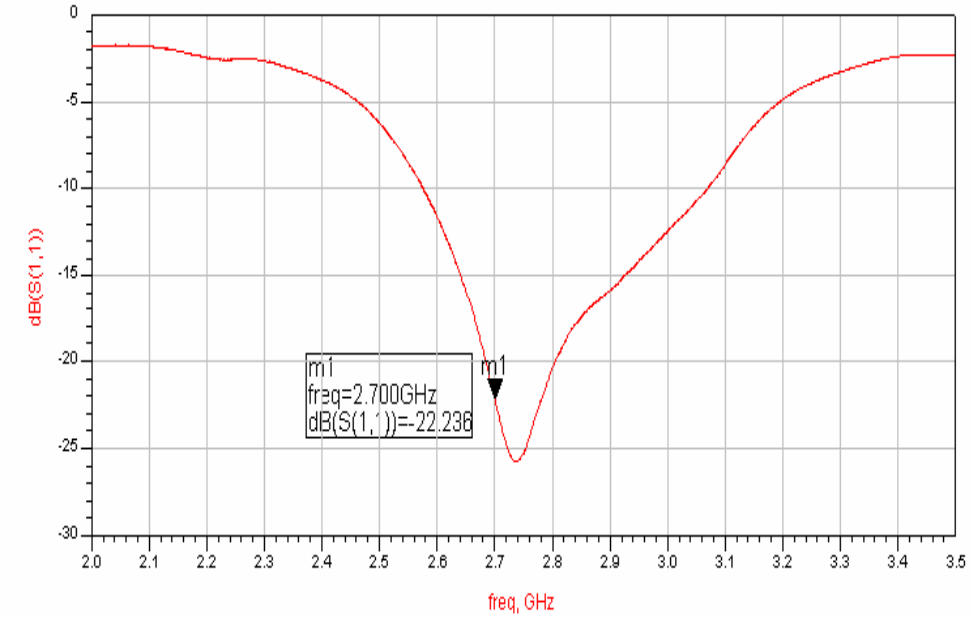



Fig. 3.8 The input matching (S11) of receiver

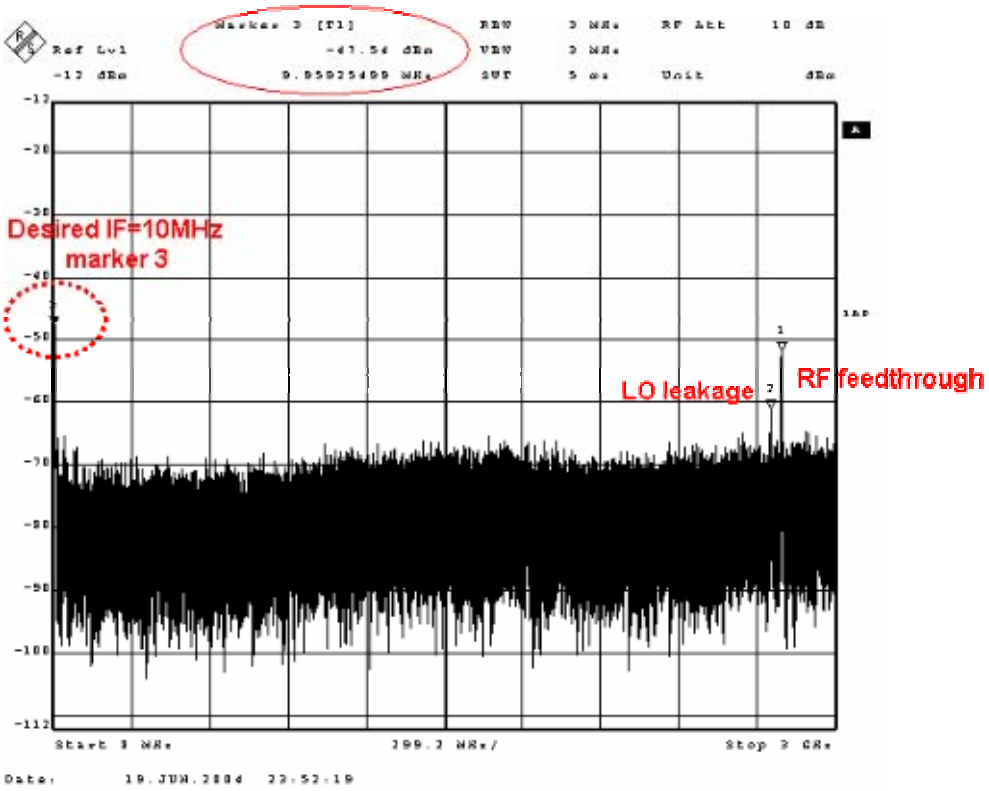



Fig. 3.9 The receiver output spectrum

The measurement of output spectrum is shown in Fig. 3.9, Markers 1~3 denote RF feedthrough, LO leakage and desired IF signal. The frequency of desired signal is 9.93-MHz. It is downconverted by mixing RF input and LO I/Q signal. RF feedthrough is about –55-dBm appears due to mixer mismatch and substrate couple. It cannot be simulated and is not predictable from an exact consideration by HSPICE simulation. LO leakage appears causes from similarly with RF feedthrough. The measured quantity of spurious emission such as RF feedthrough and LO leakage must satisfy the bluetooth specification.

To consider the loss of the external components and buffer loss, the gain of receiver must be compensated back and it performs over 7-dB gain in band.

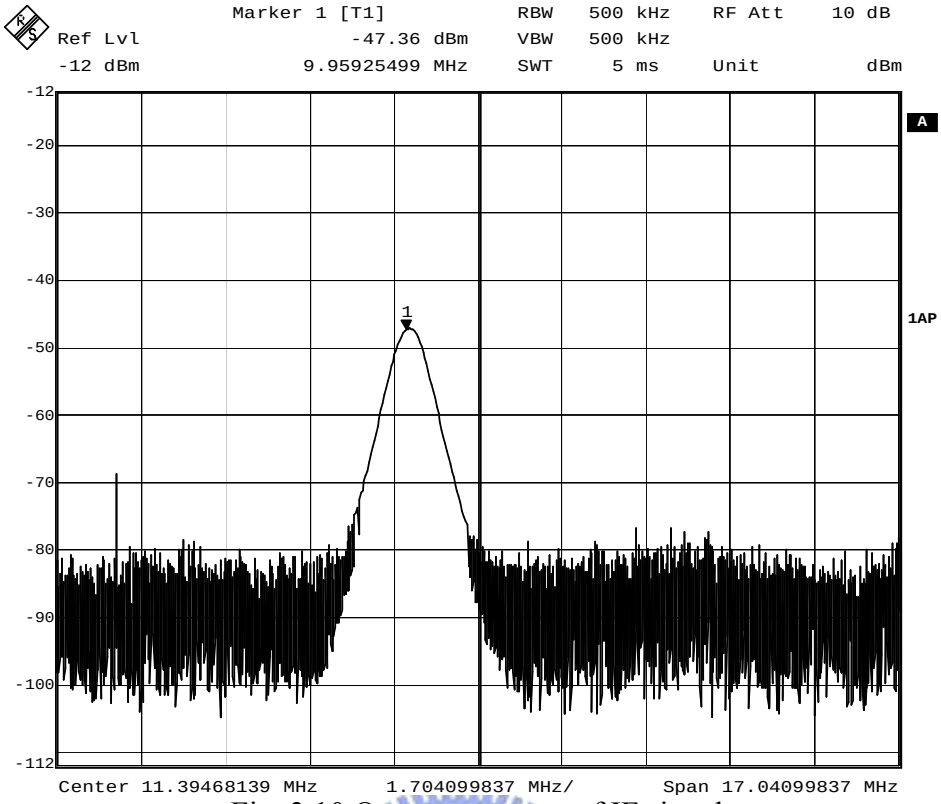



Fig. 3.10 Output spectrum of IF signal

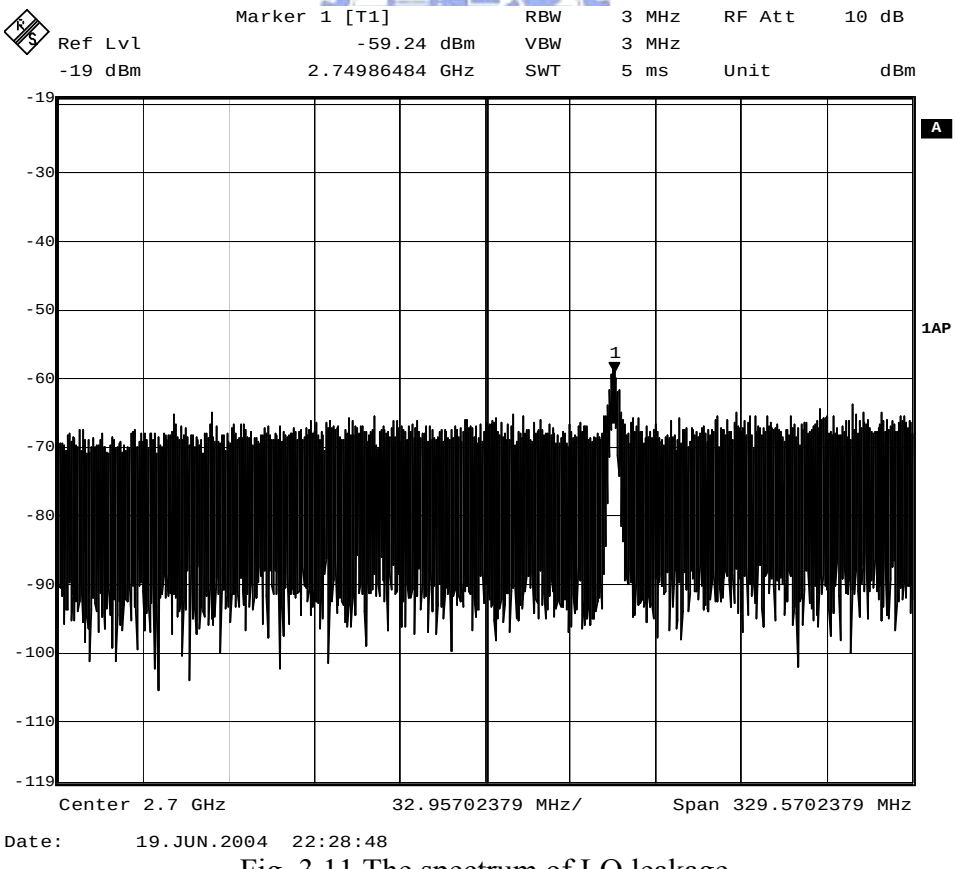



Fig. 3.11 The spectrum of LO leakage

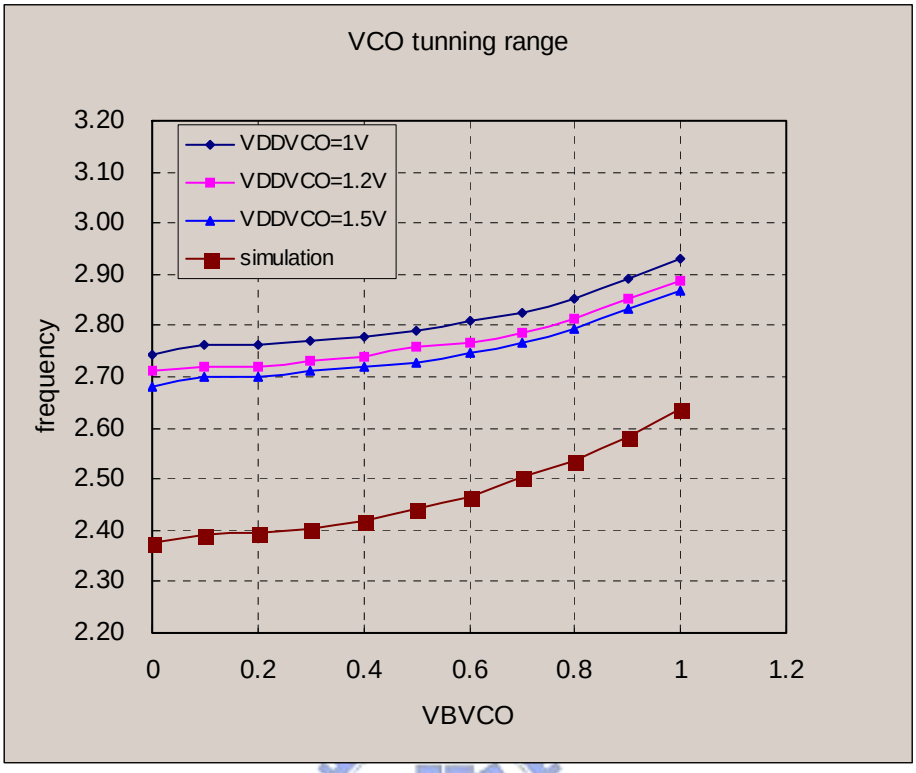



Fig. 3.12 The tuning range of VCO

Fig.3.10 shows the output spectrums of IF signal. The signal is in 10MHz IF band. The input power is -45-dBm. We can get the output power is -47.36dBm and IF frequency is 9.96-MHz. To compensate with 1.5-dB balun loss, 0.5-dB transformer loss and 8-dB PC board loss, and 6-dB output buffer loss. The receiver performs over 15-dB gain in band.

VCO tuning range can be analyzed by LO leakage observed on spectrum. Fig.3.11 shows the LO leakage spectrum in output terminal. The Fig.3.12 shows the plot of VCO tuning range. The oscillation frequency can be tuned from 2.74~2.93 GHz under tuning voltage 0V ~ 1V. The VCO gain is 190MHz/V. The Smaller capacitance of MOS varactor estimate in model causes the measured frequency shift up about 300MHz with the post-simulation result.

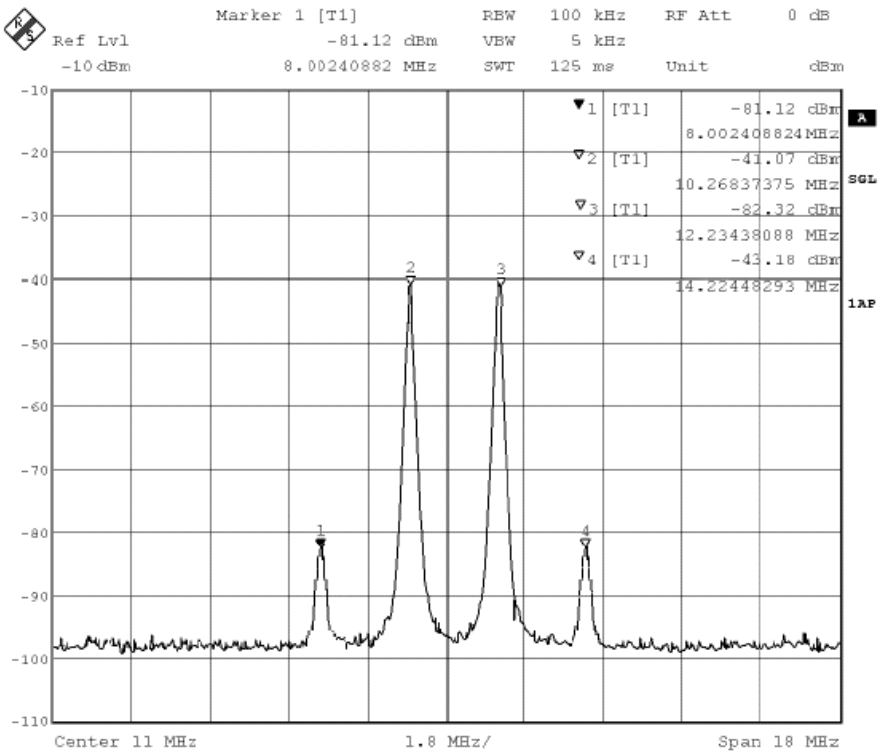



Fig. 3.13 Output spectrum of two-tone test.

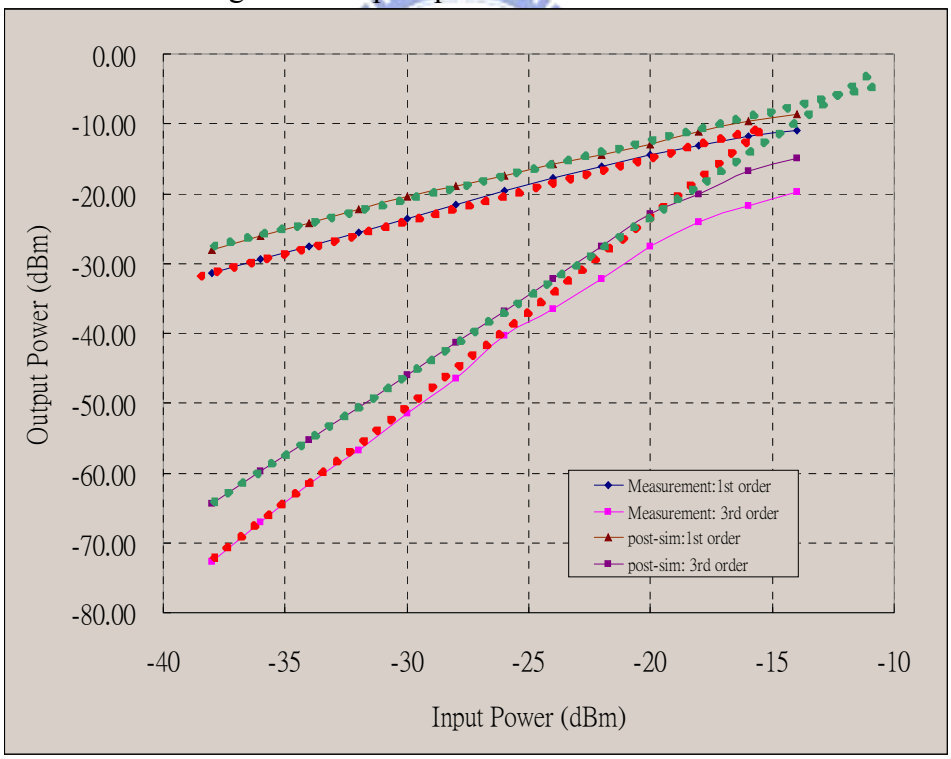



Fig. 3.14 Two-tone-test plot for IIP3

Fig 3.13 shows an output spectrum of two-tone test, where 1st-order and 3rd-order intermodulation signals are obvious. Fig 3.14 plots output-to-input power

relations. Compensate back with loss of external components. The measured receiver performs linearity of -15-dBm IIP3.

Noise figure is an indirect specification to adjust if a receiver contributes sufficiently low noise. Bluetooth requires SNR(signal to noise ration) higher than 12-dB to archive 0.1% BER(bit error rate). Noise figure is defined as ration of input SNR to output SNR. Minimum input SNR can be calculated as

Bluetooth requires SNR higher than 12-dB to achive 0.1% BER

SNRinput.miin(dB)=sensitivity - channel bandwidth - Noise Floor

=(-70) - 10log(10^6) - (-174) = 44dB

Nfmax(dB)=SNRinpu.min - SNRoutput.min = 44-12=32dB

Noise performance of the tested receiver is 15-dB. It is satisfies the bluetooth requirement. HSPICE cannot simulate noise figure if a circuit involves frequency conversion so simulated noise figure is absent in this paper. But the LNA dominates total noise performance. A receiver can perform satisfied noise figure with a well designed LNA.

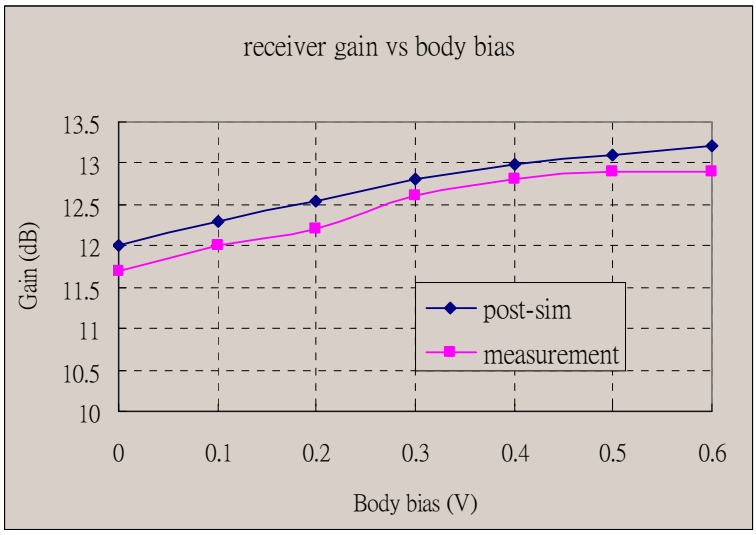



Fig. 3.15 The receiver gain with difference body-bias

To fine-tune the body-biased LNA can adjust the gain of receiver. Fig.3.15 shows the receiver gain with difference body-bias. The measurement result shows the body-bias method improved about 2-dB gain. If the body-bias voltage rises over 0.6V, the forward PN junction current is turned on and the bias supply current injection into the bulk. It is observed the gain of receiver is degraded.

Fig. 3.16 and Fig.3.17 shows the receiver gain and its image rejection capability. The IF frequency is about 10-MHz. the receiver has 15-dB conversion gain. It compensate with the balun, transformer and output buffer loss, similarly.

The operating band is 9-MHz~11-MHz. The can get 41-dB image rejection ratio at 10-MHz. The minimum IRR is 36.8-dB in IF band. It is also meet the bluetooth requirement.

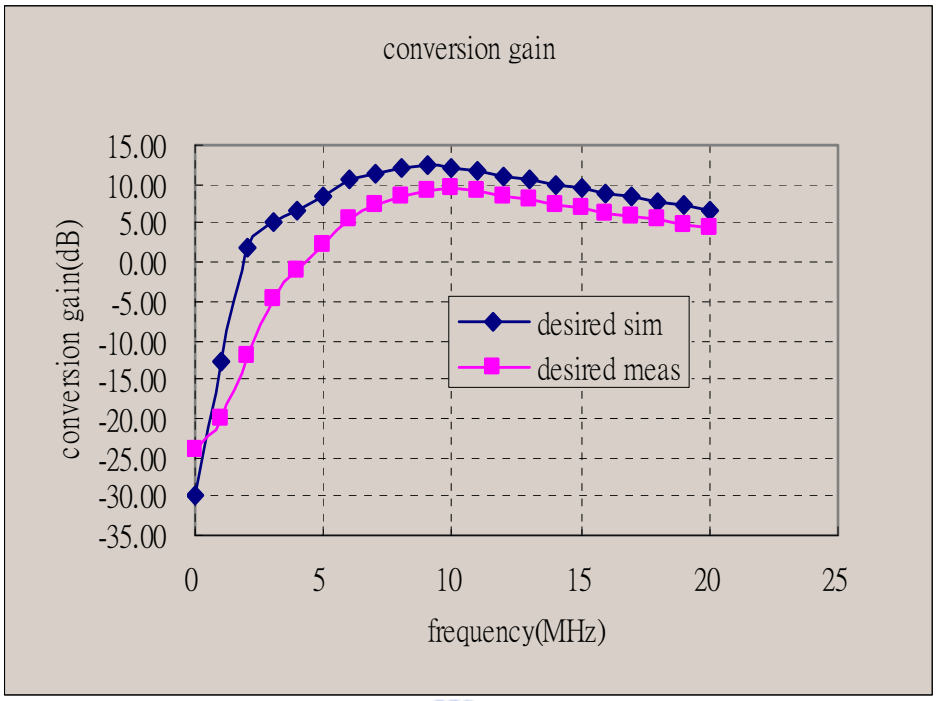



Fig. 3.16 The performance of receiver gain.

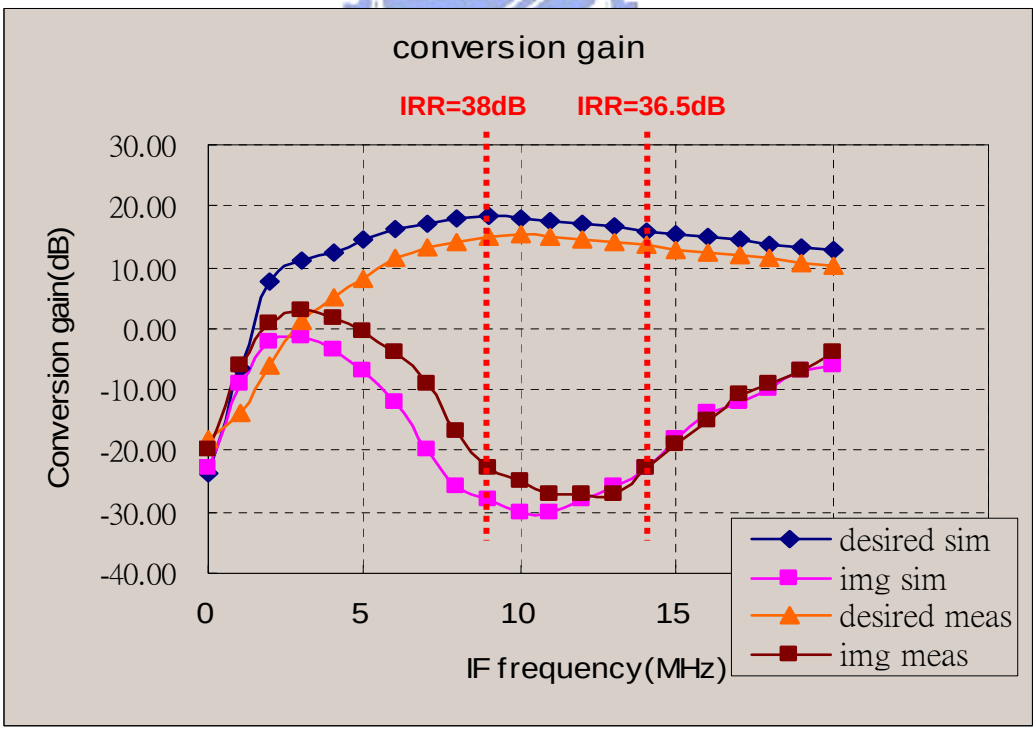



Fig. 3.17 The performance of image rejection

Table 3.2 lists the summary of the tested receiver, it comparison between post-simulation and measurement results. The gain in measurement is compensated with 1.5-dB balun loss, 0.5-dB transformer loss and 6-dB buffer loss. The measured gain and IIP3 after from the post-simulation due to the experimental biases and power consumption not identical with the post-simulation

| ITEM | Post-simulation | Measurement |
|---|---|---|
| Technology | TSMC 0.25-um 1P5M | |
| Chip area | 2452umx1112um | |
| Power Supply | 1V | |
| RF frequency | 2.4-GHz | |
| IF frequency | 10MHz | |
| S11 | -20dB | -19dB |
| Conversion gain | 18dB | 15dB |
| Noise Figure | 8.2dB | 17dB |
| VCO tuning range | 2.38~2.60 GHz | 2.74~2.93 GHz |
| VCO gain | 220MHz/V | 190MHz/V |
| Image rejection ratio | 47dB | 41dB |
| IIP3 | -13dBm | -15dBm |
| Power consumption | VDD@1V | |
| LNA | 3.17mW | 3.9mW |
| QVCO | 9.76mW | 11.175mW |
| QMIXER | 0.9mW | 0.9mW |
| PF & BUFFER | 1.6344mW | 2.6mW |
| OVERALL | 14.56mW | 18.575mW |

Table 3.2 Final summaries of measurement results

Table 3.3 lists a performance comparison between measured results and bluetooth specifications.

Table 3.4 compares the designed receiver with a similar art [12]. The paper consumed most of power due to its passive RC polyphase filter network.

| | Measurement | Requrement |
|---|---|---|
| Noise Figure | 17dB | <32dB |
| Image rejection ratio | 41dB | >20dB |
| IIP3 | -15dBm | >-16.5dBm |
| LO leakage | -60dBm | -47dBm |

Table 3.3 Measured performances compared with Bluetooth specifications

| | This receiver | Ref.[12] |
|---|---|---|
| Technology | 0.25um | 0.25um |
| Power supply | 1V | 1.5V |
| RF frequency | 2.4GHz | 1.8GHz |
| S11 | -19dB | -11.5dB |
| Noise Figure | 17dB | 8.2dB |
| Image rejection ratio | 41dB | 32.2dB |
| LO leakage | -60dBm | -83dBm |
| Power consumption | 18.575mW | 113mW |

Table 3.4 Receiver comparisons with another quadrature-designed receiver

# CHAPTER 4

# CONCLUSIONS AND FUTURE WORKS

## 4.1 CONCLUSIONS

The Low-IF receiver front-end with body-biased low-noise amplifier and integrated polyphase filter is designed, fabricated and measured. The receiver testchip comprises low-noise amplifier with body-bias, quadrature VCO, quadrature mixer, polyphase filter and an output buffer. The receiver testchip is fabricated by TSMC 0.25-um process and measurement results have been presented in this thesis. The receiver testchip occupy 2.7mm$^2$ area.

A new proposed LNA with body-bias voltage has been implemented in this design. The body-bias decreases the threshold voltage to improve the operating headroom. The body-bias applies to LNA input cascode stage and gains the best performance of gain and linearity.

The VCO's frequency is about higher than simulation results due to the parasitic capacitance not accurate to be modeled. The active polyphase filter has implemented in last stage. Its image rejection is perform to reject image about 30-dB. An active polyphase filter is also design in this testchip. To compare with RC network polyphase filter, the active polyphase filer transfer the desired signal without loss, occupy small area and lower power consumption.

The overall receiver chip with low-IF architecture is proven working well at 1-V supply, 27-dB noise figure, -27-dBm IIP3 ,lower than -55dBm LO leakage and 22mW power consumption.

## 4.2 FUTURE WORKS

A 1-V 2.4-GHz Low-IF receiver is successfully fabricated with several important key components. They are a LNA, a quadrature VCO and a quadrature mixer and a low-voltage active polyphase filter. A robust and compensation circuit should be used to reduce the affection by process and power and temperature variation.

A LNA circuit is implemented with body-bias scheme to improve its performance. It is silicon prove by this testchip. Besides, it can be researched that the other key components can also implement by body-bias to further improve the performance of low-voltage design.

A low-voltage active polyphase filter is implement in this receiver; The stable and accurate bias is needed. The designed polyphase filter is very sensitive to power supply, process and temperature variation so that the image rejection ratio may fall in a large range. The gm-bias can be considered to overcome process variation.

The LO frequency decide the frequency band of the receiver. As the measurement results, the measured quadrature VCO frequency is higher than simulation frequency. It can be fine tuned by flexible varactor switch or metal option. The parasitic resistance and capacitor should be further considered.

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