

## LIST OF FIGURES

- Fig. 1.1. A cross-sectional view of GGNMOS devices showing the gate shorted to the source, and its current dissipating path under ESD zapping.
- Fig. 1.2. The I-V curve of a gate-grounded NMOS.
- Fig. 1.3. A cross-sectional view of NMOS transistors with (a) fully-salicycided structure, and (b) salicide blocking structure.
- Fig. 1.4. Top view of NMOS transistor with salicide blocking.
- Fig. 1.5. A cross-sectional view of FOX structure GGNMOS transistor with external N-well resistors.
- Fig. 1.6. Current flow lines of (a) fully-salicycided structure NMOS transistor, and (b) dummy-gate structure NMOS transistors with N-well resistors.
- Fig. 1.7. I-V curve of gate-grounded NMOS transistor with external N-well resistors.
- Fig. 2.1. Cross-sectional view of fully-salicycided NMOS transistor.
- Fig. 2.2. Cross-sectional view of NMOS transistor with salicide blocking structure.
- Fig. 2.3. Cross-sectional view of NMOS transistor with FOX structure.
- Fig. 2.4. Cross-sectional view of NMOS transistor with dummy-gate structure.
- Fig. 2.5. Flow chart of transistor with salicide blocking and dummy-gate structure transistor with external N-well resistors.
- Fig. 2.6. Cross-sectional view of salicide blocking NMOS transistor with varied salicide blocking region to gate spacing.
- Fig. 2.7. Cross-sectional view of dummy-gate structure NMOS transistor with varied N-well to N-well spacing.
- Fig. 2.8. Cross-sectional view of FOX structure NMOS transistor with varied

N-well to gate spacing.

Fig. 2.9. Cross-sectional view of dummy-gate NMOS transistor with varied N-well to gate spacing.

Fig. 2.10. The layout pattern and corresponding devices structure of dummy-gate NMOS transistor with external N-well resistors in 0.25  $\mu\text{m}$  salicided CMOS process.

Fig. 2.11. Layout floor plane of test chips in 0.25  $\mu\text{m}$  salicided CMOS process.

Fig. 3.1. The TLP measured I-V curve of (a) fully-salicided GGNMOS, and (b) salicide blocking GGNMOS. NMOS = 240  $\mu\text{m}/0.25 \mu\text{m}$  in 0.25  $\mu\text{m}$  salicided CMOS process.

Fig. 3.2. The TLP measured I-V curve of (a) FOX structure GGNMOS with external N-well resistors, and (b) Dummy-gate structure GGNMOS with external N-well resistors. W/L = 240  $\mu\text{m}/0.25 \mu\text{m}$  in 0.25  $\mu\text{m}$  salicided CMOS process.

Fig. 3.3. The TLP measured I-V curve of fully-salicided GGNMOS, salicide blocking GGNMOS, FOX structure GGNMOS with external N-well resistors, dummy-gate structure GGNMOS with external N-well resistors, W/L = 240  $\mu\text{m}/0.25 \mu\text{m}$  in 0.25  $\mu\text{m}$  salicided CMOS process.

Fig. 3.4. Positive and negative ESD-stress on an input or output pin of an IC with respect to ground VDD or VSS.

Fig. 3.5. The TLP measured  $I_{t2}$  curve of GGNMOS with varied DCGS in 0.25  $\mu\text{m}$  salicided CMOS process.

Fig. 3.6. The measured HBM levels of GGNMOS with varied DCGS in 0.25  $\mu\text{m}$  salicided CMOS process.

Fig. 3.7. The measured MM levels of GGNMOS with varied DCGS in 0.25  $\mu\text{m}$  salicided CMOS process.

- Fig. 3.8. The TLP measured  $I_{t2}$  curve of GGNMOS with varied gate length in 0.25  $\mu\text{m}$  salicided CMOS process.
- Fig. 3.9. The measured HBM levels of GGNMOS with varied gate length in 0.25  $\mu\text{m}$  salicided CMOS process.
- Fig. 3.10. The measured MM levels of GGNMOS with varied gate length in 0.25  $\mu\text{m}$  salicided CMOS process.
- Fig. 3.11. The TLP measured  $I_{t2}$  of GGNMOS with varied fingers number in 0.25  $\mu\text{m}$  salicided CMOS process.
- Fig. 3.12. The measured HBM levels of GGNMOS with varied fingers number in 0.25  $\mu\text{m}$  salicided CMOS process.
- Fig. 3.13. The measured MM levels of GGNMOS with varied fingers number in 0.25  $\mu\text{m}$  salicided CMOS process.
- Fig. 3.14. The TLP measured  $I_{t2}$  of GGNMOS with varied channel width in 0.25  $\mu\text{m}$  salicided CMOS process.
- Fig. 3.15. The measured HBM levels of GGNMOS with varied channel width in 0.25  $\mu\text{m}$  salicide CMOS process.
- Fig. 3.16. The measured MM levels of GGNMOS with varied channel width in 0.25  $\mu\text{m}$  salicided CMOS process.
- Fig. 3.17. The TLP measured  $I_{t2}$  of GGNMOS with varied N-well to N-well spacing in 0.25  $\mu\text{m}$  salicided CMOS process.
- Fig. 3.18. The measured HBM levels of GGNMOS with varied N-well to N-well spacing in 0.25  $\mu\text{m}$  salicided CMOS process.
- Fig. 3.19. The measured MM levels of GGNMOS with varied N-well to N-well spacing in 0.25  $\mu\text{m}$  salicided CMOS process.
- Fig. 3.20. The TLP measured  $I_{t2}$  of GGNMOS with varied mask to gate spacing in 0.25  $\mu\text{m}$  salicided CMOS process.

Fig. 3.21. The measured HBM levels of GGNMOS with varied mask to gate spacing in 0.25  $\mu\text{m}$  salicided CMOS process.

Fig. 3.22. The measured MM levels of GGNMOS with varied mask to gate spacing in 0.25  $\mu\text{m}$  salicided CMOS process.

Fig. 3.23. The HP 4155C measured leakage current curves of FOX, dummy-gate structure GGNMOS with varied N-well to gate spacing.  $W/L = 240 \mu\text{m}/0.25 \mu\text{m}$  in 0.25  $\mu\text{m}$  salicided CMOS process.

Fig. 4.1. SEM failure picture of dummy-gate structure NMOS transistor with drain contact to dummy-gate spacing of  $S = 0.4 \mu\text{m}$  under HBM ESD zapping.

Fig. 4.2. SEM failure picture of dummy-gate structure NMOS transistor with drain contact to dummy spacing of  $S = 1 \mu\text{m}$  under HBM ESD zapping.

Fig. 4.3. SEM failure picture of dummy-gate structure NMOS transistor under HBM ESD zapping.

Fig. 4.4. SEM failure picture of FOX structure NMOS transistor under HBM ESD zapping.

Fig. 4.5. SEM failure picture of fully-salicided structure NMOS transistor under HBM ESD zapping.

Fig. 4.6. SEM failure picture of salicide blocking structure NMOS transistor under HBM ESD zapping.

Fig. 4.7. SEM failure picture of dummy-gate structure NMOS transistor with drain contact to dummy-gate spacing of  $S = 0.4 \mu\text{m}$  under MM ESD zapping.

Fig. 4.8. SEM failure picture of dummy-gate structure NMOS transistor with drain contact to dummy-gate spacing of  $S = 1 \mu\text{m}$  under MM ESD zapping.

Fig. 4.9. SEM failure picture of dummy-gate structure NMOS transistor under MM ESD zapping.

Fig. 4.10. SEM failure picture of FOX structure NMOS transistor under MM ESD zapping.

zapping.

Fig. 4.11. SEM failure picture of fully-salicided structure NMOS transistor under MM ESD zapping.

Fig. 4.12. SEM failure picture of salicide blocking structure NMOS transistor under HBM ESD zapping.

Fig. 4.13. The waveform of fully-salicided structure GGNMOS transistor under 1.1 kV HBM ESD zapping. (W/L = 240  $\mu\text{m}$ /0.4  $\mu\text{m}$ )

Fig. 4.14. The waveform of dummy-gate structure GGNMOS transistor with external N-well resistors under 1.1 kV HBM ESD zapping. (W/L = 240  $\mu\text{m}$ /0.4  $\mu\text{m}$ )

Fig. 4.15. The waveform of fully-salicided structure GGNMOS transistor under 130 V MM ESD zapping. (W/L = 240  $\mu\text{m}$ /0.4  $\mu\text{m}$ )

Fig. 4.16. The waveform of dummy-gate structure GGNMOS transistor with external N-well resistors under 130 V MM ESD zapping. (W/L = 240  $\mu\text{m}$ /0.4  $\mu\text{m}$ )