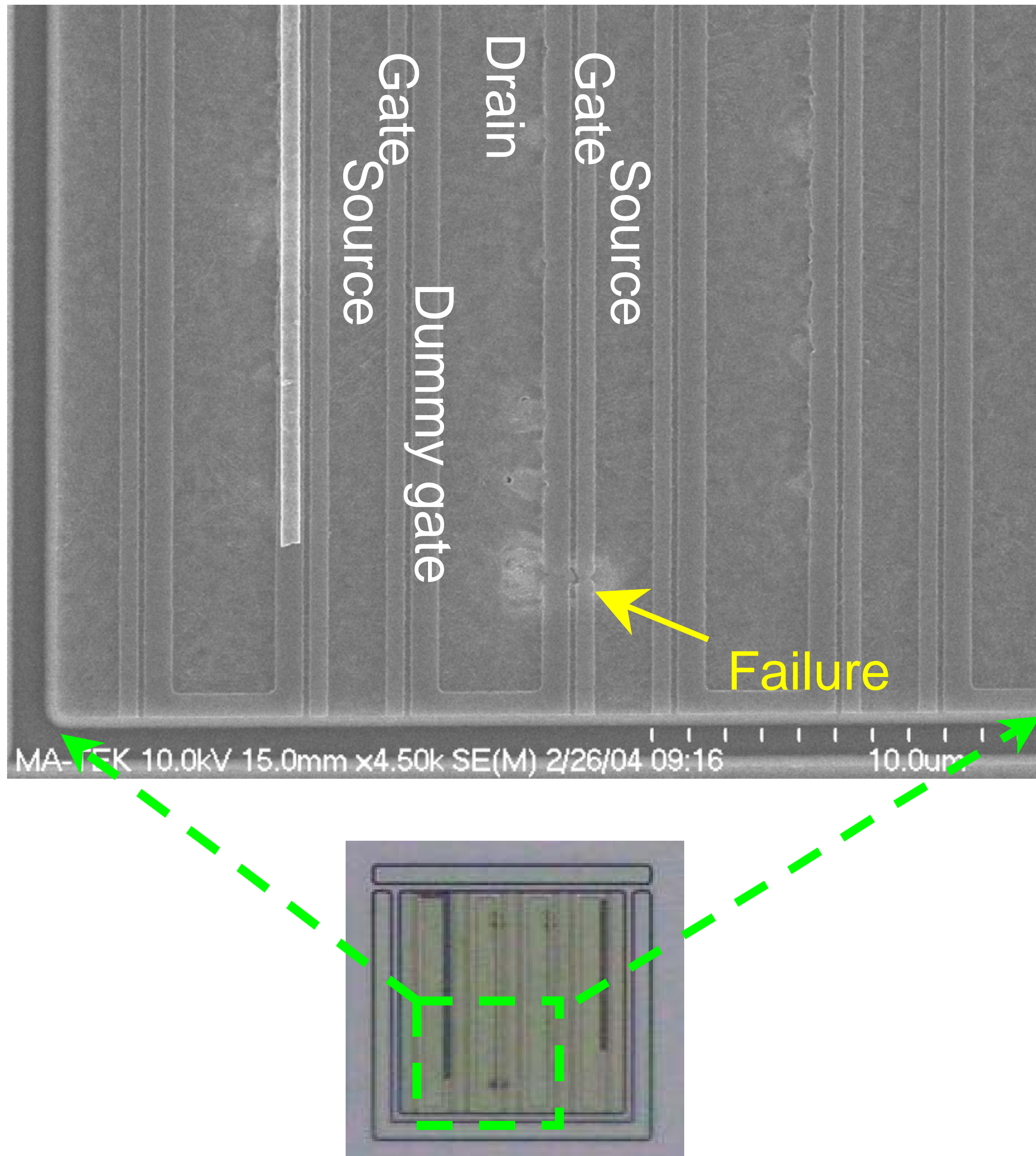

Fig. 4.9 SEM failure picture of dummy gate structure transistor under MM ESD zapping. (MM ESD robustness = 175 V, W/L = 240 μm/0.25 μm, dummy-gate length = 0.5 μm)

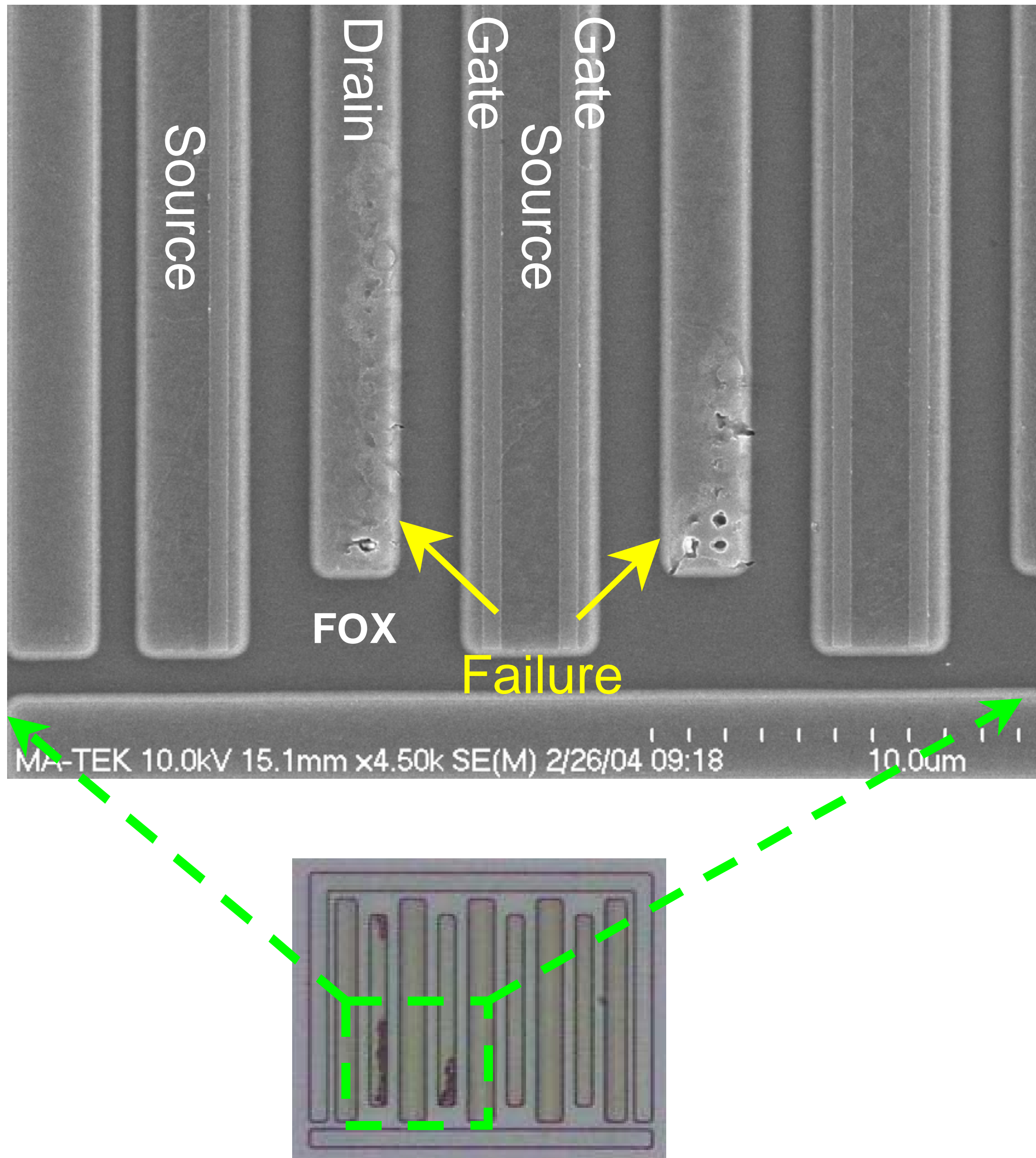

Fig. 4.10 SEM failure picture of FOX structure NMOS transistor under MM ESD zapping. (MM ESD robustness = 175 V, W/L = 240 μm/0.25 μm)

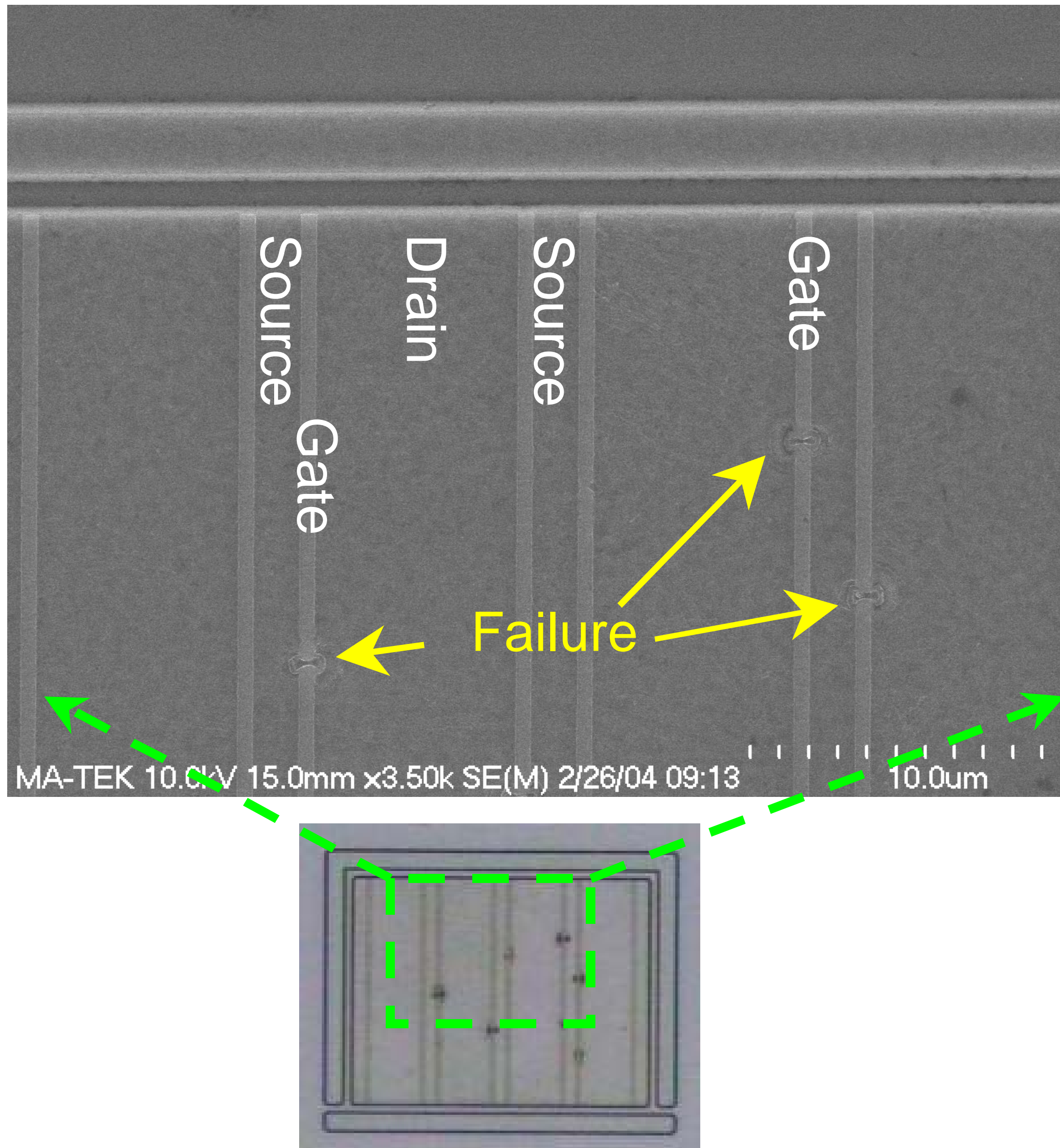

Fig. 4.11 SEM failure picture of fully-salicided structure NMOS transistor under MM ESD zapping. (MM ESD robustness = 225 V, W/L = 240 μm/0.25 μm)

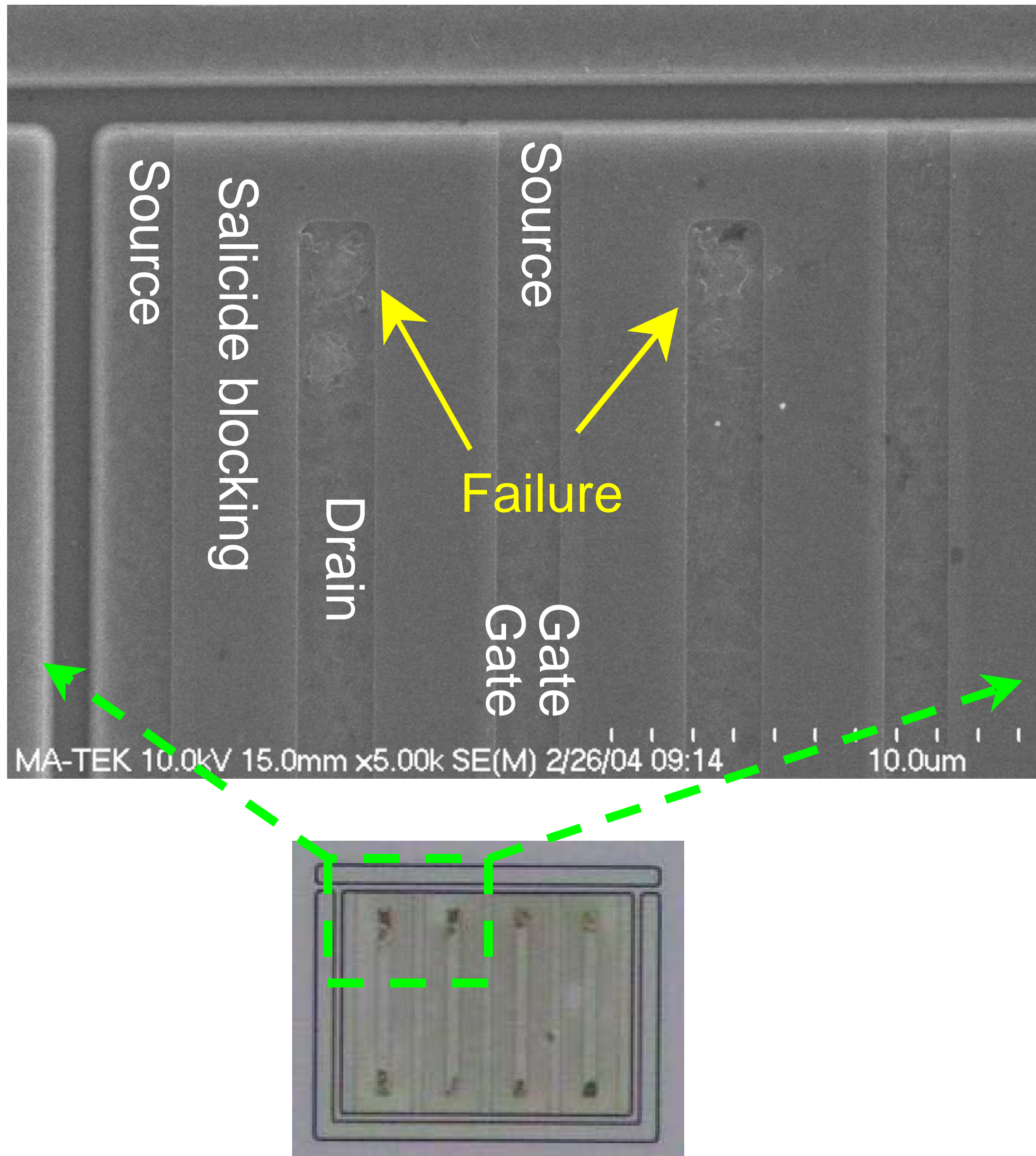

Fig. 4.12 SEM failure picture of salicide-blocking structure NMOS transistor under MM ESD zapping. (MM ESD robustness = 550 V, W/L = 240 μm/0.25 μm)

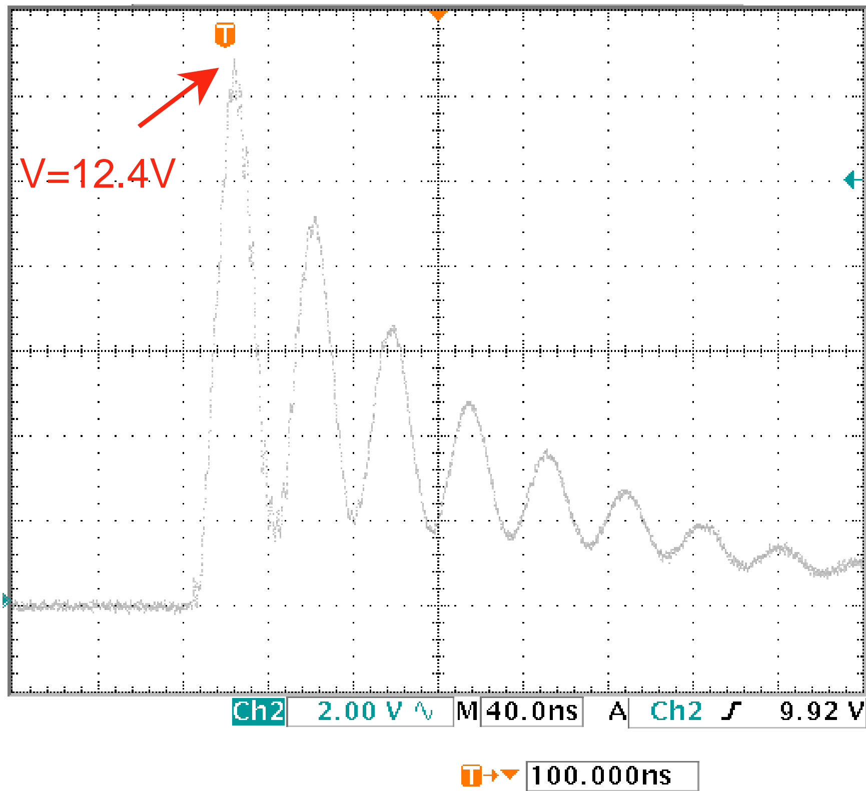

Fig. 4.13 The waveform of fully-salicided structure GGNMOS transistor under 1.1 kV HBM ESD zapping. (W/L = 240 μm/0.4 μm)

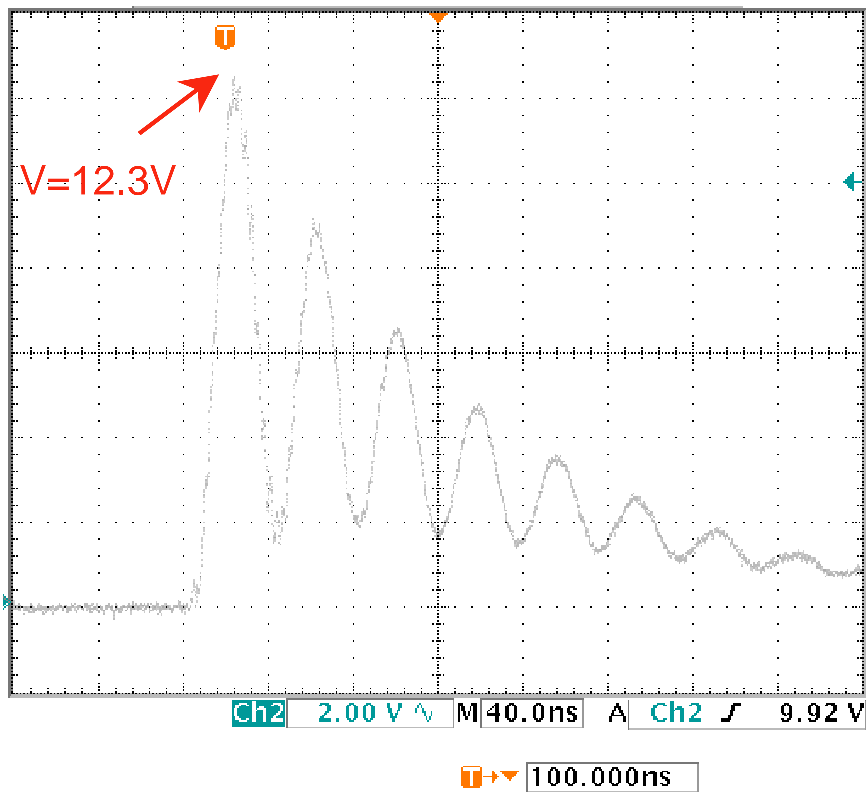

Fig. 4.14 The waveform of dummy-gate structure GGNMOS transistor under 1.1 kV HBM ESD zapping. (W/L = 240 μm/0.4 μm)

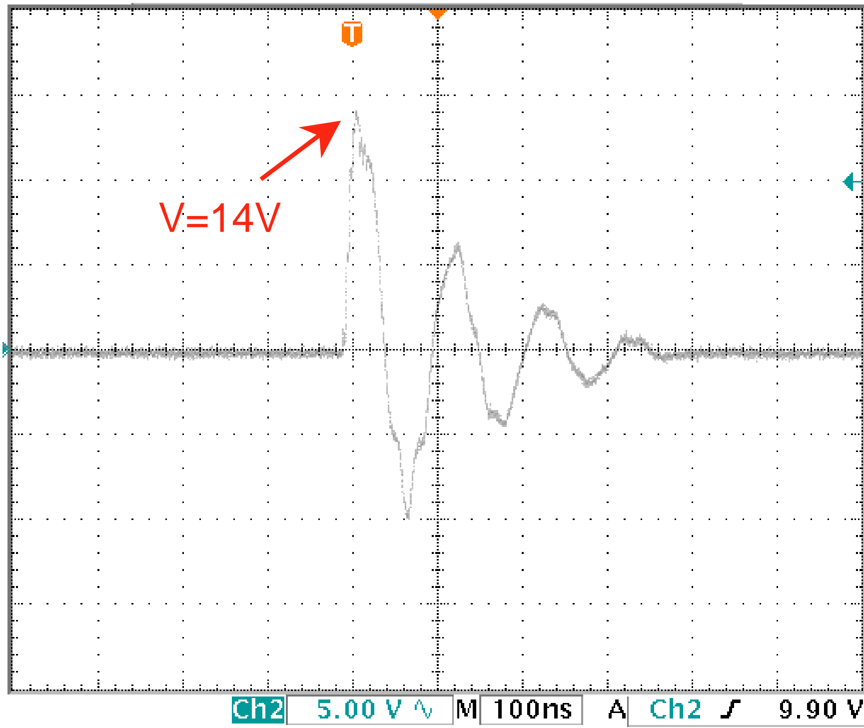

Fig. 4.15 The waveform of fully-salicided structure GGNMOS transistor under 130 V MM ESD zapping. (W/L = 240 μm/0.4 μm)

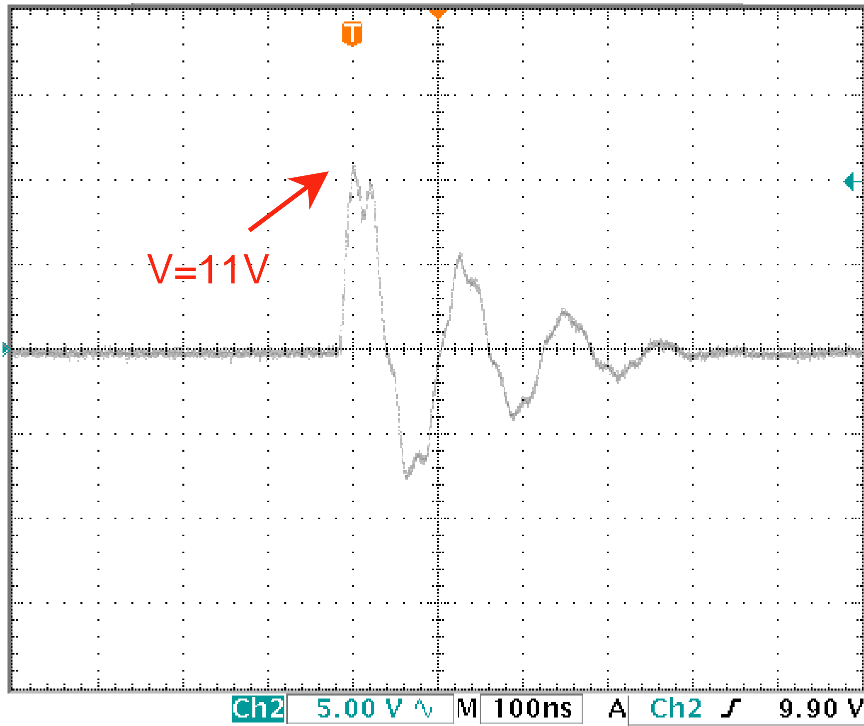

Fig. 4.16 The waveform of dummy-gate structure GGNMOS transistor under 130 V MM ESD zapping. (W/L = 240 μm/0.4 μm)

CHAPTER 5

CONCLUSIONS AND FUTURE WORKS

5.1 Conclusions

To improve the non-uniform turn-on issue and current localization in salicide CMOS technology, four different types of transistors are fabricated and compared previously. A novel dummy-gate structure NMOS transistor proposed to significantly improve machine-mode ESD robustness has been practically verified in 0.25 μm CMOS process in this work. The MM level of proposed dummy-gate structure NMOS transistor with dimension of W/L = 240 μm/0.25 μm is greater than 400 V. However, HBM ESD robustness of this kind GGNMOS is not better than that of conventional structure. The HBM ESD robustness of transistors is clamped by DCGS and drain contact to dummy-gate spacing discussed in Chapter 3 and Chapter 4. On the whole, the proposed novel dummy-gate structure NMOS transistor is process compatible with general CMOS process without any extra process to improve MM ESD robustness.

5.2 Future Works

According to the experimental results in Chapter 3 and Chapter 4, the MM ESD robustness of GGNMOS has been improved by applying novel dummy-gate structure. However, HBM ESD robustness of GGNMOS with dummy gate structure is not better than that with conventional structure. This is because HBM ESD robustness of transistors is limited by drain contact to dummy-gate spacing. So, the result is quite different with the expected goal. So, the drain contact to dummy gate spacing needs to be optimized to get a good ESD result.

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論文名稱：**矽化金屬互補式半導體製程之新型靜電放電防護元件**

New ESD protection devices with dummy-gate structure in a fully salicided CMOS technology