利用溶膠-凝膠法成長高介電常數奈米結晶粒之 SONOS 型記憶體元件

學生 :黃 建 文　　指導教授: 柯 富 祥　博士

劉 增 豐　博士

國立交通大學

奈米科技研究所碩士班

摘要

傳統浮停閘結構的快閃記憶體，當元件的穿隧氧化層厚度小於 10 奈米時，原本儲存在複晶矽浮停閘的電荷，很容易因為在氧化層的缺陷，形成漏電路徑，造成原本儲存的資料流失。因此 SONOS 結構的記憶體元件，被提出是可以解決當元件尺寸縮小時，浮停閘結構所面對的問題。傳統 SONOS 結構的記憶體元件，是使用氮化矽作為電荷陷捕層，在此種結構內，因為電荷是被儲存在分離式的陷捕位置中，故可改善在浮停閘結構中對於資料保存性的問題。但是因為氮化矽與穿隧氧化層之間的導電帶位能差太低，會使得元件的寫入、抹除速度降低，因此使用高介電常數材料作為 SONOS 結構的陷捕電荷層，目前正被廣泛研究著。

一般沉積高介電常數材料的方法有許多種，如:原子層沉積法、物理氣相沉積法(濺鍍)、金屬有機沉積法，但是上述的方法所需要的成本相當昂貴。而在本

篇論文中則提出了使用溶膠-凝膠法來沉積高介電常數材料作為 SONOS 結構的陷捕電荷層的方法。溶膠-凝膠法相較於其他方法而言的優點在於成本較便宜，而且可輕易的混合兩種或三種的高介電常數材料，藉以提昇記憶體之特性。

在本論文的第二章中，我們使用溶膠-凝膠法將二氧化鉿、以及二氧化矽的前驅物: 四氯化鉿、四氯化矽混合，一起溶入異丙醇中，藉由溶膠-凝膠法在穿隧氧化層上沉積，再經過 900 度的快速熱退火形成一種混合雙元結晶粒的高介電常數材料作為 SONOS 結構的陷捕電荷層。從論文中的 TEM 圖可看出，經過了快速熱退火步驟後，在陷捕電荷層中形成了奈米微晶粒。而元件的電性也比單一的二氧化鉿元件，表現出更大的記憶窗口與較好的電荷保存能力。這項特性應與雙元的高介電常數材料，具有比單一的高介電常數材料具有較多的陷捕電荷位置有關。由於溶膠-凝膠法是一種簡單、快速且低成本的技術，為一種製備高介電常數材料作為 SONOS 結構的陷捕電荷層的新穎方法。

而在第三章中，我們詳述了利用溶膠-凝膠法製備矽酸鉿與矽酸鋯奈米結晶粒共存於 SONOS 型記憶體的方法。由溶膠-凝膠法與快速熱退火處理製備矽酸鉿與矽酸鋯奈米結晶粒，在各項特性上都有著良好的表現。如具備更佳的電荷保存能力及良好的元件容忍度等。同時，我們也證明了其具有相較於矽酸鉿奈米結晶粒記憶體更佳的性能，應有應用於未來工業界記憶體之潛力。

SONOS-Type Memory Devices with High-K Nanocrystals by Sol-Gel Spin Coating Deposition

Student: Chien-Wen Huang Advisor: Fu-Hsiang Ko

Tzeng-Feng Liu

Institute of Nanotechnology

National Chiao Tung University

ABSTRACT

In the traditional floating gate Flash memory structure, when the tunneling oxide is below 10nm, the storage charge in the poly-silicon floating gate is easy to leak due to the defects in the tunneling oxide. The SONOS structure is proposed to solve this problem of floating gate structure when the device is scaling down. In conventional SONOS memory device, the charge trapping layer is silicon nitride and the storage charge is trapped in the discrete traps and this can improve the data retention problem of the floating gate structure. But in the traditional SONOS memory, the conduction band offset between tunneling oxide and silicon nitride is so small and this will slower the program speed. So using high-k dielectrics to replace traditional silicon nitride has been widely studied.

Traditional high-k thin films have been prepared by atomic layer deposition

(ALD), physical vapor deposition like sputter (PVD), and metal-organic chemical vapor deposition (MOCVD). However, the cost of these methods is very high. In this thesis, we propose the sol-gel spin coating method to deposit the high-k dielectrics as the purpose of charge trapping layer for the SONOS-type memory. The advantages of the sol-gel spin coating method are lower cost than other methods and easy to synthesize two or three different high-k dielectrics.

In chapter 2, we synthesize the combined film of HfO_2 and SiO_2 by using the precursor of $HfCl_4$ and $SiCl_4$ together. Prior to 900^oC rapid thermal annealing, these precursors are dissolved in the IPA and spin coating to form the binary high-k charge trapping layer for SONOS-type memory. From the TEM analysis, the nanocrystals are formed after 900^oC annealing. This binary high-k charge trapping layer show the larger memory window and better charge retention ability than HfO_2 charge trapping layer only. This observation is attributed to the more trapping sites in the binary high-k charge trapping layer. We think sol-gel spin coating method is a simple, fast, and low cost method to apply for the high-k charge trapping layer deposition of SONOS-type memory.

In chapter 3, we fabricate the SONOS-type memory with co-existed hafnium silicate and zirconium silicate nanocrystals for the first time. The performance of the co-existed hafnium silicate and zirconium silicate nanocrystals formed by the sol-gel spin coating method and RTA treatment exhibits better properties in terms of long charge retention time, and good endurance. We also found the co-existed hafnium silicate and zirconium silicate have better device performance than the hafnium silicate nanocrystal memory only. This new type of memory is beneficial for the future industry.