Chapter 2
Hafnium Silicate ($HfSi_xO_y$) Nanocrystal SONOS-Type Flash Memory Fabricated by Sol-Gel Spin Coating Method Using $HfCl_4$ and $SiCl_4$ as Precursors

2-1 Introduction

The demand for high-density, low-cost, low-power consumption, and fast program/erase speed on semiconductor memory will lead the current baseline memory technologies to several revolutionary and evolutionary approaches such as SONOS high-K memory and nanocrystal memory. But SONOS high-K memory has the electron migration problem in the charge trapping layer [39], this will cause the charge loss and degrade the charge retention performance. The nanocrystal memory can keep the trapped charge tightly to avoid the charge loss problem of SONOS memory and also possesses the advantages of fast program/erase speed, low programming voltage and good endurance as SONOS memory [40-41]. In this chapter, we propose a novel technique for the first time to form the hafnium silicate ($HfSiO_x$) nanocrystals for the charge trapping layer of the SONOS memory. We propose the sol-gel spin coating method to deposit the high-K charge trapping layer on the tunneling oxide of the SONOS device followed by 900°C 1min RTA to form nanocrystals. The film formation with spin-coating is a very simple method than ALD, PVD or CVD due to its cheaper precursor and tool. In addition, the film can be fabricated in the normal pressure system rather than an high vacuum system [42].

In this chapter, we use sol-gel spin coating method to deposit charge trapping layer on the tunneling oxide and 900°C 1min RTA to

form nanocrystals for the SONOS nanocrystal memory. Physical and electrical analysis like XPS, TEM, Id-Vg, retention, and program/erase speed are obtained to evaluate the performance of novel sol-gel-derived binary high-k nanocrystals as the charge trapping sites for SONOS-type memory application.

2-2 Experimental procedure

First, two mother sol solutions of HfO_2 and SiO_2 were prepared to synthesize the binary high-k precursor solution. $HfCl_4$ (99.5%, Aldrich, USA) was used as the precursor for the synthesis of hafnia. A mother sol solution was first prepared by dissolving $HfCl_4$ in isopropanol (IPA; Fluka; water content < 0.1%) under vigorous stirring in an ice bath. The sol solution was obtained by fully hydrolyzing $HfCl_4$ with a stoichiometric quantity of water in IPA to yield a Hf : IPA molar ratio of 1:500. $SiCl_4$ (99.5%, Aldrich, USA) was used as the precursor for the synthesis of silicide.

We also dissolved $SiCl_4$ in isopropanol (IPA; Fluka; water content < 0.1%) under vigorous stirring in an ice bath to prepare mother sol solution. The sol solution was obtained by fully hydrolyzing $SiCl_4$ with a stoichiometric quantity of water in IPA to yield a Si : IPA molar ratio of 1:500, too. Then, we recombined these two solutions ($HfCl_4$ and $SiCl_4$) of molar ratio of 1:500 and added some IPA to yield a solution of final molar ration of Hf : Si : IPA is 1:1:1000.

The fabrication of sol-gel spin coating nanocrystal memory is started with LOCOS isolation process on p-type (100) 150-mm silicon substrate. At the beginning, a 4-nm tunneling oxide was thermally grown at 925°C by furnace. The high-k layer was prepared using a sol–gel spin-coating method. The high-k layer was deposited by spin-coating at 3000rpm for 60s at ambient temperature (25°C). The spin-coater used was TEL Clean

Track Model-MK8 (Japan). After spin-coating, the wafer was subjected to rapid thermal annealing (RTA) at 900°C for 60s in O_2 ambient to form hafnium silicate ($HfSiO_x$) nanocrystals. The 30nm blocking oxide was deposited by HDPCVD TEOS, followed by poly-Si gate 200nm deposition. Finally, gate pattering, source/drain (S/D) implant, and the rest of the subsequent CMOS processes were used to fabricate this SONOS memory. The process flow and the structure of the sol-gel SONOS-type memory are depicted in Fig. 2-1 and Fig. 2-2, respectively.

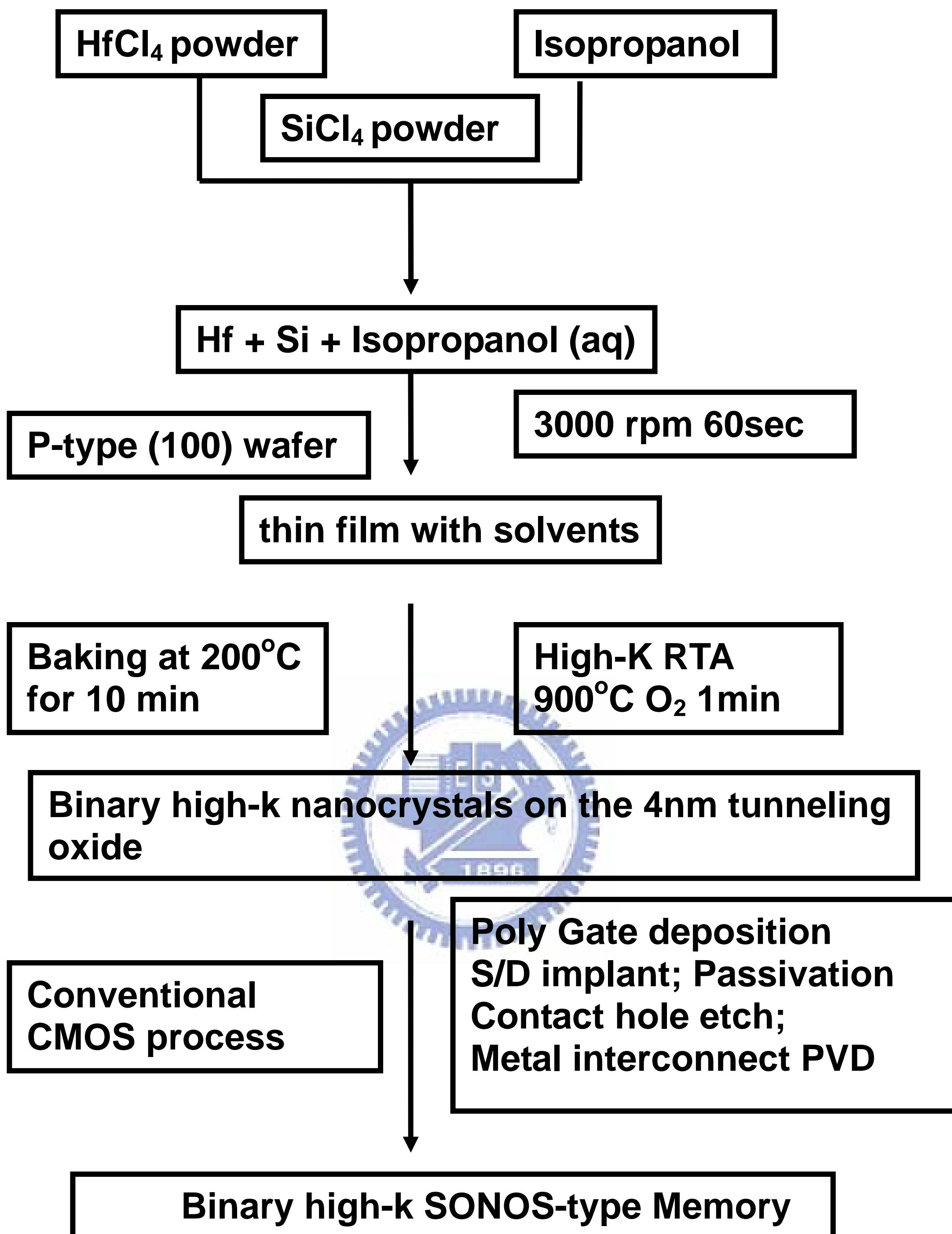

Fig. 2-1: The process flow of the binary high-k SONOS-type nanocrystal memory.

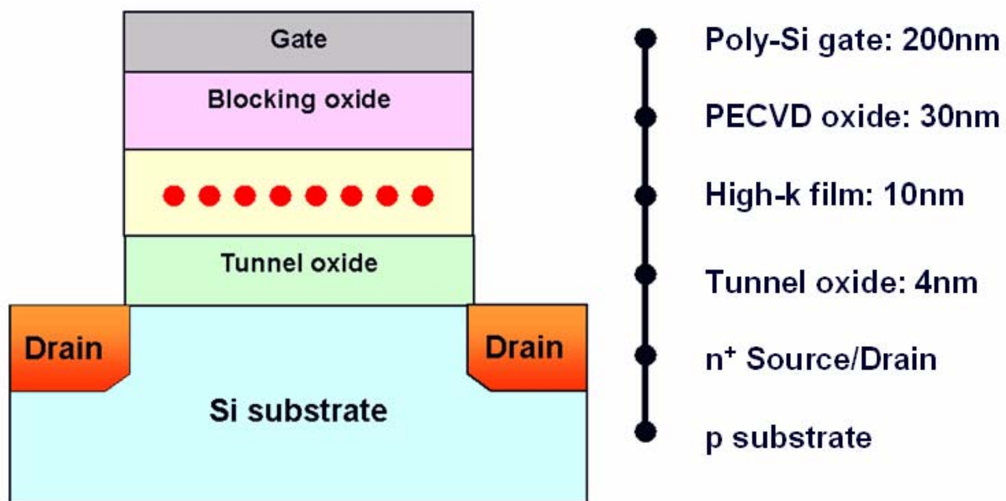

Fig. 2-2: Device structure of hafnium silicate nanocrystal memory.

2-3 Results and Discussion

In this section, the physical and electrical characteristics of sol-gel-derived binary high-k SONOS-type nanocrystal memory were discussed.

2-3.1 Electrical Characteristics

2-3.1.1 Id-Vg Curve

Figure 2-3 shows the Id-Vg curve of the state-of-the-art Device. We use channel hot electron injection to program, and band to band tunneling induced hot hole injection (BTBHHI) to erase. The program condition is Vg = 15V, Vd = 10V for 10 msec. The erase condition is Vg = -10V, Vd = 10V for 1 sec. The memory window of Device is estimated to be 3.3V.

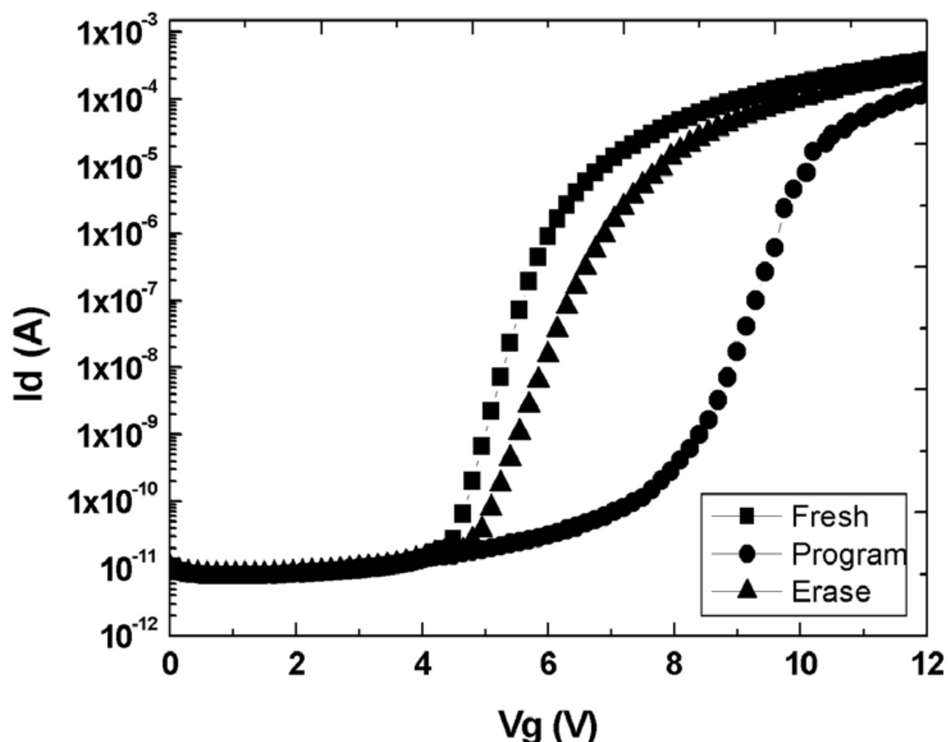

Fig. 2-3: The Id-Vg curve of the hafnium silicate nanocrystal memory.

2-3.1.2 Program/Erase Speed

Figure 2-4 shows the program speed of the hafnium silicate nanocrystal memory. We use channel hot electron (CHE) to program and the program conditions are (i) Vg= 10V, Vd= 10V; (ii) Vg= 12V, Vd= 10V; (iii) Vg= 15V, Vd= 10V, respectively. The Vth shift increases as increasing the applied gate voltage due to more “hot” electrons generated to reach the trapping layer and to be trapped in the charge trapping layer.

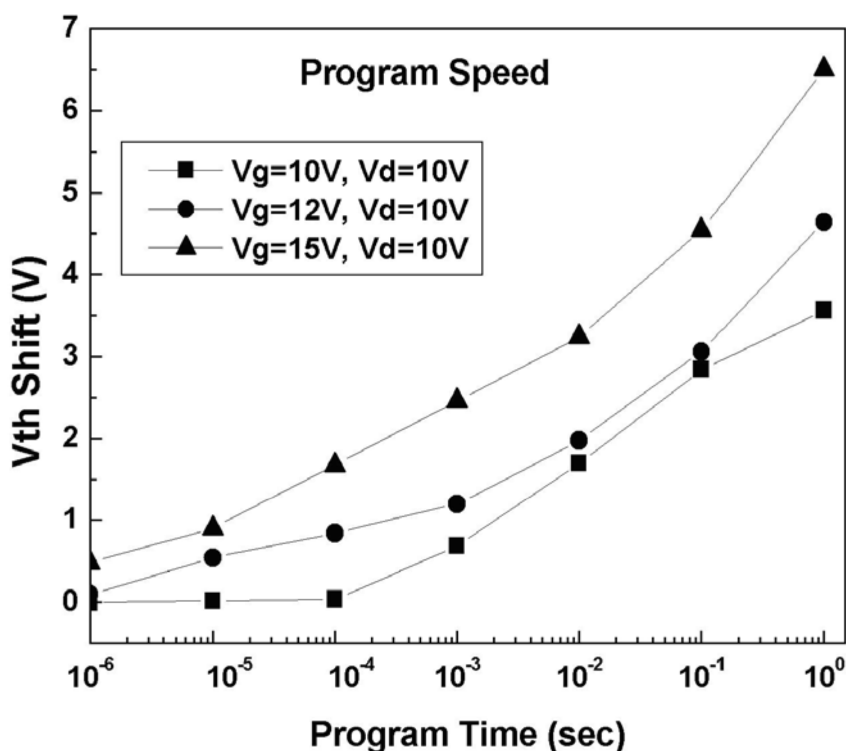

Fig. 2-4: The program speed of the hafnium silicate nanocrystal memory..

Figure 2-5 shows the erase speed of the hafnium silicate nanocrystal memory. We use band to band hot hole (BTBHH) to erase and the erase conditions are (i) Vg= -10V, Vd= 10V; (ii) Vg= -12V, Vd= 10V; (iii) Vg= -15V, Vd= 10V, respectively. It can be observed from the Figure that as the gate voltage becomes more negative, the erase effect becomes much

stronger than the less negative one does.

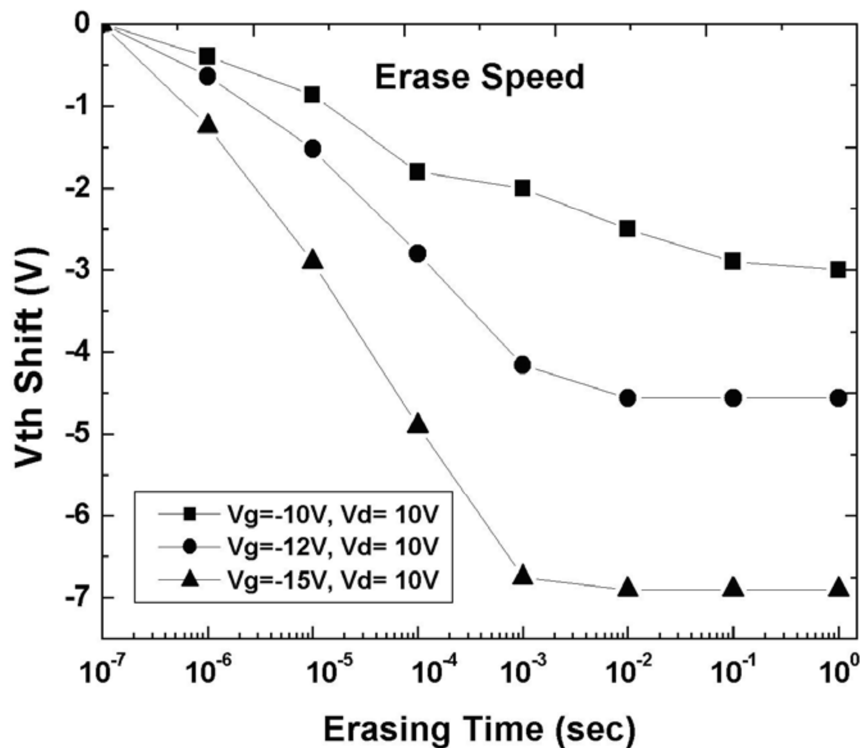

Fig. 2-5 : The erase speed of the hafnium silicate nanocrystal memory.

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2-3.1.3 Data Retention Characteristics

Figure 2-6 shows the charge retention characteristics of the hafnium silicate nanocrystal memory. The normalized Vth shift is defined as the Vth shift at time of interest divided by the Vth shift at the beginning. Using this as an indicator, we can see the charge loss in the SONOS memory. The curve is measured under program condition Vg= 12V, Vd= 10V 10msec at the room temperature of 25°C. We can see from the curve when measure time up to 10^4 sec, only 6% charge loss. This observation suggests the hafnium silicate nanocrystals in the charge trapping layer can tightly catch the tunneling electrons and the trapped electrons are hard to get out. Hence, the charge loss percentage of nanocrystal memory is very

small.

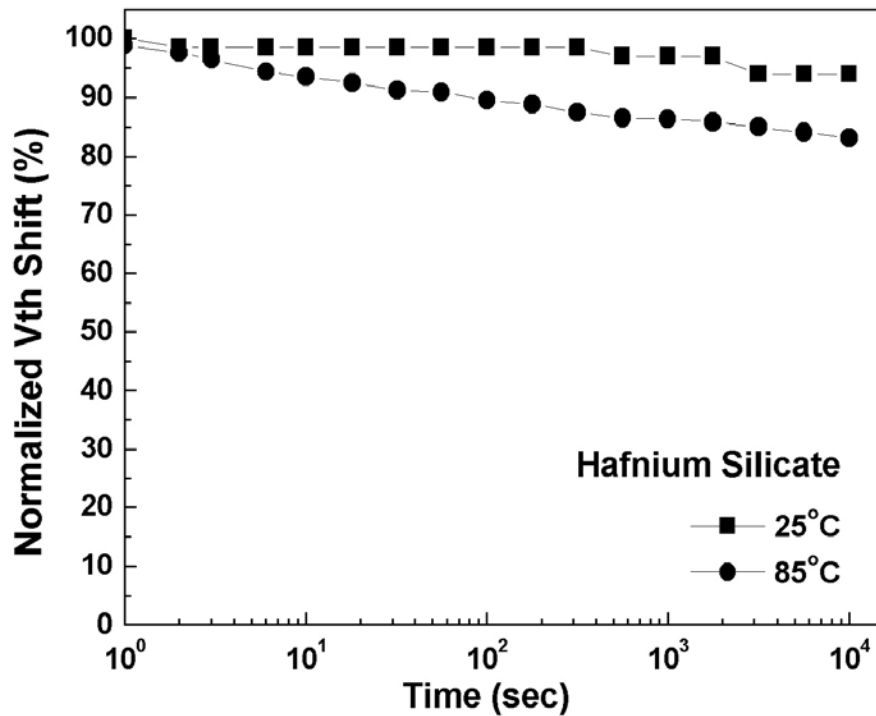

Fig. 2-6 : The data retention of the hafnium silicate nanocrystal memory.

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2-3.1.4 Endurance Characteristics

Figure 2-7 shows the endurance characteristics of the nanocrystal memory. The measure condition is program Vg = 15V, Vd = 10V, 1 msec; erase: Vg = -10V, Vd = 10V, 10 msec. As the Figure shows, the memory window is about 2.8V after 10^5 P/E cycles. No significant window narrowing is observed. This observation ensures the reliability of our hafnium silicate nanocrystal memory formed by spin-coating method. This finding suggests the developed simple sol-gel spin coating process can be incorporated into the SONOS nanocrystal memory fabrication in the future.

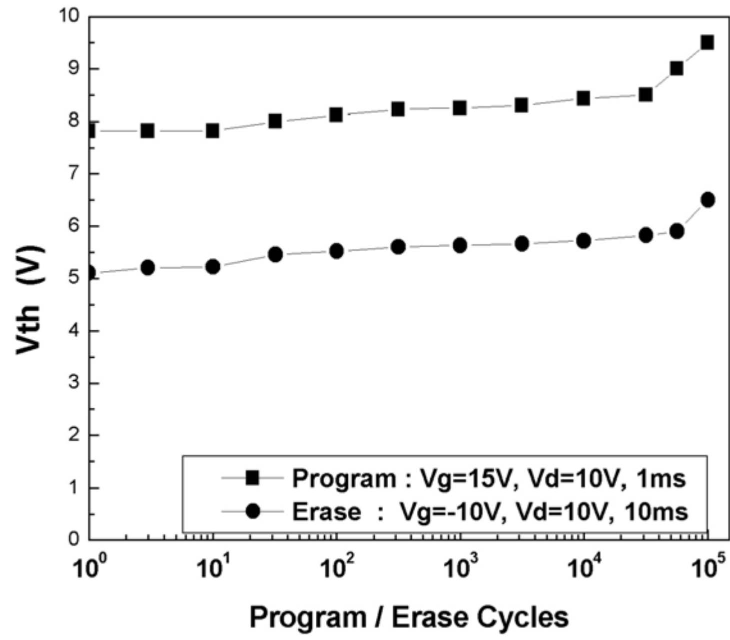

Fig. 2-7 : Endurance of the hafnium silicate nanocrystal memory.

2-3.2 Physical characterization of the sol-gel-derived hafnium silicate ($HfSi_xO_y$) nanocrystal SONOS memory

2-3.2.1 HRTEM

Figure 2-8 shows the high-resolution transmission electron microscopy (HRTEM) images of the nanocrystal on SiO_2 after annealing at 900 °C for 60 s. The average nanocrystal size is around 5 nm. The clearly visible lattice fringes denote crystallization into a well-ordered microstructure, as is typically observed [43].

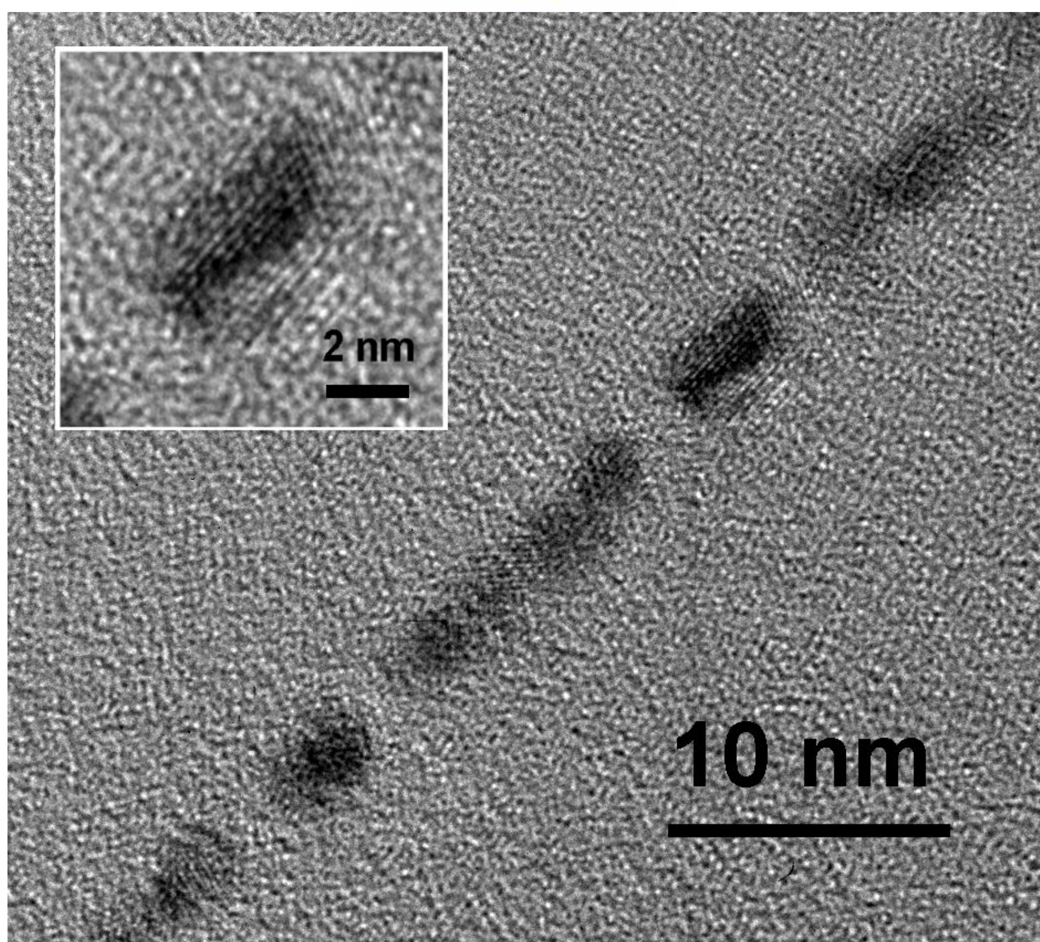

Fig. 2-8: The high-resolution transmission microscopy (HRTEM) images of the nanocrystal on SiO_2 after annealing at 900 °C for 60 s

2-3.2.2 XPS

Chemical characterization of $HfSi_xO_y$ films was accomplished by x-ray photoelectron spectroscopy (XPS). Figure 2-9 shows Hf 4 *f* XP spectra for our sample. Specifically, as the film is heated, the peak shifts from 17.4 eV (at 200°C) to 18.0 eV (at 900 °C) [44-45]. The observed binding energy shift in Figure 2-9 could be attributed to the silicate formation . Although it is not illustrated here, the Si 2p peak at ~102.8 eV in the spectrum corresponds to Hf-silicate bonding energy [46].

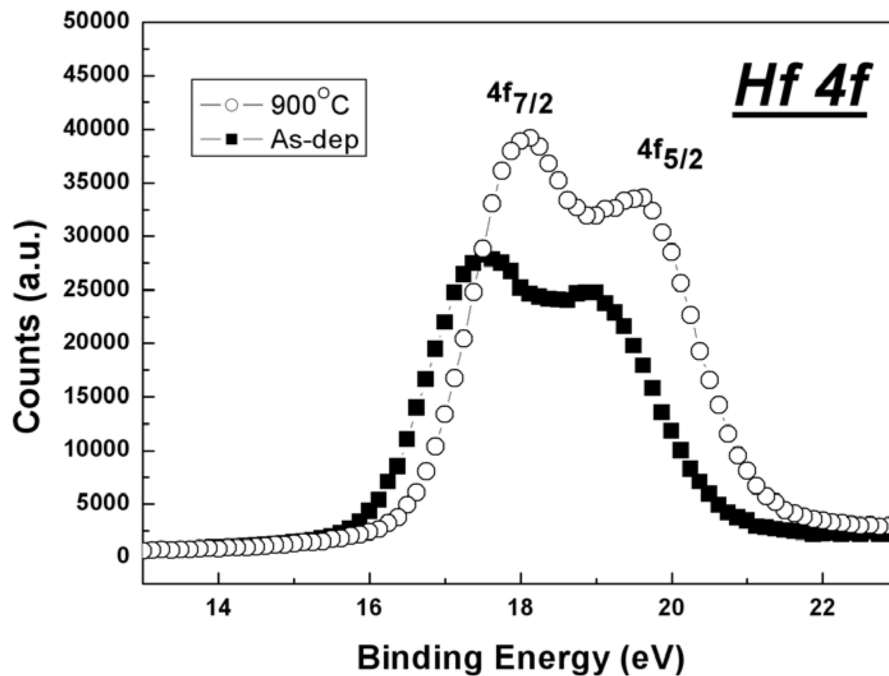

Fig. 2-9: Hf 4 *f* XP spectra for our sample.

2-4 Summary

In this chapter, we propose a new spin coating method to form nanocrystals for the charge trapping layer of SONOS memory. The XPS analysis reveals the composition of the binary high-k film. The TEM image verifies the formation of nanocrystal in the charge trapping layer. We have demonstrated the device performance with the Id-Vg curve, P/E speed, charge retention, and endurance. The quality of the nanocrystals formed by the sol-gel spin coating method and RTA treatment exhibits better properties in terms of fast P/E speed(10 usec / 1msec), long charge retention time due to hafnium silicate nanocrystals in the charge trapping layer, and good endurance up to 10^5 P/E cycles with no memory window narrowing. The proposed simple sol-gel spin coating process exhibits the potential to be incorporated into the future nanocrystal memory fabrication processes.