Chapter 3

Sol-Gel-Derived Zirconium Silicate ($ZrSi_xO_y$) and Hafnium Silicate ($HfSi_xO_y$) Co-existed Nanocrystal SONOS Memory

3-1 Introduction

In the previous chapter, we fabricate the sol-gel-derived hafnium silicate ($HfSiO_x$) nanocrystals for the charge trapping layer of the SONOS memory. We use metal halides dissolved into IPA organic solvent to prepare these precursors. By going through the hydrolysis, condensation, and polymerization steps, metal oxide networks are formed [47]. The most attractive advantage of the sol-gel method is easy to deposition the layer at low temperature. For example, the sol-gel process is a synthesis method in which ceramics are formed by mixing and reaction of liquid chemical at room temperature. As the mixing process is accomplished in the liquid state, the resulting ceramics can be very homogeneous, and uniform at the atomic or molecular level.

In this chapter, we use sol-gel method to combine three high-k precursors, i.e. $HfCl_4$, $ZrCl_4$ and $SiCl_4$ together to form hafnium silicate and zirconium silicate co-existed in a SONOS type memory device for the first time. Physical and electrical analysis like XPS, TEM, Id-Vg, retention, and program/erase speed are obtained to evaluate the performance of sol-gel-derived high-k nanocrystals to become charge trapping sites for SONOS-type memory application.

3-2 Experimental procedure

We use $HfCl_4$ (99.5%, Aldrich, USA), $ZrCl_4$ (99.5%, Aldrich, USA), and $SiCl_4$ (99.5%, Aldrich, USA) as precursors. These precursors are dissolved into isopropanol (IPA; Fluka; water content < 0.1%) to prepare respective high-k material mother solution. $HfCl_4$, $ZrCl_4$, and $SiCl_4$ are used as the precursors for the new hafnium silicate and zirconium silicate co-existed nanocrystal memory. We add some IPA solvent to yield the molar ratio: $HfCl_4$: $ZrCl_4$: $SiCl_4$: IPA = 1:1:1:1000, for charge trapping layer deposition.

The fabrication of sol-gel spin coating nanocrystal memory is started with LOCOS isolation process on p-type (100) 150-mm silicon substrate. At the beginning, a 4-nm tunneling oxide was thermally grown at 925°C by furnace. The charge trapping layer was deposited by spin coating at 3000rpm for 60 sec at ambient temperature (25°C). The spin-coater used was TEL Clean Track Model-MK8 (Japan). After spin coating, the wafer was under rapid thermal annealing (RTA) at 900°C for 60 sec in O_2 ambient to form hafnium silicates and zirconium silicates co-existed nanocrystal memory. The 30nm-thick blocking oxide was deposited by LPCVD TEOS followed by poly-Si gate 200nm deposition. After the LPCVD TEOS deposition, the TEOS oxide is densified in N_2 ambient under 900°C for 30s anneal. We think this can repair the defects and decrease the number of traps in the TEOS oxide. Finally, gate pattering, source/drain (S/D) implant, and the rest of the subsequent CMOS processes were used to fabricate this SONOS-like memory. The process flow and the structure of the sol-gel SONOS-type nanocrystal memory are depicted in Fig. 3-1 and Fig. 3-2, respectively.

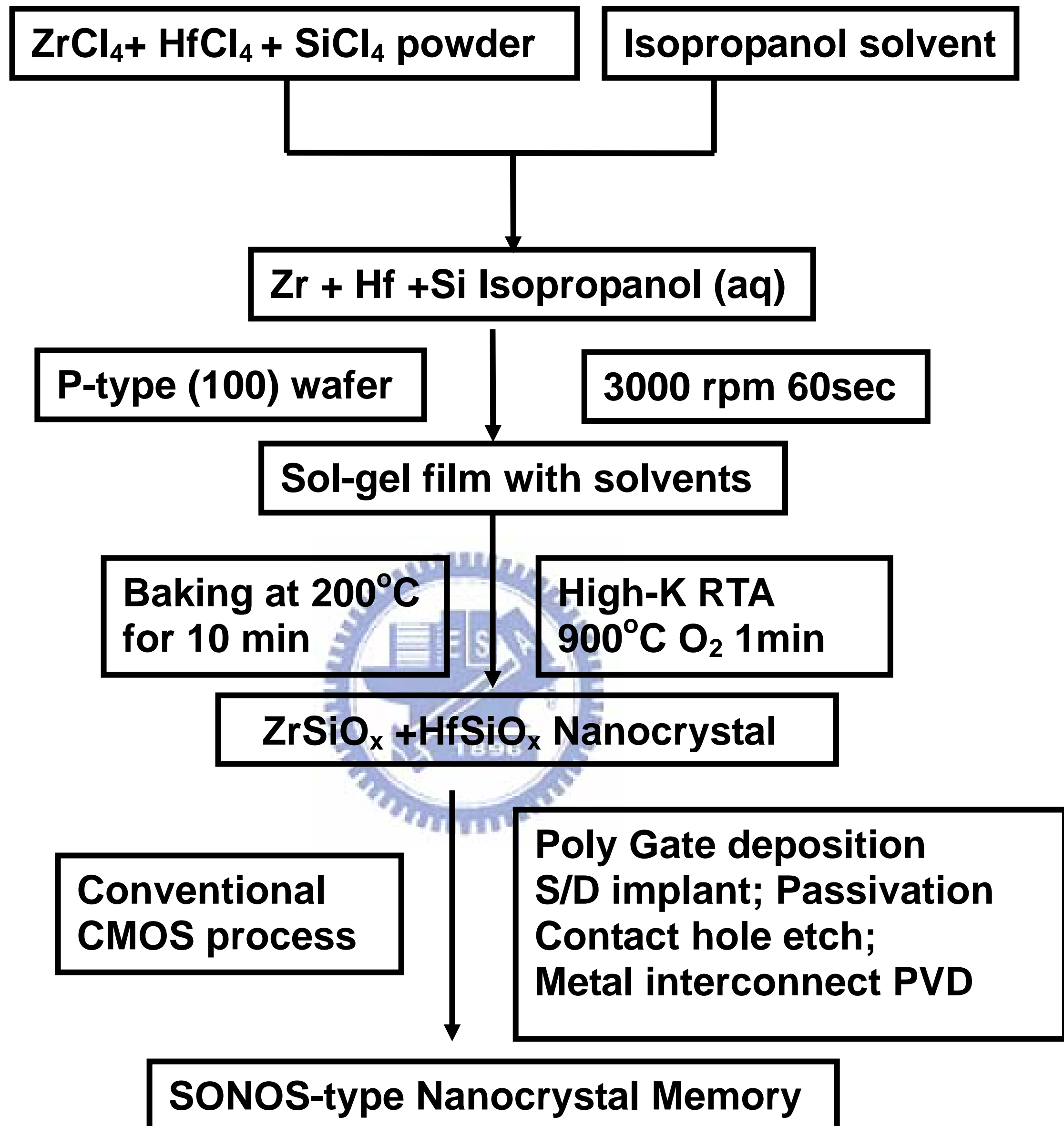


Fig. 3-1: The process flow of the high-k SONOS-type nanocrystal memory.

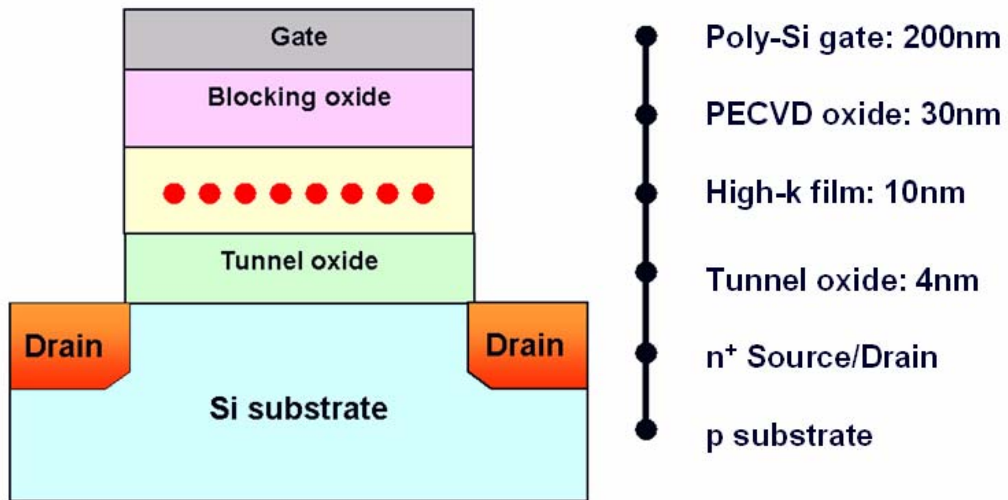


Fig. 3-2: The device structure and fabrication process for the co-existed zirconium silicate ($ZrSi_xO_y$) and hafnium silicate ($HfSi_xO_y$) memory.

3-3 Results and Discussion

In this section, the electrical and physical characteristics of sol-gel-derived SONOS-type nanocrystal memory were discussed. We also compare the electrical characteristics between co-existed hafnium-and zirconium- silicates nanocrystal memory, and hafnium silicates memory.

3-3.1 Electrical Characteristics

3-3.1.1 Id-Vg Curve

Figure 3-3 shows the Id-Vg curve of hafnium silicates and zirconium silicates co-existed nanocrystal memory. We use channel hot electron injection to program, and band to band tunneling induced hot hole injection (BTBHHI) to erase. We also show the Id-Vg curve of hafnium silicates memory again in Figure 3-4 to compare their electrical characteristics. The program condition is Vg = 15V, Vd = 10V for 10 msec. The erase condition is Vg = -10V, Vd = 10V for 1 sec. The memory window of hafnium silicates and zirconium silicates co-existed nanocrystal memory and hafnium silicates memory are 4V and 3.3V respectively. The hafnium silicates and zirconium silicates co-existed nanocrystal memory has larger Vth shift than hafnium silicates due to more nanocrystals existed in the charge trapping layer.

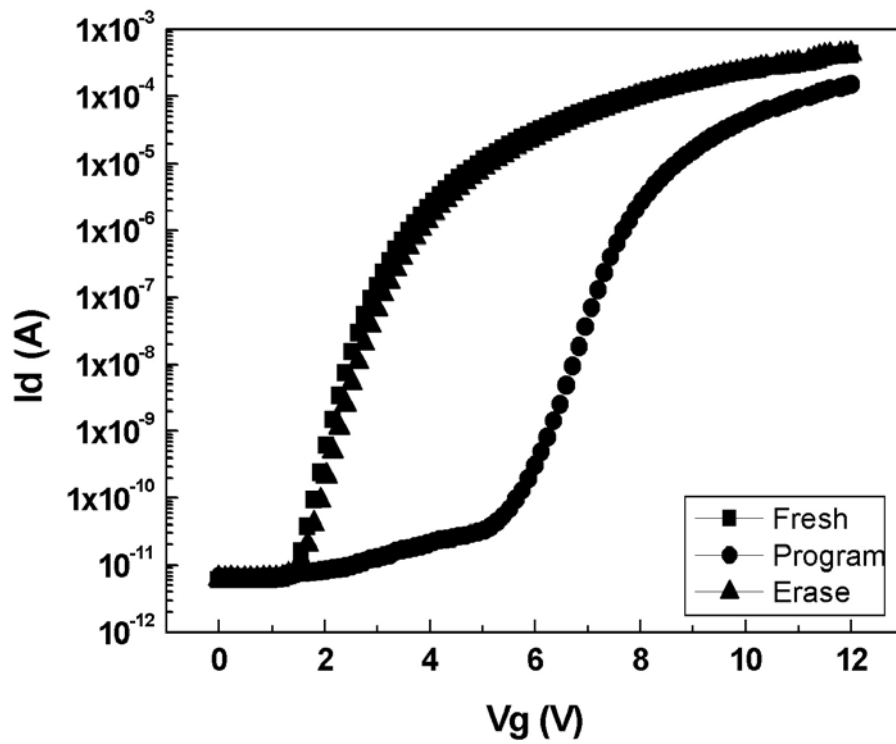


Fig 3-3: The Id-Vg curve of hafnium silicates and zirconium silicates co-existed nanocrystal memory.

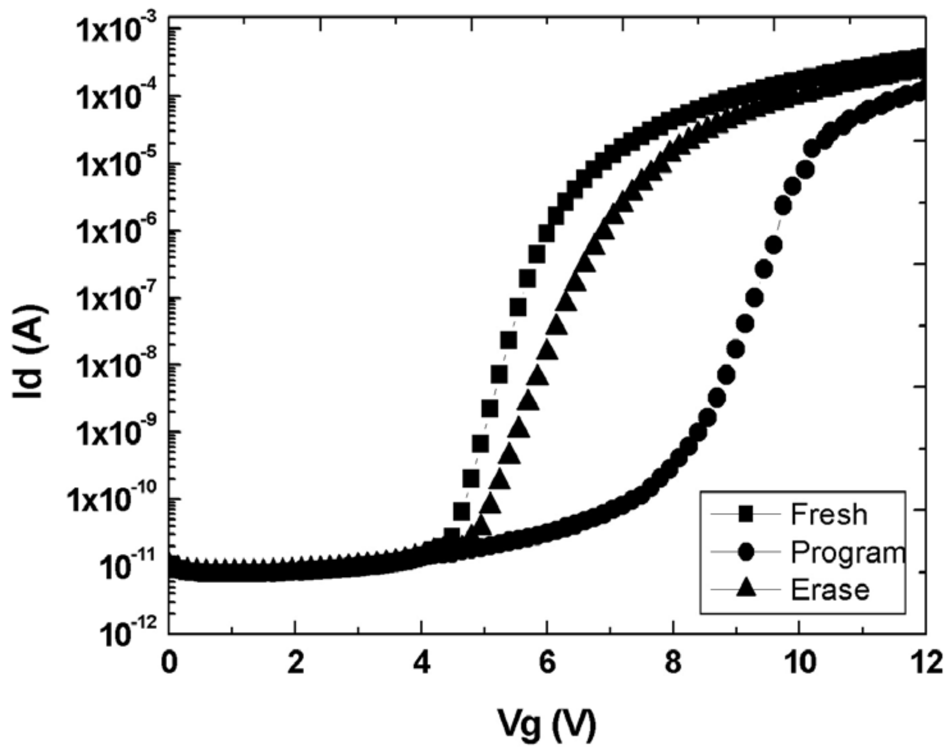


Fig 3-4: The Id-Vg curve of hafnium silicates nanocrystal memory.

3-3.1.2 Program/Erase Speed

Figure 3-5 shows the program speed curve of the hafnium silicates and zirconium silicates co-existed nanocrystal memory. We use channel hot electron (CHE) to program, and the program conditions are (i) Vg= 10V, Vd= 10V; (ii) Vg= 12V, Vd= 10V; (iii) Vg= 15V, Vd= 10V, respectively. The Vth shift increases as increasing the applied gate voltage due to more "hot" electrons generated to reach the trapping layer and to be trapped in the charge trapping layer.

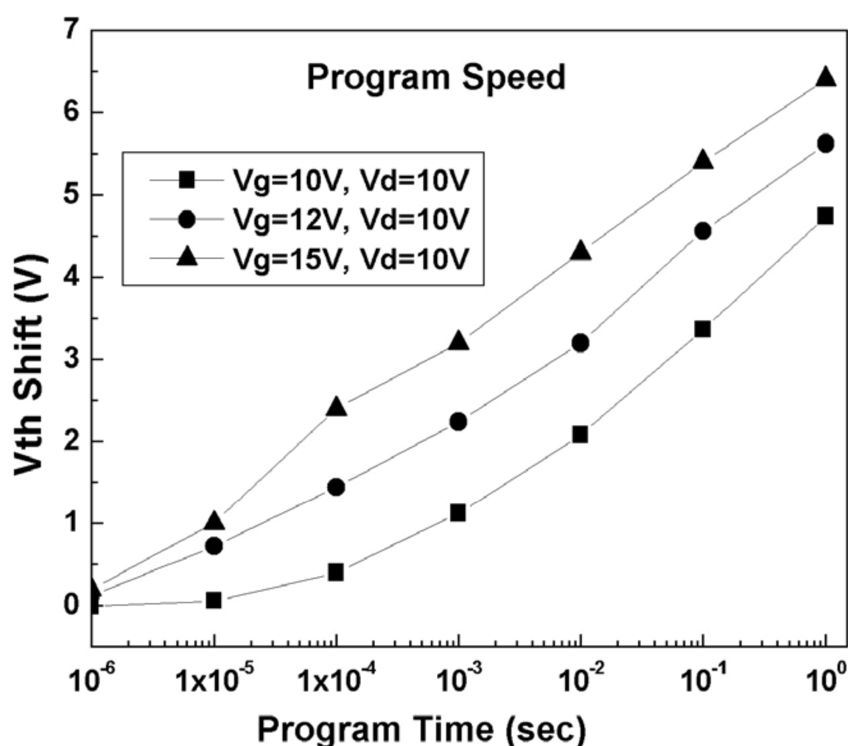


Fig. 3-5: The program speed of the hafnium silicates and zirconium silicates co-existed nanocrystal memory.

Figures 3-6 to 3-8 show their program speed comparison. We can see hafnium silicates and zirconium silicates co-existed nanocrystal memory demostrates larger Vth shift even under the same stress conditions. This phenomena is due to more trapping sites embedded in the hafnium

silicates and zirconium silicates co-existed nanocrystal memory.

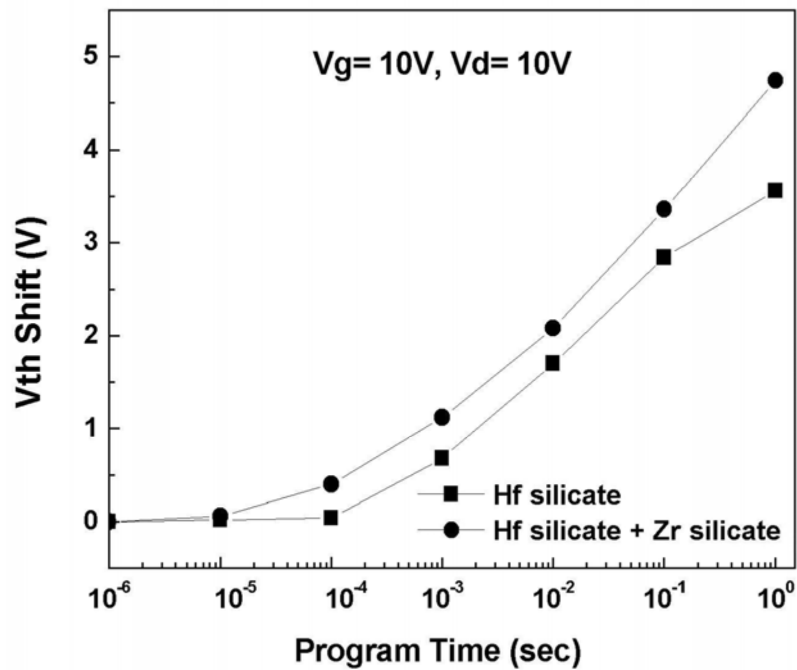


Fig. 3-6: The program speed comparison for Vg=10V, Vd=10V.

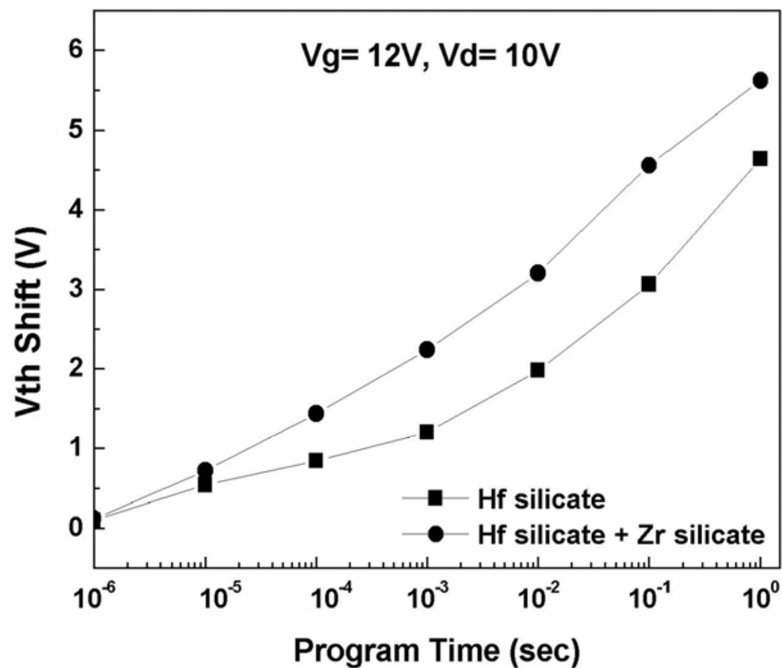


Fig. 3-7: The program speed comparison for Vg=12V, Vd=10V.

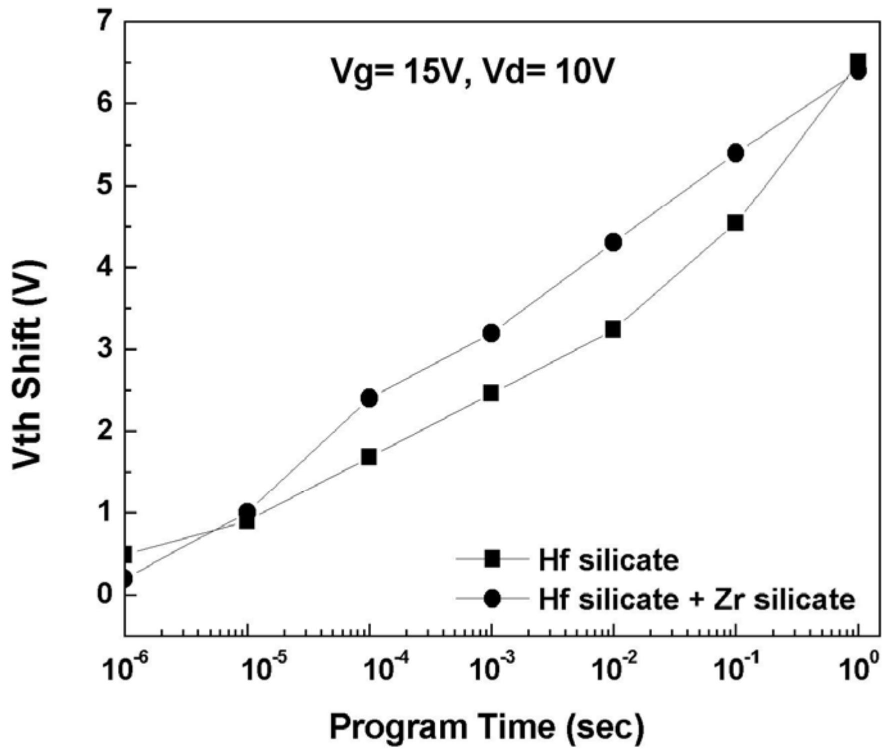


Fig. 3-8: The program speed comparison for Vg=15V, Vd=10V.

Figure 3-9 shows the erase speed curve for the hafnium silicates and zirconium silicates co-existed nanocrystal memory. We use band to band hot hole (BTBHH) to erase, and the erase conditions are (i) Vg= -10V, Vd= 10V; (ii) Vg= -12V, Vd= 10V; (iii) Vg= -15V, Vd= 10V, respectively. As the gate voltage becomes more negative, the erase effect becomes much fast.

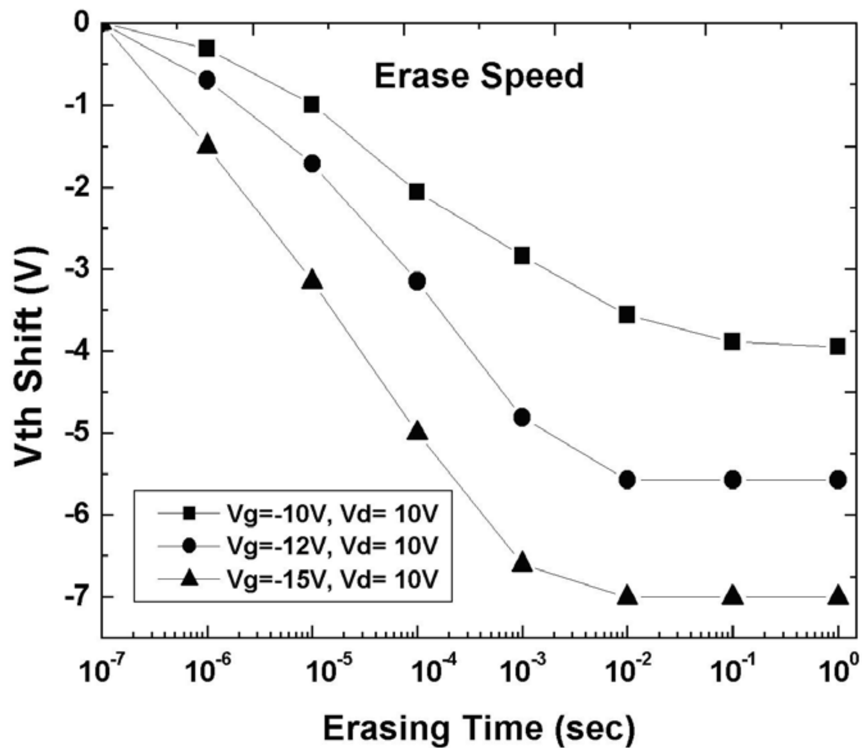


Fig. 3-9 : The erase speed of hafnium silicates and zirconium silicates co-existed nanocrystal memory.

3-3.1.3 Data Retention Characteristics

The charge retention characteristic of the hafnium silicates and zirconium silicates co-existed nanocrystal memory are demonstrated in Fig. 3-10. The normalized Vth shift is defined as the ratio of Vth shift at the time of interest and at the beginning. Using this as an indicator, we can see the charge loss for the nanocrystal memory. The data retention is measured under the room temperature 25°C and 85°C, respectively. The room temperature retention curve shows only 5% charge loss as measure time up to 10^4 sec and ~13% charge loss at 85°C for the hafnium silicates and zirconium silicates co-existed nanocrystal memory. This result indicates the nanocrystals in the charge trapping layer can tightly catch the tunneling electrons. Hence, the trapped electrons by the

sol-gel-derived nanocrystal devices are not easily to escape, and the exhibited charge loss percentage is quite low.

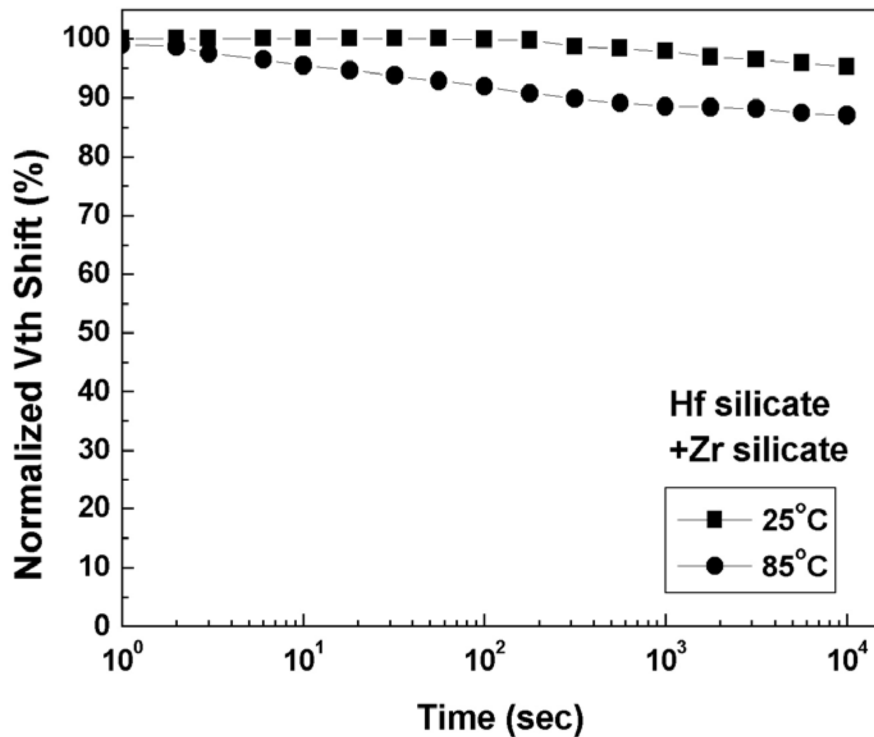


Fig. 3-10 : The data retention of the nanocrystal memory.

3-3.1.4 Endurance Characteristics

Endurance measurement of the hafnium silicates and zirconium silicates co-existed nanocrystal memory is shown in Fig. 3-11. The measured condition is - program: Vg = 15V, Vd = 10V, 1 msec; erase: Vg = -10V, Vd = 10V, 10 msec. As the Figure shows, the memory window is about 3V after 10^5 P/E cycles. No significant window narrowing is observed. This finding suggests the simple sol-gel process can be incorporated into the SONOS-like memory fabrication.

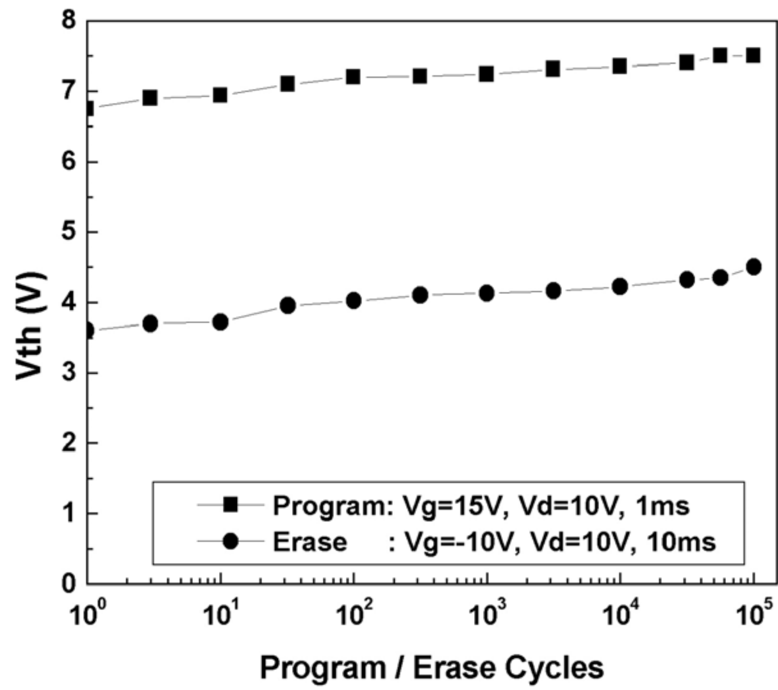
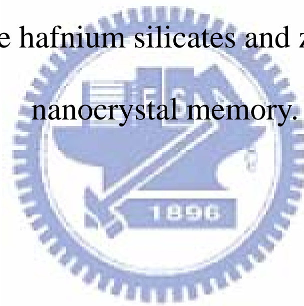


Fig. 3-11 : Endurance of the hafnium silicates and zirconium silicates co-existed nanocrystal memory.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3-3.2 Physical Characteristics

The high-resolution transmission electron microscopy (HRTEM) image in Fig. 3-12 depicts the nanocrystal on SiO_2 film after annealing at 900°C for 60s. The average nanocrystal size is around 5nm. We observed two kinds of different colors nanocrystals in the TEM image. To analyze the chemical bonding of the nanocrystals, additional x-ray photoelectron spectroscopy (XPS) analysis was done.

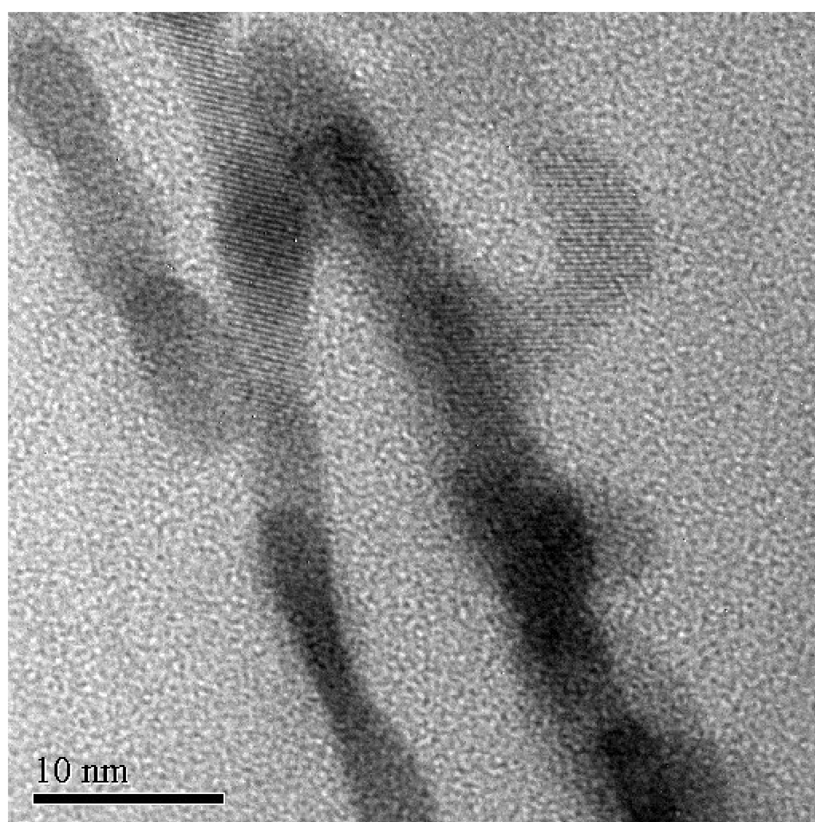


Fig. 3-12: TEM image of hafnium silicate and zirconium silicate nanocrystal.

Figure 3-13 shows the XPS data of the (a) Hf 4f and (b) Zr 3d features for as-dep and after 900 °C annealing. The literature [48] suggests the Hf 4f peaks for the hafnium silicate film. Specifically, as the film is heated, the peak shift from 17.4 eV (as-dep) to 18.0 eV (900 °C

annealing) and the enlargement of peak height are observed. Cho et al. [49] reports the peak shift to higher binding energy for $HfSi_xO_y$ and can be caused by the formation of Hf-O bonding in the vicinity of Si. Similar data were obtained for zirconium silicate formation in Zr 3d feature. Wilk and Kirsch also observe a similar behavior [50-51], and they attribute to the increased hafnium and zirconium silicate formation. Therefore, we suppose that the darker nanocrystals in Fig. 3-12 are hafnium silicate nanocrystals and the light color are zirconium silicate nanocrystals due to their XPS features and different atomic weights.

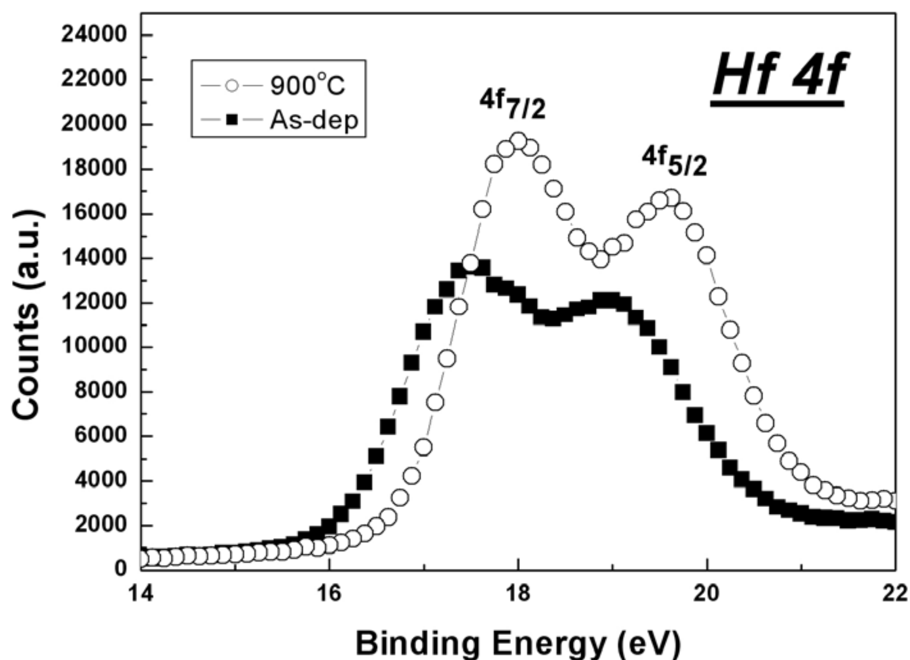


Fig. 3-13(a): XPS curve of hafnium silicate.

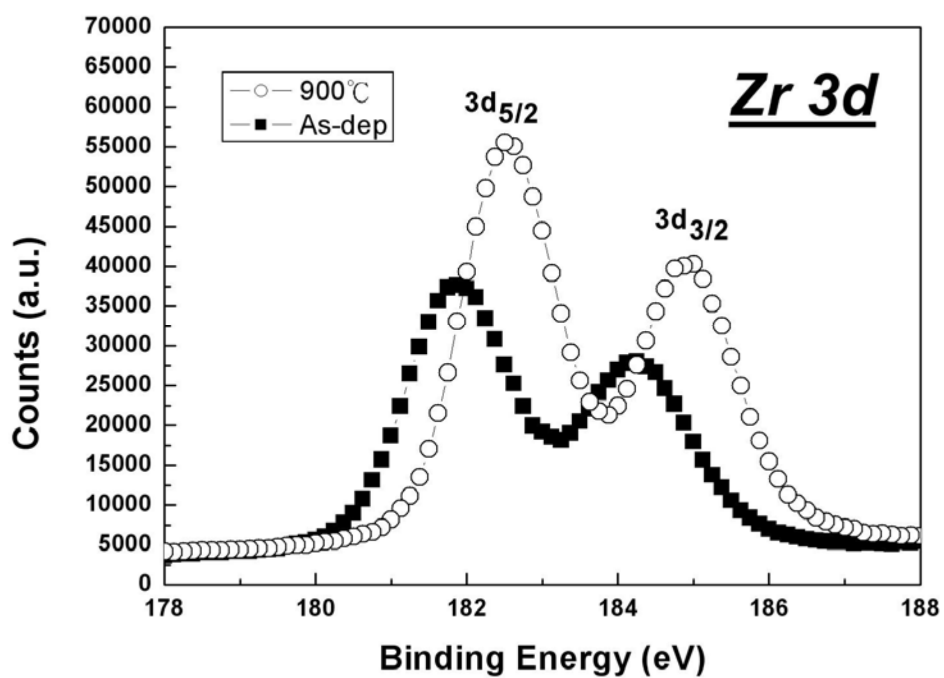
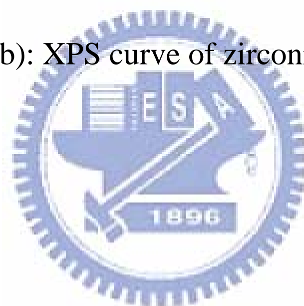


Fig. 3-13(b): XPS curve of zirconium silicate.



3-4 Summary

In this chapter, we use sol-gel spin coating method to fabricate co-existed hafnium silicates and zirconium silicates nanocrystal memory. The XPS analysis indicates the formation of hafnium silicate and zirconium silicate after $900^{o}C$ 1min RTA. From the TEM image, we also demonstrate the crystal size of co-existed hafnium silicate nanocrystal and zirconium silicate nanocrystal is near 5nm. We have verified the device performance with the P/E speed, charge retention, and endurance measurement. The quality of the co-existed hafnium silicate and zirconium silicate nanocrystals formed by the sol-gel spin coating method and RTA treatment exhibits better properties in terms of larger Vth shift due to more trapping site existed, long charge retention time (5% loss at 10^4sec), good endurance (up to 10^5 P/E cycles) with no memory window narrowing due to SiO_2 surrounded the nanocrystal increased the tunneling oxide thickness.