國 立 交 通 大 學

電信工程學系

博 士 論 文

金氧半導體元件雜訊對射頻積體電路的影響

Impacts of Noise on the CMOS RF Integrated Circuits

研 究 生：許孟庭

指導教授：高曜煌

中華民國 九十三 年 九 月

金氧半導體元件雜訊對射頻積體電路的影響

Impacts of Noise on the CMOS RF Integrated Circuits

研究生：許孟庭　　Student: Meng-Ting Hsu

指導教授：高曜煌 博士　　Advisor: Dr. Yao-Huang Kao

國立交通大學

電信工程學系

博士論文

A Dissertation

Submitted to the Institute of Communication

College of

National Chiao Tung University

In Partial Fulfillment of the Requirements

For the Degree of

Doctor of Philosophy

In

Communication Engineering

June 2004

Hsinchu, Taiwan, Republic of China

中華民國 九十三 年 九 月

金氧半導體元件雜訊對射頻積體電路的影響

研究生：許孟庭　　指導教授：高曜煌 博士

國立交通大學電信工程學系博士班

摘要

本論文的目標在研究元件的雜訊在射頻電路設計中的角色。對低雜訊放大器而言，描述在不同的頻率範圍下，具有源極迴授式之低雜訊放大器技術已被印證其可行性。經由兩種不同的方法了解雜訊與輸入阻抗之變化情形，首先經由雙埠網路觀察最小雜訊指數和等效輸入電阻隨源極電感而產生的變化。其次，經由等效模型萃取出影響最小雜訊指數和等效輸入電阻之主要元素，在 C 頻段下使用此技術，可同時獲得具有負 23 分貝的優良輸入反射損失和 1 分貝的最小雜訊指數。封裝元件應用在此源極電感迴授式之頻率限制亦同時著墨。其次，使用聯電 0.5um 金氧半導體技術製作積體化低雜訊放大器，在偏壓 3 伏特和操作頻率 2.4GHz 下，信號增益 12.5dB ，雜訊指數 5.6dB 和 40mW 的消耗功率。由於閘極電阻率較高，使得雜訊指數及訊號增益量明顯受到影響，因此在設計射頻積體電路晶片製作上需考慮低閘極電阻率之製程參數，提升電路操作性能。

另外，使用台積電 0.35um 金氧半導體技術製作積體化壓控振盪

器亦被提出，他具有 2GHz 的振盪頻率，在 3 伏特偏壓下功率消耗為 23.58mW 且有 9.1%頻寬調制。在晶片製作中，最佳化電感佈局設計不僅提升品質因素，更降低了相位雜訊。文中亦提出預測相位雜訊的計算法，經由量測結果得到在 600KHz 的偏移頻率下，其相位雜訊為 -115.5 dBc/Hz。依觀察，預測數值與量測數據相當吻合。

Impacts of Noise on the CMOS RF Integrated Circuits

Student: Meng-Ting Hsu Advisor: Dr. Yao-Huang Kao

Institute of Communication
National Chiao Tung University

Abtract

The goal of this thesis is to study the noise phenomenon and property of the device. And how noise applied to design the RF circuits. First, the noise figure to LNA is presented.

The feasibility of the technique of source inductive feedback (SIF) for low noise amplifiers (LNA) design is examined in different frequency domains. The variations in noise and input impedance are obtained by two different approaches. One is from a noisy two-port analysis to observe the variation of $F_{\min}$ and R_n, and the other is from equivalent circuit model to trace out the key element. Using ISF, the results with both good input return loss about -23dB and low minimum noise figure about 1dB at C band are demonstrated. The frequency limitations of the SIF technique in package devices are also addressed.Another circuit of 2.4GHz CMOS LNA was fabricated by the process of UMC 0.5um DPDM technology. It has 12.5dB gain and 5.6dB noise figure under 3V bias. Owing to the gate sheet resistance $30\Omega/\square$ is so high that it affects the noise figure and signal gain. From the noise analysis of gate effect to LNA, it shows very match the noise level by taking gate resistance of the device into account. In words, choosing lower sheet resistance of poly gate is necessary to RF circuits.

Secondly, the phase noise to VCO with 2GHz operating frequency is proposed. The fully integrated LC voltage controlled oscillator by TSMC 0.35um CMOS technology is demonstrated. It has 2GHz oscillation frequency, 23.58mW power consumption under 3V biased and 9.1% frequency tuning. The layout optimization

method of inductor to increase quality factor and also to reduce phase noise is used. A general method is proposed which is capable of making an effective prediction of F, device excess noise number, and acquiring to phase noise of oscillators accurately. From this proposed method, the low phase noise by calculation is attained. The phase noise of measured value which shows good match with calculating data is about -115.5dBc/Hz at offset frequency 600KHz.

誌謝

感謝上帝讓我有機會進入國立交通大學電信研究所接受微波電路和射頻積體電路相關領域的訓練與磨練。更高興的是能夠受教於高曜煌 教授的門下，一窺高頻電路和積體電路設計的堂奧。在七年的寒暑交替中，品嚐到知識累積的可貴和價值，更學習了挑戰困難及解決問題的正確態度與方法。雖然在整個學習過程中倍感艱辛、五味雜陳，但每次困難得以解決，無形中能力隨之提昇，心中亦充滿著極大的喜樂。另外也要特別感謝雲林科技大學電子系 周榮泉 教授常常給予鼓勵與關懷，並於投稿文件中的指導與建議。

在這段漫長的學習過程中，光纖通訊和高頻電路實驗室給我寬廣的成長空間，令人難忘，尤其是伴我奮鬥了好幾屆的學弟，再次重點代表題名道謝，李柏榮、謝義濱、林哲煜、吳莊雄、李佳穎、莊朝喜、游秋榮、林炯宏、柯勝民、許民傑、吳丕安、謝東憲、曾渾洸、曾耀緯…等多位學弟彼此鼓勵和幫助，使得實驗室在這幾年間於射頻積體電路領域中打響了知名度，這是本實驗室值得慶賀之處，本人能躬逢其盛，亦倍感光榮。

我還要感謝國家晶片設計製作中心(CIC)提供晶片設計及製作的優良環境，使得論文中積體電路設計之實驗應證得以順利完成。同時亦感謝工研院和奈米元件實驗室在量測儀器上的支援，使得量測數據的蒐集和整理能快速完成。此外，亦要感謝雲科大的專題生劉俊宏、蔡嘉偉、金廷嶽、鄒宜勳和方浩宇在排版及校稿上之協助，使得博士論文能夠順利完稿。

最後，我要感謝父母和家人付出的關懷和鼓勵，尤其岳父母在此期間幫忙帶小孩，使我更專心於學習而無牽掛，相信沒有這些人的幫忙與協助，就沒有今日的我。在此衷心地感謝伴我渡過七年寒暑的人、事、物。

許孟庭

書於 風城交大

九十三年九月初秋

Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Motivation

In the early 1980s a marketing firm hired by AT&T to survey the potential U.S. market for its newly inaugurated cellular phone service arrived at an estimate of less than 900,000 users by the year 2000. Like many predictions of technological progress, this one turned out to be off by a wide margin—in 1998 the number of cellular subscribers in the United States was over 60million (already an error of more than 6000 percent). It is now estimate that half of all business and personal communications will be wireless by the year 2010 [1]. Rapid growth is also occurring with other wireless systems, such as Direct Broadcast Satellite (DBS) television service, Wireless Local Area Networks (WLANs), paging systems, Global Positioning Satellite (GPS) service, and Radio Frequency Identification (RFID) systems. These systems promise to provide, for the first time in history, worldwide connectivity for voice, video, and data communications. The successes of wireless technology to date, and the technological challenges of future wireless systems, make this an exciting and rewarding field in which to work. In this section we give a brief introduction to some of the major wireless systems in use today. These include wireless cellular and PCS telephone systems, wireless data networks. Wireless systems can be grouped according to their operating frequency. Table 1.1 lists the operating frequencies of some of the most common wireless systems.

Cellular telephone systems were proposed in the 1970s in response to the problem of providing mobile radio service to a large number of users in urban areas. Early mobile radio systems could handle only a very limited number of users due to inefficient use of the radio spectrum and interference between users. In 1976, for example, the entire mobile phone system in New York City could support only 543 users [1]. The cellular radio concept introduced by Bell Laboratories solved this problem by dividing a geographical area into non-overlapping hexagonal cells, where each cell has its own transmitter and receiver (*base station*) to communicate with the mobile users operating in that cell. Each cell site may allow as many as several hundred users to simultaneously communicate with other mobile users, or through the land-based telephone system.

The first cellular telephone system to offer commercial service was built by the Nippon Telephone and Telegraph company (NTT), and became operational in Japan

TABLE 1.1 Wireless System Frequencies

Wireless System	Operating Frequency
Advanced Mobile Phone Service (AMPS)	T: 824-849 MHz R: 869-894 MHz
Global System Mobile (European GSM)	T:800-915 MHz R:925-960 MHz
Personal Communications Service (PCS)	T:1710-1785 MHz R:1805-1880 MHz
US Paging	931-932 MHz
Global Positioning Satellite (GPS)	L1:1575.42 MHz L2:1227.60 MHz
Direct Broadcast Satellite (DBS)	11.7-12.5 MHz
Wireless Local Area Networks (WLANs)	902-928 MHz 2.400-2.484 GHZ 5.725-5.850 GHz
Local Multipoint Distribution Service (LMDS)	28GHz
US Industrial, Medical, and Scientific bands (ISM)	902-928 MHz 2.400-2.484 GHz 5.725-5.850 GHZ

T/R = mobile unit transmit/receive frequency

in 1979. This was followed by the Nordic Mobile Telephone (NMT) system in Europe, which began operation in 1981. The first cellular telephone system in the United States was the Advanced Mobile Phone System (AMPS), deployed by AT&T in 1983. All of these systems use analog FM modulation and divide their allocated frequency bands into several hundred channels, each of which can support an individual telephone conversation. These early systems grew slowly at first, because of the initial costs of developing an infrastructure of base stations and the initial expense of handsets, but by the 1990s growth became phenomenal.

In 1998 88% of all cellular telephones in the United States used the analog AMPS system, but newer digital standards have been growing in popularity and will

soon replace the AMPS system. These systems are generally referred to as Second Generation Cellular, or Personal Communication Systems (PCS). Third generation PCS systems, which may include capabilities for email and Internet access, are in the planning stages.

Because of the rapidly growing consumer demand for wireless telephone device, as well as advances in wireless technology, several second generation standards have been proposed for improved service in the United States, Europe, and Japan. These PCS standards all employ digital modulation methods and provide better quality service and more efficient use of the radio spectrum than analog systems. Digital systems also provide more security, preventing eavesdropping through the possible use of encryption.

PCS system in United States use either the IS-136 time division multiple access (TDMA) standard, the IS-95 code division multiple access (CDMA) standard, or the European Global System Mobile (GSM) system [1], [2], [3]. Many of the new PCS systems have been deployed using the same frequency bands as the AMPS system. This approach takes advantage of existing infrastructure, and facilitates the use of *dual-mode handsets* that can operate on both the older AMPS system as well as one of the newer digital PCS systems. Additional spectrum has also been allocated by the Federal Communications Commission (FCC) around 1.8GHz, and some of the newer PCS systems use this frequency band.

Outside the United States, the Global System Mobile (GSM) TDMA system is the most widespread, being used in over 100 countries [1]. The uniformity of a single wireless telephone standard throughout Europe and much of Asia allows travelers to use a single handset throughout these regions. In contrast, the different PCS systems in the United States are incompatible. Table 1.2 lists the major cellular and PCS telephone systems that have been deployed throughout the world [1], [3].

It is interesting to compare how the development of first and second generation cellular services has differed in the United States and Europe [1]. The first U.S. cellular system, AMPS, provided a single standard allowing every cellular user in the United States and Canada to communicate within range of a base station. In the Europe of the early 1980s, however, individual countries developed their own analog cellular standards with different frequency bands and modulation methods, so that there were at least four incompatible systems in use (see Table 1.2). These situations were reversed for second generation digital systems. The organization of European countries under the European Union in the 1980s led to the establishment of GSM as a single digital PCS standard, which is now used by over 100 countries in Europe and elsewhere. In the United States, however, government policies relating to the allocation of radio spectrum, as well as the structure of the telecommunications

TABLE 1.2 Major Worldwide Cellular and PCS Telephone Systems

Standard	Country	Year of Introduction	Type	Frequency Bnad (MHz)	Modulation	Channel Bandwidth
NTT	Japan	1979	cellular	860-940	FM	25 KHz
NMT-450	Europe	1981	cellular	453-468	FM	25 KHz
AMPS	United States	1983	cellular	824-894	FM	30 KHz
E-TACS	Europe	1985	cellular	872-950	FM	25 KHz
C-450	Germany	1985	cellular	450-466	FM	20 KHz
NMT-900	Europe	1986	cellular	890-960	FM	12.5 KHz
JTACS	Japan	1988	cellular	860-925	FM	25 KHz
GSM	Europe	1990	PCS	890-960	GMSK	200 KHz
IS-54	United States	1991	PCS	824-894	DQPSK	30 KHz
NAMPS	United States	1992	Cellular	824-894	FM	10 KHz
IS-95	United States	1993	PCS	824-894	QPSK	1.25 KHz
PDC	Japan	1993	Cellular	810-1513	DQPSK	25 KHz
NTACS	Japan	1993	Cellular	843-922	FM	12.5 KHz

industry and the competitive nature of R&D in the United States, has allowed the technological and economic trade-offs between CDMA, TDMA, and GSM PCS systems to be decided in the marketplace. Meanwhile, wireless telephone consumers in the United States are left to choose between an out-of-date analog system and a variety of incompatible digital systems.

Wireless local area networks (WLANs) provide connections between computers over short distances. Typical indoor applications may be in hospitals, office buildings, and factories, where coverage distances are usually less than a few hundred feet. Outdoors, in the absence of obstructions and with the use of high gain antennas, ranges up to a few miles can be obtained. Wireless networks are especially useful when it is impossible or prohibitively expensive to place wiring in or between buildings, or when only temporary access is needed between computers. Mobile computers users, of course, can only be connected to a computer network by a wireless link.

In spite of their attractiveness, market penetration of WLAN products has been

slow, probably due to a combination of factors that include relatively high costs, relatively slow data rates, and poor immunity to fading and interference. In 1996 the market for WLANs was about $200M, which is a negligible fraction of the several billion dollar cellular telephone industry. It is expected, however, that market growth for WLANs will soon increase substantially. A major new WLAN initiative is the *Bluetooth* standard, where very small and inexpensive RF transceivers will be used to link a wide variety of digital systems over relatively short distances. Possible Bluetooth applications include wirelessly networking printers, scanners, cell phones, notebook and desktop computers, personal digital assistants (PDAs), and even household appliances. Current Bluetooth systems operate in the ISM band at 2.4GHz, and offer data rates up to 1Mbps. Market projections for Bluetooth devices are in the range of several hundred million units per year.

Currently most commercial WLAN products in the United States operate in the *Industria*l, *Scientific*, and *Medical* (ISM) frequency bands, and use either frequency-hopping or direct-sequence spread spectrum techniques in accordance with IEEE standard 802.11. Maximum bit rates range from 1 to 2 Mbps, which are much slower than the data rates that can be achieved with wired Ethernet lines. WLANs almost universally use Internet protocols (TCP/IP) for communication between computers. In Europe, the HIPERLAN standard provides for WLAN operation with data rates up to 20Mbps.

1.2 Review of Receiver Design

The receiver is often the most critical component of a wireless system, having the overall purpose of reliably recovering the desired signal from a wide spectrum of transmitting sources, interference, and noise. Here we review some of the fundamental principles of radio receiver design, beginning with the evolution of receivers to provide progressively improved performance.

Receiver design has evolved from the simple circuits used in the early days of radio in order to provide improved performance, ultimately allowing more efficient use of the radio spectrum for more users, communication over larger distances, and the use of lower transmit powers [1].

Receiver Requirements

The well-designed radio receiver must provide the following requirements:

- *High gain* (~100dB) to restore the low power of the received signal to a level near its original baseband value.
- Selectivity, in order to receive the desired signal while rejecting adjacent channels, image frequencies, and interference.

- *Down-conversion* from the received RF frequency to an IF frequency for processing.
- *Detection* of the received analog or digital information.
- *Isolation* from the transmitter to avoid saturation of receiver.

Because the typical signal power level from the receive antenna may be as low as -100 to -120 dBm, the receiver may be required to provide gain as high as 100 to 120 dB. This much gain should be spread over the RF, IF, and baseband stages to avoid instabilities and possible oscillation; it is generally good practice to avoid more than about 50-60dB of gain at any one frequency band. The fact that amplifier cost generally increases with frequency is a further reason to spread gain over different frequency stages.

By far the most popular type of receiver used today is the *superheterodyne* circuit, shown Figure 1.1. The block diagram is similar to the direct conversion receiver, but the IF frequency is now nonzero, and generally selected to be between the RF frequency and baseband. A midrange IF allows the use of sharper cutoff filters for improved selectivity, and higher IF gain through the use of an IF amplifier. Tuning is conveniently accomplished by varying the frequency of the local oscillator so that the IF frequency remains constant. The superheterodyne receiver represents the culmination of over 50 years of receiver development, and is used in the majority of broadcast radios and televisions, radar systems, cellular telephone systems, and data communications systems.

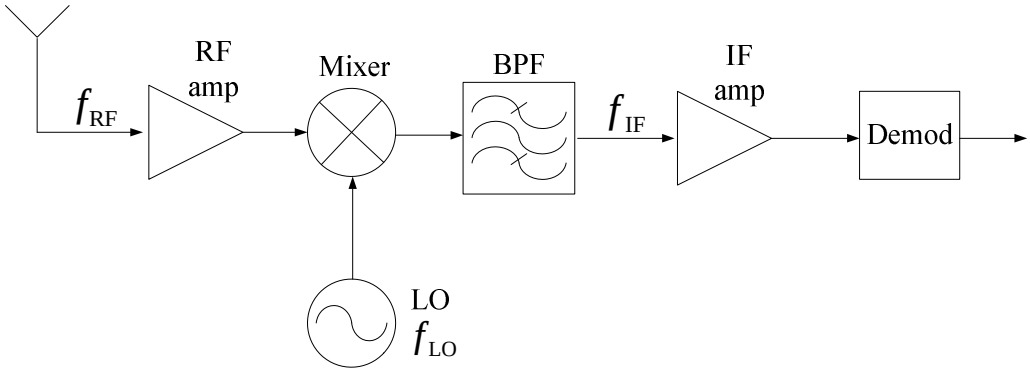

Figure 1.1 Block diagram of a single-conversion superheterodyne receiver

At microwave and millimeter wave frequencies it is often necessary to use two stages of down conversion to avoid problems due to LO stability. The *dual-conversion* superheterodyne receiver of Figure 1.2 employs two local oscillators and mixers to achieve down-conversion to baseband with two IF frequencies.

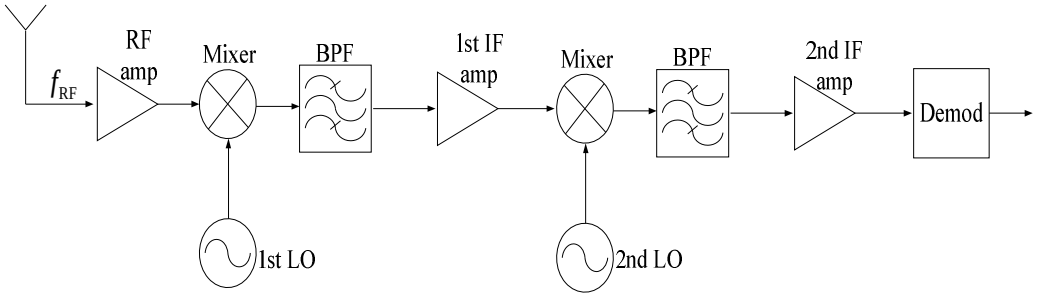

Figure 1.2 Block diagram of a double-conversion superheterodyne receiver

Figure 1.3 shows a graphical view of the input and output dynamic ranges of a typical receiver. The dynamic range of the input signal from the antenna is on the order of 100dB, while the output dynamic range of the receivers is typically about 60dB. The power gain through the receiver must therefore vary as a function of the input signal strength in order to fit the input signal range into the baseband processing range, for a wide range of input signal levels. A receiver gain on the order 60dB may be required for low level signals, while a gain of only 20-30dB may be required for high-level signals. This variable-gain function is accomplished with an *automatic gain control* (AGC) circuit. AGC is most often implemented at the IF stage, but some receivers may use AGC at the RF stage as well. Virtually all modern communications, broadcast radio, and television receivers use AGC to control signal levels.

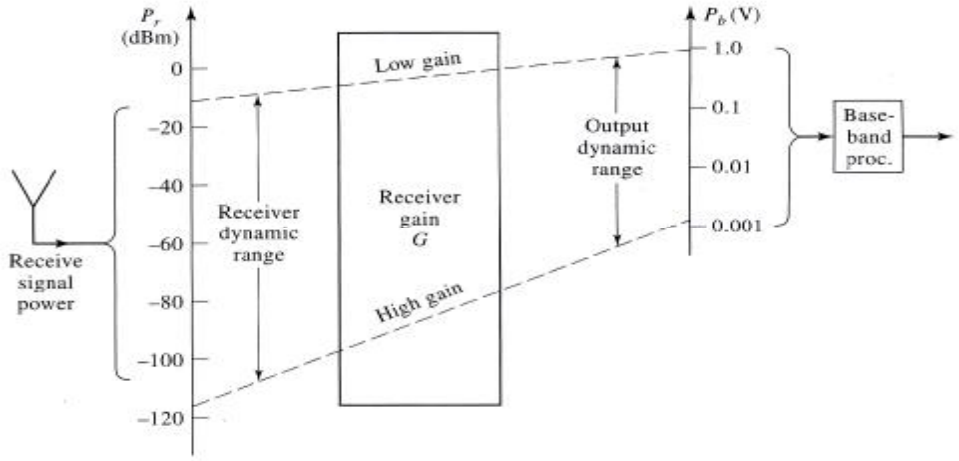

Figure 1.3 Diagram illustrating the change in power levels between the input and output of a typical receiver.

The power levels of an amplifier that exceed the 1 dB compression point P_1 will cause harmonic distortion, and power levels in excess of the third-order intercept point P_3 will cause intermodulation distortion. Thus it is important to track power levels through the stages of the receiver to ensure that P_1 and P_3 are not exceeded. This can be conveniently done with a graph of the form shown in Figure 1.4. This diagram tracks the power level of small and large input signals, analog with the noise level (noise power or noise figure may be plotted), through the front-end stages of the receiver. The compression and third-order intercept points of the amplifiers and mixers can be plotted on the graph, making it easy to see if these limits are exceeded, and to determine the effect of changing component specifications or position in the receiver circuit.

Oscillators are required in wireless receivers and transmitters to provide frequency conversion, and to provide sinusoidal sources for modulation. Typical transmitters and receivers may each use as many as 4-6 oscillators, at frequencies ranging from several kilohertz to many gigahertz. Often these sources must be tunable over a set frequency range, and must provide very accurate output frequencies (often to within a few parts per million).

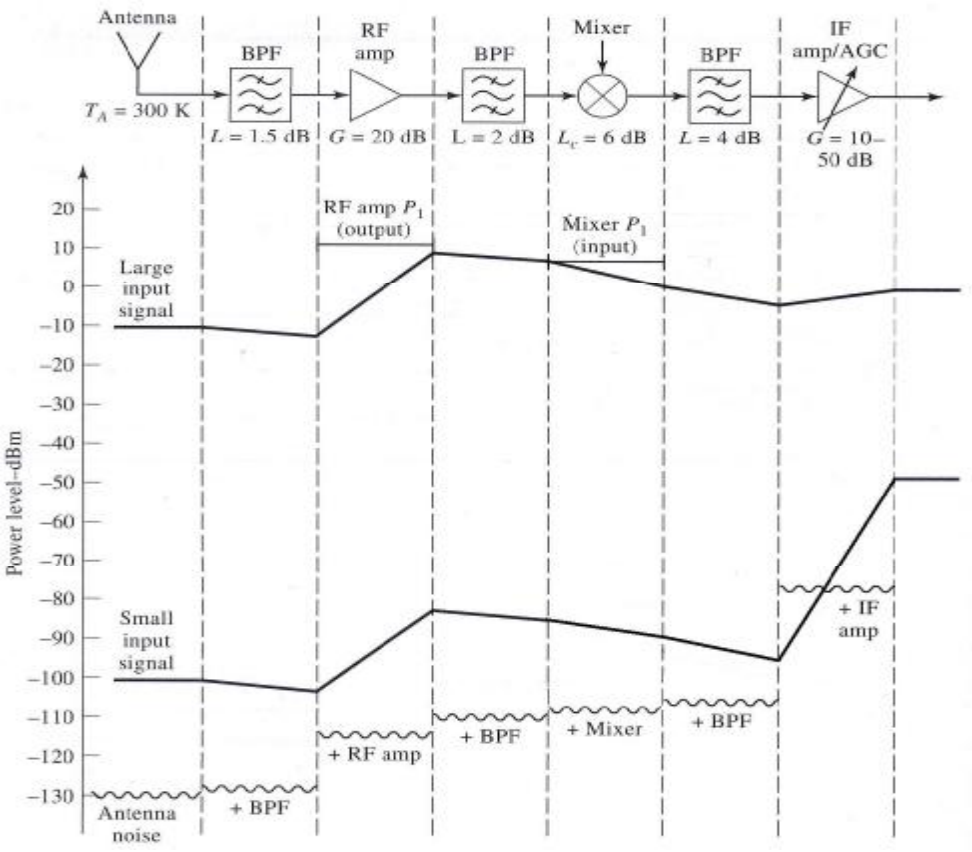

Figure 1.4 Diagram of power and noise levels at consecutive stages of receiver

The simplest oscillator uses a transistor with an LC network to control the frequency of oscillation. Frequency can be tuned by adjusting the values of the LC network, perhaps electronically with a varactor diode. Such oscillators are simple and inexpensive, but suffer from the fact that the output frequency is very susceptible to variations in supply voltage, changing load impedances, and temperature variations. Better frequency control can be obtained by using a quartz crystal in place of the LC resonator. A *crystal-controlled oscillator* (XCO) can provide a very accurate output frequency, especially if the crystal is in a temperature controlled environment. Crystal oscillators, however, cannot easily be tuned in frequency. A solution to this problem is provided by the *phase-locked loop* (PLL), which uses a feedback control circuit and an accurate reference source (usually a crystal controlled oscillator) to provide an output that is tunable with high accuracy.

Phase-locked loops and other circuits that provide accurate and tunable frequency outputs are called *frequency synthesizers*. Virtually all modern wireless systems rely on frequency synthesizer circuits for the key stages of frequency conversion. Important parameters that characterize frequency synthesizers are tuning range, frequency switching time, frequency resolution, cost, and power consumption. Another very important parameter is the noise associated with the output spectrum of the synthesizer, in particular the *phase noise*. Phase noise is a measure of the sharpness of the frequency domain spectrum of an oscillator, and is critical for many modern wireless systems.

1.3 Organization of This Thesis

It is the aim of this thesis to study the role of noise in the low noise amplifier (LNA) design and low phase noise VCO design. The noise figure plays important key for low noise amplifier circuit design. And the phase noise is another crucial property for oscillator design.

In chapter2, the noise theory of the circuit is introduced. The content of the noise properties including the noise definition, noise spectrum, noise representation of the passive and active element will be described. The noise source property of the two port network is also mentioned. Especially, the characterization of noise figure on LNA and phase noise on VCO also included in this chapter.

In chapter3, the design procedure of low noise amplifier is described first. Secondly, the structure of circuit topology of LNA with inductor feedback is used. Finally, the comparison of the simulation and measurement data is well matched for the performance with 4GHz low microwave band. Another circuit with 2.4GHz CMOS LNA was fabricated by the process of UMC 0.5um DPDM technology is also presented. We focus on the noise analysis of the circuit.

In chapter4, the basic design of microwave oscillator is described first. According to the concept of microwave oscillator design, the circuit structure with Complementary Cross-Coupled pair of voltage controlled oscillator is used. Secondly, the design methodology of VCO is mentioned. We proposed a new calculation method of the phase noise of VCO. The implementation of the VCO with the help of Chip Implementation Circuit (CIC) and Taiwan Semiconductor Manufacture Company (TSMC). The 0.35um 1P4M CMOS standard processes is employed. Finally, the proposed method of phase noise calculation is also compared to that of others.

In chapter5, the short conclusion of our work and the view of the future work.

Chapter 2

General Noise Theory

2.1 Introduction to Noise Concept

Noise is a random process. This statement means the value of noise cannot be predicted ay any time even if the past values are known. Compare the output of a sinewave generator with that of a microphone picking up the sound of water flow in a river (Fig. 2.1). While the value of $x_1(t)$ at $t = t_1$ can be predicted from the observed waveform, the value of $x_2(t)$ at $t = t_2$ cannot. This is the principal difference between deterministic and random phenomena [4].

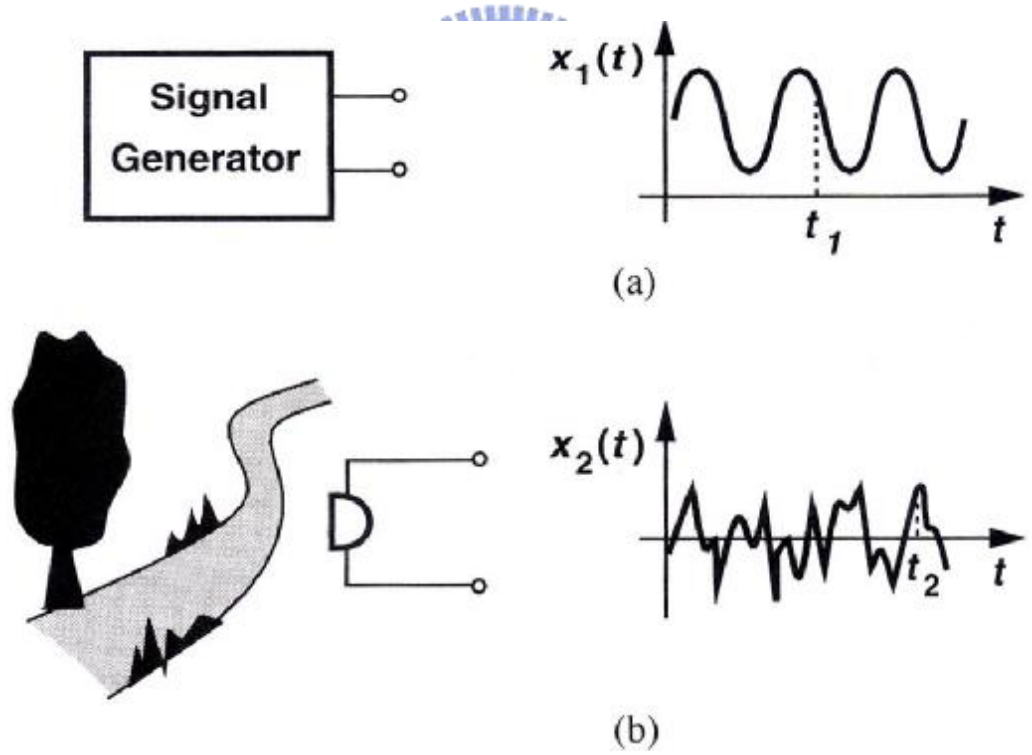

Figure 2.1 Output of a generator and the sound of a river

If the instantaneous value of noise in the time domain cannot be predicted, how can we incorporate noise in circuit analysis? This is accomplished by observing the noise for a long time and using the measured results to construct a "statistical model"

for the noise. While the instantaneous *amplitude* of noise cannot be predicted, a statistical model provides knowledge about some other important properties of the noise that prove useful and adequate in circuit analysis.

Which properties of noise can be predicted? In many cases, the average power of noise is predictable. The concept of average power proves essential in our analysis and must be defined carefully. Recall from basic circuit theory that the average power delivered by a periodic voltage $v(t)$ to a load resistance R_L is given by

$$P_{av} = \frac{1}{T}\int_{-T/2}^{+T/2}\frac{v^2(t)}{R_L}dt \tag{2.1}$$

where T denotes the period. This quantity can be visualized as the average heat produced in R_L by $v(t)$.

However, since the signals are not periodic, the measurement must be carried out over a long time:

$$P_{av} = \lim_{T\to\infty}\int_{-T/2}^{+T/2}\frac{x^2(t)}{R_L}dt \tag{2.2}$$

where $x(t)$ is a voltage quantity. Figure 2.2 illustrates the operation $x_2(t)$; each signal is squared, the area under the resulting wave form is calculated for a long time T, and the average power is obtained by normalizing the area to T.

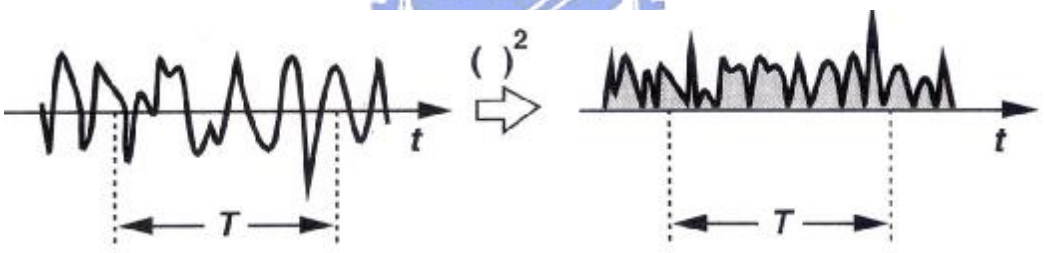

Figure 2.2 Average noise power

To simplify calculations, we write the definition of P_{av} as

$$P_{av} = \lim_{T\to\infty}\frac{1}{T}\int_{-T/2}^{+T/2}x^2(t)dt \tag{2.3}$$

where P_{av} is expressed in V^2 rather than W. The idea is that if we know P_{av} form (2.3), then the actual power delivered to a load R_L can be readily calculated as P_{av}/R_L. In analogy with deterministic signals, we can also define a root-mean-square (rms) voltage for noise as $\sqrt{P_{av}}$ where P_{av} is given by (2.3).

The concept of average power becomes more versatile if defined with regard to *frequency content* of noise. The noise made by a group of men contains weaker

high-frequency components than that made by a group of women, a difference observable from the "spectrum" of each type of noise. Also called the "power spectral density" (PSD), the spectrum shows how much power the signal carriers at each frequency. More specifically, the PSD, $S_x(f)$, of a noise waveform $x(t)$ is defined as the average power carried by $x(t)$ in a one-hertz bandwidth around f. That is , as illustrated in Fig. 2.3(a), we apply $x(t)$ to a bandpass filter with center frequency f_1 and 1-Hz bandwidth, square the output, and calculate the average over a long time to obtain $S_x(f_1)$. Repeating the procedure with bandpass filters having different center frequencies, we arrive at the overall shape of $S_x(f)$ [Fig. 2.3(b)]. While it is possible that the PSD of a random process is random itself, most of the noise sources of interest to us exhibit a predictable spectrum.

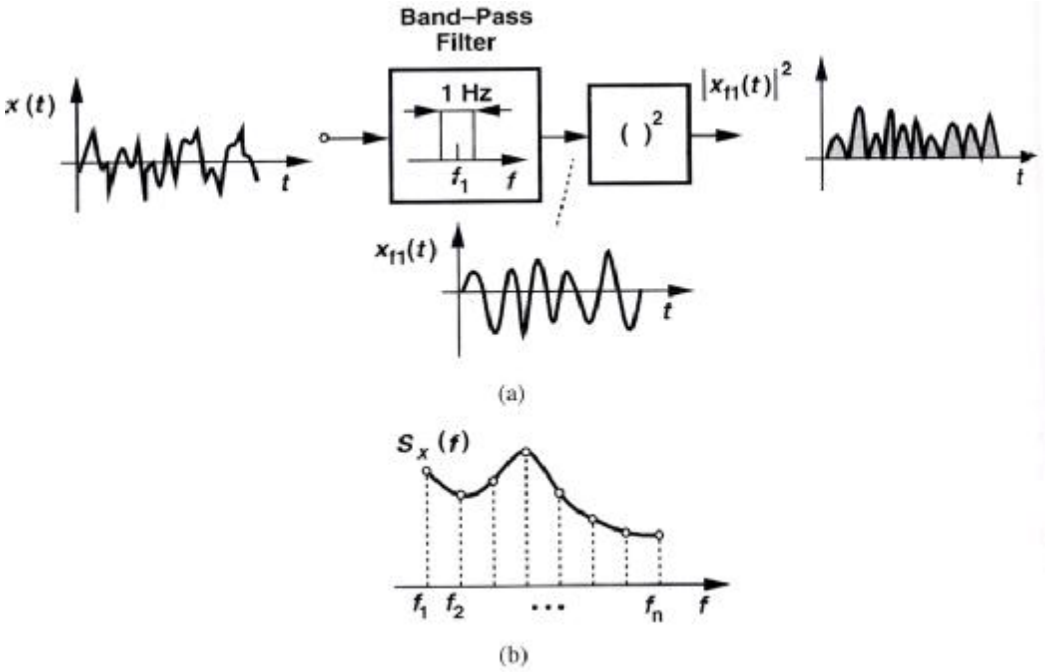

Figure 2.3 Calculation of noise spectrum

It is customary to eliminate R_L from $S_x(f)$. Thus, since each value of the plot in Fig. 2.3(b) is measured for a 1-Hz bandwidth, $S_x(f)$ is expressed in V^2/Hz rather than W/Hz. It is also common to take the square root of $S_x(f)$, expressing the result in $V/\sqrt{Hz}$.

2.2 Type of Noise

Analog signals processed by integrated circuit are corrupted by two different type of noise: device electronic noise and environmental noise. We focus on device electronic noise here. There are three main fundamental noise mechanisms—thermal

noise, shot noise and flicker noise.

2.2.1 Thermal Noise

Thermal noise is due to the thermal excitation of charge carriers in the conductor. It is also dependent on bias conditions. The random motion of electrons in a conductor introduces fluctuation is the voltage measured across the conductor even if the average current is zero. Thus, the spectrum of thermal noise is proportional to the absolute temperature.

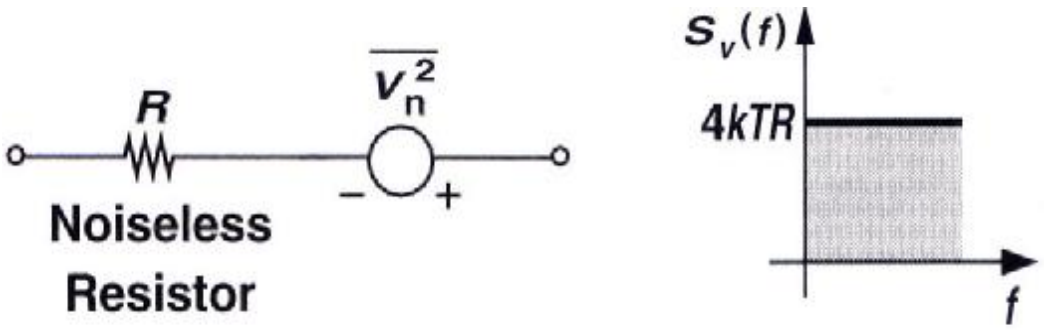

Figure 2.4 Thermal noise of a resistor

As shown Fig. 2.4, the thermal noise of a resistor R can be modeled by a series voltage source, with the one-side spectral density

$$S_v(f) = 4kTR,\ f \geq 0 \tag{2.4}$$

where k = 1.38×10^{-23} J/K is the Boltzmann constant. Note that $S_v(f)$ is expressed in V^2/Hz. Thus, we write $\overline{V_n^2} = 4kTR$, where the overline indicates averaging. We may even say the noise "voltage" is give by $4kTR$ even though this quantity is in fact the noise voltage squared.

It should be mentioned here that thermal noise is also referred to as Johnson or Nyquist noise since it was first observed by J. B. Johnson [Johnson, 1928] and analyzed using the second law of thermodynamics by H. Nyquist [Nyquist, 1928].

2.2.2 Shot Noise

Shot noise was first studied by W. Schottky using vacuum-tube diodes [Schottky, 1918], but shot noise also occurs in **pn** junctions. This noise occurs because the dc bias current is not continuous and smooth but instead is a result of pulses of current caused by the individual flow of carriers. As such, shot noise is dependent on the dc bias current. It can also be modeled as a white noise source. Shot noise is also typically larger than thermal noise and is sometimes used to create white noise generators[5].

2.2.3 Flicker Noise

Flicker noise is the least understood of the three noise phenomena. It is found in all active devices as well as in carbon resistors, but it occurs only when a dc current is flowing. Flicker noise usually arises due to traps in the semiconductor, where carriers that would normally constitute dc current flow are held for some time period and then released. Flicker noise is also commonly referred to as 1/f noise since it is well modeled as having a $1/f^{\alpha}$ spectral density, where α is between 0.8 and 1.3. Although both bipolar and MOSFET transistors have flicker noise, it is a significant noise source in MOS transistors, whereas it can often be ignored in bipolar transistor.

The flicker noise of MOSFET is more easily modeled as a voltage source in series with the gate, and roughly given by

$$\overline{V_n^2} = \frac{K}{C_{ox}WL} \cdot \frac{1}{f} \tag{2.5}$$

where K is a process-dependent constant on the order of $10^{-25}V^2F$. Note that our notation assumes a bandwidth of 1Hz. Interestingly, as shown in Fig. 2.5, the noise spectral density is inversely proportional to the frequency. For example, the trap-and-release phenomenon associated with the dangling bonds occurs at low frequencies more often. For this reason, flicker noise is also called 1/*f* noise. Note that (2.5) does not depend on the bias current or the temperature. This is only an approximation and in reality, the flicker noise equation is somewhat more complex [6].

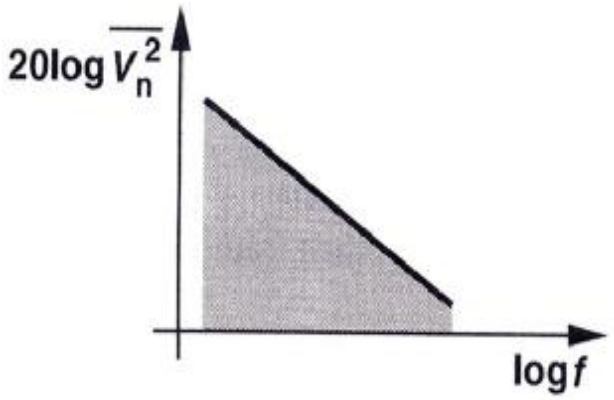

Figure 2.5 Flicker noise spectrum

The inverse dependence of (2.5) on *WL* suggests that to decrease 1/*f* noise, the device *area* must be increased. It is therefore not surprising to see devices having areas of several thousand square microns in low-noise applications. It is also believed that PMOS devices exhibit less 1/*f* noise than NMOS transistors because the former

carry the holes in a "buried channel", i.e., at some distance from the oxide-silicon interface. Nonetheless, this difference between PMOS and NMOS transistors is not consistently observed [6].

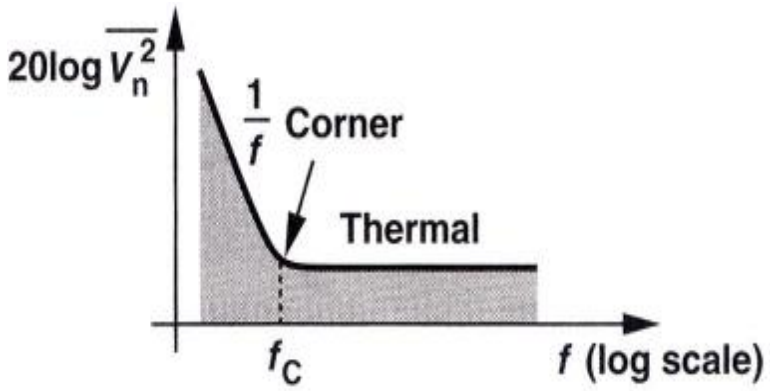

Figure 2.6 Concept of flicker noise corner frequency

In order to quantify the significance of 1/*f* noise with respect to thermal noise for a given device, we plot both spectral densities on the same axes in Fig. 2.6. Called the 1/*f* noise "corner frequency", the intersection point serves as a measure of what part of the band is mostly corrupted by flicker noise. In the above description, the 1/*f* noise corner, f_C, of the output current is determined as

$$f_C = \frac{K}{C_{ox}WL} gm \frac{3}{8kT} \tag{2.6}$$

This result implies that f_C generally depends on device dimensions and bias current. Nonetheless, since for a given *L*, the dependence is relatively weak, the 1/*f* noise corner is relatively constant, falling in the vicinity of 500KHz to 1MHz for submicron transistors [4]

2.3 Noise Models for Circuit Elements [5]

Resistors

The major source of noise in resistors is thermal noise. As just discussed, it appears as white noise and can be modeled as a voltage source, $V_R(f)$, in series with a noiseless resistor. With such an approach, the spectral density function, $V_R^2(f)$, is found to be given by

$$V_R^2(f) = 4kTR \tag{2.7}$$

where *k* is Boltzmann's constant (1.38×10^{-23} J/K), *T* is the temperature in Kelvins, and *R* is the resistance size.

An alternate model can be derived by finding the Norton equivalent circuit. Specifically, the series voltage noise source, $V_R(f)$, can be replaced with a parallel

current noise source, $I_R(f)$, given by

$$I_R^2(f) = \frac{V_R^2(f)}{R^2} = \frac{4kT}{R} \tag{2.8}$$

Both resistor models are summarized in Fig. 2.7.

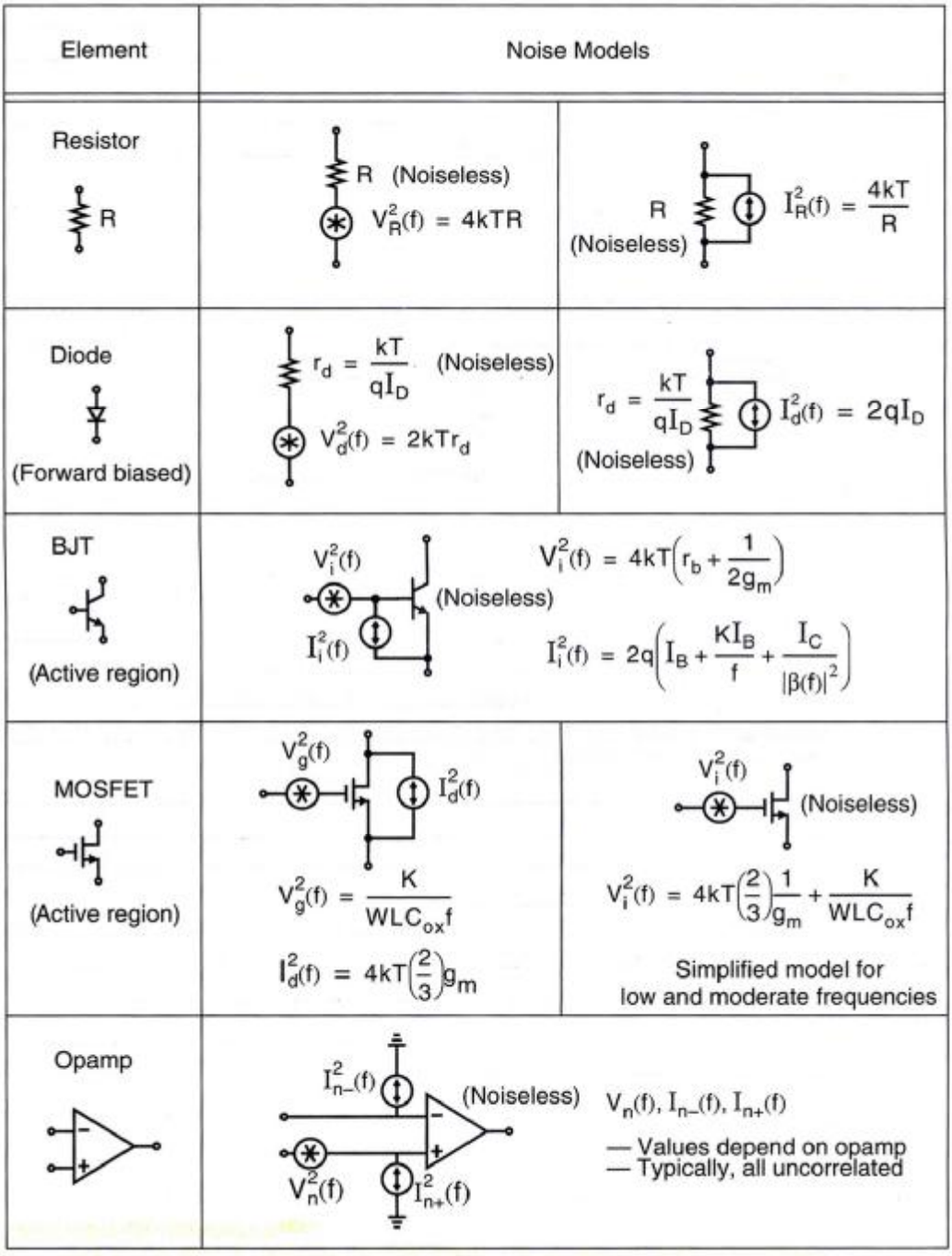

Figure 2.7 Circuit elements and their noise modes. Note that capacitors and inductors do not generate noise.

Diodes

Shot noise is typically the dominant noise in diodes and can be modeled with a current source in parallel with the small-signal resistance of the diode, as Fig. 2.7 shows. The spectral density function of the current source is found to be given by

$$I_d^2(f) = 2qI_D \tag{2.9}$$

where q is one electronic charge (1.6×10^{-19} C) and I_D is the dc bias current flowing through the diode. The small-signal resistance of the diode, r_d, is given by the usual relationship,

$$r_d = \frac{kT}{qI_D} \tag{2.10}$$

Bipolar Transistors

The noise in bipolar transistors is due to shot noise of both the collector and base currents, the flicker noise of the base current, and the thermal noise of the base resistance. A common practice is to combine all these noise sources into two equivalent noise sources at the base of the transistor, as shown in Fig. 2.7. Here, the equivalent input voltage noise, $V_i(f)$, is given by

$$V_i^2(f) = 4kT\left(r_b + \frac{1}{2gm}\right) \tag{2.11}$$

where the r_b term is due to the thermal noise of the base resistance and gm term is due to collector-current shot noise referred back to the input. The equivalent input current noise, $I_i(f)$, equals

$$I_i^2(f) = 2q\left(I_B + \frac{KI_B}{f} + \frac{I_C}{|b(f)|^2}\right) \tag{2.12}$$

where the $2qI_B$ term is a result of base-current shot noise, the KI_B/f term models 1/f noise (K is a constant dependent on device properties), and the I_C term is the input-referred collector-current shot noise (it is often ignored).

MOSFETS

The dominant noise sources for active MOSFET transistors are flicker noise and thermal noise, as shown in Fig. 2.7. The flicker noise is modeled as a voltage source in series with the gate of value

$$V_g^2(f) = \frac{K}{WLC_{ox}f} \tag{2.13}$$

where the constant K is dependent on device characteristics and can very widely for

different devices in the same process.

The derivation of the thermal noise term is straightforward and is due to the resistive channel of a MOS transistor in the active region. If the transistor was in triode, the thermal noise current in the drain due to the channel resistance would simply be given by $I_d^2(f) = (4kT)/r_{ds}$, where r_{ds} is the channel resistance. However, when the transistor is in the active region, the channel cannot be considered homogeneous, and thus, the total noise is found by integrating over small portions of the channel. Such an integration results in the noise current in the drain being given by

$$I_d^2(f) = 4kT\,g\;g_m \tag{2.14}$$

the coefficient γ is derived to be equal to 2/3 for long-channel transistors and may need to be replaced by a larger value for submicron MOSFET [7]. The exact value of this number is under active research.

Opamps

Noise in poamps is modeled using three uncorrelated input-referred noise sources, as shown Fig. 2.7. With an opamp that has a MOSFET input stage, the current noise can often be ignored at low frequencies since their values are small. However, for bipolar input stages, all three noise sources are typically required, as shown in Fig. 2.8. In Fig. 2.8(a), if $V_n(f)$ is not included in the model , a unity-gain buffer with no resistors indicates that the circuit output is noiseless. In fact, the voltage noise source, $V_n(f)$, dominates. If $I_{n-}(f)$ is not included in an opamp model, the circuit shown in Fig. 2.8(b) indicates that the output noise voltage equals $V_n(f)$. Here, the current noise may dominate if the resistance, R, is larger. A similar conclusion can be drawn with $I_{n+}(f)$, as shown in Fig. 2.8(c).

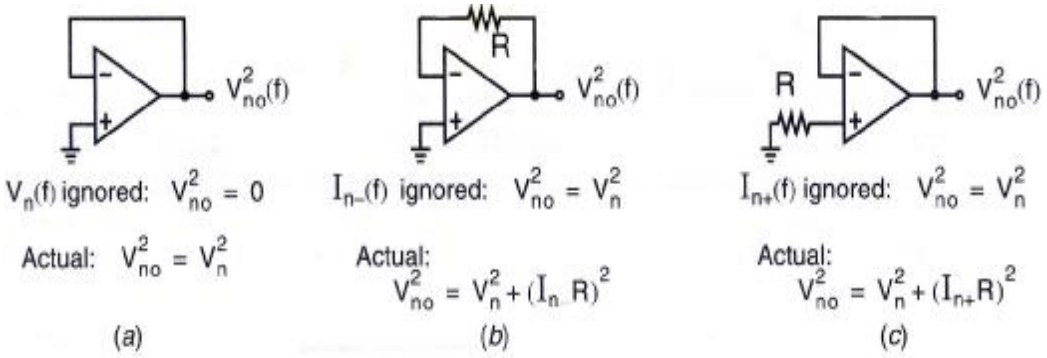

Figure 2.8 Opamp circuits showing the need for three noise source in an opamp noise model. Assume the resistance, R, is noiseless is simplified from $V_n(f)$ to V_n, and so on.

2.4 Noise Theory Apply to RF Circuit

In this section, we focus on the noise theorem applying to RF circuit design. The first circuit is the low noise amplifier (LNA) with using MESFET for 4GHz band transmission. The noise figure plays important role for LNA. Therefore, the noise figure represented by two port network will be described.

The second circuit is the oscillator at 2GHz signal generation with using MOSFET to fabricate the integrated circuit under voltage controlled. Deal with oscillator property, the phase noise shows the critical parameter for circuit design. In the following, noise figure and phase noise will be introduced separately.

2.4.1 Definition of Noise Figure by Two-Port Network

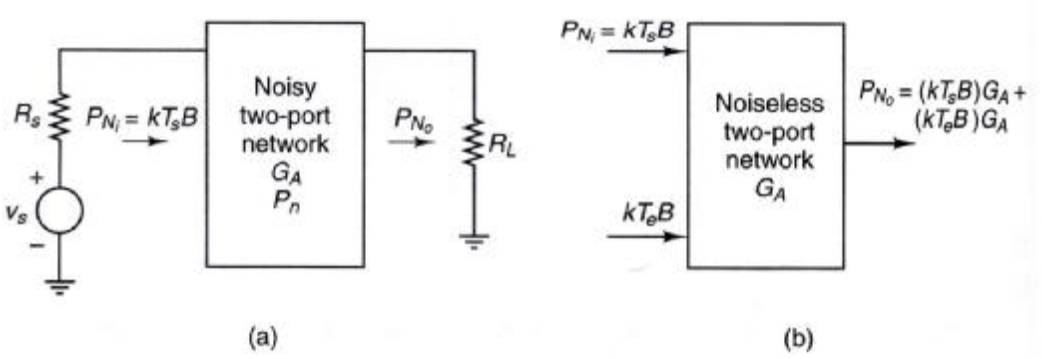

Figure 2.9 (a) Noisy two-port network; (b) noiseless two-port representation.

It is well know that the maximum noise power that a noisy resistor can deliver to a network within the bandwidth B is

$$P_N = \frac{V_{n,rms}^2}{4R} = kTB \tag{2.15}$$

Next, we consider the noise characterization of a two-port network. A two-port network is shown in Fig. 2.9, where the available input noise power from the resistor R_s at temperature T_s is $P_{Ni} = kT_sB$. This input noise power gets amplified by the available gain of the two-port network (G_A) and appears at the output. In addition, the noisy two-port network contributes a certain amount of noise power to the output, shown as P_n in Fig. 2.9a. The total available noise power at the output is

$$P_{N_o} = G_A P_{N_i} + P_N = G_A kT_s B + P_N \tag{2.15}$$

Associated with P_n, we can define an effective input noise temperature T_e such that

$$T_e = \frac{P_n}{kBG_A} \tag{2.16}$$

The noise figure *F* of a two-port network at a specific signal frequency is defined as [9]

$$F = \frac{P_{N_o}}{P_{N_i} G_A} = \frac{\text{total available noise power at the output}}{\text{amplify the available noise power at the input}} \tag{2.17}$$

By some manipulation, the noise figure is

$$F = 1 + \frac{T_e}{T_s} \tag{2.18}$$

2.4.2 Oscillator Phase Noise

For a nominally periodic sinusoidal signal, we can write $x(t) = A\cos[w_c t + f_n(t)]$, where $f_n(t)$ is a small random excess phase representing variations in the period. The function $f_n(t)$ is "called phase noise". Note that for $|f_n(t)| << 1\text{rad}$, we have $x(t) \approx A\cos w_c t - A f_n(t)\sin w_c t$; that is, the spectrum of $f_n(t)$ is translated to $\pm w_c$.

In RF applications, phase noise is usually characterized in the frequency domain. For an ideal sinusoidal oscillator operating at w_c, the spectrum assumes the shape of an impulse, whereas for an actual oscillator, the spectrum exhibits "skirts" around the carrier frequency in Fig. 2.10. To quantify phase noise, we consider a unit bandwidth at an offset Δw with respect to w_c, calculate the noise power in this bandwidth, and divide the result by the carrier (average) power [10].

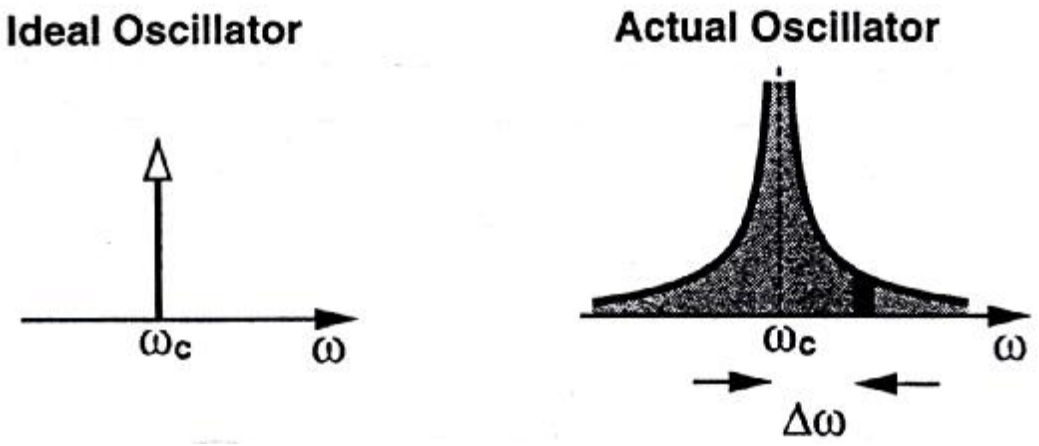

Figure 2.10 Output spectrum of ideal and actual oscillators.

Phase noise is defined as the ratio of power in one phase modulation sideband to the total signal power per unit bandwidth (one Hertz) at a given offset; f_m, from the signal frequency, and is denoted as $L(f_m)$. It is usually expressed in decibels relative to the carrier power per Hertz of bandwidth (dBc/Hz). A typical oscillator phase noise

specification for an FM cellular radio, for example, may be -110dBc/Hz at 25KHz from the carrier.

In general, the output voltage of an oscillator or synthesizer can be written as [1]:

$$v_o(t) = V_0[1 + A(t)]\cos[w_0 t + q(t)] \tag{2.19}$$

where $A(t)$ represents the amplitude fluctuations of the output, and $\theta(t)$ represents the phase variation of the output waveform. Of these, amplitude variations can usually be well controlled, and generally have less impact on system performance.

Small changes in the oscillator frequency can be represented as a frequency modulation of the carrier by letting

$$q(t) = \frac{\Delta f}{f_m}\sin w_m t = q_p \sin w_m t \tag{2.20}$$

where $f_m = w_m / 2p$ is the modulating frequency. The peak phase deviation is $q_p = \Delta f / f_m$ (also called the modulation index). Substituting (2.20) into (2.19) and expanding gives

$$v_o(t) = V_0\left[\cos w_0 t \cos(q_p \sin w_m t) - \sin w_0 t \sin(q_p \sin w_m t)\right] \tag{2.21}$$

where we set $A(t) = 0$ to ignore amplitude fluctuations. Assuming the phase deviations are small, so that q_p <<1, the small argument expressions that $\sin x \cong x$ and $\cos x \cong 1$ can be used to simplify (2.21) to

$$\begin{aligned} v_o(t) &= V_0\left[\cos w_0 t - q_p \sin w_m t \sin w_0 t\right] \\ &= V_0\left\{\cos w_0 t - \frac{q_p}{2}\left[\cos(w_0 + w_m)t - \cos(w_0 - w_m)t\right]\right\} \end{aligned} \tag{2.22}$$

This expression shows that small phase or frequency deviations in the output of an oscillator result in modulation sidebands at $w_0 \pm w_m$, located on either side of carrier signal at w_0. When these deviations are due to random changes in temperature or device noise, the output spectrum of the oscillator will take the form shown in Figure 2.10.

According to the definition of phase noise as the ratio of noise power in a singale sideband to the carrier power, the waveform of (2.22) has a corresponding phase noise of

$$L(f) = \frac{P_n}{P_c} = \frac{\frac{1}{2}\left(\frac{V_0 q_p}{2}\right)^2}{\frac{1}{2}V_0^2} = \frac{q_p^2}{4} = \frac{q_{rms}^2}{2} \tag{2.23}$$

where $q_{rms} = q_p / \sqrt{2}$ is the rms value of the phase deviation. The two-sided power spectral density associated with phase noise includes power in both sidebands:

$$S_q(f_m) = 2L(f_m) = \frac{q_p^2}{2} = q_{rms}^2 \tag{2.24}$$

2.4.3 Leeson's Model for Phase Noise

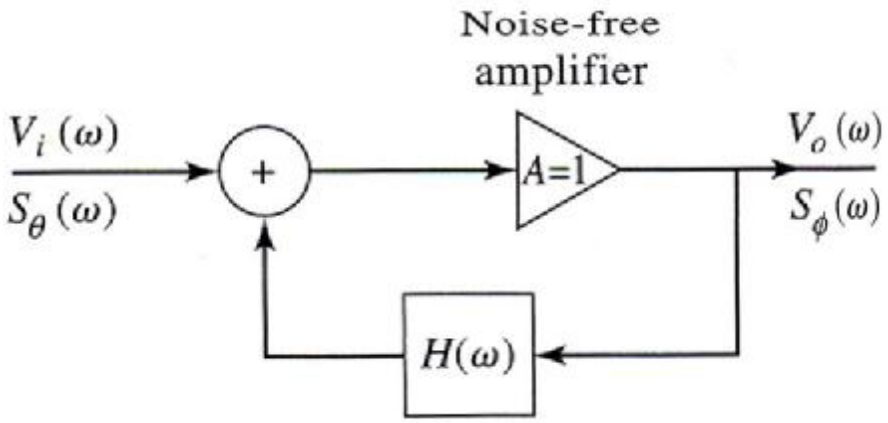

Figure 2.11 feedback amplifier model for characterizing oscillator phase noise.

In this section we present Leeson's model for characterizing the power spectral density of oscillator phase noise [9], [11]. We will model the oscillator as an amplifier with a feedback path, as shown in Figure 2.11. If the voltage gain of the amplifier is included in the feedback transfer function $H(w)$, then the voltage transfer function for the oscillator circuit is

$$V_0(w) = \frac{V_i(w)}{1 - H(w)} \tag{2.25}$$

If we consider oscillators that use a high-*Q* resonant circuit in the feedback loop, the $H(w)$ can be represented as the voltage transfer function of a parallel *RLC* resonator [4]:

$$H(w) = \frac{1}{1 + jQ\left(\frac{w}{w_0} - \frac{w_0}{w}\right)} = \frac{1}{1 + 2jQ\Delta w / w_0} \tag{2.26}$$

where w_0 is the resonant frequency of the oscillator, and $\Delta w = w - w_0$ is the offset relative to the resonant frequency. We know that the input and output power spectral densities are related by the square of the magnitude of the voltage transfer function, so we can use (2.25) to write

$$S_f(w) = \left|\frac{1}{1 - H(w)}\right|^2 S_q(w) = \frac{1 + 4Q^2 \Delta w^2 / w_0^2}{4Q^2 \Delta w^2 / w_0^2} S_q(w)$$

$$= \left(1 + \frac{w_0^2}{4Q^2 \Delta w^2}\right) S_q(w) = \left(1 + \frac{w_h^2}{\Delta w^2}\right) S_q(w) \tag{2.27}$$

where $S_q(w)$ is the input PSD, and $S_f(w)$ is the output PSD. In (2.27) we have also defined $w_h = w_0 / 2Q$ as the half-power (3dB) bandwidth of the resonator.

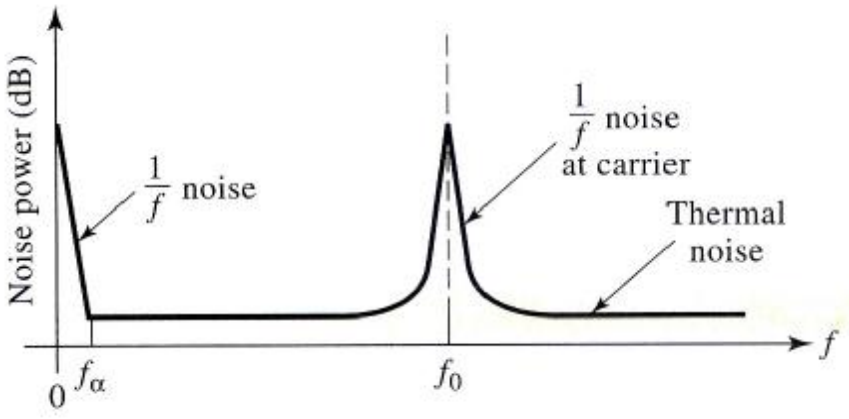

Figure 2.12 Noise power versus frequency for an amplifier with an applied input signal.

The noise spectrum of a typical transistor amplifier with an applied sinusoidal signal at f_0 is shown in Figure 2.12. Besides *kTB* thermal noise, transistors generate additional noise that varies as 1/*f* at frequencies below the frequency f_α. This 1/*f*, or *flicker* noise is likely caused by random fluctuations of the carrier density in the active device. Due to the nonlinearity of the transistor, the 1/*f* noise will modulate the applied signal at f_0, and appear as 1/*f* noise sidebands around f_0. Since the 1/*f* noise component dominates the phase noise power at frequencies close to the carrier, it is important to include it in our model. Thus we consider an input power spectral density as shown in Figure 2.13, where $K/\Delta f$ represents the 1/*f* noise component around the carrier, and kT_0F/P_0 represents thermal noise. Thus the power spectral density applied to the input of the oscillator can be written as

$$S_q(w) = \frac{kT_0F}{P_0}\left(1 + \frac{Kw_a}{\Delta w}\right) \tag{2.28}$$

where *K* is a constant accounting for the strength of the 1/*f* noise, and $w_a = 2pf_a$ is the *corner frequency* of the 1/*f* noise. The corner frequency depends primarily on the type of transistor used in the oscillator.

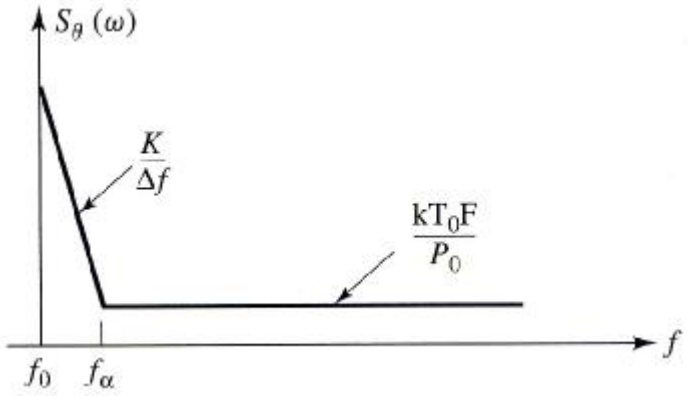

Figure 2.13 Idealized power spectral density of amplifier noise, including 1/*f* and thermal components.

Using (2.28) in (2.27) gives the power spectral density of the output phase noise as

$$S_f(w) = \frac{kT_0F}{P_0}\left(\frac{Kw_0^2w_a}{4Q^2\Delta w^3} + \frac{w_0^2}{4Q^2\Delta w^2} + \frac{Kw_a}{\Delta w} + 1\right)$$

$$= \frac{kT_0F}{P_0}\left(\frac{Kw_aw_h^2}{\Delta w^3} + \frac{w_h^2}{\Delta w^2} + \frac{K\Delta w_a}{\Delta w} + 1\right) \qquad (2.29)$$

This result is sketched in Figure 2.14. There are two cases, depending on which of the middle two terms of (2.29) is more significant. In either case, for frequencies close to the carrier f_0, the noise power decreases as $1/f^3$, or -18dB/octave. If the resonator has a relatively low Q, so that its 3dB bandwidth $f_h > f_a$, then for frequencies between f_α and f_h the noise power drops as $1/f^2$, or -12dB/octave. If the resonator has a relatively high Q, so that $f_h < f_a$, then for frequencies between f_h and f_α the noise power drops as $1/f$, or -6dB/octave.

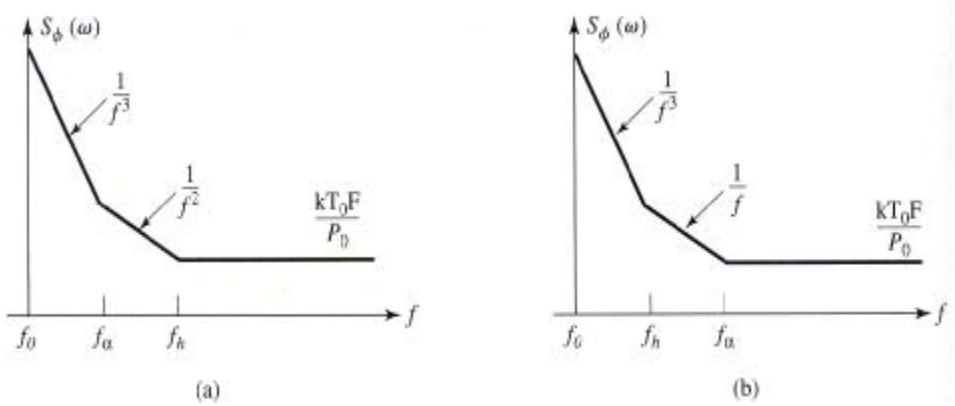

Figure 2.14 Power spectral density of phase noise at the output of an oscillator. (a) response for $f_h > f_a$ (low *Q*). (b) response for $f_h < f_a$ (high *Q*).

Chapter 3

Microwave Low Noise Amplifier with Source Inductance Feedback

3.1 Introduction

The first stage of a receiver is typically a low-noise amplifier (LNA), whose main function is to provide enough gain to overcome the noise of subsequent stages (such as a mixer). Aside from provide this gain while adding as little noise as possible, an LNA should accommodate large signals without distortion, and frequency must also present a specific impedance, such as 50Ω, to the input source[9].Recently, Source inductive feedback (SIF) has found its applications in the low noise amplifiers by MMIC and CMOS IC technologies[12-15]. The noise properties of amplifiers are described typically by minimum noise figure $F_{\min}$, equivalent noise resistance R_n and optimal reflection coefficient Γ_{opt}. A low noise amplifier is normally designed to have the source reflection coefficient Γ_s equal to Γ_{opt} to obtain the lowest noise figure $F_{\min}$, at the expanse of the return loss. The technique of SIF can introduce equivalently a resistor to achieve input impedance and noise matching simultaneously, and even slightly reduce both $F_{\min}$ and R_n [16-20]. As the frequency is raised, this technique may fail. The package parasitic is conjectured to be the crucial role. But until now, a study of the relationship between FET parameter and SIF inductance has not been detailed. The information of frequency limitations of SIF in package device are also not available. It is interesting to study the universality of the technique, especially in the discrete circuit design for practical applications. Due to the circuit complexity, the studies are explored by numerical computation. We study the noise problem with a noisy two-port network [21,22,23,24]. In section 3.2, the generic behaviors of packaged MESFET with SIF at various frequencies region are examined from the two-port scattering and noise parameters. In section 3.3, the equivalent small signal model with noise sources are extracted. The mechanisms of degradation in $F_{\min}$ are elucidated by inspecting each element of the model. Finally, the frequency limitation of SIF technique in the package device is indicated.

3.2 Calculations of Noise Parameters

3.2.1 Low-Noise Amplifier Design

Besides stability and gain, another important design consideration for a microwave low noise amplifier is its noise figure. In receiver applications especially, it is often required to have a preamplifier with as low a noise figure as possible , the first stage of a receiver front end has the dominate effect on the noise performance of the overall system. Generally it is not possible to obtain both minimum noise figure and maximum gain for an amplifier, so some sort of compromise must be made. This can be down by using constant gain circles and circles of constant noise figure to select a usable trade-off between noise figure and gain. Here we will derive the equations for constant noise figure circles, and show how they are used in transistor amplifier design.

As derived in references [1,8,9], the noise figure of a two-port amplifier can be expressed as

$$F = F_{\min} + \frac{R_N}{G_S}\left|Y_S - Y_{opt}\right|^2 \tag{3.1}$$

where the following definitions apply：

$Y_S = G_S + j\,B_S$ = source admittance presented to transistor.

Y_{opt} = optimum source admittance that results in minimum noise figure.

F_{min} = minimum noise figure of transistor, attained when $Y_S = Y_{opt.}$

R_N = equivalent noise resistance of transistor.

G_S = real part of source admittance.

Instead of the admittance Y_S and Y_{opt}, we can use the reflection coefficients Γ_s and Γ_{opt}, where

$$Y_S = \frac{1}{Z_0}\frac{1-\Gamma_S}{1+\Gamma_S} \tag{3.2a}$$

$$Y_{opt} = \frac{1}{Z_0}\frac{1-\Gamma_{opt}}{1+\Gamma_{opt}} \tag{3.2b}$$

Γ_s is the source reflection coefficient . The quantities F_{min}, Γ_{opt}, and R_N are characteristics of the particular transistor being used, and are called the noise parameters of the device; they may be given by the manufacturer, or measured.

Using (3.2), the quantity $\left|Y_S - Y_{opt}\right|^2$ can be expressed in terms of Γ_s and Γ_{opt} ：

$$\left|Y_S - Y_{opt}\right|^2 = \frac{4}{Z_0^{\,2}}\frac{\left|\Gamma_S - \Gamma_{opt}\right|^2}{\left|1+\Gamma_S\right|^2\left|1+\Gamma_{opt}\right|^2} \tag{3.3}$$

Also,

$$G_S = \mathrm{Re}\{Y_S\} = \frac{1}{2Z_0}\left(\frac{1-\Gamma_S}{1+\Gamma_S} + \frac{1-\Gamma_S^*}{1+\Gamma_S^*}\right) = \frac{1}{Z_0}\frac{1-|\Gamma_S|^2}{|1+\Gamma_S|^2} \tag{3.4}$$

Using these results in (3.1) gives the noise figure as

$$F = F_{\min} + \frac{4R_N}{Z_0}\frac{|\Gamma_S - \Gamma_{opt}|^2}{(1-|\Gamma_S|^2)|1+\Gamma_{opt}|^2} \tag{3.5}$$

For a fixed noise figure, F, we can show that this result defines a circle in the Γ_s plane. First define the noise figure parameter, N, as

$$N = \frac{|\Gamma_S - \Gamma_{opt}|^2}{1-|\Gamma_S|^2} = \frac{F - F_{\min}}{4R_N / Z_0}|1+\Gamma_{opt}|^2 \tag{3.6}$$

which is constant, for a given noise figure and set of noise parameters. Then rewrite (3.6) as

$$(\Gamma_S - \Gamma_{opt})(\Gamma_S^* - \Gamma_{opt}^*) = N(1-|\Gamma_S|^2),$$

$$\Gamma_S\Gamma_S^* - (\Gamma_S\Gamma_{opt}^* + \Gamma_S^*\Gamma_{opt}) + \Gamma_{opt}\Gamma_{opt}^* = N - N|\Gamma_S|^2,$$

$$\Gamma_S\Gamma_S^* - \frac{(\Gamma_S\Gamma_{opt}^* + \Gamma_S^*\Gamma_{opt})}{N+1} = \frac{N - |\Gamma_{opt}|^2}{N+1},$$

Now add $|\Gamma_{opt}|^2/(N+1)^2$ to both sides to complete the square to obtain

$$\left|\Gamma_S - \frac{\Gamma_{opt}}{N+1}\right| = \frac{\sqrt{N(N+1-|\Gamma_{opt}|^2)}}{(N+1)}, \tag{3.7}$$

This result defines circles of constant noise figure with centers at

$$C_F = \frac{\Gamma_{opt}}{N+1}, \tag{3.8}$$

and radii of

$$R_F = \frac{\sqrt{N(N+1-|\Gamma_{opt}|^2)}}{N+1} \tag{3.9}$$

3.2.2 Noise Two-port Network Theory of Cascode Connection

First, the generic behaviors of packaged MESFET with SIF shown in Fig.3.1 are examined through the noise and scattering parameters. In general, the noise parameters are in terms of $F_{\min}$, R_n and Γ_{opt} in the data sheet of Table 3.1. The

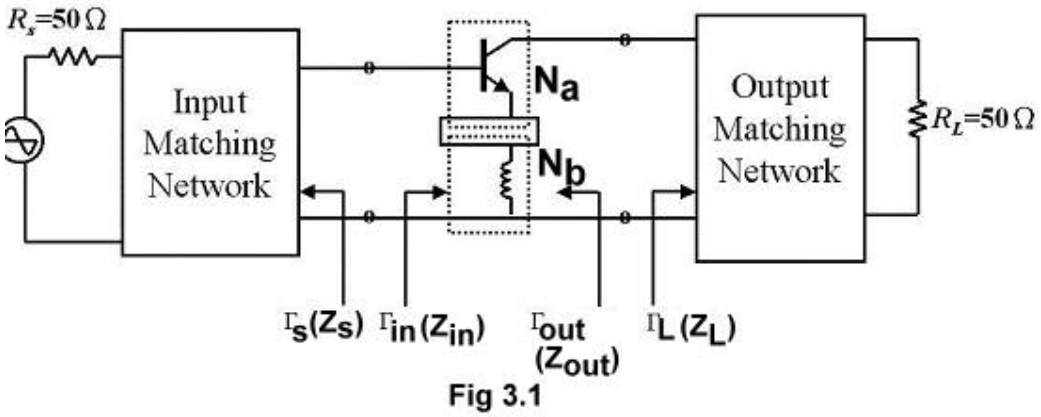

Fig 3.1

Fig.3.1 Block diagram of the single stage microwave amplifier with SIF

Table 3.1 NEC NE42484A under V_{ds} = 2V and I_{ds} = 10mA

```
! NEC NE42484A
#   GHz      S         MA         R         50
    0.1     0.999    -1.9  5.116  178.3  0.002  87.2  0.673   -1.3
    0.2     0.998    -3.9  5.115  176.2  0.004  85.5  0.672   -2.7
    0.5     0.994    -9.8  5.101  170.0  0.011  81.6  0.667   -6.7
    1.0     0.981   -19.7  5.047  160.1  0.021  75.7  0.657  -13.2
    2.0     0.944   -39.1  4.853  141.4  0.037  63.7  0.634  -26.1
    3.0     0.900   -57.5  4.594  124.0  0.050  52.4  0.604  -38.7
    4.0     0.852   -74.5  4.314  107.7  0.061  42.2  0.571  -51.0
    5.0     0.801   -89.9  4.044   92.3  0.070  33.4  0.536  -63.0
    6.0     0.750  -104.1  3.798   77.5  0.077  25.5  0.499  -75.0
    7.0     0.698  -117.2  3.584   63.2  0.084  18.4  0.462  -87.0
    8.0     0.648  -129.8  3.403   49.2  0.090  11.7  0.428  -99.4
    9.0     0.598  -142.4  3.251   35.4  0.095   5.2  0.399 -112.7
   10.0     0.551  -155.4  3.121   21.7  0.100  -1.3  0.378 -127.5
   11.0     0.508  -169.5  3.008    7.9  0.106  -7.9  0.367 -144.2
   12.0     0.469   174.9  2.902   -6.0  0.111 -14.9  0.369 -163.3
   13.0     0.435   157.6  2.796  -20.3  0.116 -22.3  0.385  175.5
   14.0     0.407   138.6  2.682  -34.9  0.121 -30.3  0.413  154.6
   15.0     0.386   118.1  2.552  -50.1  0.125 -38.9  0.452  134.2
   16.0     0.373    96.5  2.404  -65.7  0.127 -48.3  0.500  115.8
   17.0     0.370    74.9  2.234  -81.9  0.129 -58.5  0.553   99.7
   18.0     0.376    54.4  2.045  -98.1  0.128 -69.7  0.612   85.5
   19.0     0.394    37.1  1.840 -113.3  0.124 -82.0  0.673   73.0
   20.0     0.424    25.1  1.627 -124.3  0.116 -95.3  0.737   61.5
! NOISE PARAMETERS
    1.0    0.31   0.78    10  0.43
    2.0    0.34   0.76    28  0.38
    4.0    0.40   0.72    58  0.28
    6.0    0.47   0.65    84  0.21
    8.0    0.56   0.57   113  0.15
   10.0    0.66   0.50   141  0.10
   12.0    0.80   0.44   173  0.08
   14.0    0.93   0.36  -148  0.09
   16.0    1.10   0.30  -106  0.21
   18.0    1.31   0.30   -75  0.36
```

noise figure F is described again as [17].

$$F = F_{\min} + \frac{R_n}{G_s}\left|Y_s - Y_{opt}\right|^2 \tag{3.10}$$

where $Y_s = G_s + jB_s$ represents the source admittance, and Y_{opt} is the optimum admittance. The admittance Y_{opt} is equal to：

$$Y_{opt} = G_{opt} + jB_{opt} = \frac{1-\Gamma_{opt}}{1+\Gamma_{opt}} Y_0 \tag{3.11}$$

For convenience, another form of noise figure is given by：

$$F = 1 + \frac{r_n + g_n\left|Z_s + Z_c\right|^2}{R_s} \tag{3.12}$$

where r_n is the equivalent normalized noise resistance, g_n is the equivalent normalized noise conductance [25], and Z_c is the correlation impedance. Their interrelations are given as：

$$r_n = \frac{(4R_nG_{opt} - F_{min} + 1)(F_{min} - 1)}{4R_n\left|Y_{opt}\right|^2} \tag{3.13}$$

$$g_n = R_n\left|Y_{opt}\right|^2 \tag{3.14}$$

$$Z_c = \frac{F_{\min} - 1 - 2R_nG_{opt} + j2R_nB_{opt}}{2R_n\left|Y_{opt}\right|^2} = R_c + jX_c \tag{3.15}$$

Inversely, we also get another form of noise figure as following：

$$F_{\min} = 1 + 2g_n(R_c + R_{opt}) \tag{3.16}$$

After SIF is added , new parameters r_{nt} 、g_{nt} and Z_{ct} with subscript t denoted as total are represented as follows [22]：

$$r_{nt} = r_n \tag{3.17}$$

$$g_{nt} = \left|D_n\right|^2 g_n \tag{3.18}$$

$$Z_{ct} = \frac{Z_c + E_n}{D_n} = R_{ct} + jX_{ct} \tag{3.19}$$

where

$$E_n = -Z_{11a} + \frac{(Z_{11a} + Z_{11b})}{(Z_{21a} + Z_{21b})} Z_{21a} \tag{3.20}$$

$$D_n = \frac{Z_{21a}}{Z_{21a} + Z_{21b}} \tag{3.21}$$

and $Z_{ija} and Z_{ijb}$, I, j=1,2 represent the element of the impedance matrix of the transistor in network N_a and the external inductor in network N_b, respectively. The inductance involved by N_b network is $Z_{11b} = j\omega L$ and $Z_{21b} = j\omega L$. Accordingly, from (3.13) to (3.16) the new noise figure, noise resistance, and optimal admittance with SIF become：

$$F_{min\,t} = 1 + 2\left(g_{nt} R_{ct} + \sqrt{g_{nt} r_{nt} + (g_n R_c)^2} \right) \tag{3.22}$$

$$R_{nt} = r_{nt} + g_{nt} |Z_{ct}|^2 \tag{3.23}$$

$$Y_{optt} = \frac{\sqrt{r_{nt}/g_{nt} + R_{ct}^2} + jX_{ct}}{r_{nt}/g_{nt} + |Z_{ct}|^2} \tag{3.24}$$

and then

$$\Gamma_{optt} = \frac{1 - \frac{Y_{optt}}{Y_0}}{1 + \frac{Y_{optt}}{Y_0}} \tag{3.25}$$

Hereafter, the subscript t is dropped for convenience.

The scattering parameters are also changed as the inductor is included into the active device . They are obtained via a numerical manipulation of two to three port transformations [18,21]. To obtain the noise and gain matching, the portraits of new Γ_{in}^* and Γ_{opt} in the Smith chart as a function of feedback inductance are calculated. Here, Γ_{in}^* is further replaced by S_{11}^* under the assumption of small S_{12}. In fact, the behavior of Γ_{in}^* is by no means more complicated than S_{11}. The S_{11} acts as a precursor of Γ_{in}. This approach gives us a quick examination.

3.2.3 Graph of Numerical Computation with Loci of Γ_{opt} and S_{11}^{*}

Following the mentioned procedures, the total Γ_{opt} and scattering parameters can be obtained. A typical microwave FET (Pseudomorphic HJ FET NE42484 from NEC) used in satellite receiver is employed. Fig.3.2(a) and Fig.3.2(b) show the calculated loci of Γ_{opt} and S_{11}^{*} with inductance from 0~1 nH, respectively[18].Fortunately, the starting points for two corresponding portraits in Fig.3.2(a) and 3.2(b) happen to be close to each other. Hence, the portraits can approach to each other as the inductor is added. While this feature maintains only under 8GHz in Fig.3.2(b). As frequency is raised, the portrait of S_{11}^{*} deviate seriously from the constant reactance circle and even runs out off the unit circle. Thus, there is no opportunity for the Γ_{opt} and S_{11}^{*} portraits to approach each other. It implies that the SIF technique for simultaneous noise and input matching can be applied for frequency under 8GHz in our case with discrete package devices.

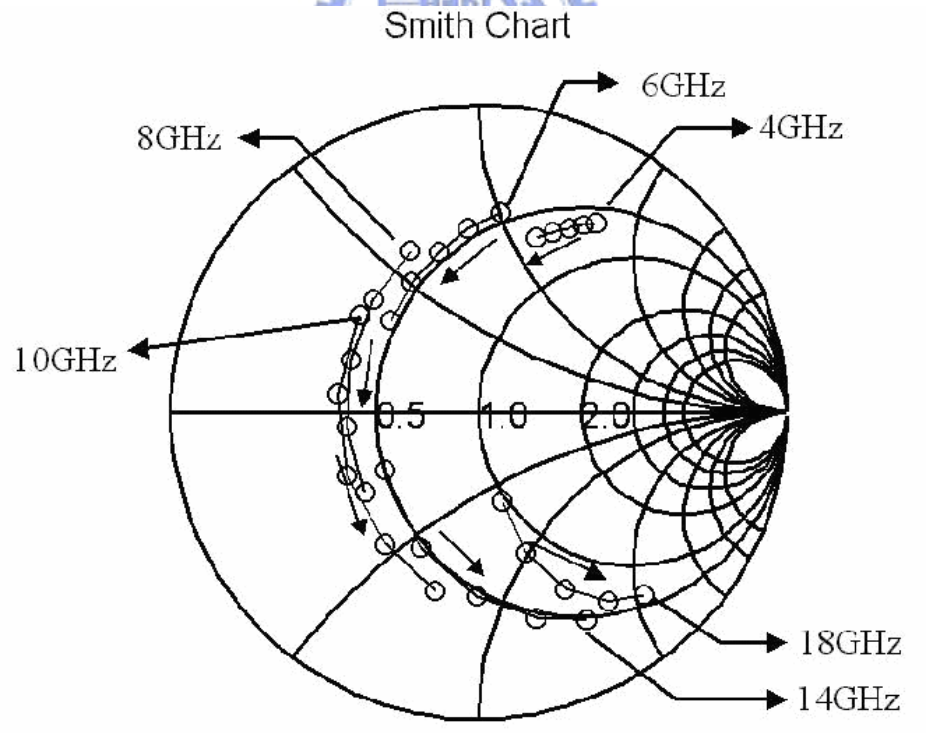

Fig. 3.2(a)

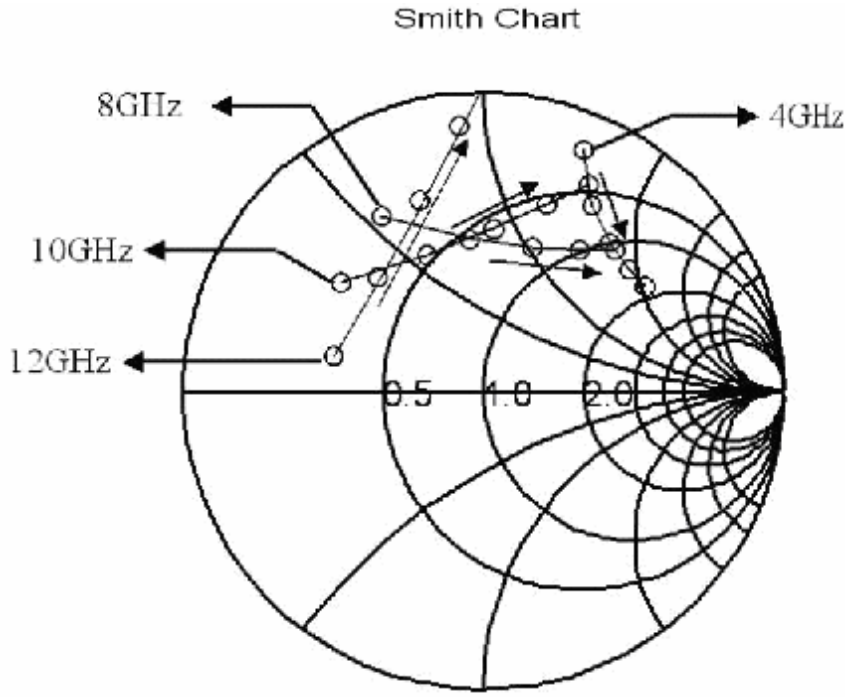

Fig. 3.2(b)

Fig.3.2 Loci of (a) Γ_{opt}, (b) S_{11}^{*} as functions of feedback inductor from 0 to 1nH at various frequencies with NE42484 biased at V_{ds}=2V, I_{ds}=10mA .

Next, the dependence of the new $F_{\min}$ and R_n as functions of source inductance L at two different operating frequencies (4GHz at C band and 14GHz at Ku band) are examined. Fig. 3.3 reveals that $F_{\min}$ is slightly improved at 4GHz as the inductance is increased. On the contrary, $F_{\min}$ is degraded at 14GHz . The equivalent noise resistance R_n reveals the same behavior as shown in Fig.3.3.Therefore, the bad grounding and parasitic effect may cause noise degradation in Ku band.

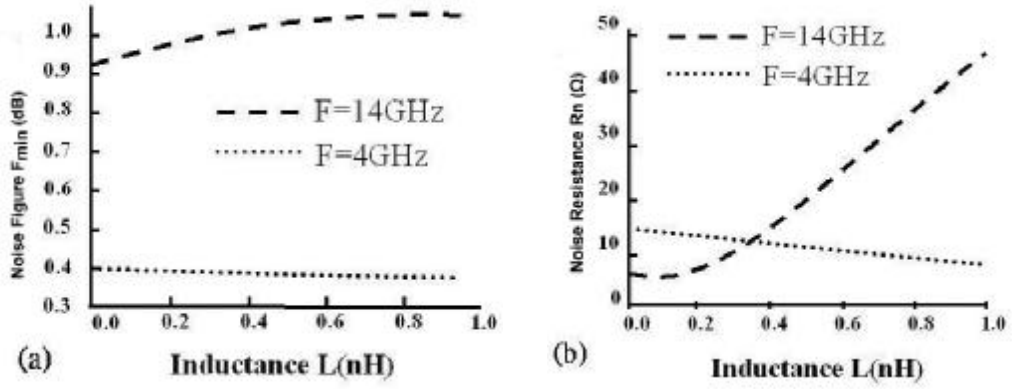

Fig.3.3 Behaviors of (a) F_{min} and (b) R_N as functions of feedback inductor for NE42484 biased at V_{ds}=2V, I_{ds}=10mA.

3.2.4 Experiment of Both Input Impedance and Noise Matching

According to the above calculation, the SIF is healthy for the C-band operation. With the help of SIF, both input and noise can be simultaneously matched. In this example the transistor NEC42484 has a minimum noise figure of 0.4dB and an associated gain of 15.5dB at 4GHz and bias at $V_{ds}= 2V$ and $I_{ds} = 10mA$. Without SIF, the input matching is only about –7dB for best noise figure. The measured results with gray lines are shown in Fig.3.4. With the help of SIF, the calculated input matching is improved to –25dB and an associated gain of 16dB under $F_{\min}$=0.39dB with inductor 0.35nH. These simulation results are shown in Fig.3.4, represented by the broken line. And the solid lines indicate measured data. In practice, the inductor is

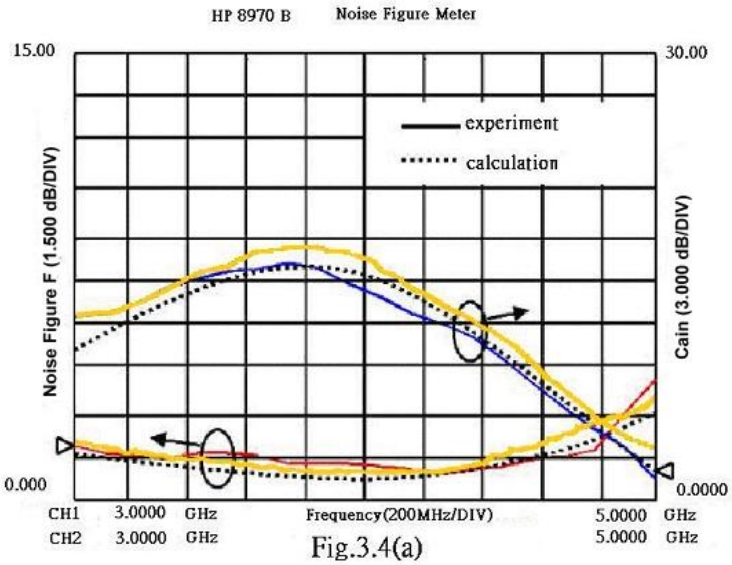

Fig.3.4(a)

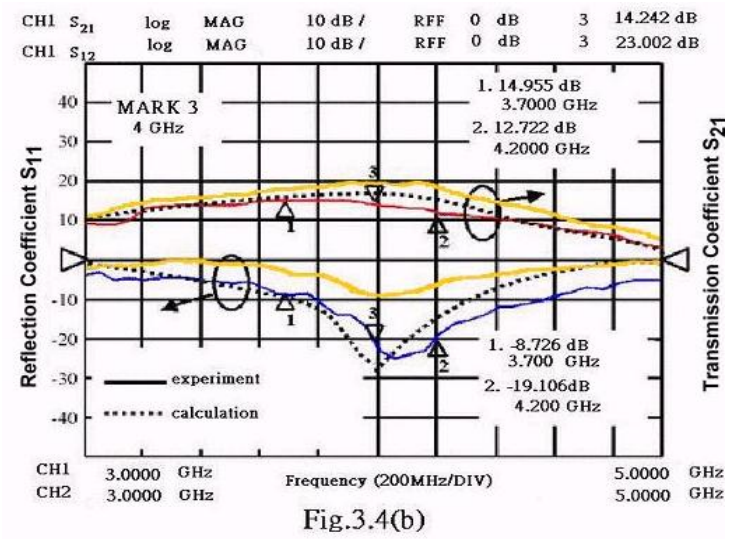

Fig.3.4(b)

Fig.3.4 Experimental results of a C-band amplifier with SIF (a) low noise performance and (b) gain and return loss.

realized by a high impedance line with characteristic impedance $Z = 92\Omega$ and the length 30 mil [13,19,26]. The inductor 0.08nH from via hole is also included. The measured result is shown in Fig3.4 with good input return loss about –23dB under mark 3 symbol, gain about 14dB and noise figure about 1 dB at 4 GHz, respectively. The deviation of noise figure level is due to the connector and microstrip to coaxial transition loss(0.3~0.4dB each).

3.3 Analysis From The Equivalent Circuit

3.3.1 Verification by small signal noise model

To clarify the origins of frequency limitation, we examine the dependence of the noise figure on each circuit element of the small-signal model, containing noise sources and packaged elements. The model including noise sources of the MESFET device as shown in Fig.3.5. The value of each element is determined by the method of extraction technique from the dc measurement, S parameters, and noise parameters [25,27,28]. The parameters are listed in table 3.2. The extracted values of the noise coefficient P, R and C are 0.65 , 0.4 and 0.76, respectively. The S parameters of the noise model in Fig.3.5 have also been calculated. They show a coincident behavior with that of the measured results in Fig.3.4.

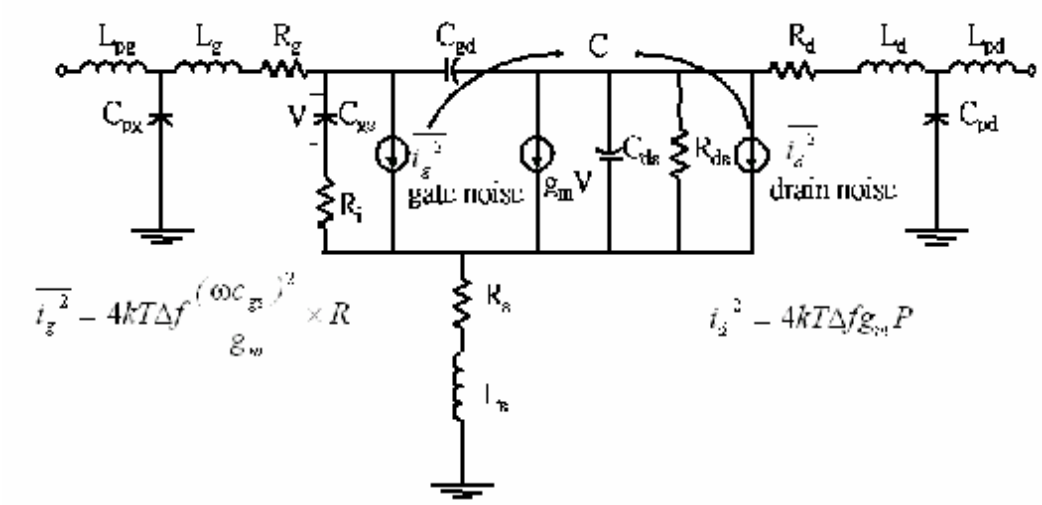

Fig.3.5 Equivalent small-signal model including the package effects and noise sources.

Table 3.2 Small signal parameters included noise parameters

The extracted values of the device NE42484			
Intrinsic Parameter		**Extrinsic Parameter**	
Cgs(pf)	**0.25**	**Rg(Ω)**	**0.31**
Cgd(pf)	**0.04**	**Rd(Ω)**	**0.0072**
Cds(pf)	**0.13**	**Rs(Ω)**	**2.54**
Rds(Ω)	**224.56**	**Lg(nH)**	**0.47**
Ri(Ω)	**2.0**	**Ld(nH)**	**0.19**
gm(ms)	**61.89**	**Ls(nH)**	**0.12**
τ (ps)	**6.1**	**Cpg(pf)**	**0.16**
P	**0.65**	**Cpd(pf)**	**0.07**
R	**0.4**	**Lpg(nH)**	**0.06**
C	**0.76**	**Lpd(nH)**	**0.16**

To test the effects from package, all parasitic elements are intentionally removed from the circuit. To explore further the variations of $F_{\min}$ in bare chip, we examine the influences from intrinsic parts step by step, especially for the elements of C_{gd}、C_{ds} and R_{ds}. The dependence is shown in Fig.3.6. It reveals that C_{gd} and R_{ds} contribute to decrement of $F_{\min}$ with SIF as in the curve A and B of Fig. 3.6, while C_{ds} contribute to increment of $F_{\min}$ as in the curve C. The contributions from C_{gd} and R_{ds} are larger than that from C_{ds} such that the overall $F_{\min}$ of the bare chip device decreases slightly.

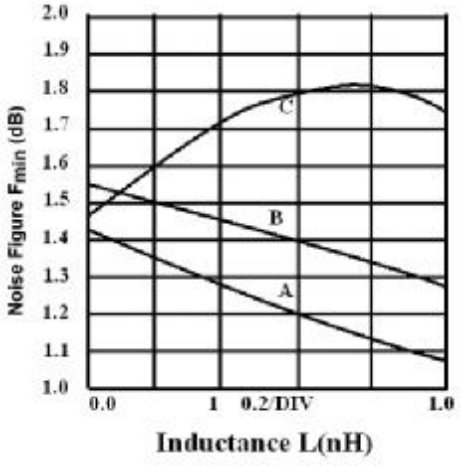

Fig.3.6 $F_{\min}$ versus L for intrinsic model plus C_{gd}, R_{ds} and C_{ds} individually for curve A, B, C respectively at frequency 18GHz.

3.3.2 Discussion of Parasitic Effects on Frequency Performance

As for the package effects, capacitance C_{pg} resided in the input port is confirmed to be the most essential, although other elements can also affect $F_{\min}$. The variations of $F_{\min}$ at various C_{pg} are detailed in Fig.3.7. When the parasitic capacitance C_{pg} is larger than 0.6 pF, F_{min} is degraded with SIF. Referring to package data, it is quite easy to produce C_{pg} above 0.6pf. We may also consider that the inductor with SIF is a part of parasitic in package device. The inductor effects at the source of the transistor can improve the amplifier stability and the input impedance matching. The inductor with proper value under given frequency makes the path go through to the ground for the noise coming from the transistor. Therefore, we detect the lower noise from the output port. These results promote the value of SNR. When the frequency is raised, the parasitic capacitance C_{pg} may destroy the functions of the inductor. The transistor noise must find another way via output port to pass through; hence, we can catch the more noise level from measurement at output port. These facts explain why the F_{min} increased as the frequency increased in Fig.3.3.

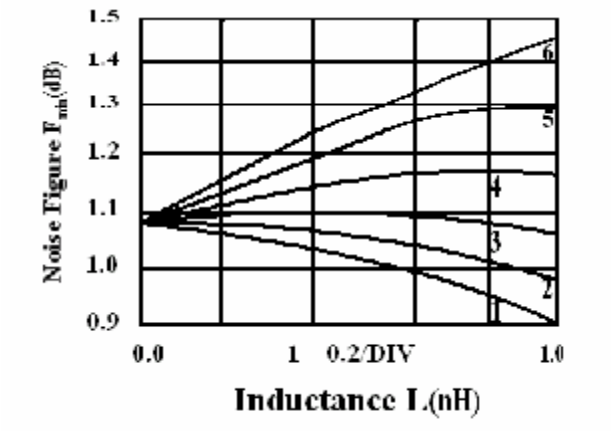

Fig.3.7 F_{min} as a fucntion of inductance L in various value of package parasitic C_{pg} from 0 pf to 0.2pf with 0.04 pf increase for each curve from curve 1 to curve 6 at 14 GHz.

3.3.3 Conclusions

The limitations of SIF technique applied to LNA design are studied by numerical computation. The variations of noise and input matching are examined both from the scattering parameters and from equivalent circuit. At low microwave frequency, both noise and return loss matching can be easily obtained. The results are also confirmed by the C-band LNA with input VSWR about –23dB and an associated gain about 14dB under low minimum noise figure. In the meantime there is a positive influence in new $F_{\min}$. While above C-band, package parasitic becomes profound and results in

degradation of F_{min} and prevents the good matching. The degradation is verified mainly from the interaction between C_{pg} and L. According to our observation, SIF technique should be carefully employed above C-band for package devices fabrications.

3.4 Noise Analysis of 2.4GHz CMOS LNA

3.4.1 Topology of Low Noise Amplifier

In this section, the SIF technique also used in the 2.4GHz CMOS LNA. The manufacture parameter for circuit design is by standard CMOS process under UMC 0.5um DPDM technology. The whole circuit is shown in the Fig 3.8[9,12,30]. The circuit consists of two stages: the input stage with M1 and M2 is formed by the cascoded SIF topology. The output stage, M3 is a common-drain buffer. The spiral inductor of L_t in the output of the first stage is chosen to resonate out with the total capacitance at the drain of M2, and gate capacitance C_{gs} of M3. The on-chip spiral inductor used the top layer metal as spiral and the bottom layer metal as the lead out bridge. L_{gnd} and L_{out} are parasitic inductors formed by bondwires which should be kept as small as possible. While choke L_{vdd} , which resonates with the bypass capacitor C_p to eliminate the noise from the supply should be as large as possible. It can be formed by a long bondwire. L_s and L_g which play the important role in noise and impedance matching are also formed by bondwires. The value of L_s set the input impedance of the LNA and Lg tunes out the input capacitance at the frequency of operation.

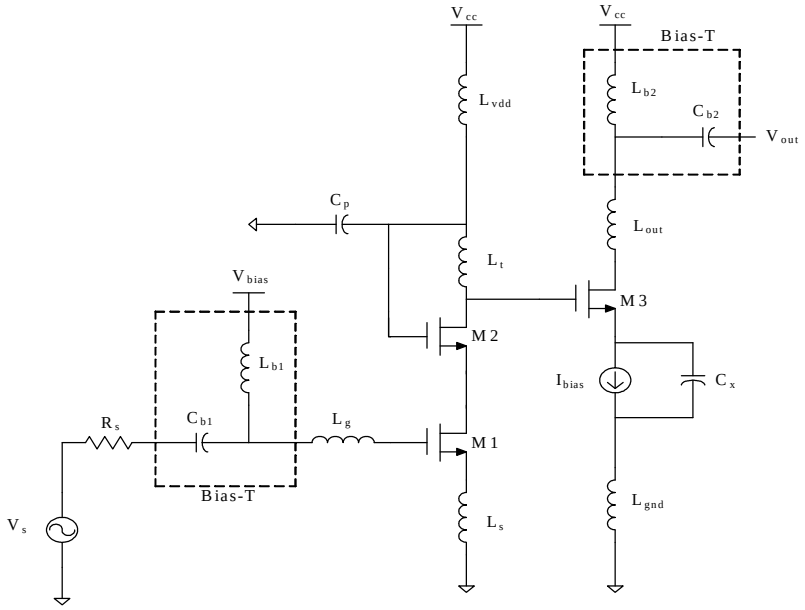

Figure 3.8 LNA whole circuit

3.4.2 Conventional Design Flow of LNA

In the study, the approach of the fixed power optimization is used to yield the minimum noise factor for a given power consumption under the assumption of input matched. According to the reference [12], the noise factor F can be expressed as follows:

$$F = 1 + \frac{gw_0 L}{3V_{sat}} \cdot P(r, P_D) \tag{3.26}$$

$$\text{with} \quad P(r, P_D) \approx \frac{P_D(1+\frac{d}{5g}) + 2|C|\sqrt{\frac{d}{5g}\, r^2} + \frac{P_0}{P_D}\frac{d}{5g}\, r^4}{P_0} \tag{3.27}$$

The optimized Q_L is hidden in the equation of (3.26). The noise figures as a function of Q_L with power consumption as parameters are plotted in Fig 3.9. This

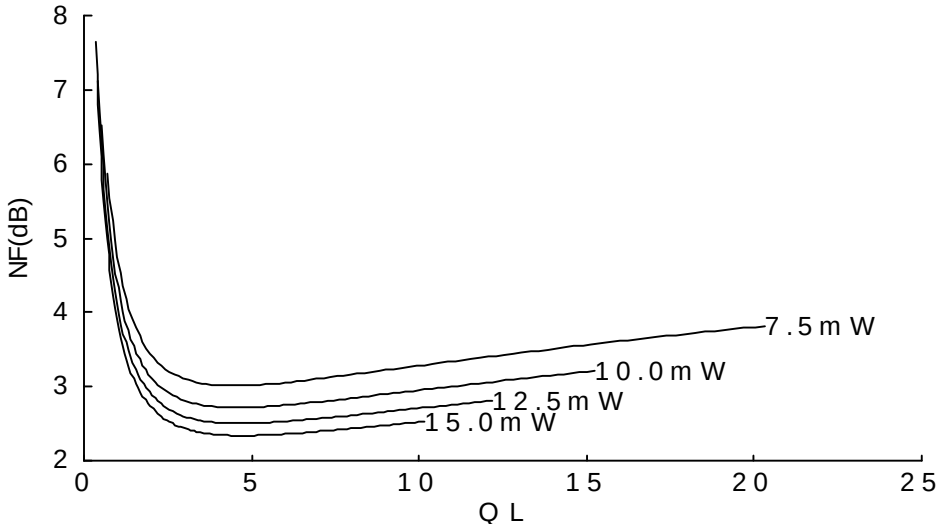

Fig 3.9 Device geometry for particular power consumption and noise figure

contour provides the guidance for choosing device geometry for particular power consumption and noise figure. Here, the power 15mW and Q_L =4.6 are choosed, then the noise figure 2.4 dB is also obtained. The optimum width of M1 device can be determined by the following equations[12]:

$$W_{M1,opt,P_D} = \frac{3}{2 \cdot w_0 \cdot L \cdot C_{ox} \cdot R_s \cdot Q_{Lopt}} \approx 465um$$

Where $w_0 = 15.08G\, rad/s$, $L = 0.37um$, $C_{ox} = 2.56\, mF/m^2$, and $Rs = 50\Omega$.

The actual width is only 450um, which is confirmed from SPICE simulation. The final design parameter of the whole LNA circuit is shown in Table 3.3.

Table 3.3 Design parameter of 0.5 um UMC DPDM technology

Frequency	2.4GHz
M1 Size	450um
M2 Size	220um
M3 Size	300um
Lt inductor	4nH
Lout inductor	4nH
Ls inductor	0.8nH
S21	20dB
NF	2.9dB
DC Power	24mW

3.4.3 Measurement and Discussion

Fig 3.10 shows the return loss S_{11} of LNA with the value of -24.7dB at 2.4GHz. On the S_{21} curve, the gain has a peak value of 12.47dB at 2.4GHz is plotted in Fig 3.11 which shows the large difference with simulation results. Both input noise and gain matching curves are shown in Fig 3.12. At 2.4GHz operation frequency, while the location of peak gain is also the place where the lower noise figure is improved than other frequency. From the noise figure chart, it shows 5.6 dB. The DC power from calculation is about 40mW.

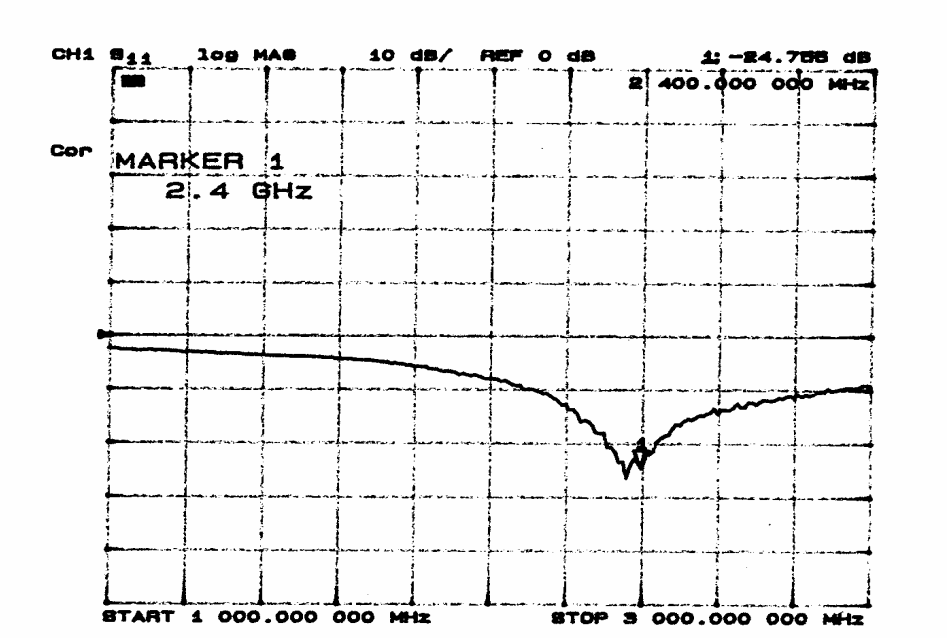

Figure 3.10 Return loss S_{11} of LNA

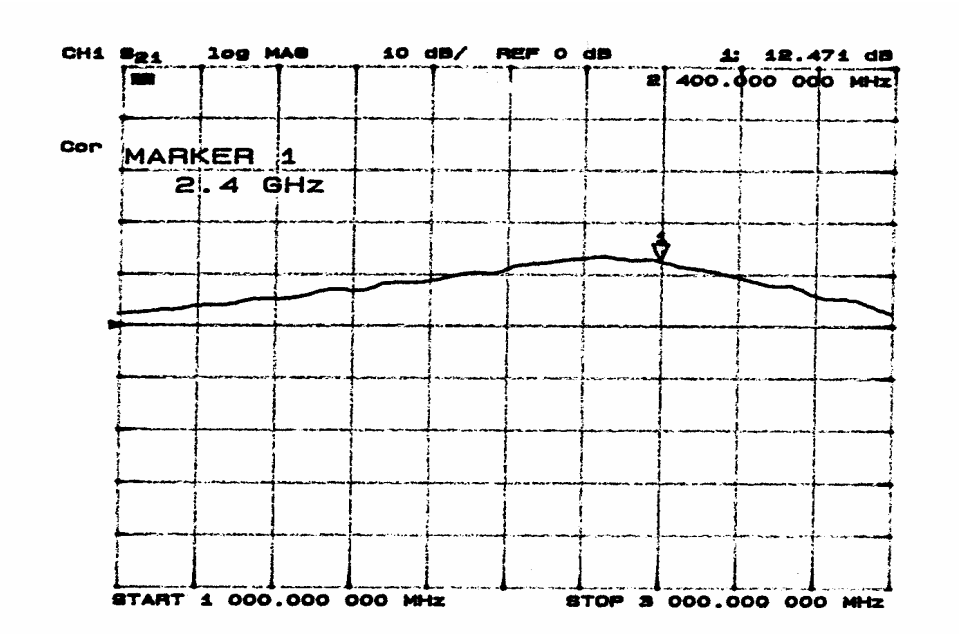

Figure 3.11 S_{21} of LNA

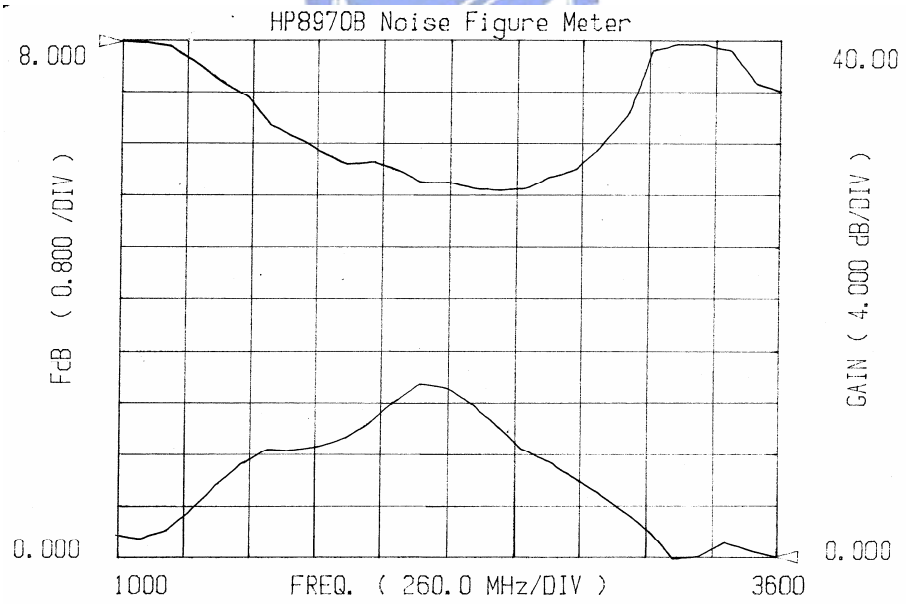

Figure 3.12 Input noise and gain matching curves

The value of noise figure with 5.6 dB is higher than the simulation of whole circuits with 2.9 dB. According our observation, the gate resistance is not included in the model from 0.5um UMC technology. Here, we should discuss the gate resistance

effect on the performance of the LNA [31,32]. The n-channel RF MOSFET with multifingers are fabricated with a 0.5um standard CMOS process. Devices with different bias are measured under the on-wafer probe station with the help of ATN-NP5B module. The HF measurement system consists of an HP8753D network analyzer, HP 85122A noise figure meter and HP4142I-V tester. The S parameters are measured for the devices at various bias conditions and de-embedded with a two step(open and short) procedure. The noise parameters are obtained under the same bias condition and the frequency range from 0.3GHz to 6GHz.The distributed gate resistance is given by [32]:

$$R_g = \frac{WR_{\square}}{3LN^2} \tag{3.28}$$

Where W is the total gate width of the device, L is the channel length, N is the number of gate fingers, $R_{\square}$ is the sheet resistivity of the polysilicon, and the factor 1/3 arises from a distributed analysis of gate. The samples are from UMC 0.5um DPDM process with sheet resistivity is $30\Omega/\square$ and the width 500um(20umX25), where N=25. To account for the high frequency behavior of R_g, the scattering parameters of NMOS are measured. The magnitude of R_g is extracted from S_{11}, from which the admittance matrix can be obtained. R_g is deduced by $R_g = \mathrm{Re}[1/Y_{11}]$. Fig 3.13 shows the measured S_{11} and those calculated with / without R_g in the BSIM3V3 model.

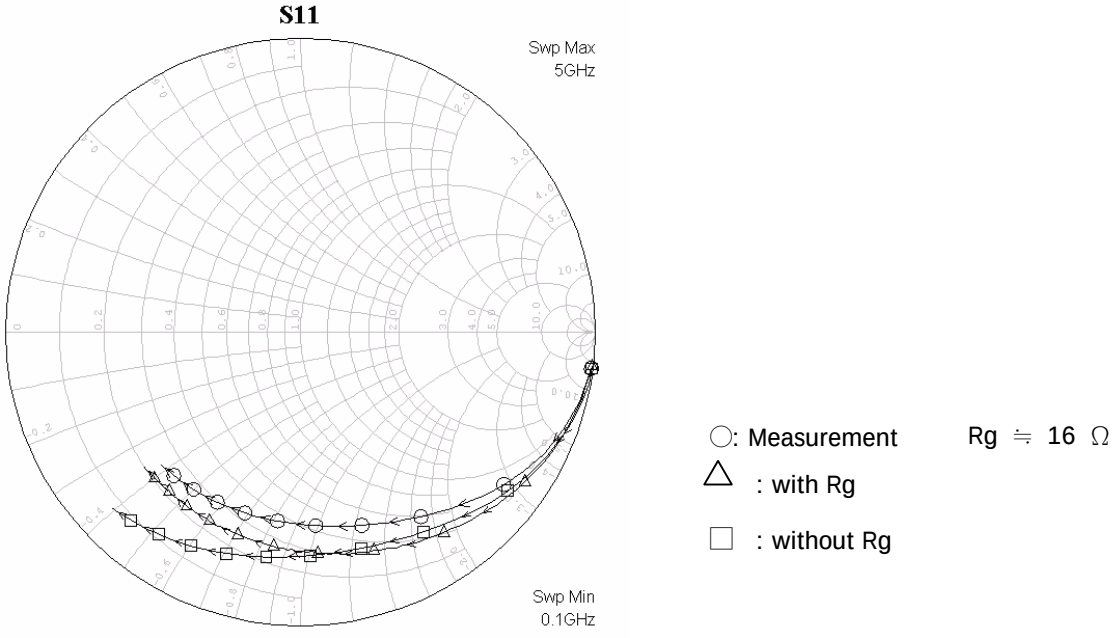

Figure 3.13 Measured S_{11} and those calculated with / without R_g in the BSIM3V3 model

The extracted and calculated R_g are equal to 18.6Ω and 16Ω, respectively. The contribution of the noise figure with $R_g = 16\Omega$ taking account in the model is about 1.21 dB. The transition loss for each SMA is 0.4 dB. Then the rest of noise figure is 0.71 dB(5.6-2.9-1.21-0.4X2=0.71), might be induced from L_s and L_g.

The gate resistance also degraded the performance of circuit, Fig 3.14 shows the measured and simulation results. The large deviation between BSIM3v3 model and measurement is that the gate resistance effect doesn't account in the model. Without Rg taking into account, the gain peak is overestimated by 4.6 dB. The modified BSIM3V3 model with gate effect taking into account shows good match with measured one. It means that gate resistance has great influence on the effect for input matching, isolation, noise figure and signal gain attenuated.

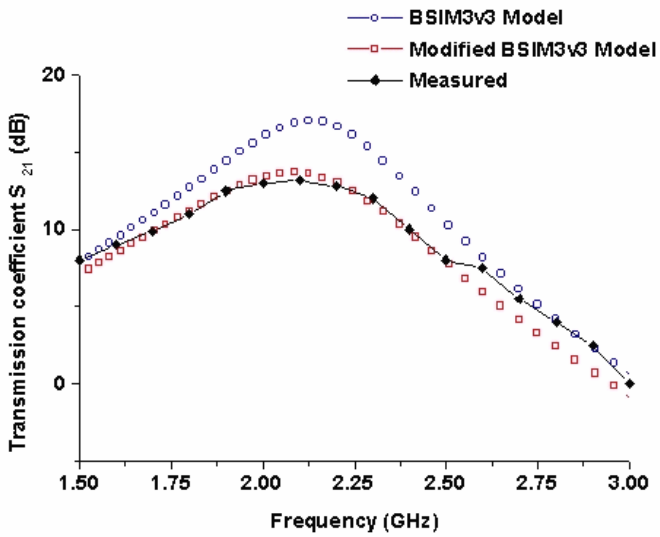

Figure 3.14 S_{21} measured and simulation results

3.4.4 Conclusions

The circuit design of 2.4GHz CMOS LNA with 12.5 dB gain and 5.6 dB noise figure was fabricated by the process of UMC 0.5um DPDM technology. The circuit with using SIF topology, the noise and input matching can be easily obtained, the gain and isolation are examined to be improved. Owing to the gate sheet resistance $30\Omega/\square$ is so high that it affects the input matching, noise figure and signal gain. Therefore, choosing lower sheet resistance of poly gate is necessary to RF design.

Chapter 4

Design of the CMOS Voltage-Controlled Oscillator

4.1 Introduction

A major challenge in the design of CMOS single-chip transceiver systems is the phase-locked-loop frequency synthesizer. The phase noise of the synthesizer is the most information transfer and is mainly determined by the phase noise of the Voltage Controlled Oscillator. LC-tank voltage controlled oscillators are a better choice than relaxation oscillators or ring oscillator to fulfill the required high frequency and noise specifications. A monolithic LC-tank VCO however, requires the integration of high quality passive devices, such as inductors and varactors in an inherently lossy CMOS technology. The design becomes even more challenging, when a high tuning range is necessary to provide the required frequency band over process tolerances. The combination of a wide tuning range and a low power supply voltage (meaning a low tuning voltage range) requires a high VCO gain (MHz/V), which makes the oscillator much more sensitive to voltage noise induced phase noise[32].

It is a well known that, from the Leeson's model, the single-sideband power spectral density is given by [9.11]:

$$L\{\Delta w\} = 10 \cdot \log\left[\frac{2FKT}{Ps} \cdot [1 + (\frac{w_o}{2Q_L \Delta w})^2] \cdot (1 + \frac{w_{1/f^3}}{|\Delta w|})\right] \quad \textbf{(4.1)}$$

where FKT is the effective thermal noise with the multiplicative factor F, K is Boltzmann's constant, T is the absolute temperature, P_S is the average power dissipated in the resistive part of the tank, Δw is the offset frequency, Q_L is the effective quality factor of the tank and is dominant by quality factor of spiral inductor, w_0 is the center frequency, and w_{1/f^3} is the corner of the flicker noise. This model describes well the shape of the spectrum. It suggests that a good oscillator needs high Q factor, low effective thermal noise and low flicker noise of the active device. While the factor F, also denoted as the device excess noise number, is a posterior fitting parameter derived from measured data[11]. These important parameters which have influence on phase noise will be discussed in the following section. The LC tank with complementary cross coupled pair circuit is used and shown in Fig. 4.1 [30.31]. The layout of die microphotograph is also shown in Fig. 4.2 by implementation with standard 0.35μm COMS process technology.

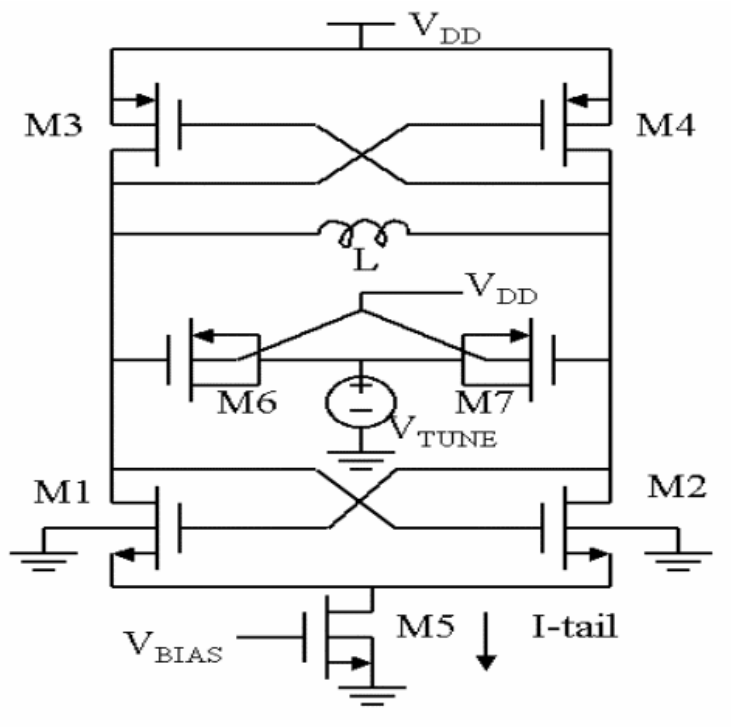

Fig. 4.1 The schematic of S35-90D VCO

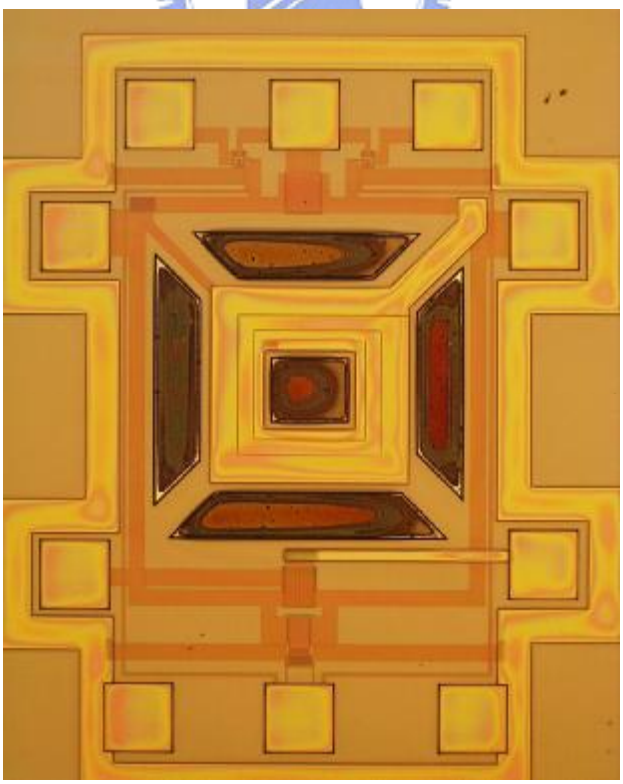

Fig. 4.2 The photograph of S35-90D VCO

4.2 Microwave Circuit Design of VCO

The traditional circuit design of microwave oscillator has separated two ways with one-port network and two-port network[1.8].

4.2.1 One-Port Negative Resistance Microwave Oscillator

Here we present some of the basic principles of operation for one-port negative oscillators; much of this material will also apply to two-port (transistor) oscillators.

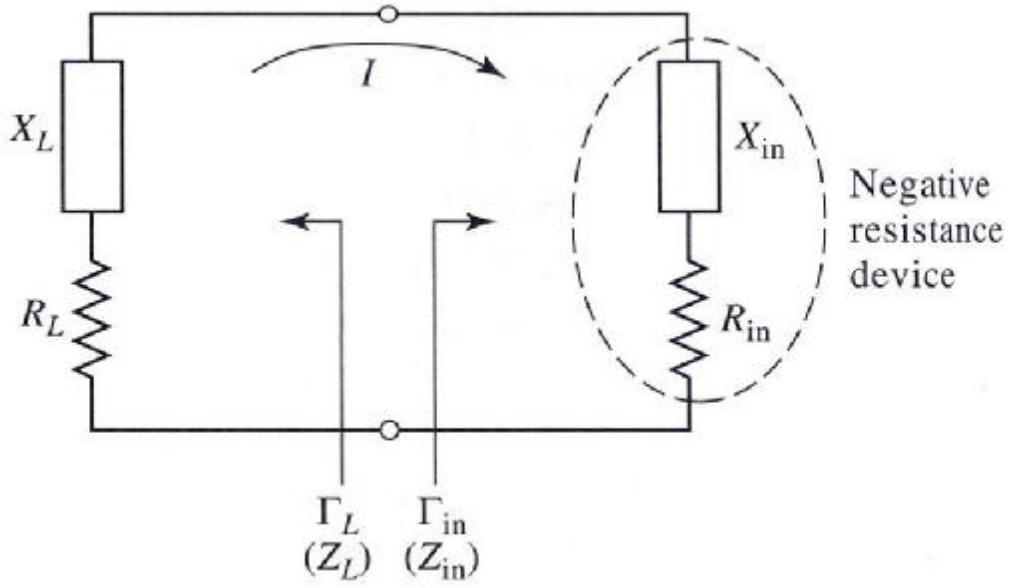

Fig. 4.3 Circuit for a one-port negative-resistance oscillator

Fig. 4.3 shows the canonical RF circuit for a one-port negative-resistance oscillator, where $Z_{in} = R_{in} + jX_{in}$ is the input impedance of the active device[1]. In general, this impedance is current (or voltage) dependent, as well as frequency dependent, which we can indicate by writing $Z_{in}(I,jw) = R_{in}(I,jw) + jX_{in}(I,jw)$. The device is terminated with a passive load impedance. $Z_L = R_L + jX_L$. Applying Kirchhoff's voltage law gives

$$(Z_L+Z_{in})I=0 \quad (4.2)$$

If oscillation is occurring, such that the RF current I is nonzero, conditions must be satisfied:

$$R_L + R_{in} =0, \quad (4.3)$$

$$X_L + X_{in} =0. \quad (4.4)$$

Since the load is passive. $R_L > 0$ and equation (4.3) indicates that $R_{in} < 0$. Thus, while a positive resistance implies energy dissipation, a negative resistance implies an

energy source. The condition of equation (4.3) controls the frequency of oscillation. The condition in equation (4.2), that $Z_L = -Z_{in}$ for steady-state oscillation, implies that the reflection coefficients Γ_L and Γ_{in} are related as

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} = \frac{-Z_{in} - Z_0}{-Z_{in} + Z_0} = \frac{Z_{in} + Z_0}{Z_{in} - Z_0} = \frac{1}{\Gamma_{in}} \tag{4.5}$$

The process of oscillation depends on the nonlinear behavior of Z_{in}, as follows. Initially, it is necessary for the overall circuit to be unstable at a certain frequency, that is, $R_{in}(I,jw)+R_L < o$. Then any transient excitation or noise will cause an oscillation to build up at the frequency, w. As I increases, $R_{in}(I,jw)$ must become less negative until the current I_0 is reached such that $R_{in}(I_0,jw_0)+R_L = 0$, and $X_{in}(I_0,jw_0)+X_L(jw_0) =0$. Then the oscillator is running in a stable state. The final frequency, w_0, generally differs from the startup frequency because X_{in} is current dependent, so that $X_{in}(I,jw) \neq X_{in}(I_0,jw_0)$.

Thus we see that the conditions of equation (4.3) and (4.4) are not enough to guarantee a stable state of oscillation. In particular, stability requires that any perturbation in current or frequency will be damped out, allowing the oscillator to return to its original state. This condition can be quantified by considering the effect of a small change, δI , in the current and a small change, δS, in the complex frequency $s = \alpha + j\omega$. If we let $Z_T(I,s) = Z_{in}(I,s) + Z_L(s)$, then we can write a Taylor series for $Z_T(I,s)$ about the operating point I_0,ω_0 as

$$Z_T(I,s) = Z_T(I_0,s_0) + \left.\frac{\partial Z_T}{\partial s}\right|_{s_0,I_0} ds + \left.\frac{\partial Z_T}{\partial I}\right|_{s_0,I_0} dI = 0 \tag{4.6}$$

since $Z_T(I,s)$ must still equal zero if oscillation is occurring. In equation (4.6), $s_0 = j\omega_0$ is the complex frequency at the original operating point. Now use the fact that $Z_T(I_0,s_0)= 0$, and that $\frac{\partial Z_T}{\partial s} = -j\frac{\partial Z_T}{\partial w}$, to solve equation (4.6) for $\delta s = \delta\alpha + j\delta\omega$:

$$ds = da + jdw = \left.\frac{-\partial Z_T/\partial I}{\partial Z_T/\partial s}\right|_{s_0,I_0} dI = \frac{-j(\partial Z_T/\partial I)(\partial Z_T^*/\partial w)}{\left|\partial Z_T/\partial w\right|^2} dI. \tag{4.7}$$

Now if the transient caused by δI and $\delta\omega$ is to decay, we must have $\delta\alpha < 0$ when $\delta I > 0$. Equation (4.7) then implies that

$$I_m\left\{\frac{\partial Z_T}{\partial I}\frac{\partial Z_T^*}{\partial w}\right\} < 0,$$

or $$\frac{\partial R_T}{\partial I}\frac{\partial X_T}{\partial w}-\frac{\partial X_T}{\partial I}\frac{\partial R_T}{\partial w}>0. \qquad (4.8)$$

For a passive load, $\partial R_L/\partial I=\partial X_L/\partial I=\partial R_L/\partial w=0$, so equation (4.8) reduces to

$$\frac{\partial R_{in}}{\partial I}\frac{\partial}{\partial w}\left(X_L+X_{in}\right)-\frac{\partial X_{in}}{\partial I}\frac{\partial R_{in}}{\partial w}>0. \qquad (4.9)$$

As discussed above, we usually have that $\partial R_{in}/\partial I>0$. So equation (4.9) can be satisfied if $\partial\left(X_L+X_{in}\right)/\partial w>>0$, which implies that a high-Q circuit will result in maximum oscillator stability. Cavity and dielectric resonators are often used for this purpose.

Effective oscillator design requires the consideration of several other issues, such as the selection of an operating point for stable operation and maximum power output, frequency-pulling, large-signal effects, and noise characteristics.

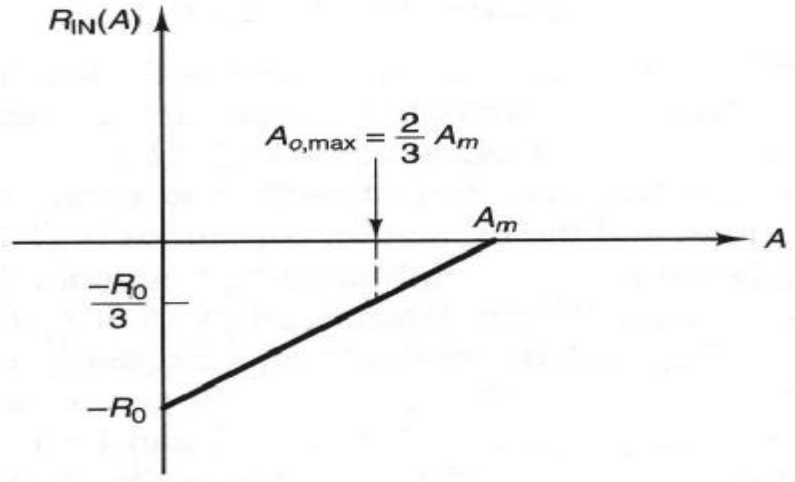

Fig. 4.4 Linear variation of the negative resistance as a function of the current amplitude

In a given oscillator design, the input impedance of the active device is known for small-signal conditions. A practical way of designing R_L is to select the value of R_L for maximum oscillator power. If the magnitude of the negative resistance is a linearly decreasing function of A which shows in Fig. 4.4, we can express $R_{in}(A)$in the form

$$R_{IN}(A)=-R_0(1-\frac{A}{A_M}) \qquad (4.10)$$

where $-R_0$ is the value of $R_{IN}(A)$ at A = 0,and A_M is the maximum value of A.

In Fig. 4.3, the power delivered to R_L by R_{IN} (for $A<A_M$) is

$$P=\frac{1}{2}\mathrm{Re}\left[VI^*\right]=\frac{1}{2}|I|^2|R_{IN}(A)|=\frac{1}{2}A^2R_0\left[1-\frac{A}{A_M}\right]$$

Hence, the value of A that maximizes the oscillation power is found from

$$\frac{dP}{dA} = \frac{1}{2} R_0 \left[2A - \frac{3A^2}{A_M} \right] = 0$$

which gives the desired value of A, denoted by $A_{o,max}$, that maximizes the power. That is,

$$A_{o,\max} = \frac{2}{3} A_M$$

At $A_{o,max}$, the value of $R_{IN}(A_{o,max})$ is

$$R_{IN}(A_{o,\max}) = -\frac{R_0}{3}$$

Hence a convenient value of R_L, which maximizes the oscillator power, is

$$R_L = \frac{R_0}{3} \tag{4.11}$$

Observe that equation (4.11) is valid when the negative input resistance varies linearly with amplitude. In practice, the selection of R_L according to equation (4.11) produces good results.

4.2.2 Two-Port Network of Microwave Oscillator

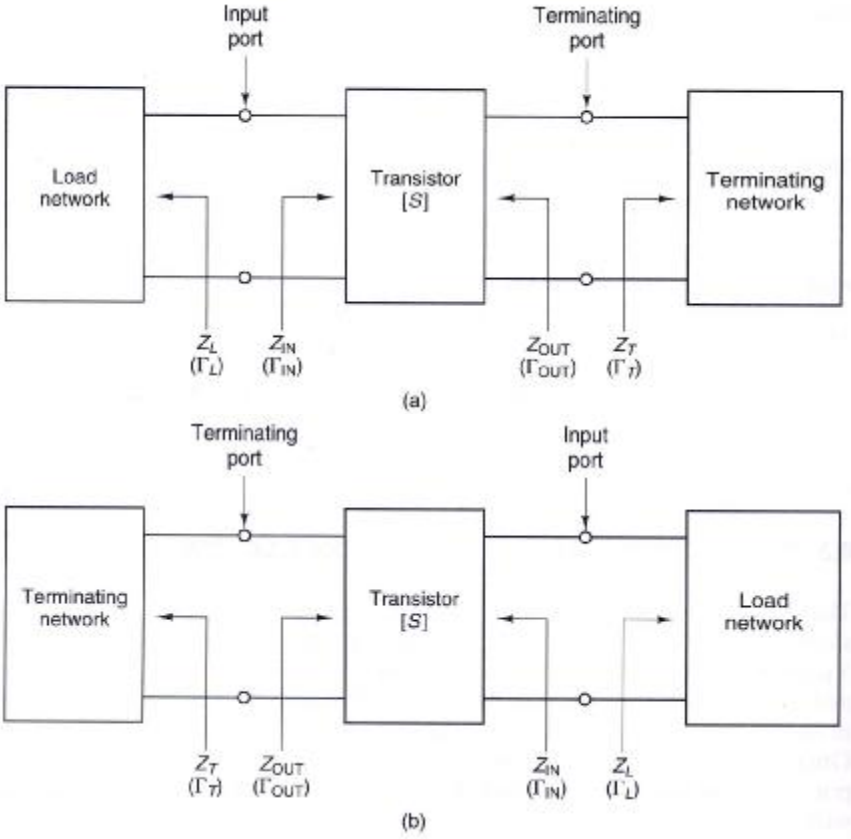

Fig. 4.5 Two-port oscillator model

The general block diagrams for two-port negative-resistance oscillators are shown in Figs. 4.5(a) and 4.5(b)[1.8].The transistor network is characterized by its S parameters, Z_T is the terminating network impedance, and Z_L is the load impedance. Observe the notation used in Figs. 4.5(a) and 4.5(b), which shows that in an oscillator either port of the transistor can be used as the terminating port. Once the terminating port is selected, the other port is referred to as the input port. The load-matching network is connected to the input port, in agreement with the one-port notation used in Fig. 4.3.

When the two-port is potentially unstable, an appropriate Z_T permits the two-port to be represented as a one-port negative-resistance device with input impedance Z_{IN}, as shown in Fig. 4.3. The conditions for a stable oscillation are given by equation (4.3), (4.4), and (4.9). To start the oscillation, the value of R_L, is selected according to equation (4.11) (i.e., $R_L = R_0/3$ or, in general, $R_L = |R_{IN}(0,\omega)|/3$).

When the input port is made to oscillate, the terminating port also oscillates. The fact that both ports are oscillating can be proved as follows.

The input port is oscillating when

$$\Gamma_{IN}\Gamma_L = 1 \tag{4.12}$$

and from $\Gamma_{IN} = S_{11} + \dfrac{S_{12}S_{21}\Gamma_T}{1-S_{22}\Gamma_T} = \dfrac{S_{11} - \Delta\Gamma_T}{1-S_{22}\Gamma_T}$ to obtain

$$\Gamma_T = \frac{1-S_{11}\Gamma_L}{S_{22}-\Delta\Gamma_L} \tag{4.13}$$

Also, from $\Gamma_{out} = S_{22} + \dfrac{S_{12}S_{21}\Gamma_S}{1-S_{11}\Gamma_S} = \dfrac{S_{22} - \Delta\Gamma_S}{1-S_{11}\Gamma_S}, \Gamma_S = \Gamma_L$ we get equation

$$\Gamma_{OUT} = \frac{S_{22}-\Delta\Gamma_L}{1-S_{11}\Gamma_L} \tag{4.14}$$

and from equation (4.13) and (4.14) it follows that

$$\Gamma_{OUT}\Gamma_T = 1$$

which shows that the terminating port is also oscillating.

A design procedure for a two-port oscillator is as follows[8]:

1. Use a potentially unstable transistor at the frequency of oscillation ω_o.
2. Design the terminating network to make $|\Gamma_{IN}| > 1$. Series or shunt feedback can be used to increase $|\Gamma_{IN}|$.
3. Design the load network to resonate Z_{IN}, and to satisfy the start of oscillation condition in equation (11).That is, let

   $$X_L(w_0) = -X_{IN}(w_0) \tag{4.15}$$

   and

$$R_L = \frac{R_0}{3} \quad \text{or, in general,} \quad R_L = \frac{|R_{IN}(0,w)|}{3} \tag{4.16}$$

This design procedure is popular due to its high rate of success. However, the frequency of oscillation will shift somewhat from its designed value at ω_0. This occurs because the oscillation power increases until the negative resistance is equal to the load resistance and X_{in} varies as a function of A (i.e., as a function of the oscillation power). Also, there is no assurance that the oscillator is providing optimum power.

4.3 Integrated Circuit Design of Complementary Cross-Couple Pair VCO

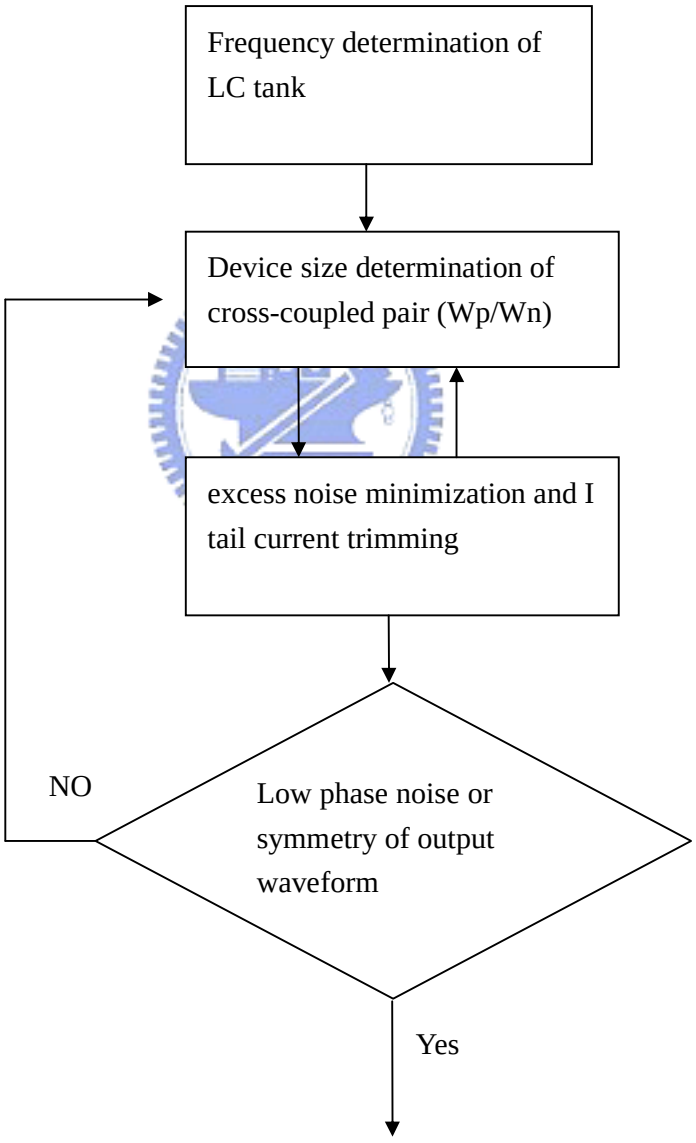

Fig. 4.6 LC complementary cross-coupled design procedure

Voltage-controlled oscillator (VCO) is the most challenging part of a monolithic RF frequency synthesizer. The phase noise and power consumption are key factors. The modified RF model is taken into account [36] for precision because the BSIM3v3 model is not suitable for RF circuits design. A simple rule is summarized for the low phase noise VCO design. Fig. 4.6 shows the block diagram in process for good phase noise design of LC tank cross-couple pair VCO. First, the dominant oscillator frequency can be determined by LC tank. The value of high Q inductor must be selected firstly. On the following, the capacitive value determined by varactor MOS and formed the inductive properties of impedance. Second, the complementary cross coupled pair circuit can supply the sufficient power to generate the LC tank oscillation and also cancel the loss of tank with necessary negative resistance. Third, the tail current should be adjusted to make all devices working at the saturation region. And it also can be trade off between output voltage and power. Then, the excess noise minimization can be done simultaneously[37].

4.3.1 On-Chip Spinal Inductor Design

In this section, we based on some design guideline to implement the good quality factor of RF spiral inductor because of demand in integration of transceiver. The availably of good quality integrated inductors is crucial in the RF integrated circuits. Parasitic effects such as losses of the silicon substrates and the series resistance of the metal strip degrade the performance. The use of the silicon micromachining techniques is the solution of substrate loss [38]. It removes the substrate under the spiral inductor and significantly increases both the self-resonant frequency (SRF) and quality (Q) factor. However, it needs extra post processing. The other solution is based on the layout optimization to minimize the series resistance [39.40]. The resistance is from ohmic losses, duo to conduction currents, and magnetically induced losses, due to eddy currents. The ohmic losses relate to the resistance of metal strip, which is inversely proportional to the width of the metal strip. The magnetically induced losses depend on the time derivative of the magnetic-field flux through the metal strip, which is proportional to both frequency and metal strip width. An optimum in metal strip width is performed to minimize the series resistance and maximize the Q factor. From equation (4.1), the larger quality factor value is, the smaller phase noise is. The fabrication of the planar inductor plays an important role to the CMOS VCO integrated circuit design because of the quality, losses and phase noise consideration.

The concept of layout optimization for planar inductor, if each turn width of coil is the same, R_S has the minimum for the same width W_{opt} given by

$$w_{opt} = \sqrt[3]{\frac{r_s(f)\sum_{n=1}^{N} l_n}{2Cf^2 \sum_{n=1}^{N} g_n{}^2 l_n}} \tag{4.17}$$

The on-chip constant width RF spiral inductor in 0.35 μm CMOS technology has been developed in our laboratory with three turns, constant width of 20 μm, spacing of 1 μm, and the length of the first turn (the most inner turn) of 564 μm [48]. Therefore, the constant C can be found using the above experimental information. Once the fitted parameter C is known, the optimum metal strip width $w_{opt,n}$ in each turn can be obtained as following

$$w_{opt,n} = \sqrt[3]{\frac{r_s(f)}{2Cf^2 g_n{}^2}} \tag{4.18}$$

The optimum metal strip width in each turn can be obtained as w_1=14.1823 μm, w_2 =22.5663 μm, w_3 =40.9718 μm. The simulated inductance and the Q factor are shown in the Fig. 4.7. The layout of the spiral inductor is shown in Fig. 4.8. The measurement of the inductance and the Q factor between the constant width and optimum width are Fig. 4.9. The Q factor of optimum width spiral inductor is enhanced about 25% with the same inductance 3.3nH. The difference between the measurement and simulation may be caused from process deviations.

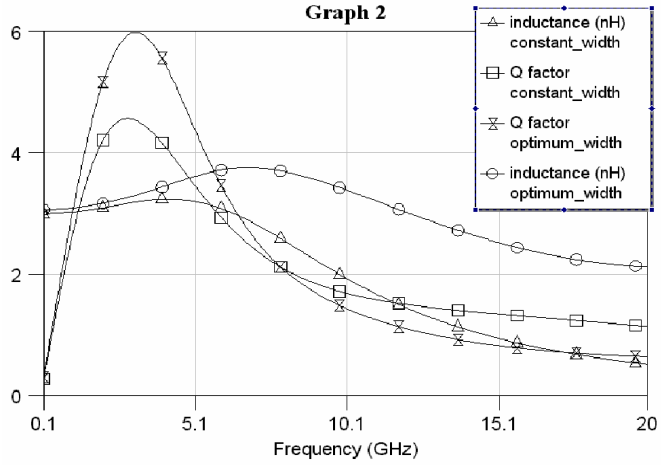

Fig. 4.7 The simulation of the inductance and the Q factor

Fig. 4.8(a) Fig. 4.8(b) Fig. 4.8(c)

Fig. 4.8 (a) Constant width spiral inductor

Fig. 4.8 (b) Optimum width spiral inductor

Fig. 4.8 (c) Dummy pad for de-embedding

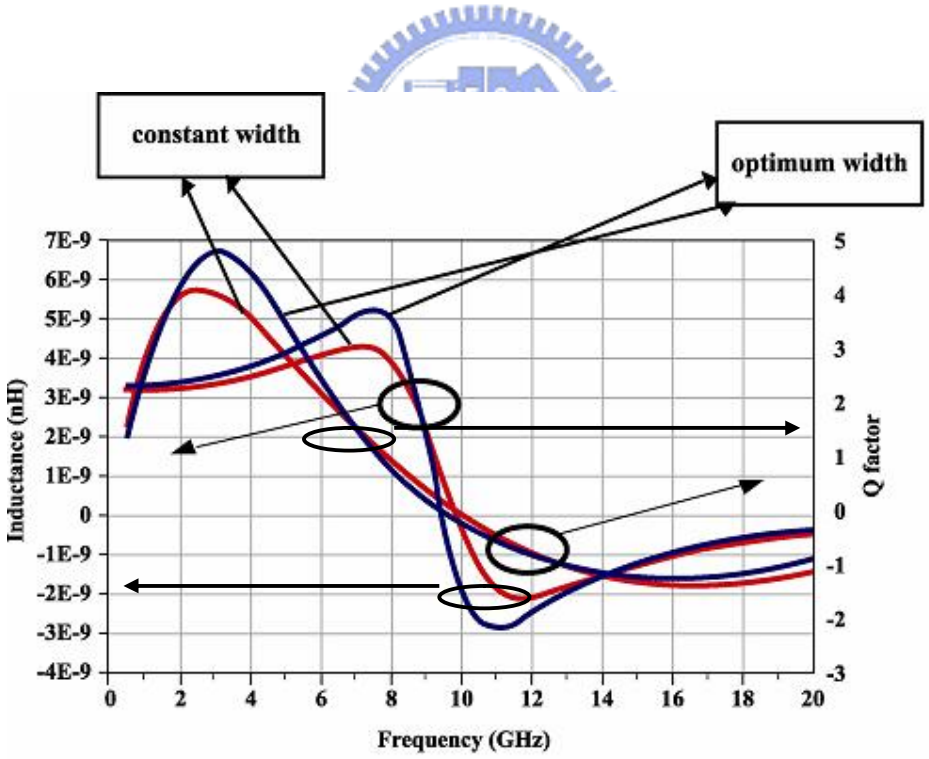

Fig. 4.9 The measured Q factor comparison between constant width and optimum width

4.3.2 Frequency Tuning by MOS Varactor

In a LC-tank VCO, the varactor is used as the tuning element. The tuning range is strongly related to the ratio of the varactors. Varactors with P+ to N-well junction have been traditionally realized by the reverse-biased diodes. When tuning with P+/N-well diodes with cathodes connected to the control voltage, the diodes will start to be forwardly biased when the tuning voltage reaches around 0.5V[41]. Forwardly biasd diodes severely degrade the oscillator's phase noise, due to extra 1/f and resistive noise. Furthermore, variable diode varactors have a more linear tuning characteristic with less gain, which results in a more limited tuning range. This type is not used in our design. For the implementation of a MOS capacitor with large tuning range, together with a much lower parasitic resistance, the use of the MOS device in the depletion and accumulation regions only can be a better solution[42.43.44]. This class of MOS capacitor is referred as accumulation-mode MOS capacitor. It reveals that the D-S diffusions (p+-doped) are removed. At the same time, the bulk contacts (n+) can be implemented to the left side of D-S which minimizes the parasitic n-well resistance of the device. Unfortunately, this device is not supported by the foundry and is not used here. It is well known that an MOS transistor with drain, source, and bulk tied together realizes an MOS capacitor with capacitance value depend on the voltage V_{BG} between bulk (B) and gate (G). The MOS varactor is shown in Fig. 4.10. According to the amplitude of V_{BG}, the operation of MOS varactor can be separated into strong inversion region and accumulation region. The tuning characteristic for the p-MOS capacitor with D≡S≡B is illustrated with Hspice simulation Fig. 4.11. It should be noted that Fig. 4.11 shows the CMOS v.s. V_{BG} characteristic for a very small signal superimposed on the bias voltage V_{BG}. For the MOS varactor is used in a VCO, the signal at the transistor gate is large such that the tuning capability of the circuit is impaired by the nonmonotonicity of Cmos[48]. One way to obtain an almost monotonic function for CMOS is by ensuring that the transistor does not enter the accumulation region for a very wide range of values of V_G. This is accomplished in removing the connection between D-S and B, and connecting B to the highest dc-voltage available in the circuit. The result via Hspice simulation is shown in Fig. 4.12. It is clear that the tuning range of the p-MOS capacitor with $V_B=V_{DD}$ is much wider than that in Fig. 4.11. This topology of the MOS is referred to the inversion-mode MOS [42]. It should be noted that an equally large tuning range can be obtained with an n-MOS capacitor with floating D-S and grounded B. The n-MOS capacitor has the further advantage of a lower parasitic resistance than the p-MOS varactor, but has the drawback of being more sensitive to substrate-induced noise, since it cannot be implemented in a separate p-well. Consequently, for designing a VCO, we would choose the p-MOS varactor to lower phase noise.

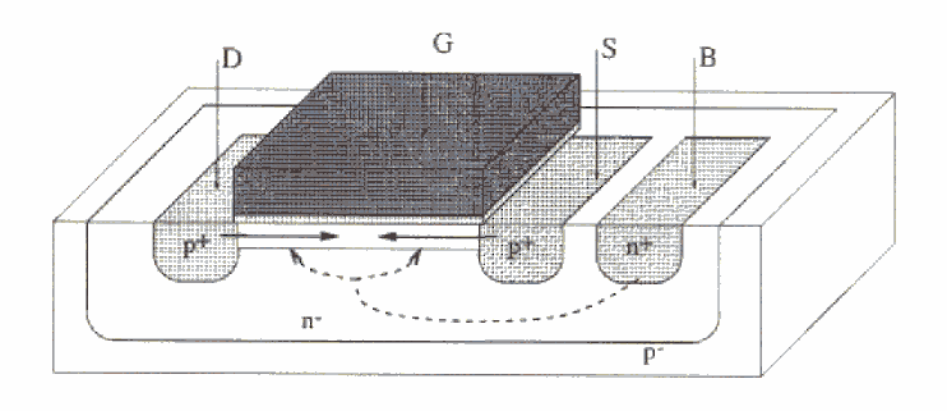

Fig. 4.10 Inversion-mode capacitor

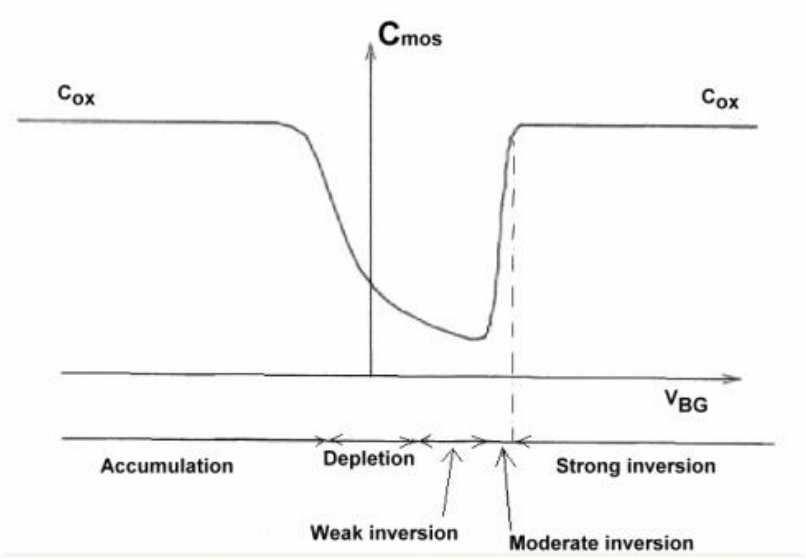

Fig. 4.11 Tuning characteristic for the p-MOS capacitor with D≡S≡B

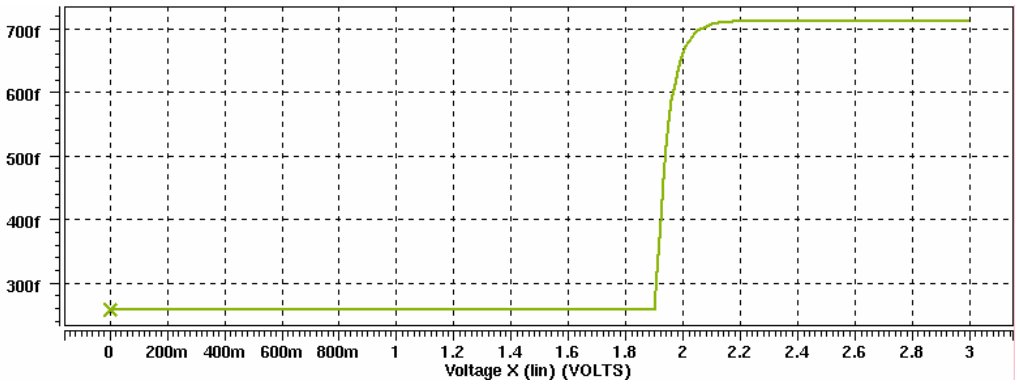

Fig. 4.12 tuning characteristics of the p-MOS via Hspice simulation with D≡S, B=Vdd , W/L=400um/0.35um

4.4 Simple Description VCO Circuit

The schematic of VCO is shown in Fig. 4.1 (a). The circuit consists of three divisions : M1~M4 is the cross-coupled pair, L and M6~M7 is the LC tank, and M5 is tail-current source. On chip spiral inductor as well as inversion-mode MOS varactor is used to form LC-tank. Here, the extra p-MOS pair is employed to form the complementary cross-coupled pair VCO to enhance the negative resistance. The cross-coupled pair circuit provides negative resistance to cancel the resistance generated by LC-tank. The concept of positive feedback in the cross-coupled pair is illustrated in Figure 4.13. If the signal at A point is 0° ,through phase shift from gate of M1 to drain is 180° . The extra phase shift from the feedback loop between gate to drain of M2 is also 180° . Therefore, the whole loop phase shift is 0° to form a positive feedback. The parallel tank plays the role of frequency selection. According to the Barkhausen criterion, oscillation occurs at the frequency for which the magnitude of the loop gain is larger than one. This implies that the pair transconductance has to overcome the tank loss at resonance. The size of cross-coupled PMOS transistors is twice to their NMOS counterparts due to hole's mobility. More important, the PMOS devices allow better symmetry to be achieved on each of the tank nodes by the positive and negative drive strength. It is this attention to symmetry on both the full circuit and each half circuit that reduces phase noise. Designing the cross-coupled pair of NMOS and PMOS transistors in saturation region is needed. Otherwise, the oscillator swing was to become voltage limited and thus, the cross-coupled pairs would no longer present a negative resistance to the LC tank. Moreover, the tail-current source M5 is used to adjust the tank amplitude which also affect the phase noise of VCO [34]. However, the I_{tail} can influence the power consumption. From above reasons, the trade-off between phase noise and power consumption have to be taken into account significantly.

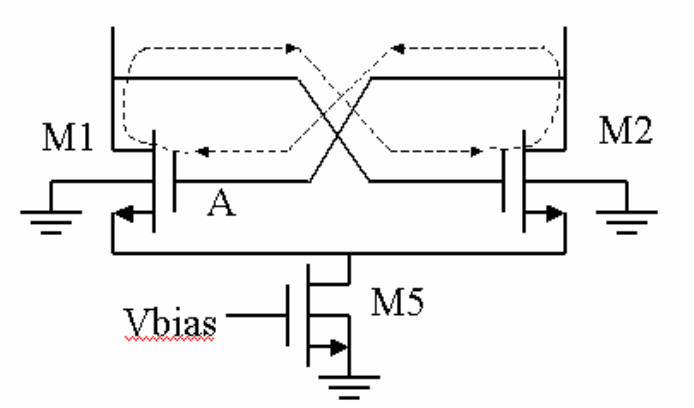

Fig.4.13 Illustration of positive feedback

4.5 Prediction Method of Phase Noise

4.5.1 Prediction of Phase Noise

Phase noise prediction of the integrated LC voltage-controlled oscillators (VCOs) is an interesting topic of research. A general method is proposed which is capable of making an effective prediction of F, device excess noise number, and acquiring the phase noise of oscillators accurately.

Integrated LC VCOs are common functional blocks in modern wireless communication systems and are used as local oscillators to convert up or down the RF signals. Phase noise of the VCO is one of the important issues regarding to the receiving quality. Active device noise usually contributes a significant portion to phase noise in the oscillator. It is well known that, from the Leeson's model, the single-side power spectral density is given by Eq. (4.1). Recently, the phase noise behaviors are studied by many authors [11.34.40.45]. In this study, the method of predicting the excess noise number is indicated.

Actually, the factor F is attributed from two parts, one is the total noise sources NF in all active devices, and the other is from the mixing mechanism in oscillation under large-signal operation. The former one is closely related to the noise figure of each device. If the multiplication factor is denoted as Km, then the excess noise number F can be given by[42]

F(dB)= NF +Km (4.19)

The total noise voltage density far from the corner frequency appeared at one of the output drain in the cross-coupled oscillator is given by

$$\frac{\overline{V_c^{\,2}}}{\Delta f} = 2\left(\frac{4KTg}{g_{m,n}} + \frac{4KTg}{g_{m,p}}\right) + \frac{4KT}{g_{\tan k}} \tag{4.20}$$

where g_m is the transconductance of transistor[4] and g is 2~3 for short channel effect due to hot-electron [7]. The subject index n or p is the nMOS or pMOS, respectively. The first two terms are from active deices. Because of the symmetry, the noise level is twice. The third one is attributed from the equivalent parallel tank conductance $g_{\tan k}$ caused by ohmic losses in the metal and substrate. Then the total device noise figure, NF , is calculated from

$$NF = 10\log\left(1 + \frac{\overline{V_c^{\,2}}/\Delta f}{4KT \cdot 50\Omega}\right) \tag{4.21}$$

The up-conversion factor Km is then obtained by finding the ratio of side band level to excited source level, ie mark B/mark A in Fig. 4.15. Accordingly, F can be predicted by Eq. (4.19). The upconversion factor Km is 4dB in our case of optimum

situation. It may be higher value move than 10 dB from the worst case.

4.5.2 Phase Noise Minimization

As indicated in [35], the smaller $L^2 g_L{}^2 / I_{bias}$ is, the better phase noise is. When the inductance decreases, the equivalent parallel conductance of spiral inductor g_L is larger but $L^2 g_L{}^2$ is smaller, which is shown in Fig. 4.14(a) and Fig. 4.14(b),

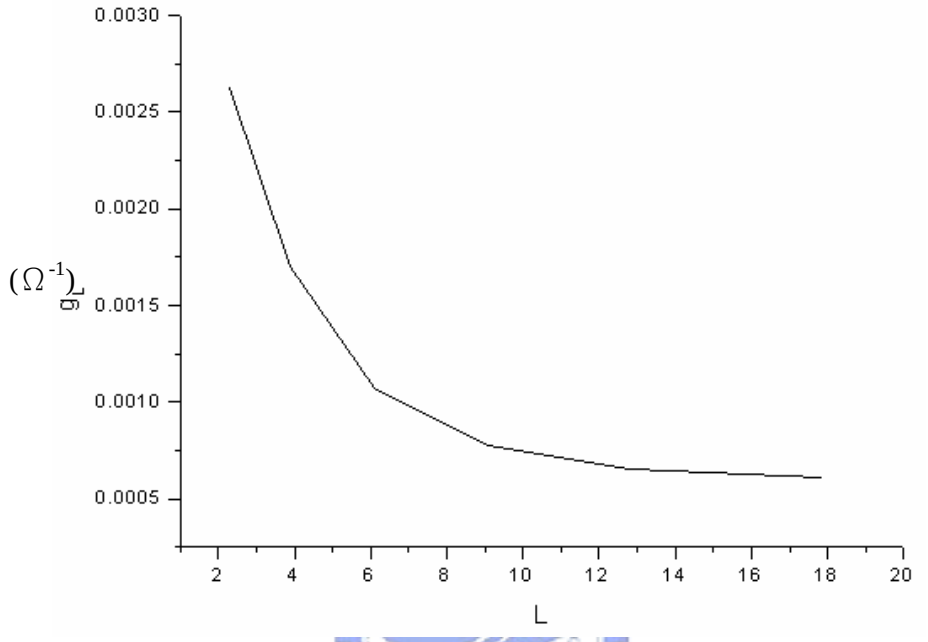

Fig. 4.14(a) g_L vs. inductance

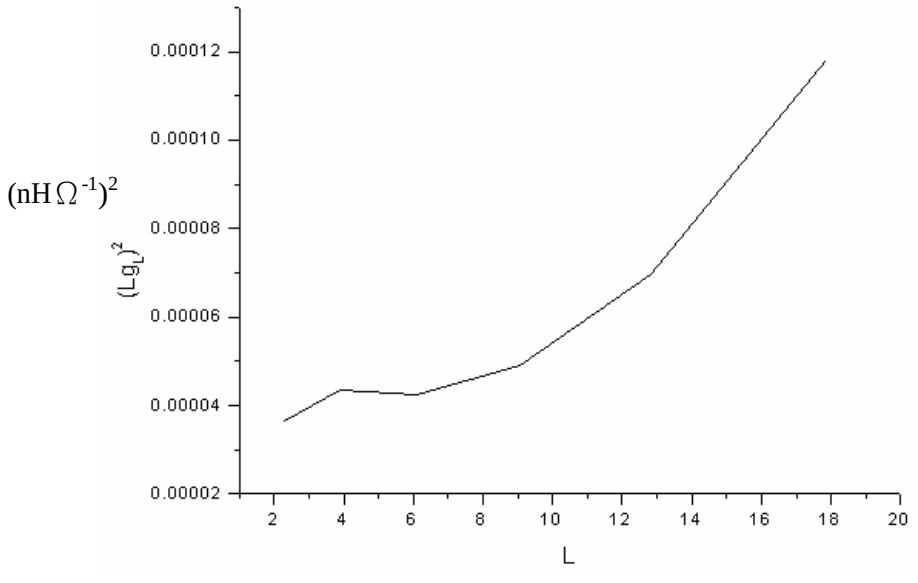

Fig. 4.14 (b) $L^2 g_L{}^2$ vs. inductance

respectively. The minimum of $L^2 g_L{}^2$ is searched in each bias current I_{bias} by decreasing the inductance (refer to Fig. 4.14(b)) and adjusting the cross-coupled pairs size to keep the same oscillation frequency. If $L^2 g_L{}^2$ is smaller than the minimum, g_L is too larger (refer to Fig. 4.14(a)) to meet start-up condition. The start-up condition with a small-signal loop gain of at least $a_{\min}$ can be expressed as $g_{active} \geq a_{\min} g_{\tan k}$ where $g_{\tan k}$, g_{active} are tank loss and effective negative conductance, respectively. The conductance $g_{\tan k}$ is dominant by equivalent parallel conductance of spiral inductor g_L. Then a small-signal loop gain is selected to equal to 7. A symmetric active circuit with the same transconductance of cross-coupled pairs is used to get the better $1/f^3$ corner of phase noise [36].

There are two variables, bias voltage and tail current source size (W/L), to control the bias current I_{bias} . The MOS flicker noise is

$$\frac{\overline{i_n^2}}{\Delta f} = \frac{K}{f}\frac{g_m{}^2}{WLC_{ox}{}^2} \propto \frac{g_m{}^2}{W} \tag{4.22}$$

By varying the bias voltage and tail current source size (W/L) with keeping the bias current constant, the optimum situation with the lowest $g_m{}^2/W$ is searched. PMOS is used for the tail current source because of low flicker noise.Therefore, the LC-tank components and bias current can be determined roughly from the minimum of $L^2 g_L{}^2 / I_{bias}$.

Then, the size of cross-coupled pair can be fine tuned as follows by current source injection method. As indicated by [45.47], a small-signal sinusoidal current is injected at a proper frequency f_m into the output node and the signal is up-converted into two sidebands at $f_o \pm f_m$ due to the mixing mechanism in oscillation under large-signal operation as shown in Fig. 4.15. The larger the difference between sidebands and carrier is, the more symmetric the waveform is [45.46]. It implies the effect of nonlinear mixing is minimized. By varying the drain current and the size of cross-coupled pairs slightly with g_m keeping constant, the optimum situation with

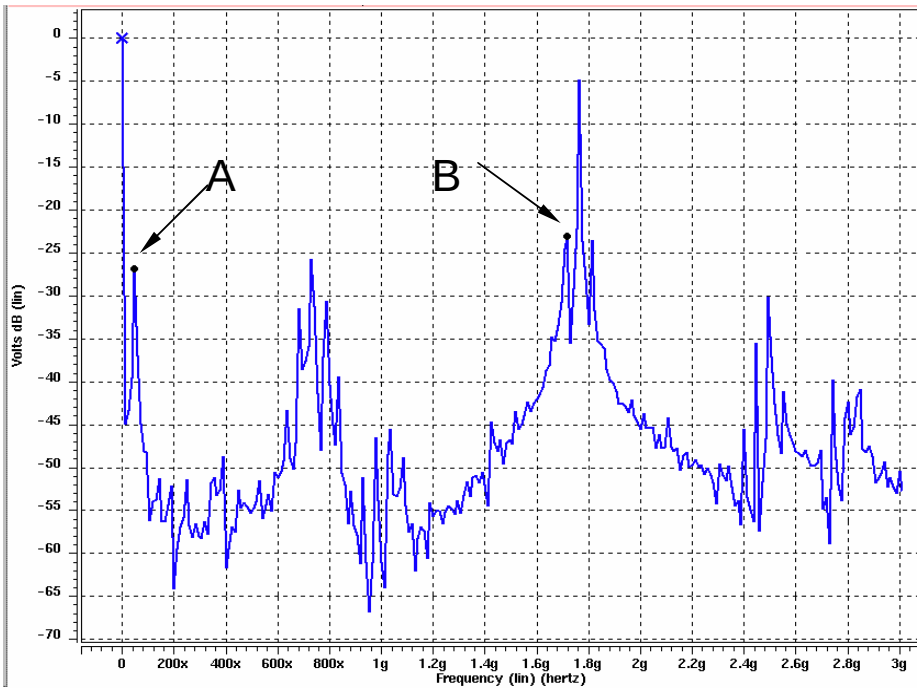

Fig. 4.15 The spectrum with current injection at f_m

the lowest side band level is attained. The situation in terms of sideband to carrier ratio is shown in Fig. 4.16. The peak of the curve is the best choice.

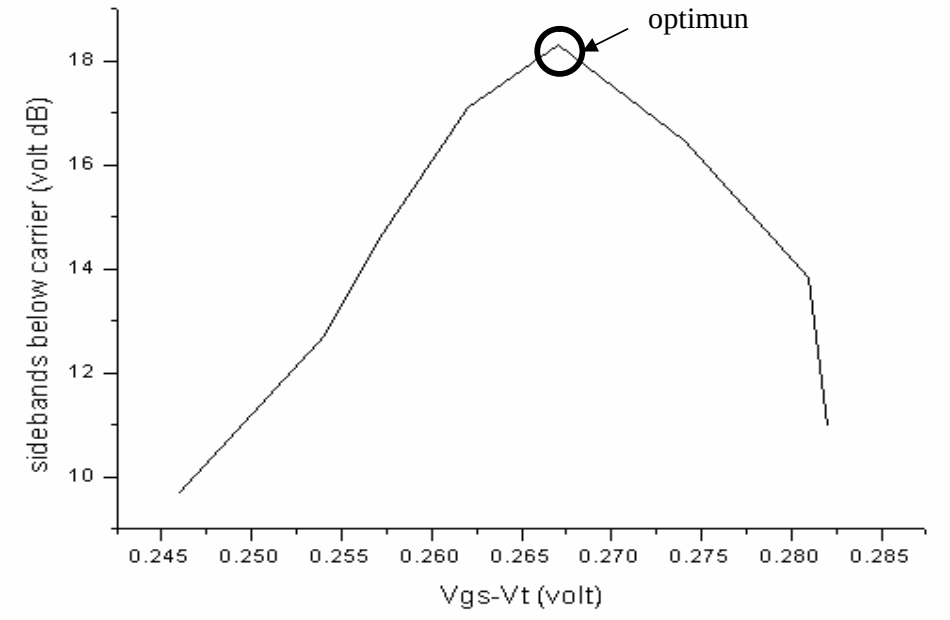

Fig. 4.16 The optimum situation with the lowest side band level

Therefore, the procedure to design a low phase noise VCO is as follows:

1. Choose the optimum width of the inductance to increase the Q factor.

2. Determine the LC-tank component and I_{bias} roughly.

3. Select a size of tail current source to keep the desired I_{bias} by minimizing its

   flicker noise $\frac{\overline{i_n^2}}{\Delta f} = \frac{K_f \cdot g_m^2}{f \cdot W \cdot L \cdot C_{ox}} \propto \frac{g_m^2}{W}$

4. The current injection method [45.46.47] on the output of the cross-coupled pairs to obtain the minimum up-conversion factor is used. By varying the drain current and the size of cross-coupled pairs slightly with g_m keeping constant, the optimum situation of the operating point is located at the larger difference between the V_{GS}-V_T value and the sideband to carrier ratio.

4.6 Simulation and Measurement

A 2 GHz fully integrated complementary cross-couple pair LC tank VCO has been developed in our laboratory with constant width spiral inductor shown in Fig. 4.8 (a). The optimum width spiral inductor shown in Fig. 4.8 (b) is substituted and is repeated in 0.35um CMOS technology again[48.49]. Fig. 4.1 and Fig. 4.2 are the schematic and the photograph of the VCO. The aspect ratio of the NMOS and PMOS cross-coupled pair is 300μm/0.35μm and 600μm/0.35μm, respectively. The aspect ratio of the tail current source is 200μm/0.35μm. The aspect ratio of the varactor is 400μm/0.35μm. The detailed size of the device is also shown in table 4.1.

Table 4.1 Device size of cross-coupled pains VCO circuit

MOSFET Size($L \times W \times M$)	0.35um CMOS technology
M1,M2	0.35 um x 5 um x 60
M3,M4	0.35 um x 5 um x120
M5	0.35 um x 5 um x 40
M6,M7	0.35 um x 5 um x 80

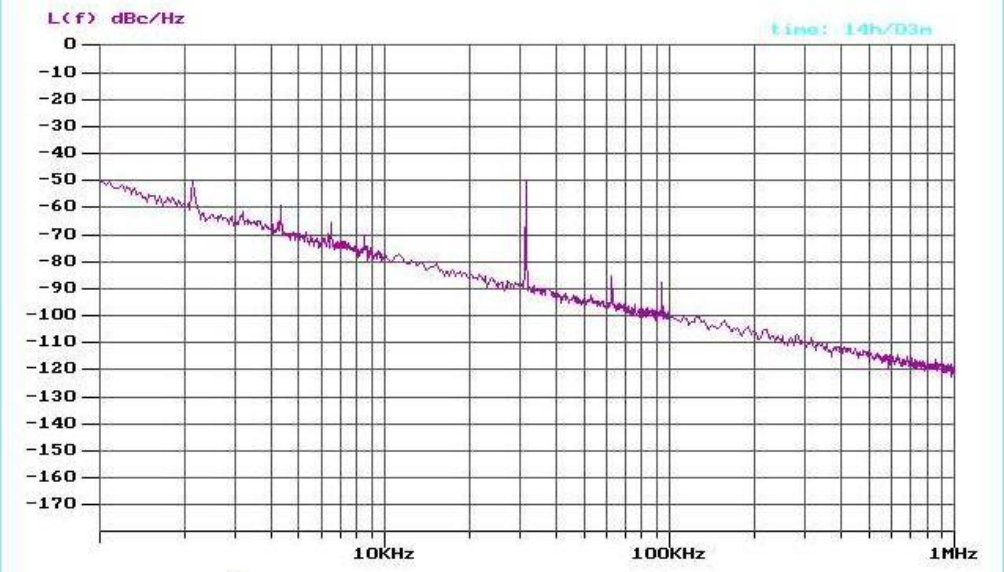

Fig. 4.17 The phase noise measurement of the S35-90D VCO

The upconversion factor, Km, is equal to 4dB. The noise figure NF from Eq. (4.21) is equal to 9.241(dB) with g =2.5, $g_{m,n}$ =30m, $g_{m,p}$ =22m, and $g_{\tan k}$ =4.1m. Therefore, F can be predicted by F (dB)= NF +Km=13.241(dB). From the Leeson's model in Eq. (4.1) the predicted phase noise is shown as Fig. 4.17 with –100dBc/Hz and -116dBc/Hz at a specific offset frequency 100 KHz and 600 KHz, respectively. Ps is around 7.16mW. Q_L is dominant by the quality factor of spiral inductor, Q_{ind}, i.e. $Q_L \approx Q_{ind} \approx 5$, which is from the measurement. The measured VCO output spectrum is shown in Fig 4.18. The peak power is around 2.3dBm. The tuning range in terms of peak power holding is shown in Fig. 4.19. The tuning range is from 2.075GHz to 2.213GHz when the varactor control voltage varies from 0V to 3V. The measurement of phase noise shown in Fig. 4.17 is measured by EUROPTEST PN9000 with 3V dry battery. The measured phase noise is –100dBc/Hz and –115.5dBc/Hz at 100KHz and 600KHz offset from the carrier, respectively. The measured result of phase noise is seems to be good match with simulated results. The corner frequency w_{1/f^3} is equal to 15KHz from measurement. Table 4.2 summarizes performance of the VCO.

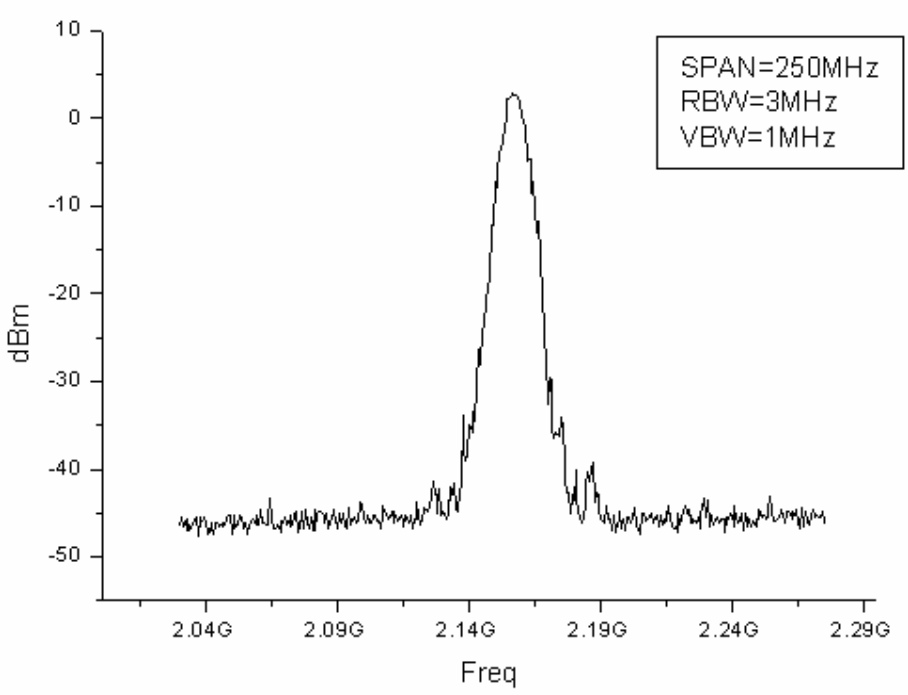

Fig. 4.18 The measured VCO output spectrum

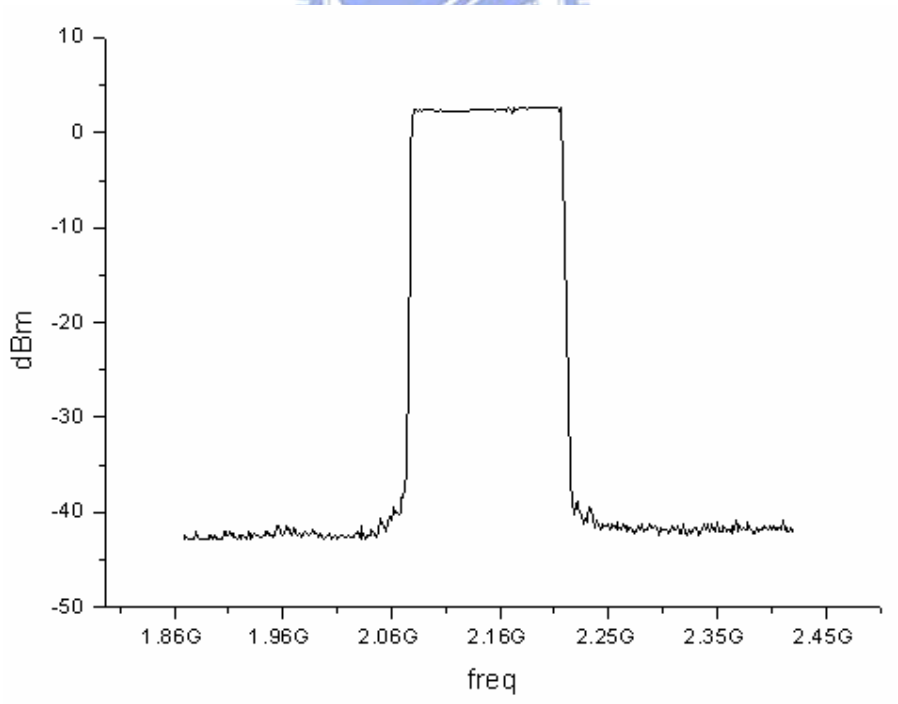

Fig. 4.19 The tuning range in terms of peak power holding

of S35-90D VCO

Table4.2 The Summary of VCO performance

	simulation	measurement
Supply voltage	**3V**	**3V**
Tuning range	**1.9663~2.1538GHz**	**2.0751~2.2138GHz**
Output power	**2.63dBm**	**2.3dBm**
Output voltage amplitude	**1.1V**	**0.9V**
Power consumption	**22.991mW**	**23.24mW**
Phase noise @ 600kHz	**-116dBc/Hz**	**-115.5dBc/Hz**

4.7 Verification of VCO Design

Here, we discuss three points for VCO design. First, the signal power is nearly attained with maximum oscillation power[8]. Second, the calculation of phase noise on the frequency domain will give us the confirmation [40]. Third, the analysis of phase noise on the time domain by linear time varying method will be discussed[45].

4.7.1 Maximize the Oscillation Power

The circuit may be separated into two parts as the passive tank and active circuit shown in Fig. 4.20(a). The active part including the PMOS and NMOS can generate the negative resistance to supply the energy to the passive tank. The ratio of W_p / W_n is equal to two due to the electron mobility than that of hole. A symmetric waveform is helpful to get the better $1/f^3$ corner in phase noise. Initially, the negative resistance is greater than positive part and leads to amplitude growing. At steady state, the negative resistance becomes smaller and is balanced by the positive resistance. Amplitude stops growing. At steady state, the negative resistance is compensated by the external positive one. The frequency is determined by the reactive part of the impedance. In general, the negative resistance is inversely proportional to oscillation amplitude. The relation between the negative resistance and current amplitude is shown in the Fig. 4.20(b). The trace seems to quite linear at large amplitude, although a slight bending at small amplitude. As a matter of fact, the steady state settles down to the linear region. Hence, the behavior around the steady state can be approximated by a linear relationship as

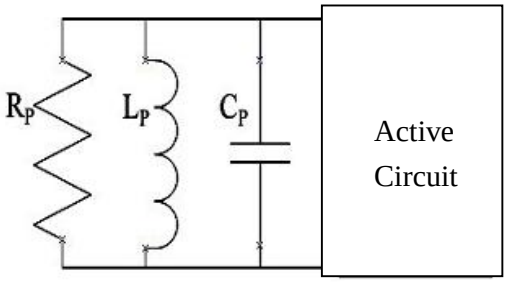

Fig. 4.20 (a) Conceptual block diagram of the oscillator

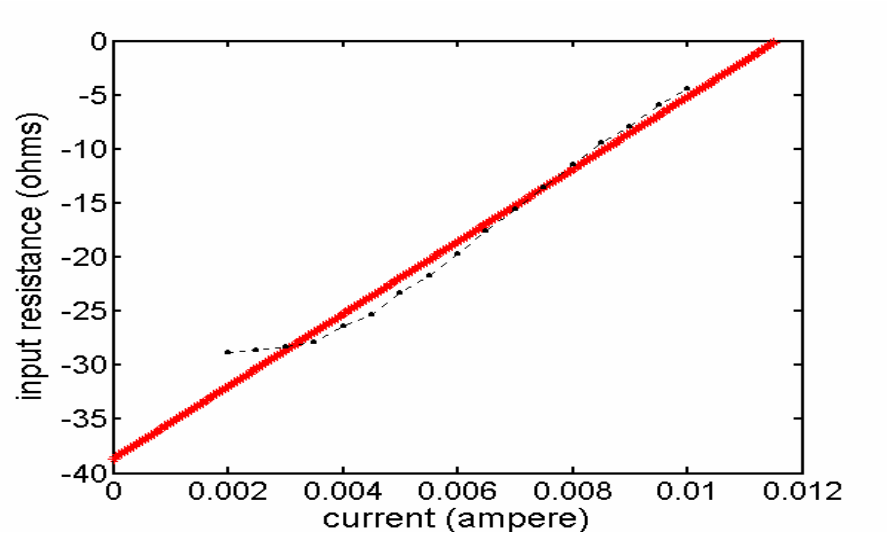

Fig. 4.20(b) Dependence of negative resistance on oscillation current at 2GHz

$$R_{in}(I) = -R_o\left(1 - \frac{I}{I_m}\right) \tag{4.23}$$

where R_o is the initial value of linear fitting resistance, I_m is the maximum value of current with zero negative resistance. The power delivered to the external load R_L (oscillator) by the active part is label P as follow:

$$P = \frac{1}{2} R_e\left[V \cdot I^*\right] = \frac{1}{2}\left|I^2\right| \cdot \left|R_{in}\right| \tag{4.24}$$

The maximum power occurs at the condition with $dP/dI = 0$. According to ref.[8], the maximum power occurs at the situation with current amplitude $I_{,max}$=2/3 $I_{m.}$ By carefully trimming the size and tail current, we can easily reach this condition. In our

case I_m=11.31mA obtained from Fig. 4.20(b) and thus, I_{max}=7.54 mA, which is basically equal to the tail current. The measured value of the tail current is 7.66mA with 3V supply voltage.

4.7.2 Prediction of Phase Noise on Frequency Domain

To calculate the single sided spectral phase noise density, the output phase noise must be integrated over a 1-Hz bandwidth and divided by the carrier power [40.49] :

$$\pounds\{\Delta\omega\} = \frac{\int_{\Delta w-1/2}^{\Delta w+1/2} dVout^2\{\Delta w\}}{carrier \quad power}$$

$$= \frac{kT \cdot R_{eff} \cdot [1+A] \cdot \left(\frac{w_0}{\Delta w}\right)^2}{V_A^2/2} \tag{4.25}$$

where R_{eff} is the total equivalent series resistance of the tank, A is the amplifier noise contribution factor, ω_o is the free-running frequency, $\Delta\omega$ is the frequency offset from the carrier, $V_A^2/2$ is the power of the carrier signal, V_A is the amplitude of oscillation. In our work, the $R_{eff} = wL/Q = 8.29\Omega$ at 2GHz, A=2.51 deduced from K_m factor (4dB), and V_{peak} =0.9V. The results in a phase noise at 600 KHz offset is given as:

$$L(600KHz) = \frac{1.38\times10^{-23}\cdot300\cdot8.29\cdot(1+2.51)\cdot\left(\frac{2GHz}{600KHz}\right)^2}{0.9^2/2}$$

$$= 3.31\times10^{-12} = -114.81\,dBc/Hz$$

The prediction is quite agreement with the measured one.

4.7.3 Analysis of Phase Noise by Linear Time Varying Method

(A) Linear Time Varying Analysis on Phase Noise

Recently, another analysis on the phase noise prediction with linear time-varying is developed [34.35.45]. This method describes a input impulse current which is injected into the circuit. It will have a phase difference to form the phase noise, except for the peak point. Fig. 4.21 shows the process with block diagram of linear time-varying analysis. The unit inpulse response for excess phase can be expressed as

$$h_f(t,t) = \frac{\Gamma_{(w_0 t)}}{q_{max}} u(t-t) \tag{4.26}$$

where q_{max} is the maximum charge displacement across the capacitor on the node and

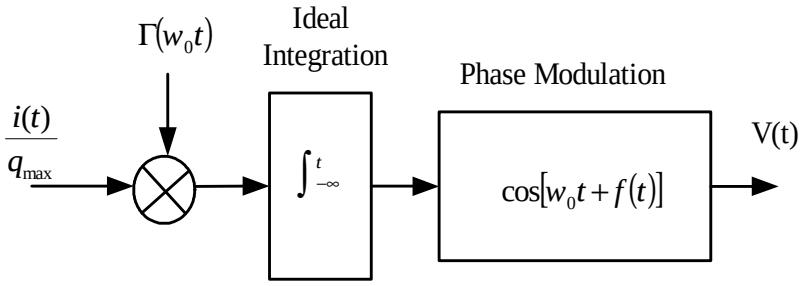

Fig. 4.21 Blook diagram of linear time-varying analysis

u(t) is the unit step. $\Gamma_{(x)}$ is called the impulse sensitivity function (ISF). $\Gamma_{(x)}$ is a function of the periodic waveform; and represents the phase variation by ISF in time τ. Given the ISF, the output excess phase $\Phi_{(t)}$ can be calculated using superposition integral

$$\Phi_{(t)} = \int_{-\infty}^{\infty} h_{\Phi}(t,t)\, i(t)dt = \frac{1}{q_{\max}} \int_{-\infty}^{t} \Gamma(w_0 t) \cdot i(t)dt \tag{4.27}$$

where i(τ) represents the input noise current injected into the node of interest.

The phase variation may be viewed as signal by phase modulation which transforms phase to voltage in Fig.4.21. The output voltage can be expressed by

$$\begin{aligned} Cos\,[w_0 + \Phi(t)] &= \cos(w_0 t)\cos[\Phi(t)] - \sin(w_0 t)\sin\Phi(t) \\ &\approx \cos(w_0 t) - \Phi(t)\sin(w_0 t) \end{aligned} \tag{4.28}$$

For a single-tone phase modulation for output voltage, the sideband power relative to the carrier is given by

$$P_{SBC}(\Delta w) = 10 \cdot \log\left(\frac{I_n C_n}{4 q_{\max} \Delta w} \right)^2 \tag{4.29}$$

The total single sideband phase noise spectral density in dB below the carrier per unit bandwidth due to the source on one node at an offset frequency of Δw is given by

$$L(\Delta w) = 10 \cdot \log\left(\frac{\dfrac{\overline{i_n^2}}{\Delta f} \sum_{n=0}^{\infty} C_n^2}{8 q_{\max}^2 \Delta w^2} \right) = 10 \cdot \log\left(\frac{\Gamma_{rms}^2}{q_{\max}^2} \cdot \frac{\bar{i}_n^2 / \Delta f}{4 \cdot \Delta w^2} \right) \tag{4.30}$$

where $\sum_{n=0}^{\infty} c_n^2 = 2 \cdot \Gamma_{rms}^2$.

This equation represents the phase noise spectrum of an arbitrary oscillator in $\frac{1}{f^2}$ region of the phase noise spectrum. And the transformation to the flicker noise is given by

$$L(\Delta w) = 10 \cdot \log\left(\frac{C_0^2}{q_{\max}^2} \cdot \frac{\bar{i}_n^2 / \Delta f}{8 \cdot \Delta w^2} \cdot \frac{w_{1/f}}{\Delta w} \right) \tag{4.31}$$

where $w_{1/f^3} = w_{1/f} \cdot \frac{c_0^2}{2 \cdot \Gamma_{rms}^2} \approx w_{1/f} \cdot \left(\frac{c_0}{c_1} \right)^2$

(B) Flicker Noise of the Device

For the purpose of prediction on phase noise, the flicker noise of the devices has been measured by way of equipment BTA 9603 FET Noise Analyzer. Two NMOS and one PMOS devices were measured separatedly under bias voltage at $|V_{gs}|$=0.8, 1, 1.3V and $|V_{ds}|$=0.8, 1, 1.3V. The mean value of the MOS flicker noise can be expressed as [4]:

$$\frac{\bar{i}_n^2}{\Delta f} = \frac{K_f \cdot g_m^2}{C_{ox} \cdot W \cdot L \cdot f^a} \tag{4.32}$$

where g_m, W and L are all known parameters. The value of K_f and f^{α} can be extracted from measurement data. The value α=1 is the ideal case of theory, but practical value with 0.87~1.2 comes from experiment. C_{ox}=4.6e^{-3}F/m is given by process parameter and expressed by the following :

$$C_{ox} = \frac{K_{ox} \cdot e_{ox}}{t_{ox}} \tag{4.33}$$

From the measuring results, the values of g_m under the same voltage V_{gs} and different voltage V_{ds} which is nearly closing are shown in Fig. 4.22. There is some more difference under different voltage V_{gs} which is shown in Fig. 4.23. The flicker noise of PMOS is smaller than NMOS at the bias V_{gs}=V_{ds}=1V, which also shown in the Fig. 4.24. Table4.3 shown the device size, bias voltage and extracted parameter with K_f and α. The value K_f of NMOS is larger than PMOS about six times. The value α of NMOS is about 0.87~0.94 and PMOS is 1~1.2, respectively[50].

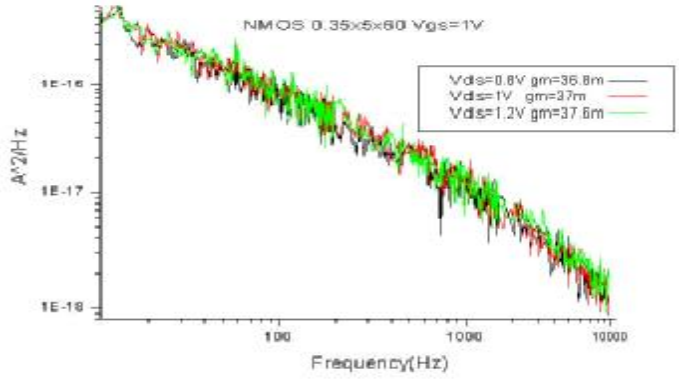

Fig. 4.22 Measurement of NMOS flicker noise with different Vds under Vgs=1V

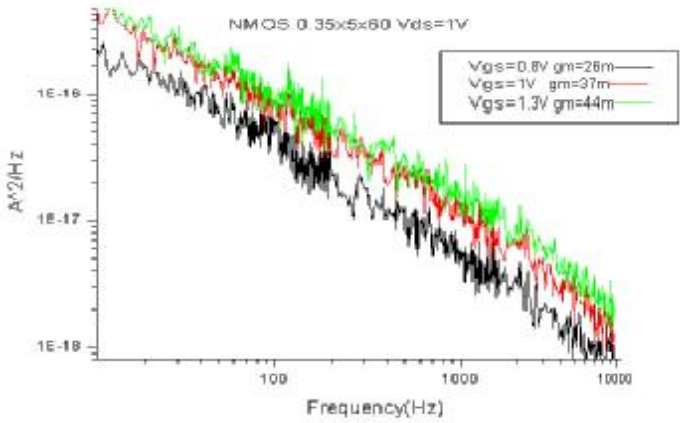

Fig. 4.23 Measurement of NMOS flicker noise with different Vgs under Vds=1V

Table 4.3 Extracted value of K_f and α of flicker noise

	Size	| Vgs |	| Vds |	Gm	Kf	α
NMOS1	L=0.35um	0.8	1	26m	$1.7e^{-24}$	0.88
	W=5um	1	1	37m	$1.7e^{-24}$	0.88
	M=60	1.3	1	44m	$1.5e^{-24}$	0.87
NMOS2	L=0.35um	0.8	1	18m	$2.2e^{-24}$	0.9
	W=5um	1	1	26m	$1.9e^{-24}$	0.89
	M=40	1.3	1	31m	$2.6e^{-24}$	0.94
PMOS1	L=0.35um	0.8	1	7.8m	$2.2e^{-25}$	0.98
	W=5um	1	1	19m	$3.5e^{-25}$	1.19
	M=120	1.3	1	30m	$4e^{-25}$	1.17

(C) Phase Noise Prediction of VCO

The excess noise multiplication factor F of the Leeson's model is determined by the experimental data fit. It gives no further information on the prediction of the phase noise for the circuit designer. The phase noise calculated by impulse sensitivity function (ISF) is a new method which proposed in Ref. [45.46.47]. This method is based on time-variant model makes explicit predictions of relationship between waveform shape and 1/f noise up-conversion. It also introduces a general method to calculated the phase noise with multiple noise source including the flicker noise induced by the nonlinear mixing mechanism with the simple relation the

sideband power due to an arbitrary source. The phase noise included the effect of flicker noise in the $1/f^2$ region under ISF can be described as follow [45] :

$$L\{\Delta w\} = 10\log\left(\frac{\Gamma_{rms}^2 \cdot \overline{in^2}/\Delta f}{q_{\max}^2 \cdot 4 \cdot \Delta w^2}\right) \tag{4.34}$$

where $q_{\max}$ is the maximum charge displacement across the capacitor of the tank, Γ_{rms} is the root mean square value of impulse sensitivity function, and $\overline{in^2}/\Delta f$ is the current noise density. In Fig.4.1, if the bias noise and tank loss are taken into account, the phase noise can be modified into the following :

$$L\{\Delta w\} = 10\log\left\{\begin{array}{l}\left(\frac{\Gamma_{rms}^2 \cdot \overline{inp^2}/\Delta f}{q_{\max}^2 \cdot 8 \cdot \Delta w^2}\right)\cdot\left(1+\frac{w_p \cdot 1/f^3}{\Delta w}\right)+\left(\frac{\Gamma_{rms}^2 \cdot \overline{inn^2}/\Delta f}{q_{\max}^2 \cdot 8 \cdot \Delta w^2}\right)\cdot\left(1+\frac{w_{n\cdot 1/f^3}}{\Delta w}\right) \\ +\left(\frac{\Gamma_{b,rms}^2 \cdot \overline{inb^2}/\Delta f}{q_{\max}^2 \cdot 8 \cdot \Delta w^2}\right)\cdot\left(1+\frac{w_n \cdot 1/f^3}{\Delta w}\right)+\left(\frac{\Gamma_{rms}^2 \cdot \overline{inl^2}/\Delta f}{q_{\max}^2 \cdot 4 \cdot \Delta w^2}\right)\end{array}\right\} \tag{4.35}$$

where $\overline{inn^2}/\Delta f$, $\overline{inp^2}/\Delta f$, $\overline{inb^2}/\Delta f$ are the current noise density of cross-couple NMOS and PMOS and bias, respectively, $\overline{inl^2}$ is the tank noise and is equal to $4KTg_{tank}$, g_{tank} is the equivalent tank parallel conductance[34.35], w_{1/f^3} is the angular corner frequency, and Δw is the angular offset frequency. The impulse sensitivity function (ISF) in time-variant model is periodic and can be expanded in a Fourier series:

$$\Gamma(w_0 t) = c_0 + \sum_{n=1}^{\infty} c_n \cos(n w_0 t + q_n) \tag{4.36}$$

The coefficients satisfy the relation:

$$4c_0 + \sum_{n=1}^{\infty} c_n^2 = \frac{1}{p}\int_0^{2p} |\Gamma(w_0 t)|^2 \, dw_0 t = 2\Gamma_{rms}^2 \tag{4.37}$$

The corner frequency in oscillator is closely related to low corner frequency and is

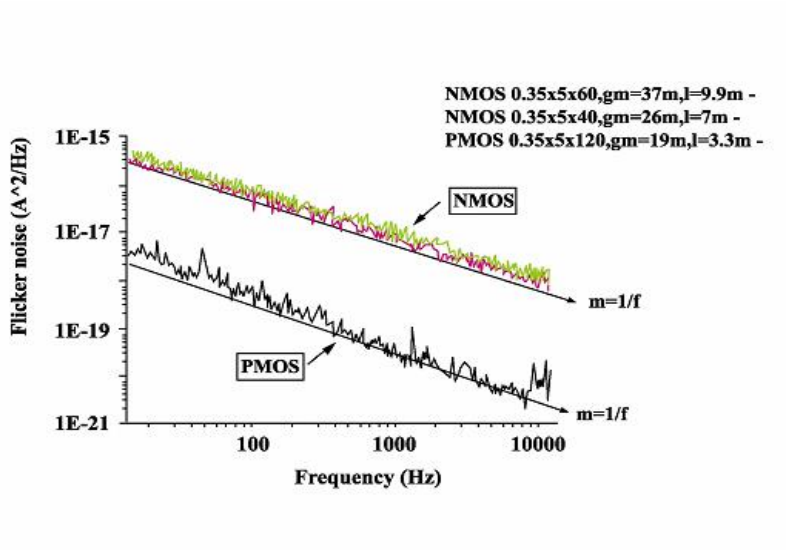

Fig. 4.24 MOSFET flicker noise

indicated as $w_{1/f^3} = w_{1/f} \cdot 2 \cdot \left(\frac{c_0}{\Gamma_{rms}} \right)^2$. The MOSFET $1/f$ noise is shown in Fig. 4.24. The corner frequency fc is the intersection point between the $1/f$ noise and thermal noise, which generally depends on device dimensions and bias current. The mean square 1/f MOSFET drain noise current per unit bandwidth is given by [4]:

$$\overline{in^2}/\Delta f = \frac{K_f \cdot g_m^2}{C_{ox} \cdot W \cdot L \cdot f} \tag{4.38}$$

where K_f is a process-dependent constant. Furthermore, MOSFETs thermal noise per unit bandwidth is given as [4]:

$$\overline{in^2}/\Delta f = 4KTg \cdot g_m \tag{4.39}$$

where the short channel effect is in terms of $g = 2/3 \sim 3$. Accordingly, the corner frequency is obtained

$$f_c = \frac{K_f \cdot g_m}{C_{ox} \cdot W \cdot L \cdot 4KTg} \tag{4.40}$$

where $C_{ox} = 4.6 \times 10^{-3}\, F/m^2$ in the 0.35um CMOS technology process. From the measurement, the coefficients K_f extracted are K_{fp} (PMOS)=1.5e-25 ,

K_{fn}(NMOS)=4e-24. The results reveal that PMOS devices have less 1/f noise than NMOS transistors. From thermal noise measurement with NF=1.5 for device g_m=60m, frequency=300 MHz (not shown) results in that g is roughly equal to 1.6. From the measurement of the device flicker noise in Fig. 4.24, the corner frequency is in the vicinity of 150 KHz for PMOS, and in the vicinity of 9 MHz for NMOS[50].

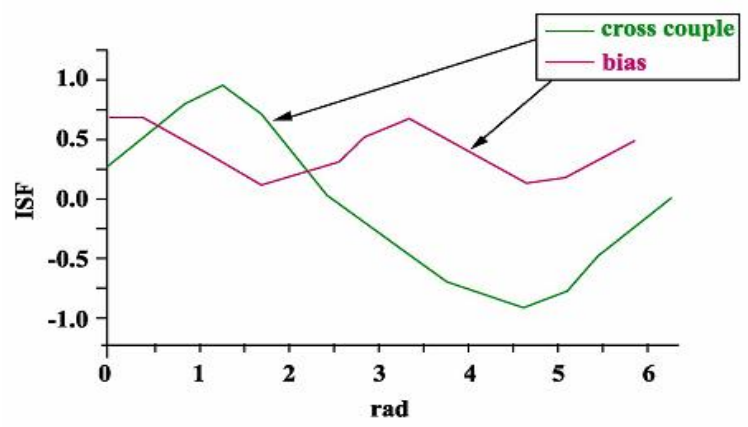

Fig. 4.25 Impulse sensitivity function (ISF) of MOS current noise.

To apply the prediction of equation in (4.35), the calculated ISF is first obtained as shown in Fig. 4.25. The ISF of cross-coupled pair is obtained by way of using differential current noise injection on the output of VCO. And ISF of bias is also obtained with the help of current noise injection from the node of bias to the node of output of VCO. The coefficients calculated are C_0=0.07, Γ_{rms}^2 =0.52 for cross-coupled MOS and C_0 =0.13, $\Gamma_{b,rms}^2$ =0.14 for tail current MOS. In our design, $q_{\max} = 1.73\times10^{-12}, C = 1.92\times10^{-12}, V_{\max} = 0.9$, corner frequency 15 KHz. The calculated phase noise by equation (4.35) is shown in Fig. 4.26. with = -98.0 dBc/Hz at offset 100kHz and -114.5 dBc/Hz at offset 600 KHz, respectively. The calculated data is very closed to the measurement data. The noise contribution percentage of each part under the condition of 2GHz oscillation frequency at offset 100 KHz is listed in Table 4.4. It reveals that the tail current source take a major part in phase noise performance. This fact should not be overlooked during the design.

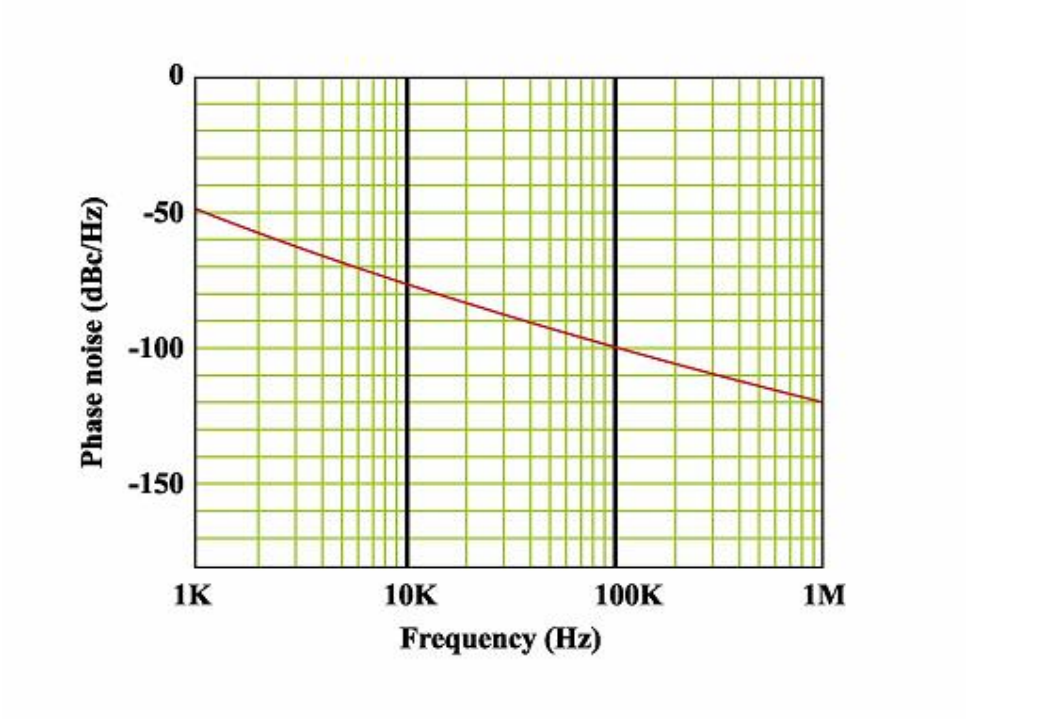

Fig. 4.26 The calculated phase noise spectrum by linear time-varying model

Table 4.4 Phase noise contribution of each part in the VCO circuit

LC tank	4.5%
Cross-couple PMOS	12.2%
Cross-couple NMOS	31.6%
Current Source	51.7%

The VCO performance by means of a figure of merit is defined as [35]

$$\text{FOM}\ (dBc) = S_{SSB} \cdot \left(\frac{f_{offset}}{f_C} \right)^2 \cdot P_{diss}\ (mW) \qquad (4.41)$$

where S_{SSB} is the signal sideband noise at offset frequency f_{offset}. The value of FOM from equation (4.41) is -173.2dBc/Hz. The comparison with some reported papers basing on the same structure and related technology is also listed in Table 4.5. The performance of our work can be compatible with some reported papers[35.51.52]. Though a less value of FOM, our VCO has large output power of signal than others.

Table 4.5 Comparison with some reported papers basing on the same structure and related technology

Reference	This Work	[35]	[51]	[52]
Technology	CMOS 0.35μm	CMOS 0.35μm	CMOS 0.25μm	CMOS 0.18μm
f_o (GHz)	2.06	2.03	2.45	12
Vdd (V)	3	2.5	2.5	1
Power Diss. (mw)	22.62	10	10.6	7.7
Phase Noise (dBc/Hz)	-116@ 0.6MHz	-117@ 0.6MHz	-115@ 0.6MHz	-102@ 0.6MHz
FOM(dBc)	-173.2	-177.6	-176.8	-179.4
Tuning range	9.1%	26%	17.9%	3.33%
Output power(dBm)	2.33	0	NA	NA

4.8 Conclusion

The 2GHz low phase noise VCO with complementary cross-couple pair structure is implemented by the 0.35um CMOS technology. The phase noise reduces by the quality factor of the inductor using the layout optimization firstly. From the effective method we proposed, the minimum noise number F degrades the phase noise directly. The determination of excess noise number F during the phase noise design is indicated. The measured phase noise with -115.5 dBc/Hz is optimized by choosing the suitable sizes of the cross-coupled pairs to achieve a lower mixing factor. The prediction of phase noise which we proposed according the Leeson's model is in good agreement with the measurement. This confirmation provides a simple rule for the low phase noise VCO design.

Chapter 5

Conclusion

In the thesis, we first show that noise property containing passive and active device. And how noise applied to the circuit design for LNA and VCO is described.

For LNA design, we focus on the noise property and parasitic effect of low noise amplifiers with source inductance feedback SIF in the C-band. The topology of LNA with SIF to improve that input and noise match can be achieve simultaneously by adding an inductor within the amplifier.

The feasibility of the technique of source inductive feedback(SIF) for low noise amplifier(LNA) design is examined in different frequency domains. The variations in noise and input impedance are obtained by two different approaches. One is from a noisy two-port analysis to observe the variation of F_{min} and R_n, and the other is form equivalent circuit model to trace out the key element. Using SIF, the results with both good input return loss about –23 dB and low minimum noise figure about 1 dB at C band are demonstrated. Another circuit design of 2.4GHz CMOS LNA with 12.5 dB gain and 5.6 dB noise figure was fabricated by the process of UMC 0.5um DPDM technology. The circuit with using SIF topology, the noise and input matching can be easily obtained, the gain and isolation are examined to be improved. Owing to the gate sheet resistance $30\Omega/\square$ is so high that it affects the input matching, noise figure and signal gain. Therefore, choosing lower sheet resistance of poly gate is necessary to RF design.

A fully integrated LC-tank VCO with cross coupled pair is designed for 2GHz wireless application. The fabrication of VCO is in term of TSMC 0.35 μm CMOS process. The oscillation frequency and tuning range of VCO are determined by LC-tank. Regarding to LC tank, the layout optimization of spiral inductor to increase quality factor and also to reduce the phase noise is used. The inversion mode MOS varactor is used at extend the tuning range with 9.1% under 2GHz. From our proposed method , the low phase noise by calculation is attained. The phase noise of measured value which shows good match with calculation data is about –115.5dBc/Hz at off set frequency 600kHz.

Reference

[1] D. M. Pozer, Microwave and RF Design of Wireless System, John Wiley and Sons, 2001.

[2] L. E. Larson, RF and Microwave Circuit Design for Wireless Communications, Artech House, Dedham, MA, 1996.

[3] T. S. Rappaport, Wireless Communication: Principles and Practice, Prentice Hall, Englewood Cliff, NJ, 1996.

[4] B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, 2001.

[5] D. A. Johns and K. Martin, Analog Integrated Circuit Design, New York: Wiley, 1997.

[6] J. Tsividis, Operation and Modeling of the MOS Transistor, Second Ed, Boston: Mc Graw-Hill, 1999.

[7] A. A. Abidi, "High-Frequency Noise Measurement on FET's with Small Dimensions" IEEE Transactions Electron Devices, vol.33, pp. 1801-1805, Nov, 1986.

[8] G. Gonzales, Microwave Transistor Amplifiers, Analysis and Design, 2nd edition, Precctice Hall, Upper Saddle River, New Jersey, 1997.

[9] T. H. Lèe, The Design of CMOS Radio Frequency Integrated Circuits, Cambridge University Press, 1998.

[10] B. Razavi, RF Microelectronics, Upper Saddle River, NT: Precctice Hall, 1998.

[11] D. B. Leeson, "A Simple Model of Feedback Oscillator Noise Spectrum," *Proc*. IEEE vol.54, pp. 329-330, 1966.

[12] D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," *IEEE Journal of Solid State Circuits.*, vol. 32, no.5, pp. 745-749, May 1997.

[13] R. Lehmann and D. D. Heston, "X-band monolithic series-feedback LNA," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-33, pp. 1560~1566, Dec. 1985.

[14] H. Uchida, S. Takatsu, K. Nakahara, T. Katoh, Y. Itoh, R. Imai, and M. Yamamoto, " Ka-band multistage MMIC low-noise amplifier using source inductors with different values for each stage, " IEEE Microwave and Guided Wave Letters , vol. 9, no 2, pp. 71-72,Feb. 1999.

[15] Y. Ge and K. Mayaram, "A comparative analysis of CMOS low noise amplifiers for RF applications," ISCAS'98, proceeding of the IEEE International symposium on Vol. 4, pp. 349-352, 1998.

[16] M. J. O. Struct and A. Van Der Ziel, "Suppression of spontaneous fluctuations in amplifiers and receivers for electrical communication and for measuring devices," Physica, vol. Ⅸ, no. 6, pp. 513-538, June 1942.

[17] H. Fukui, “Available power gain, noise figure, and noise measure for two-ports and their graphical representations,” IEEE Transactions on circuit theory, vol. CT-13, no.2, June 1966.

[18] J. Engberg, “Simultaneous input power match and noise optimization using feedback,’ in Dig. Tech. Pap. Fourth Eur. Microwave Conf. Montreaux, Switzerland, pp. 385-389. Sept. 1974.

[19] L. Besser, “Stability considerations of low-noise transistor amplifiers with simultaneous noise and power match,” IEEE MTT-S Int. Microwave Symp., pp. 327-329, 1975.

[20] N. Shiga, S. Nakajima, K. Otobe, T. Sekiguchi, N. Kuwata, Ki. Matsyzajum and H. Hayashi, “X band MMIC amplifier with pulsed doped GaAs MESFETs,” *IEEE Trans. Microwave Theory Tech*, vol. 39, no.12, pp. 77-80, Dec. 1991.

[21] H. Rothe and W. Dohlke, “Theory of noisy fourpoles,” Proc. IRE, vol. 44, pp.811-818, June, 1956.

[22] S. Iversen, “The effect of feedback on noise figure,” Proceedings of the IEEE, vol. 634, pp. 540-542, May. 1975.

[23] J. Engberg, “Noise parameters of embedded noisy two-port network,” IEE Proceedings, vol. 132, No. 1, pp. 17-22, Feb. 1985.

[24] B. Albinsson, “Noise parameters transformation of interconnected two-port network,” IEE Proceedings, vol. 134, no. 2, pp. 125-129, Apr. 1987.

[25] A. Cappy, “Noise modeling and measurement technique,” *IEEE Trans. Microwave Theory Tech.*, vol. MTT-36, no.1, pp. 1~10, Jan. 1988.

[26] B. M. Albinsson, “A Graphic Design Method for Mateched Low-Noise amplifiers,” IEEE Trans. Microwave Theory Tech., vol. 38, no.2, pp. 118-122, Feb. 1990.

[27] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, “A new method for determining the FET small-signal equivalent circuit,” IEEE Trans. Microwave Theory Tech. vol. MTT-36, no. 7, pp. 1151-1159, July 1988.

[28] R. A. Pucel, H. A. Haus, and H. Statz, Advances in Electronics and Electron Physics, pp.195-265, Academic Press, New York, 1975.

[29] Bo-Long Lee, Study of Low Noise Amplifier with Source Inductance Feedback, thesis of NCTU, Taiwan, R.O.C, 1998.

[30] Yi-Bin Hsieh, The Design and Analysis of a 2.4GHz CMOS Low Noise Amplifier, thesis of NCTU, Taiwan, R.O.C, 1998.

[31] B. Razavi, R. H. Yan, and K. F. Lee “Impact of distributed gate resistance on the performance of MOS devices.” IEEE Trans, Circuit and System. 1, vol.41, pp. 750 - 754, Nov 1994.

[32] R.R.J. Vanoppen, etc, “The high frequency analogue performance of MOSFETs”,

IEEE,IEDM pp. 173-176,1994.

[33] Bram De Muer, Nobuyuki Itoh, Marc Borremans, and Michiel Steyaert, "A 1.8GHz highly-tunable low-phase-noise CMOS VCO," IEEE Custom Integrated Circuits Conference, pp.585-588, 2000.

[34] A. Hajimiri and T. H. Lee, "Design issues in CMOS differential LC oscillators," IEEE J. Solid-State Circuits, vol. 34, no. 5, pp. 717-724, May 1999.

[35] D. Ham and A. Hajimiri, "Concepts and methods in optimization of integrated LC VCOs" IEEE J. Solid-State Circuits. vol.36, no. 6, pp.896-909, June 2001.

[36] Chao-Chih Hsiao, and Yi-Jen Chan, "RF Large-Signal Models with 0.35um Process," NCU, May 20, 2000.

[37] F. Svelto, S. Deantoni and R. Castello, "A 1mA, -120.5dBc/Hz at 600kHz from 1.9GHz fully tunable LC CMOS VCO," IEEE Custom Integrated Circuits Conference, pp.577-580, 2000.

[38] Chia-Ying Lee, "High Q Suspended Spiral Inductors on Silicon and Their Use in a Active Bandpass Filter", thesis of NCTU, Taiwan, R.O.C, pp.8, 2000.

[39] J. M. Lopez-Villegas, J. Samitier, C. Cane, P. Losantos, and J.Bausells, "Improvement of the quality factor of RF integrated inductors by layout optimization", IEEE Trans. Microwave Theory and Techniques, vol.48, no.1, pp. 76-83, January 2000.

[40] J.Craninckx and M. Steyaert, "A 1.8 GHz low phase noise CMOS VCO using optimized hollow spiral inductors", IEEE J. Solid-State Circuit, vol. 32, no. 5, pp. 736-744, May 1997.

[41] A. Kral, F. Behbahani, and A. A. Abidi, "RF-CMOS oscillators with switched tuning." Proc. of Custom Integrated Circuits Conference, pp. 555-558, 1998.

[42] Pietro Andreani and Sven Mattisson, "On the Use of MOS Varactors in RF VCO's," IEEE J. Solid-State Circuits, vol. 35, pp.905-910, June 2000.

[43] T. Soorapanth, C. P. Yue, D. R. Shaeffer, T. H. Lee, and S. S. Wong, "Analysis and optimization of accumulation-mode varactor for RF ICs," in 1998 Symp. VLSI Circuit Dig. Tech. Paper, 1998,June, pp.32-33.

[44] R. Csatello, P. Erratico, S. Manzini, and F. Svelto, "A $\pm$30% tuning range varactor compatible with future scaled technologies," in 1998 Symp. VLSI Circuit Dig. Tech. Paper, 1998,June, pp.34-35.

[45] Ali Hajimiri and Thomas H. Lee, "A general theory of phase noise in electrical oscillators, " IEEE J. Solid-State Circuits. vol. 33, no. 2, pp.179-194, Feb. 1998.

[46] Y. H. Kao, M. C. Hsu, and M. T. Hsu, "An effective method for low phase noise CMOS VCO design", Proceedings of IEEE-MTT Asia-Pacific Microwave Conference (APMC), pp. 1483-1486, Nov. 2002, Kyoto.

[47] B. Razavi, “A study of phase noise in CMOS oscillators,” IEEE JSSC, vol. 31, no. 3, pp. 331-343, 1996.

[48] Sheng-Min Ke, ”A Fully Integrated Suspended Spiral-LC CMOS VCO with Prescaler,” thesis of NCTU, Taiwan, R.O.C, 2001.

[49] Min-Chieh Hsu, “The Design of A 1.8GHz CMOS RF Frequency Synthesizer for DCS-1800 Application” thesis of NCTU, Taiwan, R.O.C, 2002.

[50] Pi-An Wu,”CMOS RF Frequency Synthesizers with Quadrature Phase Qutputs” thesis of NCTU, Taiwan, R.O.C, 2002.

[51] Tser-Yu Lin. Ying-Zong Juang, and Chin-Fong Chiu “A low power 2.2-2.6GHz CMOS VCO with a symmetrical spiral inductor,”IEEE International Symposium on Circuit and System, pp. 641-644 , 2003.

[52] Tommy K. K. Tsang and Mourad N. El-Gamal, “A high figure of merit and area-efficient low-voltage(0.7-1V) 12GHz CMOS VCO,” IEEE Radio Frequency Integrated Circuits Symposium., pp. 89-92, 2003.

自傳 – Vita

許孟庭 **Meng-Ting Hsu**

彰化縣埤頭鄉合興村文鄉路 192 號 hsumt@yuntech.edu.tw

學歷 Educations

- 國立交通大學 電信研究所博士班 1997/9~2004/9
- 私立中原大學 電子研究所碩士班 1989/9~1991/6
- 私立中原大學 電機工程學系 1986/9~1989/6
- 國立高雄工業專科學校 電機科 1976/9~1981/6

經歷 Experiences

- 國立雲林科技大學 電子工程系講師 1997/8~
- 國立雲林技術學院 電子工程系講師 1994/8~1997/7
- 國立雲林技術學院 電子工程系助教 1992/8~1994/7
- 私立大華工商專科學校 電機科講師 1992/2~1992/7
- 工研院光電研究所副工程師 1991/9~1992/1

論文名稱：金氧半導體元件雜訊對射頻積體電路的影響

Impacts of Noise on the CMOS RF Integrated Circuits

著作目錄 - Publication List

(A)學術期刊論文(Journal Papers)

[1] Yao-Huang Kao and **Meng-Ting Hsu**, ”Theoretical Analysis of Low Phase Noise Design of CMOS VCO “ accepted by IEEE Microwave and Wireless Components Letters, July 9, 2004.
[2] Yao-Huang Kao, **Meng-Ting Hsu,** Min-Chieh Hsu, and Pi-An Wu “A Systematic Approsch for Low Phase Noise CMOS VCO Design” IEICE Trans.Electron.,Vol.
E86-C, No.8 PP.1427~1432 August 2003.(NSC 89-2213-E-009-245).
[3] **Meng-Ting Hsu,** Bo-Long Lee and Yao-Huang Kao , " Study on Noise Properties and Parasitic Effect of Low Noise Amplifiers with Source Inductance Feedback " Journal of the Chinese Institute of Electrical Engineering. Vol. 10, NO.2 PP.197~202, May, 2003(NSC87-2213-E009-114)

(B)研討會論文(Conference Papers)

[4] Yao-Huang Kao, Min-Chieh Hsu, **Meng-Ting Hsu.** " An Effective method for Low Phase Noise CMOS VCO Design”, International Asia-Pacific Microwave Conference. Kyoto.Nov.2002,PP.1483~1486(NSC89-2213-E-009-245)
[5] Yao-Huang Kao, **Meng-Ting Hsu** and Yuan-Min Hsu, " Extraction of Noise Source from Noise Parameters with RF CMOS Devices” International Asia-Pacific Microwave Conference Taipei.Dec.2001 PP.1326~1329 (NSC89-2213-E-009-055)
[6] Yao-Huang Kao, **Meng-Ting Hsu** and Ming-Sheng Wu,” Parasitic Resistance Effects on Noise Figure of CMOS Devices for RF Integrated Circuit Design” International Symposium on Communications Tainan. Dec.2001 section 8.3 (NSC89-2213-E-009-055)
[7] Yao-Huang Kao, **Meng-Ting Hsu**, and Chau-Shi Juang, “Measurement of S parameter and Noise parameters in CMOS RF devices”, Cross Strait Tri-regional Radio Science and Wireless Technology Conference. City University of Hong Kong.Dec.2000 PP.295~298.