Journal of The Electrochemical Society, **156** (4) H276-H280 (2009)
0013-4651/2009/156(4)/H276/5/$23.00 © The Electrochemical Society

Improvement of Charge-Storage Characteristics of Mo Nanocrystal Memory by Double-Layer Structure

Chao-Cheng Lin,[a] Ting-Chang Chang,[b,*,z] Chun-Hao Tu,[a] Wei-Ren Chen,[a] Li-Wen Feng,[a] Simon M. Sze,[a] Tseung-Yuen Tseng,[a] Sheng-Chi Chen,[c] and Jian-Yang Lin[c]

[a]*Institute of Electronics, National Chiao Tung University, Hsin-Chu 300, Taiwan*
[b]*Department of Physics and Institute of Electro-Optical Engineering, Center for Nanoscience and Nanotechnology, National Sun Yat-Sen University, Kaohsiung 804, Taiwan*
[c]*Graduate School of Opto-Electronic Engineering, National Yunlin University of Science and Technology, Yunlin 64002, Taiwan*

An oxygen-incorporated Mo silicide layer was explored to form the Mo nanocrystals after rapid thermal annealing. Transmission electron microscopy showed the nanocrystals embedded in SiO_x. Charge-storage characteristics of Mo nanocrystals influenced by Mo oxide and its surrounding oxide were investigated through X-ray photoelectron spectroscopy and electrical measurement. X-ray photoelectron spectral analyses revealed a redox reaction in the oxygen-incorporated Mo silicide layer after rapid thermal annealing at a critical temperature. The memory window and retention were improved because of the reduction of Mo oxide. Furthermore, the double-layer nanocrystal structure was fabricated through the annealed stacked oxygen incorporated Mo silicide layer. A larger memory window and long retention were found for the double-layer nanocrystal structure. We used an energy band diagram to explain the difference in retention characteristics between single- and double-layer structures.
© 2009 The Electrochemical Society. [DOI: 10.1149/1.3079358] All rights reserved.

Manuscript submitted November 16, 2008; revised manuscript received December 18, 2008. Published February 13, 2009.

Nonvolatile memory based on the floating gate structure plays an important role in portable electronic productions for its advantages of nonvolatility and low power consumption. However, scaling of the floating gate structure is limited by thin tunneling oxide in terms of reliability.[1] To address this, discrete nanocrystals as a charge-storage layer have recently been investigated to replace the electrical continuous poly-Si layer in the floating gate structure.[2-4] Using discrete nanocrystals as charge-storage centers instead of a poly-Si layer can prevent the total stored charges from being lost through a leakage path in the tunnel oxide and therefore allows further scaling of the memory structure. Among nanocrystals, such as semiconductors, high-permittivity insulators and metal nanocrystals, the metal nanocrystals have received much attention than the others because the metal nanocrystals have the advantages of a higher density of states around the Fermi level, stronger coupling with the conduction channel, a wide range of available work functions, and smaller energy perturbation due to carrier confinement.[3] Nevertheless, metal interaction with the tunnel oxide is an important issue because the interaction will deteriorate memory retention. The interaction may occur during the thermal process in the fabrication process of the device, such as dopant activation. Li et al. proposed the use of a combination of Mo–$MoSi_x$ gate electrodes for dual-metal-gate technology on SiO_2 gate dielectric.[5] Their results show good thermal stability of Mo on SiO_2 and are compatible with the metal-oxide semiconductor field effect transistor fabrication process. However, little research has been done on Mo for nanocrystal memory applications.

In this study, nonvolatile memory characteristics of Mo nanocrystals embedded in SiO_x were investigated by thermal annealing an oxygen-incorporated Mo silicide layer. Our experimental results show that Mo oxide was formed in the as-deposited layer. Lee et al. proposed that the cobalt-oxide in the charge-storage layer can deredate the memory window.[6] Therefore, they need an extra hydrogen annealing for 30 min at 300°C to reduce the cobalt-oxide to gain a large memory window. In our result, the Mo oxide can be reduced and the Mo nanocrystals can form after the rapid thermal annealing at a critical temperature without an additional long-term hydrogen annealing process. Furthermore, we employed a method of the Mo nanocrystal formation to fabricate the double-layer nanocrystal structure and investigated its memory characteristics. It was found that the double-layer structure provided an enhanced two-dimensional storage with improved charge-storage characteristics.

Experimental

The process flow and memory structure are shown in Fig. 1. The memory structures were fabricated on a 6 in. p-type Si substrate. A 5 nm thick dry oxide (tunnel oxide) was grown at 950°C on the substrate in a horizontal furnace after a standard RCA cleaning process. An 8 nm thick oxygen-incorporated Mo silicide layer was deposited on the tunnel oxide by cosputtering Mo and Si targets in Ar (24 sccm)/O_2 (2 sccm) ambience. The blocking oxide was deposited by a plasma-enhanced chemical vapor deposition system at 300°C with precursor gases N_2O (120 sccm) and SiH_4 (75 sccm). A thermal annealing process at 800 and 900°C was performed in N_2 for 60 s to investigate the temperature's influence on the memory characteristics of the oxygen-incorporated silicide layer. Finally, a 500 nm thick Al gate electrode patterned with a shadow mask was evaporated by a thermal coater to form the memory structures. For the double-layer memory structure, stacked oxygen-incorporated Mo silicide layers were deposited on the tunnel oxide with a 5 nm thick middle oxide layer between the two layers. Process numbers 4–6 in Fig. 1 were followed to form the metal-oxide semiconductor (MOS) structure. In process 5, the temperature was at 900°C. Trans-

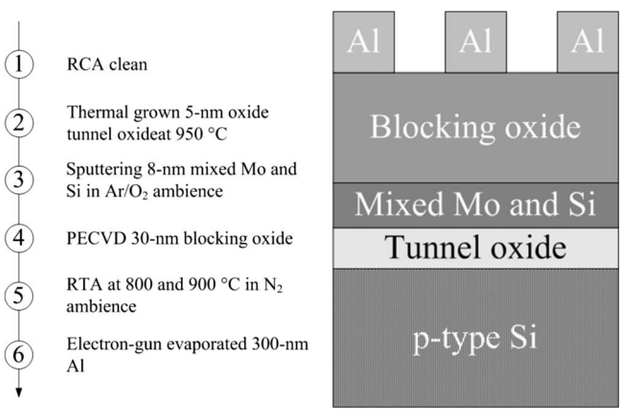

Figure 1. The process flow and memory structure of this work.

* Electrochemical Society Active Member.
z E-mail: tcchang@mail.phys.nsysu.edu.tw

Downloaded on 2014-04-25 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

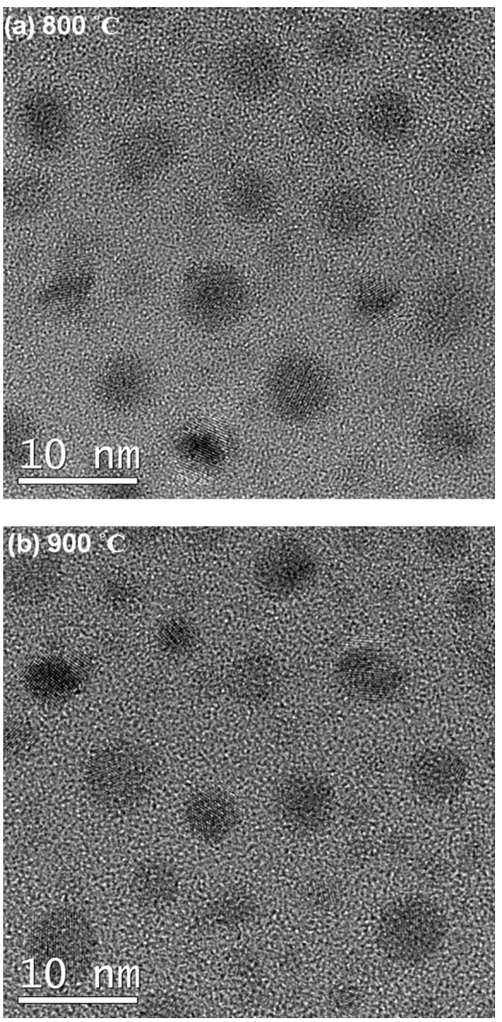

Figure 2. Plane-view TEM image of the (a) 800- and (b) 900°C-annealed samples.

mission electron microscopy (TEM) and X-ray photoelectron spectroscopy (XPS) were used to analyze the microstructure and chemical composition of the nanocrystals and their surrounding oxide. Electrical characteristics of the capacitance–voltage (*C-V*) hysteresis were measured by an HP4284 Precision LCR Meter with frequency of 1 MHz.

Results and Discussion

Figure 2 shows a plane-view TEM image of the 800- and 900°C-annealed samples. The average size of the nanocrystals is about 4 nm for both 800- and 900°C-annealed samples. The aerial density of the nanocrystals was estimated from a TEM image to be about 1.07 and 1.01×10^{12} cm^{-2} for both the 800- and 900°C-annealed sample, respectively. The lattice fringes are obvious in the figure, indicating crystallization of the as-deposited oxygen-incorporated Mo silicide layer after 800 or 900°C annealing treatment.

To investigate the chemical composition of the oxygen-incorporated Mo silicide layer after annealing, XPS analyses were performed using an Al Kα (1486.6 eV) X-ray. Figure 3 shows the XPS Mo 3d and Si 2p core-level spectra. In Fig. 3a, the Mo 3d spectrum of the 800°C-annealed sample containing Mo–Mo and Mo–O bonds indicates the existence of metallic Mo and Mo oxide.[7-9] However, the Mo oxide was reduced for the sample after

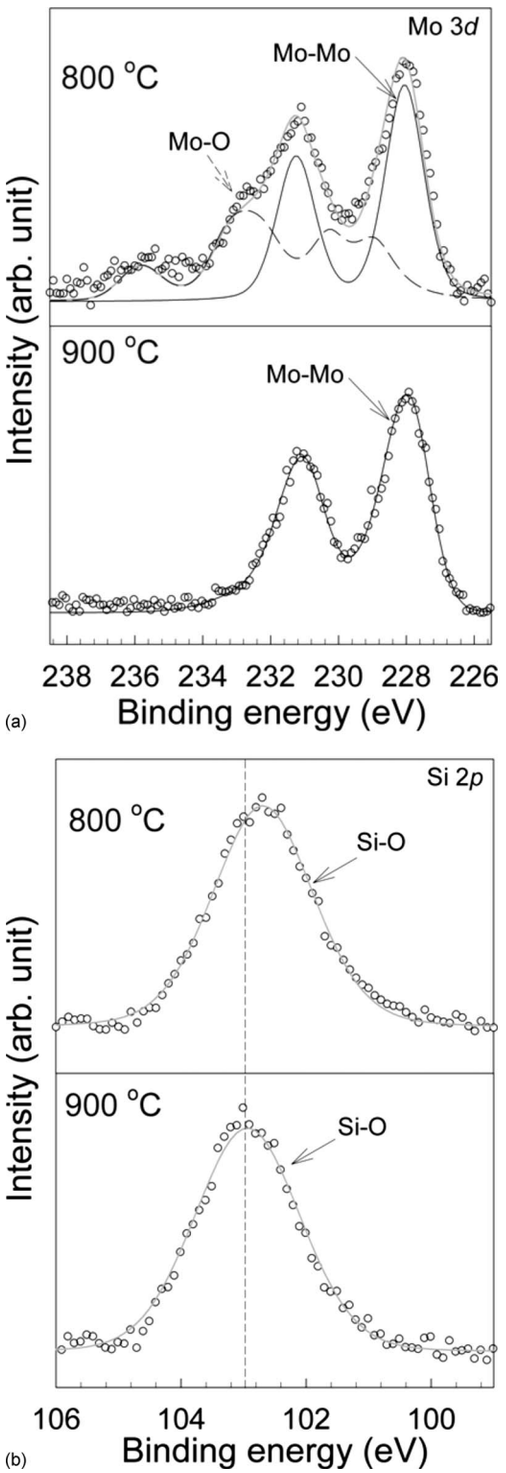

Figure 3. (a) Mo 3d and (b) Si 2p core-level spectra of the oxygen-incorporated Mo silicide layer for as-deposited 800- and 900°C-annealed samples.

900°C annealing, as shown in Fig. 3a. In the Si 2p spectra (Fig. 3b) there are Si–O bonds, indicating the existence of silicon oxide in the 800- and 900°C-annealed samples. For the 800°C-annealed sample, the peak position of Si–O bonds (102.9 eV) is less than 103.3 eV (binding energy of SiO_2).[10] This suggests that the oxide around the nanocrystals is incomplete (SiO_x, $x < 2$). The peak position of Si–O

Downloaded on 2014-04-25 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

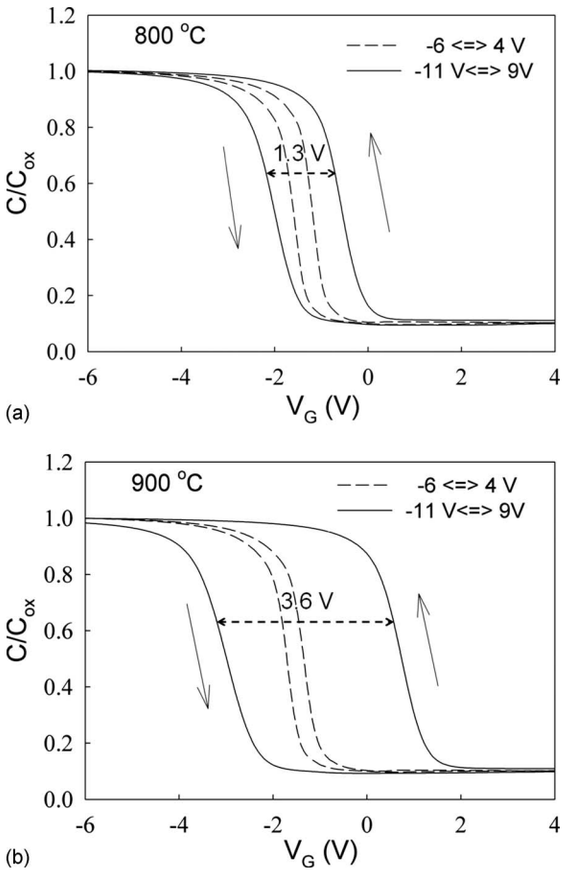

Figure 4. *C-V* curve of (a) 800- and (b) 900°C-annealed samples.

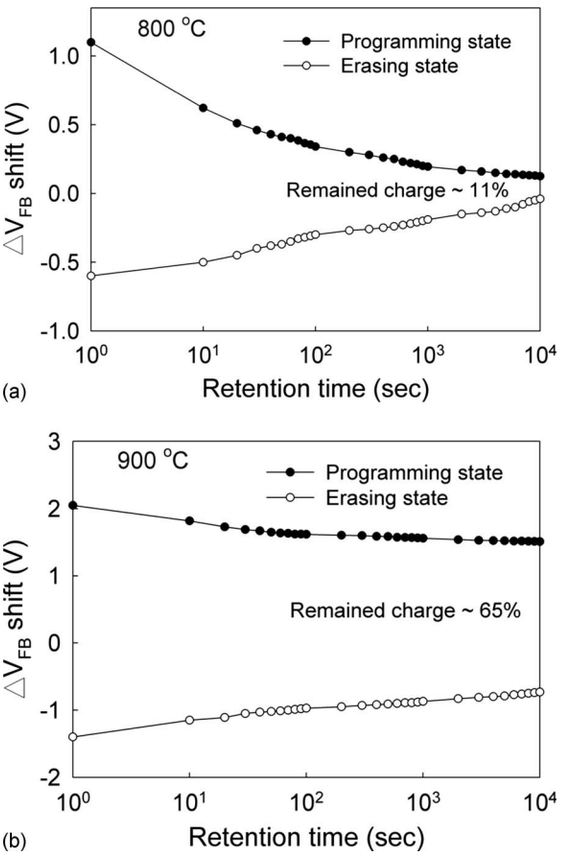

Figure 5. Retention characteristic of (a) 800- and (b) 900°C-annealed samples at room temperature (27°C).

bonds shifted toward higher binding energy for the sample annealed at 900°C. According to the literature, the increment of Si 2p binding energy is attributed to the oxygen bonding with insufficient silicon oxide.[11] The XPS results show that a redox between MoO_x and SiO_x occurred during the thermal annealing process. For the redox behavior in the oxygen-incorporated Mo silicide layer, the formation energy of Si oxide (−750 kJ/mol) is larger than that of Mo oxide (−450 kJ/mol).[12] Therefore, the oxygen of Mo oxide prefers to bond with Si rather than Mo during the thermal annealing at 900°C, which results in the reduction of Mo oxide and improves the quality of SiO_x.

Figure 4a and b shows the *C-V* curves for the 800- and 900°C-annealed samples, respectively. The curves were obtained after the gate voltage swept from the inversion to the accumulation region of the substrate (4 to −6 and 9 to − 11 V) and the reverse (−6 to 4 and −11 to 9 V). The hysteresis loop of both samples is counterclockwise due to substrate injection through the tunnel oxide. It can be found in the figure that the memory window changes with the amplitude of the sweeping voltage, because the V_{FB} shift corresponds to stored charges divided by the capacitance of the blocking oxide ($Q_{storage}/C_{blocking}$). Compared with the lower amplitude of sweeping voltage, more charge can be stored in nanocrystals at the higher amplitude, which results in the larger memory window (larger V_{FB} shift). We note that the memory window for both samples is approximately at the smaller sweeping voltage range (4 to − 6 V). However, at the larger sweeping voltage range (9 to −11), the memory window for the 900°C-annealed sample (3.6 V) is twice larger than that for the 800°C one (1.3 V). According to XPS results, we speculate that the larger memory window for the 900°C-annealed sample was due to the reduction of Mo oxide that has been proposed as a semiconductor-like metal oxide. Therefore, the Mo oxide has lower density of state than metallic Mo for charge storage. The larger memory window of the 900°C-annealed sample has benefits with regard to retention tolerance and the circuit design of nonvolatile memory applications. In the retention mode (no external applied voltage on the device), the memory window will reduce as time passes due to charges lost from nanocrystals. The larger memory window can maintain a larger margin for the logic circuit to identify the different states (logic "0" and "1"), which can simplify the circuit design.

Figure 5a and b shows the retention behavior of 800 and 900°C samples, respectively. The retention was measured at stress voltage of 10 V (programming state) and −10 V (erasing state) on the gate electrode for 5 s. The memory window is obtained by comparing the *C-V* curves of a charged state to a quasineutral state. The memory window of the 800°C-annealed sample decreased significantly and remained at ~11% after 10^4 s. In contrast, the retention of the 900°C-annealed sample remained at ~65%. The XPS results (Fig. 2) reveal that the different retention behaviors were related to the quality of the oxide around the nanocrystals. When charges are stored in the nanocrystals, the stored charges can escape laterally through the traps in the surrounding oxide. If the tunnel oxide has a leakage path, the escaped charges will leak into the substrate. Because the surrounding oxide quality of the 900°C-annealed sample was improved by the redox reaction between Mo oxide and SiO_x, more charge remained in the Mo nanocrystals.

Figure 6a is a cross-sectional TEM image of a double-layer nanocrystal sample. From the cross-sectional TEM in Fig. 6a, it can be found that the double-layer nanocrystals were formed after the 900°C annealing. Figure 6b is a *C-V* curve of a double-layer sample after the gate voltage is swept from the inversion to the accumula-

Downloaded on 2014-04-25 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

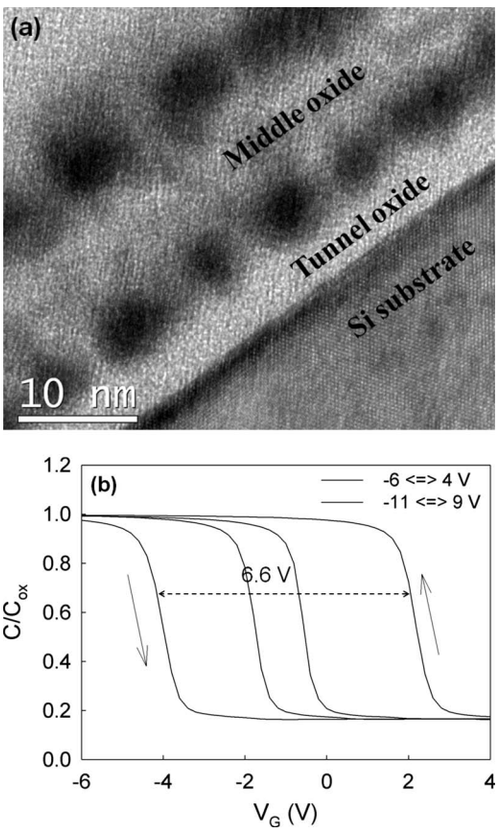

Figure 6. (a) Cross-sectional TEM image and (b) *C-V* curve of the double-layer structure.

tion region of the substrate (4 to − 6 V and 9 to − 11 V) and the reverse (−6 to 4 and −11 to 9 V). The *C-V* curve is also a counter-clockwise hysteresis. It is seen that the memory window at the larger sweeping voltage of −11 to 9 V is about 6.6 V, which is larger than that of the single layer (3.6 V).

Figure 7 shows a comparison of the memory window between the single- and double-layer structures at various amplitudes of sweeping voltage. It can be found that as the sweeping voltage increases, the memory window increases in both structures. We note that the memory windows of the double-layer structure are larger than those of the single layer. For the difference in the memory window between the single- and double-layer memory structures,

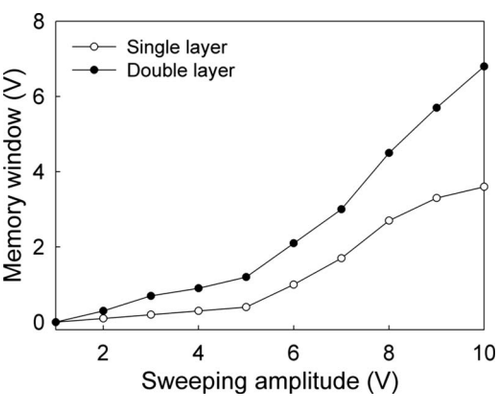

Figure 7. Comparison of memory windows between the single- and double-layer structures at various sweeping voltages.

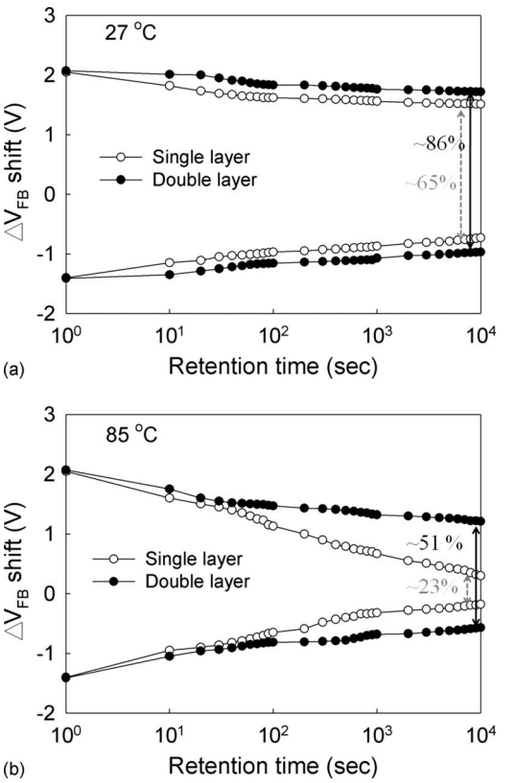

Figure 8. Comparison of retention characteristics for single- and double-layer structures at (a) room temperature (27°C) and (b) 85°C.

we consider that the injected carriers can be stored in the nanocrystals at the upper and lower layer of the double-layer structure, leading to the larger memory window than the window of a single-layer structure. Furthermore, the increment of the memory window becomes less and saturates in the single-layer structure at sweeping amplitudes higher than 8 V. This phenomenon can be attributed to the charging energy effect.[2] As the sweeping voltage increases, the increment of memory window indicates the increase of stored charge in the nanocrystals. The stored charges in the single-layer nanocrystals can lead to a large charging energy, which reduces the electric field on the tunnel oxide and blockades the injected carriers into nanocrystals. However, there was no observed memory window saturation phenomenon in the double-layer structure. It was considered that the charges stored in the lower layer of the double-layer structure can be released to the upper layer, which reduces the charge energy in the lower layer. Therefore, the memory saturation phenomenon is not serious in the double-layer structure. The double-layer memory structure can increase the memory window and is preferred for applications in nonvolatile memory.

Figure 8a and b shows the comparison of the retention between the single- and double-layer structure at room temperature and at 85°C, respectively. It can be found in Fig. 8a that the retention characteristics of both structures are similar. However, the retention characteristics at 85°C in Fig. 3b show that the double-layer structure has better retention (51% charge remained after 10^4 retention times) than the single-layer structure (23% charge remained). The good retention of the double-layer structure is due to the coulombic blockade effects on the upper-layer nanocrystals from the bottom-layer nanocrystals. As shown in Fig. 9b, after the charge is stored in the nanocrystals of both layers, the stored charges in lower layer nanocrystals can raise the electronic energy in the middle oxide to blockade the stored charges in the upper-layer nanocrystals. So the memory effects of the nonvolatile memory device can be improved by using the double-layer nanocrystal structure.

Downloaded on 2014-04-25 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

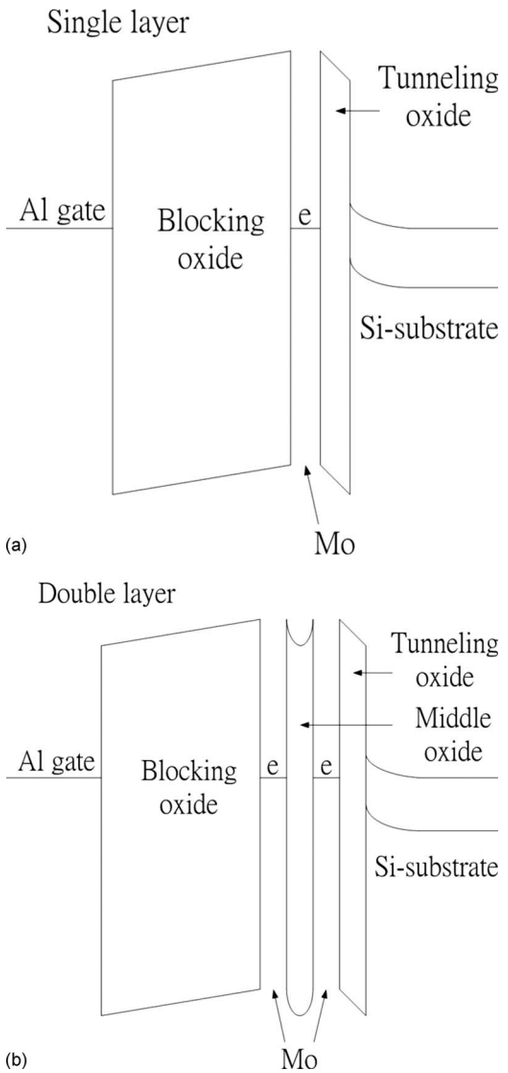

Figure 9. Band diagrams of (a) single- and (b) double-layer structures in retention.

Conclusion

Mo nanocrystals embedded in SiO_x were fabricated for nonvolatile memory application through thermal annealing an oxygen-incorporated Mo silicide layer. The average size and density of the Mo nanocrystals was estimated at about 4 nm and 1×10^{-12}, respectively. The XPS results indicated the existence of Mo oxide and SiO_x in the oxygen-incorporated Mo silicide layer after an 800°C anneal and the Mo oxide was reduced after a 900°C anneal. The 900°C-annealed sample had better retention (65%) and a larger memory window (3.6 V) than the 800°C-annealed sample due to the reduction of Mo oxide. Furthermore, the double-layer nanocrystal memory was fabricated through annealing the stacked oxygen-incorporated Mo silicide layer at 900°C. The results showed that the double-layer structure has a larger memory window (6.6 V) and better retention (51%) than the single-layer structure (23%) at 85°C. Therefore, the double-layer structure, which can enhance memory characteristics, is promising for applications in nonvolatile memory.

Acknowledgments

This work was performed at National Nano Device Laboratories, Taiwan. The authors acknowledge the financial support of the National Science Council (NSC) under contract no. NSC 96-2221-E-009-202-MY3, NSC 96-2112-M-110-013, and NSC-97-3114-M-110-001.

National Sun Yat-Sen University assisted in meeting the publication costs of this article.

References

1. S. Tiwari, F. Rana, K. Chan, H. Hanafi, W. Chan, and D. Buchanan, *Tech. Dig. - Int. Electron Devices Meet.*, **1995**, 521.
2. S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbe, and K. Chan, *Appl. Phys. Lett.*, **68**, 1377 (1996).
3. J. D. Blauwe, *IEEE Trans. Nanotechnol.*, **1**, 72 (2002).
4. C. H. Tu, T. C. Chang, P. T. Liu, H. C. Liu, S. M. Sze, and C. Y. Chang, *Appl. Phys. Lett.*, **89**, 162105 (2006).
5. T. L. Li, W. L. Ho, H. B. Chen, C. H. Wang, C. Y. Chang, and C. Hu, *IEEE Trans. Electron Devices*, **53**, 1420 (2006).
6. C. Lee, J. H. Kwon, J. S. Lee, Y. M. Kim, Y. Choi, H. Shin, J. Lee, and B. H. Sohn, *Appl. Phys. Lett.*, **91**, 153506 (2007).
7. C. B. Roxlo, H. W. Deckman, J. Gland, S. D. Cameron, and R. R. Chianelli, *Science*, **235**, 1629 (1987).
8. Y. C. Lu and C. R. Clayton, *Corros. Sci.*, **29**, 927 (1989).
9. T. S. Sian and G. B. Reddy, *Sol. Energy Mater. Sol. Cells*, **82**, 375 (2004).
10. S. S. Chao, Y. Takagi, G. Lucovsky, P. Pai, R. C. Custer, J. E. Tyler, and J. E. Keem, *Appl. Surf. Sci.*, **26**, 575 (1986).
11. J. X. Wu, M. S. Ma, H. G. Zheng, H. W. Yang, J. S. Zhu, and M. R. Ji, *Phys. Rev. B*, **60**, 17102 (1999).
12. R. Mitra, *Int. Mater. Rev.*, **51**, 13 (2006).

Downloaded on 2014-04-25 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).