國立交通大學

電機資訊學院 電信學程

碩 士 論 文

KU-Band 頻率合成器設計

KU-Band frequency synthesizer design

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KU-Band 頻率合成器設計

KU-Band frequency synthesizer design

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KU-Band 頻率合成器設計

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摘　　要

本論文主要分為二部份，使用離散元件(distributed component)設計 Ku-band 頻率合成器及利用 0.25um CMOS 技術來模擬 5GHz RF 電路。

在 Ku-band 的頻率合成器的設計上，以壓控介質振盪器(VTDRO)為基礎，加上鎖相迴路(PLL)及自動增益控制(AGC)電路。其中，PLL 電路將根據控制界面的設定值，來控制 VTDRO 的頻率。而 AGC 電路使整個頻率合成器的輸出功率保持在一個固定值，改善 VTDRO 因為輸出頻率的變化而產生輸出功率的變動(output power flatness) 。相對的，AGC 電路也能根據控制界面的設定值，來控制 VTDRO 的輸出功率。最後我們利用 LabVIEW*來設計控制界面，使頻率合成器的頻率和輸出功率皆能被電腦的 Print port 控制和設定。最後，頻率合成器的頻率可由 11.22GHz 到 11.28GHz 之間變換，相位雜訊為–96dBc/Hz at 100kHz，輸出功率平坦度為 ±0.62dB，輸出功率從+4dBm 到 –15dBm。

在第二部份，利用 0.25um CMOS 技術來模擬 5GHz 壓控振盪器和除頻器電路。整理出積體電路(integrated circuit) 在設計上所必須遵行的流程與準則。

* : LabVIEW 是由 National Instruments 所發展的圖控系統。

KU-Band frequency synthesizer design

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ABSTRACT

The thesis is divided into two parts. In the section 1, we describe the Ku-band synthesizer. Section 2 describes the CMOS RF circuits simulation for the 5GHz frequency range.

In the Ku-band synthesizer, the voltage tuned dielectric resonator oscillator (VTDRO), Phase-locked loop (PLL) controller and automatic gain control (AGC) circuits are combined by the distributed devices. The synthesizer frequency and output power level could be control by PLL and AGC control loop. Finally, the measured phase noise is –96dBc/Hz at 100kHz offset from 11.25GH. The dynamic range of output power from +4dBm to –15dBm was achieved by the AGC function and ±0.62dB output power flatness.

In the CMOS RF circuits simulation section, the 5GHz LC-tank voltage controlled oscillator and high frequency divider has been designed in a standard 0.25u CMOS process.

誌　　謝

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目　　錄

Chapter 1
Introduction

The thesis is divided into two parts. In the section 1, we describe the Ku-band synthesizer. The major goals in the design of a Ku-band frequency synthesizer are achieve low phase noise and output power can be set.

Section 2 describes the CMOS RF circuit simulation for the 5GHz frequency range.

1-1 Outline of Ku-band synthesizer

Nowadays in communication technology, the communication system, were all requests to have the stable communication frequency, the channel switching and stable input/output power. Figure1-1 shows the conventions Ku-band frequency synthesizer. The structure can be tuned frequency by the Phase-locked loop (PLL) control lines and the output power is fixed. Unfortunately, the output power was changed by the tuning frequency of Voltage Controlled Oscillator. (See figure1-2)

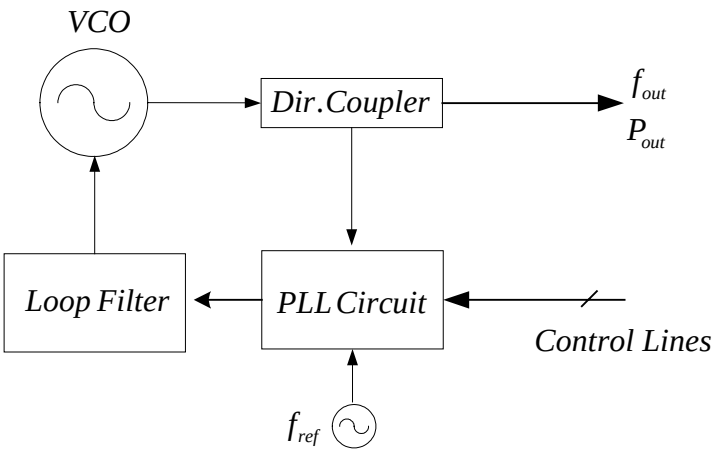


Figure 1-1 the structure of conventions Ku-band frequency synthesizer

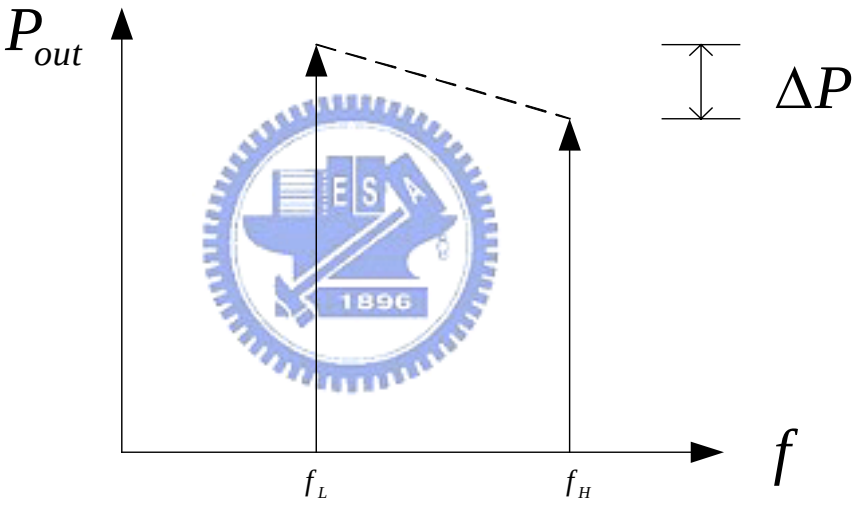
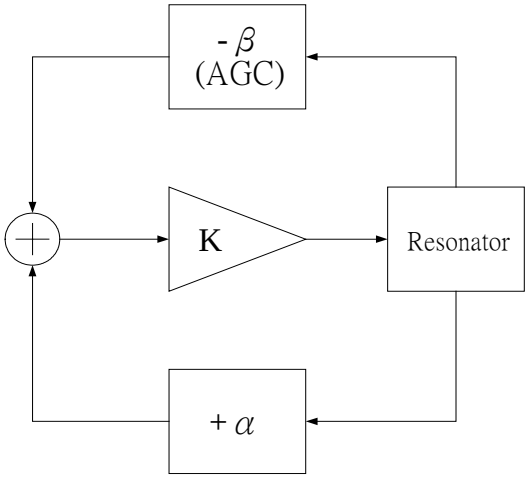
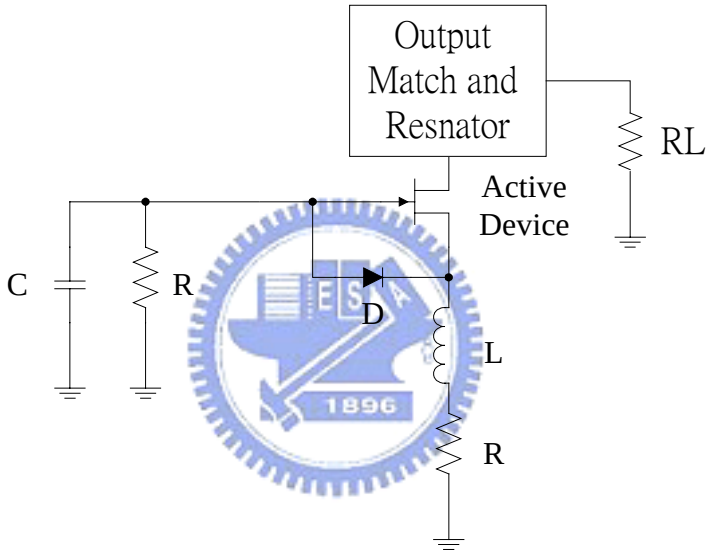


Figure 1-2 the output spectrum conventions Ku-band frequency synthesizer

The amplitude stability method of oscillator is presented [40][41][42][43]. Conventional diagram are shown in figure1-3. The Diode is automatic gain control (AGC) circuit and it controls the active device current and stables the amplitude of oscillator. In this thesis, we will discuss how to achieve frequency and power level control loops.



(a)



(b)

Figure 1-3 the convention diagram of Oscillator with AGC circuit (a) convention diagram (b) typical circuit

Usually, if we add AGC circuit into oscillator, we'll consider some condition. The condition shows as follows:

(1) In the fast channel switch case, oscillator maybe cannot oscillation.

(2) Keeping open loop gain of oscillator on the width temperature range operation. The suitable open loop gain can reduce phase noise.

The Ku-band frequency synthesizer of this thesis is shown as figure 1-4. The voltage tuned dielectric resonator oscillator (VTDRO), Phase-locked loop (PLL) controller and automatic gain control (AGC) circuits are combined by the distributed devices. The VTDRO produced high quality Ku-band frequency and output power. PLL controller does changing frequency of VTDRO. The flatness of output power can be compensated by the AGC function (see figure figure1-5).

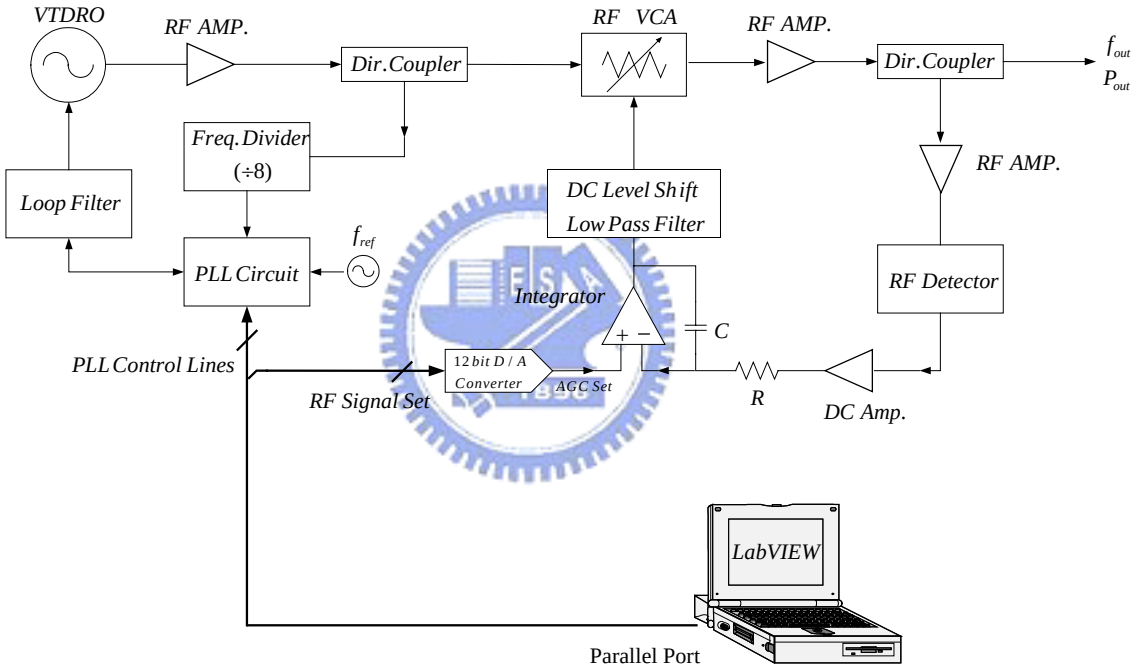


Figure 1-4 the structure of new Ku-band frequency synthesizer

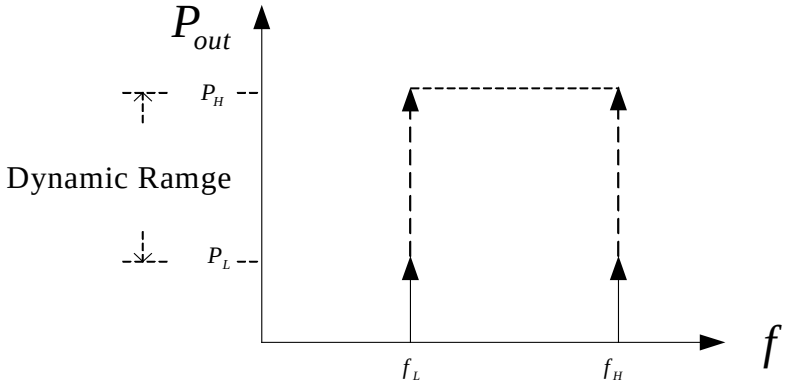


Figure 1-5 the output spectrum new Ku-band frequency synthesizer

In other words, the synthesizer frequency and output power level could be control by PLL and AGC control loop. Finally, the measured phase noise is –96dBc/Hz at 100kHz offset from 11.25GH. The dynamic range of output power from +4dBm to –15dBm was achieved by the AGC function and 75MHz bandwidth frequency tuned range.

1-2 Outline of CMOS RF circuit simulation

In the CMOS RF circuit simulation section, the 5GHz LC-tank voltage controlled oscillator and high frequency divider has been designed in a standard 0.25u CMOS process.

1-3 Outline of thesis

In this thesis, voltage tuned dielectric resonator oscillator (VTDRO) and Phase-lock loop controller is discussed in Chapter 2. In Chapter 3, an automatic gain control (AGC) loops that circuit and implementation of the structure is shown. Finally, full structure of Ku-band frequency synthesizer is done.

At the last, the integration of the CMOS RF circuit, including VCO and frequency divider is done in Chapter 4. The conclusions are given in Chapter 5.

Chapter 2

KU-Band Frequency Control Loop Design

In this chapter, we will discuss theory KU-Band frequency control loop design and implementation. The block diagram is shown as figure 2-1.

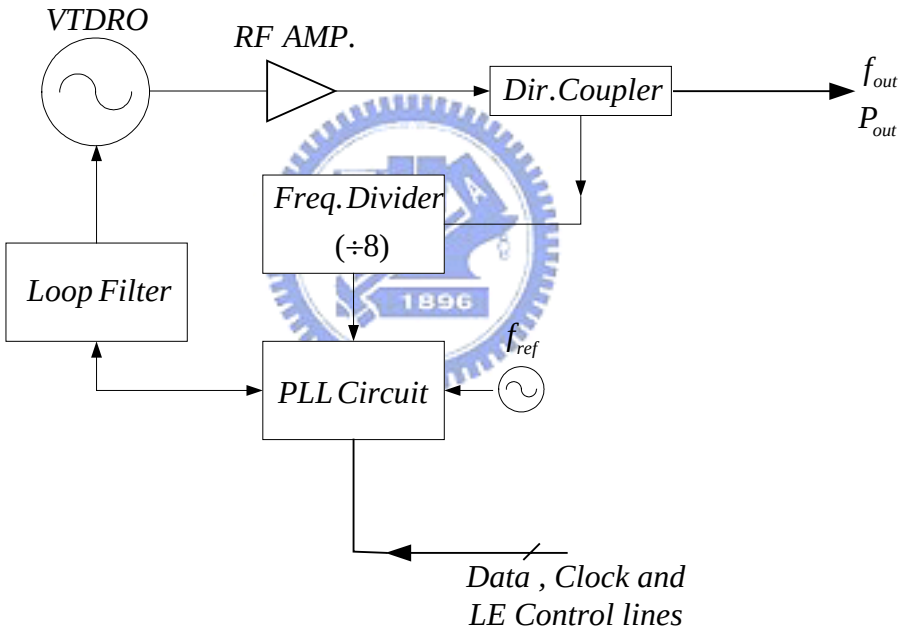


Figure 2-1 KU-Band frequency control loop block diagram

2-1 Outline of Theory

2-1-1 Outline of Phase-Lock Loop [3][4]

Figure 2-2 shows a basic Phase-Lock Loop. The compared frequency of the phase detector is f_{comp} and

$$f_{comp} = f_{div} = f_{ref} \tag{2-1}$$

The output frequency of the VCO is expressed by

$$f_{VCO} = N \times f_{div} \tag{2-2}$$

The frequency switching is performed by changing the count number N. The spacing between channels is given by

$$f_{ch} = f_{comp} \times (N+1) - f_{comp} = f_{comp} \tag{2-3}$$

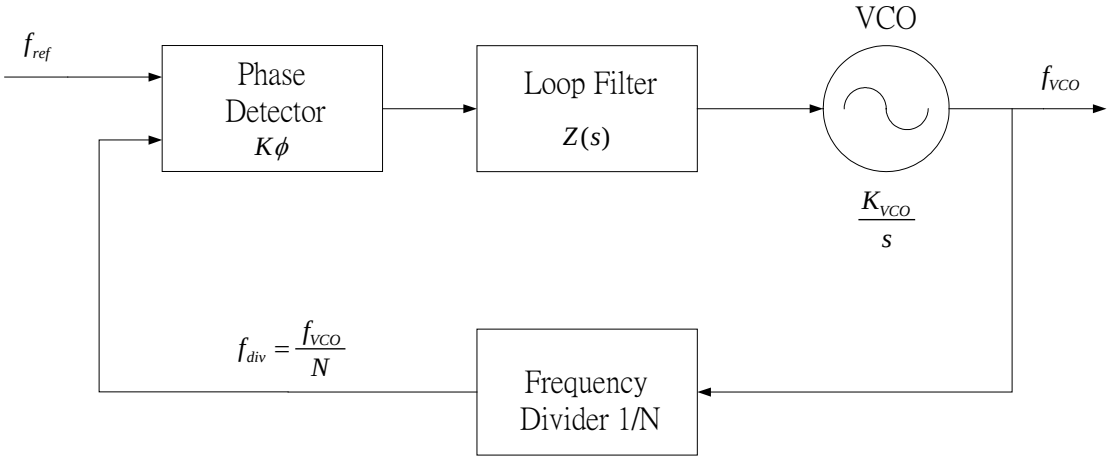


Figure 2-2 basic Phase-Lock Loop

From (2-3), clearly shows that reference frequency is equal to the frequency spacing. The primary function of loop filter is reducing ripple into the VCO. That bandwidth determines how fast the PLL can correct any phase error. In generally, the resultant versus bandwidth can be describe as follows:

(1) A PLL with narrow bandwidth can reject the input noise but cannot correct the VCO timing errors quickly. The resultant output noise is VCO noise limited and provides more stable PLL design.

(2) A PLL with wider bandwidth can correct VCO errors. However, if the bandwidth is too wide, the resultant system is input noise limited.

In addition, the following categories cover most of the common causes of PLL output noise.

(a) Power supply noise.

(b) PLL dead-zoom region.

(c) Noise from input reference/feedback signal.

(d) Internal switching noise.

(e) Internal and external crosstalk/reflection noise.

Figure 2-3 shows a third order filter topology and constant define as follow:

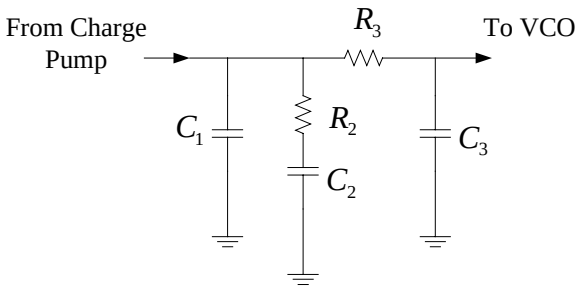


Figure 2-3 third order filter topology

and transfer function of the loop filter is given by

$$\begin{aligned} T_0 &= C_2R_2 \\ T_1 &= C_1C_2C_3R_2R_3 \\ T_2 &= C_2C_3R_2 + C_1C_2R_2 + C_1C_3R_3 + C_2C_3R_3 \\ T_3 &= C_1 + C_2 + C_3 \end{aligned} \tag{2-4}$$

and

$$Z(s) = \frac{1+sT_0}{s[s^2T_1 + sT_2 + T_3]} \tag{2-5}$$

The close-loop transfer function for figure 2-2 is

$$Z_{CL}(s) = \frac{K\phi K_{VCO}N(1+sT_0)}{s^4NT_1 + s^3NT_2 + s^2NT_3 + sK\phi K_{VCO}T_o + K\phi K_{VCO}} \tag{2-6}$$

In this case, (2-6) will be approximated by a second order expression. It is assumed that these higher order terms are small relative to the lower order terms. The Initial Value Theorem (2-7) suggests that the consequences of ignoring these terms are more

on the initial characteristics, such as overshoot, and less on long time behavior, such as lock time.

$$\lim_{s\to\infty} sY(s) = \lim_{t\to 0} y(t) \tag{2-7}$$

The simplified second order close-loop transfer function expression is

$$Z_{CL}(s) = \frac{[\frac{K\phi K_{VCO}}{NT_3}](1+sNT_0)}{s^2 + s(\frac{K\phi K_{VCO}T_0}{T_3 N})} \tag{2-8}$$

and

$$\omega_n = \sqrt{\frac{K\phi K_{VCO}}{N(C_1+C_2+C_3)}}$$
$$\xi = \frac{R_2 C_2 \omega_n}{2} \tag{2-9}$$

It can be seen that the poles of this function are at:

$$-\xi\omega_n \pm j\omega_n\sqrt{1-\xi^2} \tag{2-10}$$

Now consider a PLL, which is initially locked at frequency f_1, and the N counter is changed such to cause the PLL to switch to frequency f_2. It should be noted that the value for N that is used in all of these equations should be the value of N corresponding to f_2. This event is equivalent to changing the reference frequency from $\frac{f_1}{N}$ to $\frac{f_2}{N}$. The first terms in the numerator (2-8) shows the primary effects, and the second expression shows the secondary effects due to the zero. The zero in the transfer function has a lot of effect on the overshoot and the rise time, but has little effect on the lock time. Using inverse Laplace transforms it follows that the time frequency response is:

$$F(t) = f_2 + (f_1 - f_2)e^{-\xi\omega_n t}[\cos(\omega_n t\sqrt{1-\xi^2}) + \frac{\xi - R_2C_2\omega_n}{\sqrt{1-\xi^2}}\sin(\omega_n t\sqrt{1-\xi^2})] \quad (2\text{-}11)$$

Since the term in brackets has a maximum value of

$$\frac{1 - 2\xi R_2C_2\omega_n + R_2{}^2C_2{}^2\omega_n}{\sqrt{1-\xi^2}} \quad (2\text{-}12)$$

It follows that the lock time in seconds is given by

$$LockTime = \frac{-\ln[\frac{tol}{f_2 - f_1}\frac{\sqrt{1-\xi^2}}{1 - 2\xi R_2C_2\omega_n + R_2{}^2C_2{}^2\omega_n}]}{\xi\omega_n} \quad (2\text{-}13)$$

Many times , this is approximated by

$$LockTime = \frac{-\ln[\frac{tol}{f_2 - f_1}\sqrt{1-\xi^2}]}{\xi\omega_n} \quad (2\text{-}14)$$

Figure 2-4 shows the second order model for the frequency response.

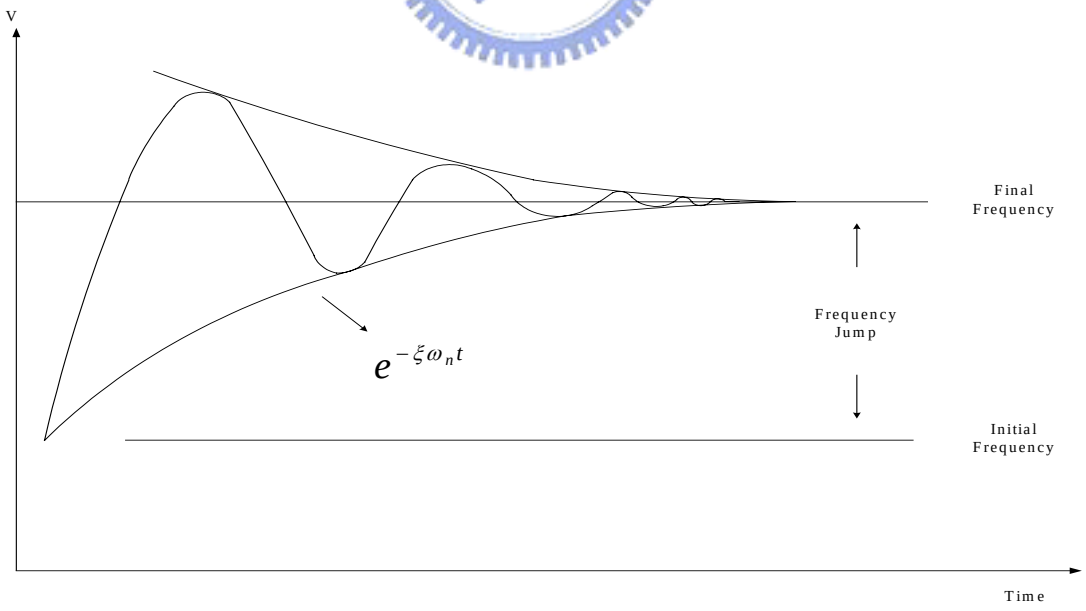


Figure 2-4 second order model for the frequency response

For second order filter, the following relationships exist for loop filters design. These relationships are given by

$$\omega_c = 2\xi\omega_n$$
$$\sec\phi - \tan\phi = \frac{1}{4\xi^2} \tag{2-15}$$

2-1-2 Outline of Oscillator [1][39]

This section describes a method of designing oscillators using small signal S-parameters. Microwave transistors can be used for both amplifier and oscillator application. Form the small signal S-parameters of the transistor, the stability factor k can be calculated form:

$$k = \frac{1+|D|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{21}||S_{12}|} \tag{2-16}$$

where

$$D = S_{11}S_{22} - S_{21}S_{12} \tag{2-17}$$

The k>1 is unconditionally stable of transistor at any frequency. This condition guarantees that at the specified frequency the transistor will not oscillate into any termination at either port that has a positive resistance.

If we can design a circuit for which k<1 and either Γ_r or Γ_L is in the unstable region, we will in reality have designed an oscillator (See figure 2-5).

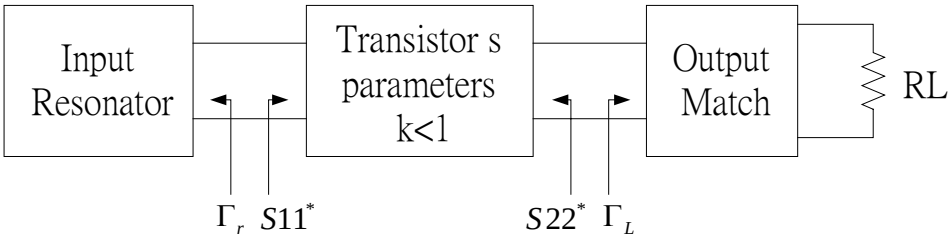


Figure 2-5 Block diagram of microwave oscillator

The necessary conditions for oscillation is given by:

$$K<1 \tag{2-18}$$

$$S_{11}^{*}\Gamma_r = 1 \quad \text{and} \quad S_{22}^{*}\Gamma_L = 1 \tag{2-19}$$

If the active device selected has a stability factor grater than one at the desired frequency of oscillation, condition (2-18) can be achieved either by changing the two-port configuration or by adding feedback .For example, the source reactance will define the amount of negative resistance at gat of active device (see figure 2-6).

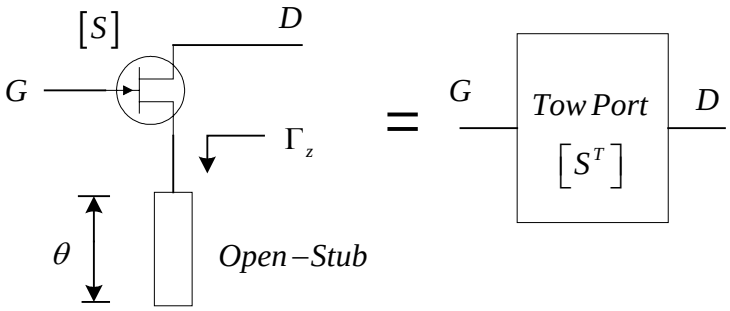


Figure 2-6 negative resistance generator

The new S-parameters will redefine as follower:

$$[S]=\begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \tag{2-20}$$

$$[S^T]=\begin{bmatrix} S_{11}^T & S_{12}^T \\ S_{21}^T & S_{22}^T \end{bmatrix}=\begin{bmatrix} S_{11}+\dfrac{S_{31}S_{13}\Gamma_z}{1-S_{33}\Gamma_z} & S_{12}+\dfrac{S_{13}S_{32}\Gamma_z}{1-S_{33}\Gamma_z} \\ S_{21}+\dfrac{S_{31}S_{23}\Gamma_z}{1-S_{33}\Gamma_z} & S_{22}+\dfrac{S_{23}S_{32}\Gamma_z}{1-S_{33}\Gamma_z} \end{bmatrix} \tag{2-21}$$

From (2-21), we will adjust the electrical length (θ) of open-stub to generation for the $|S_{11}^T|>1$ *or* $|S_{22}^T|>1$. Condition (2-19) simply confirms that the oscillator produces power at both ports. If either condition in (2-19) is satisfied, the other condition is automatically satisfied. Once we have achieved k<1, condition (2-19) gives the necessary relationship to complete the oscillator design. We will adopt the technique of resonating the input port and designing a match that satisfies condition (2-19) at the output.

With k<1 we know that an input matching circuit having Γ_r which produces $|S22^*|>1$ can be found. The design condition is therefore

$$\left|S22^{*}\right|>1 \qquad (2\text{-}22)$$

This condition can be viewed as stating that there is a negative resistance at that output port of the terminated transistor. There are many techniques for realizing such an input circuit, or resonator. One method is to use a computer simulation and optimize for the condition that S_{11} of the one port consisting of the resonator cascaded with the transistor is greater than unity. A resonator satisfying the property that $\left|\Gamma_r\right|=1$ is lossless. In general, the lossless resonator have cavity resonator,YIG, Dielectric Resonator, lossless transmission lines and lossless lumped Element. With the input circuit established, the load circuit is designed to satisfy

$$\Gamma_L=\frac{1}{S22^{*}} \qquad (2\text{-}23)$$

which follows directly form condition (2-19). Note that since $\left|S22^{*}\right|>1$, this equation guarantees $\left|\Gamma_L\right|<1$, i.e. the load resistor will be positive.

For the special case where the oscillator is intended to oscillate directly into a 50Ω load, no load circuit needs to be designed , and the condition for oscillation can be re–expressed . If the load is 50Ω, $\Gamma_L=0$. Therefore, since $\left|S22^{*}\right|\Gamma_L=1$, we have $\left|S22^{*}\right|=\infty$. In practices it has proven sufficient to design for

$$\left|S22^{*}\right| > 100 \qquad (2\text{-}24)$$

Satisfying condition (2-19)requires $\left|\Gamma_L\right| < 0.01$, which corresponds to a load that is essentially $50\,\Omega$.

The above method will only predict the frequency of oscillation. It provides no information about output power, harmonics, phase noise, or other parameters of possible interest. In general the output power of the oscillator will approach the 1 dB compression power (P_{1dB}) of the transistor used as an amplifier if the dc bias is designed for maximum P_{1dB}. Other performance parameters would typically have to be measured from the finished oscillator.

2-1-3 Outline of frequency resonator [1][14] [37]

Resonant circuits are importance for oscillator circuit. It will be worthwhile to review some of these by using a lumped RLC parallel network. Figure 2-7 show a typical resonant circuit.

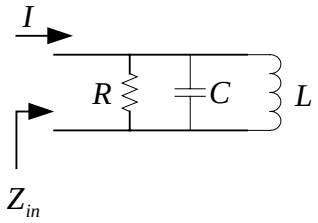


Figure 2-7 typical resonant circuit

The resonant frequency ω_0 is found by

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{2-25}$$

The quality factor is important parameter specifying the frequency selectivity. It general definition given by

$$Q = \omega RC = \frac{R}{\omega L} \tag{2-26}$$

Because of resistor R represents the losses in the resonant circuit, The Q is called the unloaded Q and denoted Q. From RLC parallel network, the input impedance can be expressed in a relatively simple form. We have

$$Z_{in} = (\frac{1}{R} + \frac{1}{j\omega L} + j\omega C)^{-1} = (\frac{1}{R} + j\omega_0 C + j\Delta\omega C + \frac{1 - \frac{\Delta\omega}{\omega_0}}{j\omega_0 L})^{-1} \tag{2-27}$$

and

$$\omega = \omega_0 + \Delta\omega \tag{2-28}$$

A plot of Z_{in} as a function of $\frac{\Delta\omega}{\omega_0}$ is given in figure 2-8

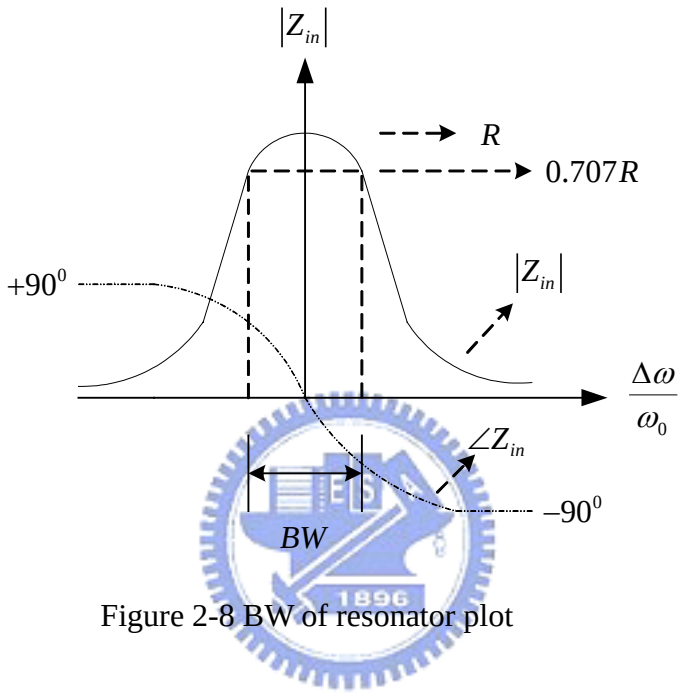


Figure 2-8 BW of resonator plot

The frequency bandwidth between the $0.707R$ point is twice this; hence

$$Q = \frac{\omega_0}{2\Delta\omega} = \frac{1}{BW} \tag{2-29}$$

If the resonant circuit is coupled to an external load that loading effect can be represented by an additional resistor RL in parallel with R. It is reduce the resistance and the new quality factor is also smaller.

The new quality factor is called the loaded Q and denoted Q_L. hence

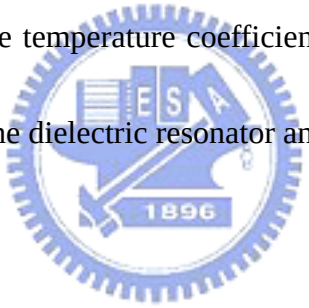
$$Q_L = \frac{RR_L \big/ R + R_L}{\omega L} \tag{2-30}$$

Unfortunately, the lumped circuit has too high losses at microwave frequency that are from conductor loss and radiation loss. In order to achieve the purpose of high-quality microwave system, the primary characteristics of the ceramic material to be used for dielectric resonators (DR) are:

(1) The dielectric constant (ε_r), which can reduce the size of the DR.

(2) The quality factor (Q), which is approximately equal to the inverse of the loss tangent.

(3) The temperature coefficient of the resonant frequency (τ_f), which include the combined effects of the temperature coefficient of the dielectric constant and the thermal expansion of the dielectric resonator and the shielding package.



The dielectric calculations can be performed using techniques given by Kajfez[2]. The DR resonates in various mode at frequency determined both by its dimensions and its surroundings. Figure 2-9 shows the cylindrical dielectric is placed on a dielectric substrate. From the electromagnetic wave theory, both magnetic and electric field of outside and inside of dielectric material must satisfy the Maxwell equation and boundary condition.

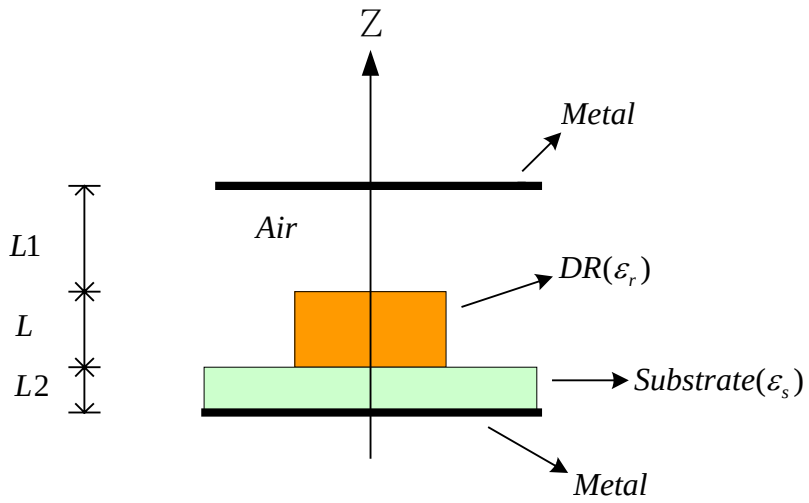


Figure 2-9 a shows the cylindrical dielectric is placed on a dielectric substrate

In the $TE_{01\delta}$ mode, magnetic field lines are contained in the meridian plane while the electric field lines are concentric circles around z-axis as shown in figure 2-10. For a distant observer, this mode appears as a magnetic dipole, and for this reason it is sometimes referred-to as the “magnetic dipole mode”. When the relative dielectric constant is around 40,more than 95% of the stored electric energy, and more than 60% of the stored magnetic energy is located within the cylinder. The remaining energy is distributed in the air around the resonator, decaying rapidly with distance away from the resonator surface.

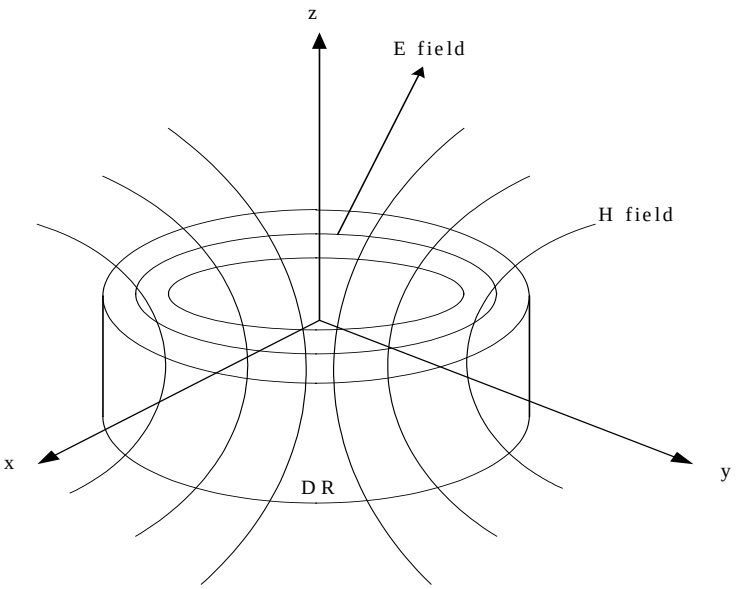
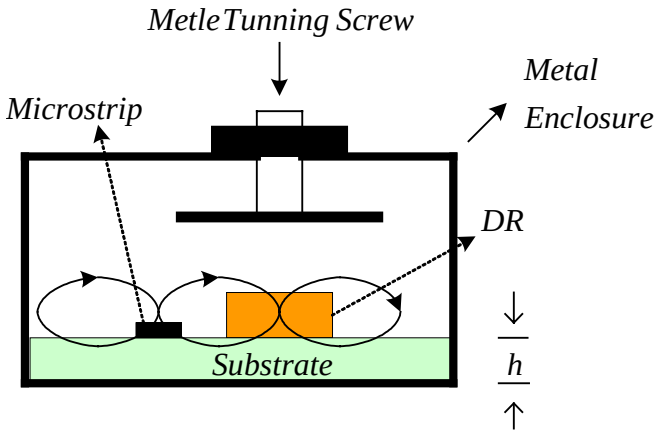


Figure 2-10 Field distribution of $TE_{01\delta}$ mode in a DR

The DR is often used in conjunction with a microstrip line. Figure 2-11 a shows the DR coupled to a microstrip line and corresponding equivalent circuit.



(a)

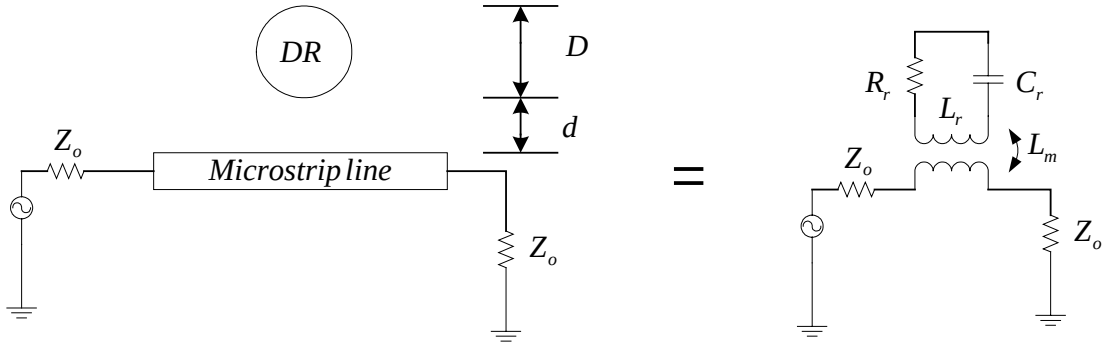


Figure 2-11 Basic DR coupling structure (a) DR coupled to a microstrip line (b) corresponding equivalent circuit

The characteristics in corresponding equivalent circuit of DR are defined by the resonator capacitance(Cr), resonator impedance(Lr), resonator resistance(Rr), while mutual inductance(Lm) give the coupling factor. These parameters are related to the distance from the lines to the DR and surrounding metallic enclosure.

The DR equivalent circuit transforms into parallel RLC resonator in series with the line (see figure 2-12). The RLC value are given by:

$$R = \omega_0 Q_U \frac{L_m^2}{L_r} \tag{2-31}$$

$$L = \frac{L_m^2}{L_r} \tag{2-32}$$

$$C = \frac{L_r}{\omega_o^2 L} \tag{2-33}$$

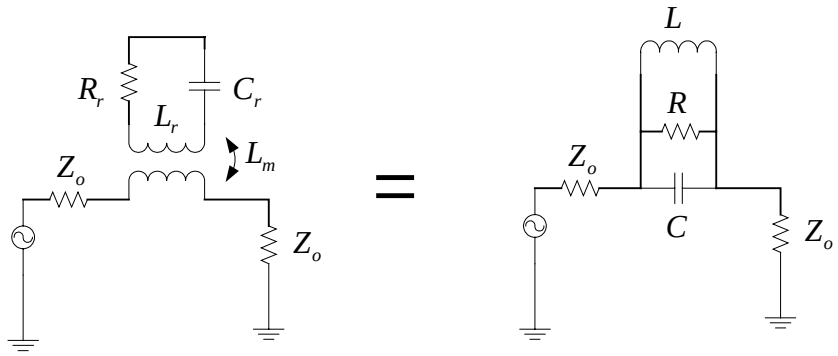


Figure 2-12 DR equivalent circuit transforms into parallel RLC resonator

This circuit generally provides sufficient accuracy for computer simulation and all parameter are easily extracted via the fitting of measurements.

At the resonant frequency of the DR, The S-parameters of the configuration can be extraction. it are given by[14]:

$$\beta = \frac{Q_U}{Q_E} = \frac{R}{R_E} = \frac{R}{2Z_0} = \frac{S_{11}}{S_{21}} \tag{2-34}$$

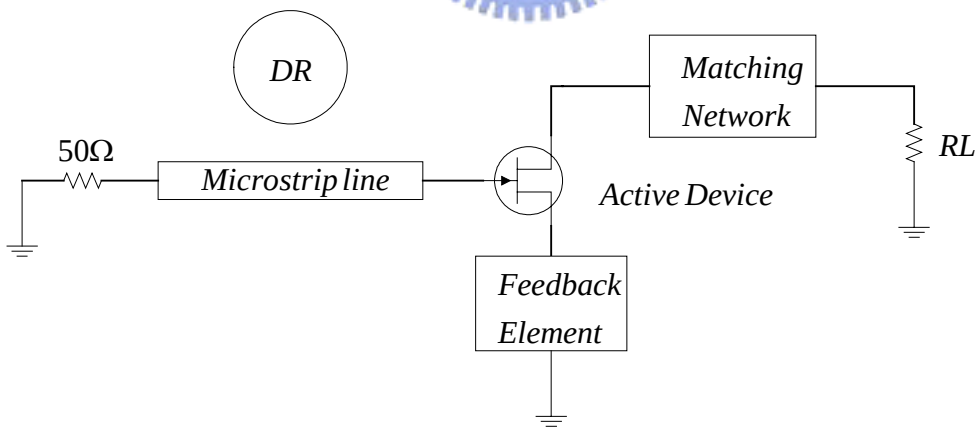
The Q_U is the unloaded Q of the circuit. That is

$$Q_U = \frac{R}{\omega_o L} = \omega_o RC = \frac{\omega_0}{BW} \tag{2-35}$$

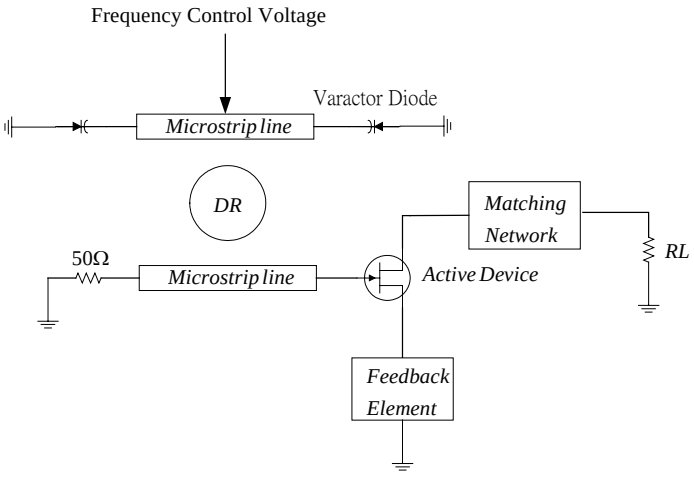
At present, commercially available temperature stable DR materials exhibit dielectric constants of about 36 to 40. Numerous references are available describing the advantages of different ratio in height (h), and diameter (D) from dielectric resonator manufacturers. However, a choice of H/D = 0.4 is recommended to avoid spurious modes oscillations and optimal Q_U .

2-1-4 Basic Configuration DRO Type [38]

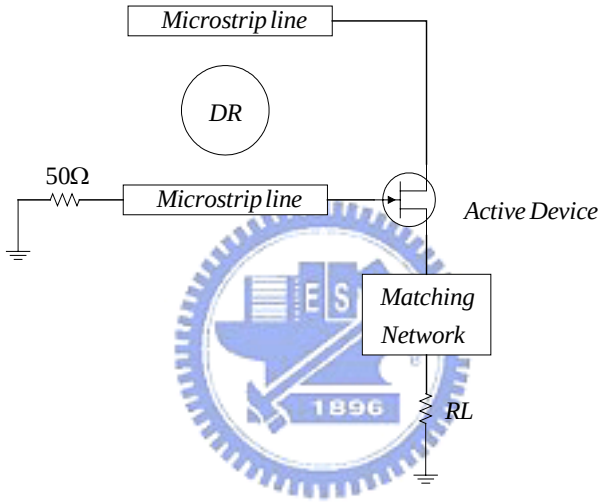
The basic configurations of the DRO are series feedback and parallel feedback. Figure 2-13 shows different configurations of each type.



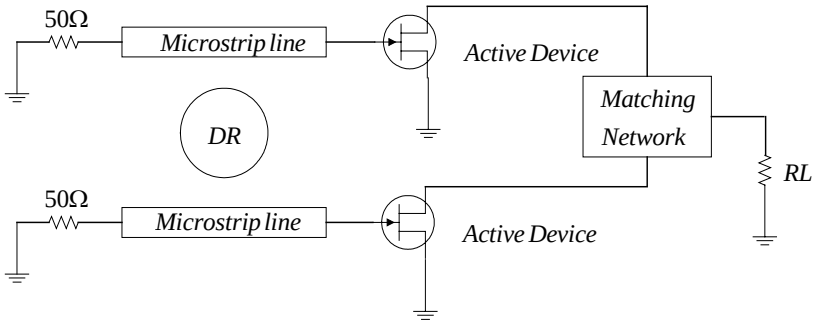
(*a*)



(*b*)



(*c*)



(*d*)

Figure 2-13 Basic DRO configurations (a) series feedback DRO (b) VTDRO (c) parallel feedback (d) Push-Push DRO

The Push-Push DRO is special circuit and it uses a common DR for two transistors. The fundamental frequency is cancelled and second harmonics are added at output of the oscillator.

2-2 VTDRO Design Procedures

The Ku-band VTDRO design technique based on small-signal parameter in a linear simulation. The linear simulation will provide a good initial circuit layout. In this thesis, the simulation software of Microwave Office is used.

The DRO can be designed using following design procedure [14]:

(1) The first step is choosing the DRO configuration.

(2) Select a DR that is resonant at design frequency, and measure the S-parameters of DR with microstrip line.

(3) This step is choosing the active device that is capable of oscillation at the design frequency. The linear S-parameters are taken from manufacturers' data. A linear simulation will provide a good initial circuit layout before fin tuning the design. For the available output power, that will then be about 10 to 20 percent of the product $V_{ds}I_{dss}$.

(4) Add a feedback element to ensure that the stability factor of the active device is less than unity. It is negative resistance of active device to make oscillation. For

example, the source reactance will define the amount of negative resistance at gat of active device (see figure 2-14).

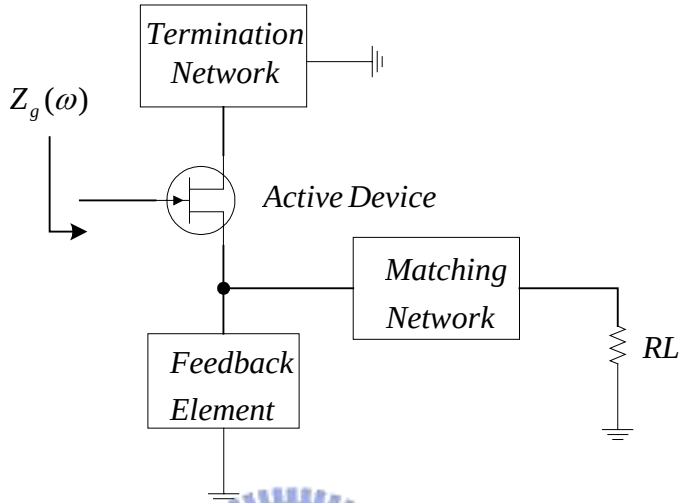


Figure 2-14 negative resistance of active device

(5) From an active one-port that consists of the feedback element, the active device, the matching network and the load, as shown in figure 2-14.

(6) This step is adjustment of the electrical length (θ) to compensate for the imaginary part of $Z_g(\omega)$ by the opposite value (see figure 2-15).

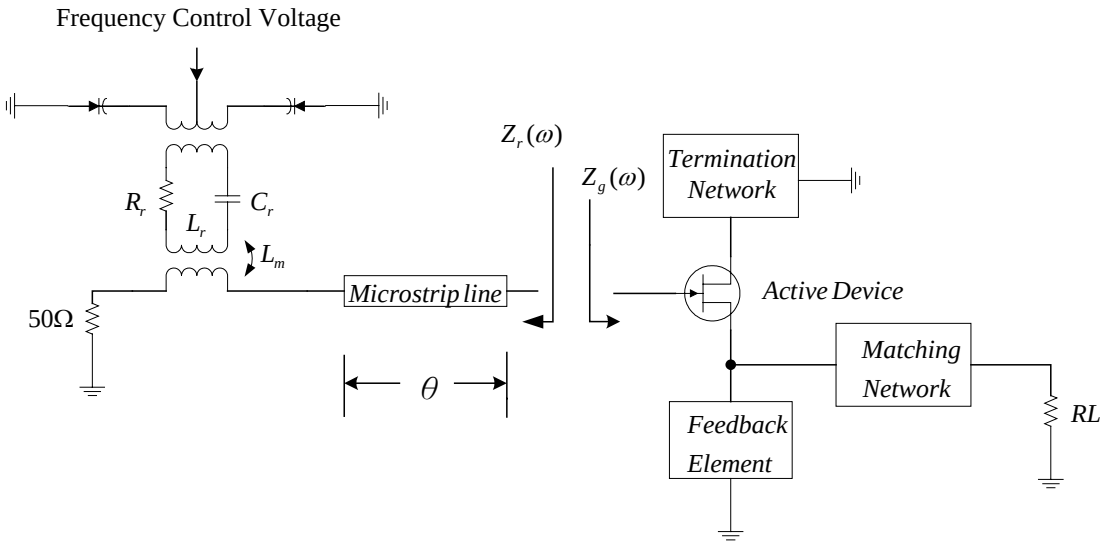


Figure 2-15 VTDRO design configuration

2-2-1 Frequency Resonator Simulations

In this case, the Ku-band DRO design was achieved by the design procedure. The DRO configuration chosen is series feedback VTDRO (see figure 2-13(b)), An advantage of the series feedback design is the relative ease of coupling to a single line, compared to the parallel circuit's requirement for coupling to two lines. The parameters of DR acquirement show as follows:

1.We can be extracted parameters of DR by the network analyzer.

2.The parameter is providing by the manufacturers.

From method 1, the DR is placed on top of the microstrip substrate in the metal

enclosure and extracting the intrinsic parameters of the DR equivalent circuit. We can be extracted parameters of DR by the network analyzer. This is easily achieved with the use of software programs such as microwave offices. Figure 2-16 shows the measurement setup of DR.

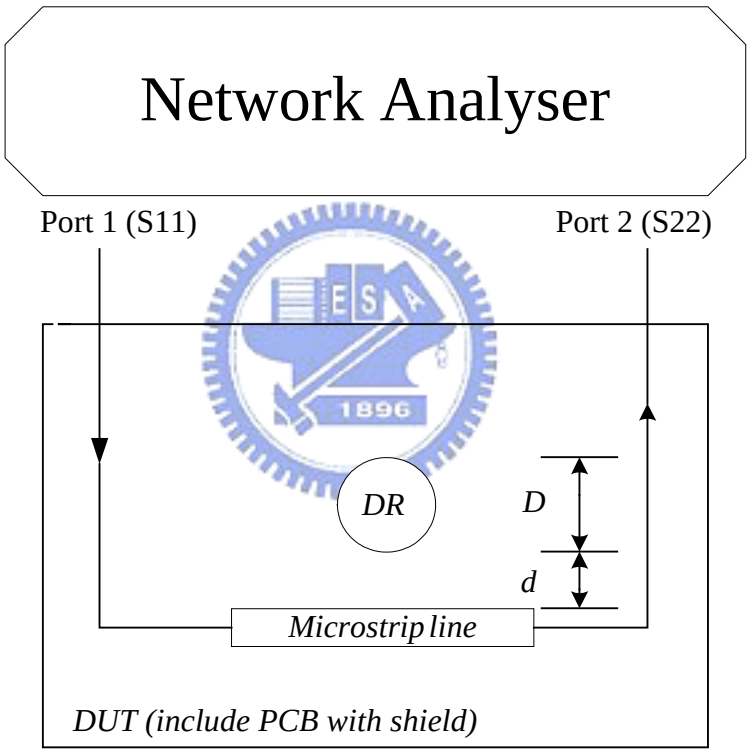
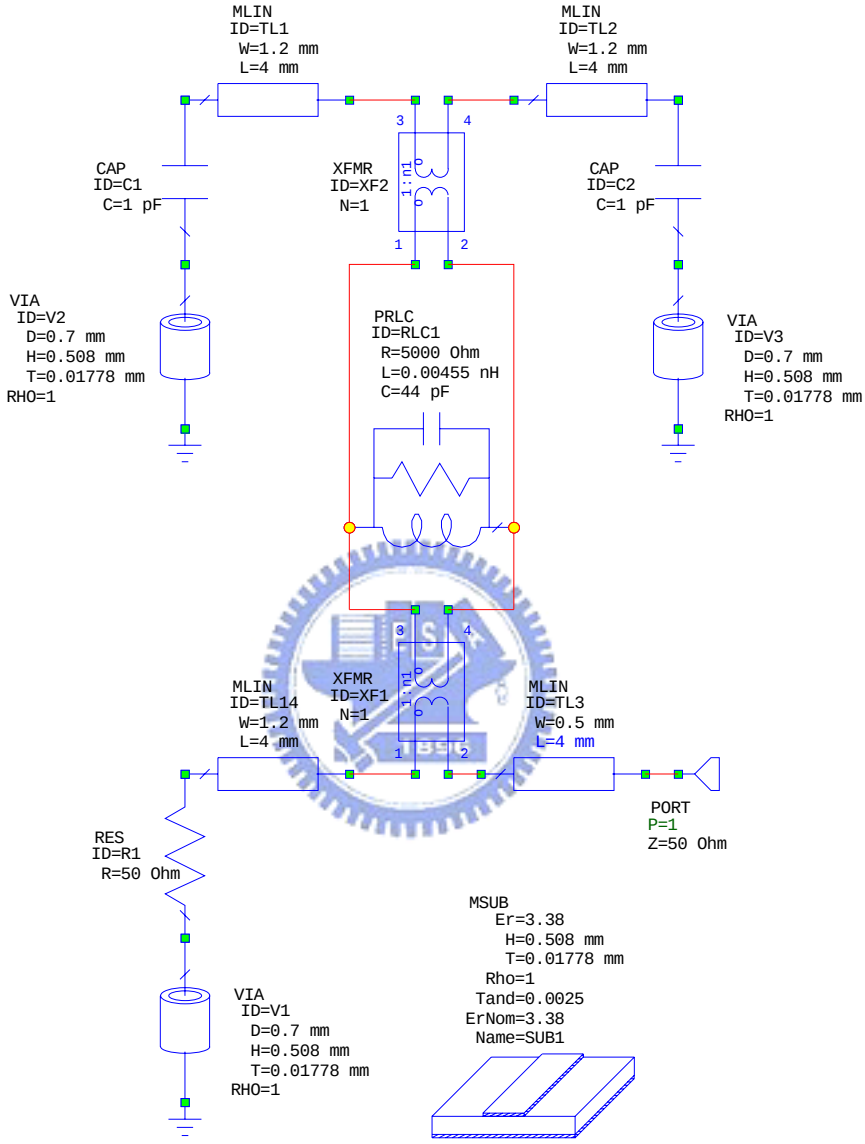
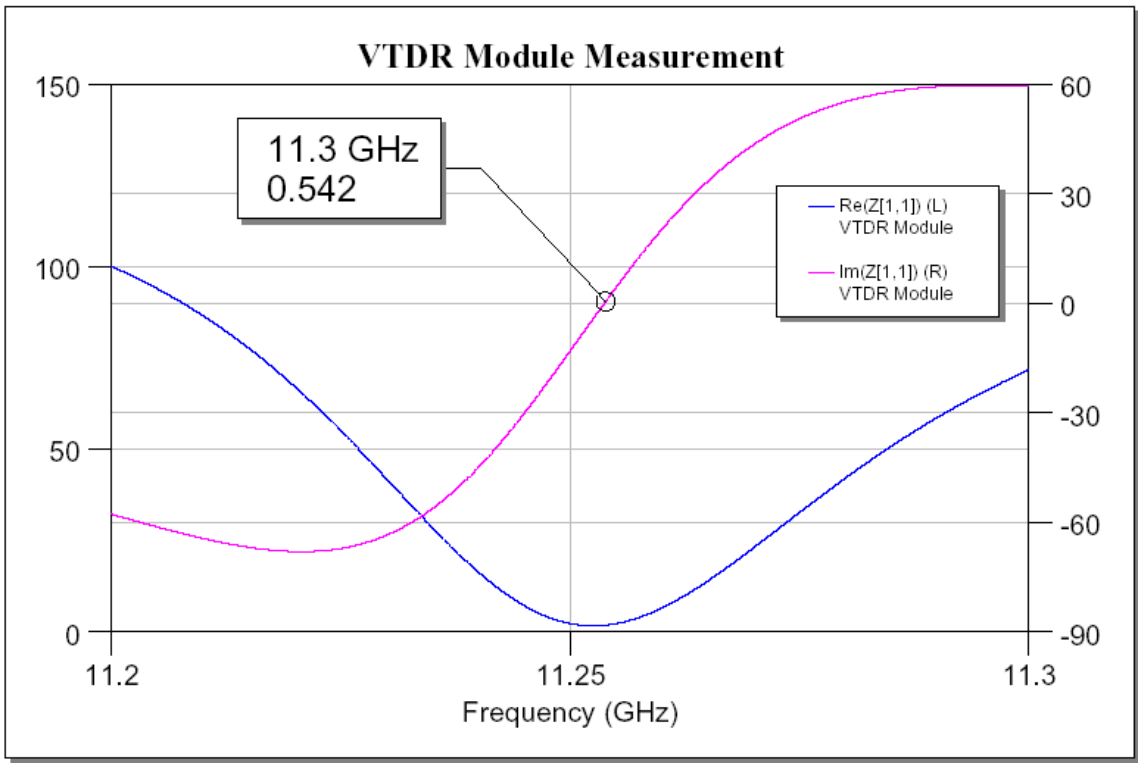


Figure 2-16 DR parameter measurement setup

In this case, we took parameters from Trans-Tech Inc. Figure 2-18 shows the module and simulation result.



(a)

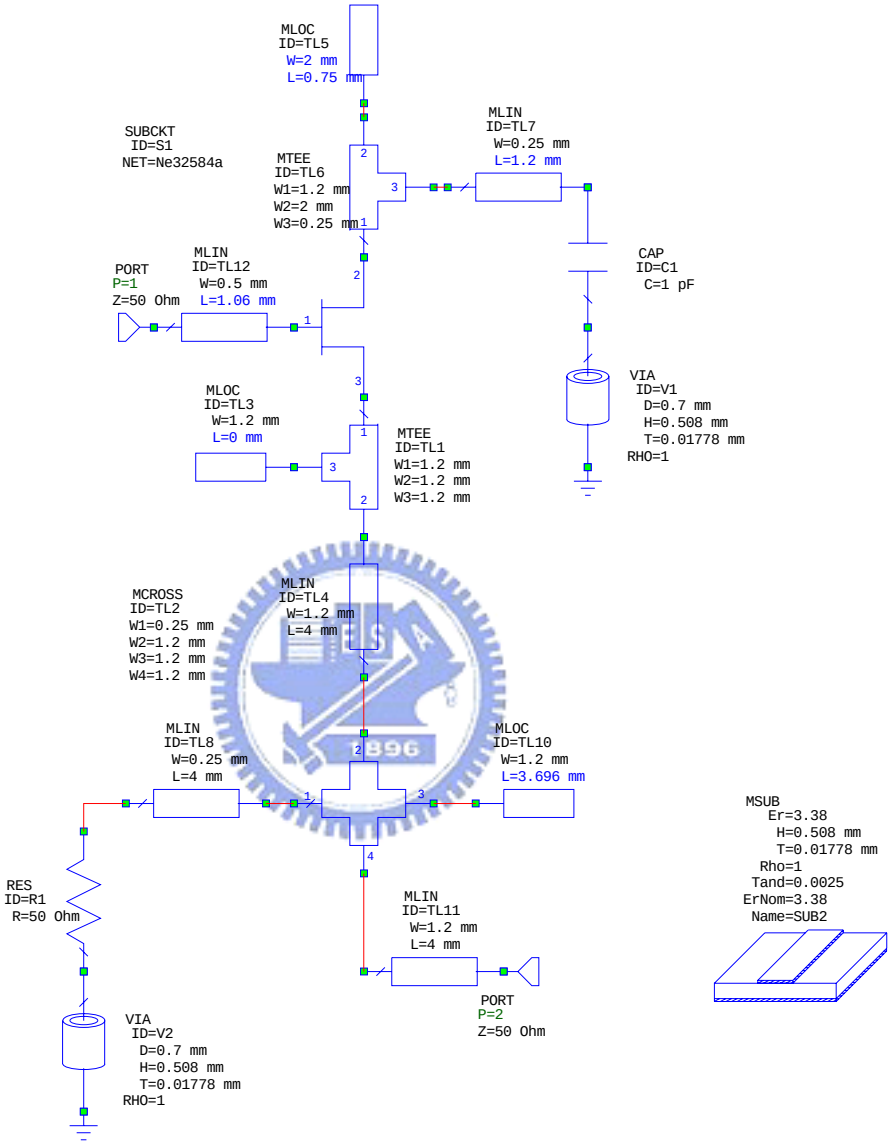


(b)

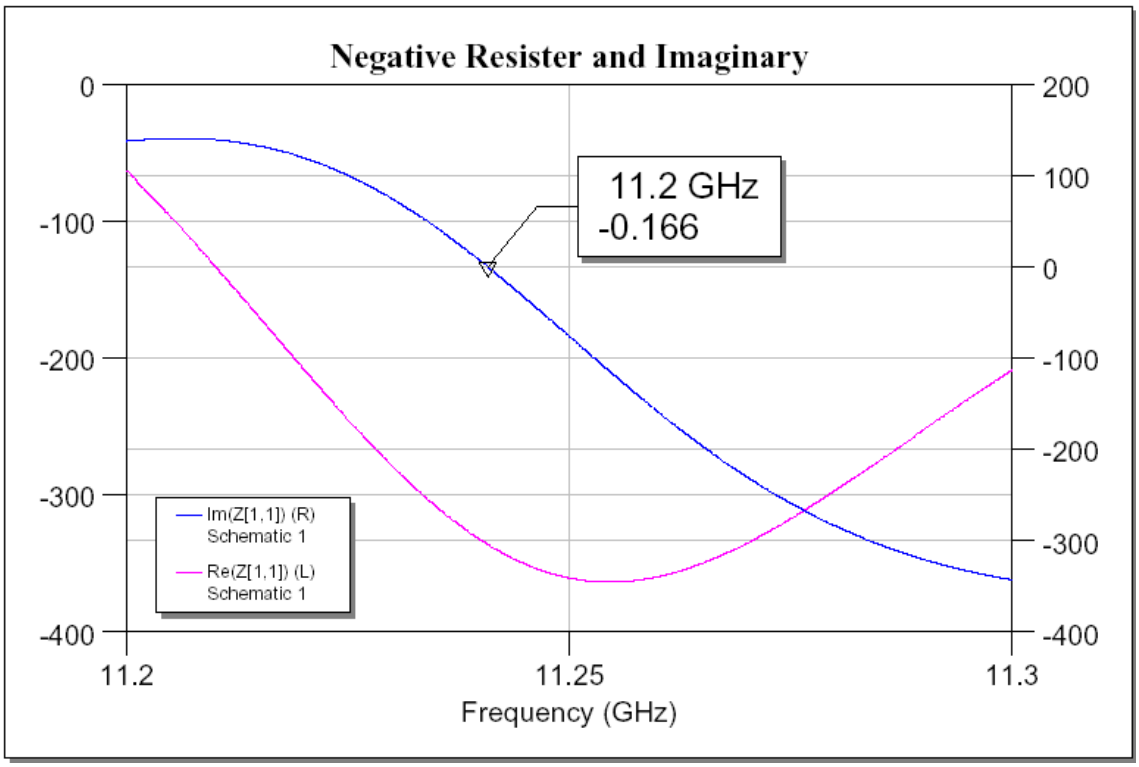
Figure 2-18 DR module for software (a) equivalent circuit (b) simulation result

2-2-2 Negative Resister Generator Simulations

The active device chosen is a NE54586 FET and the small-signal parameters are given for a bias of $V_{ds} = 2V$ at $I_{ds} = 10mA$. In the drain of FET, the matching circuit was optimized at design frequency. Because of the structure is easy tuning, the feedback element chosen is a open-stub . It is connect with gate of FET. The open-stub is optimized so that the real part of the gate is as negative as possible. Figure 2-19 shows the one-port topology and simulation value.


MLOC
ID=TL5
W=2 mm
L=0.75 mm
SUBCKT
ID=S1
NET=Ne32584a
MTEE
ID=TL6
W1=1.2 mm
W2=2 mm
W3=0.25 mm
MLIN
ID=TL7
W=0.25 mm
L=1.2 mm
CAP
ID=C1
C=1 pF
PORT
P=1
Z=50 Ohm
MLIN
ID=TL12
W=0.5 mm
L=1.06 mm
VIA
ID=V1
D=0.7 mm
H=0.508 mm
T=0.01778 mm
RHO=1
MLOC
ID=TL3
W=1.2 mm
L=0 mm
MTEE
ID=TL1
W1=1.2 mm
W2=1.2 mm
W3=1.2 mm
MCROSS
ID=TL2
W1=0.25 mm
W2=1.2 mm
W3=1.2 mm
W4=1.2 mm
MLIN
ID=TL4
W=1.2 mm
L=4 mm
MLIN
ID=TL8
W=0.25 mm
L=4 mm
MLOC
ID=TL10
W=1.2 mm
L=3.696 mm
MSUB
Er=3.38
H=0.508 mm
T=0.01778 mm
Rho=1
Tand=0.0025
ErNom=3.38
Name=SUB2
RES
ID=R1
R=50 Ohm
MLIN
ID=TL11
W=1.2 mm
L=4 mm
PORT
P=2
Z=50 Ohm
VIA
ID=V2
D=0.7 mm
H=0.508 mm
T=0.01778 mm
RHO=1

(a)



(b)

Figure 2-19 The negative resister generator of NE54586 simulation circuit

2-2-3 VTDRO Measurement

The final linear circuit is provided in figure 2-20. We can adjustment of the electrical length (θ) to compensate for the imaginary part of $Z_g(\omega)$ by the opposite value . The linear simulation will provide a good initial circuit layout before fine tuning . Figure 2-22 presents the layout of the DRO that was tested. Figure 2-23 and figure 2-24 presents the measured output power and phase noise performance that was achieved. Figure 2-25 presents the measured frequency tune range.

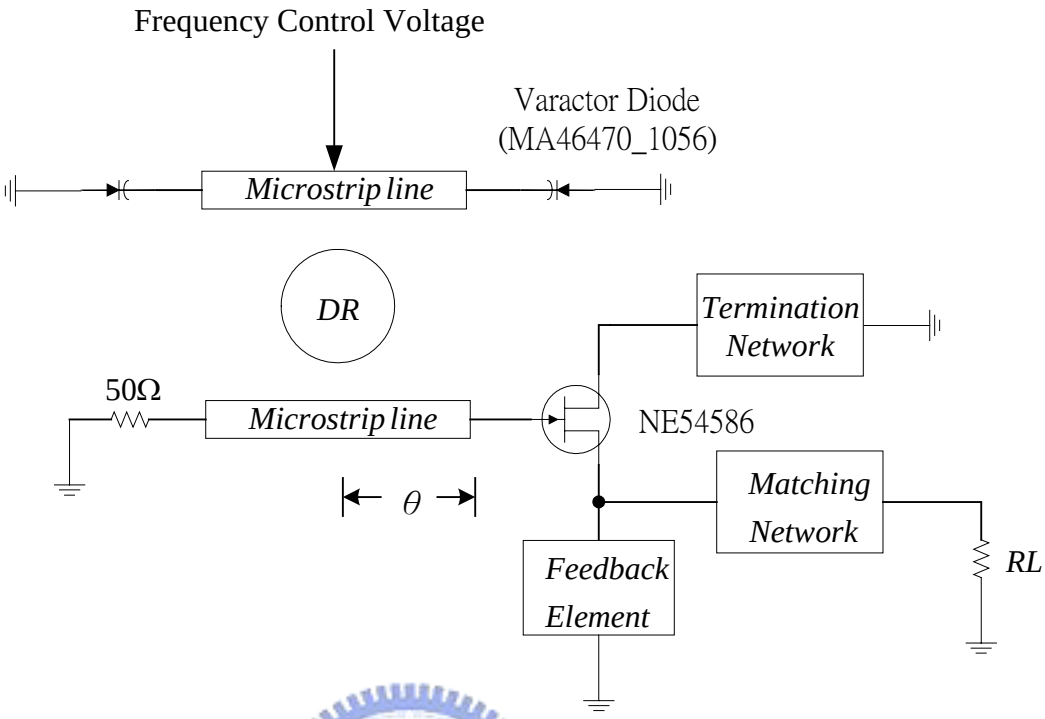
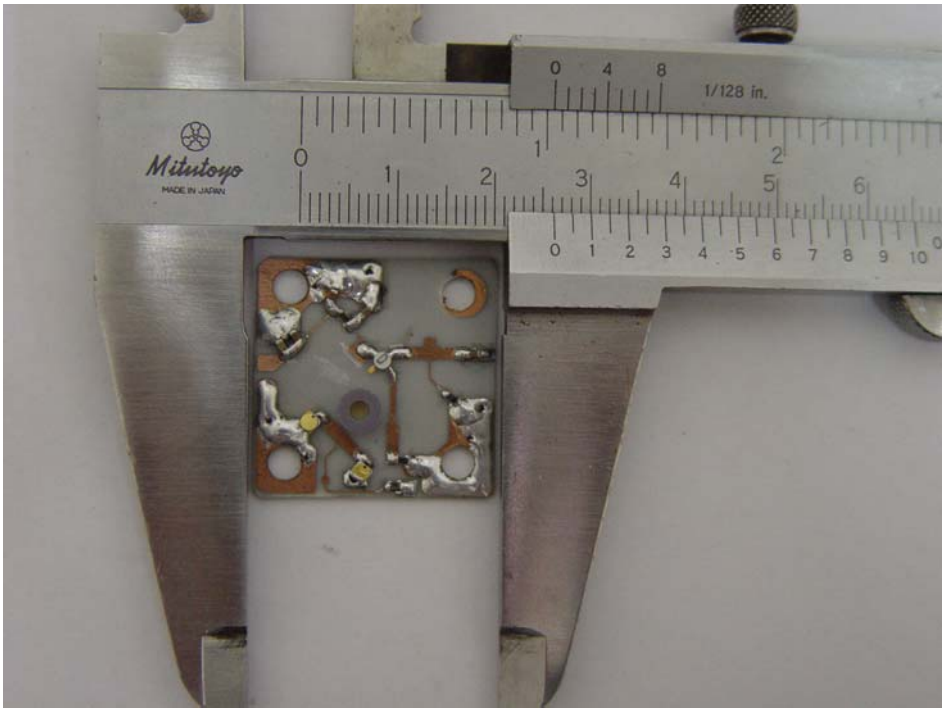
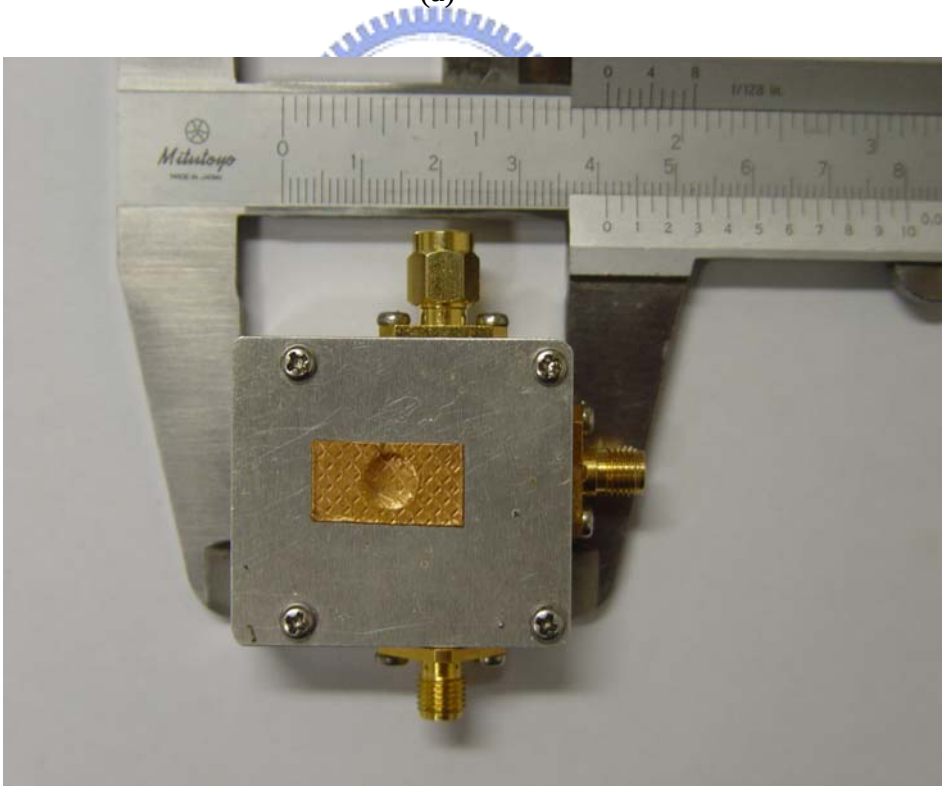


Figure 2-20 VTDRO block diagram

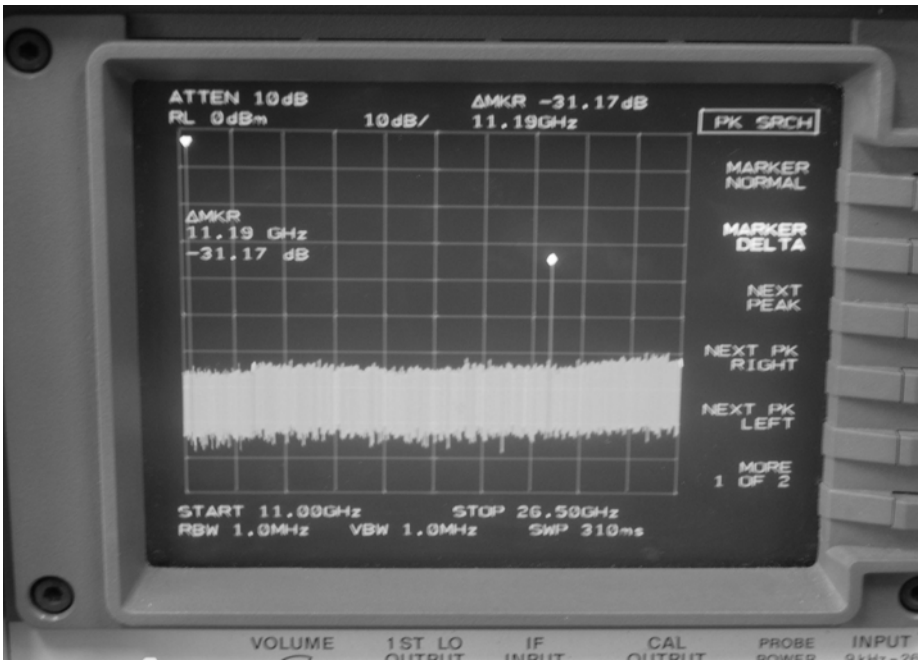


(a)



(b)

Figure 2-22 Layout and module of the VTDRO (a) layout (b) VTDRO module



(a)

(b)

Figure 2-23 VTDRO Output measure (a) Output power spectrum (b) Output power flatness.

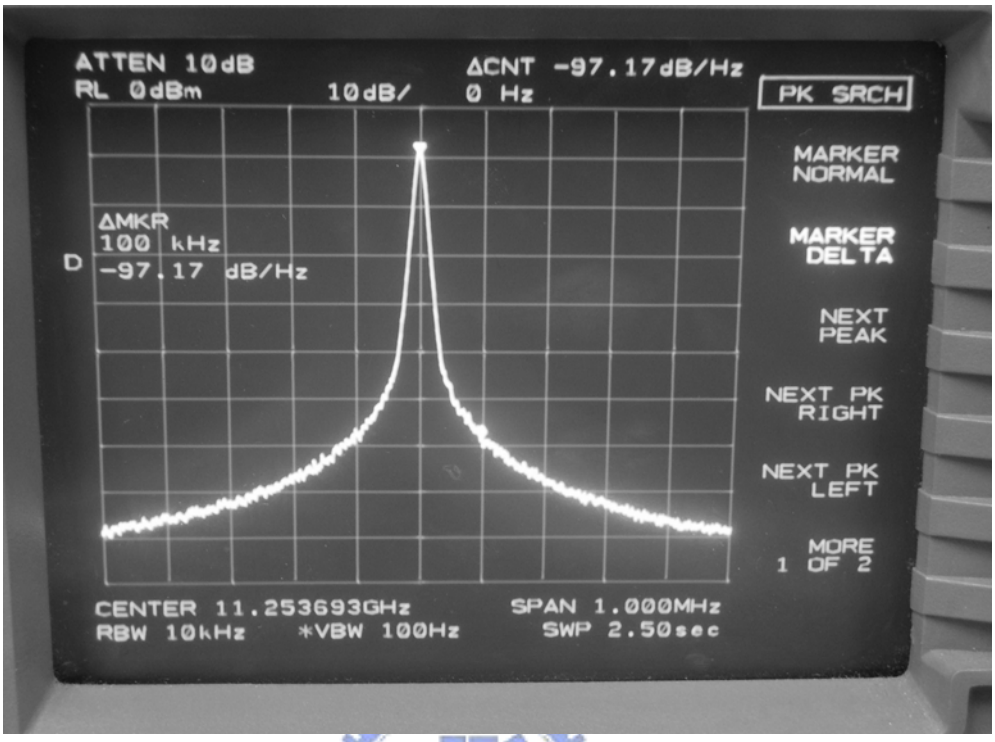


Figure 2-24 VTDRO phase noise @ 100 KHz

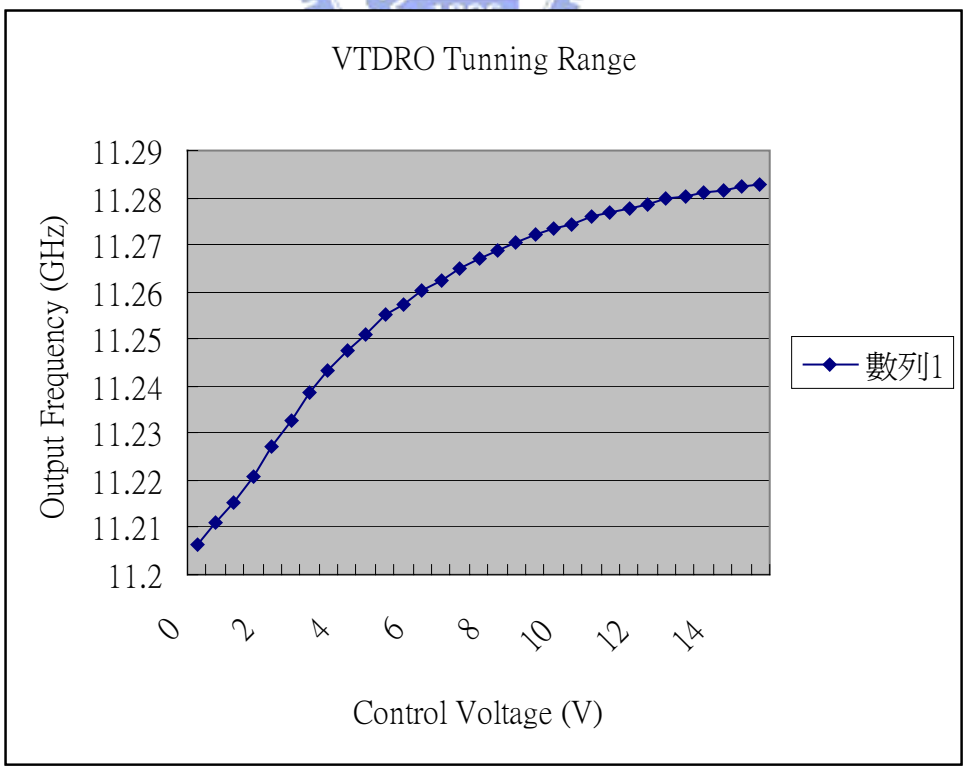


Figure 2-25 VTDRO frequency tune range

2-3 Microwave Amplifier and Direction Coupler Design

The amplifier and direction coupler provide the amplitude gain and tape amplitude from main signal path. They can be performed using techniques given by McGraw-Hill[1]. In this case, the amplifier device is NBB-300. It is broadband InGaP/GaAs MMIC amplifier and provides 8dB gain from 11GHz to 12 GHz. We illustrate a microstrip directional coupler that involves two coupled microstrip lines. The design frequency is 11.25 GHz and coupling of -13 dB.

2-4 PLL Controller Design

The PLL controller schematic is shown as figure 2-35. The controller uses a serial interface from a computer to load data to the PLL chip. PLL chip of LMX1600L frequency operates up to 2.5GHz. The HMC363S8G is a low noise divide-by-8 static divider. This device operates from dc to 12GHz input frequency with a single +5.0V DC supply.

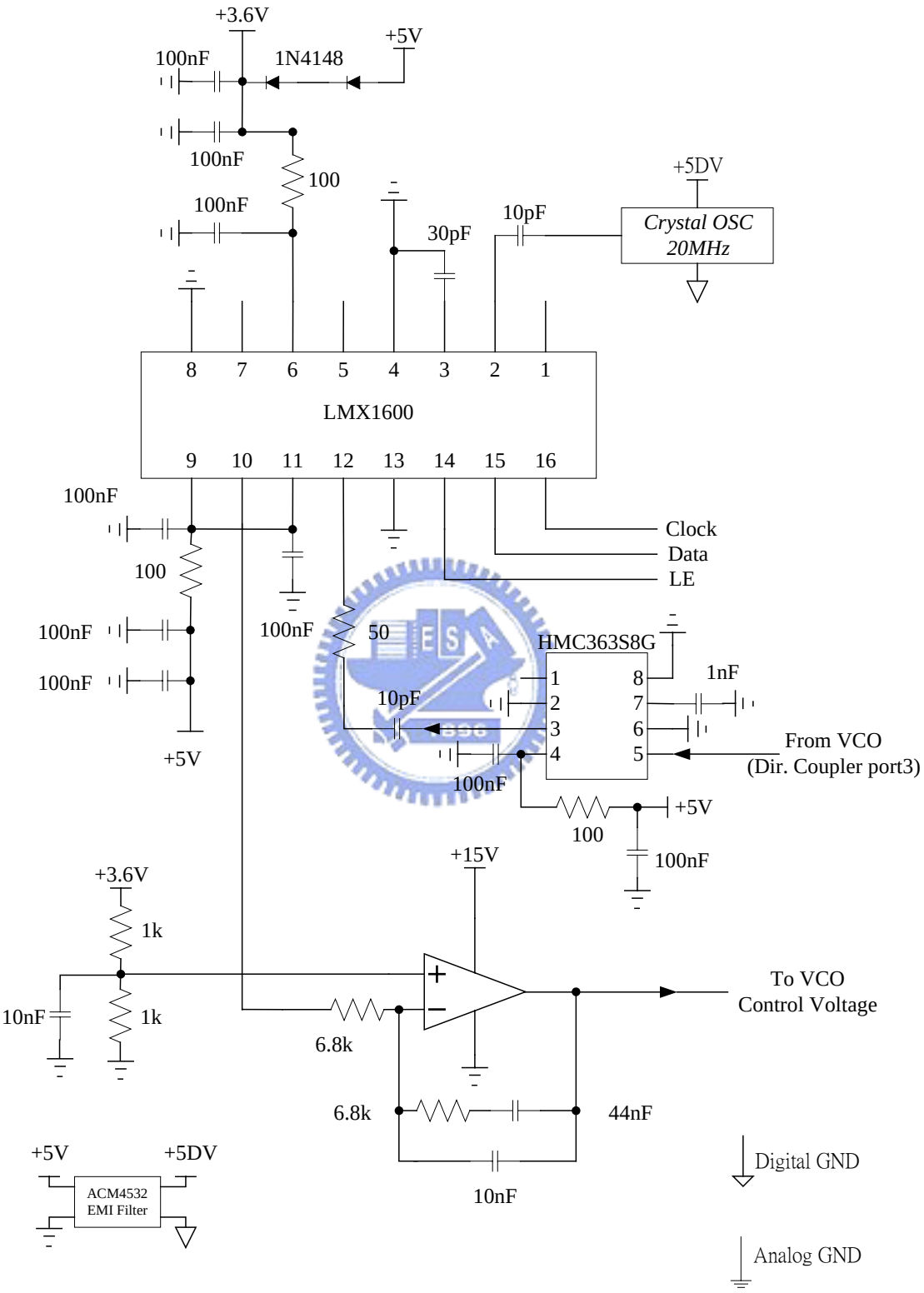


Figure 2-35 PLL controller schematic

The loop filter integrates the pulsed output from the phase detector to produce a smoothed "DC" VCO control voltage. The loop performance can be set by varying the component values in the loop filter.

The simplest is an RC low pass section (see figure 2-36 (a)). This will always include a second resistor in series with the capacitor. A further section of RC filtering can be added to produce a third order loop with improved sideband and noise performance(see figure 2-36 (b)). However it is more difficult to analyse higher order loops for stability and other parameters. If a simple RC filter is used, the VCO control voltage swing is limited to 0-5V in systems with a digital phase detector. For best phase noise performance it is necessary to use the full available control range of the varactor diode. To do this, a second OP amplifier can be configured as a DC amplifier to bring the output voltage to a higher figure (see figure 2-36 (c)). All components in the loop filter should be designed for low noise (eg. low noise OP amplifier and metal film resistors). The calculation of loop filter is shown in Appendix A.

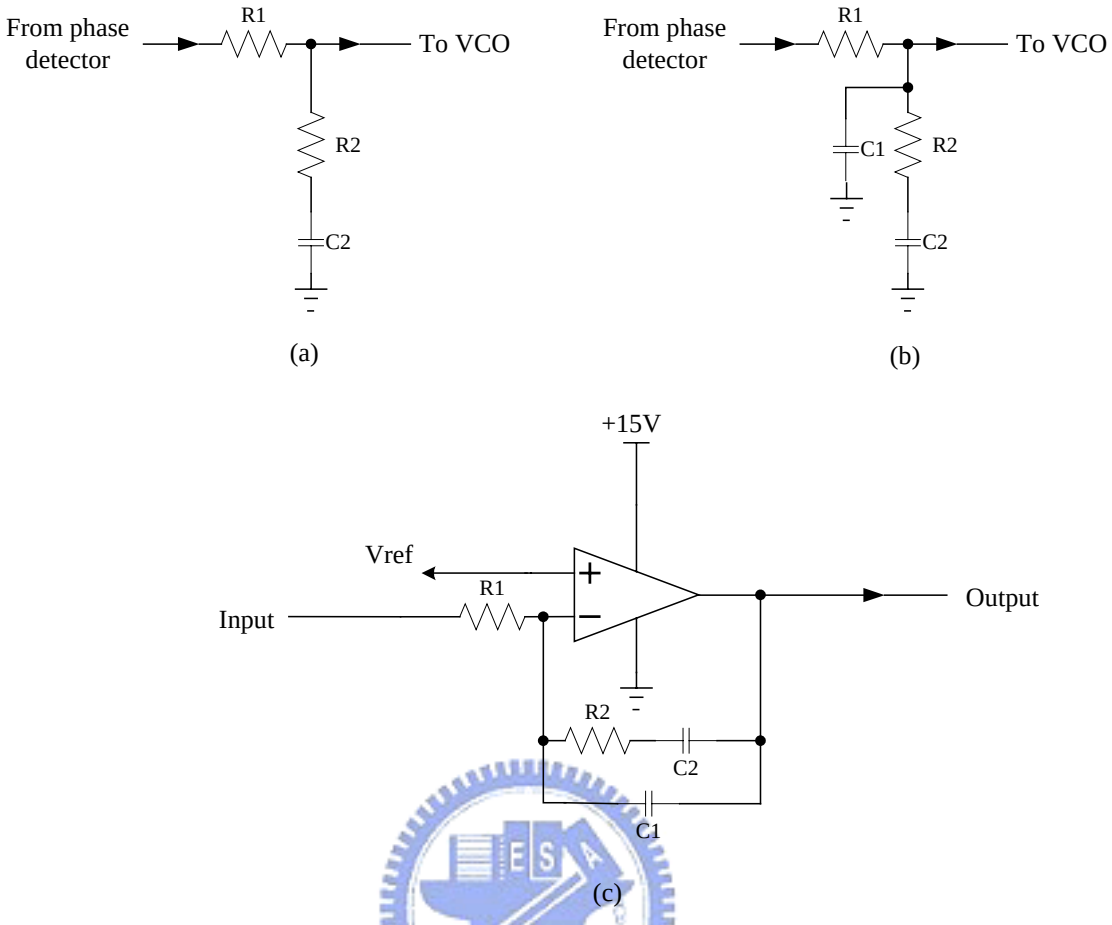


Figure 2-36 Loop filter type (a) basic second order filter (b) passive third order filter (c) active third order filter

2-5 KU-Band frequency control loop measurement

Figure 2-37 shows the KU-Band frequency control loop measurement setup diagram. This is the software that can be used to program a PLL via the parallel port of a computer. The software introduction is shown in Appendix B.

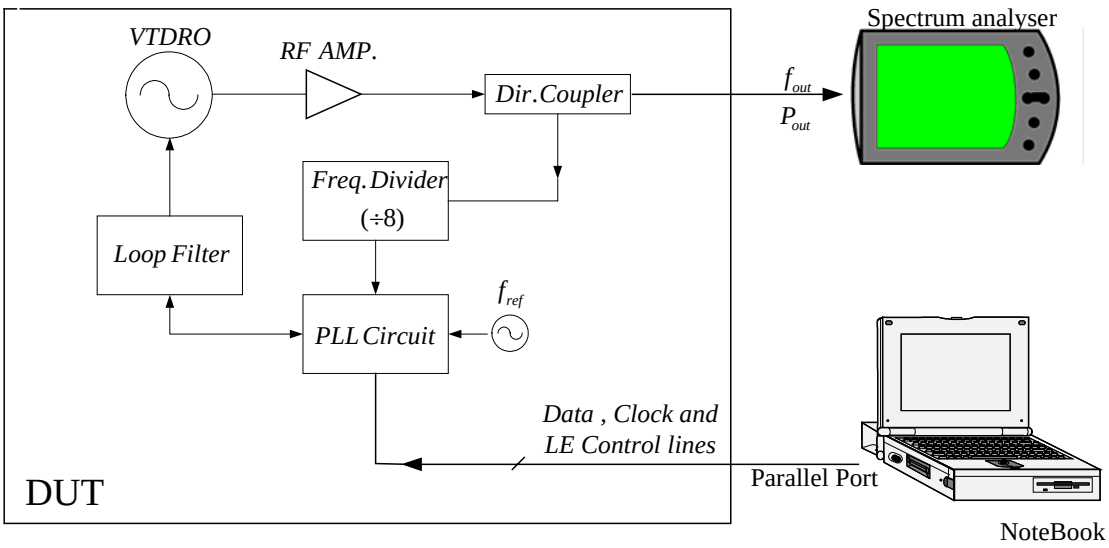


Figure 2-37 KU-Band frequency control loop measurement setup diagram

Figure 2-38 is the lock-in time measurement of frequency control loop. Figure2-39 shows the spurious of the reference frequency leakage. The spur due to reference leakage is about 66.8 dBc. Figure 2-40 is the phase noise measurement of Ku-band frequency control loop. The value of phase noise is 97.17 dBc/Hz at 100KHz offset.

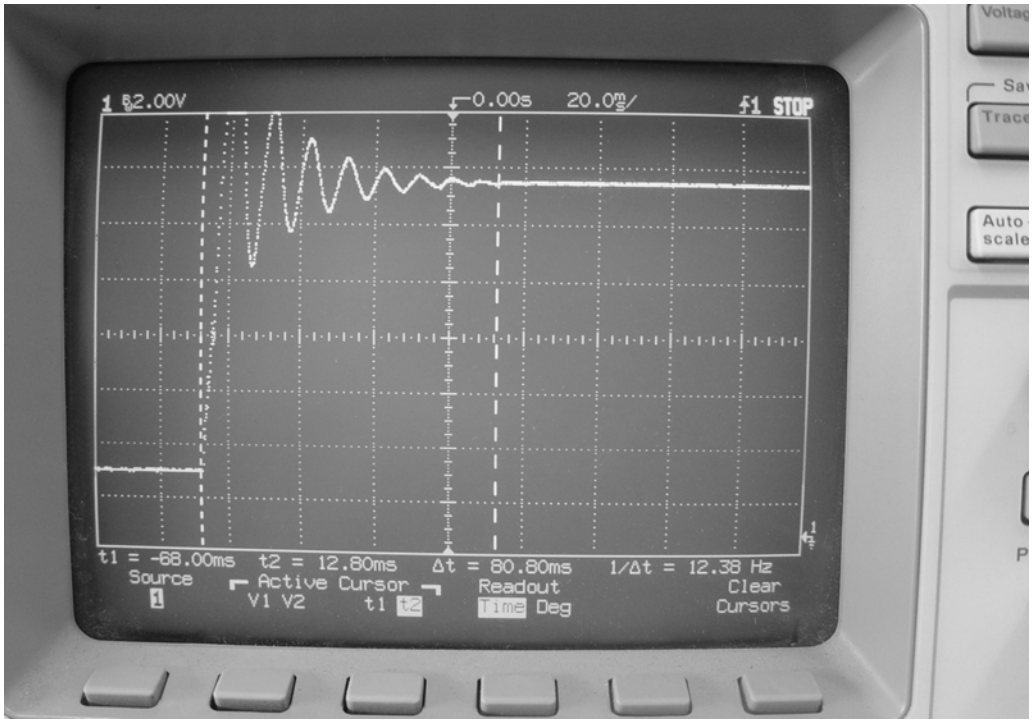


Figure 2-38 Lock-in time measurement of frequency control loop (11.225GHz jump to 11.275GHz)

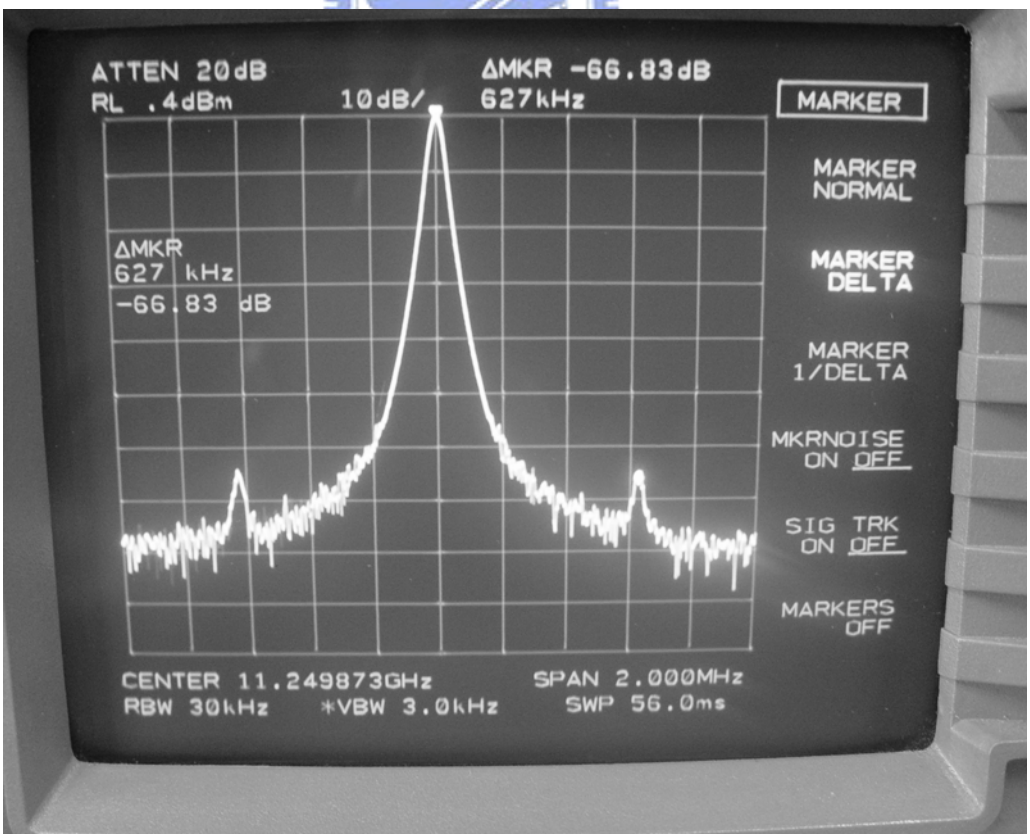


Figure 2-39 Spurious of the reference frequency leakage

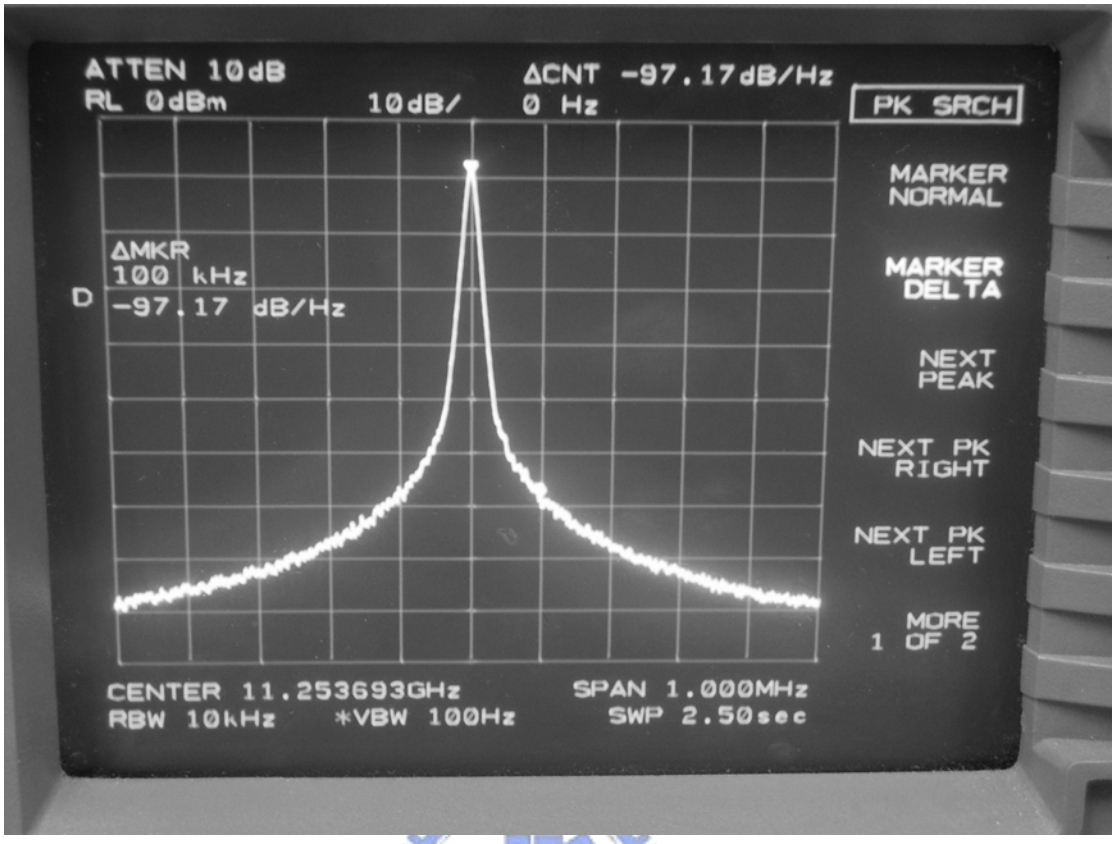


Figure 2-40 phase noise measurement of Ku-band frequency control loop at 100KHz offset

Chapter 3

RF Power Control Loop

In this chapter, we will discussed theory and design of the RF power automatic gain control (AGC) loop. The block diagram is shown as figure 3-1.

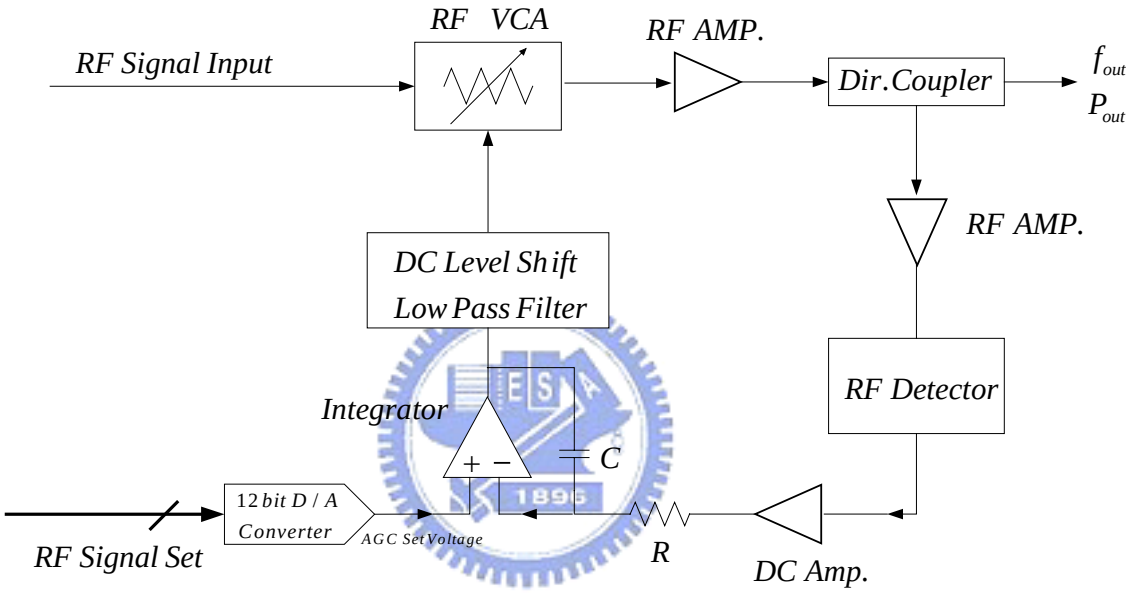


Figure 3-1 RF Power Control Loop block diagram

The function of RF control loop discussed as follow:

1、The input signal passes through the VCA to produce the output level to be stabilized. The D/A converter was set by the computer and produces a reference DC voltage (AGC Set voltage).

2、The directional coupler tap the output power and feed it to RF detector and produces

a DC voltage proportional to the RF output power.

3、The DC amplifier provides a DC gain and produce detector's output voltage.

4、The detector's output voltage is compared against a AGC Set voltage to produce an error signal, which is then integrated to produce a control positive voltage.

5、The DC level shift circuit transforms the control positive voltage into negative voltage for the VCA and adjusts RF output power.

3-1 Outline of Power Control Loop

3-1-1 Outline of AGC [5][6][19]

Many attempts have been made to fully describe an AGC system in terms of control system theory, from pseudo linear approximations to multivariable systems. Each model has its advantages and disadvantages, first order models are easy to analyze and understand but sometimes the final results show a high degree of inaccuracy when they are compared with practical results. On the other hand, non-linear and multivariable systems show a relative high degree of accuracy but the

theory and physical implementation of the system can become really tedious.

The basic block of automatic gain control loop show in figure 3-2. The input signal is amplified by a variable gain block (VGB) whose gain is controlled by a control

voltage V_c. A cascade amplifier to generate and adequate level of V_o can amplify the output from the VGB. The power detector senses the output level, any undesired component is filtered out and the remaining signal is compared with a reference signal VR. The result of the comparison is used to generate the V_c and adjust the gain of the VGB.

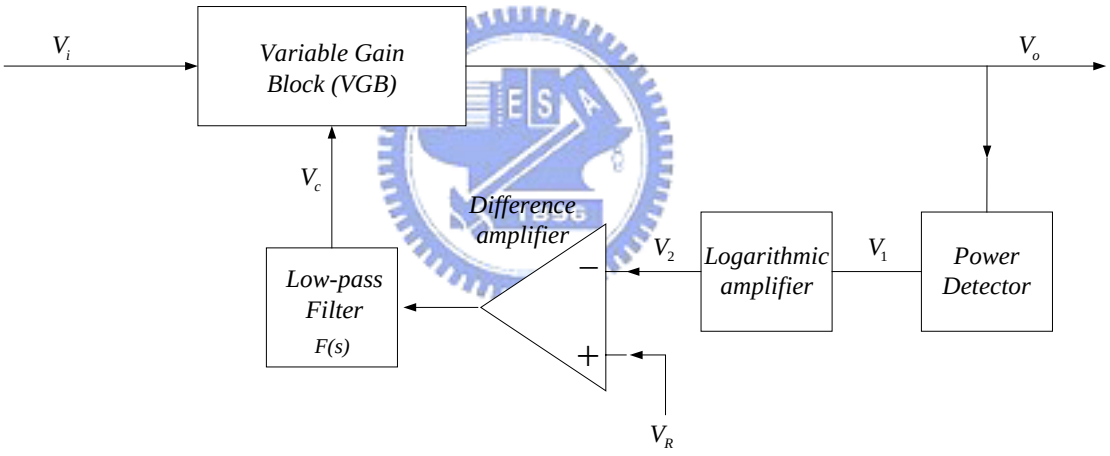


Figure 3-2 basic block of automatic gain control loop

From figure 3-2, the AGC block diagram is essentially a negative feedback system and the system can be described in terms of its transfer function.

The idealization of AGC transfers function show in figure 3-3. For low input level the AGC is disabled and the output is a linear function of the input, when the output reaches a threshold value, V_{i1}, the AGC becomes operative and maintains a constant output level until it reaches a second threshold value (V_{i2}). At point of V_{i2}, the AGC becomes inoperative again; this is usually done in order to prevent stability problems at high levels of gain.

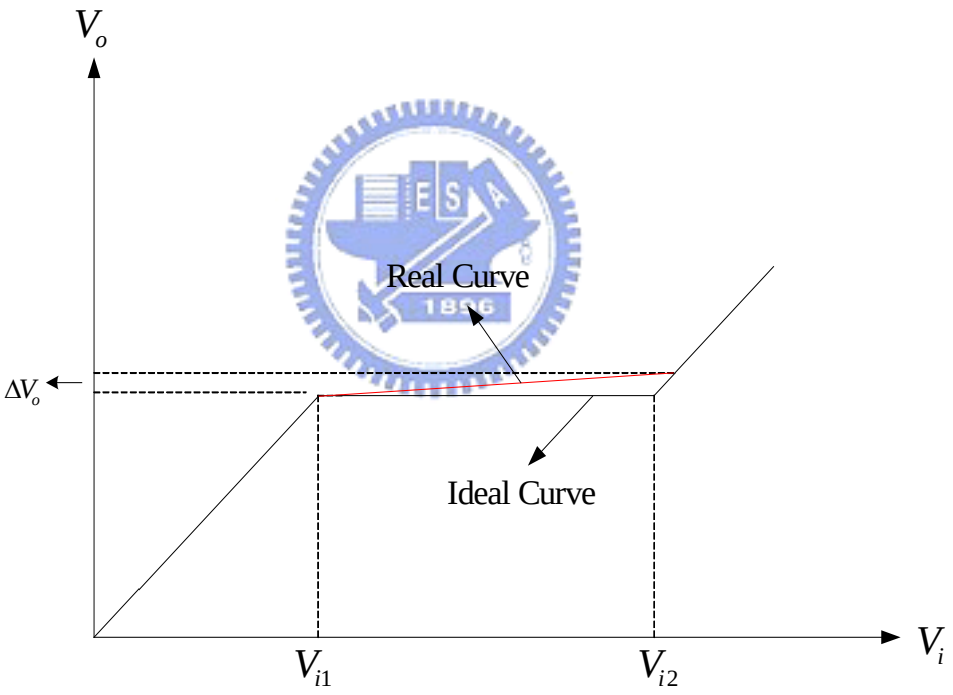


Figure 3-3 the idealization of transfer function for an AGC system

Unfortunately, the AGC system is considered a nonlinear systems and it is very hard to find solutions for the nonlinear analysis.

However, there is a linear model that describes the AGC loop function with a good degree of accuracy and are relatively easy to implement when the small signal transfer equations of the main blocks are known. The block diagram for this model is show in figure 3-2. The variable gain block has the following transfer function and it expression is by

$$P = K_1 e^{+aV_c} \tag{3-1}$$

and

$$V_o = V_i K_1 e^{+aV_c} \tag{3-2}$$

Where

V_i and V_O are the input and output level.

K_1 is a constant and *a* is a constant factor of the VGB.

The logarithmic amplifier gain can be defined as follow

$$V_2 = \ln V_1 = \ln K_2 V_o \tag{3-3}$$

Where

K_2 represents the gain of the envelope detector.

In order to simplify, we assume that the output of the envelope detector is always positive. The control voltage becomes:

$$V_c = F(s)(V_R - V_2) = F(s)(V_R - \ln K_2 V_o) \tag{3-4}$$

where

F(s) represents the filter transfer function.

By expending (3-2), the V_c can be written as:

$$aV_c = \ln V_o - \ln K_1 V_i \tag{3-5}$$

From (3-4) and (3-5), we get :

$$\ln V_o[1 + aF(s)] = \ln V_i + aF(s)V_R + \ln K_1 - aF(s)V_R \ln K_2 \tag{3-6}$$

Since we are only interested in the output-input relationship, let K_1 and K_2 be equal to one. Thus, the above equation becomes:

$$\ln V_o[1+aF(s)] = \ln V_i + aF(s)V_R \tag{3-7}$$

If V_o and V_i are expressed in decibels, we can use the following equivalence

$$\ln V_o = 2.3\log V_o \tag{3-8}$$

$$\ln V_o = \frac{2.3}{20}V_{odB} = 0.115V_{odB} \tag{3-9}$$

Finally, the equation (3-7) that relates input and output can be rewritten as

$$V_{odB} = \frac{V_{idB}}{1+aF(s)} + \frac{8.7aF(s)V_R}{1+aF(s)} \tag{3-10}$$

The equation (3-10) shows a linear relationship as long as input and output quantities are expressed in decibels and it is easy to see that the function of the system is determined by the filter *F(s)* and the *a* factor of the VGB. *F(s)* is usually a low pass filter, since the bandwidth of the loop must be limited to avoid stability problems and to ensure that the AGC does not respond to any amplitude modulation that could be present in the input signal.

In any control system, an important parameter is the steady-state error that is defined as :

$$e_{ss} = \lim_{t\to\infty} e(t) = \lim_{s\to 0} sE(s) \qquad (3\text{-}11)$$

where E(s) is the error signal in the feedback path.

Applying the definition given above to the AGC loop we find that the position error constant is given by:

$$e_{ss} = \frac{1}{1 + aF(0)} \qquad (3\text{-}12)$$

where

$F(0)$ is the DC gain of the *F(s)* block.

a is the constant factor of the variable gain block .

Thus, in order to maintain the steady state error as small as possible the DC gain of the *F(s)* block must be as large as possible .The *F(s)* block that can be used in the loop is a first order low pass filter whose transfer function is defined as follows:

$$F(s) = \frac{K}{\frac{s}{B} + 1} \qquad (3\text{-}13)$$

where

K is the DC gain of the filter.

B is the bandwidth.

Using this expression in the equation of the steady state error we find that:

$$e_{ss} = \frac{1}{1+aK} \tag{3-14}$$

The total DC output of the AGC loop is given by:

$$V_{oDC} = \frac{V_{IDC}}{1+aK} + \frac{8.7aKV_R}{1+aK} \tag{3-15}$$

It can be seen that if the gain loop K is much greater than 1, the output is almost equal to $8.7V_R$ and the steady state change in the input is greatly reduced. AGC loop that include a reference voltage inside the control loop are referred as delayed AGC.

Since we are interested in the change in the output voltage due to a change in the input voltage we can take the derivative of V_o with respect to V_i. From (3-1) and (3-2), the output voltage becomes:

$$V_o = PV_i \tag{3-16}$$

therefore

$$\frac{dV_o}{dV_i} = \frac{d}{dV_i}(PV_i) = P + V_i \frac{dP}{dV_i} \tag{3-17}$$

From $\frac{dP}{dV_i}$, we can be further developed applying the chain rule and using the equation for the control voltage, thus:

$$\frac{dP}{dV_i} = \frac{dP}{dV_c}\frac{dV_c}{dV_i} = \frac{dP}{dV_c}\frac{dV_c}{dV_o}\frac{dV_o}{dV_i} = \frac{dP}{dV_c}\frac{dV_o}{dV_i}(\frac{-F}{V_o}) \tag{3-18}$$

Therefore, the equation (3-17) can be rewritten as:

$$\frac{dV_o}{dV_i}[1 + \frac{F}{V_o}V_i \frac{dP}{dV_c}] = P \tag{3-19}$$

Alternatively

$$\frac{\frac{dV_o}{V_o}}{\frac{dV_i}{V_i}} = \frac{1}{[1 + \frac{F}{P}\frac{dP}{dV_c}]} \tag{3-20}$$

From (3-20), It is clear that the loop gain is a function of the input signal. That translates into a relative degree of non-linearity and complicates the analysis of the transient response of the system.

However, it is possible to numerically evaluate the characteristic parameters of the loop if the $P(V_c)$ function is know and a set of initial conditions is taken as a starting point.

3-1-2 Outline of VCA

In the microwave circuit, attenuators are useful in reducing the power level of RF signals by a specific amount. The basic structure is shown as figure 3-4.

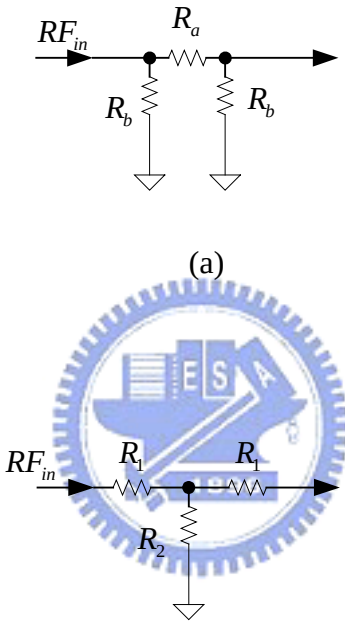


Figure 3-4 Basic structure of attenuator (a) π type (b) T type

In the application, the fixed attenuators and variable attenuators are two general configurations. The fixed attenuators allow one or more discrete levels of attenuation. The variable attenuators allow a specific value of attenuation to be selected from an analog control voltage.

The PIN diode and the FET are commonly used in variable attenuators. In this case, we discuss the FET voltage variable attenuator of the T type. Figure 3-5 shows the T type resistance attenuator and equivalent circuit of FET.

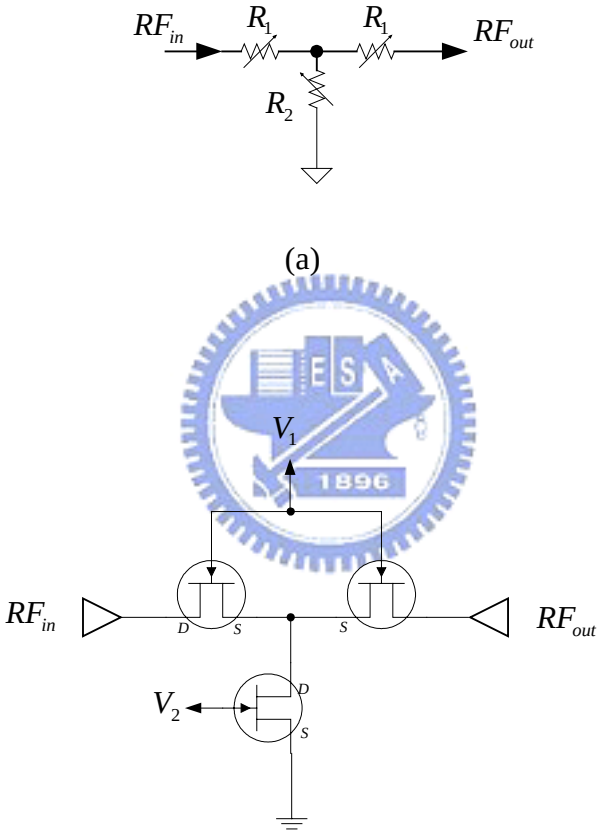


Figure 3-5 The T type resistance attenuator (a) resistance attenuator (b) equivalent circuit of FET

In generally, the attenuator of FET requires two bias voltages, one applied to the series FETs (V_1) and one applied to the shunt FETs (V_2). As voltages V_1 and V_2 are

varied between V_{c1} and V_{c2} the FETs “on” resistance changes. At V_{c1} control, the FET is turned fully “on” resulting in a low resistance state. At V_{c2} control, the FET is in a fully “pinchedoff” state resulting in a high resistance state. When the control voltages are between V_{c1} and V_{c2}, the FETs are neither fully “on” nor fully “off” but are in a variable resistance state that is a function of control voltage.

The control voltage vs. attenuation curve is shown in Figure 3-6 and is typical for the AT006N3-01 of Alpha Industries, Inc. We can find the curves are not a linear function. This occurs because the FET’s resistance is a non-linear relationship with respect to control voltage and increases very quickly as the control voltage approaches “pinch-off”.

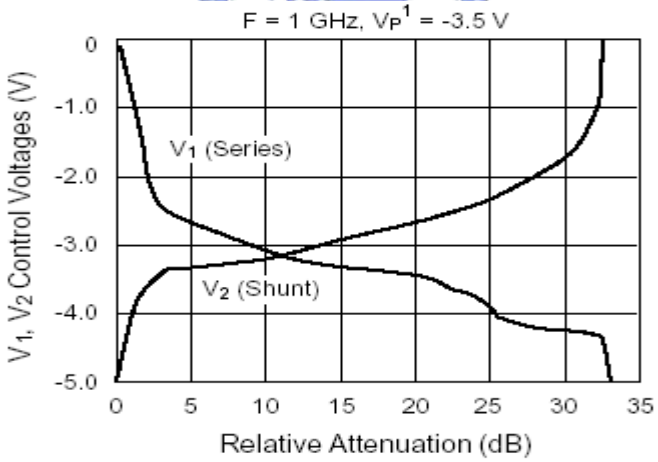


Figure 3-6 Typical for the AT006N3-01 of Alpha Industries, Inc

3-2 Power Control Loop Design

3-2-1 Ku-band Power Detector Design

Figure 3-7 shows the basic construction of the RF detector[1]. The matching network is necessary so the maximum power can reach the diode and the conversion from RF to DC can take place efficiently.

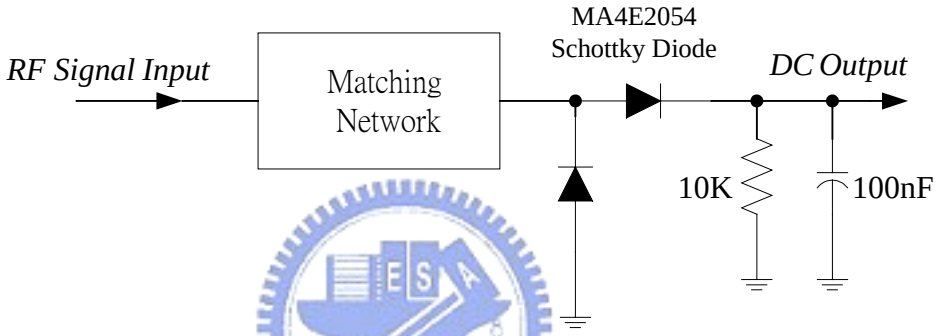
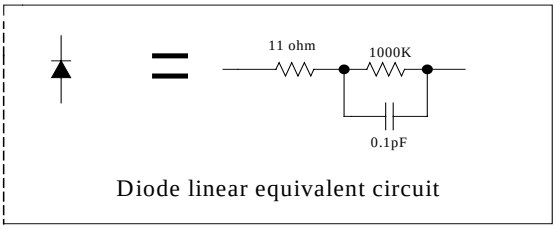


Figure 3-7 Basic construction of the RF detector

The RF power from amplifier and feeds it to a Schottky diode detector. It produces a DC voltage proportional to the output, which is then fed back to the AGC controller. The linear equivalent circuit can provide insight into the performance of the Schottky diode (see figure 3-8). Lp and Cp are package parasitics. A three eelement equivalent circuit can represent the diode chip itself, including Rs (parasitic series resistance), Cj (parasitic junction capacitance) and Rj (the junction resistance). Figure 3-10 shows the RF imputer power versus output dc voltage.



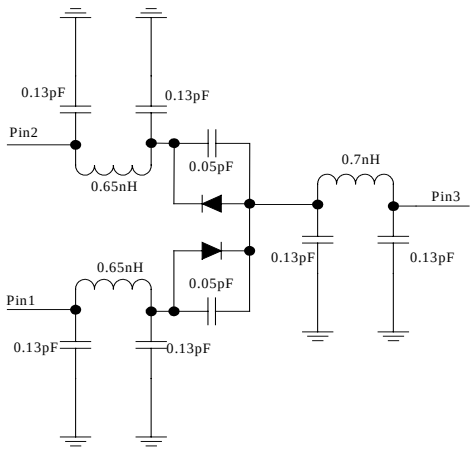


Figure 3-8 equivalent circuit of Schottky diode

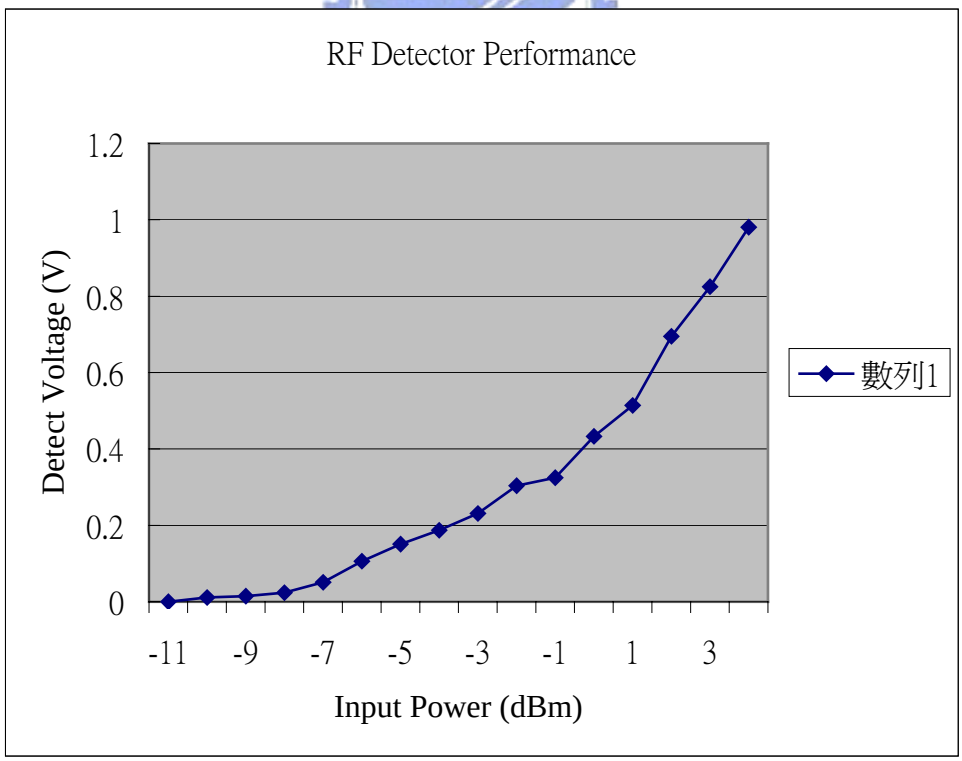
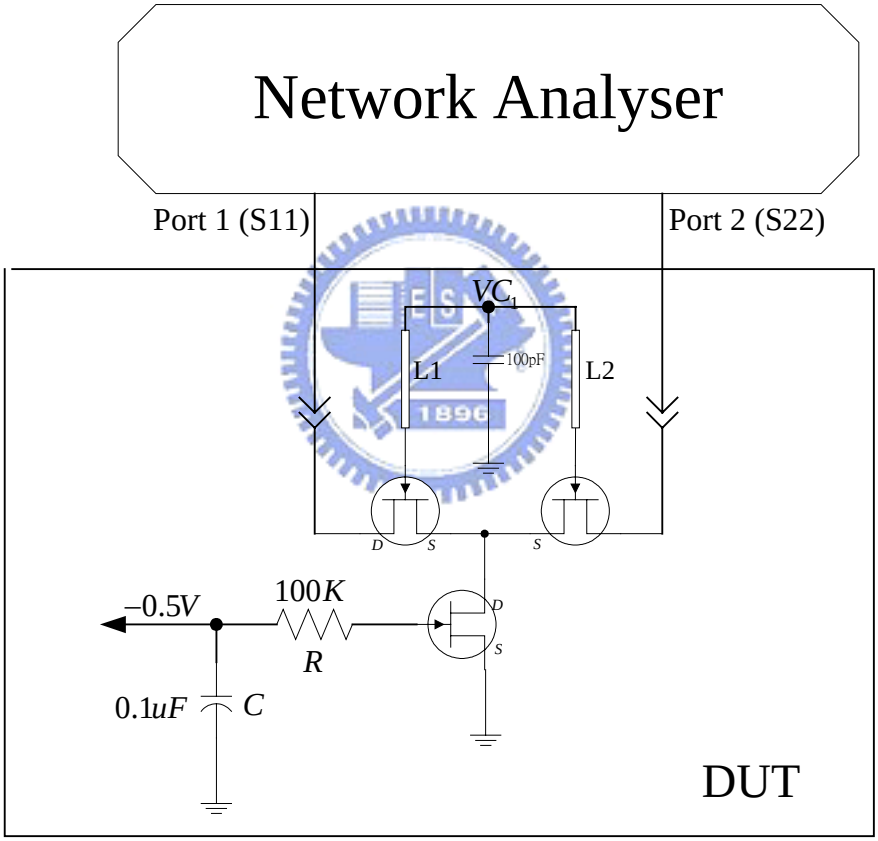


Figure 3-10 RF imputer power versus output dc voltage

3-2-2 Ku-band VCA Design

The GaAs MESFETs at zero drain bias have been used as variable resistors to construct a new module of T-type attenuator. The S parameter of new module must reconstruction. In this case, the NE32584c can provided R_{ds} by the V_{gs}. The test setup is shown figure 3-11.



L1 , L2 =>1/4 λ Transmission Line @11.25GHz

Figure 3-11 T-type attenuator module of NE32584c

In second step, input and output the simulation software designed match circuits. The final circuit and simulation result are shown as figure 3-12 and figure 3-13. It can provide 18 dB dynamic range by the VC_1 and 3 dB insertion loss. The network analyzer and spectrum analyzer measured the characteristic of VCA. The measurement data are shown as figure 3-14 and figure 3-15.

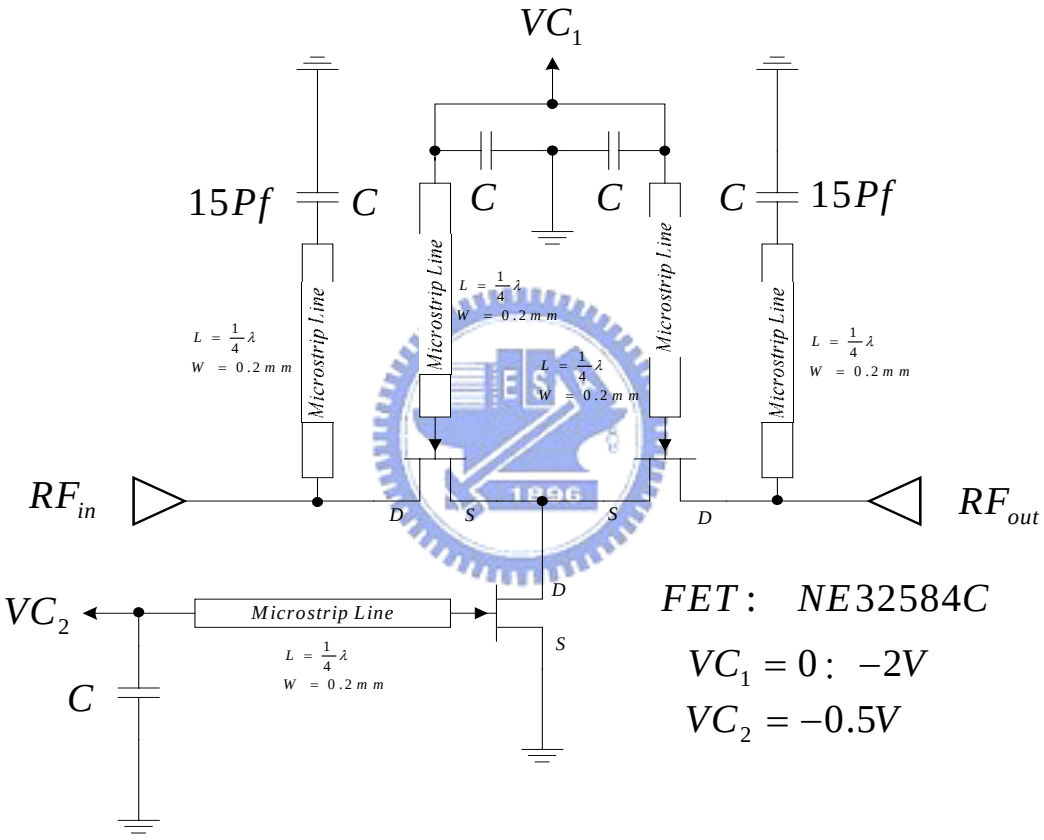
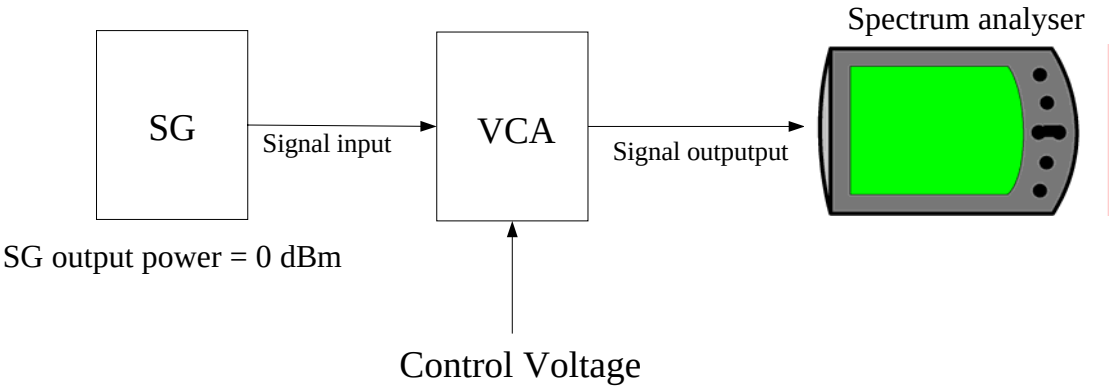
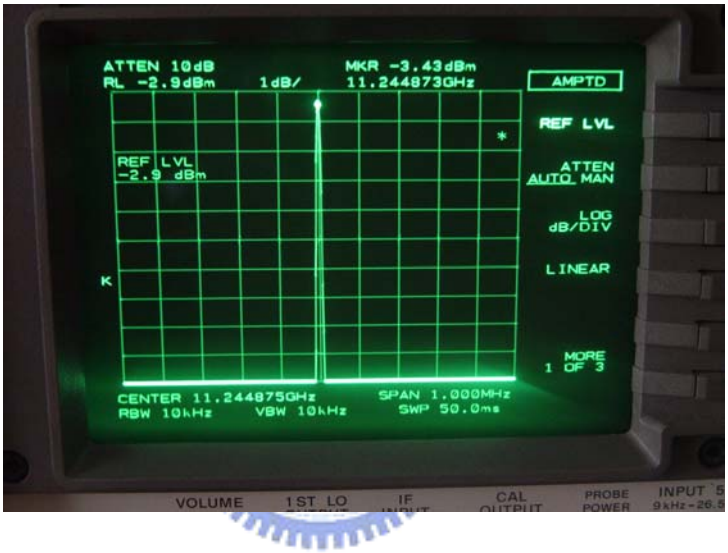


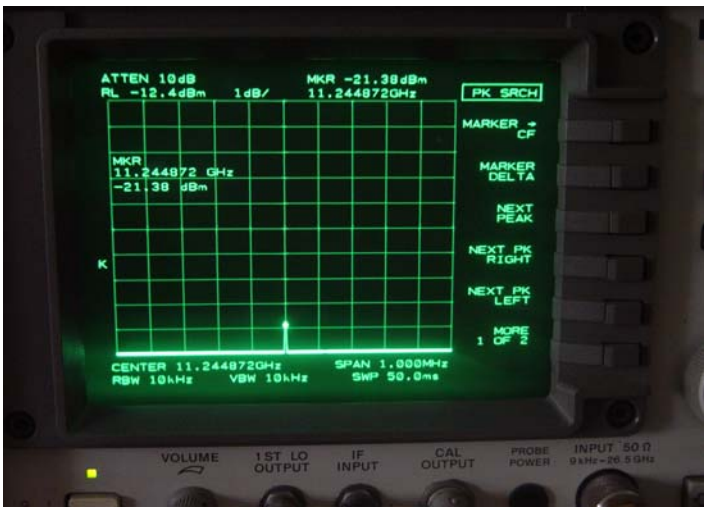
Figure 3-12 VCA final circuit



(a)



(b)



(c)

Figure 3-14 VCA measurement (a) measurement setup (b)insertion loss measure(c) attenuation performance at 0V control voltage

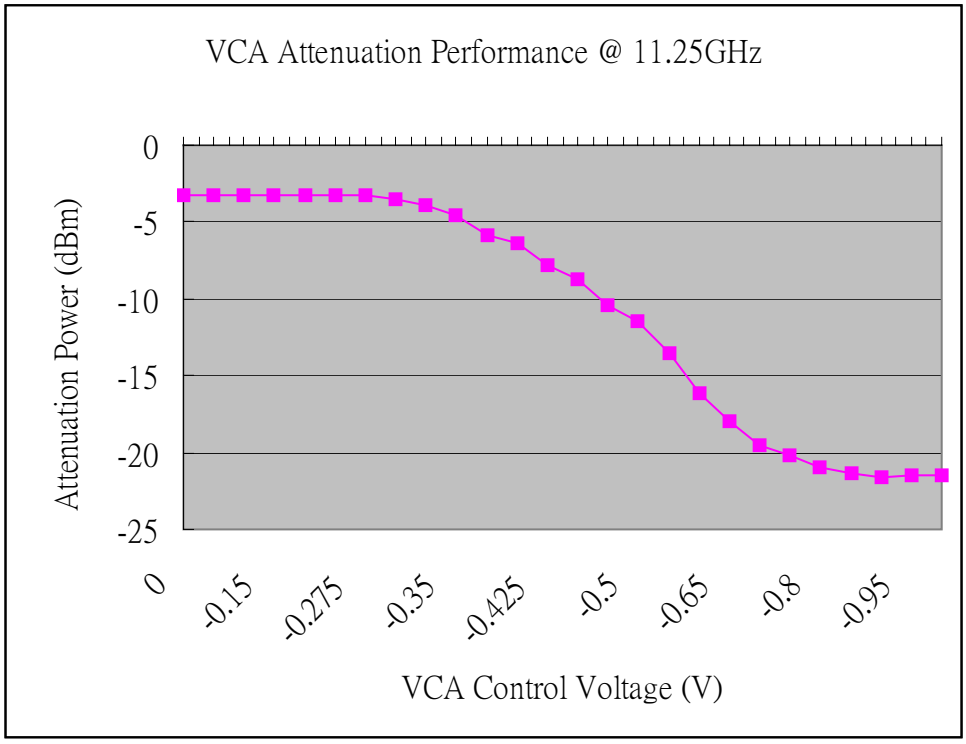
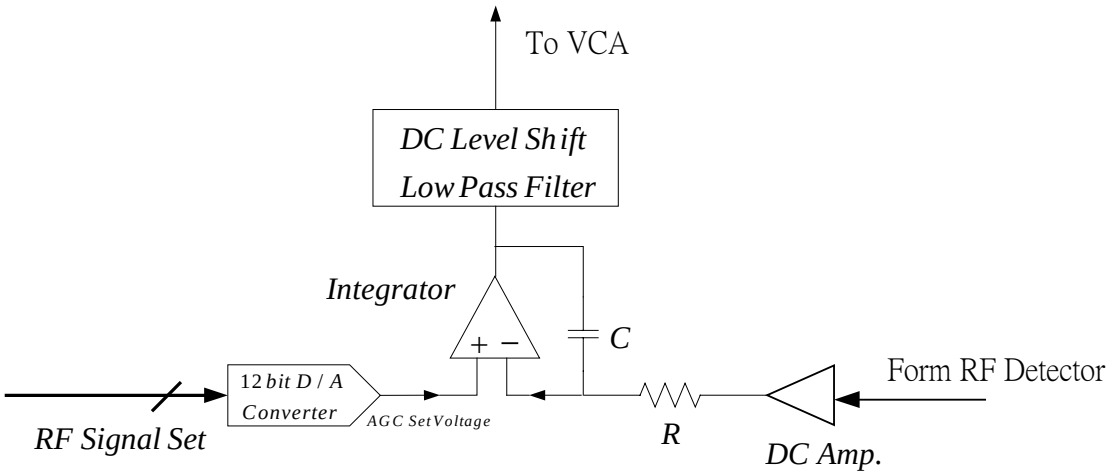


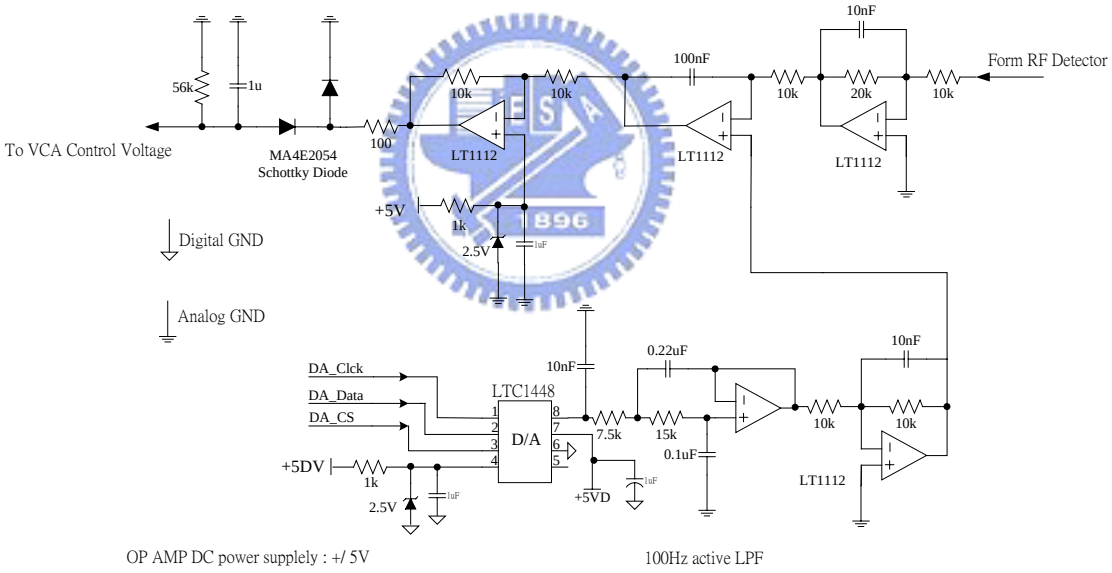
Figure 3-15 VCA attenuation performance

3-2-3 AGC Loop Design

The AGC loop controller block diagram and schematic are shown figure 3-16. The LT1112 is dual op amps and achieve DC amplifier, Integrator and DC level shift circuits. The LTC1448 is a dual rail-to-rail voltage output, 12-bit digital-to-analog converter (DAC). It includes rail-to-rail output buffer amplifiers and an easy-to-use 3-wire serial interface.



(a)

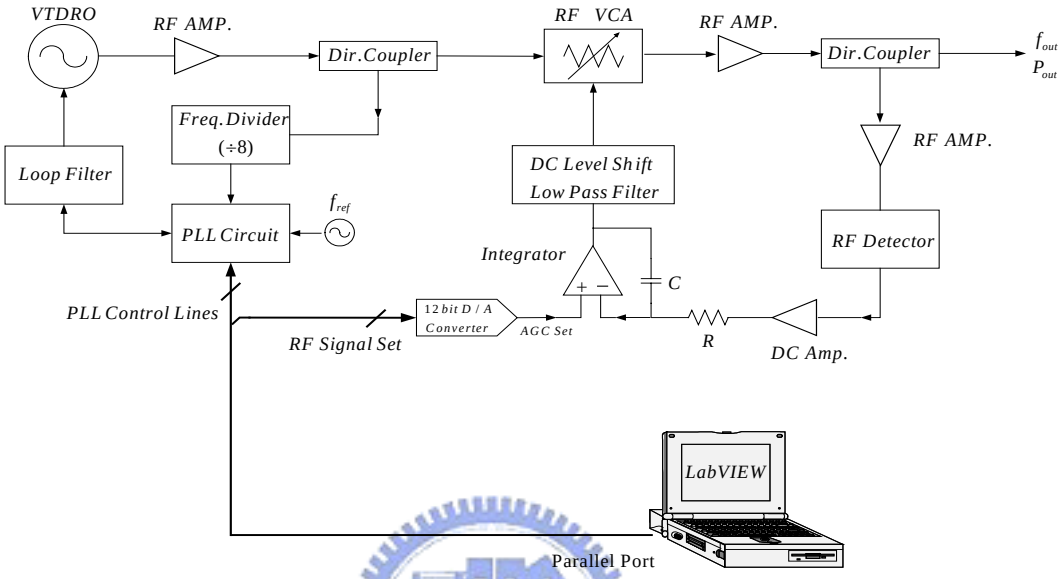


(b)

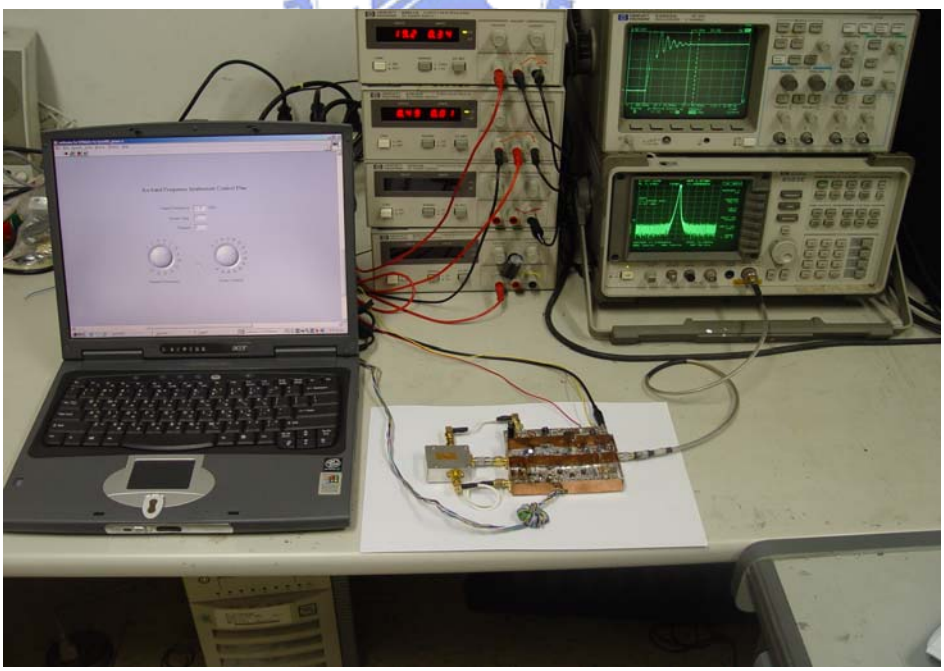
Figure 3-16 AGC loop structure (a) block diagram (b) schematic

3-3 Power Control Loop Measurements

Finally, we should measure the power control loop performance. The test setup is shown as figure 3-17.



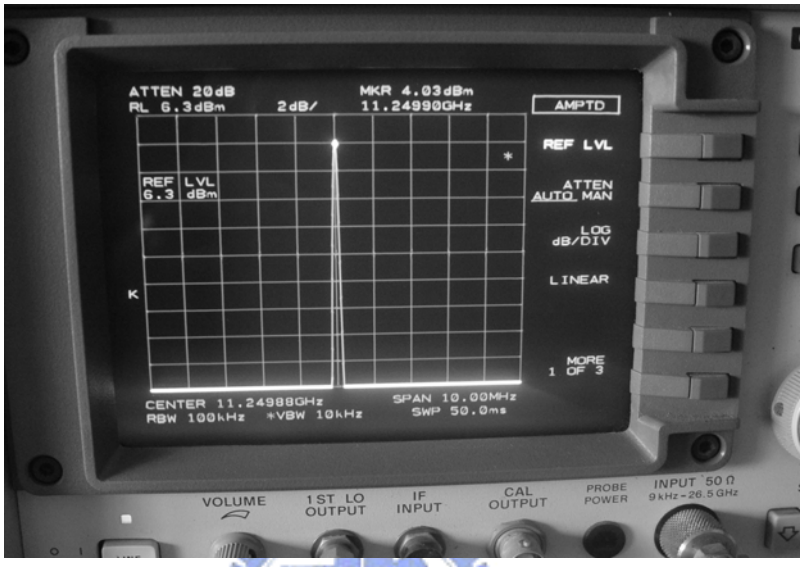
(a)



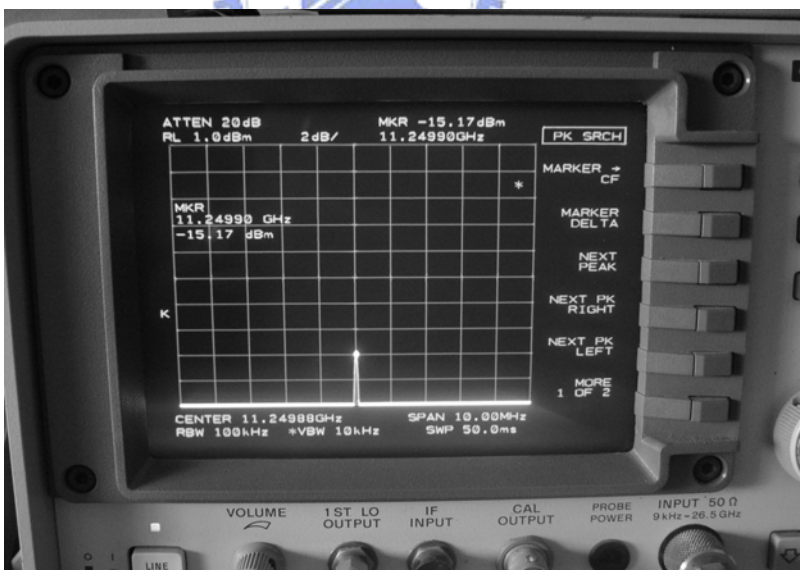
(b)

Figure 3-17 Power control loop measurement setup (a) block diagram (b) measurement etup

The dynamic range of control loop measurement is shown figure 3-18. The range adjust from 4 dB to -15 dB and the flatness of output measurement is shown figure 3-19.



(a)



(b)

Figure 3-18 Dynamic range measurement

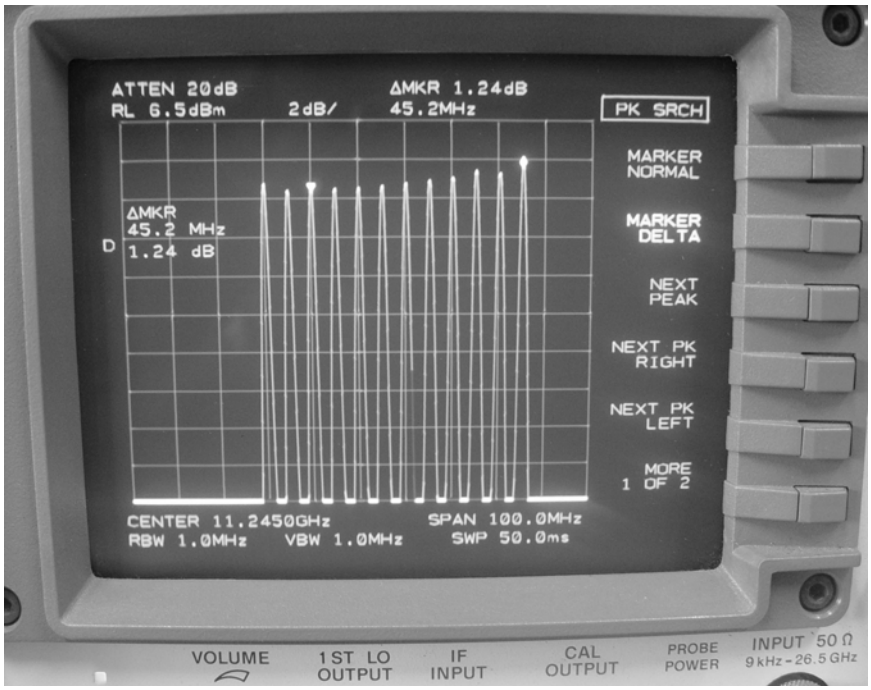
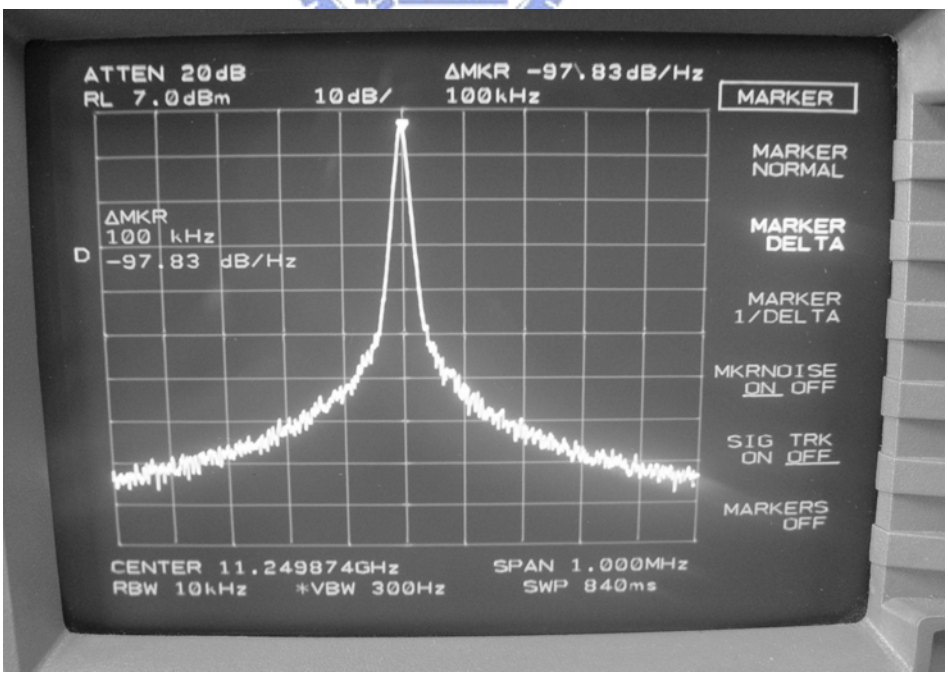


Figure 3-19 synthesizer output flatness

The synthesizer phase noise measure is shown figure 3-20. The power control loop not degrades phase noise performance.



(a)

Figure 3-20 synthesizer phase noise at 100 KHz offset

Figure 3-19 presents the measured frequency tune range. The output power of synthesizer was kept by the power control loop and adjustment output power. The table 3-1 shows the synthesizer specifications.

Frequency Range	11.23GHz to 11.85GHz
Output Power	+4 dBm to –15dBm
Phase noise	97.83 dBc @ 100KHz
DC power supply	+15V ; -5V

Table 3-1 The synthesizer specifications.

Chapter 4

CMOS LC Oscillator and Frequency Divider Design

In this chapter, we present a method for design of CMOS Voltage controlled oscillator (VCO) and frequency divider. They are fully integrated in bulk CMOS technology operating at 5GHz. Figure 4-1 is shown the block diagram.

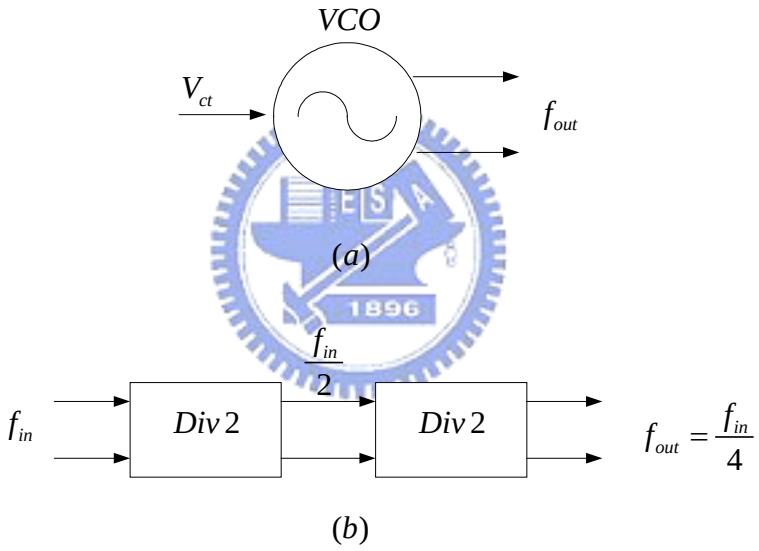
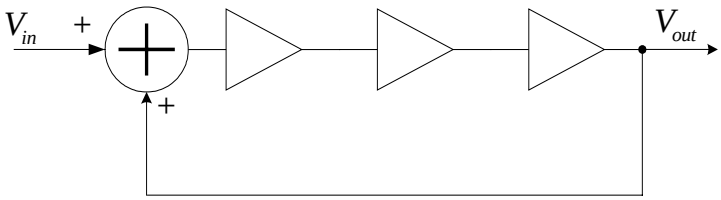


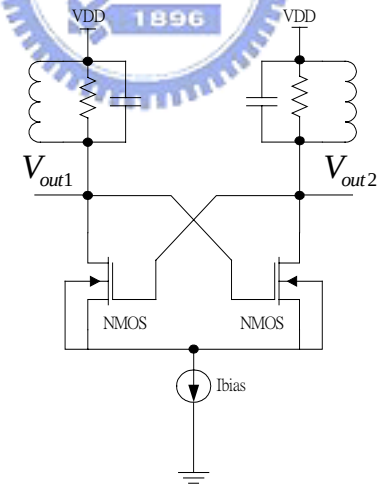
Figure 4-1 CMOS simulation block diagram (a) CMOS VCO simulation block diagram (b) frequency divider simulation block diagram

4-1 CMOS Voltage controlled oscillator (VCO) Design

For fully integrated CMOS oscillator, two common approaches are ring oscillators and LC oscillators (see figure 4-2). The advantage of ring oscillators is without any passive element such as inductors and capacitors. Because of there is no filtering action shaping the phase noise of the output signal, the ring oscillators generally show a very poor phase noise performance compared to LC oscillators [32].



(*a*)



(*b*)

Figure 4-2 CMOS common approaches oscillator (a)Three-stage ring oscillators (b) LC oscillators

A LC oscillator consists of a parallel LC tank and active circuit that compensated for the losses in the passive elements. The LC tank resonates at the

frequency

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{4-1}$$

In the RF CMOS design, the lack of high-quality on-chip inductors is one of the major drawbacks. The most common topology of on-chip inductors is the square spiral and circular spiral inductors.

In the VCO, the oscillators frequency must be tunable by the varactor element .The capacitance of a varactor can be controlled between C1 and C2 by a control voltage. For ideal VCO, it is a linear function of the control voltage .The function and block of VCO are shown in figure 4-3.

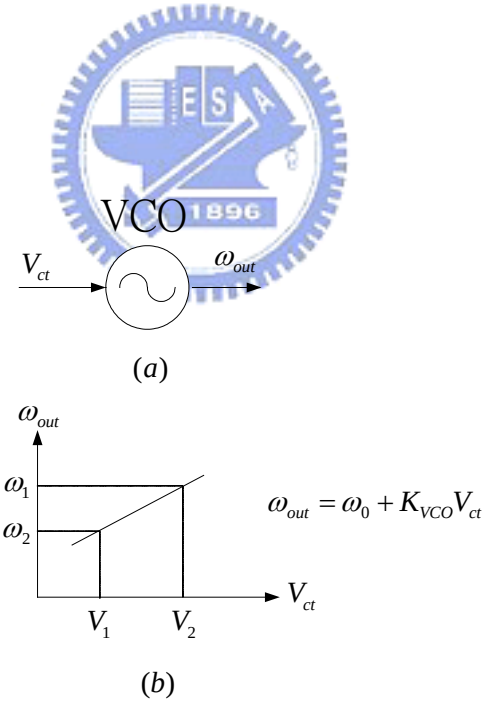


Figure 4-3 VCO function and block diagram (a) VCO diagram (b) VCO function

4-1-1 Topology of an NMOS-PMOS LC oscillator

In this case, the conventions NMOS-PMOS cross-coupled oscillator (see figure 4-4) is used as the design for several reasons. The differential operation mitigates undesirable common-mode effects such as DC supply noise and extrinsic substrate. For the same bias circuit, the oscillation amplitude of this configuration is a factor of two large than that of the NMOS-only structure. The rise and fall time symmetry of oscillation waveform reduces the up-conversion of the transistor noise.

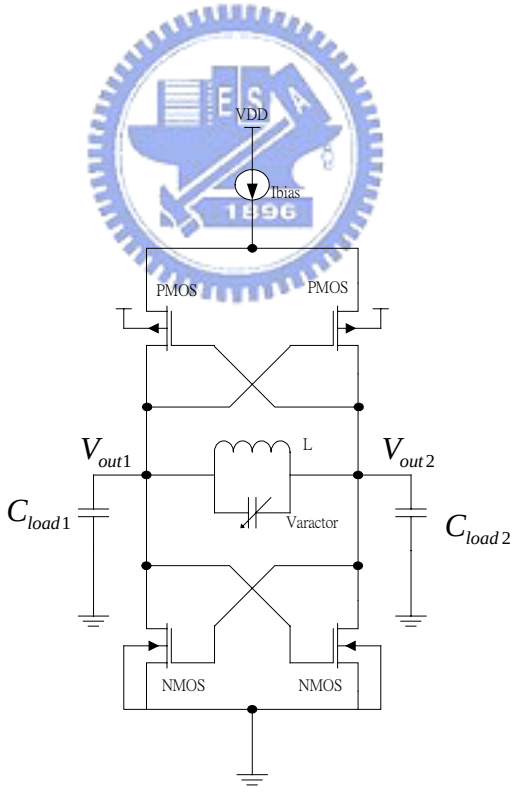


Figure 4-4 NMOS-PMOS cross-coupled oscillator schematic

The small-signal equivalent model of NMOS-PMOS cross-coupled oscillator is shown in figure 4-5. The equivalent capacitance of a NMOS-pair and a PMOS-pair between the two nodes are thus [33]:

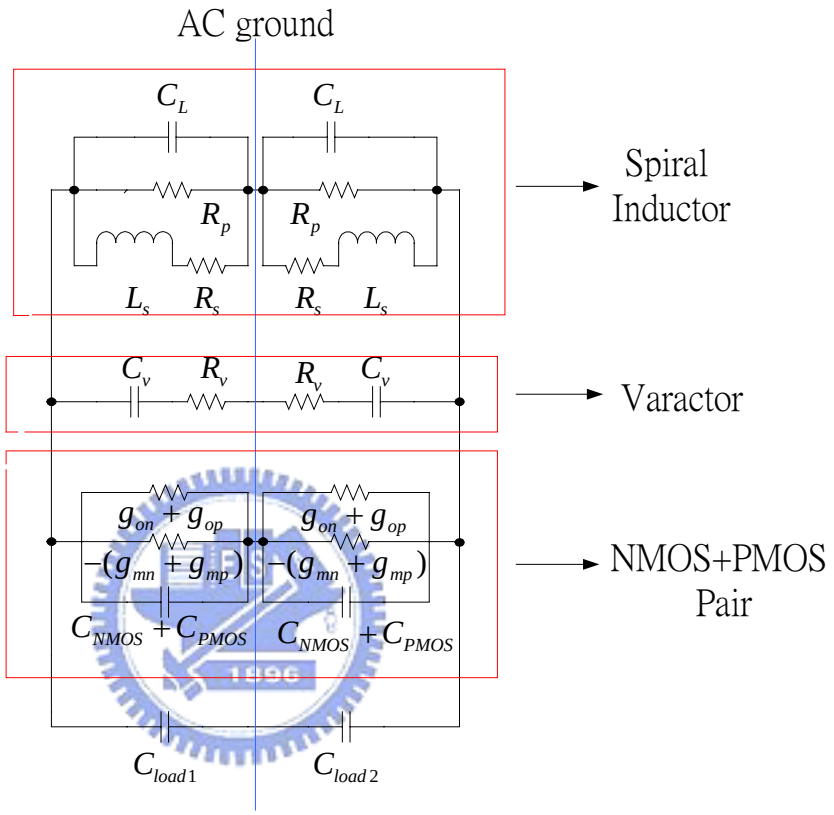


Figure 4-5 Small-signal equivalent circuit of the VCO core

The small-signal transconductance of a single NFET and PFET were defined g_{mn} and g_{mp}. In the NMOS-PMOS LC VCO, the output signal is the differential voltage $V_{out1}-V_{out2}$. From figure 4-4, the $V_{\tan k}=V_{out1}-V_{out2}$. The tank voltage can be expressed as [32][33]:

$$V_{\tan k}=\begin{cases} I_{bias}R_{\tan k}=\dfrac{I_{bias}}{g_{\tan k}} & \text{for current limited regime} \\ V_{\lim it} & \text{for voltage limited regime} \end{cases} \tag{4-2}$$

The design process can be summed up in following steps:

1、 Set $g_{mn}=g_{mp}$ to improved the $1/f^3$ corner of phase noise.

2、The tail current is set depending on the power consumption limit .

3、 The conductance is calculated keeping in mind the voltage swing specification

$$V_{out}\le I_{bias}R_{\tan k} \tag{4-3}$$

4、 To ensure start-up the gm of cross-couple devices are set 4 time more than $g_{\tan k}$

$$\frac{gm}{g_{\tan k}}\ge 4 \tag{4-4}$$

5 、The maximum and minimum capacitance value needed for the required tuning range of frequency is calculated as

$$\begin{aligned} \omega_{\min}&=\frac{1}{\sqrt{L_{\tan k}C_{total,\max}}} \\ \omega_{\max}&=\frac{1}{\sqrt{L_{\tan k}C_{total,\min}}} \end{aligned} \tag{4-5}$$

6、 The phase noise in $1/f^2$ region can be predicted using Leeson's equation [][]:

$$L(\Delta f)=10\log\left\{0.5\left[\left(\frac{F_0}{2Q\Delta f}\right)^2+1\right]\left(\frac{F_c}{\Delta f}+1\right)\left(\frac{FkT}{P_0}\right)\right\} \quad dBc/Hz \tag{4-6}$$

where

F_0 =Oscillator frequency

Q =Loaded resonator quality

Δf =Frequency offset with respect to the carrier

F_c =Flicker noise cutoff frequency of the transistor amplifier

F =Noise factor of the transistor amplifier

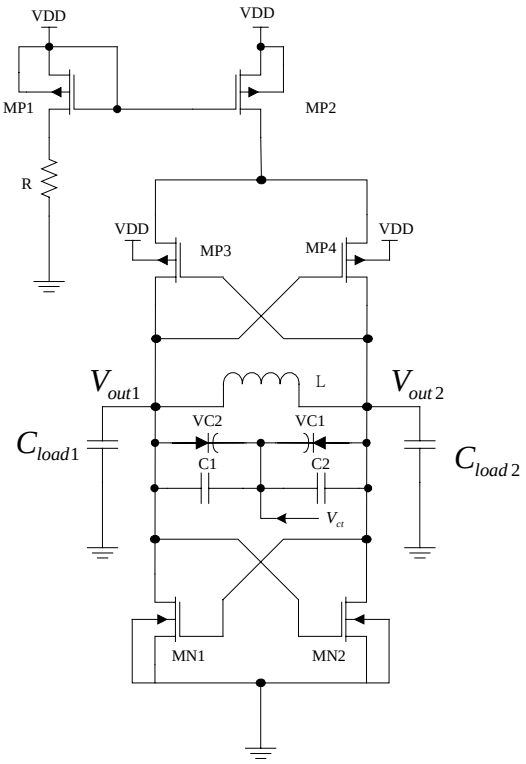
k =Boltzmann's constant

T =Temperature in Kelvin

P_0 =Output power of the oscillator

4-1-2 Simulation result of a 5GHz NMOS-PMOS LC VCO

In this case, the Hspice and Laker software achieved the 5GHz NMOS-PMOS LC VCO design. Figure 4-6 presents the schematic of the VCO. The post simulation result is show in Figure 4-7. Figure 4-8 and table 4-1 are shown the VCO layout and VCO specifications.

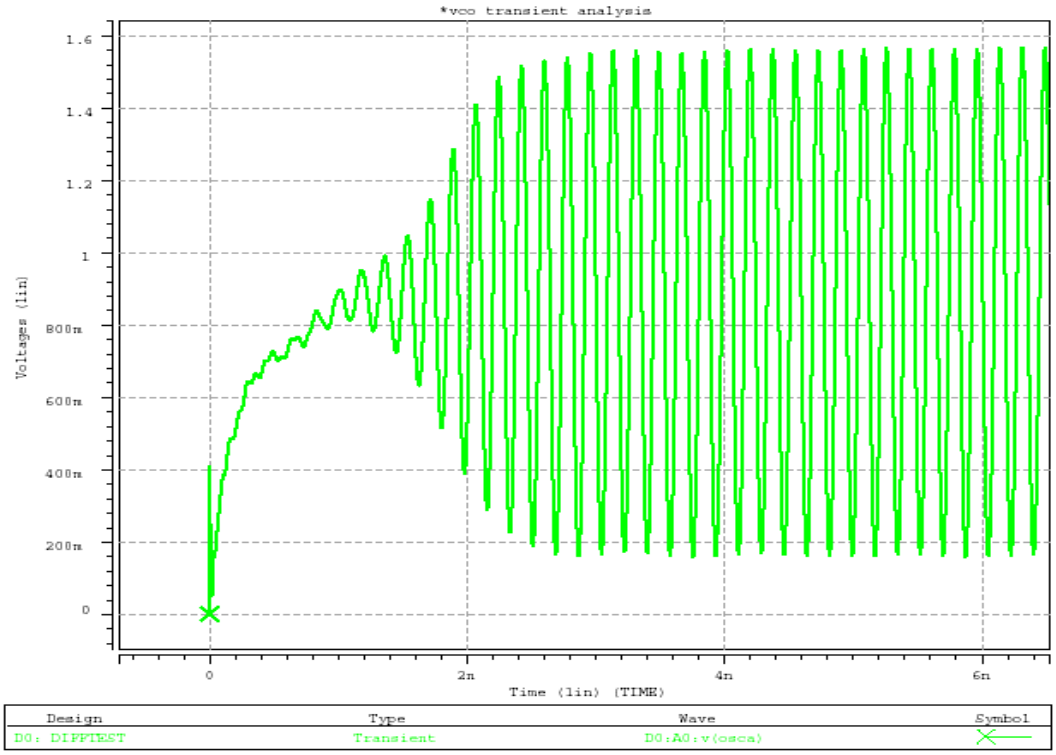


(a)

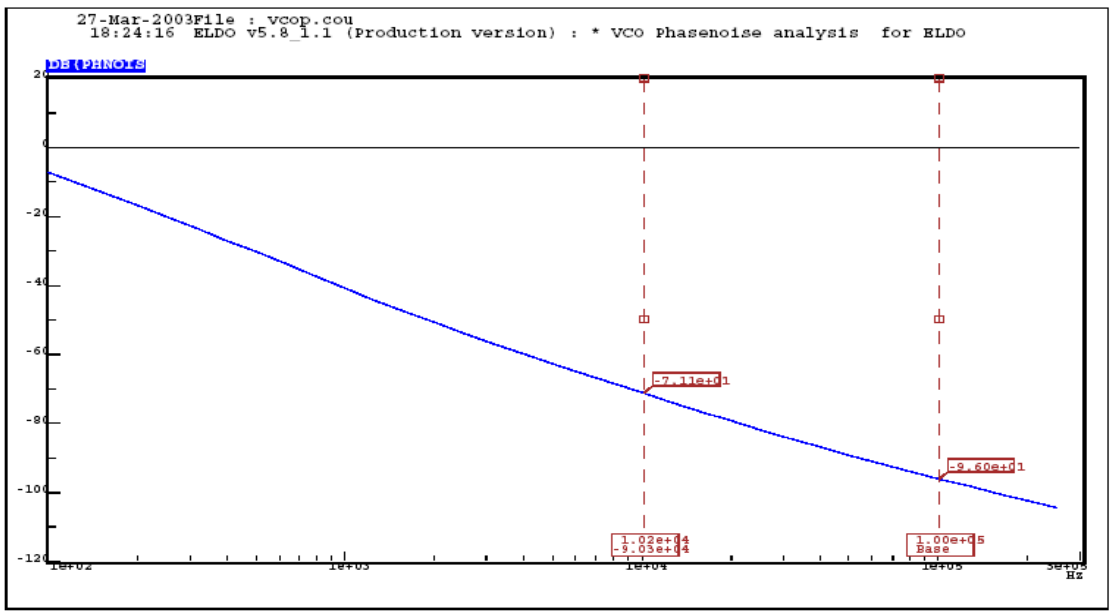
Device	MP1	MP2	MP3,MP4	MN1,MN2	C1,C2	R
L/W	0.24u / 50u	0.24u / 140u	0.24u / 120u	0.24u / 40u	NC	2.7K
Device	L	C_{load1}, C_{load2}	VC1, VC2			
	2nH	0.4pF	0.5pF			

(b)

Figure 4-6 VCO schematic (a) schematic (b) CMOS size


*vco transient analysis
Voltages (lin)
1.6
1.4
1.2
1
800m
600m
400m
200m
0
0
2n
4n
6n
Time (lin) (TIME)
Design
Type
Wave
Symbol
DO: DIPPTEST
Transient
DO:A0:v(osca)

(a)


27-Mar-2003File : vcop.cou
18:24:16 ELDO v5.8_1.1 (Production version) : * VCO Phasenoise analysis for ELDO
DB(PHNOIS)
-7.11e+01
-9.60e+01
1.02e+04
-9.03e+04
1.00e+05
Base
Hz

(c)

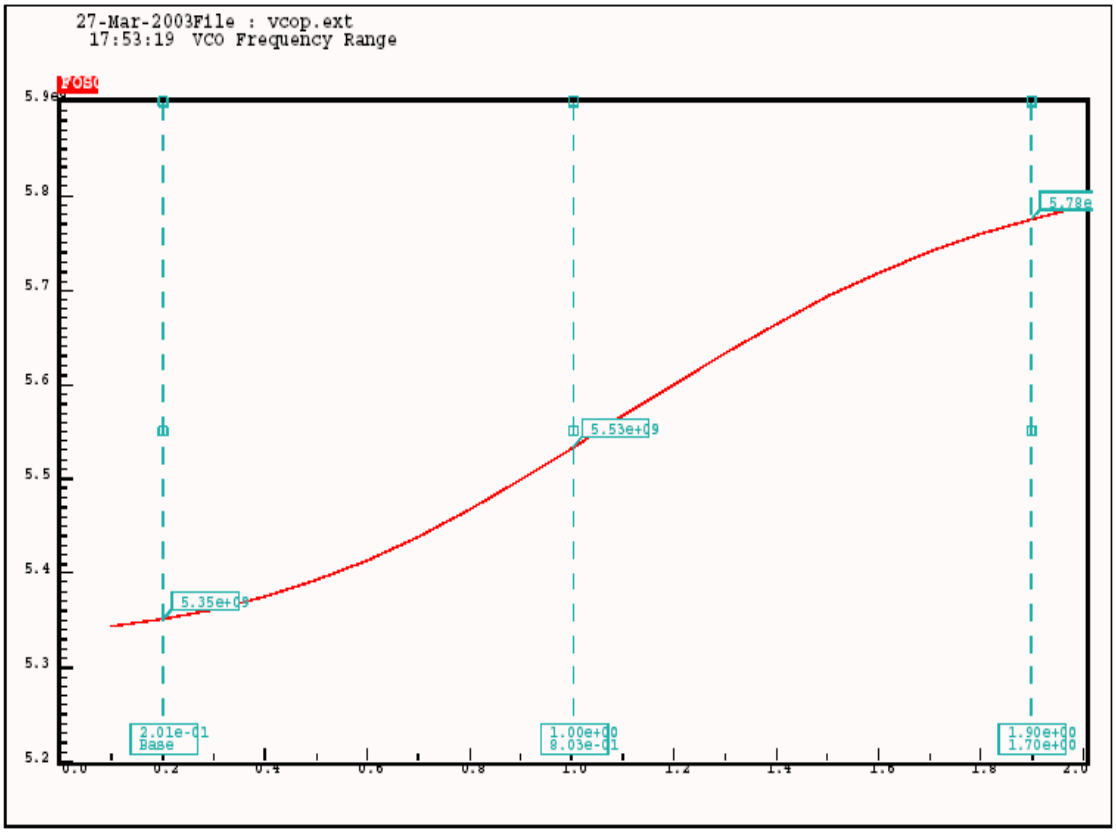


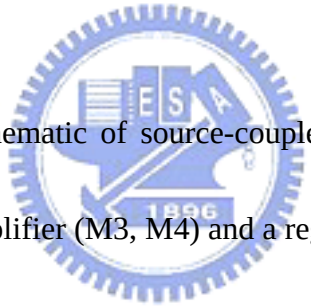
Figure 4-7 CMOS VCO simulation result (a) VCO start up (b) phase noise (c) VCO tuning range

Item	
Voltage Supply	2.5V
Frequency Tuning range	5.3GHz to 5.7GHz
Output Load	0.4pF
Output Swing Amplitude	1.3 V_{p-p}
Power Consumption	< 20 mW

Table 4-1 VCO specification

4-2 Frequency divider design

In the 5GHz frequency synthesizer, the frequency divider is important circuit . It is to be used in a phase locked loop to step down the frequency of VCO. The circuit most difficult to design is the first stage of diver, which should operated at 5GHz .In the case, the source-coupled latch has a reduced output swing that facilitates high speed. The block diagram of the frequency divider is shown in figure 4-1(b). This divider implemented a cascade of 2 divider by 2 circuits.



The conventions schematic of source-coupled latch is shown in figure 4-9. It consists of a differential amplifier (M3, M4) and a regenerator (M5, M6) . Two FETs are placed between the current source and differential/regenerator, they are acting switches controlled by the CK and $\overline{CK}$ signals. When the M2 is turn on by the clock activated, the function of differential amplifier is passing the input signal to the outputs. When the M1 is turn on by the clockbar activated, the regenerator lactching the outputs Q and $\overline{Q}$.

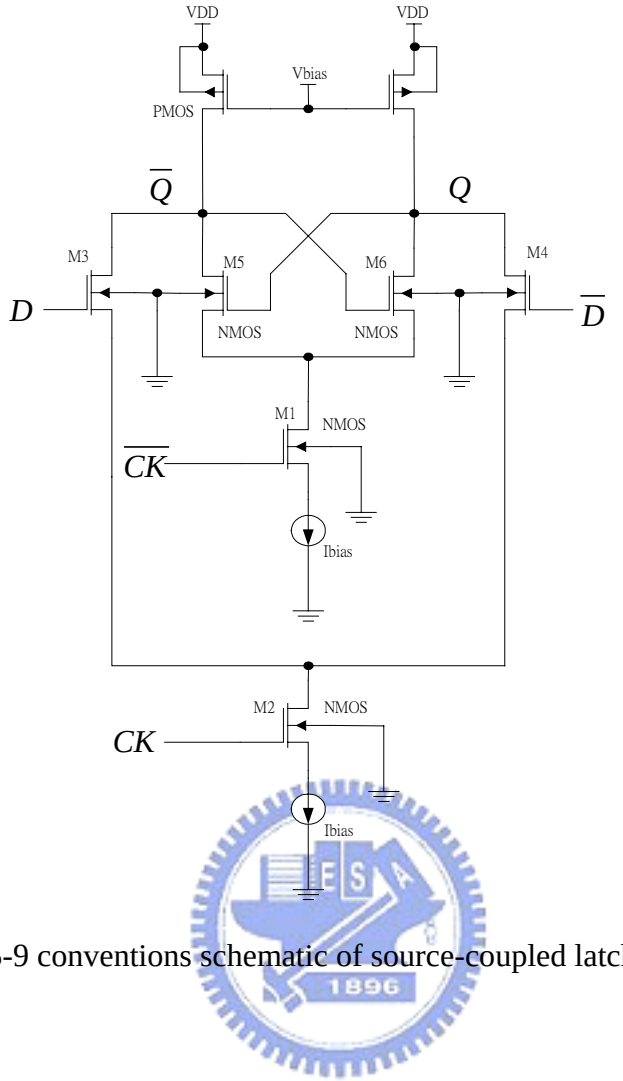


Figure 5-9 conventions schematic of source-coupled latch

The two latches achieved the unit stage of divider. Two latches can be connected as shown in figure 4-10. The output of one latch is fed to the input of the second, whose output is inverted and tied back to the inputs of the first latch. This results in an output signal, taken from the outputs of the second latch, that has half the frequency of the clock signal.

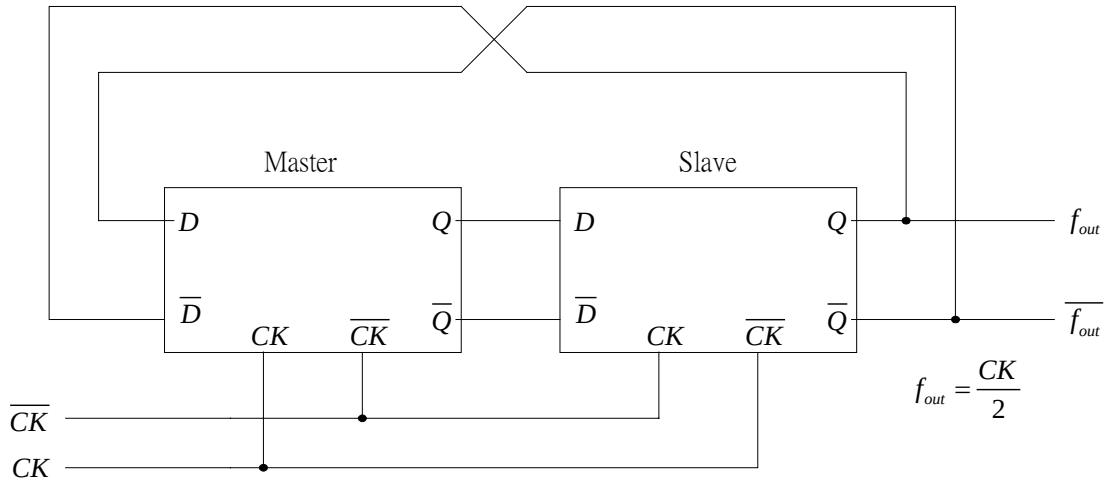


Figure 4-10 unit stage of divider

The design considerations of the basic latch are as follows:

1、 The FETs are biasing in the active region , they will allow for fast operation of the FETs. The proper overdrive voltages and sizeing of the FETs can cerated by the proper biasing of the gate voltage.

2、 The regenerator FETs have a large enough gm can overcome the pull up resistors . This is keep the outputs Q and $\overline{Q}$ latched to VDD and id*R.

4-2-1 Simulation result of a 5GHz frequency divider

In this case, the 5GHz frequency divider design was achieved by the Hspice and Laker software. Figure 4-11 presents the block diagram of the divider and the schematic of divider is shown figure 4-12. The post simulation result as show in Figure 4-13. Figure 4-14 and table 4-2 are shown the divider layout and VCO specifications.

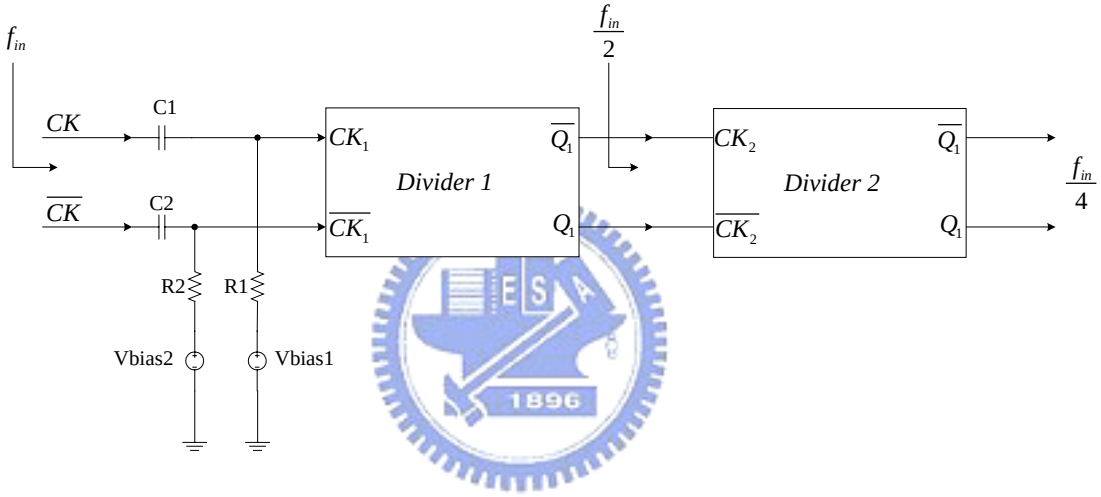
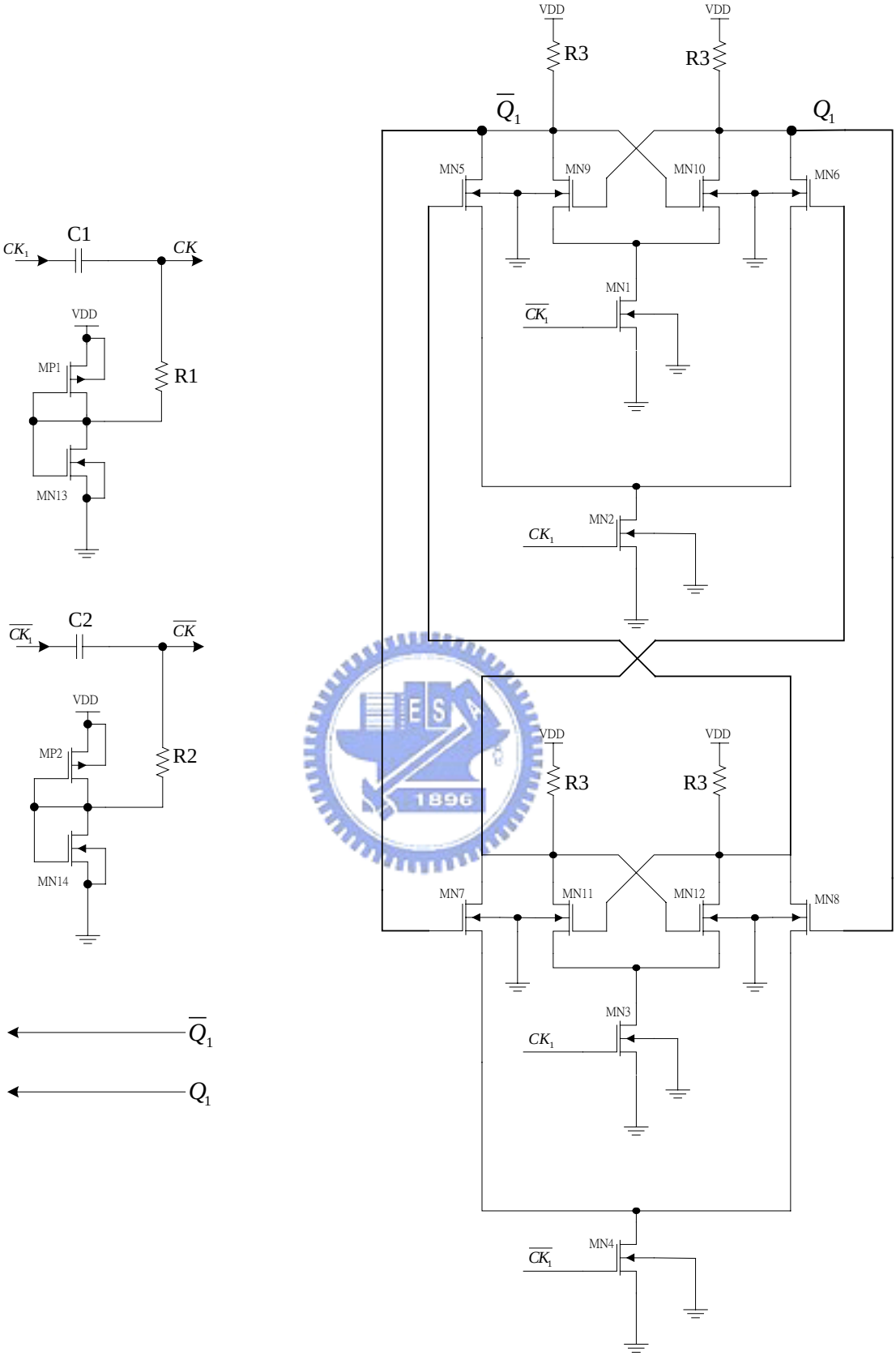
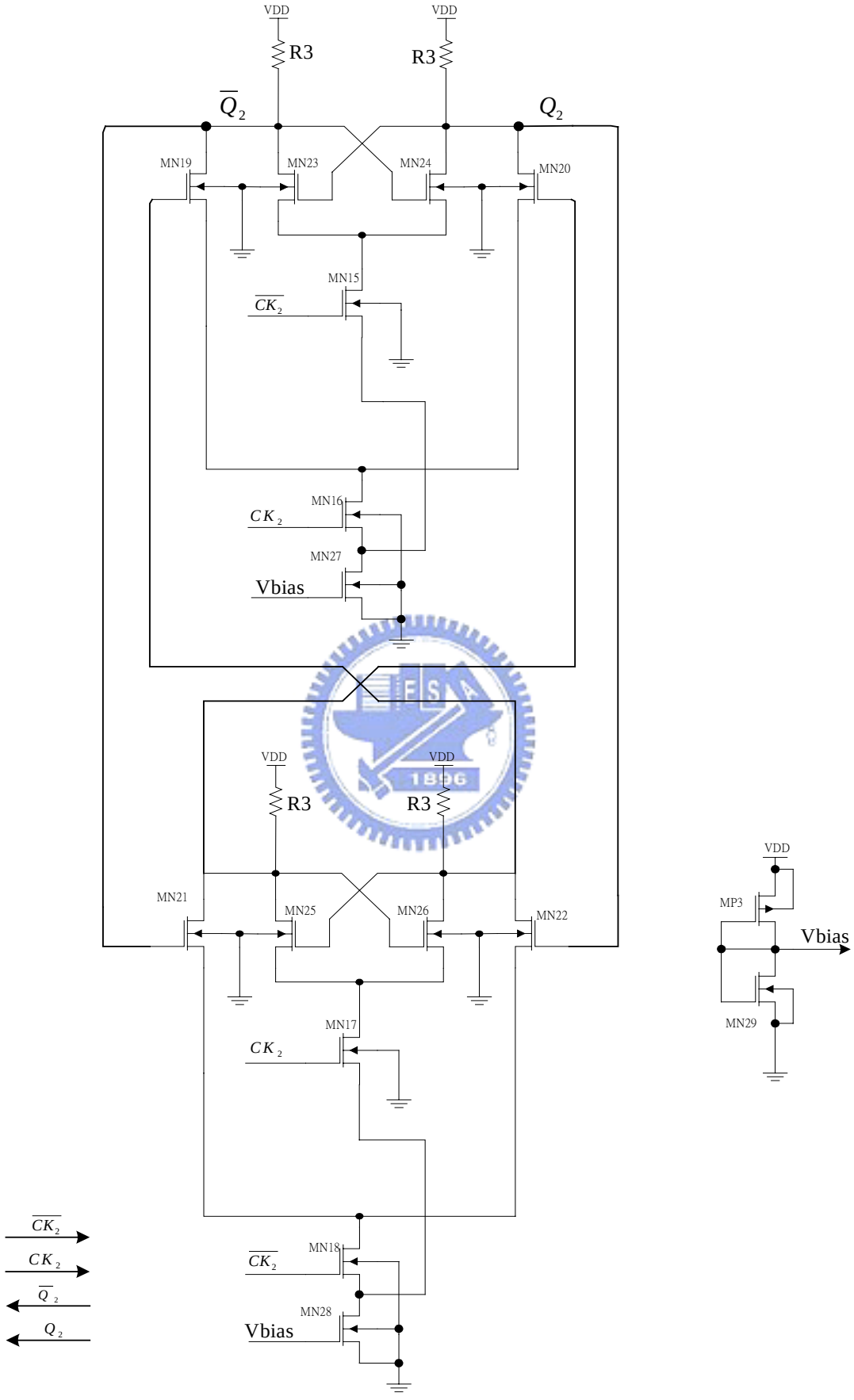


Figure 4-11 Frequency divider block diagram


C1
CK_1
CK
VDD
MP1
R1
MN13
C2
$\overline{CK_1}$
$\overline{CK}$
VDD
MP2
R2
MN14
$\overline{Q_1}$
Q_1
VDD
VDD
R3
R3
$\overline{Q_1}$
Q_1
MN5
MN9
MN10
MN6
MN1
$\overline{CK_1}$
MN2
CK_1
VDD
VDD
R3
R3
MN7
MN11
MN12
MN8
MN3
CK_1
MN4
$\overline{CK_1}$

(a)


VDD
R3
VDD
R3
$\overline{Q}_2$
Q_2
MN19
MN23
MN24
MN20
MN15
$\overline{CK}_2$
MN16
CK_2
MN27
Vbias
VDD
R3
VDD
R3
MN21
MN25
MN26
MN22
MN17
CK_2
$\overline{CK}_2$
CK_2
$\overline{Q}_2$
Q_2
MN18
$\overline{CK}_2$
MN28
Vbias
VDD
MP3
Vbias
MN29

(b)

Device	MP1,MP2	MN1,MN3	MN2,MN4	MN5,MN6	MN7,MN8	MN9,MN10
L/W	0.24u / 35u	0.24u / 40u	0.24u / 80u	0.24u / 80u	0.24u / 80u	0.24u / 40u
Device	MN11,MN12	MN13,MN14	MN15,MN16	MN17,MN18	MN19,MN20	MN21,MN22
L/W	0.24u / 40u	0.24u / 10u	0.24u / 40u	0.24u / 40u	0.24u / 40u	0.24u / 40u
Device	MN23,MN24	MN25,MN26	MN27,MN28	MN29	MP3	
L/W	0.24u / 40u	0.24u / 40u	0.24u / 160u	0.24u / 10u	0.24u / 35u	
Device	C1,C2	R1,R2	R3			
L/W	30u / 30u	1.6k	0.2k			

(c)

Figure 4-12 Frequency divider schematic (a) divider1 schematic (b) divider2 schematic

(c)CMOS size

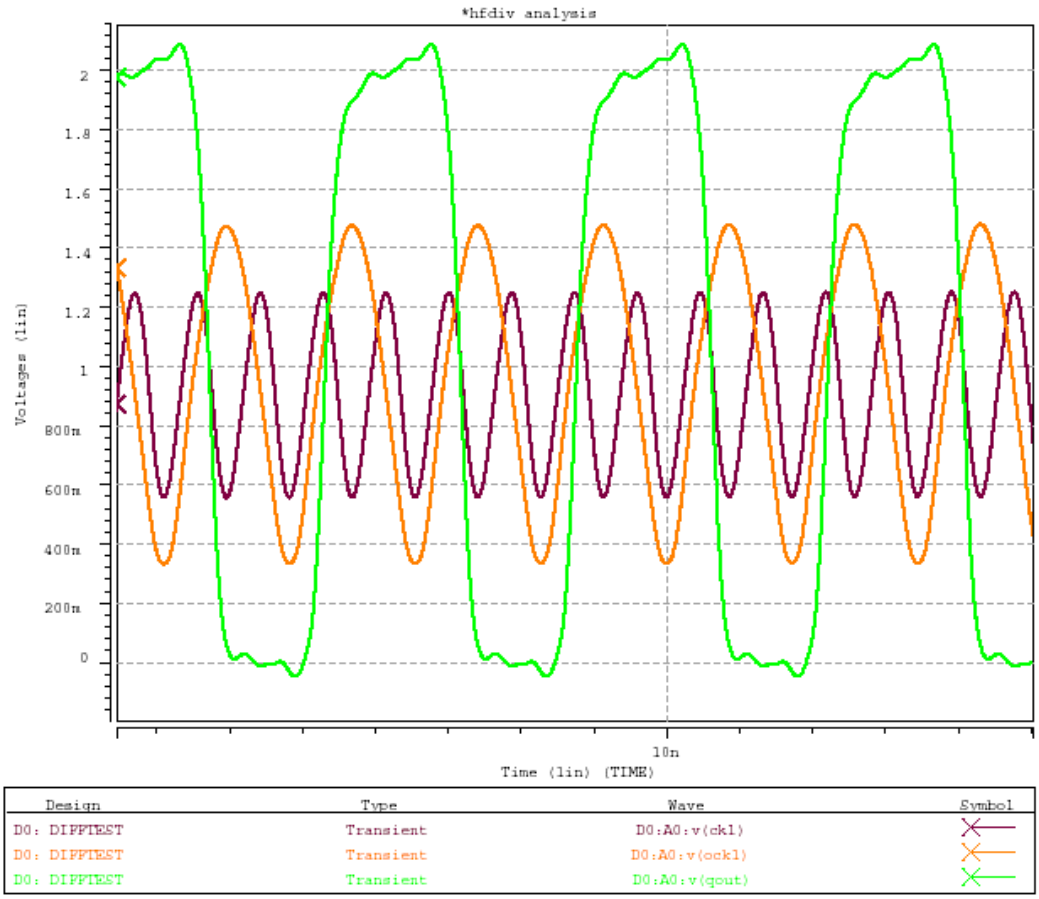


Figure 4-13 the post simulation result

Item	
Voltage Supply	2.5V
Input Frequency range	5.3GHz to 5.7GHz
Output Frequency range	1.325Ghz to 1.425GHz
Input Swing Amplitude	0.6 V_{p-p}
Output Swing Amplitude	$1V_{p-p}$
Power Consumption	< 80 mW

Table 4-2 divider specification

Chapter 5
Conclusion

In this thesis, the basic principles of phase-locked loop, automatic gain control loop and CMOS integrated circuit are explored. Special attentions have been directed to the performance of power level control and frequency control.

In the Ku-band frequency synthesizer, this new structure is realized by inserting AGC loop behind the phase-locked loop. The power level and frequency can be controlled. The frequency change and output power level of synthesizer will be compensated or set by the computer. In the thesis, we show the measurement data of AGC loop function. It can reduce VTDRO output power flatness from ±3dB to ±0.6dB and the output power of synthesizer can be set from +4dBm to –15dBm. Unfortunately, we found some problem of synthesizer. The output power flatness had varied ±0.7dB by the AGC loop steady-state error. That is from device nonlinear characteristic. Other problem of synthesizer, the divider of PLL controller degrades phase noise at 10KHz offset. We will cope with problems in the future. For application, this synthesizer connects with mixer or frequency multiplier generator and adjusting the synthesizer output power and frequency for the optimum performance.

In the CMOS integrated circuit, the conventional analysis of mentioned briefly. The analysis method gives designers a clear insight so the high performance voltage-controlled oscillator and frequency divider can be obtained. The circuit design process, simulation and layout are shown in the thesis.

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Appendix A

In this chapter, we will discuss the design and analysis of active loop filter. There are also op-amp based loop filter topologies as shown in the figure A-1.

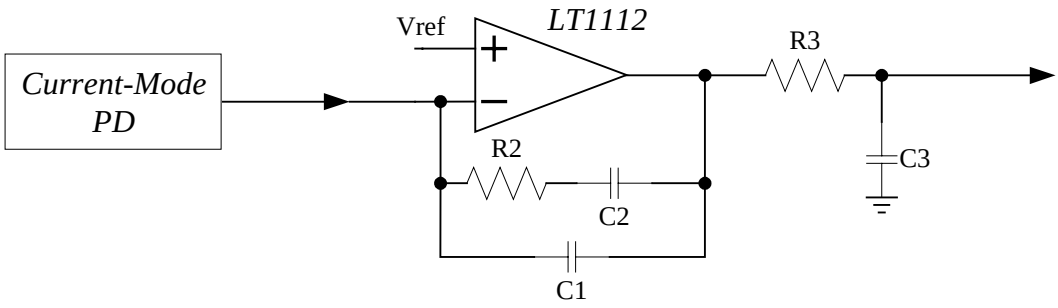

Figure A-1

From (2-15), we can find the relationships of Phase margin, Damping factor and Natural frequency. The table A-1 is show the relationships.

Phase margin , ϕ	Phase margin , ξ	Natural frequency , ω_n
30.00 degrees	0.6580	$0.7599 \times \omega_c$
35.00 degrees	0.6930	$0.7215 \times \omega_c$
36.87 degrees	0.7071	$0.7071 \times \omega_c$
40.00 degrees	0.7322	$0.6829 \times \omega_c$
45.00 degrees	0.7769	$0.6436 \times \omega_c$
50.00 degrees	0.8288	$0.6033 \times \omega_c$
55.00 degrees	0.8904	$0.5615 \times \omega_c$
60.00 degrees	0.9659	$0.5177 \times \omega_c$
61.93 degrees	1.0000	$0.5000 \times \omega_c$
65.00 degrees	1.0619	$0.4700 \times \omega_c$
70.00 degrees	1.1907	$0.4199 \times \omega_c$

Table A-1

The term of loop filter shown in as follows:

(1) f_{Range} – Frequency range of synthesizer.

(1) f_{step} – Maximum frequency change during a step or hop, from one frequency to another.

(3) f_{CH} – Channel spacing.

(2) t_s – The desired time for the carrier to step to a new frequency.

(3) f_a – The frequency of the carrier, within the desired time (ts), after a step or hop.

(4) ξ – Damping Factor.

(5) ω_n – Natural frequency

(6) I_{cp} – Charge Pump Current

(7) K_{VCO} – VCO sensitivity

With given values for ξ, t_s, K_{VCO}, f_{step}, f_a, I_{cp} and N, we can solve for the loop filter components .

$$\omega_n = \frac{-1}{t_s \zeta} \ln\left(\frac{f_a}{f_{step}}\right) \quad \text{(A-1)}$$

$$C_2 = \frac{I_{cp} K_{VCO}}{N(2\pi f_n)^2} \quad \text{(A-2)}$$

$$R_2 = 2\zeta \sqrt{\frac{N}{I_{cp} K_{VCO} C_2}} \quad \text{(A-3)}$$

$$C1 = \frac{C_2}{10} \tag{A-4}$$

$$R_3 = R_2 \tag{A-5}$$

$$C_3 = \frac{C_2}{10} \tag{A-6}$$

$$Loop\ Bandwidth = \frac{2\pi f_n(\zeta + \frac{1}{4\zeta})}{2} \tag{A-7}$$

Appendix B

In this chapter, we will discuss PLL and D/A converter code generator. This program is designed to run LMX1600 and LTC1448. The code generator is base on LabVIEW. The LMX1600 is integrated dual frequency PLL and the IF band was disabled by program code. The LMX1600 data registers and a sample setting is shown as Figure B-1. The R counter determines the channel bans width. The N counter determined the output frequency. Figure B-2 shows the LMX1600 registers structure. In the table B-1, for each register the MSB and is loaded first.

For the LTC1448, The data is loaded as one 24-bit word where the first 12 bits are for DAC A channel and the second 12 are for DAC B channel. For each register the MSB and is loaded first . The data structure is shown as figure B-3.

The series data was generator by the LabVIEW and program signals from the parallel port of the computer. When the load command is used, all data in all registers is sent . The LabVIEW control plane and program process are shown as figure B-4 and figure B-5. Figure B-6 show the time chart.

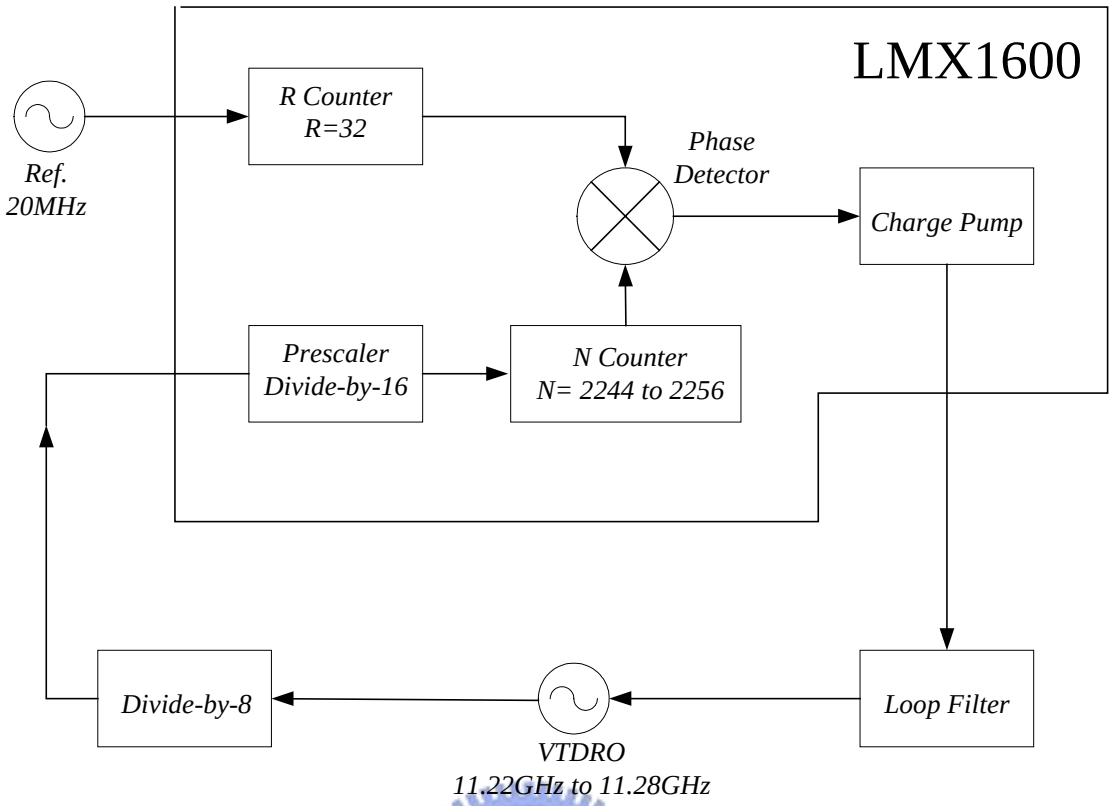

Figure B-1 LMX1600 data registers

	First Bit				SHIFT REGISTER BIT LOCATION												Last Bit	
	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AUX_R	FoLD				AUX_R_CNTR												0	0
AUX_N	AUX_B_CNTR												AUX_A_CNTR				0	1
MAIN_R	CP_WORD				MAIN_R_CNTR												1	0
MAIN_N	MAIN_B_CNTR and MAIN_A_CNTR																1	1

Figure B-2 LMX1600 data registers structure

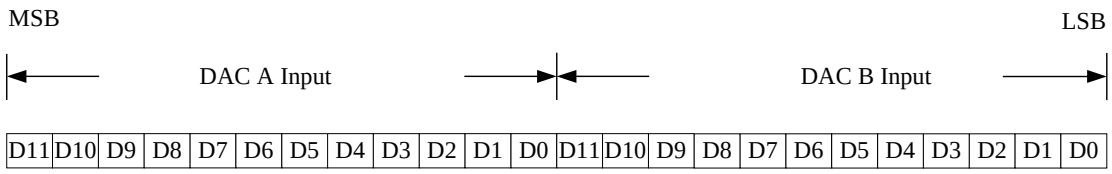

Figure B-3 LTC1448 data registers structure

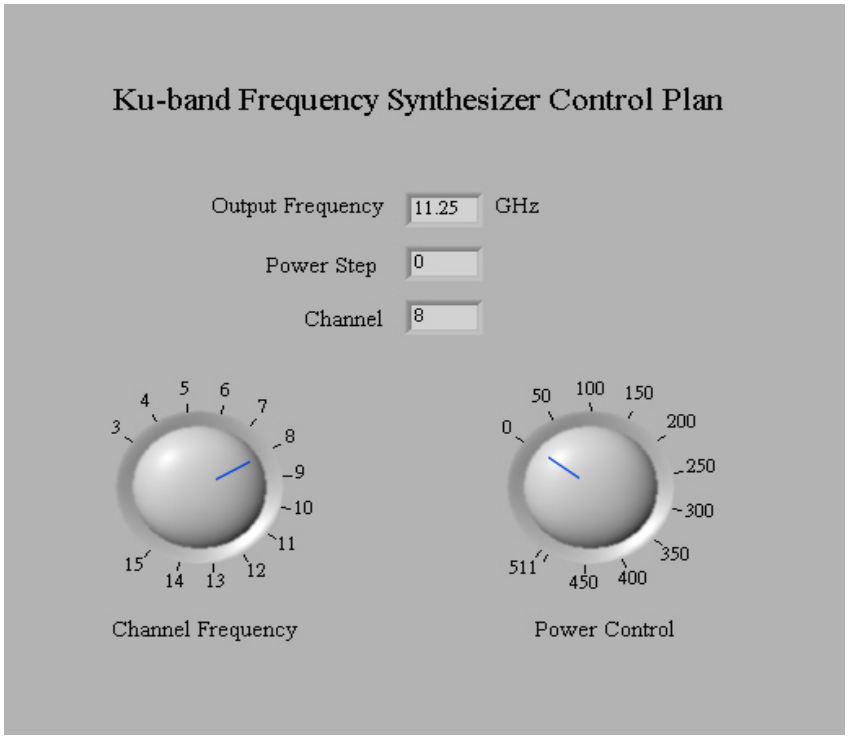

Figure B-4 LabVIEW control plane

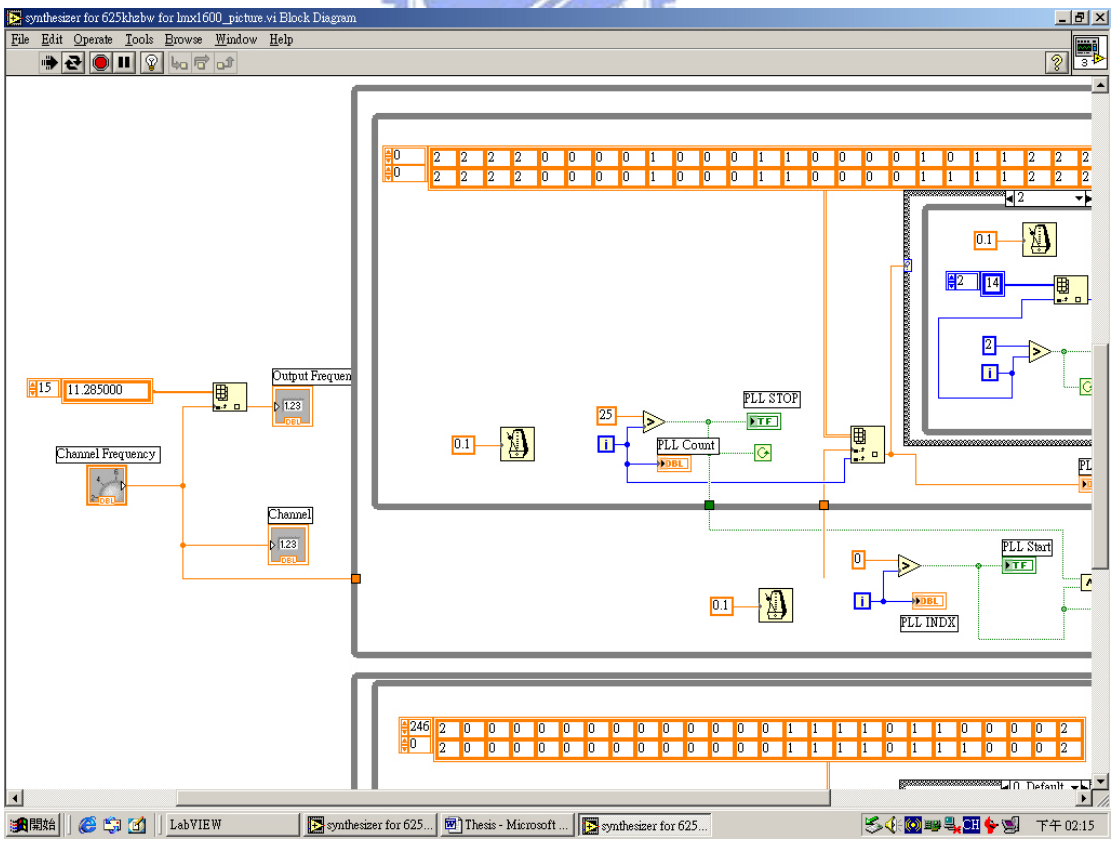

Figure B-5 LabVIEW program process

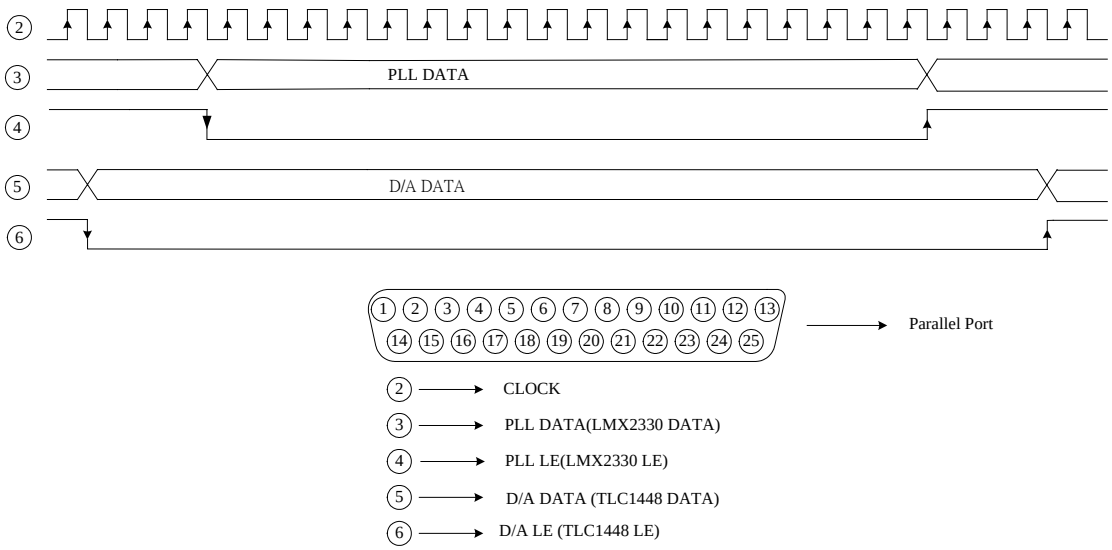

Figure B-6 Time chart