

國立交通大學

電機學院 電子與光電學程

碩士論文

應用於 1.5 伏特 3~10-GHz 超寬頻  
頻率合成器

The Design of 1.5-V 3~10-GHz CMOS  
Frequency Synthesizer for Ultra-Wide  
Band (UWB) Applications

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中華民國九十六年六月

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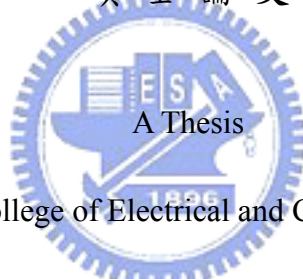
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電機學院 電子與光電學程  
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## 摘要

UWB(Ultra-Wideband; 超寬頻) 是一種以低功率、高速傳輸資料的短距離無線通訊技術，利用 ns 至 ps 的非正弦波窄脈衝傳輸。由於目前無線通訊系統的傳輸速率要求越來越高，例如：Bluetooth(藍芽)的傳輸率要 1MHz/bps，WLAN 的 Data Rate 大約 54MHz/bps。但在一些產品像 IEEE 1394 cables; 3G cell phones; print and external storage devices 的 Data Rate 都在幾百 Mbps，而 UWB 的 Data Rate 從 55 到 480Mbps，其高 Data Rate 的產品應用範圍就可以很寬泛，再加上頻帶非常寬及傳輸功率非常小，以致於抗干擾能力很強。綜合以上特點，所以 UWB 的架構才會孕育而生。因此已有一些 UWB Frequency Synthesizer 成功的以 CMOS 製作。但除了此電路有完整的頻率範圍(3432MHz~10032MHz)及低功率消耗(55.1mW~161.62mW)之外，其餘的發表均僅止於一部份的頻率範圍及高低功率消耗。這主要是因為在頻寬超過 6~7GHz 後，將 CMOS 整合於收發機中仍有一定的困難度。本篇論文闡述一個應用於 3~10 GHz 之超寬頻頻率合成器的設計方法與製作技術並依據國際電子電機學會所制定的 802.15.3a 規格作設計。論文中提出一個新的架構是由一個負迴授的鎖相迴路為

主體，它包含的元件有相位頻率偵測器(Phase Frequency Detector)、電荷充放器(Charge Pump)、迴路濾波器(Loop Filter)、壓控振盪器(Voltage Controlled Oscillator)、VCO 緩衝器(VCO Buffer)、多相位濾波器(Poly Phase Filter)、單邊帶混波器(SSB Mixer)、電流模式邏輯除法器(CML Divider)、頻帶選擇器(Band Selector)組合而成。便可得到整個頻率合成器所需要的頻段(3432MHz~10032MHz)，並且整合於單一晶片中。

在晶片設計上，針對一個 1.5V 3~10GHz 的頻率合成器，以 0.18  $\mu\text{m}$  1P6M CMOS 製程完成。在 1.5V 的操作電壓下，功率消耗為 55.1~161.62 mW，晶片面積為 1900  $\mu\text{m} \times 1900 \mu\text{m}$ 。



# The Design of 1.5-V 3~10-GHz CMOS Frequency Synthesizer for Ultra-Wide Band (UWB) Applications


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## Abstract

The logo of National Chiao Tung University is a circular emblem with a gear-like border. Inside the circle, there is a stylized representation of a building or structure with the letters 'ES' and 'A' visible. The logo is positioned behind the abstract text.

UWB (Ultra-Wideband; Ultra wide band) is a kind of wireless communication technology of short distance of transmitting the materials with low power, at a high speed; utilize ps or ns non- sinusoidal wave narrow pulse to Transmission. Because the transfer rate of the wireless communication system requires higher and higher at present, for example: data rate of Bluetooth require 1MHz/bps, date rate of WLAN probably 54MHz/bps. But look like IEEE 1394 cables in some products; 3G cell phones; date rate of print and external storage devices is in several hundred Mbps, and data rate of UWB is from 55 to 480Mbps, high products of Date Rate its range of application can very wide to suffused. In addition, frequency band very wide to transmit power very much little, anti-interference very capable. According to synthesize the above characteristic, so the structure of UWB will just be arisen. So already some UWB frequency synthesizer has been made successfully with CMOS

process. But except this circuit has intact for frequency range (3432MHz~10032MHz) and low power consumption (55.1mW~161.62mW), the rest are issued and only stopped in the frequency range of a part and high power consumption. This because in frequently wide to after exceeding 6~7 GHz, is it still have sure difficulty in transceiver to combine CMOS mainly. This thesis is explained and according to 802.15.3 a which the international electronic electrical machinery society make in an ultra wide-band frequency synthesizer design method to apply 3~10 GHz and manufacturing technology. It is a subject by the phase lock loop circuit that negative feedback a new structure in the thesis, the frequency synthesizer is composed of a phase frequency detector, a charge pump, a loop filter, a VCO, a VCO buffer, four poly phase filter, three SSB mixer, five CML divider, two band selector be make up. Can receive the frequency band (10032MHz of 3432MHz) that the whole frequency synthesizer need, and combine in the single chip. On chip design, a 1.5V 3~10GHz frequency synthesizer, make with 0.18um 1P6M CMOS process finish. Under the voltage of operation of 1.5V, power consumption is 55.1~161.62mW, the area of the chip is 1900 $\mu$ m \* 1900 $\mu$ m.

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首先，我要對我的指導教授吳重雨老師致上最誠摯的感謝。老師在這三年裡不論在硬體或是軟體上提供了我一個最佳的學習環境，不但使我學會了積體電路設計的專業知識以及培養面對問題、解決問題的態度與方法。在老師的諄諄教誨下，讓我得到許多電路設計的專業知識，更學習解決問題的正確態度與方法。雖然過程中倍感艱辛，但卻獲益良多。

其次，在這三年內，承蒙加爾發半導體的同意得以進修，在此感謝幫助過我的同仁給予我的支持與鼓勵。特別是黃伯修董事長、廖慶安總經理和高宏鑫經理，因為有了他們的支持才得以順利完成研究所的學業。

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郭豐維

96年5月

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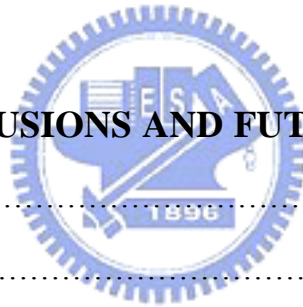
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# Chapter 1

## Introduction

### 1.1 Motivation

Nowadays, wireless products become more and more popular. This creates a large demand on RF transceivers chips. In RF transceiver, frequency synthesizer is one of the key components. Therefore, the design of synthesizers remains one of the challenges in RF systems. The demands make the performance of low spur level, low phase noise, high frequency resolution and fast settling time more important. On the other hand, the channel is more and more closer each other then the spurious tones must be suppressed otherwise should be interfered with adjacent channel. And for the receiver of image-reject architecture, we also need the outputs of frequency synthesizer would be quadrature signals. So synthesizer design still remains one of the challenging blocks in RF systems because it must meet very stringent requirements.

Some published frequency synthesizer for UWB applications have been reviewed and surveyed. Based on the drawbacks of previous works and considerations mentioned above, an attempt to design a low power, full band frequency synthesizer for UWB applications has come to play. The design of the frequency synthesizer would try to realized a 3~10 GHz frequency range in TSMC 0.18- $\mu$ m technology under 1.5-V supply voltage.

The frequency synthesizer is fulfilled according to IEEE 802.15.3a specification, which specifies an operating spectrum for MultiBand-UWB (MB-UWB) from 3 to 10 GHz and divides it into 5 band groups and 14 bands with spacing of 528MHz. The basis access is based on QPSK modulation and minimum input power level is -78.5 dBm.

## 1.2 Thesis Organization

In order to achieve low voltage, full bands problem, a new frequency synthesizer architecture is used. Chapter 2 describes the detailed specification of IEEE 802.15.3a, design considerations of the frequency synthesizer, then the basic theory of the PLL and the proposed 3~10 GHz frequency synthesizers are introduced. In Chapter 3 shows the circuit realizations and the simulation results of this design. In Chapter 4 shows the measurement results of this design. Finally, conclusion and future work are presented in chapter 5.





# Chapter 2

## A 1.5-V 3.1~10.6 GHz CMOS Frequency Synthesizer

So far, with the IEEE 802.15.3a PHY standardization activity staggering, an independent effort to draw the UWB regulation policy has been accelerated when various UWB interference tests have been performed to assess its potential harmful impacts on other victim receivers operating nearby UWB devices. For this purpose major groups have participated in the tests. This research has been conducted in order to provide specification on UWB, the underlying next generation wireless network technology, Business Model and to support UWB technology itself by extending its MAC and standard contribution. UWB Forum is expected to recommend a policy by collecting and analyzing the latest UWB technology trends, and thus promote the technical advances in domestic UWB industry. However the system design considerations, theoretical analysis, as well as architecture of the proposed Frequency Synthesizer are discussed and presented in chapter 2.

### 2.1 Multi-Band OFDM Physical Layer Proposal for IEEE

#### 802.15.3a

The purpose of this task group is to provide a specification for a low complexity, low cost, low-power consumption and high data rate wireless connectivity among devices within or entering the Personal Operating Space. The data rate must be high enough (greater than 55 Mbps) to satisfy a set of consumer multimedia industry needs for WPAN (Wireless Personal Area Networks) communications. There are two types of UWB technology: “DS-CDMA” and “OFDM-UWB”. Motorola and OFDM-UWB

by Multi-Band OFDM Alliance Members including 170 member companies support impulse-UWB, among others. Roughly it can be said that Impulse technology is better for locating, because of the better accuracy, and OFDM can rather be used for data communications because of better multiple access possibilities and better interference robustness. The transmitter of the proposed MB-H-UWB system is shown in Fig. 2.1, the transmitted simultaneously in 13 sub-bands to realize frequency diversity. Then, The FCC requires that UWB devices occupy more than 528 MHz of bandwidth in the 3.1~10.6-GHz band. The band center frequencies are given as:

$$\text{Band center frequency} = 2904 + 528 \times n_b \text{ (MHz)}, \quad n_b = 1, \dots, 14 \quad (2-1)$$

Where  $n_b$  represents band numbers. Band #1~Band #3 are used for Mode 1 application (mandatory mode), while Band #1~Band #3 and Band #6~Band #9 are used for Mode 2 application (optional mode). The remaining channels are reserved for future use. The UWB system provides a wireless PAN with data payload communication capabilities of 55, 80, 110, 160, 200, 320, and 480 Mb/s. It incorporates orthogonal frequency division multiplexing (OFDM) modulation using quadrature phase shift keying (QPSK). According to the spectrum mask in Fig. 2.2 and Fig. 2.3 the power spectral density (PSD) measured in 1-MHz bandwidth must not exceed the specified 41.25 dBm, which is low enough not to cause interference to other services operating under different rules, but sharing the same bandwidth. Cellular phones, for example, transmit up to 30 dBm, which is equivalent to 10 higher PSD than UWB transmitters (TX) are permitted. The next chapter focuses on the most important design blocks of the synthesizer.

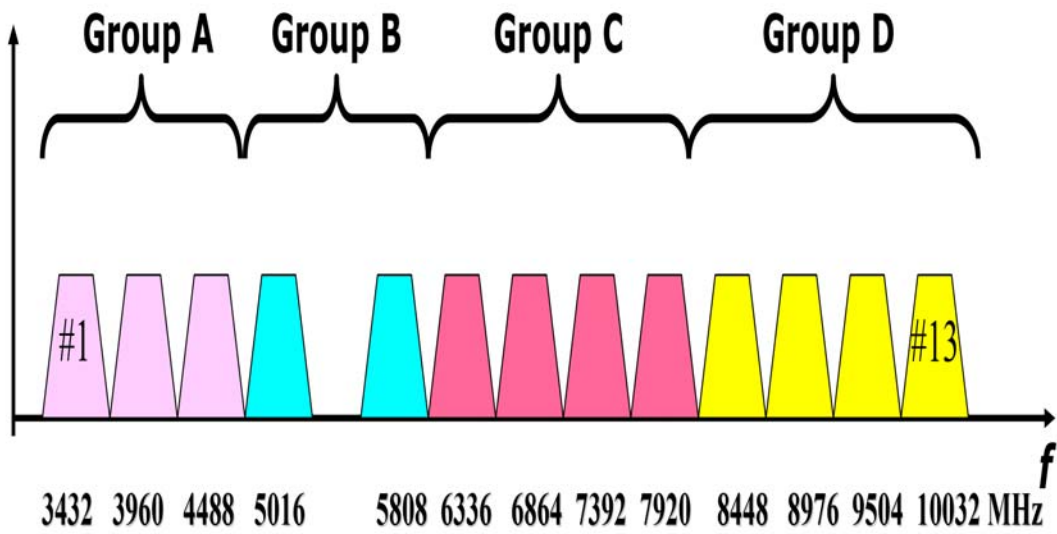


Fig. 2.1 Frequency plan of MB-OFDM UWB systems

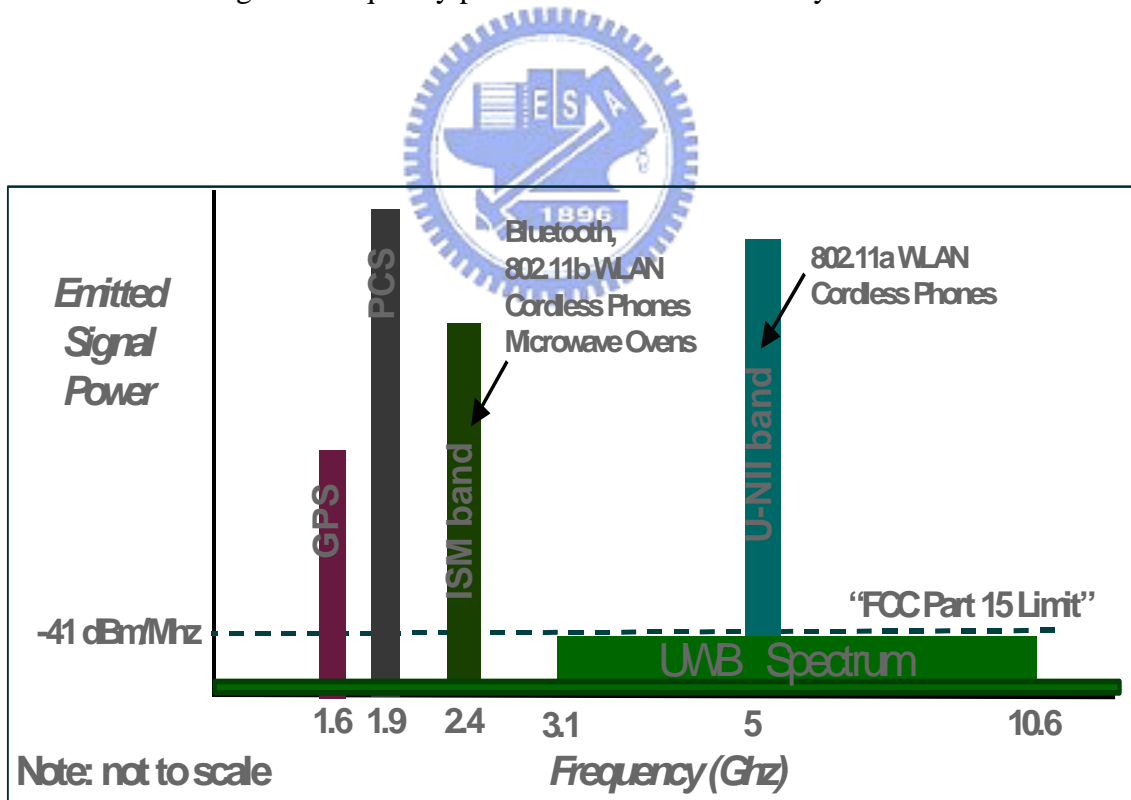


Fig. 2.2 Power spectrum for UWB systems

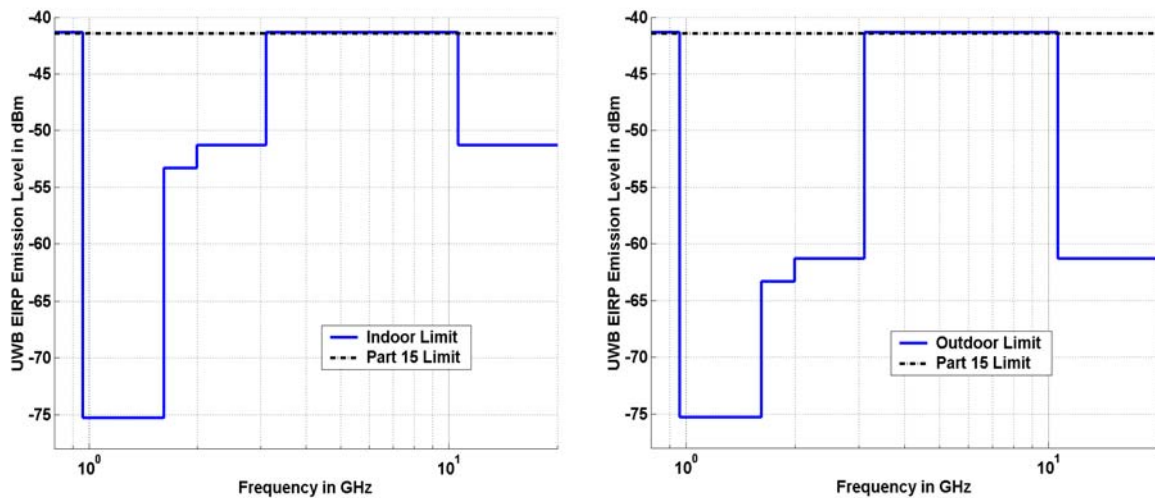


Fig. 2.3 UWB spectral masks for indoor and outdoor communication systems.

## 2.2 Role of Frequency Synthesizer and Operational Principle

In a MB-OFDM UWB system, the very wide frequency band is divided into third-teen groups. Then, frequency synthesizers designed at 10GHz such a high frequency are not popular yet, and a frequency synthesizer that can operates from 3.1GHz~10.6GHz needs not only more control signals than usual but also raising the circuit implementation complexity. Besides, a designing work of a frequency synthesizer that covers all band groups is undergoing. In this work, we will prove that the all band is possibly realizable by using the proposed PLL architecture. The block diagram of the proposed Frequency synthesizer is shown in Fig. 2.4, which consists of a PLL Basic (include VCO, VCO buffer, divider, PFD, CP, LF),  $I/Q$  quadrature single side-band (SSB) mixers, band-selector and poly-phase filter. The local oscillator (LO) is usually embedded in a phase-locked loop (PLL) so as to achieve the output

frequency signal (10.032GHz). The full spectrum is partitioned into four groups and every group except for the fourth one has 3 sub-bands. VCO generates the center frequency of 10032MHz in the fourth group and the reference clock realizes the band spacing frequency of 528MHz and the group spacing frequencies of 5016MHz, 3168MHz, 1584MHz and 1056MHz. The second mixer (Mixer2) by down-converting the group spacing frequencies realizes the 8 sub-bands (3432MHz, 3960MHz, 4488MHz, 5808MHz, 6336MHz, 6864MHz, 7392MHz, 7920MHz) in the first, second, and third groups are obtained. The fourth group is obtained from the first mixer (mixer1) by down-converting the VCO frequency with the group spacing frequency of 528MHz, 1056MHz and 1584MHz. This frequency generation scheme makes the first-order unwanted sidebands caused by mixing fall outside the 5.544GHz, 6.072GHz and 6.6GHz spectrum so that a lower spur level is achieved. To generate all the required quadrature signals for the SSB mixers, 2-stage poly-phase filters are adopted in this PLL. Then, second harmonics are obtained from the drains of the tail current sources in the NMOS differential buffers. Using harmonics saves chip area and power consumption. In PLL, the clock frequency of 1056MHz and 3168MHz must be generated from a divide-by-3 circuit. The divide-by-2 circuit generated 528MHz, 1056MHz and 5016MHz clock frequency. By using this poly-phase filter and a SSB mixer with switched-capacitor *LC* tanks, a sideband rejection over 30dB is achieved for every group.



# Chapter 3

## Design Of The Circuits

### 3.1 DESIGN CONSIDERATION

In the previous chapter, we proposed wideband PLL architecture to implement a high performance frequency synthesizer with noisy on-chip components. In this chapter, we also discussed the optimization of the loop bandwidth. We pointed out that the optimization of the loop bandwidth depends on the noise spectrum of each individual noise source. And we will discuss the low-noise design of each block in a PLL. The most important block is the integrated VCO. Even though the wideband loop can suppress the noise from the VCO, the suppression may not be enough because the integrated VCO is noisy, and the loop bandwidth cannot go arbitrarily high. A low-noise VCO is crucial in achieving a high performance frequency synthesizer. The phase/frequency detector, loop filter, frequency divider, poly-phase filter and SSB mixer are also important in realizing a high performance frequency synthesizer. The noise from the PFD and frequency divider is multiplied by the divider ratio at the output of the PLL. When a wideband PLL is used, the divider ratio may be reduced. However, because the loop bandwidth is very wide, noise is not suppressed until the frequency is above the loop bandwidth, which is usually above the frequency of interest. The noise from loop filter also has a peak gain depending on the VCO gain and loop bandwidth. Careful design of the loop filter is required to maintain good spectral purity at frequencies around the loop bandwidth. We will discuss how to design all functional blocks later. In this thesis, we focus on design a full bands frequency synthesizer circuit with perfect charge pump to suppress

spurious tone, and quadrature phase output for image-rejected mixer. And we will use SpectreRF to simulate the physical circuit of integer-N frequency synthesizer. A complete 3.1~10.6 GHz frequency synthesizer would be integrated with these building blocks and the simulation results are presented.

### 3.2 CIRCUIT REALIZATION

Fig. 3.1 shows the architecture of integer-N frequency synthesizer in this thesis. We will discuss each block in the next section.

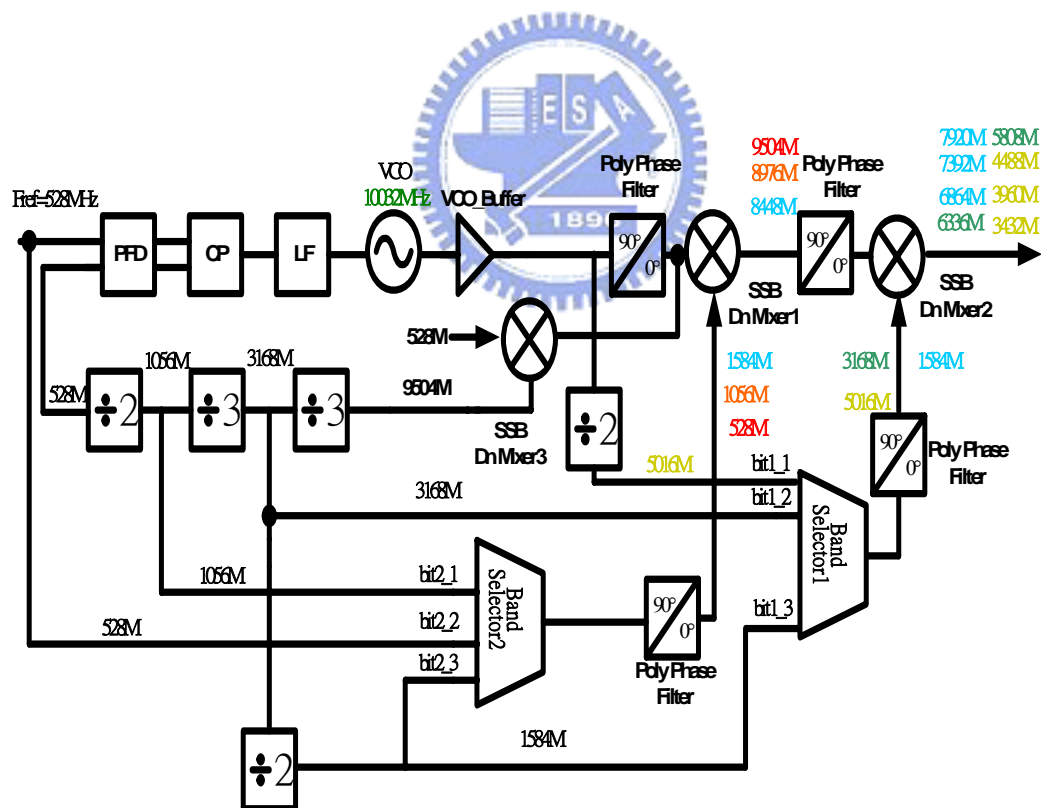


Fig. 3.1 The architecture of integer-N frequency synthesizer in this thesis



### 3.2.1 Low Phase Noise VCO

As we know, the LC VCO usually uses the cross couple pair as the negative resister. The VCO can roughly divide into two kinds. They are N-MOS (P-MOS) only cross-coupled VCO and complementary cross-coupled VCO. It has been mentioned in [2] that the complementary cross-coupled VCO has the better phase noise than the N-MOS or P-MOS only cross-coupled VCO.

#### 3.2.2.1 Trade-off between $K_{VCO}$ and tuning range

In this design, there is another trade-off become more critical. Because the VDD becomes lower, the output voltage range of the charge pump is suppressed. So, the  $K_{VCO}$  must be increase to maintain the same tuning range. But if the  $K_{VCO}$  is larger, the VCO is more sensitive to the noise that comes from the control voltage.

An ideal VCO's mathematic expression is

$$V_{out}(t) = V_o \cos(\int \omega_{out} dt + \phi_o) \quad (26)$$

And

$$\omega_{out} = \omega_o + K_{VCO} \int V_{cont} dt + \phi_o \quad (27)$$

In fact the  $V_{cont}$  is a function of time. Assume the  $V_{cont}$  has a small sinusoidal noise above its DC level.

$$V_{cont} = V_{dc} + V_m \cos \omega_m t \quad (28)$$

Put it into (27) and assume  $\frac{K_{VCO}}{\omega_m} \ll 1 rad$ , then the VCO's mathematic expression will be rewritten as follow.

$$V_{out}(t) \approx V_o \cos \omega_o t - \frac{K_{VCO} V_m V_o}{2\omega_m} [\cos(\omega_o - \omega_m)t - \cos(\omega_o + \omega_m)] \quad (29)$$

So,  $V_{out}(t)$  consists of three components, those tones at  $\omega_o \pm \omega_m$  are called spur.

When the spur appears in the local frequency of RF receiver, it will decade the SNR

after demodulation.

As it is seen in (29), the sidebands' amplitude relates to the value of  $K_{VCO}$ . So, if we can let the  $K_{VCO}$  as small as possible, the VCO output will have much smaller spur level.

### 3.2.2.2 Band-switching VCO

The VCO circuit is shown in Fig. 3.2 and Table 3.1 show VCO Datas. The operating frequency is decided by resonance frequency of the LC tank. But because the inductor and capacitor are not ideal, they have parasitic resistance. Without the negative resistance, the circuit will not oscillate, because of the left half plane poles. So we add the parallel negative resistance to insure the VCO can oscillate. In Fig. 3.2 the cross-coupled PMOS and NMOS are two negative resistances, spiral inductor shown in Fig. 3.3 realized the inductor and the equivalent model is shown in Fig. 3.4 and the two MOS varactors are used here to make oscillating frequency be tunable shown in Fig. 3.5.

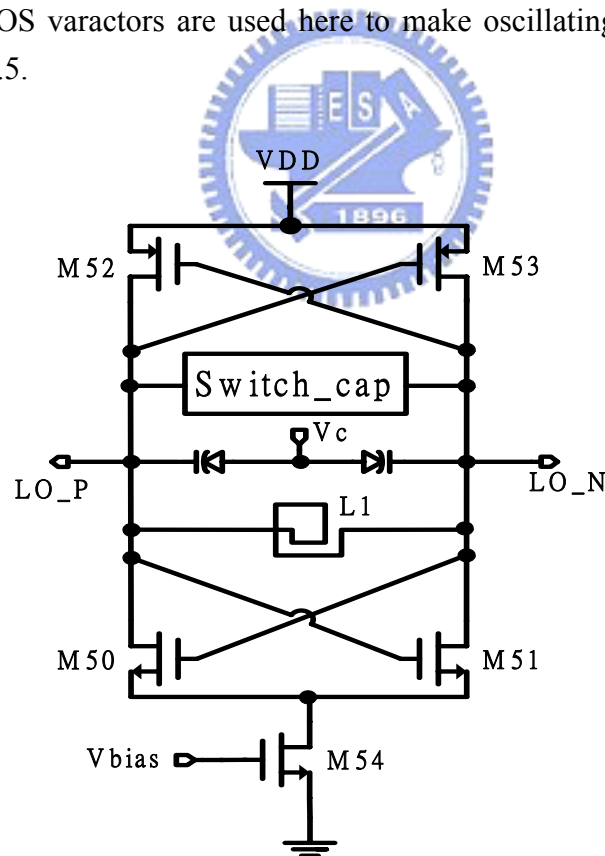


Fig. 3.2 VCO circuit

Table 3.1 Detail parameters of the VCO.

$M_{1-2}$	8 um / 0.18 um m=10
$M_{3-4}$	20 um / 0.18 um m=10
$M_5$	20 um / 0.18 um m=20
$L_1$	w=30 um r =65 um nr= 1
Varactor	l=0.5 um w=2.5 um br=10 g=1

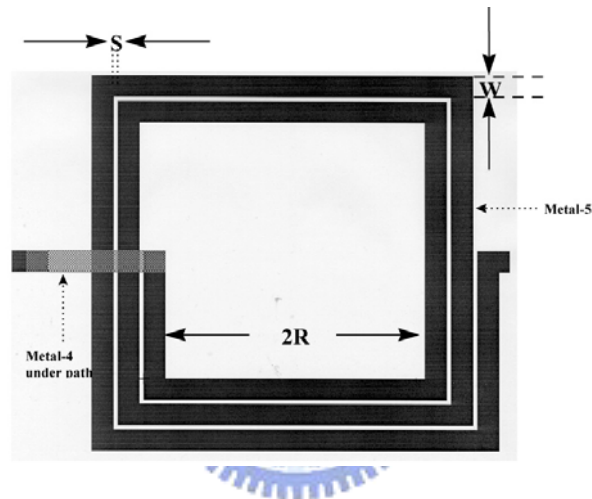


Fig. 3.3 Layout of spiral inductor

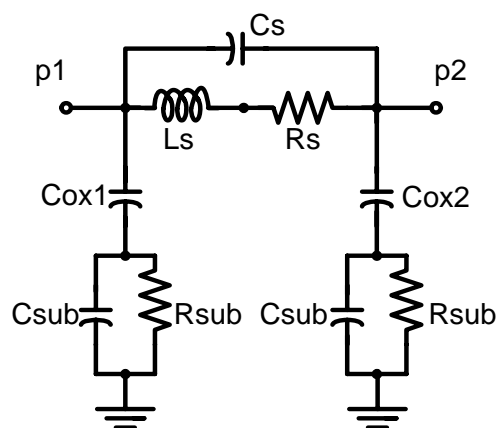


Fig. 3.4 Equivalent circuit of the spiral inductor

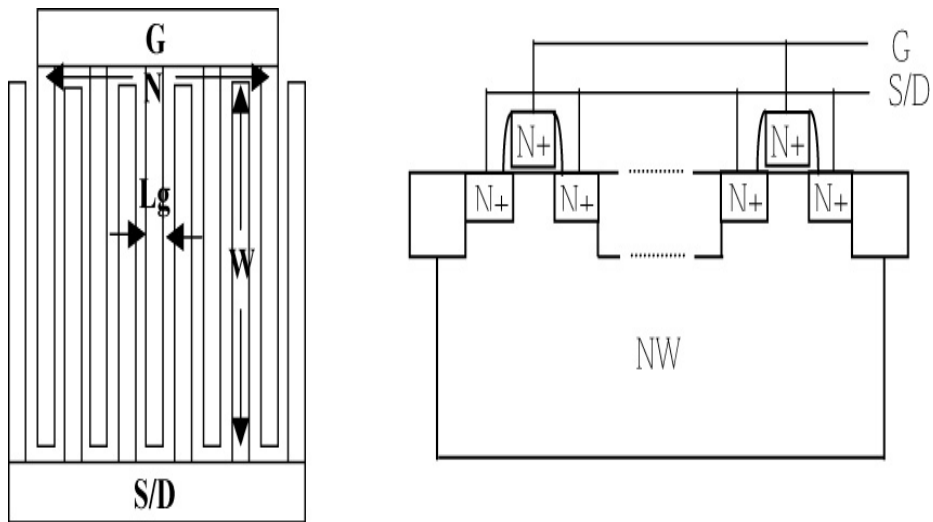


Fig. 3.5 MOS varactor layout structure

The ideal 4-bits VCO output frequency vs. the control voltage is shown in Fig. 3.6 the frequency range of VCO is split into four bands. By this way, the  $K_{VCO}$  can be lower to about 1/4 of the original  $K_{VCO}$ , and the spur level will be decade.

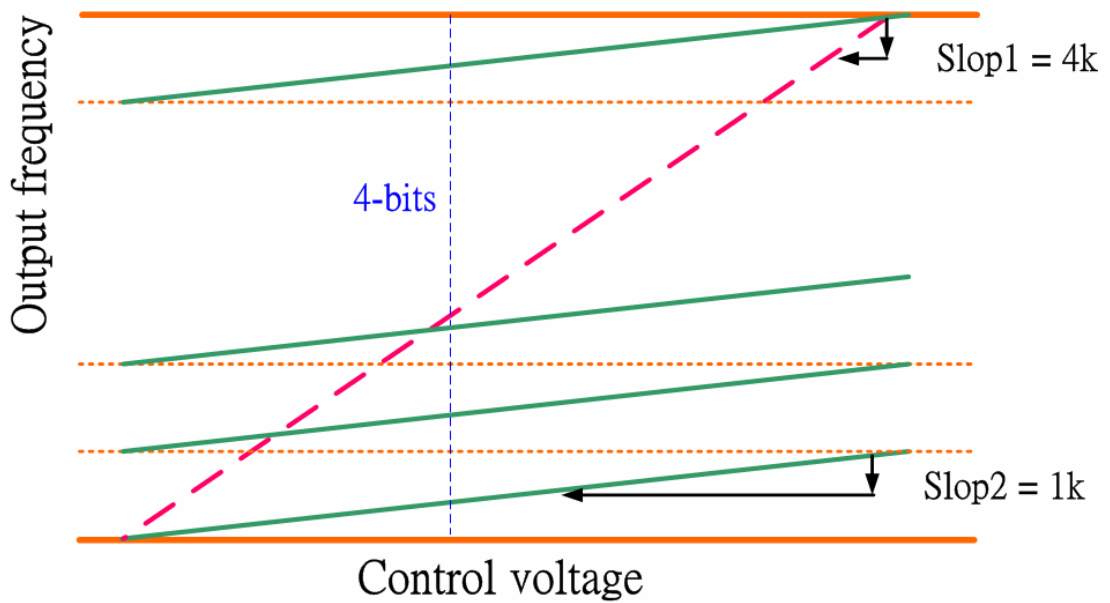


Fig. 3.6 The ideal 4-bits VCO output frequency v.s. control voltage.

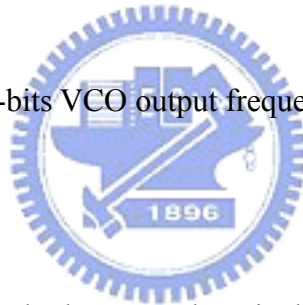


Fig.3.3 and Fig. 3.4 show the layout and equivalent model of the spiral inductor. We can see the inductor value is decided by the  $L_s$ , and  $R_s$  is the parasitic resistance that is canceled by the negative resistance. The one-port S-parameter simulation result is shown in Fig. 3.7. The simulated inductance of the inductor is decreased with increasing frequency and the inductance is about 284.664 pH and  $Q$  is above 16 when the frequency is larger than 10GHz.

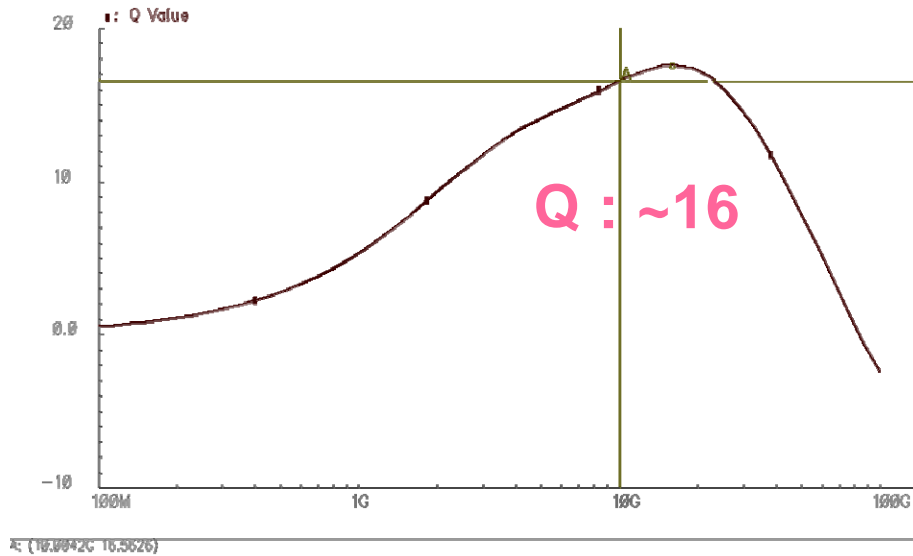


Fig. 3.7 Inductance and quality factor ( $Q$ ) of the proposed inductor.

As for the MOS varactors used in the LC-VCO, the accumulation type has been a popular choice for VCO varactors. The cross-section view of an n-type AMOS varactor is shown in Fig. 3.5. Adjusting the voltage across its G and D/S terminals alters the capacitance and the DN-well is used to reduce the parasitic capacitance and noise from substrate. While the connection of the varactor between its control voltage and VCO output nodes, LO\_P and LO\_N, is important: the gate terminal of the varactor is better connected to the output node of the VCO (LO\_P~LO\_N), for which the output signal quality would be less degraded by the substrate noise and the frequency tuning range could sustain for less parasitic capacitance seen there. With the aid of these features mentioned above, a VCO with wide frequency tuning range can be realized. The simulated C-V characteristic at 10 GHz is shown in Fig. 3.8 and the varactor has a  $C_{\max}/C_{\min}$  ratio of about 4.2.

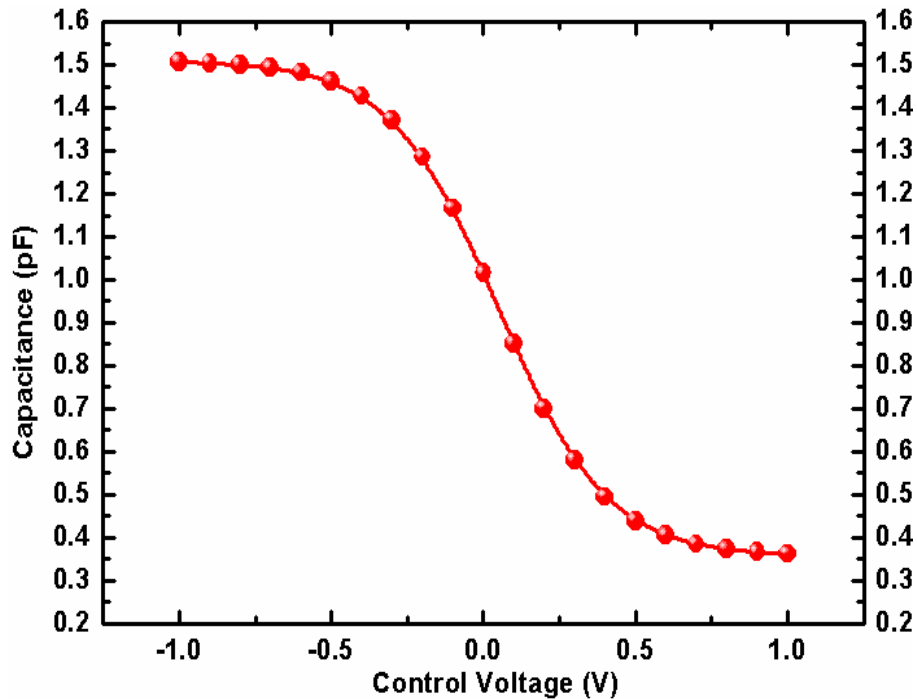


Fig. 3.8 Varactor C-V curve

### 3.2.2 Frequency Divider

The most delicate piece of the divider is the first divide-by-two stage and divide-by-three stage and challenging compare to other building blocks in the frequency synthesizer. First, the divider operates at the highest frequency and it must still functions properly under the process and temperature variation. Furthermore, it must generate quadrature outputs. At last, in our architecture, the output load of the first divide-by-2 circuit contains not only the next stage divider and wiring capacitance but also two buffers for Band-selectors. This means the load capacitance will be very large, nearly 200fF in our design. The divide-by-two stage and

divide-by-three stage separately work at 5.016GHz and 3.168GHz. Given the high frequency and the necessity to have a differential structure, very few approaches work for us. First, we simulated many different structures of dividers. To avoid polluting the substrate, the differential structure has been chosen over the single-ended one although the latter possesses all the other advantages. The need of a differential clock is not a problem since we already have a differential signal coming out of the VCO. The differential dividers are realized with current-mode logic (CML) flip-flops. Fig. 3.9 shows a typical CML flip-flop. It consists of a master and an identical slave latch that are clocked on opposite clock phases. In the Fig. 3.10 The latch consists of resistance loads (R1-R2), gain stage (M91-M92), positive-feedback transistors (M93-M94) for latching, clocked differential pair (M95-M96) and current source (M97). Transistor M97 provides the latch with a constant current and minimizes the noise injection into the power supply and ground lines. This structure does not provide full swing at its output. Due to the number of stacked transistors, the NMOS tend to suffer of the body effect and that degrades the speed of the structure since the devices are in the triode region and thus their resistance is larger. In order to have the FF work at more than 5.016GHz, we had to remove the current source transistor (M97). This new FF works at a higher speed but consumes also more current. It is also more prone to process variations since the swing is only dictated by the transistor sizes. The right size ratio has to be found between the NMOS and the PMOS devices to balance the rise and fall times as much as possible. For the CML structure, the use of doughnut may help at certain nodes of the structure but it will increase the source capacitance, which might be a problem with the stacked structure. Due to the timing of divide-by-3 is critical, the cells of AND0 and AND1 as shown in Fig. 3.10 has to integrate into cells DFF\_AN0 and DFF\_AN1 to reduce the propagating delay. In a typical PLL type frequency synthesizer, frequency divider is usually used to select the desired lock



frequency. The logic block diagram of the divider is shown in Fig. 3.9 then the upper block diagram is a divide-by-2 circuit with frequency up to 5016MHz. The below block diagram is a divide-by-3 circuit with frequency up to 3168MHz. The first divide-by-two consumes about 16.37mA; the amplitudes (peak) are 0.76V, then the first divide-by-three circuit consumes about 7.077mA; the amplitudes (peak) are 1.27V.

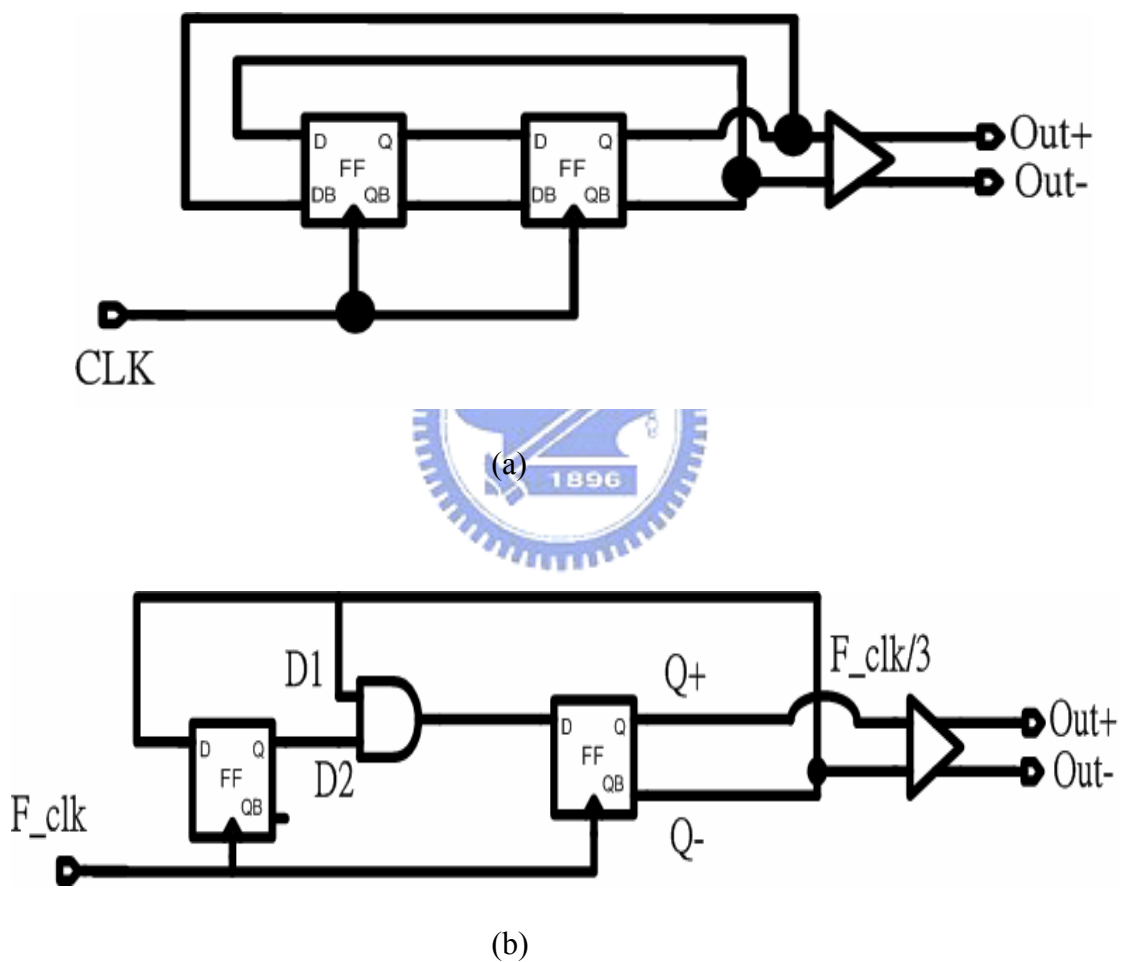
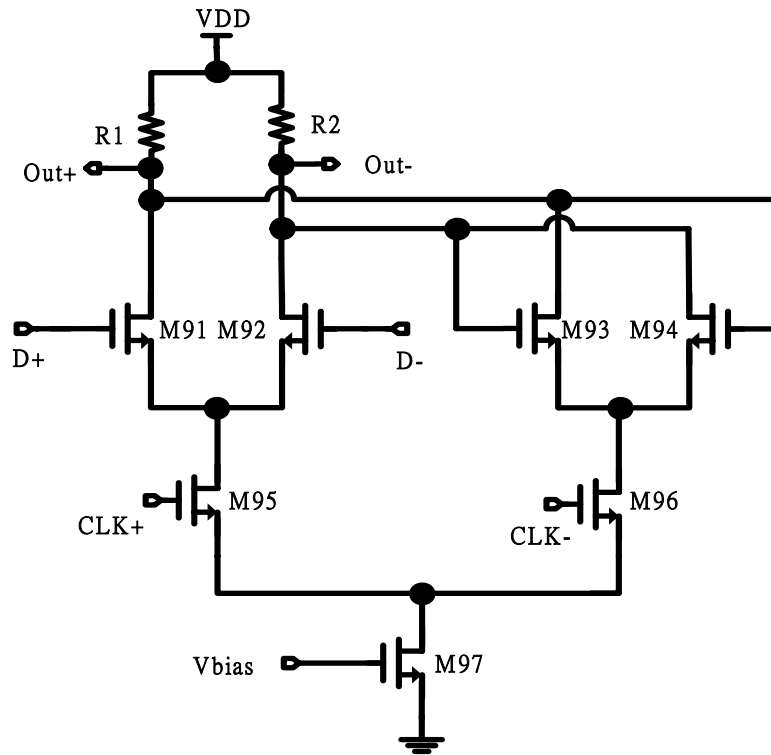
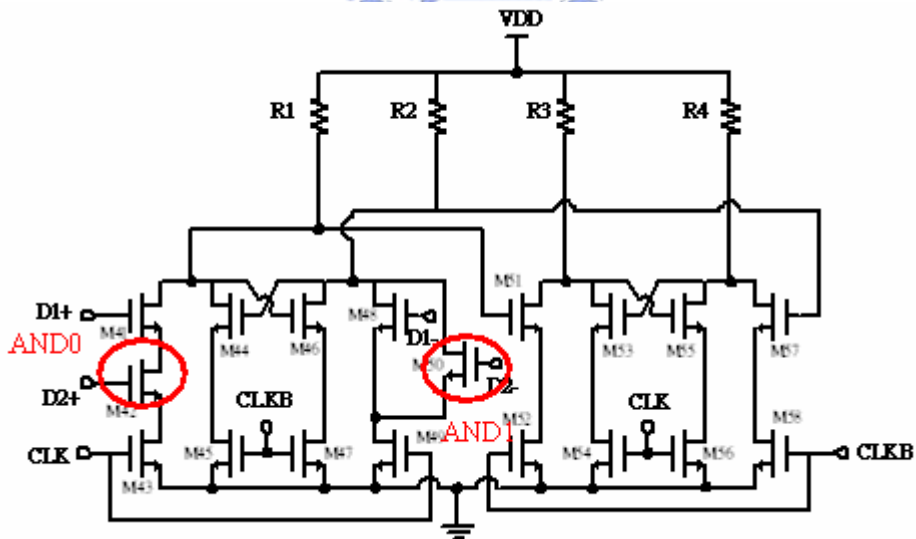


Fig. 3.9 (a) Logic block diagram of the Divider\_by\_two\_stage (b) Divider\_by\_three\_stage



(a)

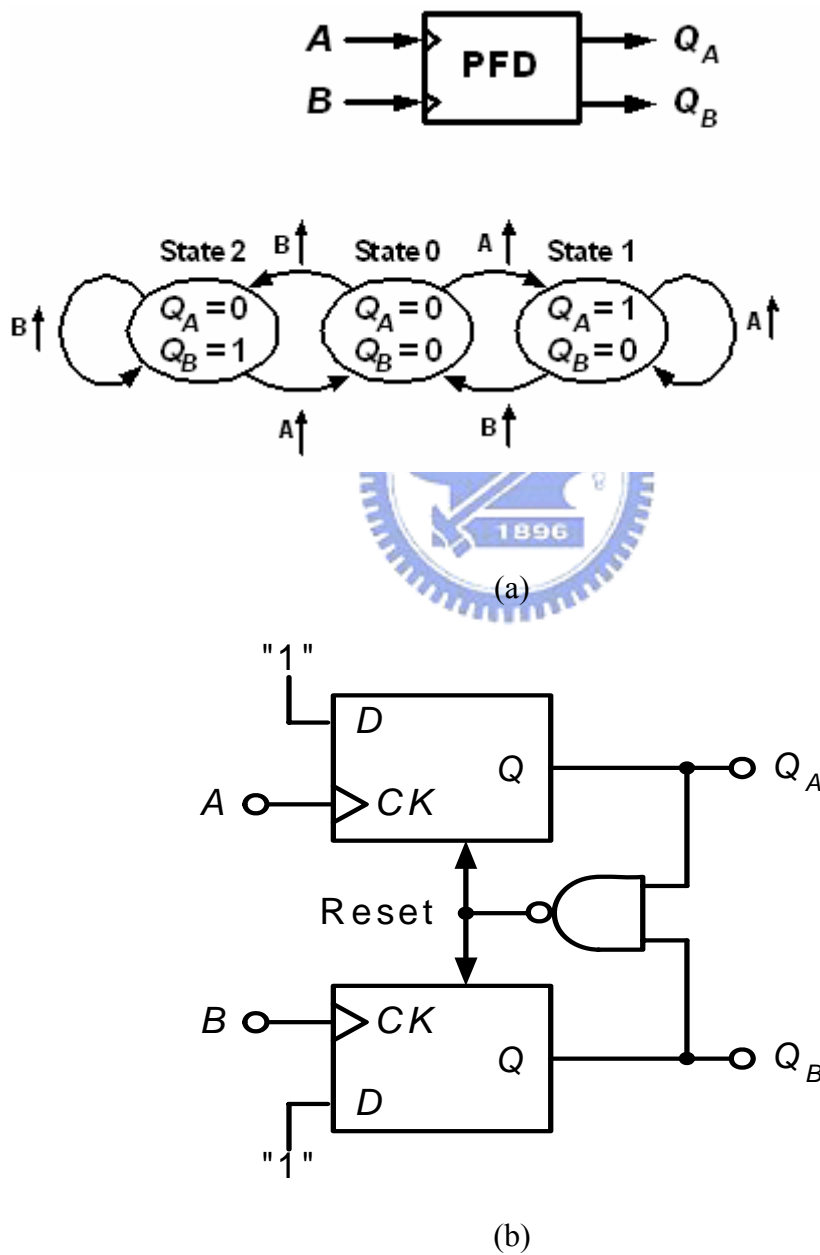


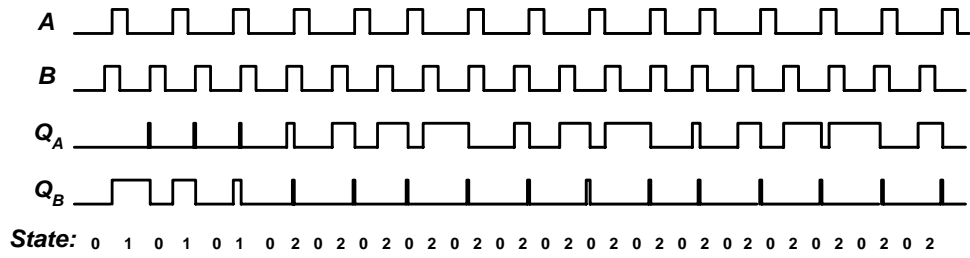
(b)

Fig. 3.10 (a) D Flip-Flop Stage (b) D Flip-Flop Stage with builds in AND gate

### 3.2.3 Phase Frequency Detector

A conventional three-state phase detector has been used in this design. The three-state phase detector is widely because it is simple, has a linear range of  $\pm 2\pi$  radians, and can act as phase and frequency detector. A state diagram for the circuit is shown in Fig. 3.11 (a). Base on the state diagram it can be implement as Fig. 3.11 (b).





(c)

Fig. 3.11 (a) PFD block diagram (b) PFD state diagram (c) PFD timing diagram

The timing diagram of three-state PD has been illustrated in Fig. 3.11 (c). Let's combine PD and charge pump, Fig. 3.12, and deriving its transfer curve as shown in Fig. 3.13. The action of a three-state PD as a frequency detector is now clear.

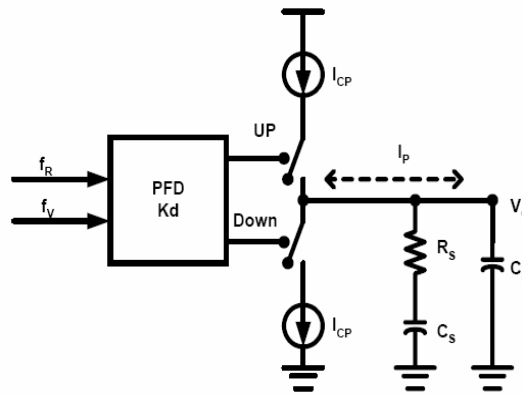


Fig. 3.12 Block diagram of charge pump and PFD

For  $f_V > f_R$ ,  $\theta e$  decreases with time, and  $I_p$  remains negative. For  $f_V < f_R$ ,  $\theta e$  increase with time, and  $I_p$  remains positive. This is a great aid in acquiring lock when the two frequencies are initially different [20].

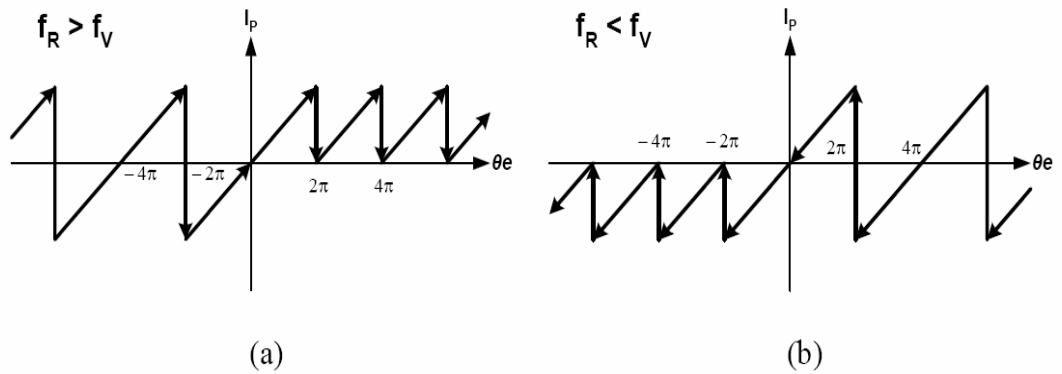


Fig. 3.13 PFD transfer curve when (a)  $f_R > f_V$  (b)  $f_R < f_V$

In Fig. 3.11 (b), static logic blocks such as D-type flip-flop (DFF's) and NAND gates are used. Note that the D-input of the two DFF's are always at high logic-level. Hence simplified static DFF's that hides the D-input can be found constructed by only four NOR gates or four NAND gates [21]. Fig. 3.14 is the PFD circuit in our design.

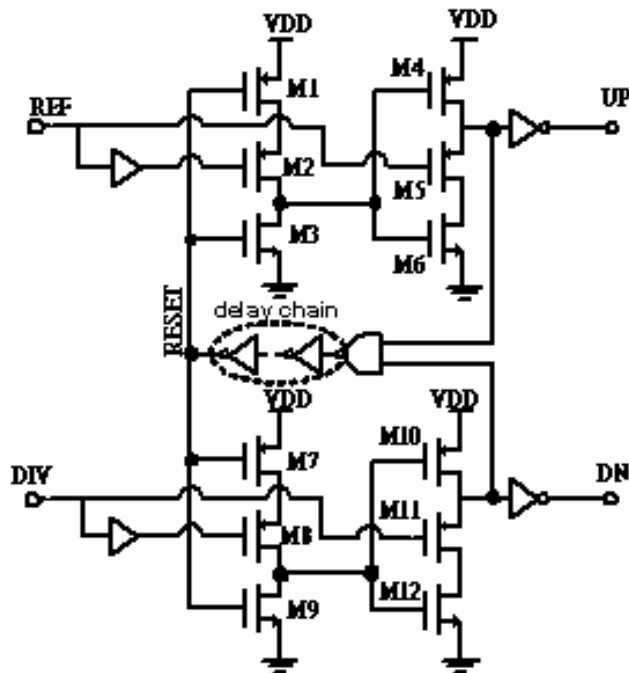


Fig. 3.14 Phase frequency detector

When this type of phase detector incorporated with charge pump circuit, it has a drawback that exist a dead zone, as shown in Fig. 3.15. If the reset signal is not delayed sufficiently. That will cause the output of charge pump dies not change for small phase error thus the dead zone translates to jitter in PLL and must be voided. In Fig. 3.14, the delay chain is increased delay of reset signal for eliminating dead zone.

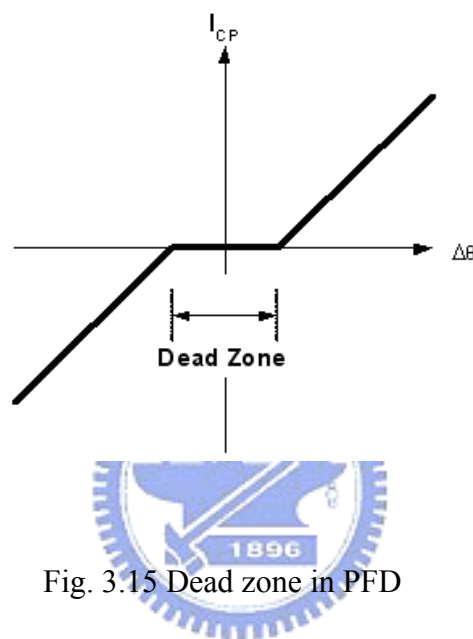


Fig. 3.15 Dead zone in PFD

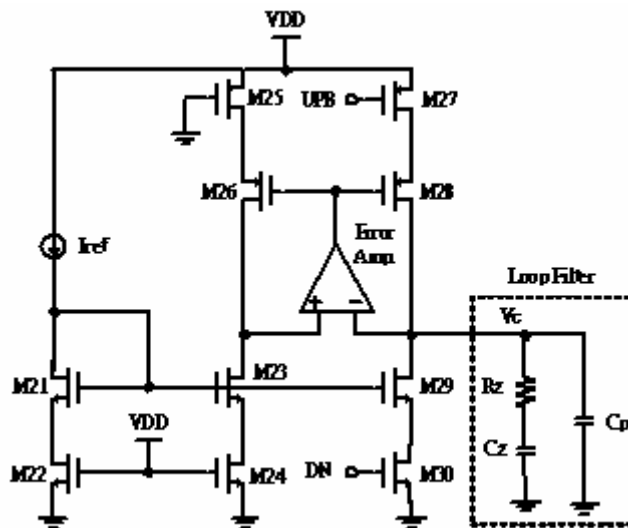
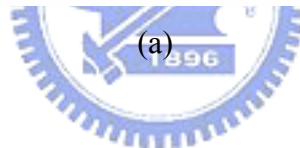
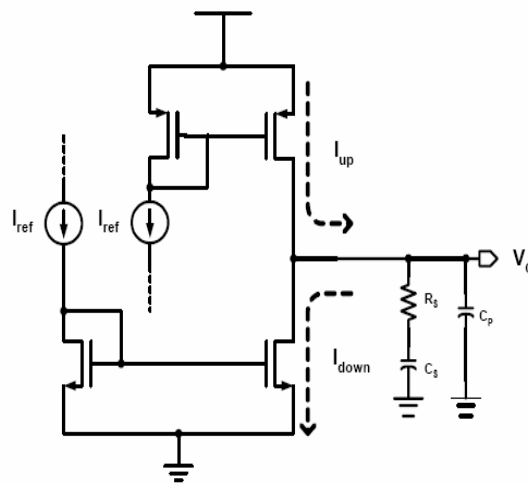
### 3.2.4 Perfect Current-Matched Charge Pump

In this design the current-steering charge pump is used. But the current-steering charge pump still suffers from the current mismatch issue. So, the current-match technique is used in this design.

#### 3.2.1.1 Current-match charge pump

Because of the effect of channel length modulation, in the conventional current-steering charge pump circuit  $I_{up}$  and  $I_{down}$  cannot mach at whole  $V_c$  voltage, even if M10 and M11 are sizing as the ratio of their mobility ratio and same over-drive voltage. At every reference clock edges, the  $I_{up}$  and  $I_{down}$  will both turn on

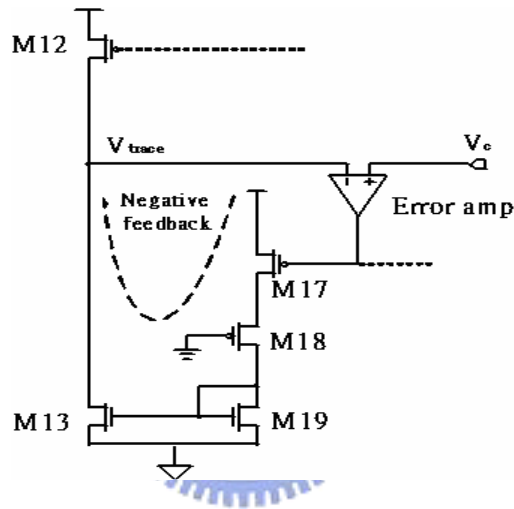
for a very short time to cancel the dead zone effect of PFD. At this moment, if the  $I_{up}$  and  $I_{down}$  are not match each other, the mismatch current will become noise to next stage (LPF). This noise will increase the spur level of VCO output spectrum. Fig. 3.16 shows the current-match charge pump circuit. The current-match charge pump has a function, which can make the up and down currents match each other.



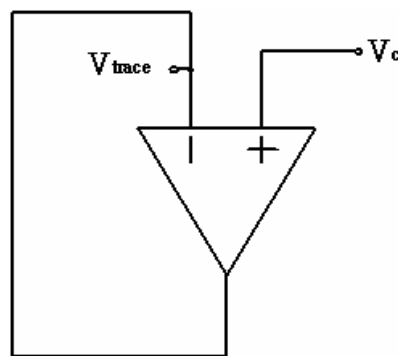
(b)

Fig. 3.16 (a) Sinking/Source Current in CP (b) Current-Switching CP Circuit

Fig. 3.17 shows the half circuit of Fig. 3.16 and it can be equivalent to unit gain buffer. We can view the error-amp as the first stage, the M17 is the second stage amplify and the M18 in triode region series with M19 in diode connecting. The third stage is common source amplify M13 with the output load  $r_{O12}/r_{O13}$ . Those stages amplify the difference of  $V_c$  and  $V_{trace}$ . And the negative feed back to  $V_{trace}$ . We can view these three stages as an op-amp as Fig. 3.17(b) shows. This is a voltage follow buffer and it means the  $V_{trace}$  will tracing  $V_c$  when  $V_c$  varies its value. So, we can calculate the gain of op-amp in Fig. 3.17(b) as follow.



(a)



(b)

Fig. 3.17 (a)The feedback loop of the current-match charge pump shows in fig 3-1,

(b)The equivalent circuit of the circuit in (a)



Assume the gain of the first stage error-amp is  $A_{error}$ . Then the next stage a PMOS common source stage, and the gain is as follow

$$A_2 = g_{m17} \cdot \left( R_{18} + \frac{1}{g_{m19}} \right) \cdot \frac{\frac{1}{g_{m19}}}{R_{18} + \frac{1}{g_{m19}}} \quad (20)$$

$$= \frac{g_{m17}}{g_{m19}}$$

Where  $R_{18}$  is the equivalent resistor of M18 in triode region and  $1/g_{m19}$  is the equivalent resistor of M19 in diode connecting.

The third stage is also a common source stage and its gain is as follow

$$A_3 = g_{m13} \cdot (r_{o12} // r_{o13}) \quad (21)$$

The overall gain of the feedback loop is

$$A_{open} = A_{error} \cdot A_2 \cdot A_3 \quad (22)$$

$$= A_{error} \cdot \frac{g_{m17} \cdot g_{m13}}{g_{m19}} \cdot (r_{o12} // r_{o13})$$

Then assume the difference between  $V_c$  and  $V_{trace}$  is  $V_{error}$

$$V_{error} = (V_c - V_{trace}) = \frac{1}{1 + A_{open}} \cdot \left( V_c - \frac{V_{DD}}{2} \right) \quad (23)$$

And the channel-length modulation coefficient is  $\lambda \cong 0.2$ . So, if we assume the maximum  $(V_c - 1/2V_{DD})$  is 0.3V. According to the square law of MOS  $I_D = 1/2K W/L \cdot V_{ov} \cdot (1 + \lambda V_{DS})$ , we can calculate the maximum mismatch current by follow equation

$$\text{The mismatch current} \cong 2 \times \lambda \times V_{error} \times I_{up/down} = \frac{0.12}{1 + A_{open}} \cdot I_{up/down} \quad (24)$$

So, if the  $A_{open}$  is large than 22.27 dB, the current mismatch will less than 1%.

In simulation, when  $V_c$  is equal to 0.8 V and  $A_{open}$  is 30 dB, the current mismatch is about 1.06%.

### 3.2.1.2 The Input rail-to-rail Op-amp Used in the Current-match charge pump

The error amplifier is shown in Fig. 3.18. To make sure the MOS away from weak inversion, the gate drive voltage,  $V_{gs}-V_t$ , always to be 150mV~250mV, we can obtain gate drive voltage by SpectreRF simulation. If assume gate drive voltage is 200mV and VDD is 1.5V, thus Fig. 3.18 will operate normally at  $V_c=0.2V\sim 1.3V$ . The operated voltage of  $V_c$  means that the input voltage of error amplifier is among 0.2V~1.3V, close to ground and supply voltage, thus the error amplifier must have the ability for rail-to-rail input operating.

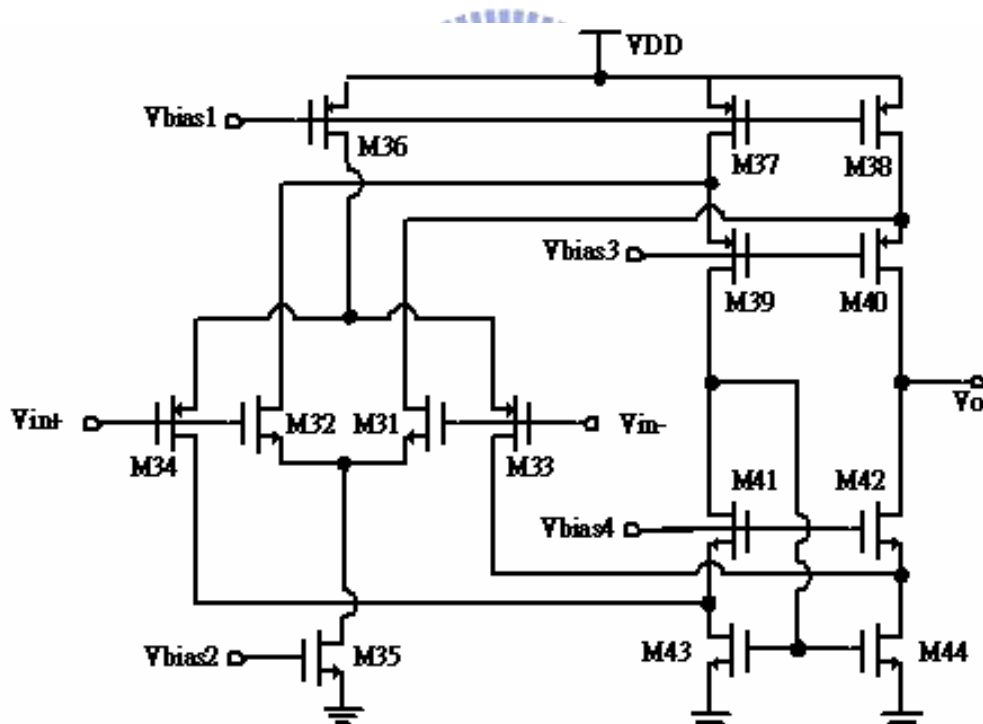


Fig. 3.18 Operation amplifier for rail to rail input

### 3.2.5 Loop Filter

The loop filter is an important block in a synthesizer because it determines most of the system specifications such as phase noise performance, spur level and locking time. It is a low pass filter that will convert a discrete-time current signal to a continuous dc-like signal to control the voltage-controlled oscillator. Besides, it filters out all high frequency noise in the close-loop circuit. Conventional 2<sup>nd</sup>-order loop filter is shown in Fig. 3.19(a) by making circuit analysis; we can get its transfer function:

$$\frac{Vo(s)}{Icp(s)} = Z(s) = \frac{1}{(C1+C2)} \frac{1+sRCz}{s \cdot [1+sR(\frac{C1 \cdot C2}{C1+C2})]} = \frac{1}{C1+C2} \frac{1+s\tau_z}{s \cdot [1+s\tau_p]} \quad (2-1)$$

Where  $\tau_z = RCz, \tau_p = R(\frac{C1 \cdot C2}{C1+C2})$

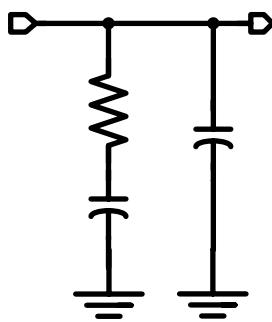


Fig. 3.19(a) 2<sup>nd</sup>-order

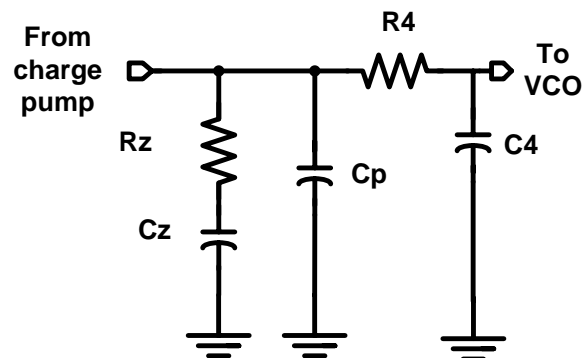
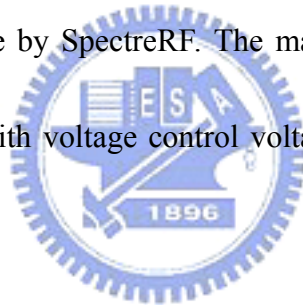


Fig. 3.19(b) 3<sup>rd</sup>-order

As we can see, 2<sup>nd</sup>-order loop filter has two poles and one zero. If we incorporate it into a synthesizer, it forms a 3<sup>rd</sup>-order close-loop system. For the purpose of getting better noise performance, one may adopt a 3<sup>rd</sup>-order loop filter in Fig. 3.19(b). However, it is a little bit hard, complicated to get the value of the components and the additional resistance, R4, will induce extra thermal noise. Most important of all, we are also limited to design the loop filter with the small area constraint for on-chip loop filter in addition to other specifications.

To verify the loop filter and decide the close-loop characteristics of the synthesizer, behavioral simulation is made by SpectreRF. The macro model is in Fig. 3.20. The circuit blocks are idealized with voltage control voltage sources and voltage control current sources.



Given parameters, gain of the voltage-controlled oscillator,  $K_{vco}=160\text{MHz/V}$ . Charge pump current,  $I_{cp}=100\mu\text{A}$ . Counts of the divider,  $N=18$ .

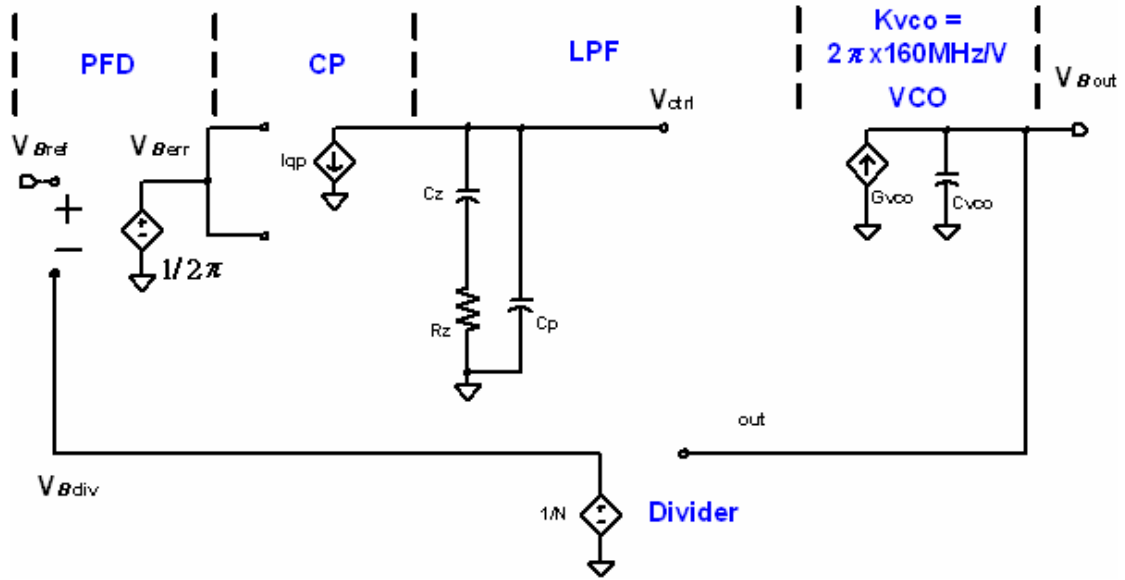


Fig. 3.20 Behavioral simulation setup

Then we can get  $C_z = 3\text{pF}$ ,  $R_z = 43.15\text{k}\Omega$ ,  $C_p = 0.156\text{pF}$ , Phase Margin =  $65^\circ$ . The simulation result is in Fig. 21.

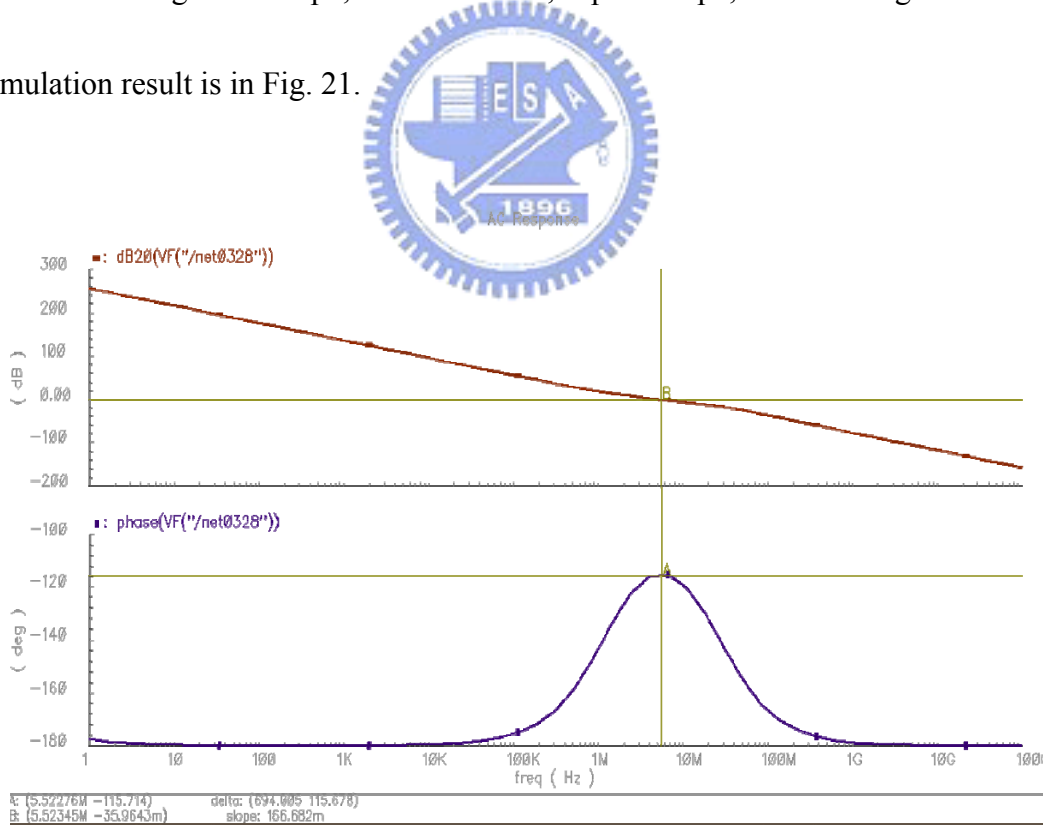


Fig. 3.21 Behavioral simulated results crossover frequency = 5.5MHz Phase Margin =  $65^\circ$

### 3.2.6 Single Sideband Mixer

The SSB Mixer (image-reject Mixer) in this architecture was designed, the center operating frequency is chosen at 3432 ~9504MHz. The mixer translates the RF signal at the frequency band from 528 MHz-5.016 GHz to the base band signal. Among the proposed active mixers, the Gilbert-cell mixer has been widely used so far, and the double-balanced mixer topology has been preferred since it can suppress (LO) leakage signals at the output. Fig. 3.22 is the conventional double-balanced CMOS Gilbert Cell mixer. The Tran conductance stage consists of M115 and M116, and current-commutating stage comprises M11~M114.  $R_1 \sim R_2$  is the load resistor. M115 and M116 always operate in the saturation Region. LO power must be carefully chosen such that M111-M114 periodically turn on. Assume LO is approximated by a sinusoidal wave and  $gm_1 = gm_2 = gm$ , then the voltage gain ( $A_v$ ) of the Gilbert Cell mixer can be determined by the following expression:

Voltage gain equation:

$$A_v \approx \frac{2}{\pi} \cdot g_m \cdot R_L \cdot \left( 1 - \frac{\sqrt{2}(V_{gs} - V_t)_{sw}}{\pi V_{Lo}} \right) \quad (5)$$

Where  $gm$  is the transconductance,  $R_L$  is the load resistor.

From (5), conversion gain is increased with higher load resistors, but the supply voltage is kept constant. The simultaneous achievement on these requirements is a very challenging task in the mixer design. Especially, the high linearity requirement is the most difficult one to achieve since the mixer is required to operate at a very low supply voltage and low power consumption. Higher gain and better linearity can be achieved by increasing the bias current through the Tranconductance stage. In overall mixer design, higher gain, higher linearity, lower noise and low power consumption

are required. However, these parameters are not easy to achieve simultaneously. Higher gain and better linearity can be achieved by increasing the drive current through the transconductance stage, but power consumption will be increased. Furthermore the larger current through the switching quads causes voltage headroom problems especially if resistive loads are used. The larger amount of current through the switching quads mandates the larger LO drive voltage, which is troublesome in the CMOS technology, since it is not easy to get the large enough voltage swing at high LO frequency. Fig. 3.23 shows the block diagram of a single-sideband mixer, which consists of two-stage passive poly-phase filter, two DSB mixers, and an output combiner. In the ideal case, the SSB mixer only generates either upper ( $W_1+W_2$ ) or lower ( $W_1-W_2$ ) sideband component. However, both sidebands are present due to non-quadrature phase (non-zero  $\theta_1$ , and  $\theta_2$ ) or amplitude imbalance (between  $A_1$  and  $B_1$ ,  $A_2$  and  $B_2$ ) introduced by the 90-degree Phase Shifters to eliminate such a design issue. A two-stage passive poly-phase filter is shown in Fig. 3.25. We may employ this type of phase shifters to generate amplitude-balanced signals and then subsequently correct the phase error prior to the output combining operation. Note that it is more difficult to correct errors in amplitude domain than in phase domain, since mixers introduce amplitude nonlinearity (from LO port) but preserve linear input-output relationship for phase. If difference combining is performed at the SSB mixer output as shown in Fig. 3.24. It can be shown through simple trigonometric identities that the lower sideband (difference frequency) is rejected provided that the two. Two-stage passive poly-phase filter produce balanced amplitudes ( $A_1=B_1$  and  $A_2=B_2$ ) and identical phase shifts, i.e.,  $\theta_1=\theta_2$ . As a result, an absolute accuracy of 90-degree phase is not needed for each phase shifter, as long as they produce identical phase shift. After passing through the 90-degree delay circuit, the desired signals in the I and Q channels are in phase but the image signals are out

of phase. A combiner, shown in Fig. 3.24, adds the signals from the I and Q channels together to cancel the image signal. M105 and M108 are added to control the bias current to adjust the amplitude balance, and the control signal comes from the off-chip control circuit.

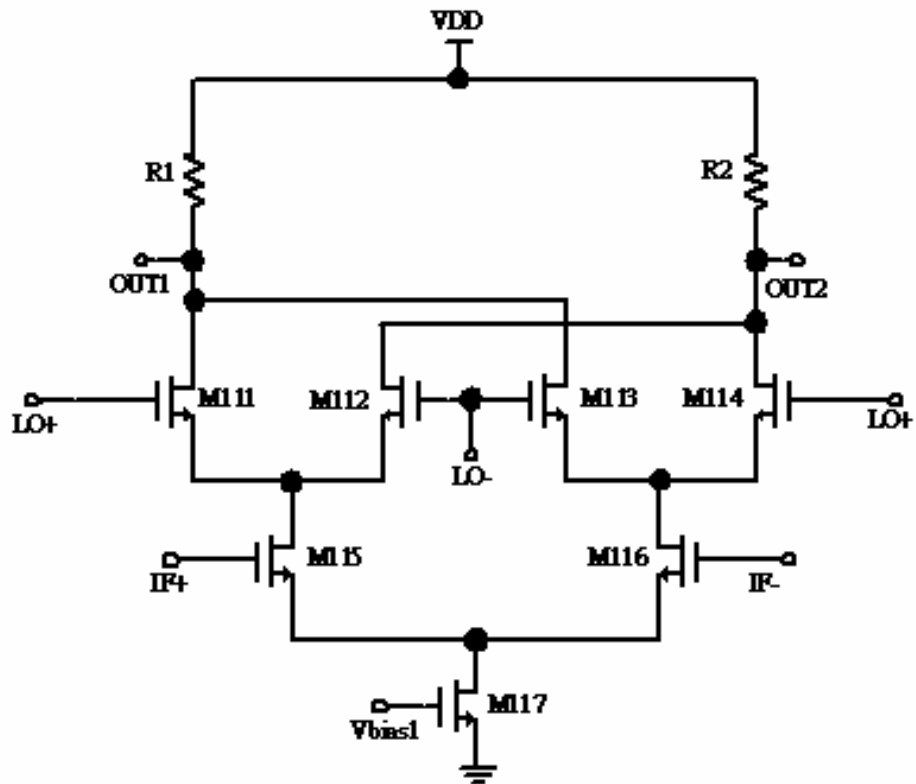


Fig. 3.22 Double-balanced Gilbert-type mixer topology



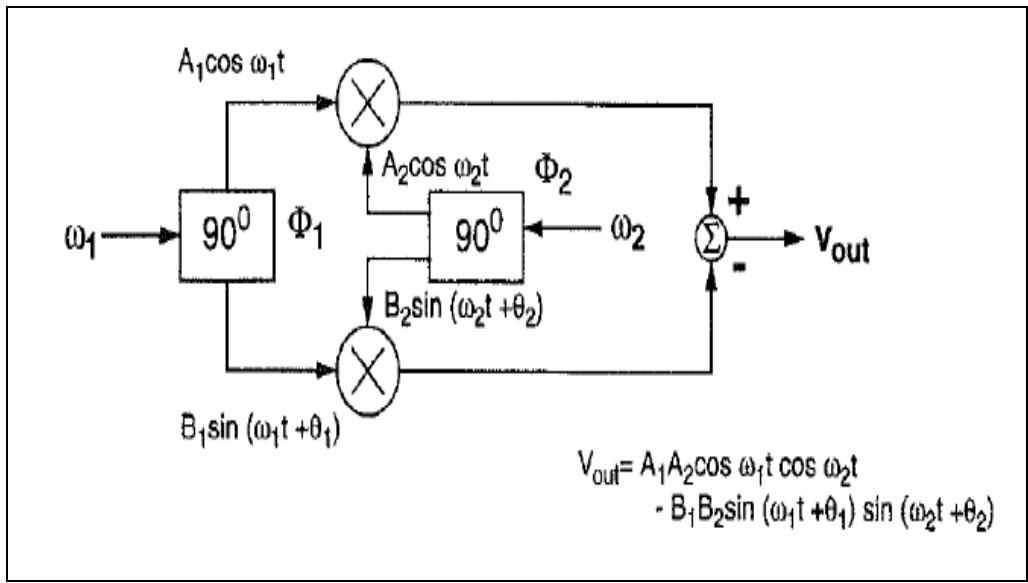


Fig. 3.23 Single-sideband mixer topology

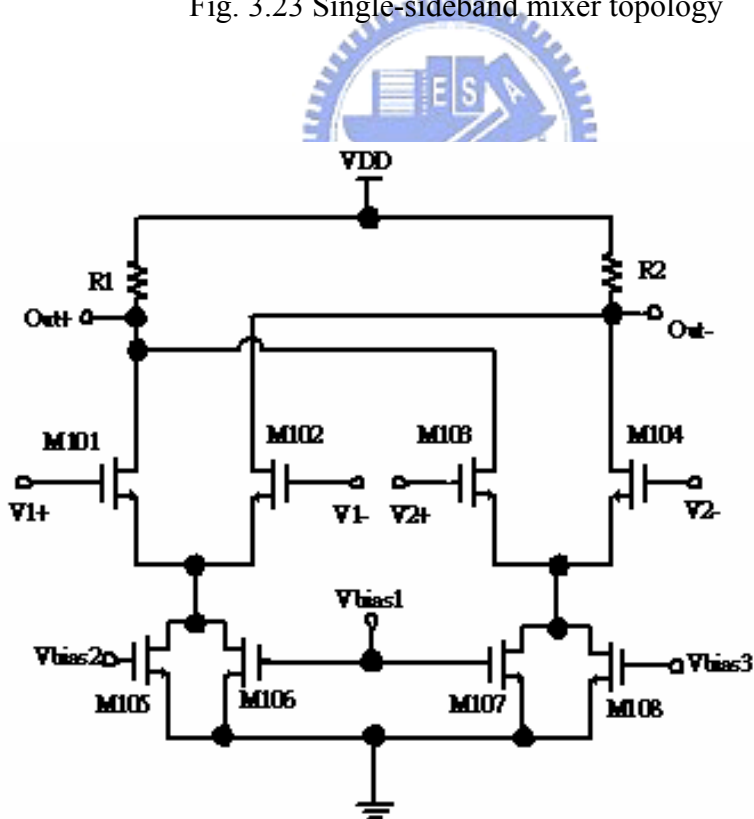


Fig. 3.24 Schematic of the combiner

### 3.2.7 Poly-Phase Filter

A poly-phase filter offers an accurate phase shift and amplitude balance in a fairly wide band. The overall image-rejection ratio (IRR) is strongly affected by the characteristics of this block. Therefore, Careful designing is essential. In this design, using one-stage poly-phase filter results in large RC variation. However, using three-stage poly-phase filter results in small output signals. Therefore, a two-stage poly-phase filter is used in this design to achieve moderate RC variation and level of output signals. To reduce the RC variation, MIM-capacitors and poly resistors are used in this design. Moreover, the interlocking method is adopted in the layout and some dummy devices are placed on two edges of the poly-phase filter to reduce the RC variation further. Finally, two buffers are inserts before and after the filter to maintain the signals. A two-stage poly-phase filter is depicted in Fig. 3.25. The stages are inherently suitable for cascading. Along with the number of stages the image-rejection ratio offered by the filter increases but at the same time the signal attenuation and the physical die size are increased, too. If the center frequencies at each stage are equal, the IRR value is high but only at a limited band. If the center frequencies are selected properly for each stage, larger bandwidth with sufficient IRR values is achieved. In our case an 10.032GHz bandwidth is required. For us, two stages were required for achieving enough image rejection. The RC values of the two-stage poly-phase filter is depicted in Table 3.2 The two-stage RC poly-phase filter rejects the image of the first mixer by about 35 dB. For this image rejection, the phase accuracy of the quadrature LO should almost be commensurate. The outermost peaks (center frequencies) are shifted further away from the center of the band for ensuring that despite the process spread a high IRR value is always achieved. Also, a proper selection of the resistance and capacitance values is required for achieving a

high immunity to process spread. Finally, to avoid any confusion, it is worth emphasizing that a poly-phase filter does not separate the signal and image. Instead, in the other output port the signal appears in a 90-degree phase shift. This port is terminated with appropriate impedance in our designs. The turn-on resistors of MOS switches have been considered in the post-simulation, so R used in the simulation includes these resistors.

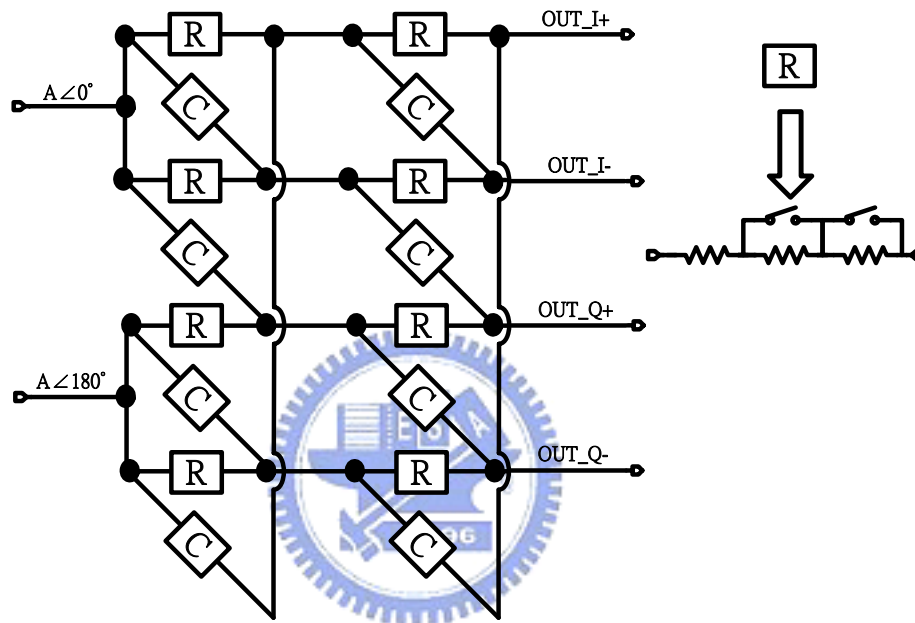


Fig. 3.25 A two-stage poly-phase filter

Table 3.2 RC values of the two-stage poly-phase filter

Frequency (MHz)	C (fF)	R ( $\Omega$ )
10032	100	158.6
9504	100	167.5
8976	100	177.3
8448	100	188.4
5016	100	317.3
3168	100	502.4
1584	100	1004.7
1056	100	1507.2
528	100	3014.3

### 3.2.8 Band-Selector

A selector must provide fast switching and symmetry with respect to its three inputs. A conventional current-steering selector may suffer from undesired modulation, since the unselected signal in the disabled pair would still couple to the output through the parasitic capacitance. This circuit is shown in Fig. 3.26, where three dummy pairs, M47–M48; M49–M50 and M51–M52, are introduced to eliminate the unwanted coupling to the first order while consuming no extra power. Then the control bit can control frequency selector. When one bit is work, the other bits are disabling. It cans effective control current consumption And reduce noise couple, then the Band-Selector1 frequency control in turn 1584MHz、3168MHz、5016MHz, the Band-Selector2 frequency control in turn 528MHz、1056MHz、1584MHz.

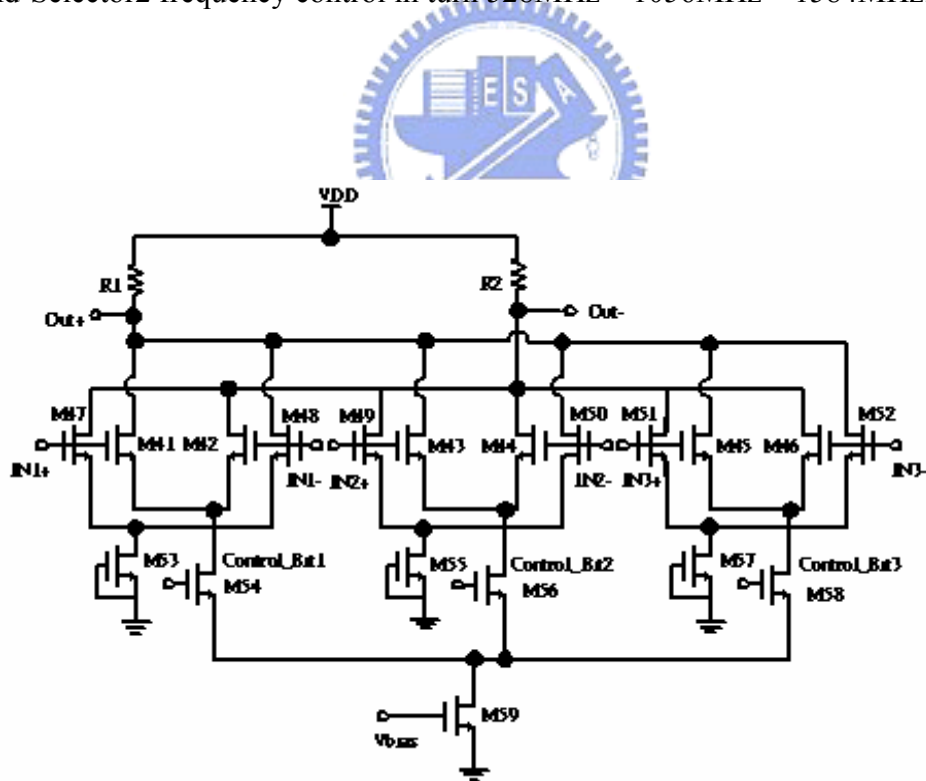


Fig. 3.26 Band-Selector Schematic

### 3.3 SIMULATION RESULTS

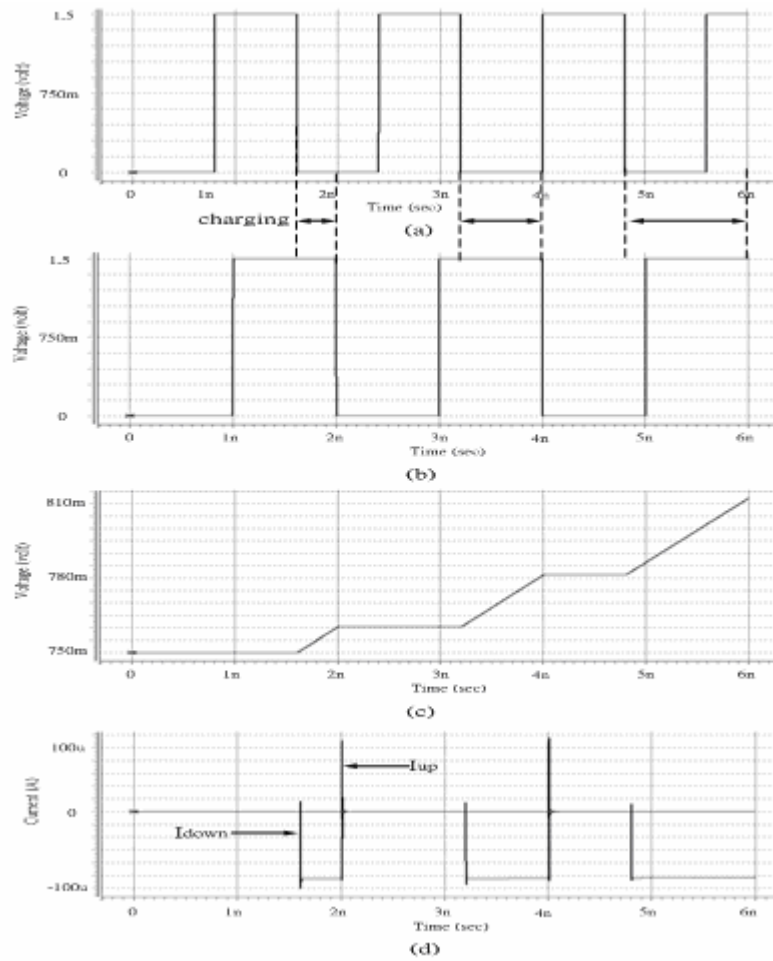


Fig. 3.27 Charging simulation of charge pump (a) reference clock. (b) Divider output. (c) the control voltage of VCO. (d)  $I_{up}$  and  $I_{down}$  of the charge pump.

In the Fig. 3.27, the charge pump is in charging mode. In Fig. 3.27 (a) and (b), we can find that the phase of the reference clock goes beyond the divider output and the frequency is higher than the divider output. So, the charge pump charges between the clock falling edges of the reference clock and output of divider. So, the control voltage is getting higher.

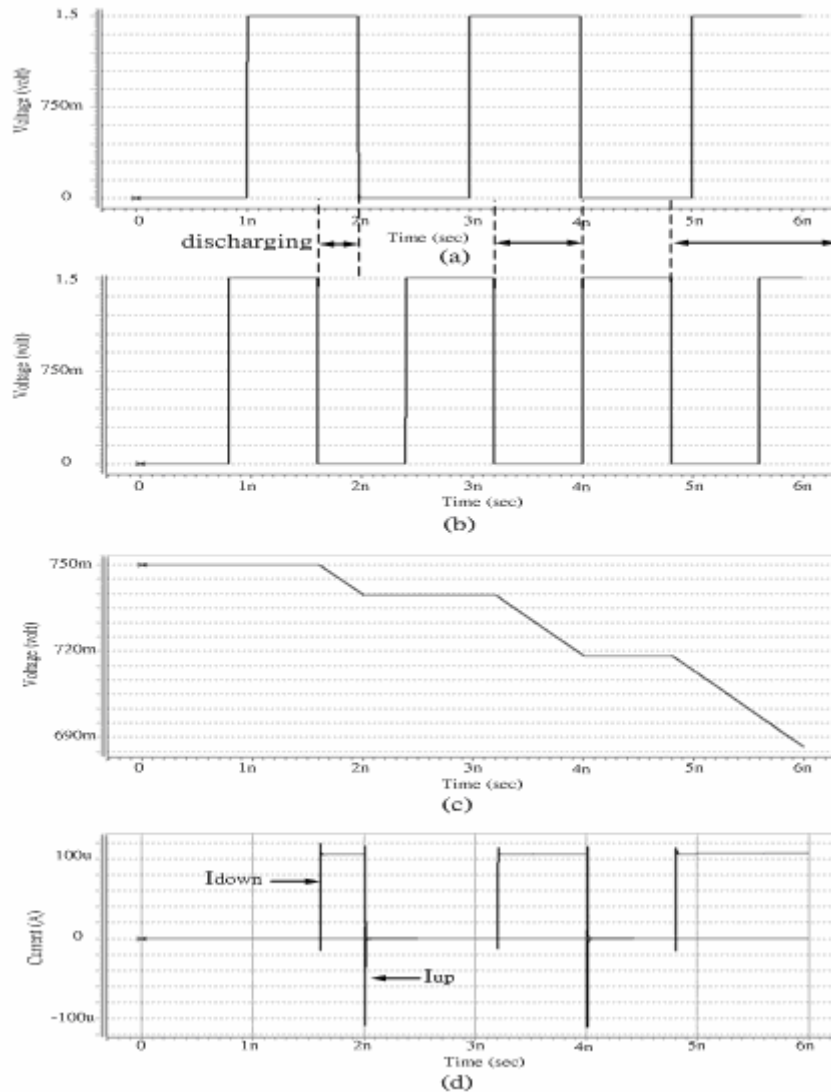


Fig. 3.28 Discharging simulation of charge pump (a) reference clock. (b) Divider output. (c) the control voltage of VCO. (d)  $I_{up}$  and  $I_{down}$  of charge pump

In the Fig. 3.28, the charge pump is in discharging mode. In Fig. 3.28 (a) and (b), we can find that the phase of the reference clock goes behind the divider output and the frequency is lower than the divider output. So, the charge pump discharges between the clock falling edges of the reference clock and divider output. So, the control voltage is getting lower.

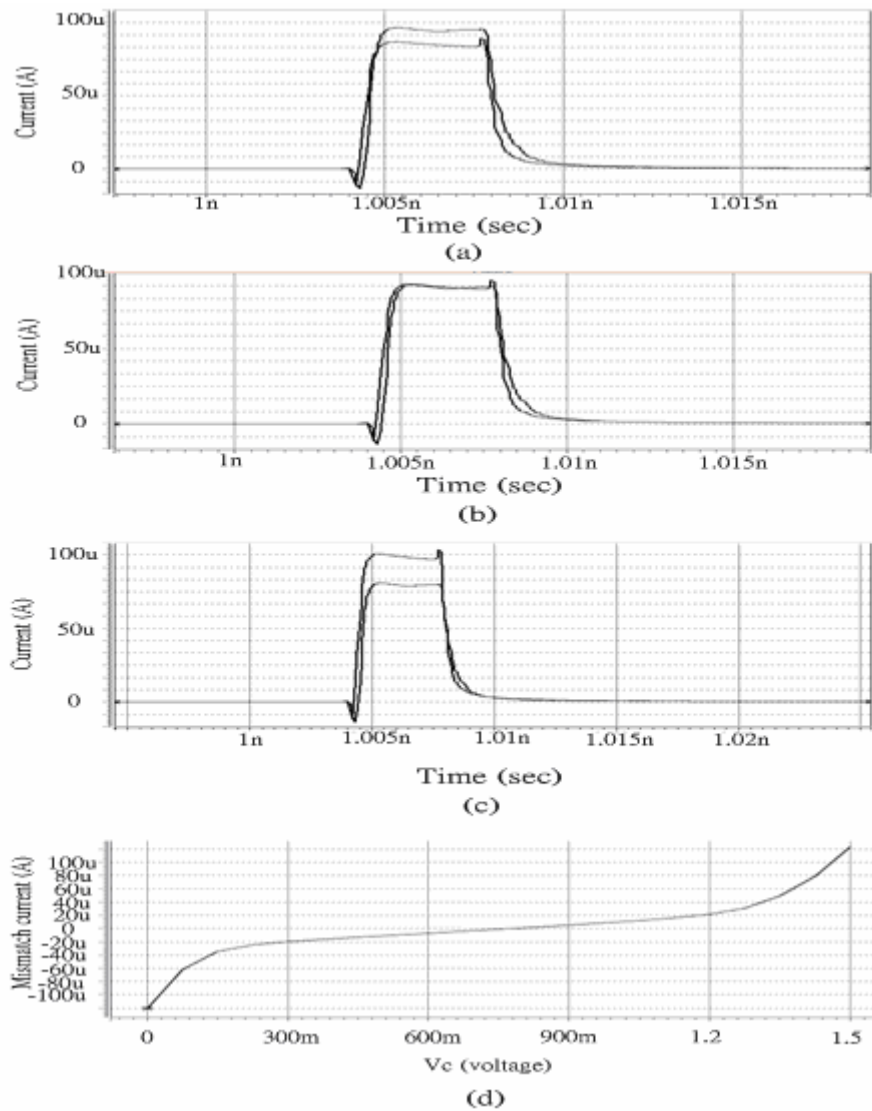


Fig. 3.29 Simulation results of the current-steering charge pump without current-match structure (a) The  $I_{up}$  and  $I_{down}$  at  $V_c=0.3V$  (b) The  $I_{up}$  and  $I_{down}$  at  $V_c=0.75V$  (c) The  $I_{up}$  and  $I_{down}$  at  $V_c=1.3V$  (d) The mismatch current v.s.  $V_{control}$

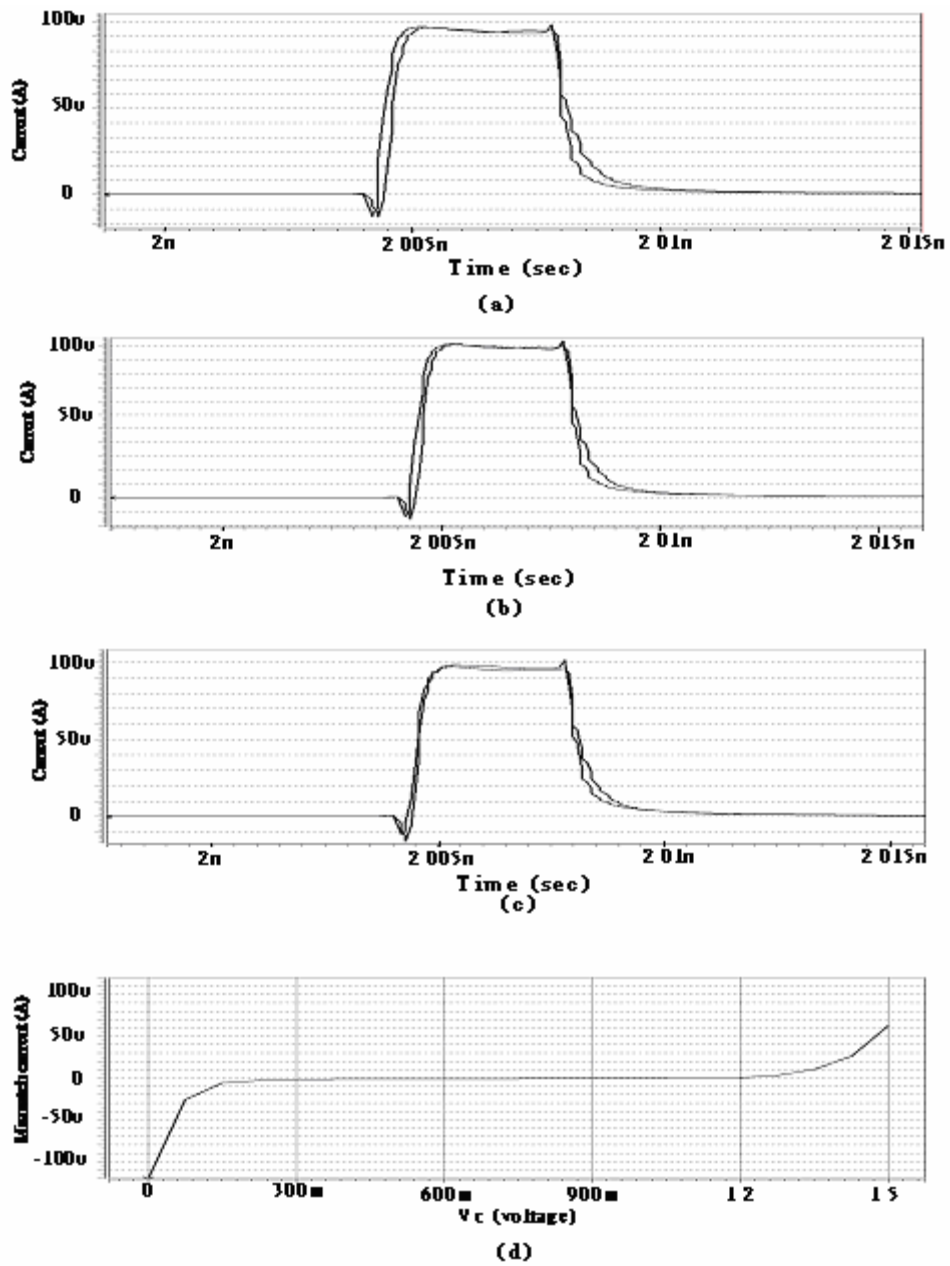


Fig. 3.30 Simulation results of the new current-match charge pump (a) The  $I_{up}$  and  $I_{down}$  at  $V_c=0.3V$  (b) The  $I_{up}$  and  $I_{down}$  at  $V_c=0.75V$  (c) The  $I_{up}$  and  $I_{down}$  at  $V_c=1.3V$  (d)

The mismatch current v.s.  $V_{control}$ .



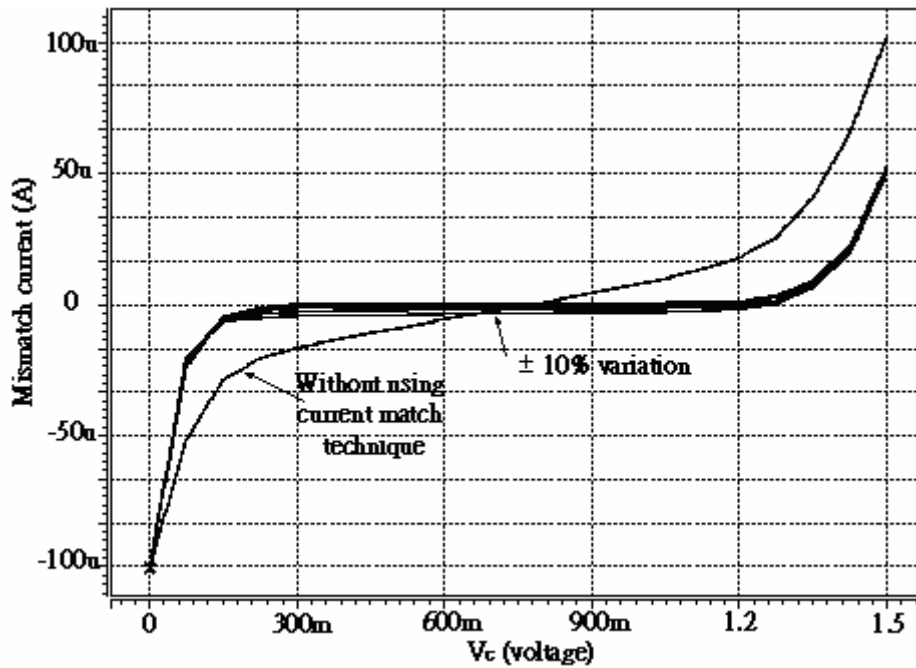
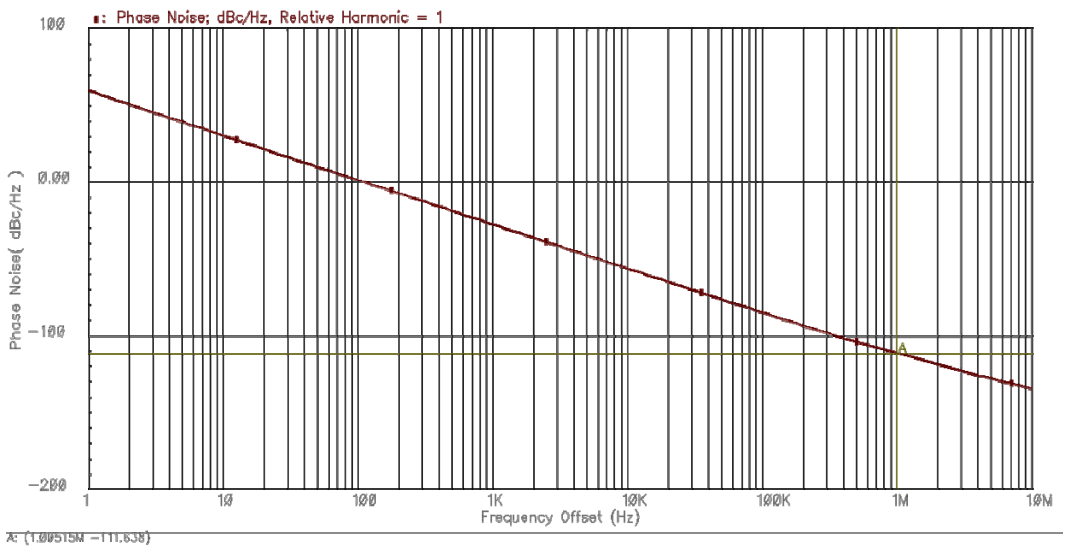
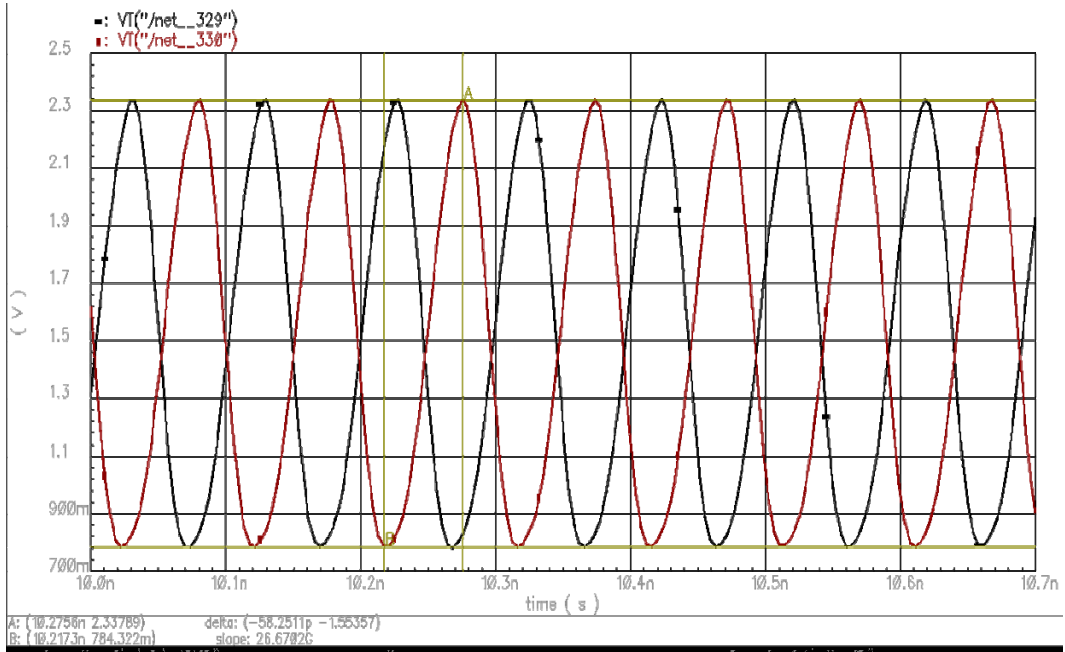


Fig. 3.31 The mismatch current simulations of charge pump with process variation, and compare the results with the charge pump without feedback loop.

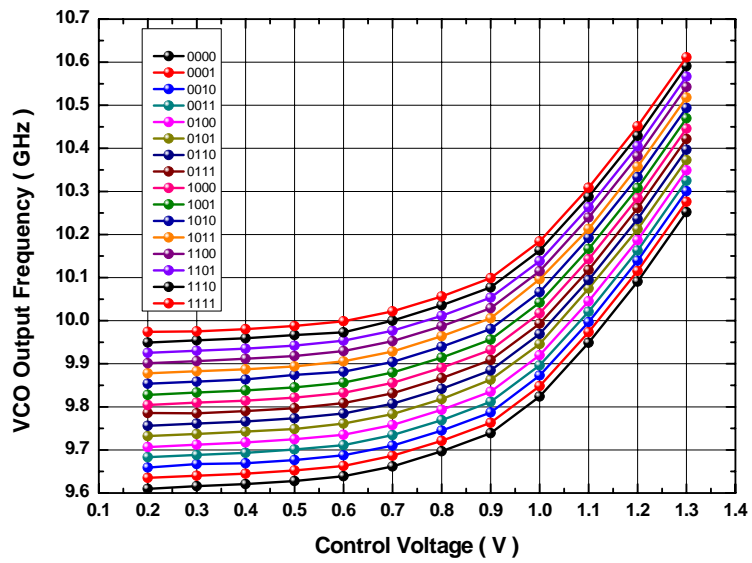
The current-steering charge pump without feedback loop is simulated in Fig. 3.29 (a) to (c) shows  $I_{up}$  and  $I_{down}$  at different  $V_c$  and we can find that the  $I_{up}$  and  $I_{down}$  just match at  $V_c=0.75V$ . In Fig. 3.29 (d) shows the mismatch current at different  $V_c$ . The maxim difference between  $I_{up}$  and  $I_{down}$  is about 20% of the charge pump current.

The current-match charge pump which used in this design is simulated in Fig. 3.30 (a) to (c) shows  $I_{up}$  and  $I_{down}$  at different  $V_c$  and we can find that when the  $V_c$  varies,  $I_{up}$  and  $I_{down}$  still match to each other. In Fig. 3.29 (d) shows the mismatch current at different  $V_c$  and the maxim difference between  $I_{up}$  and  $I_{down}$  is about 1.5% of the charge pump current.

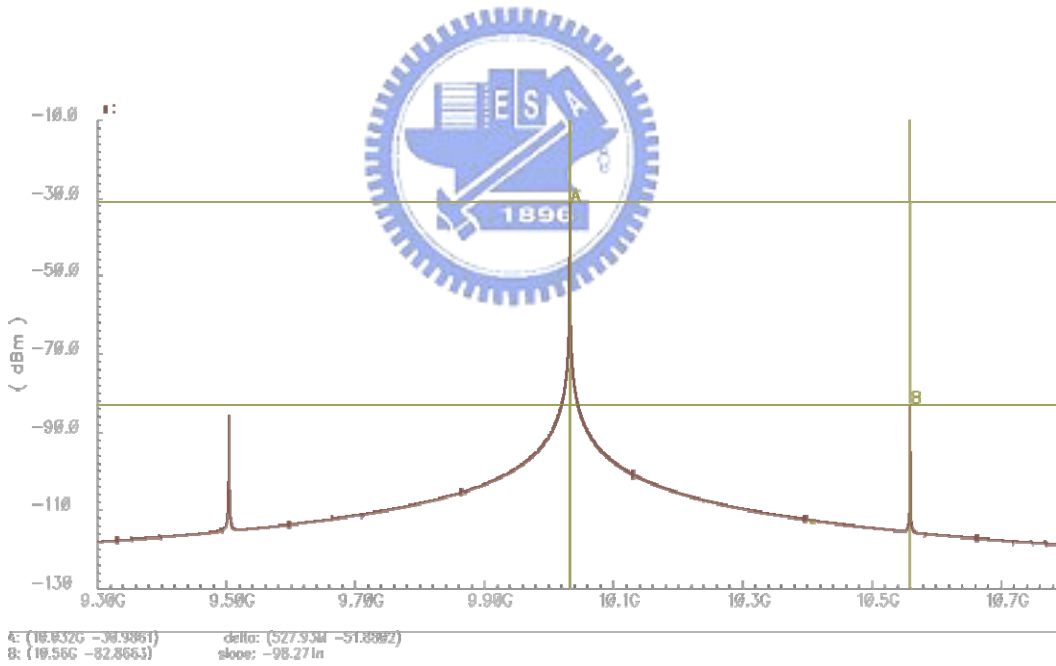
Fig. 3.31 shows the process variation impact of the current-match charge pump. We can find that even if the variation up to 10%, the mismatch current is smaller than witch without feed back loop.



(b)



(c)



(d)

Fig. 3.32 The simulation results of the band-switching VCO (a) The output waveform of the VCO (b) The phase noise simulation results by Spectre-RF (c) The tuning ranges of the sixteen bands simulation (d) Spurious tones simulation.

The simulation results of the VCO are shown in Fig. 3.32. The differential output waveforms of VCO are shown in (a) and the peak-to-peak amplitude is 1.55V. The phase noise of VCO is simulated by Spectre-RF and is shown in (b). In (b) we can find that the phase noise at offsets frequencies 1-MHz is  $-111.6\text{dBc}$ . This performance is suitable for UWB application. The tuning range of the 4-bits VCO is shown in (c). As mentioned in 3.2.2.2, the 4-bits band-switching VCO uses mimcap as the bank and split the tuning range into 16 bands as show in (c). When the control word of bank is 0000, the bank has the maximum capacitance. So, the VCO has the minimum frequency band. On the contrary, when the control word is 1111, the VCO changes the frequency band to the maximum frequency band. Beside, when the control word changes to 0111 or 1000, the frequency band of VCO changes to the middle band. In (e) is the simulation of spurious tones about  $-51\text{dBc}@528\text{MHz}$  offset.



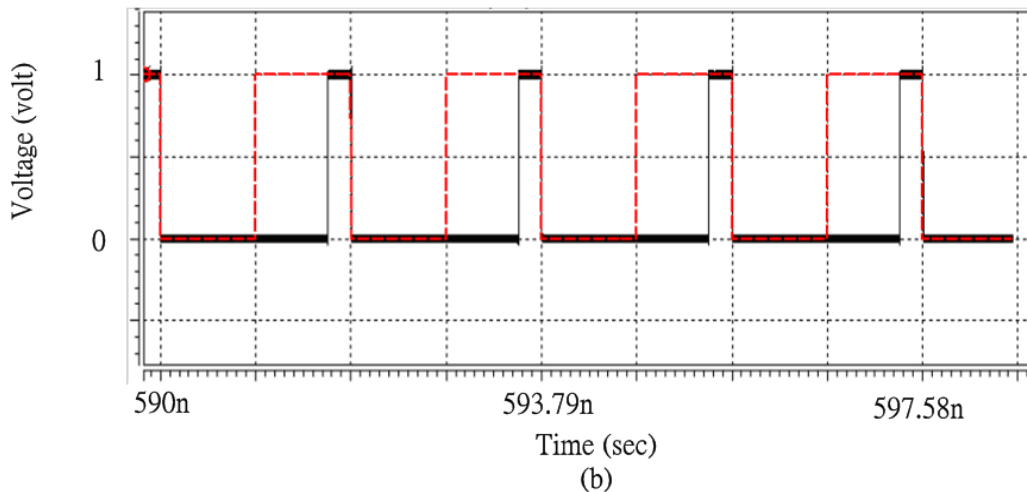
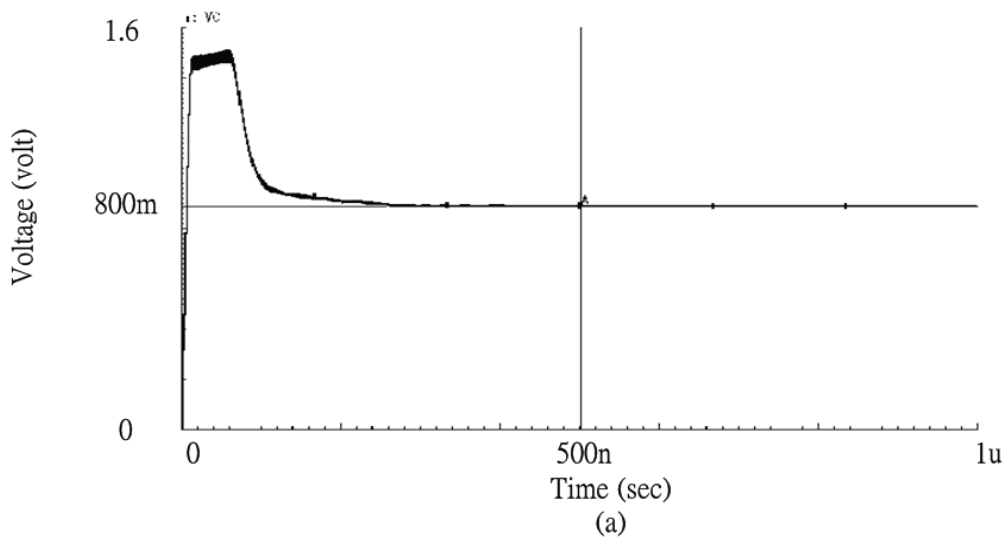
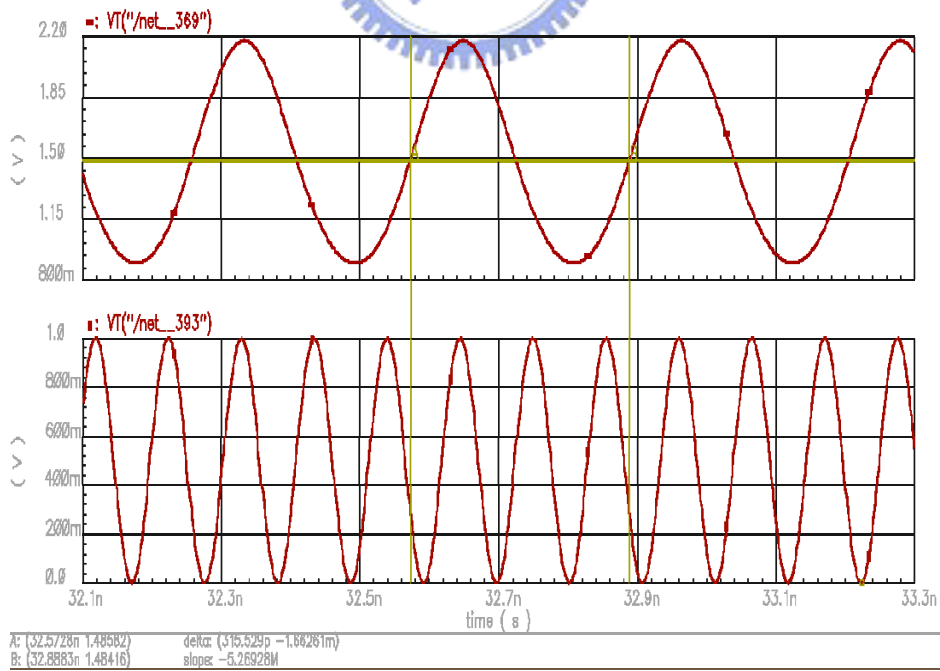
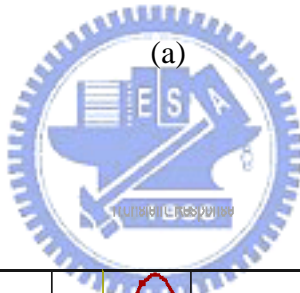
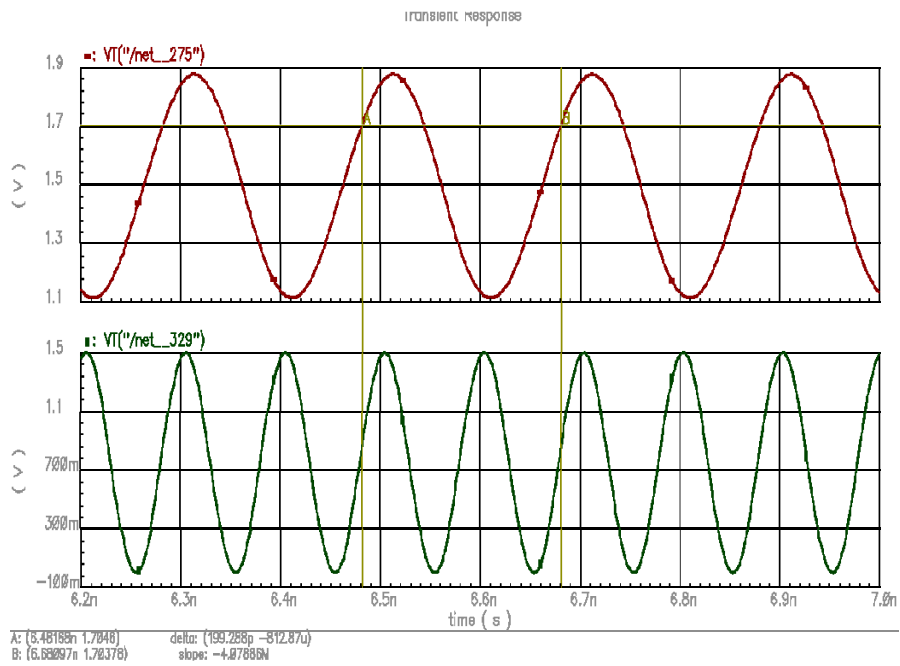


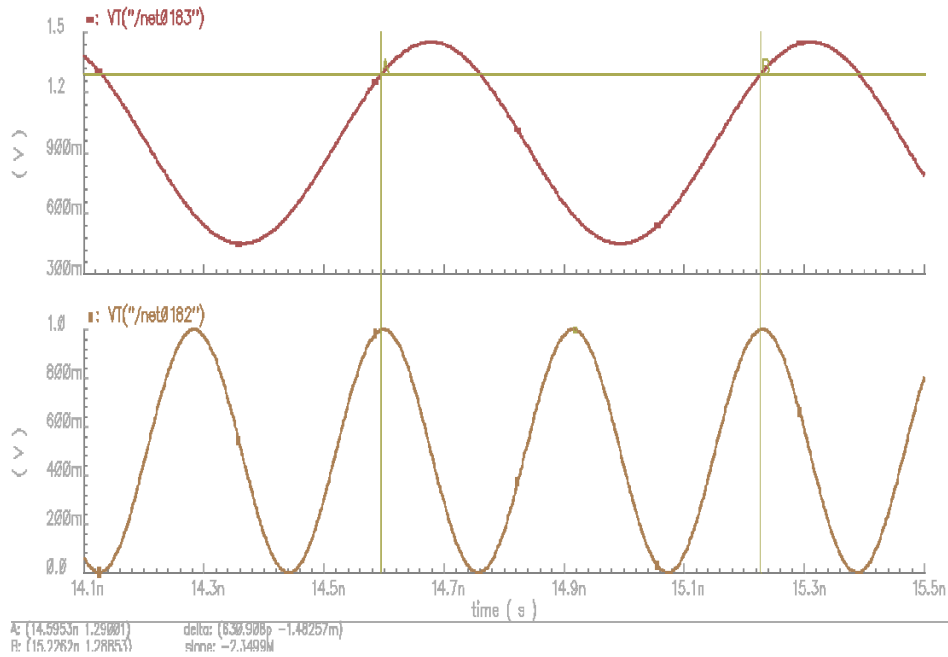
Fig. 3.33 The close loop simulation of the PLL (a) The control voltage of VCO (b)

The reference clock and the output waveform of counter

The close loop simulation of the frequency is shown in Fig. 3.33. The  $V_c$  which controls VCO is shown in (a) and we can find that it is locked within 1 usec. Fig 29 (b) shows the reference clock and the output waveform of counter. We can find that the edges of reference clock and output of counter match to each other. This means that the frequency synthesizer is locked.

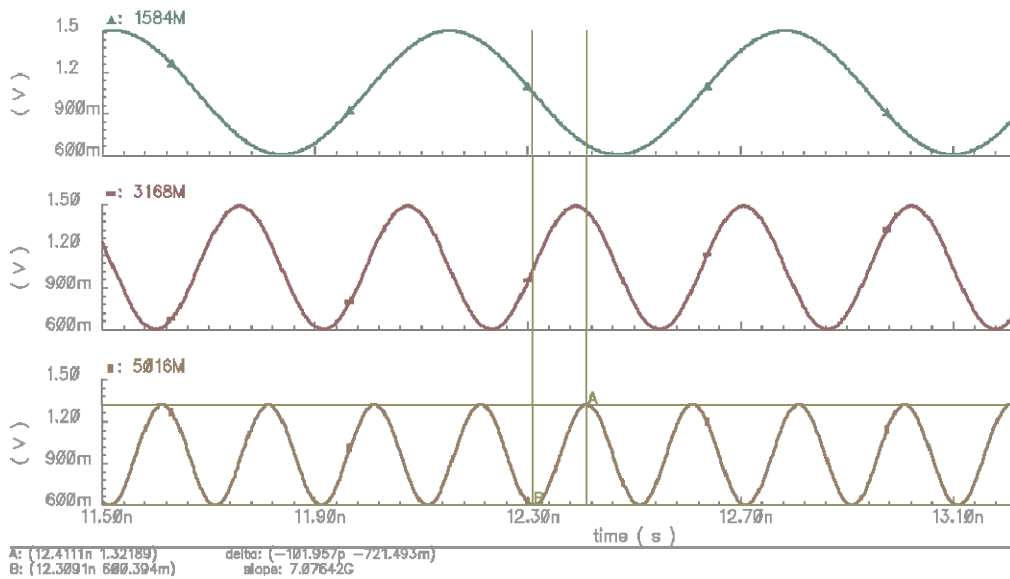


(b)



(c)

Fig. 3.34 Simulation results of the Divider (a) Divide-by-2 Stage for 5016MHz (b) Divide-by-3 Stage for 3168MHz (c) Divide-by-2 Stage for 1584MHz



(a)

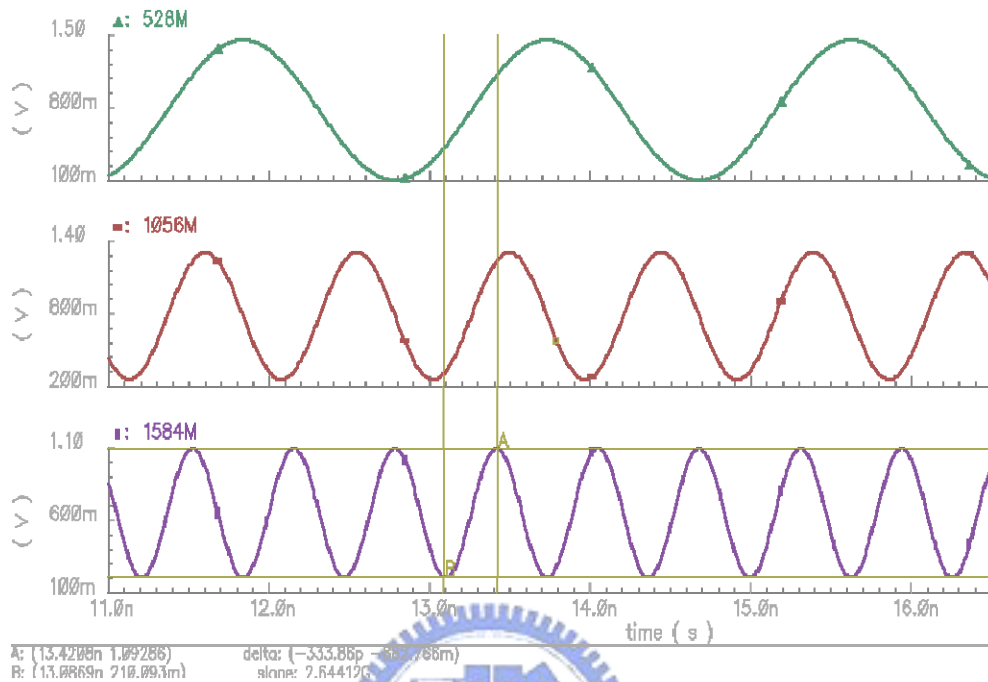
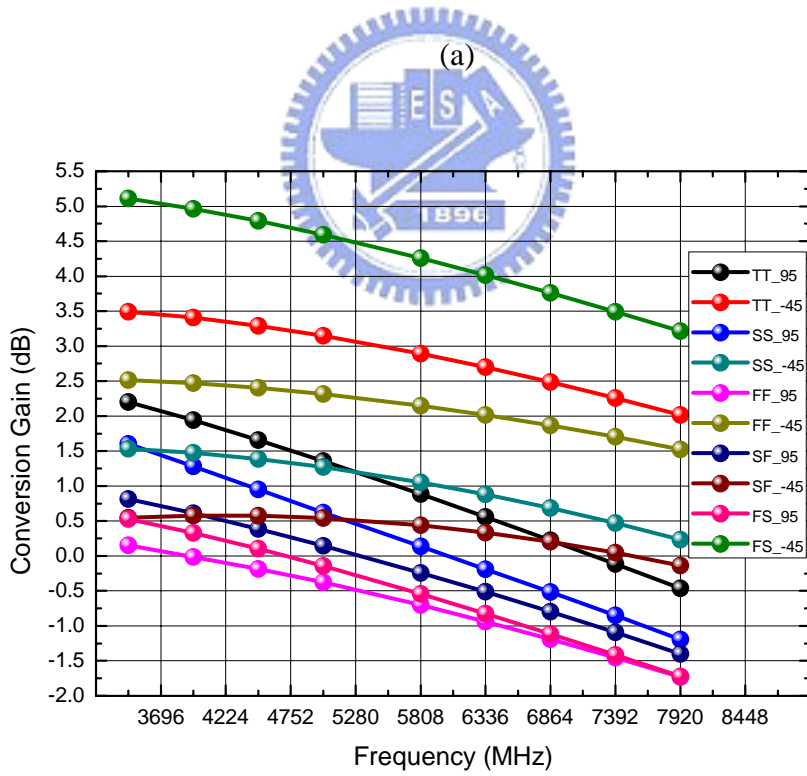
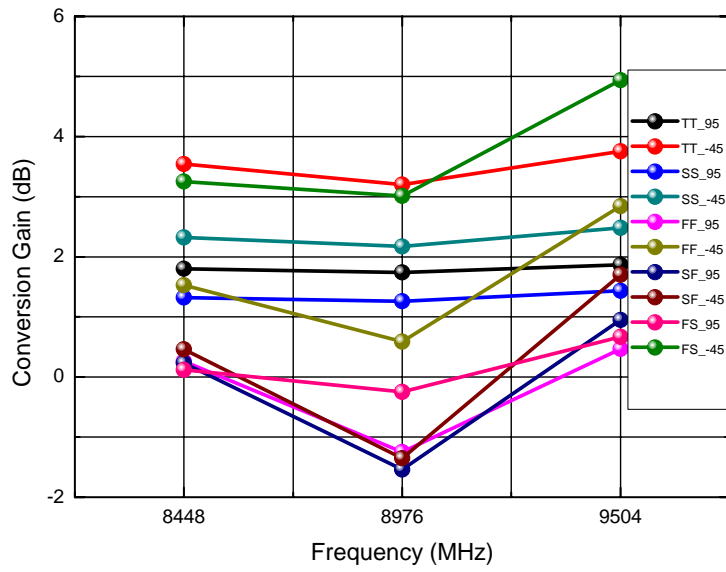


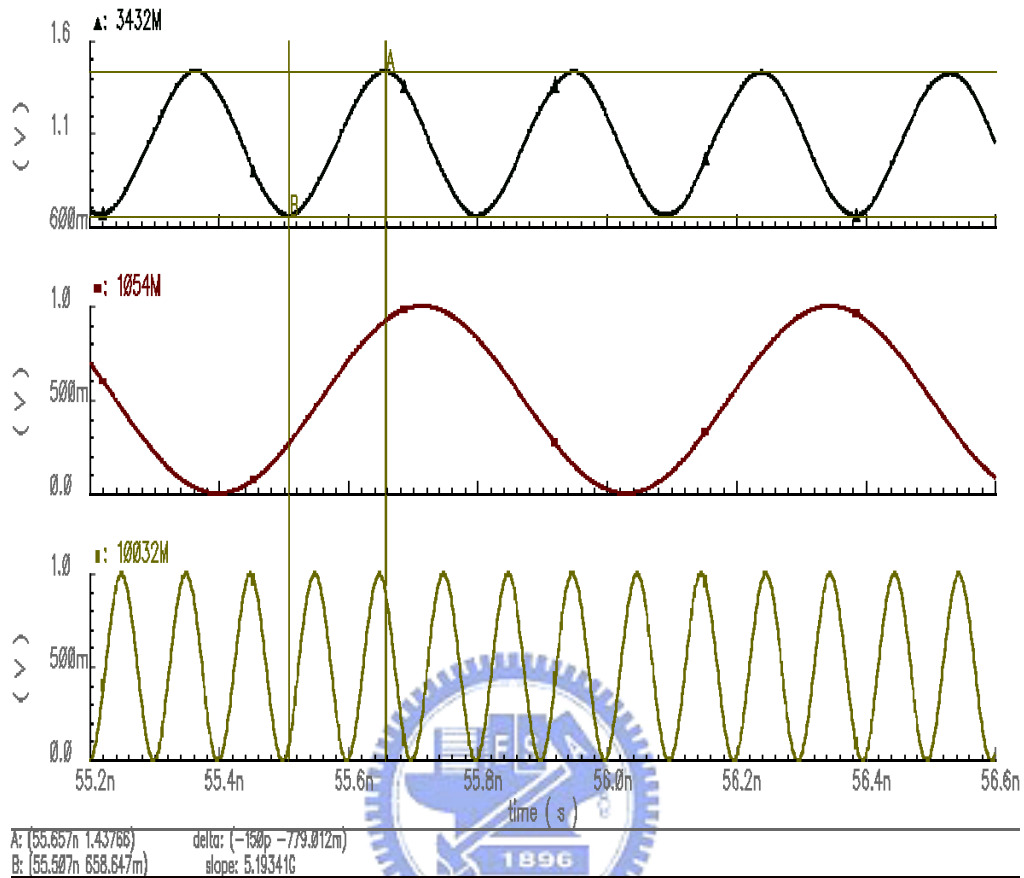
Fig. 3.35 Simulation results of the Band-Selector (a) Output Amplitude of the Band-Selector1 (b) Output Amplitude of the Band-Selector2

The simulation results of Divider and Band-Selector are shown in Fig. 3.34 and Fig. 3.35. In Fig. 3.34 the divider is dividing 2 and 3. Then, the minimum peak-to-peak amplitude is 760mV for a 5016MHz sinusoidal output. In the Fig. 3.35, the Band-Selector1 frequency control in turn 1584MHz、3168MHz、5016MHz, the Band-Selector2 frequency control in turn 528MHz、1056MHz、1584MHz. Then, The minimum peak-to-peak amplitude is 725mV for a 5016MHz sinusoidal output.





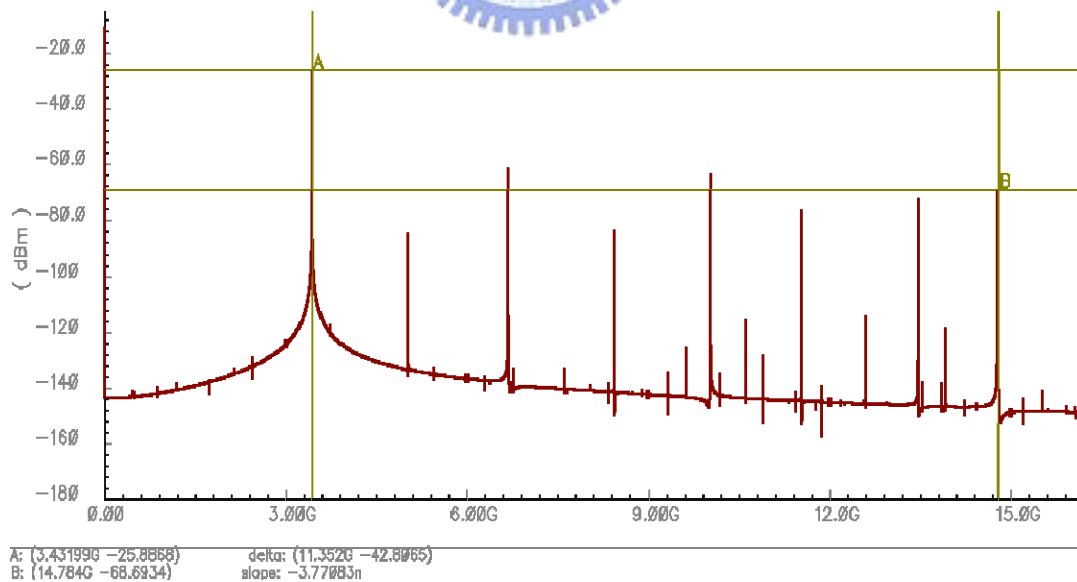
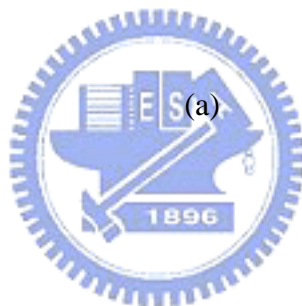
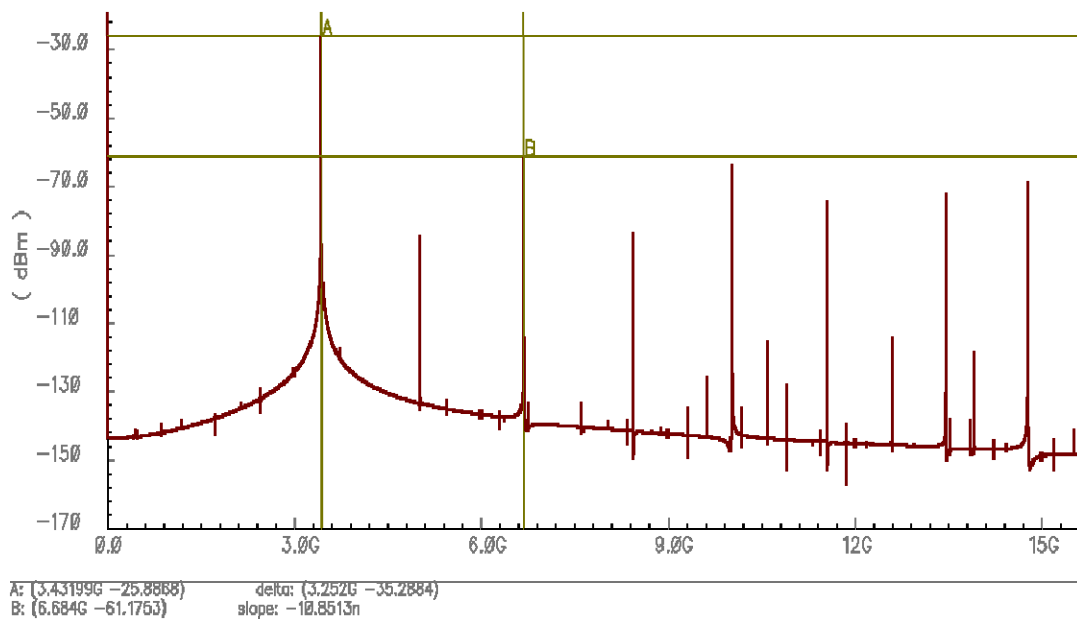
(b)



(c)

Fig. 3.36 The simulation results of the Mixer (a) Mixer1,3 Conversion Gain (b) Mixer2 Conversion Gain (c) Output waveforms for a 3.432GHz sinusoidal output.

The simulation results of mixer are shown in Fig. 3.36. As shown in (a) (b) the voltage conversion gain of the all mixers are above 0dBm for UWB application. In Fig. 3.36(c), the minimum peak-to-peak amplitude is 770mV for a 3.432GHz sinusoidal output.



(b)

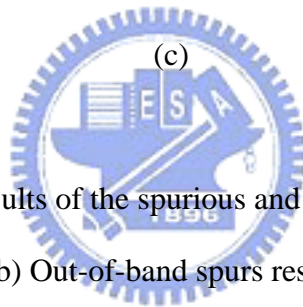
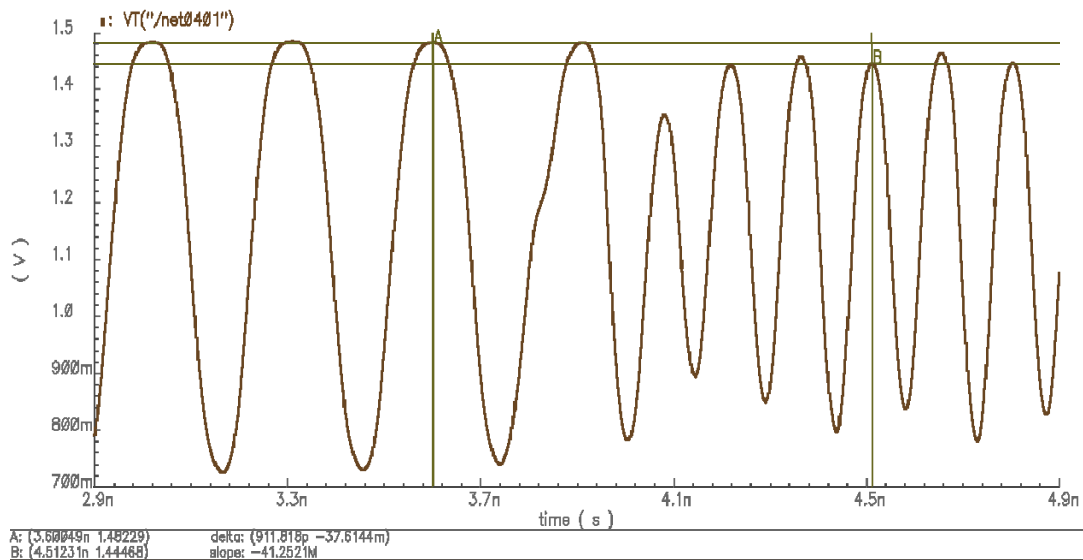


Fig. 3.37 The simulation results of the spurious and switching time (a) In-band spurs response at 3.432 GHz (b) Out-of-band spurs response at 3.432 GHz (c) Switching time between adjacent bands.

The simulation results of the spurious and switching time are shown in Fig. 3.37. As shown in (a) and (b), the additional in-band spurs are generated at 6.864GHz with spurious response of  $-35.2$  dBc, and out-of-band spurs are generated at 14.784 GHz with spurious response of  $-42.8$  dBc respectively. In (c) the bands are switched periodically and the synthesizer output is monitored. The longest switching time is approximately equal to 911ps.

Table 3.3 The summary of the post-simulation

	Post-simulation
Supply voltage	1.5 V
Frequency range	3.432~10.032 GHz
Reference clock	528 MHz
K <sub>vco</sub> (VCO gain)	160MHz/V
Phase noise (using SpectreRF)	-112 dBc/Hz @1MHz offset
Charge pump current	100uA
Loop bandwidth	5500 kHz
Close loop PM	65°
PLL lock time	500 ns
Switching time	0.911ns
In-band spur	-35.2dBc
Out-of-band spur	-42.8dBc
Mixer conversion gain	>0dBm
Chip area	1900 X 1900 um <sup>2</sup>
Power consuming	50.07~147.35 mW
Technology	TSMC 0.18um CMOS

# Chapter 4

## Experiment Results

The chip, UWB frequency synthesizer for UWB applications is designed and fabricated in TSMC 0.18- $\mu\text{m}$  CMOS process. In this chapter, the chip layout, test environment, and experiment results are presented. Measured performance is compared with post-simulation results and discussion is made for further study.

### 4.1 Layout Description

The chip is designed and fabricated by TSMC 0.18 $\mu\text{m}$  1P6M CMOS technology. The process is implemented to fulfill the applications for mixed signal/RF, such as inductor with low receptivity and good conductivity and lower capacitance to substrate. Besides, deep n-well topology is employed to surround the N-MOS device, which allows the connection of source and body terminals to avoid body effect. Dummy gates and dummy resistors are equipped at the margin of every MOS device to cope with process variation. The MOS varactors are separated into two groups, one with deep n-well while the other without. With the aid of deep n-well, parasitic capacitance and noise coupling from substrate can be reduced. Meanwhile, the MIM capacitor in this technology is somehow special, with or without under ground metal shielding is provided: the former has high immunity to substrate noise and the latter presents less parasitic capacitance.

In the experimental chip, all of the function blocks including PLL, Mixer, Band-selector, and Poly Phase Filter circuits are integrated on the same chip. The overall layout is shown in Fig. 4.1. We present the measured results, the spurious tones  $-30.6$  dBc @ 3432 MHz is worst. The tuning range of VCO shift about

350MHz which be compared with simulation. The phase noise is -106 dBc/Hz @ 1MHz offset is achieved. The power consumption is 55.1~161.62 mW. The overall area is 1900 $\mu\text{m}$  $\times$ 1900 $\mu\text{m}$ .

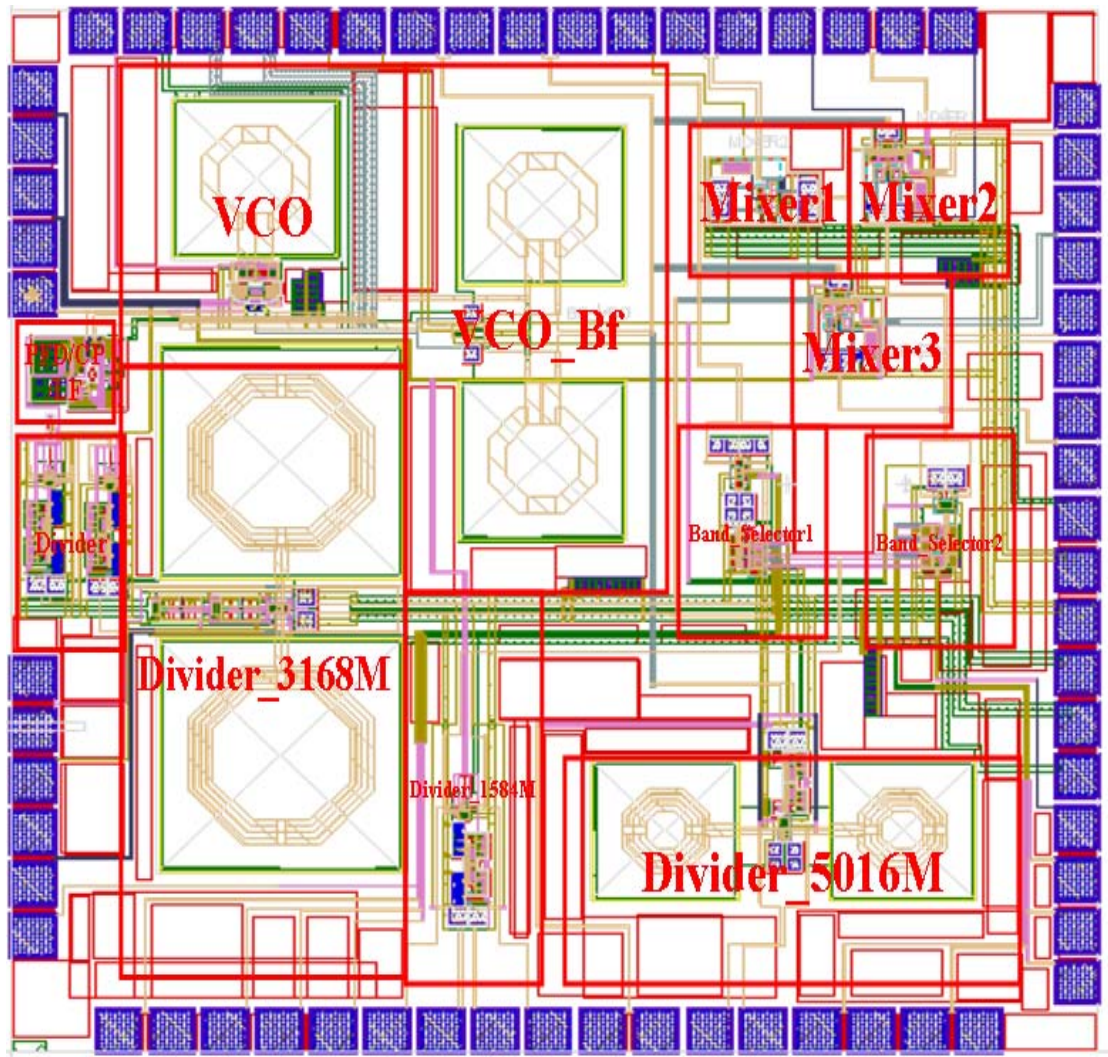


Fig. 4.1 The frequency synthesizer layout view.

## 4.2 Measurement Results of the Frequency Synthesizer

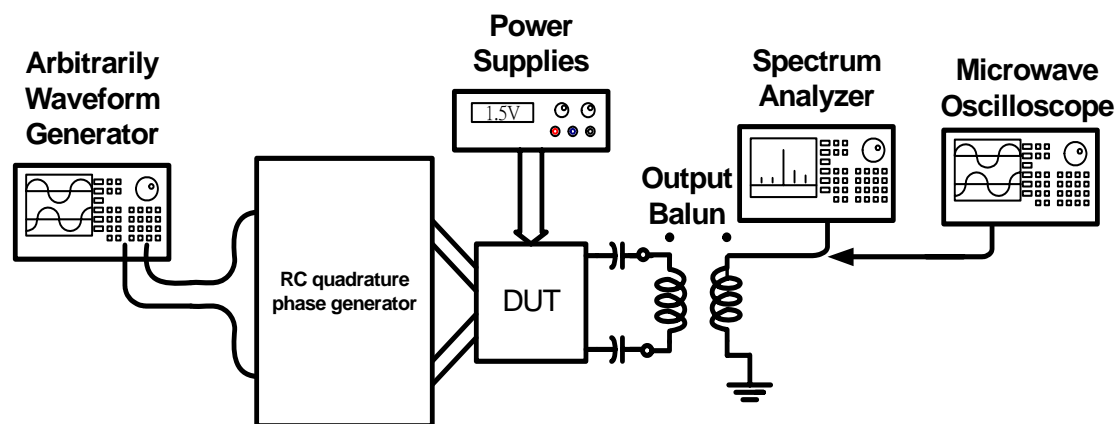


Fig. 4.2 Measurement setup of the frequency synthesizer

In Fig. 4.2 we show the measurement setup diagram of frequency synthesizer. And the input reference signal is provided by AWG. At the output terminals, a BALUN converts differential output to single output and feeds this output to spectrum analyzer and microwave oscilloscope. At the output terminals, a BALUN converts differential outputs to single output and feeds this output to spectrum analyzer. We can measure the spurious tone, phase noise and lock time on spectrum analyzer. And measure the switching time on microwave oscilloscope.

As shown in Fig. 4.3, the chip is bonded on a testing module. On this testing module. At the center of the testing module, a SMD packaged BALUN “BL2012” made by Advanced Ceramic X corporation converts differential output to single output and connects to spectrum analyzer by a SMA at lower side. All DC bias terminals are connected to a bias board by pin headers. All pin headers at outer side are grounded to provide some shielding ability.



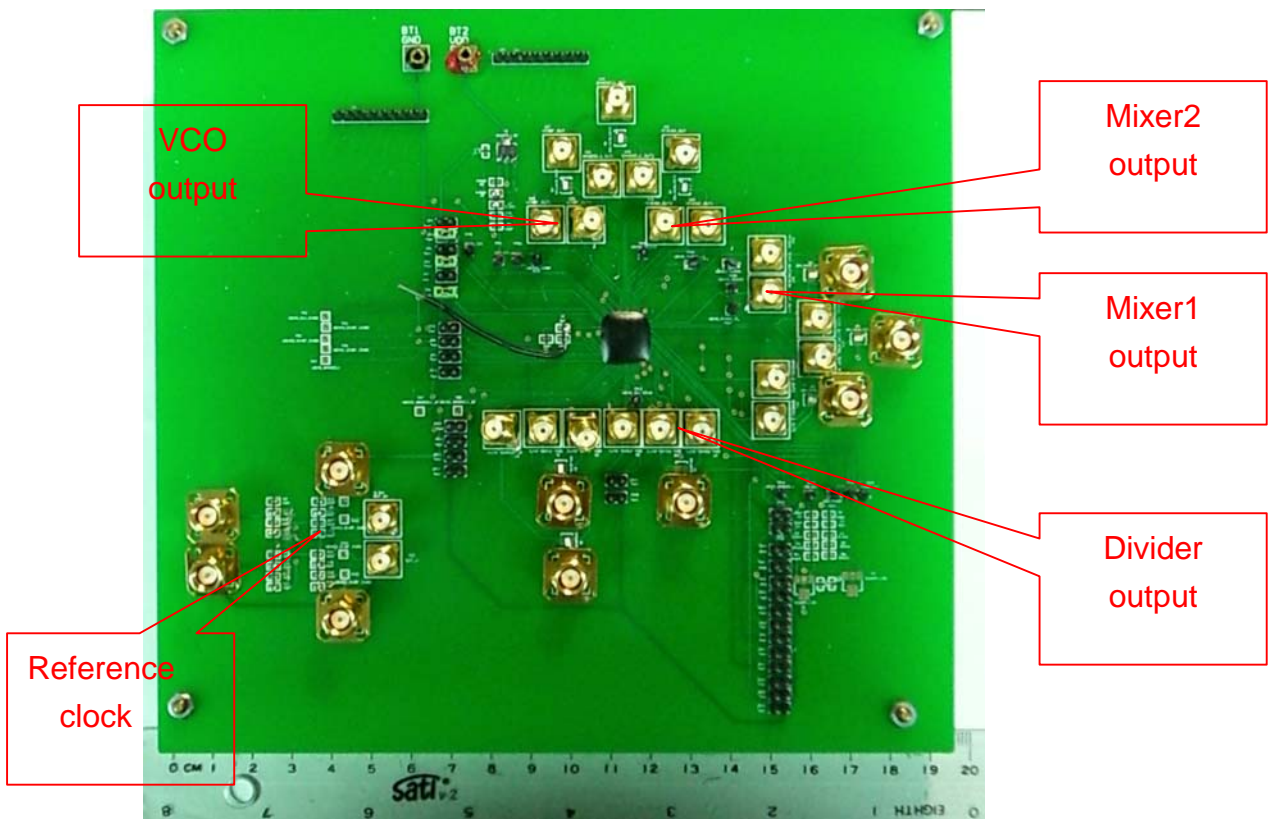


Fig. 4.3 Testing module of frequency synthesizer

#### 4.2.1 Measurement Results of the Band-switching VCO

The simulation and measurement of the band -switching VCO are shown in Fig. 4.4 and Fig. 4.5. The measurement result shows that the frequency range shift down about 350 MHz, but the tuning range is similar than simulation and the VCO frequency meet requirement. Initially, the 16 bands are designed to cover the unexpected process variation and the reduction in the tuning range. Therefore, some bands are indeed redundant as shown in the measurement results. The  $K_{VCO}$  is calculated for every 0.1 V step of the control voltage and the  $K_{VCO}$  of the tuning range is 160 MHz/V. The summary of VCO measurement and simulation results is shown in Table. 4.1.

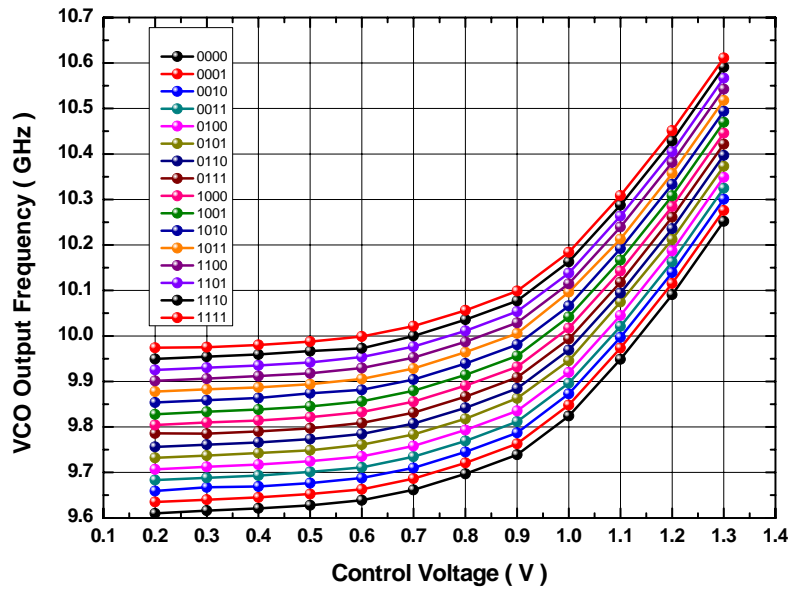


Fig. 4.4 The tuning ranges of simulation result.

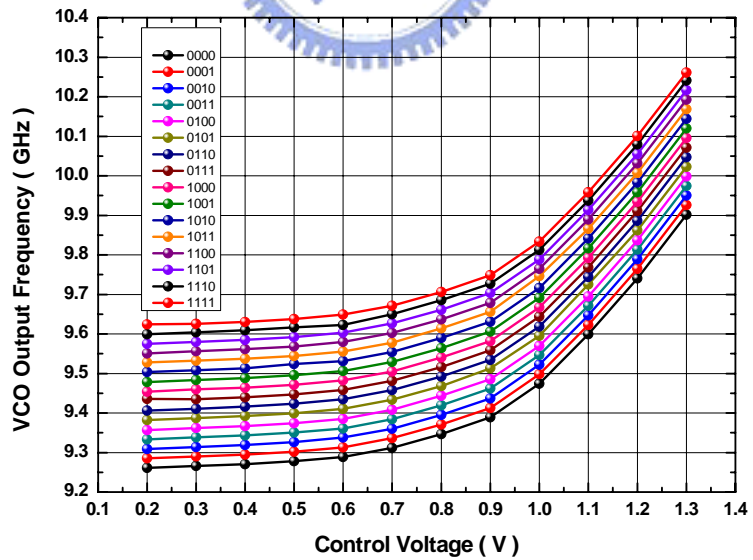


Fig. 4.5 The tuning ranges of measurement result.

Table 4.1 VCO summaries

	Post-simulation	Measurement
VDD_VCO (V)	1.5 V	1.5 V
Frequency Range (GHz)	9.6~10.6	9.27~10.25
VCO Gain (MHz/V)	160	160
Phase Noise@1MHz (dBc/Hz)	-111.6	-106
Current Consumption (mA)	10	11.4

#### 4.2.2 Phase Noise and Lock-Time Measurement Results

In Fig. 4.6 show the performance of phase noise when the measurement conditions are VCO frequency at 10.032GHz, reference frequency is 528MHz and loop bandwidth is 5500 kHz. In chapter 3, we mention that the phase noise should benefit from wider loop bandwidth of frequency synthesizer. Indeed, the phase noise of 5500kHz loop bandwidth is lower in this measurement, and it will be improved by paralleling larger capacitance to supply node. While paralleled capacitor is increased from 0.1uF to 22.1uF then the phase noise is decreased about 10dB. Thus, we must care the supply quality to get better performance of phase noise. The measurement results show that the phase noise performance is -106dBc/Hz at 1 MHz offset. In Fig. 4.7 shows the settling time measurement results, the settling time is about 600 ns. Thus, the settling time is a little large than simulation result.



Fig. 4.6 Phase noise measurement result, -106.48 dBc/Hz at 1MHz offset

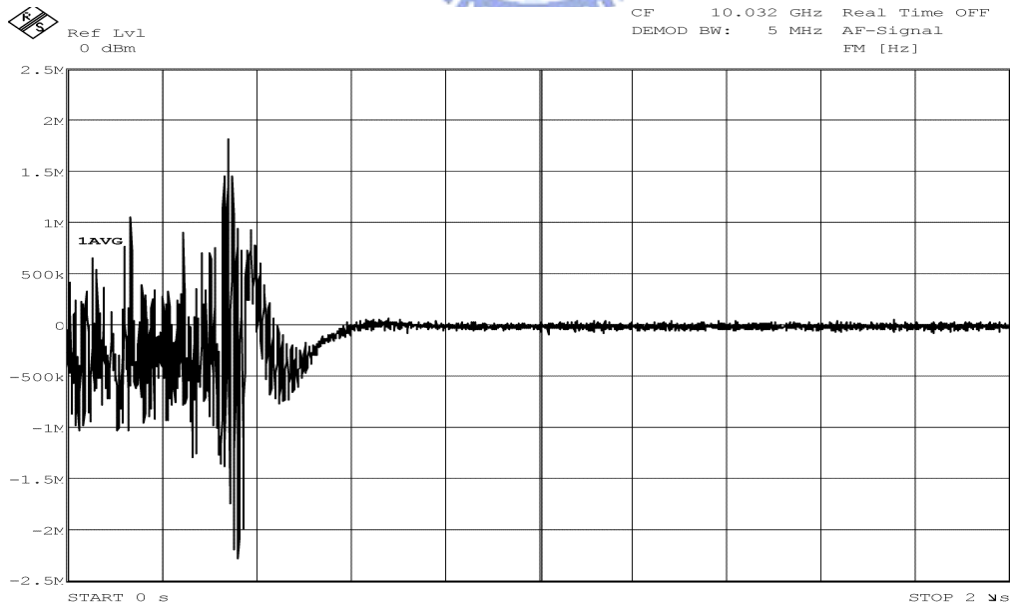
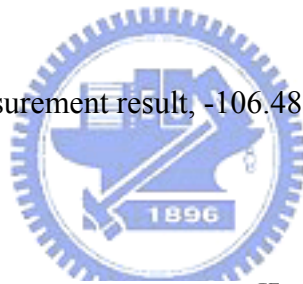


Fig. 4.7 Lock time measurement result

### 4.2.3 Spurious-Tones and Switching-Time Measurement Results

There are 2 types of spurs in this synthesizer. One type of spur is caused by the frequency mixing with 528MHz in mixer1. Hence, the spurs in the fourth group will decide those in other groups. Fig. 4.11 shows the sideband rejection at 8976MHz. Mixer1 provides 34dB suppression of the unwanted sidebands. The other type of spur is due to cascading mixers. Although fifth-order unwanted sidebands have been prevented by the frequency generation scheme in Fig. 4.12 higher-order spurious tones must be taken into consideration when the groups are down-converted by mixer1 and mixer2. The worst case occurs in the first group in Fig. 4.8 is  $-30.6\text{dBc}$ . The 3rd harmonics on the RF and LO ports of mixer2 will generate spurs in the adjacent group. The frequencies of the spurious tones are given, with the center frequency of 3432MHz in the first group, the RF frequency is 5016MHz and the LO frequency is 8448MHz, which introduces spurs at 6600MHz and 11616MHz. This effect can be observed by monitoring the whole UWB spectrum and noting that the sideband rejection is over 32 dB because the 2-stage SSB mixer was used. Other spurious measurement results in Fig. 4.9 and Fig. 4.10 are  $-46\text{dBc}$  and  $-32.6\text{dBc}$ . The band switching behavior is shown in Fig. 4.13 and the frequency switching time is about 3.75ns, a value much less than the 9.5-ns guard interval defined in UWB. The switching time are influenced by three sources: ① mixer turn on time, ② Poly-phase filter switch time and ③ band-selector switch time. The best switching time is probably 3.75ns, but the worst switching time is probably 15.1ns. The reason of the difference of the switching time is that the function generators used to switch bands are asynchronous, so in the different switching situation, the switching times are also different.

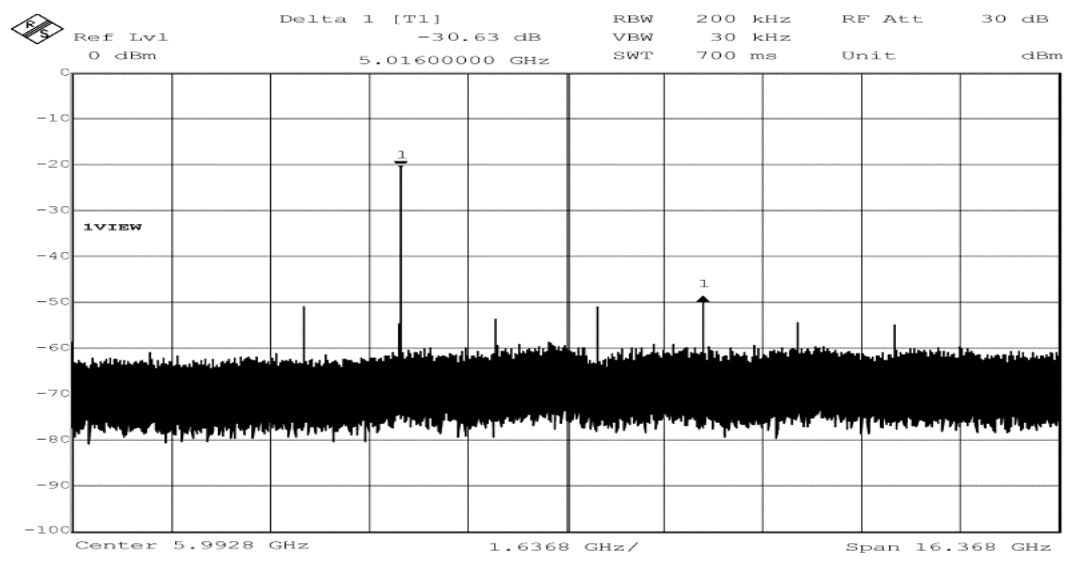


Fig. 4.8 Measured SSB mixer2's spurs in the first group (<-30.6dBc)

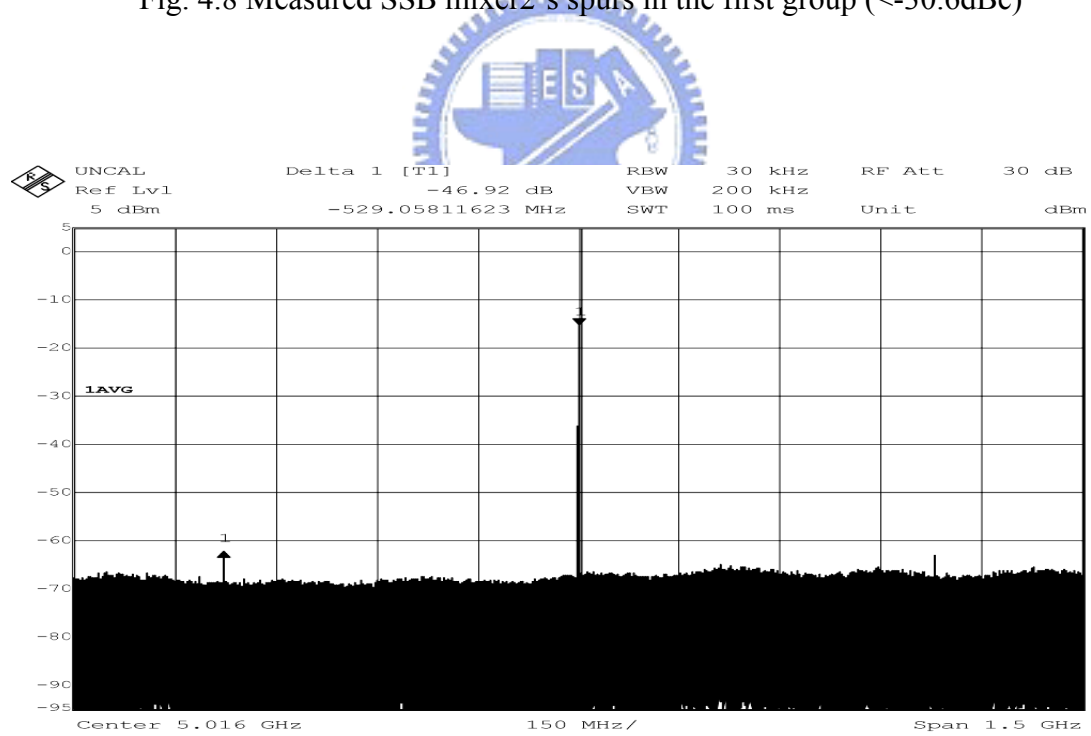


Fig. 4.9 Measured Divider's spurs in the second group (<-47dBc)

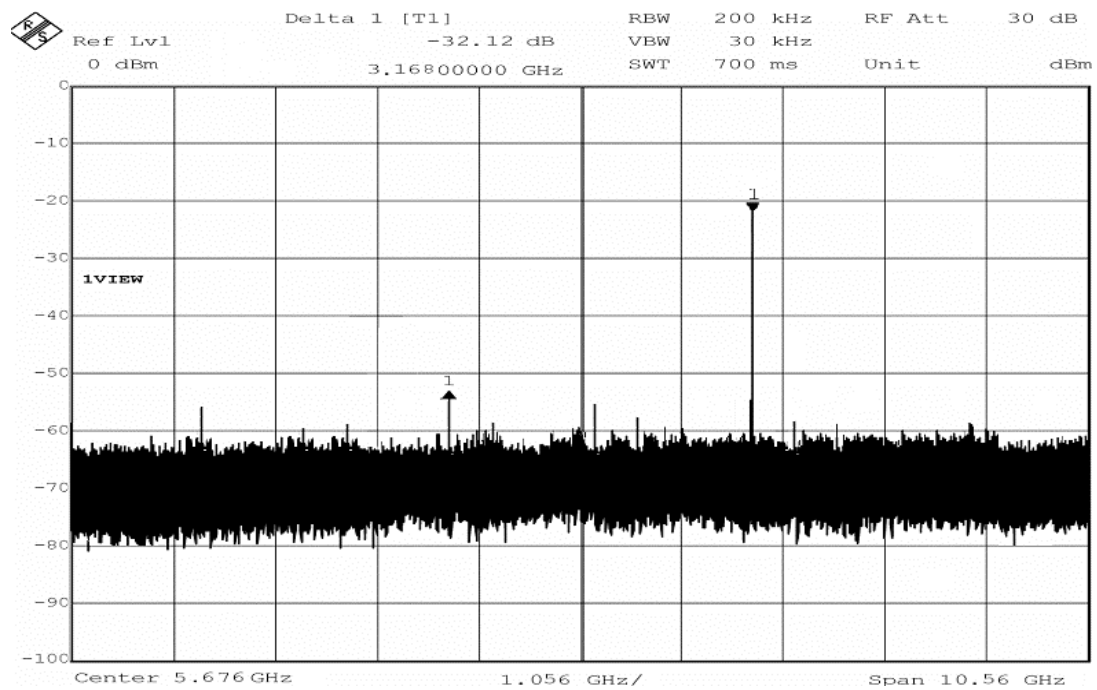


Fig. 4.10 Measured SSB mixer2's spurs in the third group (<-32dBc)

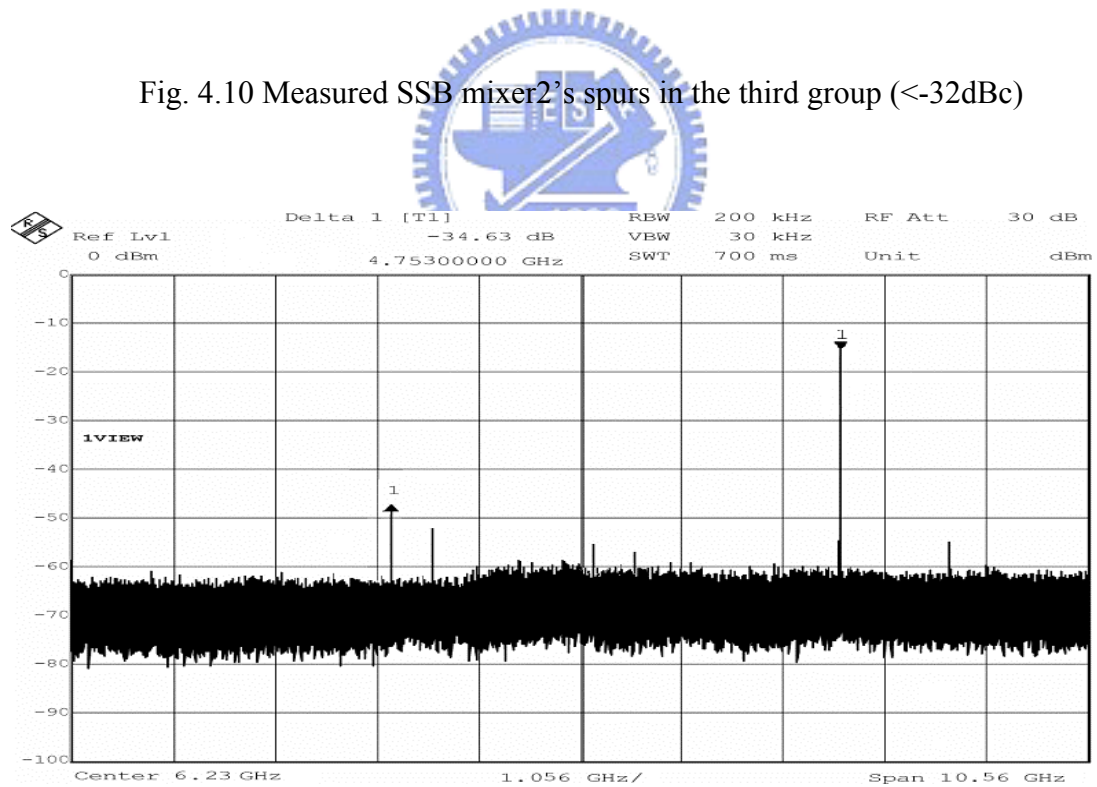


Fig. 4.11 Measured SSB mixer1's spurs in the fourth group (<-34dBc)

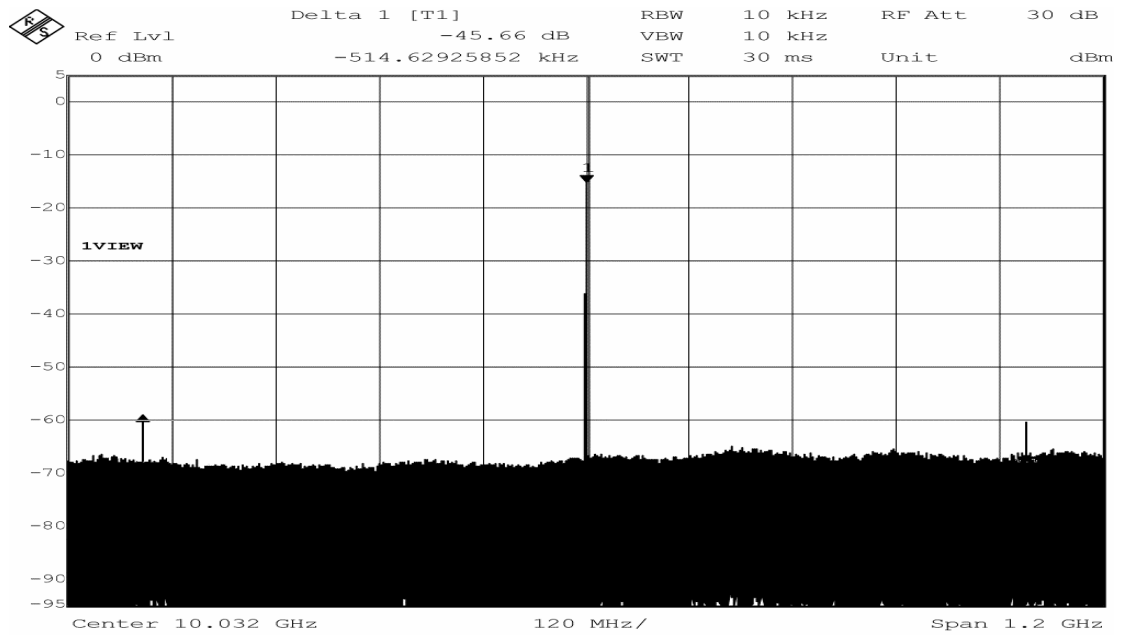


Fig. 4.12 Measured VCO's spurs in the fifth group (<-45dBc)

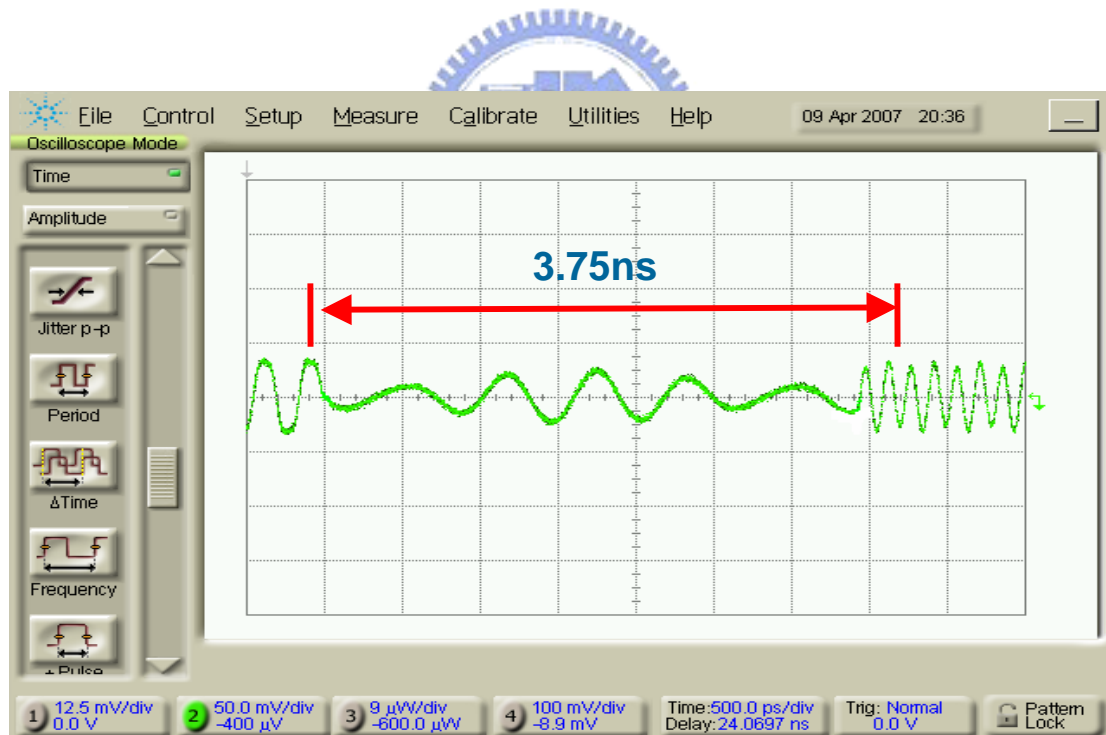


Fig. 4.13 Band-switching behavior (From group 3 to group 1)



### 4.3 Summary of Measurement Results

Table. 4.2 and Table. 4.3 summarize the chip performance of frequency synthesizer. And the tables summarize all measurement results compared with the post-simulation outcome and other architecture.

Table 4.2 Summary of the performance of the frequency synthesizer

		<i>Post-simulation</i>	<i>Measurement</i>
<b>VDD (V)</b>	<b>VCO</b>	1.5	1.5
	<b>MIXER</b>	1.5	1.5
	<b>DIVIDER</b>	1.5	1.5
<b>Channel spacing (MHz)</b>		528	528
<b>Lock time (ns)</b>		500	600
<b>Switching time (ns)</b>		0.911	3.75
<b>VCO gain (MHz/V)</b>		160	160
<b>Frequency band (GHz)</b>		3.1 ~10.6	3.1~10.6
<b>Tuning range (GHz)</b>		9.6~10.6	9.27~10.25
<b>Loop bandwidth (kHz)</b>		5500	5500
<b>Phase noise@1MHz (dBc/Hz)</b>		-111.6	-106
<b>In-Band spur (dBc)</b>		-35.2	-30.6
<b>Out-of-band spur (dBc)</b>		-42.8	-40
<b>Total power(mW)</b>		50.07~147.35	55.1~161.62

Table 4.3 Performance comparison with other UWB frequency synthesizer

	[2]	[3]	[4]	[5]	This work
Frequency range (MHz)	6336~8976	3432~7920	3432~4488	3432~10032	3432~10032
Reference clock (MHz)	528	264	N/A	66	528
PLL used	1	2	3	2	1
Bands	6	7	3	14	14
PLL locking time (ns)	150@26MHz BW	N/A	N/A	N/A	600@5.5MHz BW
Phase noise@1MHz (dBc/Hz)	-109.6	-103	-104	N/A	-106
SSB mixer used	0	1	3	3	3
In-band spur (dBc) Out-of-band spur (dBc)	-52 N/A	<-37 <-48	-30	<-35	-30.6 -40
Switching time(ns)	~100 6336~7392	1 3432~5016	9.47	<3 group3~group2	3.75 3432~6864
VCO tuning range(MHz)	6336~8976	900,470	3432~4488	N/A	9270~10250
Current consumption (mA)	47.3x3=141.9 1.8V	21.8x2=43.6 2.2V	70x3=210 1.5V	90 1.8V	72.24 1.5V
Process	0.18um CMOS	0.18um CMOS	0.13um CMOS	0.18um CMOS	0.18um CMOS

# Chapter 5

## Conclusion and Future Work

### 5.1 Conclusions

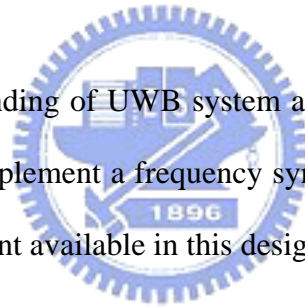
A 1.5-V frequency synthesizer with integrated PLL, mixer, band-selector, and poly phase filter for UWB applications has been designed, fabricated and tested in a 0.18- $\mu\text{m}$  CMOS technology. The architecture of the frequency synthesizer is simple and suitable for low power and high data-rate UWB applications. Though seven inductors are used in this design and the frequency synthesizer occupies an area of  $1900\mu\text{m}\times 1900\mu\text{m}$ , this is mainly dominated by the output pad and a large region on the chip is filled with dummy metal, poly and oxide required to raise the yield rate; subsequently, base-band circuits can be further combined and drawn in place of the region of dummy layers.

The frequency synthesizer is tested under 1.5-V supply, except the supply voltage of VCO frequency being adjusted lower due to the oscillating frequency drift, The measurement result shows that the frequency range shift down about 350 MHz, but the tuning range is similar than simulation and the VCO frequency meet requirement. This work is measured and has the following performances. The in-band spurious signals of Group #1~ Group #5 are measured after adjust the bias voltages. The worst case occurs in the first group, the measurement result about -30.6dB. Then out-band spurious measurement result about -40dB. The phase noise is -106dBc/Hz @1MHz offset, locking time is 600ns and switching time is 3.75ns(From Group 5 to Group 1). The total power consumption is 55.1~161.62mW. The power consumption mostly increases in mixer to compensate the loss of the parasitic resistors and caps.

## 5.2 Future work

The proposed frequency synthesizer for UWB applications could be fabricated again with the cut MIM-caps in VCO by adjusting the center frequency. This would help provide the required carriers for entire UWB bands. Furthermore, for more thorough and complete frequency synthesizer design, the MUX output test buffer can be included, to avoid signal become smaller and current consumption more large. The large current consumed also appears in other functional block of the UWB frequency synthesizer, the summary of current consumed as shown in Table. 4.2 For lower battery operation, this frequency synthesizer must reduce its current consumed. It also appears the poor performance of spurious tone, which is  $-30.6 \text{ dBc@ } 3432\text{MHz}$ . The reasonable value is smaller.

Finally, a full understanding of UWB system and a more careful consideration are essential to design and implement a frequency synthesizer for UWB applications. There is still large improvement available in this design.



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