

NROM 資料保存能力之研究

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摘 要

當快閃記憶體的發展邁向十億位元領域的同時也面臨到許多的挑戰，這些挑戰限制了元件面積的縮小。傳統的浮動閘快閃記憶體所面臨的最大挑戰就是穿隧氧化層的厚度無法再做進一步的微縮，根據記憶體元件的物理特性與電性特性研究，再使用外差法來推算，浮動閘快閃記憶體的製程極限大約可以到達 45 奈米。與浮動閘快閃記憶體相比之下，SONOS 結構的快閃記憶體擁有較佳的製程微縮能力與簡單的製程。SONOS 結構的快閃記憶在經過資料的寫入與抹除的操作之後，在寫入的狀態下會發現到電荷的損失，而在抹除的狀態下會發現到電荷的增加。這些變化都會影響記憶體元件資料保存的正確性。

本論文研究 NROM(Saifun 公司所發明的 SONOS 結構的快閃記憶體)在抹除狀態下如何降低儲存電荷的增加。在研究中我們發現到護層中的水氣是影響抹除狀態時電荷增加的關鍵。製程中殘留的水氣會加速熱電子效應所導致的元件退化，熱電子效應會使得被補抓在底層氧化層中的正電荷增加。所以我們藉由降低護層中的水氣含量以及避免水氣擴散到元件這兩種方式來改善抹除狀態時的電荷增加。

在降低水氣含量的實驗中，我們發現在 SAUSG 沉積之後將晶片在 420 °C 的溫度下烘烤 30 分鐘可以讓抹除狀態的臨界電壓飄移由 1.6V 降低為 0.2V。即使在較差的護層結構下也可以得到相當好的資料保存能力的改善。

在避免水氣擴散到元件的實驗中，將第一層護層的材料由低功率電漿化學沉積的二氧化矽換成氮化矽可以讓臨界電壓飄移由 1.6V 降低為 0.3V。將介層阻障層中鈦的厚度由 15 奈米增加到 40 奈米可以讓臨界電壓飄移由 1.7V 降低為 0.3V。綜合這兩種改善，不但可以讓臨界電壓飄移維持在 0.3V 以下，還可以使沒有產生臨界電壓飄移的實驗樣本超過 30%。

在這些實驗中，抹除狀態下的電荷增加可以獲得大幅改善。這些改善使得元件在經過寫入與抹除的操作之後，讀取“1”的資料空間變得更大，進而改善了資料保存能力。使得 NROM 有機會從多次寫入的記憶體變成真正的快閃記憶體。

The Study on Data Retention of NROM

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ABSTRACT

As flash memories move toward giga-bits era, several challenges limit their scalability. The major problem of floating gate flash memories is un-scalable tunnel oxide. Although SONOS (Silicon Oxide-Nitride-Oxide Silicon) type flash memories show better scalability and simpler process, there are still some difficulties. Both charge gain at erase state and charge loss at program state after cycles will diminish read window and finally decrease data retention after cycling.

In this study, charge gain at erase state was investigated. In the investigation, we found moisture in passivation layer is the key factor to affect charge gain at erase state. The moisture will increase positive charge trapped in bottom oxide of NROM (NROM is a registered trademark of Saifun) memory. Reduce moisture in passivation layer and prevent moisture diffuse to memory cell is investigated to reduce charge gain at erase state.

To reduce moisture in passivation layer, we bake experiment wafer at 420 °C for 30min after SAUSG (Sub Atmosphere Undoped Silicate Glass) film deposition. The threshold voltage shift at erase state can decrease from 1.6V to 0.2V even with worst passivation film structure.

To prevent moisture diffuse to memory cell, change first passivation film material from low power plasma enhanced oxide to silicon nitride can reduce erase state threshold voltage shift from 1.6V to 0.3V. Increasing titanium thickness in via barrier from 15nm to 40nm can lower threshold voltage shift from 1.7V to 0.3V. Combine passivation film modify and increase titanium thickness not only threshold voltage shift can keep under 0.3V no threshold voltage shift samples also can exceed 30%.

Charge gain at erase state was greatly improved in these investigates. The enlarged of read "1" window can improve data retention after cycling and make NROM cell has chance from multi time programming become true flash.

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Contents

Chinese Abstract	i
English Abstract	ii
Acknowledgement	iii
Contents	iv
Table Captions	vi
Figure Captions	vii
Chapter 1 Introduction	1
1.1 Background	1
1.2 Motivation	3
1.3 Thesis organization	4
Chapter 2 Device Fabrication and Basic Operation Mechanism	5
2.1 Device Fabrication	5
2.1.1 Well Engineering	5
2.1.2 Active Region Engineering	6
2.1.3 Memory Cell Engineering	7
2.1.4 Logic Circuit Engineering	8
2.1.5 ILD and Metal layer Engineering	9
2.1.6 Passivation Engineering	9
2.2 Basic Operation Mechanism of NROM	10
2.2.1 Program Mechanism of NROM	10
2.2.2 Erase Mechanism of NROM	11
2.2.3 Read Mechanism of NROM	12
Chapter 3 Experiment and Discussion	14
3.1 Data Retention Mechanism	14
3.2 Passivation Process Experiments	15
3.2.1 Introduction	15
3.2.2 Experiment	16
3.2.3 Result and Discuss	18
3.2.3.1 SAUSG vs. HDP	18
3.2.3.2 Varied LP-PEOX Thickness	18
3.2.3.3 LP-PEOX vs. PESIN vs. SION	19
3.2.3.4 Post Annealing	20
3.2.4 Summary	21
3.3 Via Barrier Process Experiment	22
3.3.1 Introduction	22
3.3.2 Experiment	23
3.3.3 Result and Discuss	24

3.3.3.1	Varied Ti Thickness	24
3.3.3.2	Varied TiN Thickness	25
3.3.3.3	H ₂ Partial Pressure	26
3.3.4	Summary	27
Chapter 4	Conclusions	29
References	100
Vita	104



Table Captions

Table 1 : Properties of Silicon Nitride for LPCVD vs. PECVD

Table 2 : Passivation layer experiment condition



Figure Captions

- Fig. 1 : MOS memory tree
- Fig. 2 : MOS and Flash memory structure compare
- Fig. 3 : Floating-gate MOSFET reading operation
- Fig. 4 : Threshold voltage distribution for 2b/cell compared with the standard 1b/cell
- Fig. 5 : (a) Cross section and (b) top view of an NROM cell
- Fig. 6 : Band diagram of oxide trapped charge induce barrier lower
- Fig. 7 : Schematics of band diagrams and carrier transport mechanisms at various bias conditions
- Fig. 8 : NROM device fabrication flow, (a) after well engineer and (b) after field oxidization
- Fig. 9 : TEM cross-section of LOCOS field oxide
- Fig. 10 : Dopant segregation at Si/SiO₂ interface
- Fig. 11 : Illustration of Kooi effect
- Fig. 12 : NROM device fabrication flow, (a) after cell S/D implantation and (b) after ONO remove in periphery circuit
- Fig. 13 : NROM device fabrication flow, (a) after gate patterning and (b) after periphery circuit S/D implantation
- Fig. 14 : TEM cross-section of metal film
- Fig. 15 : NROM device fabrication flow - after metal 1 patterning
- Fig. 16 : NROM device fabrication flow – after metal 2 patterning
- Fig. 17 : passivation film structure, (a) Without SAUSG, (b) With SAUSG
- Fig. 18 : NROM device fabrication flow – after pad window opening
- Fig. 19 : Schematics illustration of cross section of NROM cell and the program and erase injected charge distributions
- Fig. 20 : Illustration of hot hole generation mechanism
- Fig. 21 : Equivalent device structure of NROM memory cell
- Fig. 22 : Illustration of NROM cell in read operation
- Fig. 23 : V_t shift versus disturb time of a 10-K P/E cycled cell at various drain biases.
- Fig. 24 : various disturb of NROM device during read operation
- Fig. 25 : V_t shift versus applied gate bias of a 10-K P/E cycled cell
- Fig. 26 : P/E cycle dependence of erase-state V_t drift after 10⁴ sec storage
- Fig. 27 : Read disturb characteristics of a fresh cell and a 10-K P/E cycled cell
- Fig. 28 : Schematic illustration of the cross section of the spatial distribution of the charge before ((a),(b)) and after ((c),(d)) retention bake
- Fig. 29 : V_t compare of SAUSG and HDP experiment in WAT test key

- Fig. 30 : Cell current compare of SAUSG and HDP experiment in WAT test key
- Fig. 31 : Vt shift distribution of SAUSG and HDP experiment after 100 cycles
- Fig. 32 : Illustration of moisture diffusion with first passivation film using LP-PEOX
- Fig. 33 : Vt compare of different LP-PEOX thickness experiment in WAT test key
- Fig. 34 : Cell current compare of different LP-PEOX thickness experiment in WAT test key
- Fig. 35 : Vt shift distribution of different LP-PEOX thickness experiment after 100 cycles
- Fig. 36 : TEM of passivation film structure
- Fig. 37 : Vt compare of different passivation film material experiment in WAT test key
- Fig. 38 : Cell current compare of different passivation film material experiment in WAT test key
- Fig. 39 : Vt shift distribution of different passivation film material experiment after 100 cycles
- Fig. 40 : Illustration of moisture diffusion with first passivation film using Si_3N_4
- Fig. 41 : Vt compare of curing after SAUSG DEP experiment in WAT test key
- Fig. 42 : Cell current compare of curing after SAUSG DEP experiment in WAT test key
- Fig. 43 : Vt shift distribution of curing after SAUSG DEP experiment after 100 cycles
- Fig. 44 : TDS spectra of water desorbed from TiN/Ti/TEOS- O_3 SiO_2 , with various Ti thickness.
- Fig. 45 : TDS spectra of hydrogen desorbed from TiN/Ti/TEOS- O_3 SiO_2 , with various Ti thickness.
- Fig. 46 : Depth profiles of Ti 2p XPS-spectra for TiN/Ti/TEOS- O_3 SiO_2 , before and after TDS measurement, (a)before TDS measurement, (b)after TDS measurement
- Fig. 47 : Depth profiles of O 1s XPS-spectra for TiN/Ti/TEOS- O_3 SiO_2 , before and after TDS measurement, (a)before TDS measurement, (b)after TDS measurement
- Fig. 48 : Vt compare of different Ti thickness experiment with old passivation film in WAT test key
- Fig. 49 : Cell current compare of different Ti thickness experiment with old passivation film in WAT test key
- Fig. 50 : Via chain resistance compare of different Ti thickness experiment with old passivation film in WAT test key
- Fig. 51 : Vt shift distribution of different Ti thickness experiment with old

- passivation film after 100 cycles
- Fig. 52 : V_t compare of different Ti thickness experiment with new passivation film in WAT test key
- Fig. 53 : Cell current compare of different Ti thickness experiment with new passivation film in WAT test key
- Fig. 54 : Via chain resistance compare of different Ti thickness experiment with new passivation film in WAT test key
- Fig. 55 : V_t shift distribution of different Ti thickness experiment with new passivation film after 100 cycles
- Fig. 56 : V_t compare of different TiN thickness experiment with old passivation film in WAT test key
- Fig. 57 : Cell current compare of different TiN thickness experiment with old passivation film in WAT test key
- Fig. 58 : Via chain resistance compare of different TiN thickness experiment with old passivation film in WAT test key
- Fig. 59 : V_t shift distribution of different TiN thickness experiment with old passivation film after 100 cycles
- Fig. 60 : V_t compare of different TiN thickness experiment with new passivation film in WAT test key
- Fig. 61 : V_t compare of different TiN thickness experiment with new passivation film in WAT test key
- Fig. 62 : Cell current compare of different TiN thickness experiment with new passivation film in WAT test key
- Fig. 63 : V_t shift distribution of different TiN thickness experiment with new passivation film after 100 cycles
- Fig. 64 : V_t compare of plasma treatment gas partial pressure experiment with old passivation film in WAT test key
- Fig. 65 : Cell current compare of plasma treatment gas partial pressure experiment with old passivation film in WAT test key
- Fig. 66 : Via chain resistance compare of plasma treatment gas partial pressure experiment with old passivation film in WAT test key
- Fig. 67 : V_t shift distribution of plasma treatment gas partial pressure experiment after 100 cycles