Chapter 1

Introduction

1.1 Background

In personal computer system, DRAM (Dynamic Random Access Memory) and SRAM (Static Random Access Memory) are the most using memory type. DRAM has the most output value of memory industry and is the important role to push semiconductor process scaling down. But data storage in DRAM and SRAM will be lost after system power off. These memory types are also classified as volatile memory. Comparison to violate memory, another memory type is nonvolatile memory, which can keep data in memory cell even when system power off. This category of memory includes ROM (Read Only Memory), PROM (Programmable Read Only Memory), EPROM (Erasable Programmable Read Only Memory), EEPROM (Electrically Erasable Programmable Read Only Memory) and Flash [1] as Fig. 1. In nonvolatile memory group, flash memory has the most applications and market. Nonvolatile memory has been used in a number of applications, such as communication (cellular phones, modems, set top boxes), consumer (digital cameras, mp3 players, games), computer and peripherals (desk top personal computers, notebooks, hard disk drives), and transportation (automotive).

The basic structure of flash memory is similar with MOSFET (Metal Oxide Semiconductor Field Effect Transistor). The difference between flash memory and MOSFET is flash memory has a floating gate between control gate and substrate channel [1], as Fig. 2. When charge was injection into floating gate, threshold voltage of memory cell will be changed. The difference of threshold voltage can be analyzed as data storage in memory cell, as Fig. 3. If charge can

be sealed in floating gate without lost, data will be kept in memory cell even when power is removed from system.

To fabricate larger capacity flash memory with acceptable yield, process must be scaling down to get reasonable die size. But scaling down for conventional floating gate flash memory is difficult, because reliability problem will limit tunnel oxide thin down. Some idea for multi bits per cell is investigated. Intel's MLC (Multilevel Cell) is one of the solutions to realize multi bits per cell [2-4]. The principle of MLC is to control precision charge amount injection into floating gate. Different amount of charge in floating will cause different degree of threshold voltage shifting. Different degree of threshold voltage shifting means different data storage in floating gate as Fig. 4.

Saifun's NROM (NROM is a registered trademark of Saifun) is another technology to realized multi bits per cell [5-7]. NROM memory cell is base on SONOS (Silicon Oxide-Nitride-Oxide Silicon) memory structure. The role of nitride film is same as poly floating gate in conventional flash memory as charge storage layer. Charge in nitride layer is trapped and cannot move as in poly floating gate. After charge is injection into separate position in nitride layer as Fig. 5, data in NROM cell can be analysis by reverse read method. In NROM memory cell, 4 bits/cell can be achieved by combination with 4 levels MLC. In conventional floating gate structure flash memory, to achieve 4 bits/cell, sixteen difference threshold voltage levels are needed and more difficult to realize than NROM cell.

NROM fabrication process flow is simple and many process stages are same as CMOS (Complement Metal-Oxide-Semiconductor) process except ONO (Oxide-Nitride-Oxide) engineering process. So NROM device can integrate with CMOS logic circuit more easily than conventional floating gate flash memory. Another advantage of NROM memory cell than conventional flash memory cell is more immunity against point defects in tunnel oxide. In conventional flash

memory cell, floating gate can be thought as a conductor. If any point defects in tunnel oxide will lower barrier potential and charges in floating gate will leak out through point defects more easily as Fig. 6. In NROM memory cell, charge is trapped by trapping center in nitride layer and will be fixed. Only small amount of charge may leak out through point defects.

1.2 Motivation

Although NROM memory cell has many advantages than conventional flash memory, NROM memory cell still has some problems to be solved. The worst problem is poor data retention ability. Bottom oxide of NROM memory cell will trap positive charges after more than 10 program/erase cycles. The positive charges in bottom oxide will assist electrons injection into nitride layer in normal read operation or positive charges will de-trap from bottom oxide [8-11] as Fig. 7. These two behaviors will cause net charge in nitride more negative. The threshold voltage of erased memory cell will increase then cause read “1” window more narrow. The worst case will cause data sensing circuit can not judge data in memory cell and induce reliability problem.

This paper will investigate data retention ability improvement base on not change front-end process and memory cell electric characteristic. In our investigation, moisture in SAUSG (Sub Atmosphere Undoped Silicate Glass) is the major factor to degrade data retention ability of NROM memory cell. The change of passivation layer engineering and passivation layer structure can greatly improve threshold voltage shift after program/erase cycling. Another improvement is via barrier modification. Thicker Ti in via barrier engineering also can eliminate threshold voltage shift. Data retention improvement by increasing Ti thickness is not as obvious as modify passivation process or passivation structure. But combination of via barrier and passivation process modification can further improve data retention of NROM memory cell. To

improve data retention, reduce moisture source and prevent moisture diffuse to memory cell is the key point.

1.3 Thesis organization

In chapter 2, we will introduce fabrication process flow and basic operation mechanism of NROM memory cell. The basic operation mechanism of NROM memory cell will include data programming into memory cell, erasing from memory cell and how to read data from NROM memory cell.

In chapter 3, some factors that affect data retention of NROM device will be discussed. Data retention improvement experiments including passivation process and via barrier process will also be discussed.

In chapter 4, conclusion of data retention improvement experiments result will be performed.

Chapter 2

Device Fabrication and Basic Operation Mechanism

2.1 Device Fabrication

The NROM device used in this investigation is fabricated with 1P2M 0.25 μm CMOS compatible process. The extra fabrication flow of NROM device is ONO process before gate oxidation. The ONO module in NROM device is data storage material as floating gate in conventional flash memory and decides channel length of NROM memory device. The channel length of NROM memory device is 0.49 μm and pitch is 0.88 μm. Besides memory array in prime die, WAT (wafer acceptance test) test key in scribe line also has same CD (Critical Dimension) and structure as memory array to monitor memory cell characteristic. In the followed experiments, test key performance need to be monitor to confirm experiments has no influence to memory cell characteristic. The followed sections will detail describe fabrication flow of NROM device.

2.1.1 Well Engineering

Silicon wafer resistance of this studying is P-type 8~12 $^{\Omega}/_{\square}$. Crystal orientation of wafer material is (100). At first, we use thermal oxidation method to grow 20nm Oxide as screen oxide. The screen oxide has three purposes as being used here. First purpose of screen oxide is to define global alignment mark for lithograph process and second purpose is to avoid wafer contamination by photo-resist. The other purpose is as an amorphous layer to eliminate channeling effect of Ion Implantation. After screen oxide growth, photo-resist is coating on silicon wafer and Stepper is used to define N-type well region. To formation N-well, phosphorous is injected into silicon substrate by Ion Implantation and Drive in process is followed to activation dopant and get expected well depth.

When N-well engineering is complete, P-type well with Boron doping is fabricated at the same way. Well engineering is complete after P-well drive in process as Fig. 8(a).

When memory cell in program/erase operation, voltage more than 10 volts may be used. Lightly doped P-well for higher junction breakdown voltage is needed and the solution of NROM fabrication is place P-well in N-well region. Some p-type dopant will be compensated by n-type dopant then lightly doped P-well is formed.

2.1.2 Active Region Engineering

Active region is the place which memory cell and logic circuit located. First step for active region engineering is to strip screen oxide by HF dip. After HF wet etching, 20nm pad oxide by thermal oxidation is grown in high temperature furnace followed by 140nm CVD (Chemical Vapor Deposition) silicon nitride deposition.

Silicon nitride is used as hard mask for active region define and to eliminate field oxide encroaching on active region. CVD silicon nitride has a high tensile stress on the order of 10^{10} dynes/cm^2 as Table 1. If silicon nitride is used as hard mask only, high tensile stress of silicon nitride will easily induce substrate dislocation. Substrate dislocation will cause junction leakage current high and induce device function fail. A buffer layer is necessary to compensate stress of silicon nitride and silicon dioxide is selected as such purpose. Silicon dioxide has bad ability to block oxygen or water. Oxygen and water will encroach on active region from hard mask sidewall at field oxidation process. The phenomenon of encroachment on active region edge is called Bird's beak as Fig. 9. The Bird's beak will reduce active region and diminish circuit area. The ratio of pad oxide and silicon nitride is in the range 1:5 to 1:10. Thinner pad oxide can reduce Bird's beak effect but will increase silicon nitride stress remaining.

After pad oxide and silicon nitride is formed. Lithograph and etching is

performed to define active region on hard mask. Before field oxidation process, boron is injected into P-well region by Ion Implanter as Channel stop Implantation.

Solid solubility of boron in oxide is higher than in silicon. In thermal oxidation process, silicon will be oxidized and boron in silicon will diffuse to oxide. The segregation of boron will cause boron concentration low at silicon/oxide interface as Fig. 10. The low boron concentration at silicon/oxide interface will make field device turn on more easily. Channel stop Implantation will inject more boron to pull up boron concentration at silicon/oxide interface to avoid circuit function fail by parasitic field device turn on.

After Channel stop Implantation, high temperature furnace is used to thermal oxidation 600nm field oxide then silicon nitride hard mask is removed by phosphoric acid dip and cross-section is as Fig. 8(b). Field oxidation process of NROM is same with CMOS LOCOS (Local Oxidation) process. In field oxidation process, NH_3 is generated from the reaction between water and silicon nitride. NH_3 will penetrate pad oxide and react with silicon to form silicon nitride spots or ribbon in active region. Chemical reaction formula is as below:

$$Si_3N_4 + 6H_2O \rightarrow 3SiO_2 + "4NH_3"$$

$$3Si + "4NH_3" \rightarrow Si_3N_4 + 6H_2$$

The phenomenon is named Kooi effect, as Fig. 11. Silicon nitride on silicon surface in active region will eliminate follow-up oxidation process. Unexpected thinner oxide will be formed if Kooi effect is not removed. Sacrificial oxide is the general solution for removing Kooi effect after field oxidation process.

2.1.3 Memory Cell Engineering

After sacrificial oxide process, cleanly silicon surface is got and then 5nm thermal bottom oxide is formed by high temperature furnace. When bottom oxide is formed, 13nm silicon nitride is deposited and 6nm top oxide is formed by oxidation silicon nitride. The final O-N-O thickness is 5nm, 7nm and 6nm

respectively. Channel length is then defined by lithograph.

Before ONO etching process, large angle Pocket Implantation with boron is performed. Pocket Implantation in memory cell has two major purposes. First is to enhance program and erase efficiency by increase electric field under channel edge. Second is to raise punch through voltage. When Pocket Implantation process is finished, etching process is used to define channel length of memory cell on ONO film. Then source/drain is engineering by high dosage arsenic implantation and cross-section is as Fig. 12(a).

NROM device only use N-type poly silicon as gate electrode. Threshold voltage of NMOS and PMOS mismatch will appear. Low dosage BF_2 implantation is used solve threshold voltage mismatch of NMOS and PMOS. After threshold voltage adjusting implantation, ONO film on periphery circuit region is removed by dry etching and cross-section is as Fig. 12(b). Then gate oxide is thermal growth by dry oxidation. N-type poly silicon and WSi_2 is deposited after gate oxidation. Lithograph and etching is used to define gate electrode pattern and cross-section is as Fig. 13(a).

2.1.4 Logic Circuit Engineering

As critical dimension scaling down, hot carrier effect will be enhanced due to channel length scaling down. LDD (Lightly Doped Drain) structure is used to solve the problem. First step to engineer LDD structure is to provide low dosage n-type ion implantation for NMOS and p-type ion implantation for PMOS after poly etching. Then 230nm LPTEOS (Low Pressure Tetraethylorthosilicate) is deposited and followed by anisotropic dry etching to form oxide spacer. Then high dosage n^+/p^+ implantation for S/D (Source/Drain) engineering is executed and cross-section is as Fig. 13(b).

2.1.5 ILD and Metal layer Engineering

After device was fabricated, ILD (Inter Layer Dielectric) is engineering to isolate device and metal interconnection layer. In ILD engineering, 200nm USG

(Undoped Silicate Glass) is deposited first and followed by 1.1um BPSG (Borophosphosilicate Glass) deposition. Boron and Phosphorous concentration in BPSG is 5wt% each. The concentration of BPSG dopant is high enough to affect device electric characteristic. USG is used as buffer layer between BPSG and device. In advance process, thin silicon oxynitrides and silicon nitride layer is also used to replace USG as buffer layer.

After BPSG reflow and etch back, contact hole was etched. Before tungsten plug was deposited, Ti/TiN as barrier layer was deposited by CVD. After contact barrier engineering, CVD tungsten is deposited and tungsten etch back is performed to remove excess tungsten. Then Al-Cu and TiN is deposited to form metal interconnection.

In metal interconnection engineering, if Al is used as metal line only, serious EM (Electromigration) will happen easily. There are two ways to improve EM of metal line. First is adding heavy metal in pure Al such as Cu. Second is adding hard layers at Al layer top and bottom as sandwich structure. TiN is usually used as cap layer to improve EM of metal line, as Fig. 14. Another purpose of top TiN is to be ARC (Anti Reflection Coating) for followed lithograph process. After first metal layer was patterned by lithograph and etch process, the cross-section is as Fig. 15. The IMD (Inter Metal Dielectric) layer is engineering to isolate metal layers and via is engineering to provide interconnection of metal layers. Fig. 16 is the cross-section after second metal layer patterning.

2.1.6 Passivation Engineering

After device and metal interconnection engineering is complete, passivation layer is deposited to provide protection of moisture or alkali metal contamination from environment. PESIN (Plasma enhanced chemical vapor deposition silicon nitride) provide excellent protection ability to moisture and alkali metal and usually to be used as passivation layer. But step coverage ability

of silicon nitride is bad with 800nm top metal. Using silicon nitride as passivation layer only will easily induce void in passivation film. Void in passivation film will contain EKC solution easily in the following wet strip process and to induce reliability problem.

To get void free passivation film, SAUSG or SOG (Spin on Glass) is usually used to fill-in metal gap. Fig. 17(a) is TEM (Transmission Electron Microscope) graph of passivation layer without SAUSG and Fig. 17(b) is passivation layer with SAUSG. In the TEM graph, we can find out serious void problem in passivation layer without SAUSG and add SAUSG in passivation layer can greatly improve void problem. SAUSG or SOG is easily to absorb moisture. For reliability concern, low power plasma enhanced chemical vapor deposition oxide is deposited under SAUSG film to isolate SAUSG and metal layer. Finally, when passivation film deposition is completed, lithograph and etch process is performed to open bonding pad and H_2 sintering alloy is performed to reduce metal resistance. The final device cross-section is as Fig. 18.

2.2 Basic Operation Mechanism of NROM

2.2.1 Program Mechanism of NROM

NROM memory cell is programming by CHE (Channel Hot Electron) injection. Hot electron injection occurs when electrons are accelerated to a high enough energy level to surmount bottom oxide barrier. There are several mechanisms that may accelerate the electrons, but acceleration of electrons by lateral fields in the channel is the only hot electron mechanism that is currently used by flash memories for programming. For efficient programming, the transistor should be biased in saturation region so that a high lateral electric field is created in the depletion region near pinch-off point. When drain side of transistor is biased at high voltage, the channel inversion layer is wider near the source and narrows as it approaches the pinch-off point. As the electrons pass

through the pinch-off point, they are strongly accelerated in the high field of the drain depletion region. Some of the hot electrons are scattered in a direction such as to reach the Si/SiO_2 interface. The shape of the SiO_2 barrier varies along the channel length because the potential along the channel varies from source to drain while the gate potential remain constant.

The highest density of hot electrons is toward the drain, where the oxide field is repulsive. Near the source, where the oxide field is very strongly collective, there are almost no hot electrons. Only near the pinch-off point can hot electrons and a collecting oxide field be found in conjunction. Because only a small portion of the channel length is effective for programming, the programming efficiency is rather low.

To program drain bit of NROM memory cell, drain side is provided 5V and control gate is biased at 11V. Electrons are accelerated from source side toward drain side by electric field in channel. As in Fig. 19, electrons will gain enough energy during acceleration to tunnel bottom oxide then injection into silicon nitride layer when near drain side junction [5,12]. If higher voltage is provided on drain side or on control gate, more electrons will gain enough energy to tunnel bottom oxide. With increase of bottom oxide thickness, tunneling rate of hot electron will decrease and then increasing programming time.

During programming of a NROM memory cell, the gate is biased to 11V. The other erased memory cells with same gate electrode will subject to a considerable electric field across bottom oxide, which may lead to an unwanted threshold voltage shift. The phenomenon is named gate disturb. The gate disturb will induce charge gain in erased memory and charge loss in programmed memory cell then induce data error in memory cells.

2.2.2 Erase Mechanism of NROM

Erasing data in NROM memory cell is achieved by band-to-band HHI (hot holes injection). Under the conditions in which the vertical field at the silicon

surface is high (>0.8MV/cm) and surface potential drop is larger than the silicon band gap energy (1.12eV), electrons and holes are generated by the tunneling of electrons from the silicon valence band into the conduction band. This process occurs predominantly in an area close to the p-n junction, where the surface doping of the n+ region is ~5×10^{18} atoms/cm^3.

In HHI Erase operation, the generated holes flow toward the p-type substrate and injection into charge storage layer by vertical field when negative bias is applied on gate electrode. In particular, the holes that flow through the surface depletion region are heated by the electric field across the junction and become “hot”. Because this current is produced by band-to-band tunneling process, it is referred to as the band-to-band tunneling current. Therefore, this current exhibits only a weak dependence on temperature.

In Erase operation, -3V is applied on gate electrode and 8V is applied on drain side. Under this condition, hole flow is generated by band-to-band tunneling in deep depletion region in drain side junction, accelerated by lateral electric field and then injection into nitride layer by vertical electric field [5]. Fig. 20 is hot holes generation mechanism.

Some of hot holes are injected into bottom oxide in hot-hole erase step and become trapped there. Trapped holes in the oxide have been showed to affect the data retention of the memory cell.

When memory cell in hot-hole erase step, most of hot holes injection into nitride layer will not recombine with electrons [12-14]. Initially the electrical neutralization of holes and electrons is the major mechanism. Holes are known to be more mobile in the nitride layer than electrons [15]. When holes are injected into a negatively charged nitride layer they will spread fast to erase the negatively charged bit.

2.2.3 Read Mechanism of NROM

The architecture as reverse read is used in NROM memory read operation.

The NROM memory cell can be considered as three transistors in series as show in Fig. 21. Center transistor only plays the part of channel. Left and right transistors play the roles as data storage cell. Fig. 22 is the illustration of reverse read mechanism. Assume data storage in right bit is programming. To read data in right bit, 1.6V is applied on left side and no current flow will be sensed which indicate data is “0”. To read data in left bit, 1.6V is applied on right side and induced depletion region will cover the region which threshold voltage higher then standard. The current flow then will pass through programmed bit and be sensed at left side. The current sensed at left side indicate data in left bit is “1”.

When source side data will be read, 2.5V gate bias and 1.6V drain bias is applied. The applied drain bias will induce lateral electric field and accelerate electrons in channel. The accelerated electrons will inject into nitride layer by vertical field then cause threshold voltage shift. The phenomenon will be more obviously when reverse side is “1” state and is known as Soft-Write [16]. Soft-Write in read operation will be more serious when applied bias is higher or read period is longer [8], as show in Fig. 23.

When selected memory cell undergo read disturb, unselected memory cell will suffer gate disturb at same word line and drain disturb at same bit line as Fig. 24. The gate disturb induce threshold voltage shift will be more serious with higher gate bias as Fig. 25. Under higher gate bias, vertical field cross ONO stack film will be higher. The higher vertical field will let electrons injection from substrate to nitride layer more efficiency and finally increase memory cell threshold voltage. The increased threshold voltage will induce read “1” margin loss then cause data retention problem.

Chapter 3

Experiment and Discussion

3.1 Data Retention Mechanism

Threshold voltage shift of NROM memory cell will proportional to program/erase cycles as Fig. 26. When reading data in memory cell, bias condition is similar with program step but bias level is lower. As in Fig. 27, during read operation, memory cells undergo slight channel hot electron injection. The amounts of electron injection into nitride layer increase while read operation time increasing and finally induce memory cell threshold voltage higher.

In the report by M. Janai *et al.*, memory cell threshold voltage shift is mainly caused by charge redistribution [17]. As in Fig. 28(a), Negative and positive charges exist individual and do not disappear by charge recombination. The holes distribution is narrow than electrons. Fig. 28(b) is net charge distribution after memory cell erase operation. After long time baking, charge in nitride layer will redistribute as Fig. 28(c), and net charge in nitride layer will be more negative as Fig. 28(d) then causes threshold voltage higher.

In the report by W.J. Tsai *et al.*, the mechanism to cause data retention problem is positive charge assisted tunneling [8]. When positive charge is trapped in bottom oxide of ONO layer, it will assist electron tunneling into nitride layer or positive charge will de-trap from bottom oxide. The final net charge in nitride layer will be more negative. The increased oxide trap charge is believed caused by oxide damage during program/erase operation [18,19]. The phenomenon is named “hot carrier degradation” and is suitable to explain the result of experiments.

The hot carrier degradation will generate interface state and increase

oxide-trapped charge during program/erase operation. The increasing of oxide trapped charge is thought to assist electron injection into nitride layer more easily during gate disturb and read disturb. The positive oxide charge detrapping also increases net negative charge in nitride layer. Both positive charge assisted tunneling and positive charge detrapping from bottom oxide will cause threshold voltage shift.

It is well known that using silicon nitride passivation layer will enhance hot carrier degradation [20,21]. The hydrogen diffusion model [22-24] and water diffusion model [25,26] have been proposed as the probable mechanism to enhance hot carrier degradation. Base on the report of M. Shimaya *et al.* [21], water diffusion model is the most possible mechanism to explain hot carrier degradation in this study. Base on water diffusion model, moisture reduction in passivation layer or prevent moisture diffuse to memory cell is needed to eliminate hot carrier degradation.

3.2 Passivation Process Experiments

3.2.1 Introduction

Silicon nitride is widely used as passivation film, since it has excellent endurance to water penetration and immunity to contamination from environment. But silicon nitride has bad step coverage ability and void is easily formed during passivation film deposition. The void in passivation film will cause some reliability problem and need avoid. To solve silicon nitride bad step coverage problem, SAUSG is used to fill-in metal gap before silicon nitride film deposition. Since SAUSG is easily to absorb moisture if expose to environment, the LP-PEOX (low power plasma enhanced chemical vapor deposition oxide) is deposited under SAUSG to avoid moisture in SAUSG react with metal.

Moisture in SAUSG is thought the source to cause hot carrier degradation in memory cell [20]. To reduce moisture in SAUSG film, some modification of

passivation layer process is needed. In experiments of reducing moisture in passivation layer, using SAUSG and HDP (high-density plasma) oxide as metal gap fill-in is studied. Beside moisture reduction in metal gap fill-in material, some material of first passivation film is also studied to eliminate remaining moisture penetrate first passivation film then diffuse to memory cell. The PESIN, SION (silicon oxynitrides) and LP-PEOX as first passivation film material is studied in this experiment. The conditions of passivation process experiments are list as Table 2.

3.2.2 Experiment

In PESIN deposition process, SiH_4 and NH_3 are used as deposition material. The gas flow of SiH_4 is 184 sccm and NH_3 is 160 sccm. During PESIN deposition, high frequency RF (radio frequency) power is 515W and low frequency RF power is same as high frequency. Under above condition the deposition time of 200nm silicon nitride is 21 sec and 700nm silicon nitride is 73 sec.

In LP-PEOX deposition process, reaction gas is SiH_4 and N_2O. The flow rate of SiH_4 is 25 sccm and N_2O is 900 sccm. High frequency RF power is 100W and low frequency RF power is turn off in LP-PEOX deposition. The deposition time of 100nm LP-PEOX is 20 sec, 200nm LP-PEOX is 41 sec and 300nm LP-PEOX is 60 sec.

In SAUSG deposition process, system is waiting for stable in first 2 sec and turn on TEOS gas flow. Next step is SAUSG deposition. At this step, process chamber pressure is set at 450 torr. Reaction gas flow of TEOS is 335 sccm and O_3 is 5000 sccm. The deposition time of 700nm SAUSG is 210 sec.

Two-step deposition is performed in HDP oxide deposition. In first deposition step, reaction gas flow of SiH_4 is 99 sccm and O_2 is 157 sccm. Low frequency RF power is 3500W and high frequency RF power is turn off in this step. The deposition time of first step is 2 sec and no ion bombardment will be

performed at this step. After first step, thin liner oxide will be deposited to protect sidewall of under layer from ion bombardment damage. In second deposition step, gas flow setting is same as first step. Low frequency RF power is 3500W and high frequency RF power is 2700W. The deposition time of second step is 75 sec. Etch and deposition ratio must be well controlled to get better gap fill-in and avoid under layer profile damage.

In SION deposition process, reaction gas flow of SiH_4 is 250 sccm and N_2O is 450 sccm. High frequency RF power is 470W and low frequency RF power is 430W. Under above condition the deposition time of 200nm SION is 13 sec.

The post annealing process after second passivation film deposition is processing in furnace. After wafer is loaded into furnace the temperature is ramp up from 250℃ to 420℃. To avoid serious temperature overshot, two-step temperature ramp up is performed. In first ramp up step, temperature is ramp up from 250℃ to 370℃ in 42 min and ramp up rate is 3℃/min. After 3 min temperature stable step, second ramp up is performed and temperature is ramp up again from 370℃ to 420℃ with ramp up rate 5℃/min. After 30 min 420℃ curing, two-step temperature ramp down is performed. The two-step temperature ramp down is applied to avoid passivation film crack after fast temperature change. Temperature ramp down in first step is from 420℃ to 400℃ and ramp down rate is 2℃/min. Temperature in second step is ramp down from 400℃ to 250℃ and ramp down rate is 5℃/min. After furnace temperature is stable at 250℃ then wafer is unloaded.

The samples for data retention test are 64mega bits density NROM memory cell and amount of each experiment condition samples are different. So normalize data is aligned to compare experiment result more fair. The data retention test is designed to find out maximum threshold voltage shift at erase state in 64mega bits memory cells after 100 program/erase cycles.

3.2.3 Result and Discuss

3.2.3.1 SAUSG vs. HDP

To get better metal gap fill-in ability, SAUSG is used as second layer in passivation structure. When SAUSG is exposed in environment, SAUSG will absorb moisture easily. The moisture in SAUSG is thought to cause memory cell threshold voltage shift [20].

The HDP oxide is usually used for gap fill-in in inter-meter-dielectric layer or STI (shallow trench isolation) fill-in process. This experiment is to find out if second layer of passivation film change from SAUSG to HDP oxide can reduce amount of moisture. In this experiment, bottom passivation film is 200nm LP-PEOX, second passivation film material including SAUSG and HDP oxide and thickness is 700nm. Top passivation film is 700nm PESIN.

Total amount of SAUSG samples are 701 dies and HDP samples are 752 dies. In WAT testing, no obvious electrical performance difference is found between SAUSG and HDP oxide samples. The memory cell current of HDP oxide samples is 2uA slightly lower than SAUSG samples as Fig. 29 and Fig. 30. The cell current difference is come from geometry and process difference. The data retention test result is as Fig. 31. Threshold voltage shift of samples with SAUSG film is between 0.8V to 1.6V and maximum shift is at 1.1V. Threshold voltage shift of samples with HDP oxide film is between 0.8V to 1.7V and maximum shift is same as SAUSG samples. No obvious threshold voltage shift difference is found between SAUSG and HDP in data retention test. Base on the experiment result, change second passivation material from SAUSG to HDP is no improvement to threshold voltage shift.

3.2.3.2 Varied LP-PEOX Thickness

The moisture in second passivation layer such as SAUSG is thought to cause memory cell threshold voltage shift. When H_2 sintering Alloy is applied after top passivation film deposition, moisture in SAUSG is hard to dissipate out

from passivation film. The moisture will be blocked by top PESIN and penetrate first passivation film such as LP-PEOX then diffuse to memory cell [20], as Fig. 32.

The experiment of varied LP-PEOX thickness is to find out if thicker LP-PEOX can improve moisture-blocking ability. In this experiment, bottom passivation film is different thickness of LP-PEOX, second passivation film is 700nm HDP oxide and top passivation film is 700nm PESIN. Total amount of 200nm LP-PEOX samples are 701 dies, 100nm LP-PEOX samples are 523 dies and 300nm LP-PEOX samples are 602 dies. As Fig. 33 and Fig. 34, memory cell threshold voltage and cell current have no obvious difference which indicating modification LP-PEOX thickness is no impact to memory cell electrical performance. The data retention test result is as Fig. 35. Threshold voltage shift distribution of 100nm LP-PEOX is from 0.9V to 1.6V. The distribution of 200nm LP-PEOX is from 0.8V to 1.6V and 300nm LP-PEOX is from 1.2V to 1.7V. Data retention performance of 100nm and 200nm LP-PEOX almost has no difference. The LP-PEOX with 300nm thickness shows worst data retention performance than thinner oxide film. In LP-PEOX deposition process, no ion bombardment is performed. So LP-PEOX film is not as dense as PEOX and is thought to absorb moisture easily than PEOX. Increase LP-PEOX thickness to improve moisture-blocking ability is not effective as expect. To improve moisture-blocking ability, the change of first passivation film material is needed.

3.2.3.3 LP-PEOX vs. PESIN vs. SION

The origin first passivation film of NROM memory device is 200nm LP-PEOX. The previous experiment has show that thicker LP-PEOX does not have good moisture-blocking ability. To get better moisture-blocking ability, change first passivation film material is needed for data retention improvement.

Since PESIN has excellent moisture-blocking ability. Thin PESIN is chosen as first passivation film material in this experiment. Because the stress of PESIN

exceeds 10^9 dynes/cm^2 and step coverage ability of PESIN is bad, cross-section check by SEM (Scanning Electron Microscope) of passivation film is needed. As Fig. 36, thin silicon nitride almost has no step coverage problem. Beside PESIN, SION is another material in first passivation film experiment.

In this experiment, first passivation film material is different which include LP-PEOX, PESIN and SION, second passivation film is 700nm SAUSG and top passivation film is 700nm PESIN. Total amount of LP-PEOX samples are 701 dies, PESIN samples are 713 dies and SION samples are 672 dies. As Fig. 37 and Fig. 38, no obvious difference is found in memory cell threshold voltage and current in WAT testing. The data retention test result is as Fig. 39. Threshold voltage shift distribution of LP-PEOX is between 0.8V to 1.6V. The distribution of PESIN is from 0.1V to 0.3V and SION is from 0.1V to 0.2V. First passivation film material using PESIN or SION can greatly improve threshold voltage shift of memory cell after 100 cycles. Because PESIN has excellent moisture-blocking ability, moisture is hard to penetrate first passivation. The moisture may diffuse through metal interconnection then cause hot carrier degradation, as Fig. 40. Since the area of via hole is small compare with whole wafer area, moisture-blocking ability of first passivation film will dominate data retention of NROM memory cell.

3.2.3.4 Post Annealing

Although replacing first passivation film from LP-PEOX to PESIN or SION can get better data retention performance. The moisture source to cause threshold voltage shift is not reduced. The replacement of first passivation film is just to prevent moisture diffuse to memory cell not remove moisture source from device. The moisture in passivation layer may cause reliability problem after more operation cycles. The post annealing after SAUSG deposition and before top PESIN deposition is performed to eliminate amount of moisture in passivation layer which is the source to cause hot carrier degradation.

In post annealing experiment, first passivation film material is 200nm LP-PEOX, second passivation film is 700nm SAUSG and top passivation film is 700nm PESIN. Total amount of no post annealing samples are 701 dies and with post annealing samples are 812 dies. WAT testing result is as Fig. 41 and Fig. 42, memory cell performance has no obvious difference between two conditions. The data retention test result is as Fig. 43. Threshold voltage shift distribution of no post annealing samples is from 0.8V to 1.6V. The distribution of samples with post annealing is from 0V to 0.2V. The experiment data shows that post annealing after second passivation film deposition can greatly improve data retention by dissipate moisture from SAUSG film even using LP-PEOX as first passivation film. After post annealing, if top passivation film is deposited immediately amount of moisture can be guarantee to extremely low degree. The source to cause threshold voltage shift can be eliminated. But after post annealing if top passivation film is not deposited in 24 hrs, SAUSG will re-absorb moisture then another post annealing is needed to dispel moisture before top passivation film deposition.

3.2.4 Summary

In the passivation process experiment, first passivation film using different thickness LP-PEOX or second passivation film using HDP has no improvement of data retention. First passivation film using PESIN or SION shows excellent moisture-blocking ability. The threshold voltage shift can control within 0.3V. To completely solve threshold voltage shift, post annealing after SAUSG deposition can dispel moisture from passivation film effectively and greatly eliminate the source to cause data retention problem even first passivation film material using LP-PEOX.

3.3 Via Barrier Process Experiment

3.3.1 Introduction

In recent VLSI process, Ti and TiN is the most commonly used film for contact or via barrier. The application of Ti is to be an oxygen-getting material and oxide-reducing agent, which dissolve the native oxide layers on silicon surface and to adhere well to both silicon and oxide. In addition, because the Schottky-barrier height of Ti on n-type silicon is about half the silicon band gap, Ti can form good ohmic contacts to both types of heavily doped silicon [27].

TiN is an attractive material as a contact diffusion barrier because the activation energy for the diffusion of other impurities is high. TiN is also chemically and thermodynamically very stable, and it exhibits one of the lowest electrical resistivities of the transition metal carbides, borides, or nitrides [27]. The contacts or via structure consisting of W-TiN-Ti exhibit very low specific contact resistivities and high thermal stability, with the ability to withstand temperatures up to 550℃.

In the report of M. Yoshimaru *et al.* [28], with thicker titanium thickness the amount of moisture measured by TDS (Thermal Desorption Spectroscopy) will be eliminate and amount of hydrogen will be higher as Fig. 44 and Fig. 45. In XPS (X-ray Photoelectron Spectroscopy) measurement, metallic titanium is observed before TDS measurement as Fig. 46(a) and no titanium oxide is measured as in Fig. 47(a). After TDS measurement, the intensity of metallic titanium decreases as Fig. 46(b) and intensity of titanium oxide increases as in Fig. 47(b). It is considered that the titanium layer is to deoxidize water into hydrogen and titanium is oxidized by water.

To reduce hot carrier degradation induce memory cell threshold voltage shift, via barrier experiment of Ti and TiN is studied. Different thickness of Ti and TiN experiment is performed to investigate the relationship between

moisture-blocking ability and thickness of via barrier material. The deposition condition of TiN is also changed to improve moisture-blocking ability.

3.3.2 Experiment

The first step of via barrier process, 300W ion bombardment is applied to clean native oxide on the via hole bottom. The process time of this step is in the range of 35 sec and 20nm of via hole bottom is etched to guarantee no isolate material in via barrier layer and metal interface.

The next step is titanium deposition. In titanium 15nm experiment, DC (Direct current) power and RF (Radio Frequency) power is 2250W and 2750W respectively. The AC (Alternating current) bias is 200W and total deposition time is 12 sec. In the titanium 20nm, 30nm and 40nm experiment, process condition of DC power, RF power and AC bias is same as titanium 15nm experiment. The difference is deposition time of titanium 20nm is 16sec, titanium 30nm is 22 sec and titanium 40nm is 32 sec.

The third step is titanium nitride deposition. The standard sample is heating to 400℃ and wait 60 sec for system stable and gas flow adjustment then titanium nitride deposition is processing. Titanium nitride deposition process time is 10 sec and deposited film thickness is 5nm. Then N_2/H_2 plasma treatment is performed to reduce film resistance. In standard plasma treatment condition, H_2 and N_2 gas flow is 300 sccm and 200 sccm respectively. In comparison experiment, H_2 and N_2 gas flow is 100 sccm and 400 sccm respectively. After plasma treatment, titanium nitride thickness of each deposition cycle is 5nm. The deposition cycle of titanium nitride 10nm is 2, titanium nitride 50nm is 10 and titanium nitride 120nm is 24.

The samples of data retention test are 64mega bits density NROM memory cell and amount of each experiment condition samples are different. So normalize data is aligned to compare the result of experiment more fair. The data retention test after 100 program/erase cycles is the maximum threshold voltage

shift in 64mega bits memory cell.

3.3.3 Result and Discuss

3.3.3.1 Varied Ti Thickness

Ti is the most commonly material in contact or via barrier process, because Ti promotes good adhesion to both oxide and silicon and can form good ohmic contacts to both types of heavily doped silicon. Ti is also an oxygen-gettering material. In the report of M. Yoshimaru *et al.* [28], the ability of Ti to reduce amount of moisture increases with increasing the thickness of Ti. The different Ti thickness experiment is performed to verify the result of reference 26 and check if increase Ti thickness can improve data retention of NROM device.

The first passivation film of test samples use LP-PEOX and no post annealing performed between SAUSG deposition and top PESIN deposition. Total amount of 15nm Ti samples are 592 dies, 20nm Ti samples are 601 dies, 30nm Ti samples are 551 and 40nm Ti samples are 632 dies. Memory cell electrical performance has no difference in WAT testing as Fig. 48 and Fig. 49. Via resistance of different Ti thickness increase proportional to Ti thickness as Fig. 50. Because Ti deposition of via barrier is accomplished by IMP (Ion metal plasma) Ti process, the resistivity of Ti (40 $\mu\Omega$-cm) is higher than that of tungsten (8~12 $\mu\Omega$-cm). So thicker Ti will result higher via resistance.

The data retention test result is as Fig. 51. Threshold voltage shift distribution of 15nm Ti samples are between 1.2V to 1.7V, 20nm Ti samples are between 1.1V to 1.7V, 30nm Ti samples are between 0.1V to 1.2V and 40nm Ti samples are between 0V to 0.3V. Base on experiment data, thicker Ti thickness gets smaller threshold voltage shift. The result of Ti thickness experiment can fit in with the report of M. Yoshimaru *et al.* [28] which further prove that threshold voltage shift of NROM memory cell is caused by water diffusion induce hot carrier degradation.

With first passivation film using PESIN total amount of 15nm Ti samples

are 473 dies, 20nm Ti samples are 493 dies, 30nm Ti samples are 521 and 40nm Ti samples are 596 dies. As in Fig. 52 and Fig. 53, memory cell electrical performance has no obvious difference. Similarly, the via resistance is increasing proportional to Ti thickness as in Fig. 54.

The data retention test result is as Fig. 55. Threshold voltage shift distribution of different Ti thickness is all controlled within 0.3V. No obvious retention difference is found between different Ti thickness except amount of no threshold voltage shift samples. In Fig. 55, the amount of no threshold voltage shift samples increases proportion to Ti thickness. More than 30% of 40nm Ti samples have no threshold voltage shift after 100 program/erase cycles.

The experiment result show that first passivation film material dominate the threshold voltage shift, because via area is below 5% compare to whole chip area. If first passivation film using PESIN, via hole become the major path when moisture diffuse to memory cell. If first passivation film using LP-PEOX, only when via barrier use thicker Ti the local concentration of moisture will be lower at via area then moisture will diffuse toward via by concentration difference (Ti layer can deoxidize water into hydrogen). Under this condition, Ti thickness in via barrier will greatly influence threshold voltage shift.

3.3.3.2 Varied TiN Thickness

The activation energy for the diffusion of other impurity through TiN is high. So TiN has good impurity blocking ability. The different thickness of TiN experiment is performed to check if TiN also has good blocking ability to moisture.

With first passivation film material using LP-PEOX total amount of 10nm TiN samples are 412 dies, 50nm TiN samples are 435 dies and 120nm TiN samples are 471 dies. No obvious difference is found in cell electric performance in WAT testing as Fig. 56 and Fig. 57. Via resistance of different TiN thickness has great difference. As Fig. 58 exceed 10% difference is found

between 10nm and 120nm TiN. TiN deposition in via barrier is accomplished by MOCVD (Metalorganic chemical vapor deposition). The resistivity of MOCVD film is thought higher than sputtering film even after plasma treatment and cause via resistance higher.

The data retention test result is as Fig. 59. The threshold voltage shift distribution of 10nm TiN samples is between 1.2V to 1.7V, 50nm TiN samples is between 1.1V to 1.7V, and 120nm TiN samples is between 0.9V to 1.6V. Base on experiment data, thicker TiN can reduce threshold voltage shift slightly. The TiN also can be a diffuse barrier to moisture but not so effective. To control threshold voltage shift within 0.3V more than 300nm is needed. In actual condition, via dimension of NROM device is 0.48μm and over 120nm TiN in via barrier layer will cause tungsten fill-in problem. The thicker TiN will also rise via resistance and then degrade device performance. To improve data retention by increasing TiN thickness in via barrier is unsuitable.

With first passivation film material using PESIN total amount of 10nm TiN samples are 218 dies, 50nm TiN samples are 308 dies and 120nm TiN samples are 274 dies. As Fig. 60 and Fig. 61, memory cell performance has no obvious difference. In Fig. 62, via resistance of this experiment has same phenomenon as first passivation film using LP-PEOX.

The data retention test result is as Fig. 63. Threshold voltage shift distribution of different TiN thickness is all controlled within 0.3V. No obvious difference is found between different TiN thickness with first passivation film using PESIN.

3.3.3.3 H_2 Partial Pressure

In the hot carrier degradation MOS performance, hydrogen diffusion model and moisture diffusion model are the probable mechanism to explain the phenomenon. The moisture diffusion model is thought the most possible mechanism to explain the root cause of NROM memory cell data retention

problem. The purpose of this experiment is to clarify if hydrogen diffusion model also can explain the phenomenon of memory cell threshold voltage shift.

The TiN deposition of NROM device is accomplished by MOCVD. After TiN deposition, plasma treatment is needed to purification TiN film and reduce film resistivity. In the standard condition, gas partial pressure of H_2/N_2 in plasma treatment process is 300/200 sccm respectively. Comparison to standard condition, H_2/N_2 ratio in plasma treatment experiment is adjusted to 100/400 sccm. If hydrogen diffusion can explain the phenomenon of threshold voltage shift, reduce H_2 partial pressure should have some improvement in data retention testing.

Total amount of 60% H_2 partial pressure samples are 251 dies (H_2/N_2 ratio 300/200 sccm) and 20% H_2 partial pressure samples are 224 dies (H_2/N_2 ratio 100/400 sccm). As in Fig. 64 and Fig. 65, memory cell electric characteristic has no obvious difference. Via resistance of 20% H_2 partial pressure samples is higher as in Fig. 66. With lower H_2 partial pressure, MOCVD TiN purification is insufficient. Higher organic impurities may exist in TiN film and induce via resistance increasing.

The data retention test result is as Fig. 67. Threshold voltage shift distribution of 60% H_2 partial pressure samples is between 1.2V to 1.7V and 20% H_2 partial pressure samples is between 1.1V to 1.7V. Reduce H_2 partial pressure in plasma treatment process after TiN deposition seem no improve of threshold voltage shift. The experiment result can prove that hydrogen diffusion model cannot explain the mechanism of hot carrier degradation in NROM device.

3.3.4 Summary

In via barrier process experiment, thicker Ti can greatly improve threshold voltage shift but improvement of thicker TiN is minor. The increasing of Ti thickness from 15nm to 40nm can great improve threshold voltage high

boundary from 1.7V to 0.3V. But increasing TiN thickness from 10nm to 120nm only can improve threshold voltage low boundary from 1.2V to 0.9V, main distribution of 120nm TiN is slightly lower (about 0.3V) and no improve in threshold voltage high boundary. Modification of TiN deposition condition also has no obvious improvement of threshold voltage shift.

With first passivation film using PESIN, even origin via barrier condition can get good data retention improve. The experiment results indicate that first passivation film material is the most important factor to affect threshold voltage shift. Modification of via barrier process can further improve data retention ability by increasing percentage of no threshold voltage shift samples from 2% to 30%.

Chapter 4

Conclusions

In this work, many experiments were performed to improve data retention ability of NROM device. Base on experiment result, positive charge trap and de-trap in bottom oxide of ONO layer is the major mechanism to cause threshold voltage shift after over 100 program/erase cycles. The trapped positive charge will assist negative charge tunneling into nitride layer or de-trap from bottom oxide. The final net charge in memory cell will be more negative and cause threshold voltage higher [8].

Base on hot carrier degradation by moisture diffusion model, the diffusion of excess moisture from SAUSG film in passivation layer into BPSG will release positive charge (ex. sodium) trapped in the BPSG [26]. The positive charge will be trapped in bottom oxide during hot hole erase or hot electron program operation. To reduce positive charge trapping in bottom oxide, diminishing moisture content in passivation film and prevent remaining moisture diffusion should be achieved.

In the experiments of diminishing moisture content in passivation film, wafer curing before top passivation film deposition can greatly improve data retention ability of NROM device. After wafer curing, content of moisture in SAUSG film will down to a minor level and not affect BPSG gettering ability. So positive charge gettered in BPSG will not be released to affect memory cell.

To prevent moisture diffusion from SAUSG film, thin blocking layer such as PESIN or SION under SAUSG film is more effective. With PESIN blocking layer, threshold voltage shift after 100 program/erase cycles can be controlled in 0.3V even no wafer curing applied before top passivation film deposition. The increasing of Ti thickness in via barrier also has improvement in data retention

of NROM device. The threshold voltage shift of memory cell is inverse proportional to Ti thickness. With combination of PESIN blocking layer and 40nm Ti, threshold voltage shift after 100 program/erase cycles can be controlled in 0.2V and no threshold voltage shift samples can increase to over 30 percent.

Base on experiment result, modification of passivation film and via barrier process can effective prevent moisture to affect data retention ability of NROM memory cell and no influence on memory cell characteristic. The hot carrier degradation by moisture diffusion model is suitable to explain the mechanism of memory cell threshold voltage shift high phenomenon.