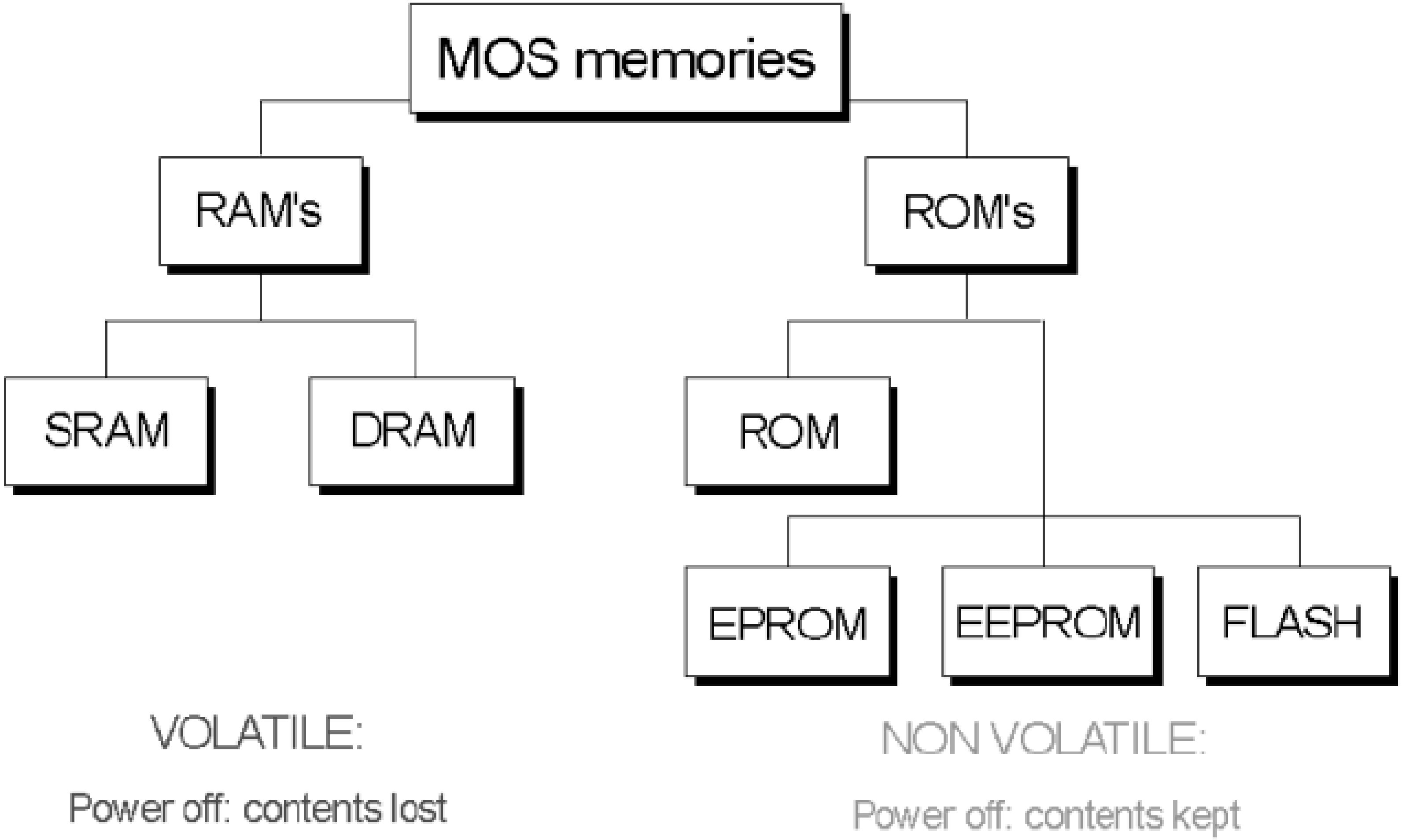
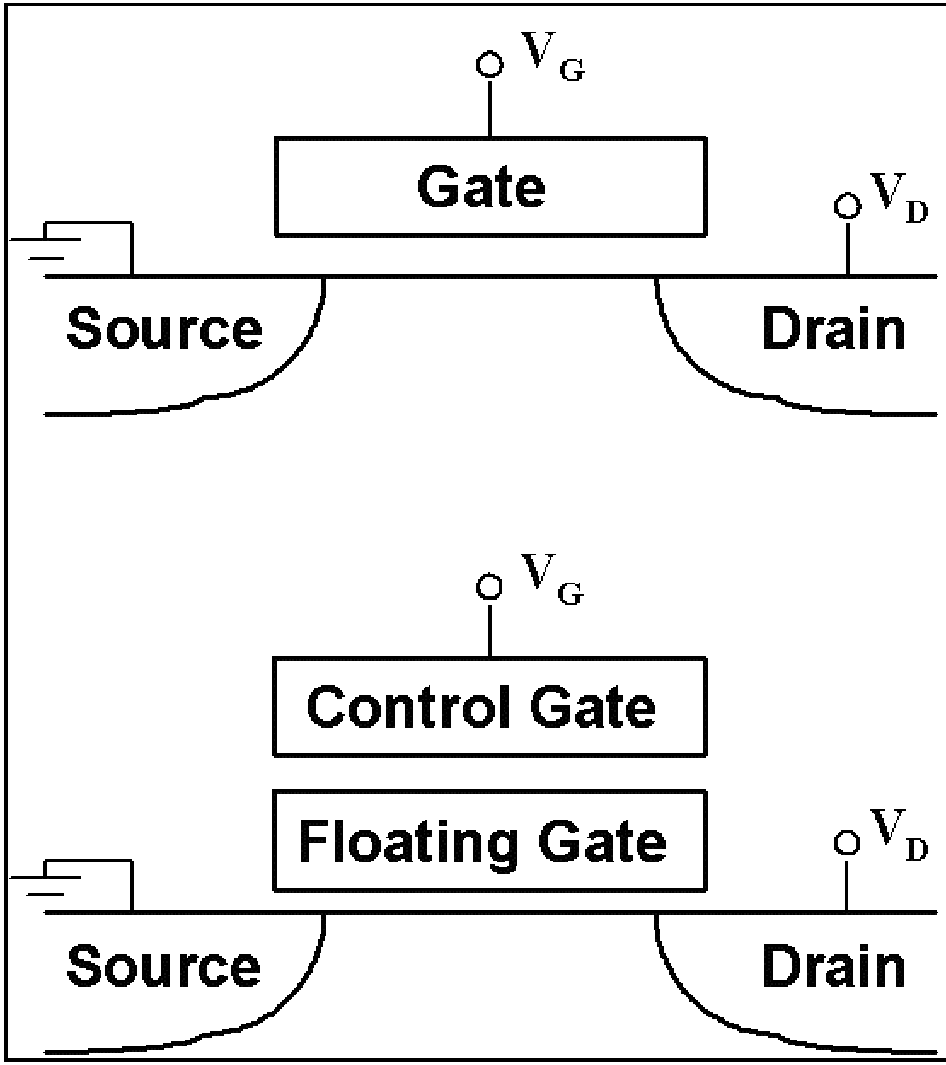


Figure 1 MOS memory tree

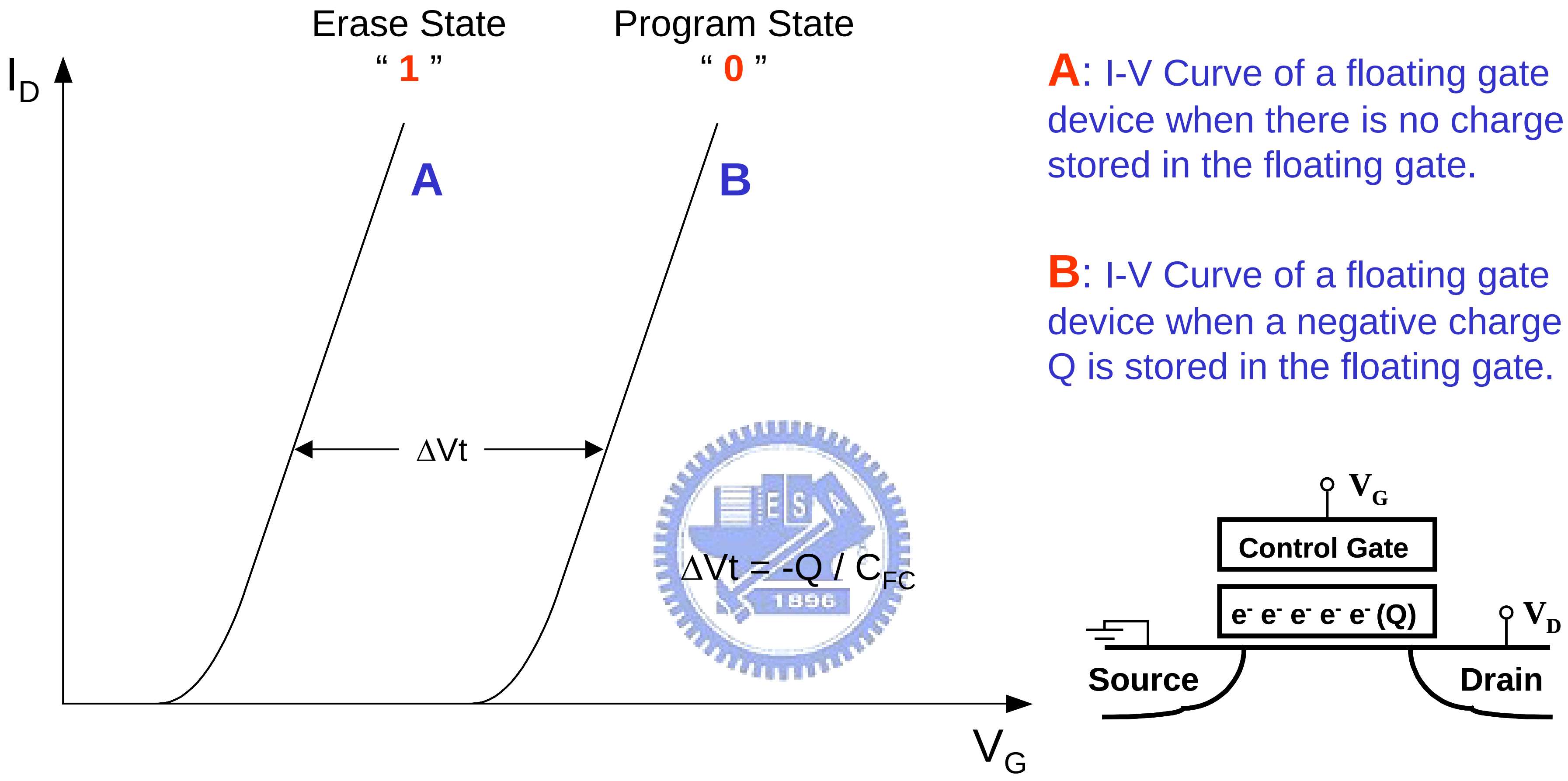
Reference from “Introduction to Flash Memory,” *PROCEEDINGS OF THE IEEE*, VOL. 91, NO. 4, APRIL 2003



- Gate bias is directly control by external voltage

- Gate bias (floating gate) is determined by capacitance coupling of control gate, drain, source, and bulk
- Floating gate can stored the charges and change the cell states

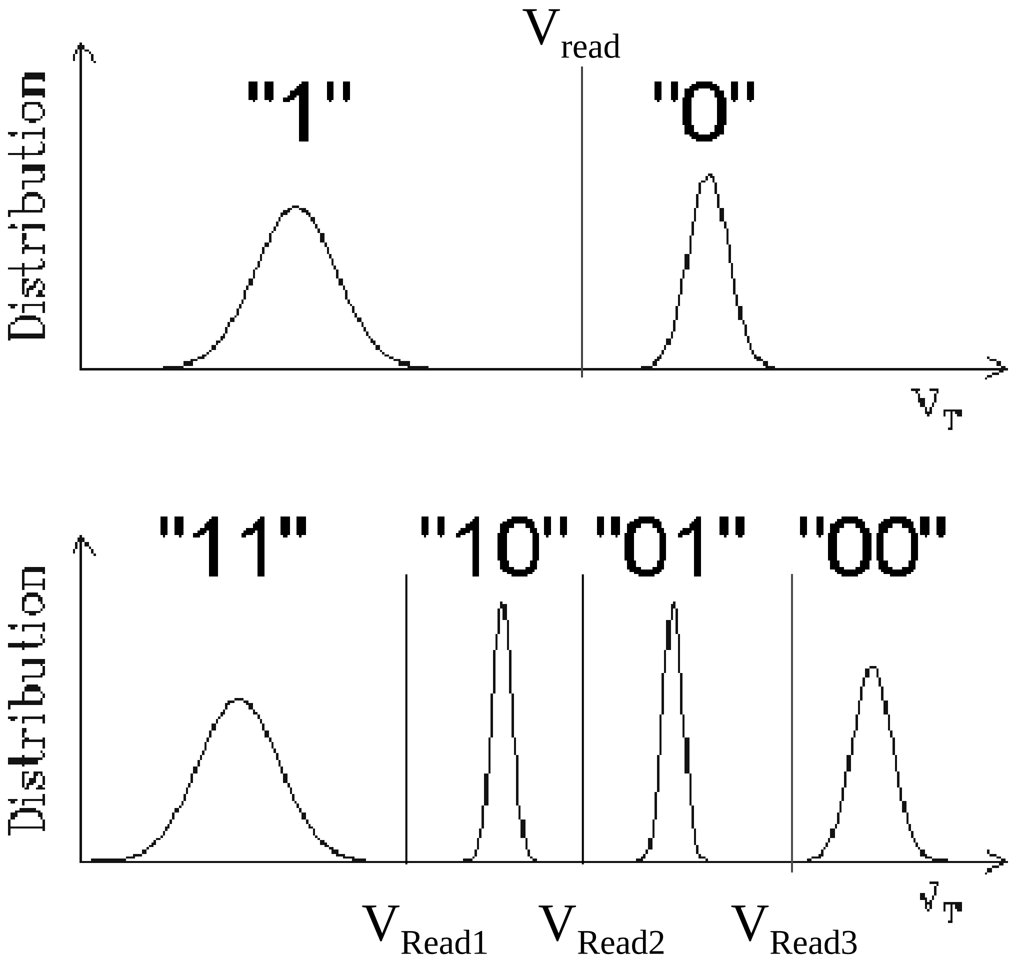
Figure 2 MOS and Flash memory structure compare



A: I-V Curve of a floating gate device when there is no charge stored in the floating gate.

B: I-V Curve of a floating gate device when a negative charge Q is stored in the floating gate.

Figure 3 Floating-gate MOSFET reading operation



- ❑ 1 bit/cell => 2 levels
- ❑ 2 bit/cell => 4 levels

Figure 4 Threshold voltage distribution for 2 b/cell compared with the standard 1 b/cell

Reference from “Introduction to Flash Memory,” *PROCEEDINGS OF THE IEEE*, VOL. 91, NO. 4, APRIL 2003

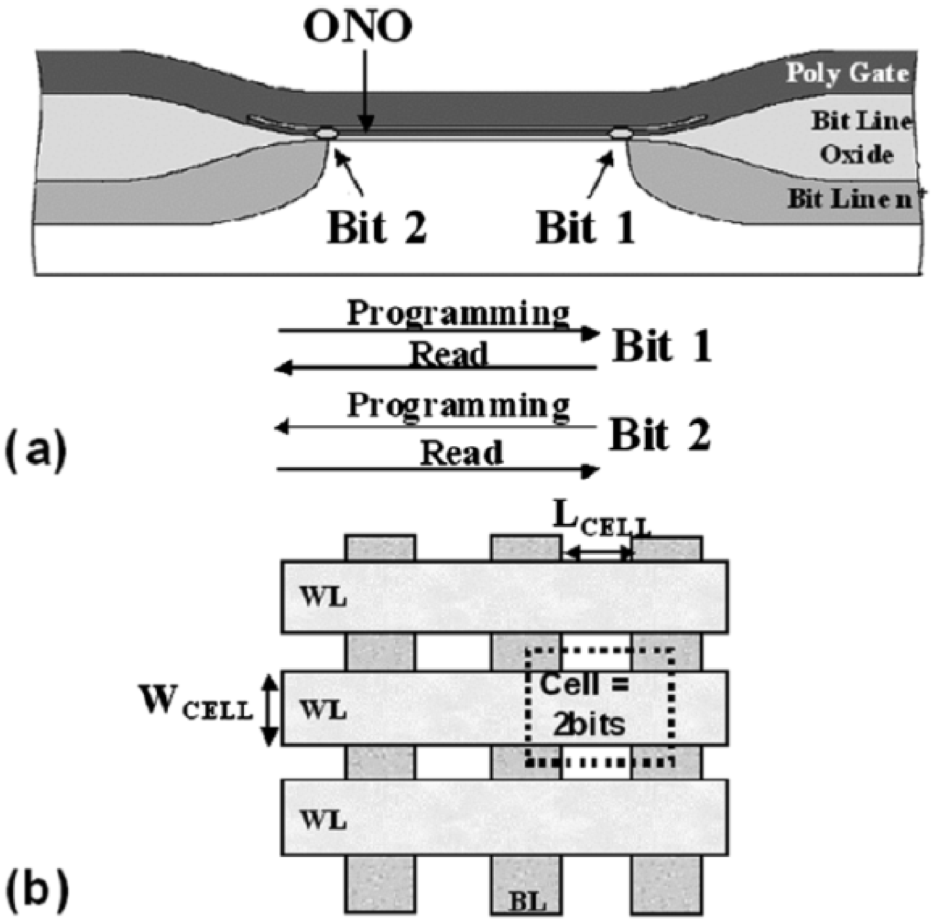


Figure 5 (a) Cross section and (b) top view of an NROM cell.

Reference from “Data Retention Reliability Model of NROM Nonvolatile Memory Products”, in *IEEE Transactions on Device and Materials Reliability*, 2004

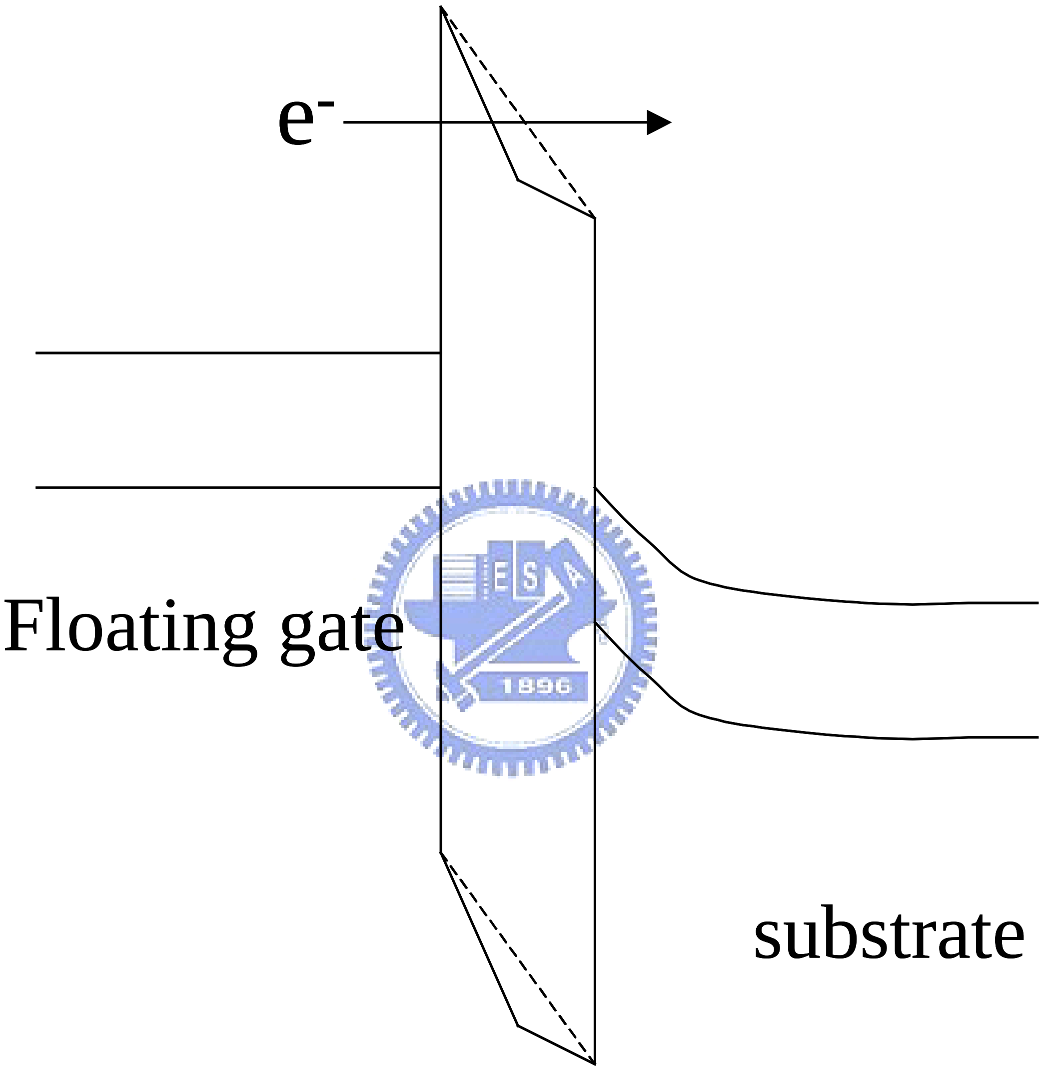


Figure 6 Band diagram of oxide trapped charge induce barrier lower

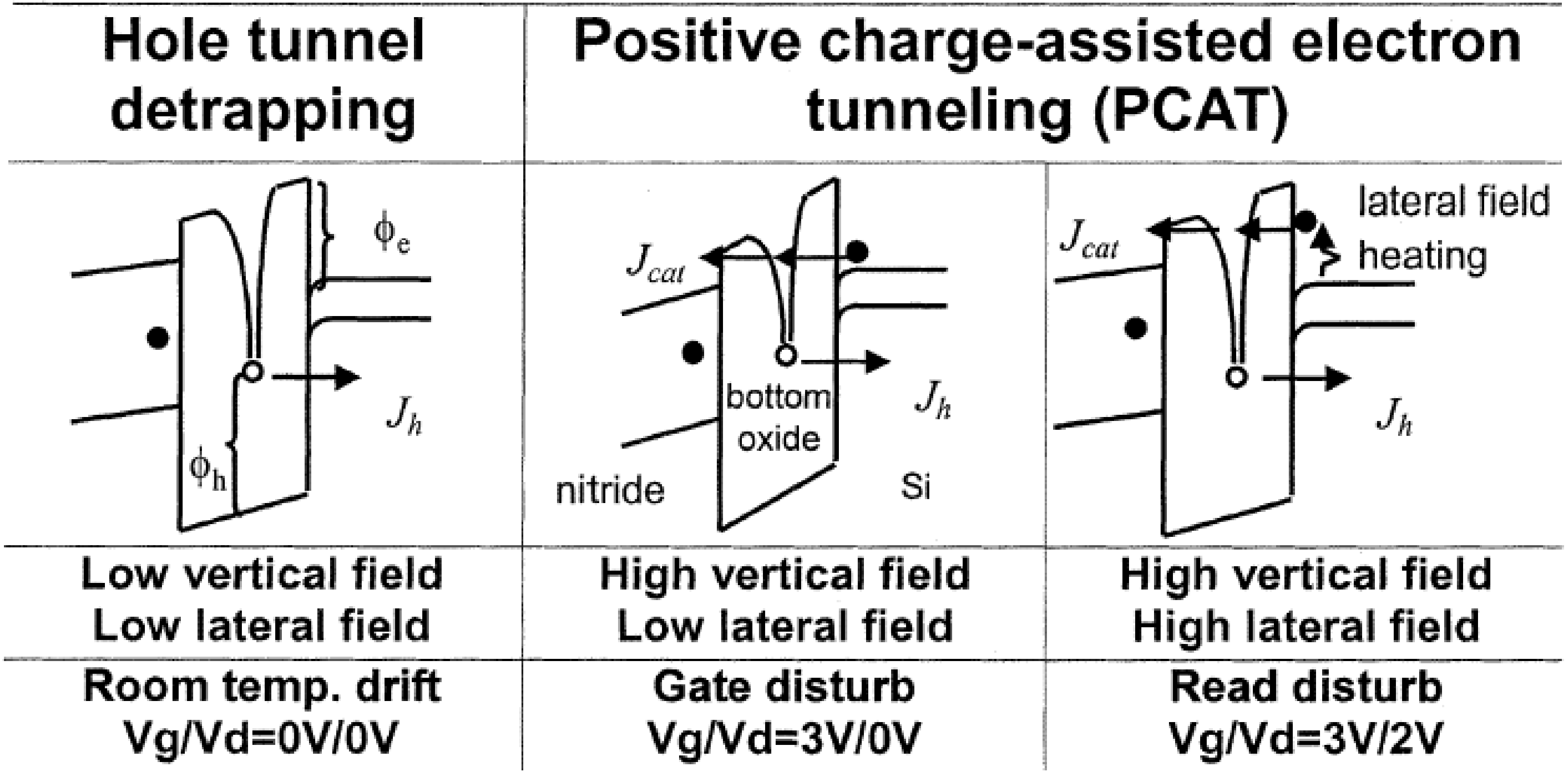
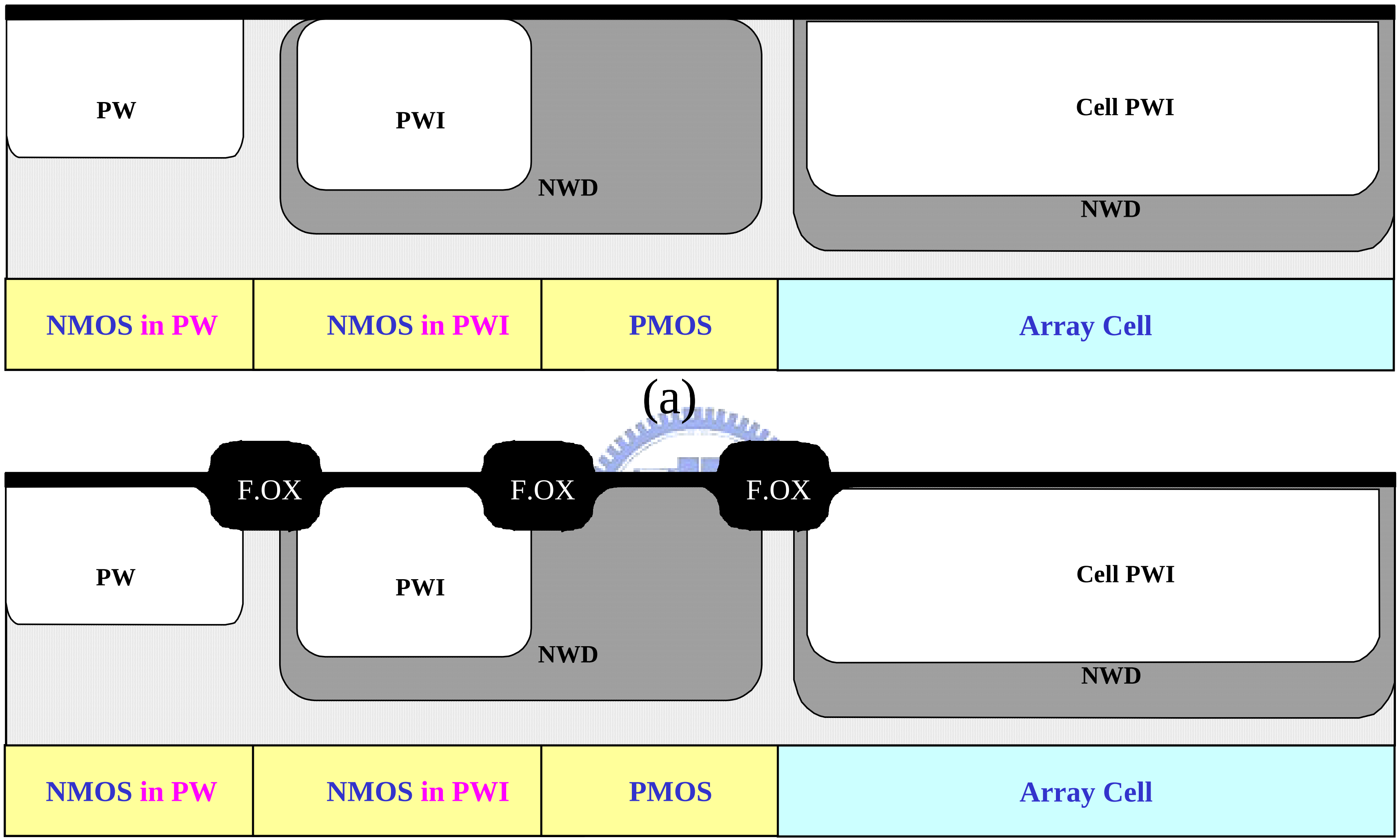


Figure 7 Schematics of band diagrams and carrier transport mechanisms at various bias conditions

Reference from “Positive oxide charge-enhanced read disturb in a localized trapping storage flash memory cell,” *IEEE Trans. Electron Devices*, no. 4, pp. 434–439, Apr. 2004



(a)

(b)

Figure 8 NROM device fabrication flow, (a) after well engineer and (b) after field oxidization

Property	**LPCVD**	**PECVD**
Deposition temperature (℃)	700 to 800	300 to 400
Composition	Si_3N_4	$Si_xN_yH_z$
Step coverage	Fair	Conformal
Stress at 23℃ on silicon (dynes/cm^2)	$1.2 \sim 1.8 \times 10^{10}$ (tensile)	$1 \sim 8 \times 10^{9}$ (tensile or compressive)

Table 1 Properties of Silicon Nitride for LPCVD vs. PECVD

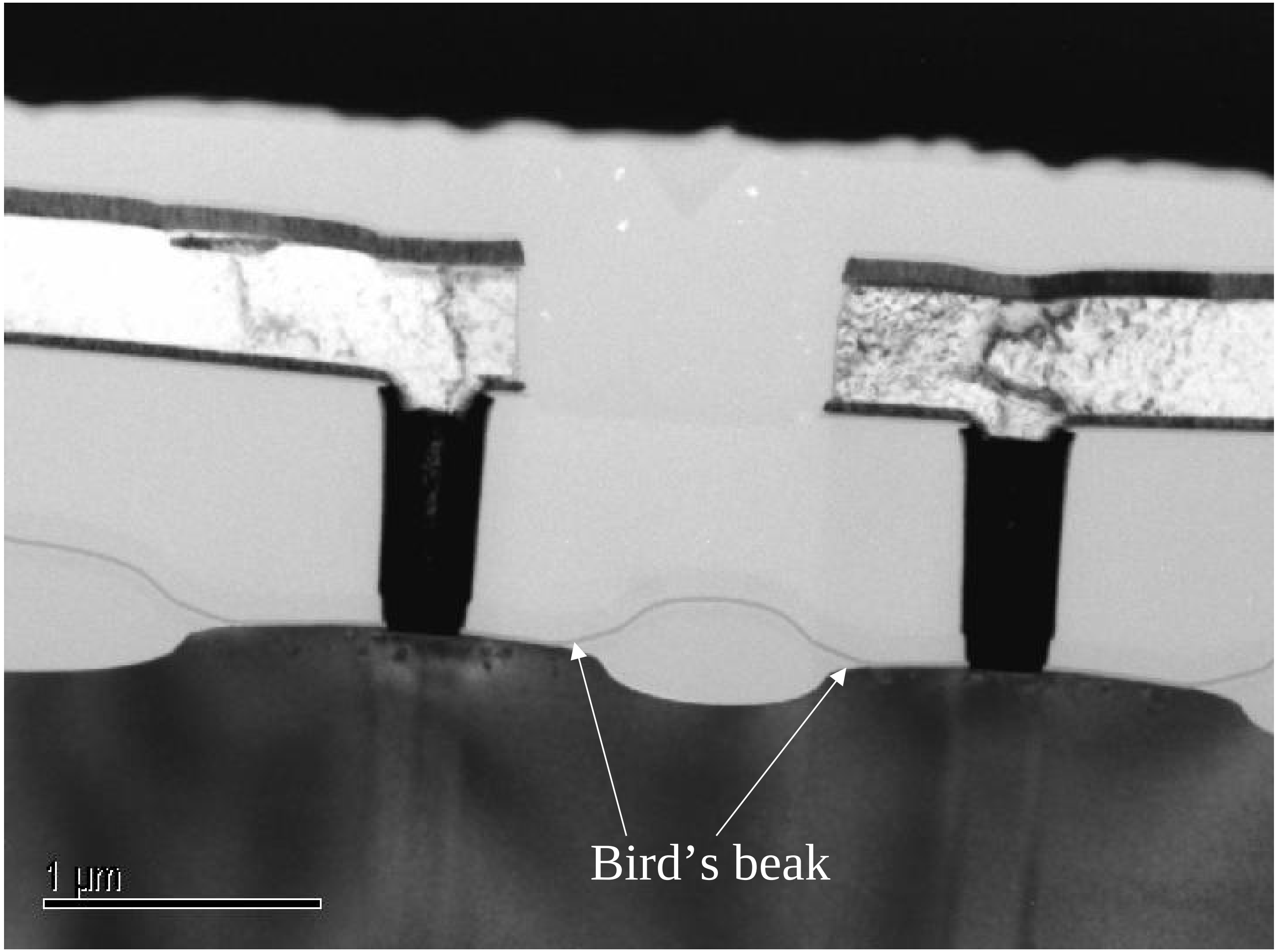


Figure 9 TEM cross-section of LOCOS field oxide

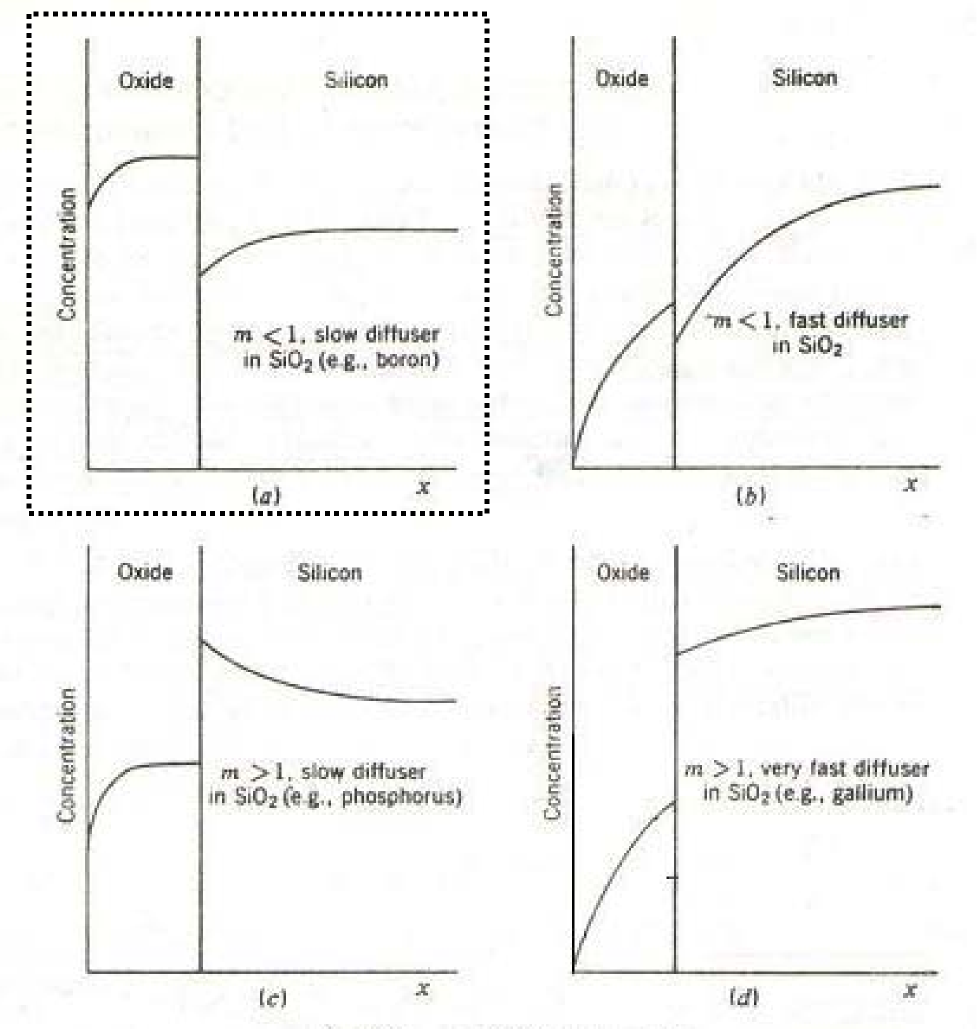


Figure 10 Dopant segregation at Si/SiO_2 interface

Reference from *“Silicon Processing for the VLSI Era.”* Sunset Beach, CA: Lattice, vol.1, ch. 7, pp. 229

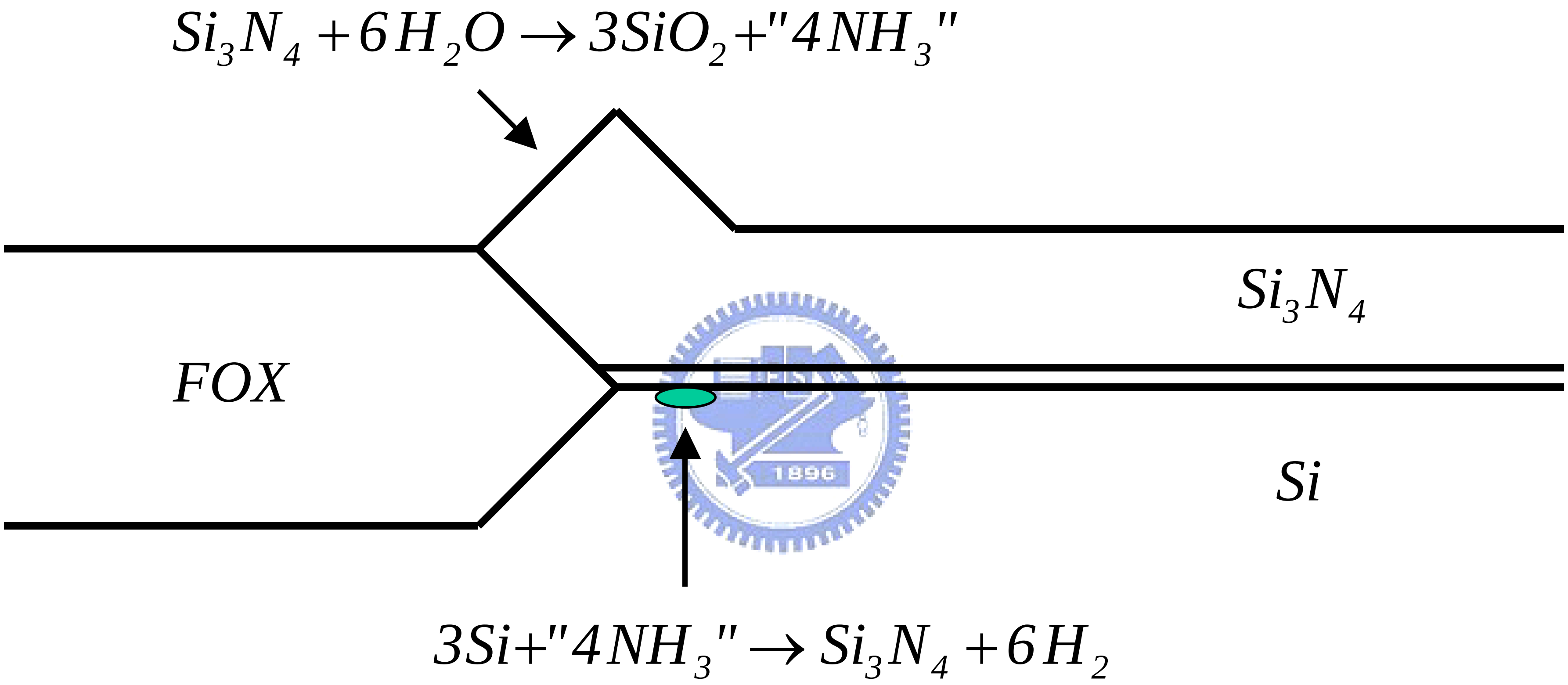
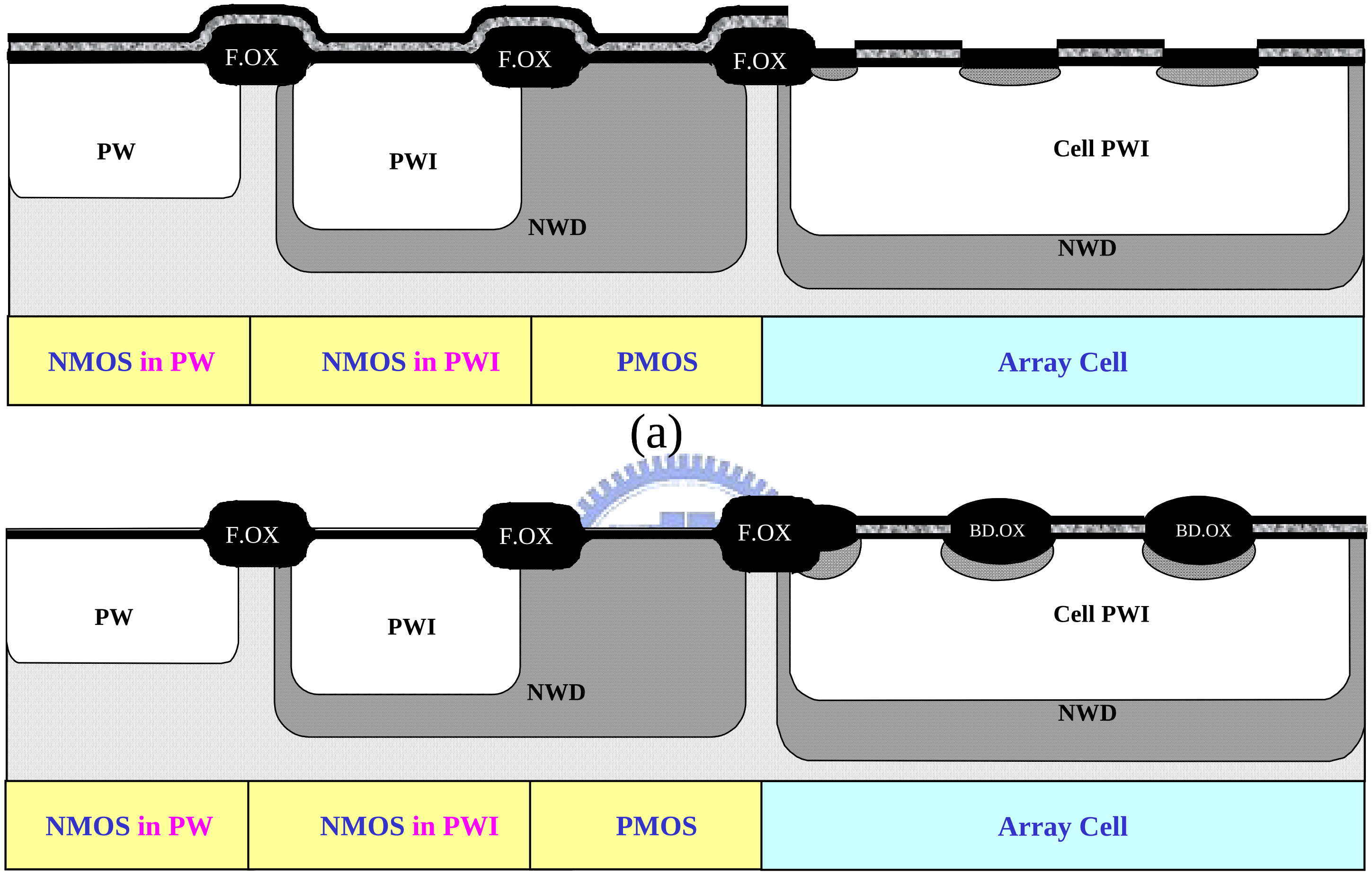


Figure 11 Illustration of Kooi effect



(a)

(b)

Figure 12 NROM device fabrication flow, (a) after cell S/D implantation and (b) after ONO remove in periphery circuit

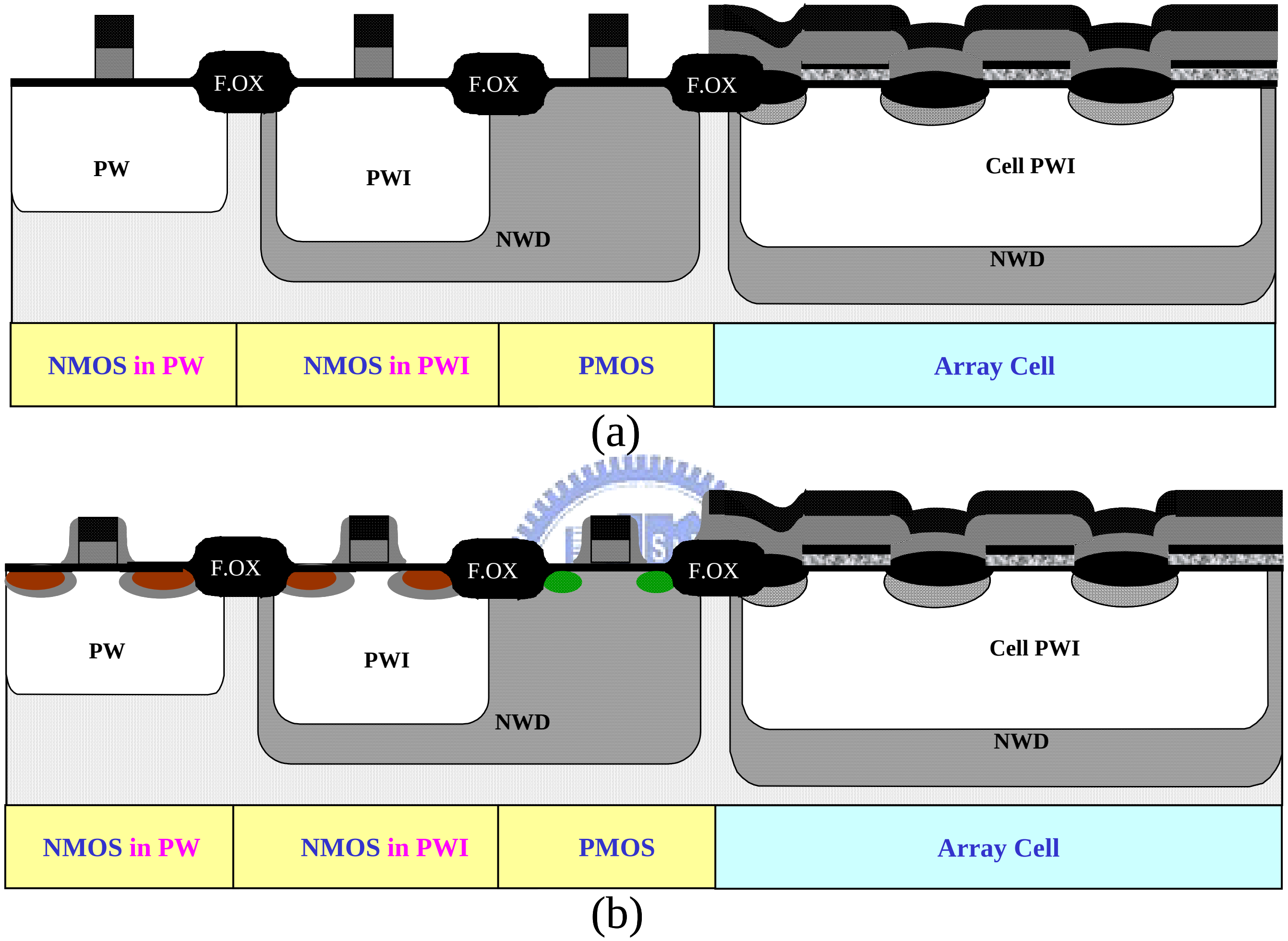


Figure 13 NROM device fabrication flow, (a) after gate patterning and (b) after periphery circuit S/D implantation

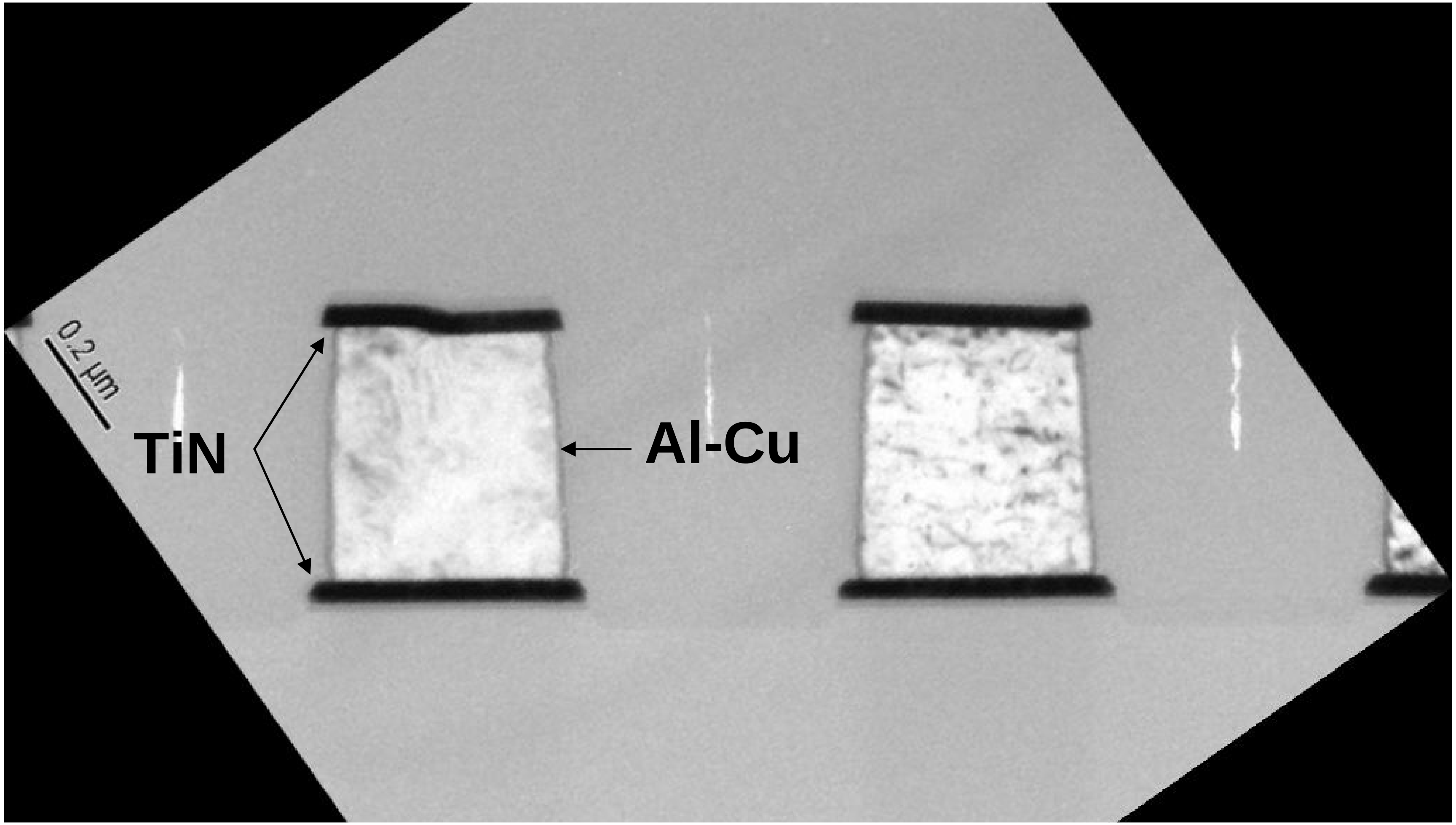


Figure 14 TEM cross-section of metal film

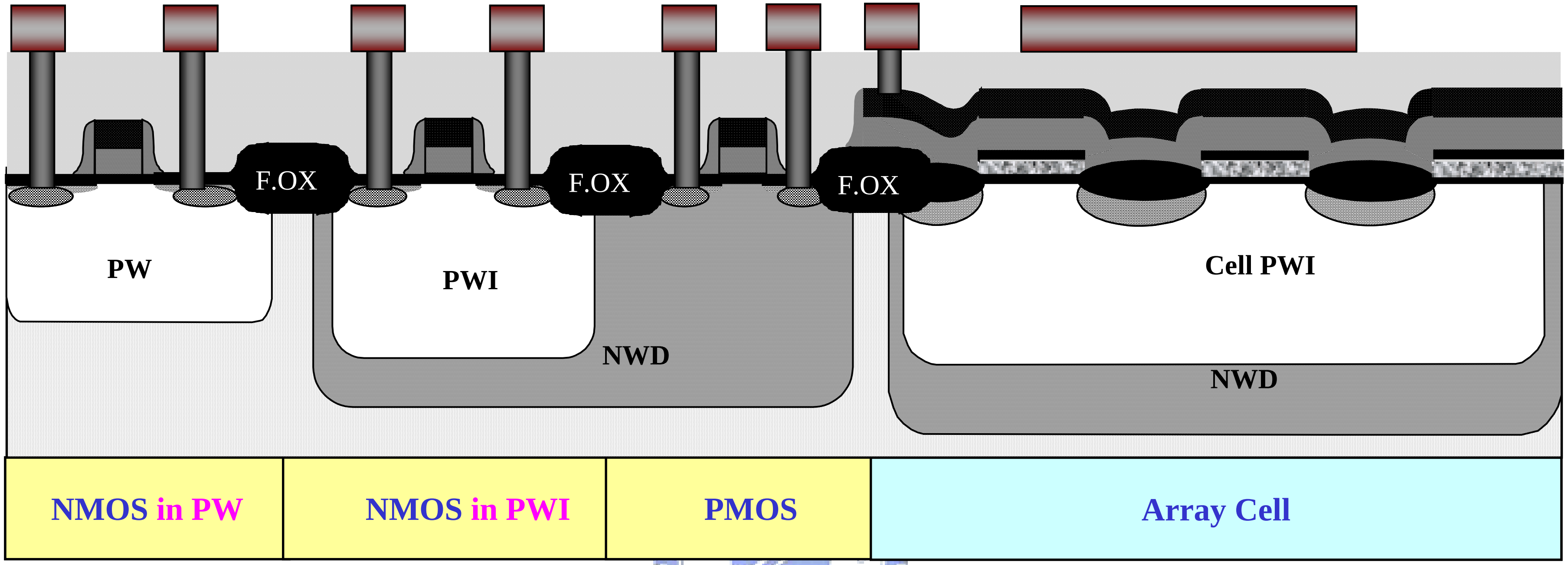


Figure 15 NROM device fabrication flow - after metal 1 patterning

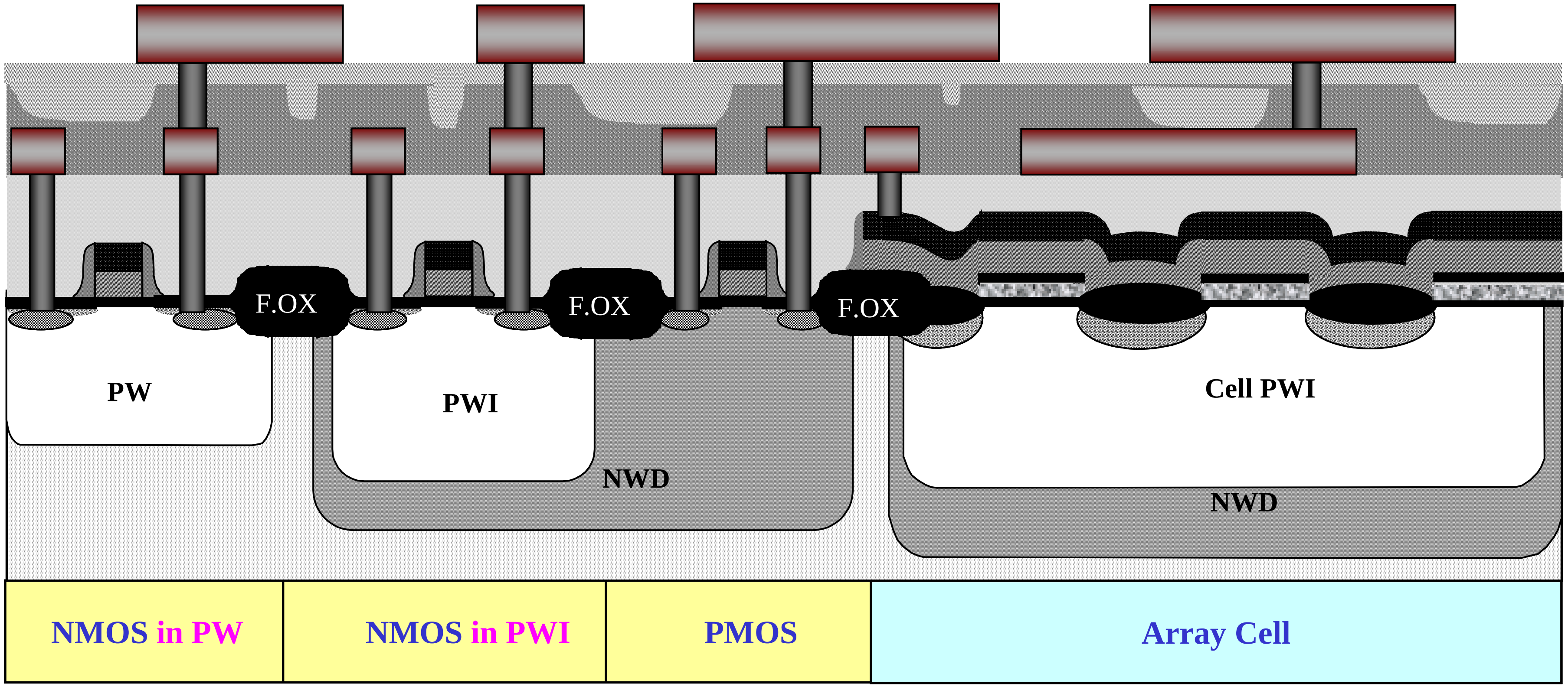


Figure 16 NROM device fabrication flow – after metal 2 patterning

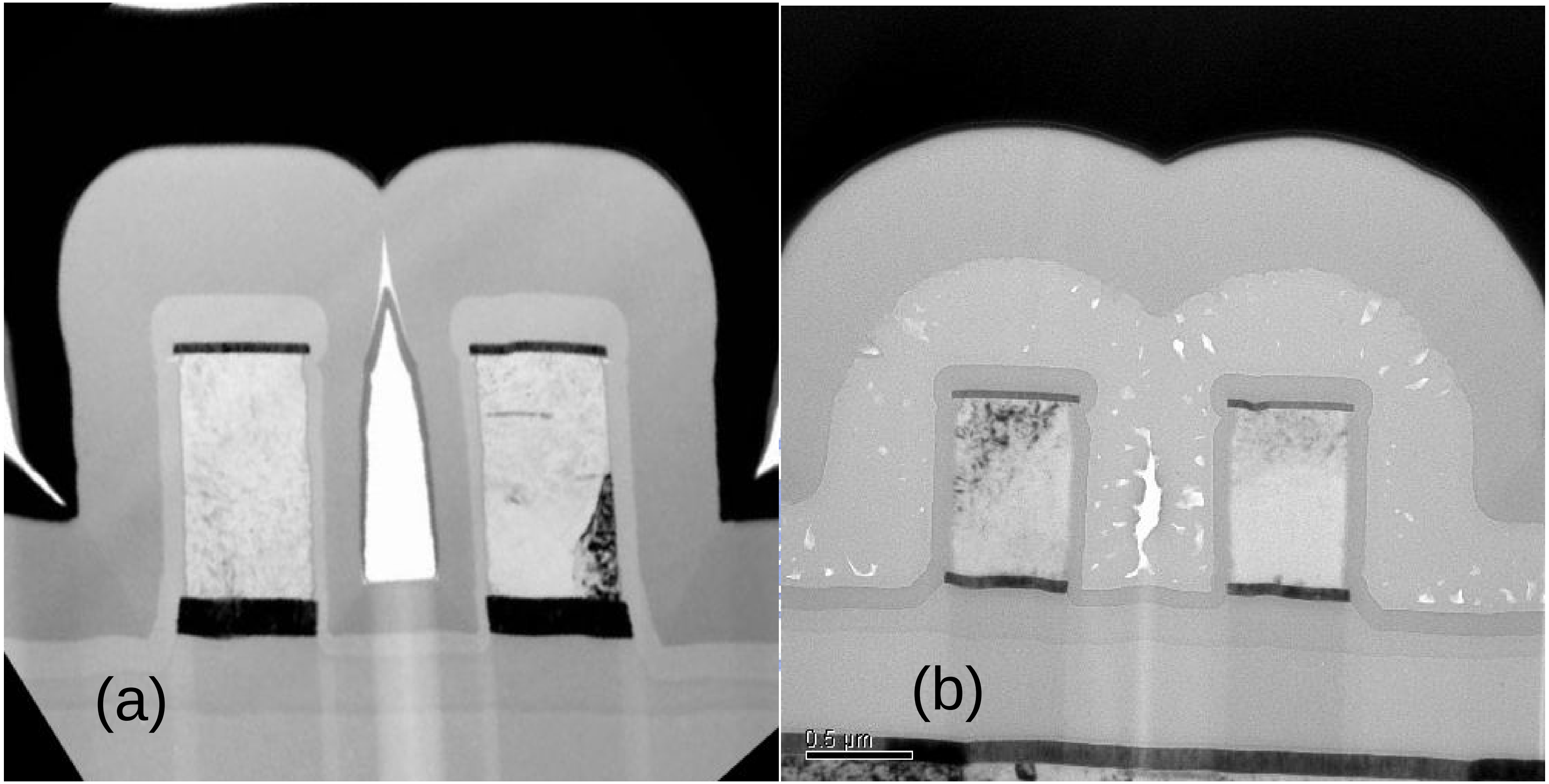


Figure 17 passivation film structure, (a)Without SAUSG, (b)With SAUSG

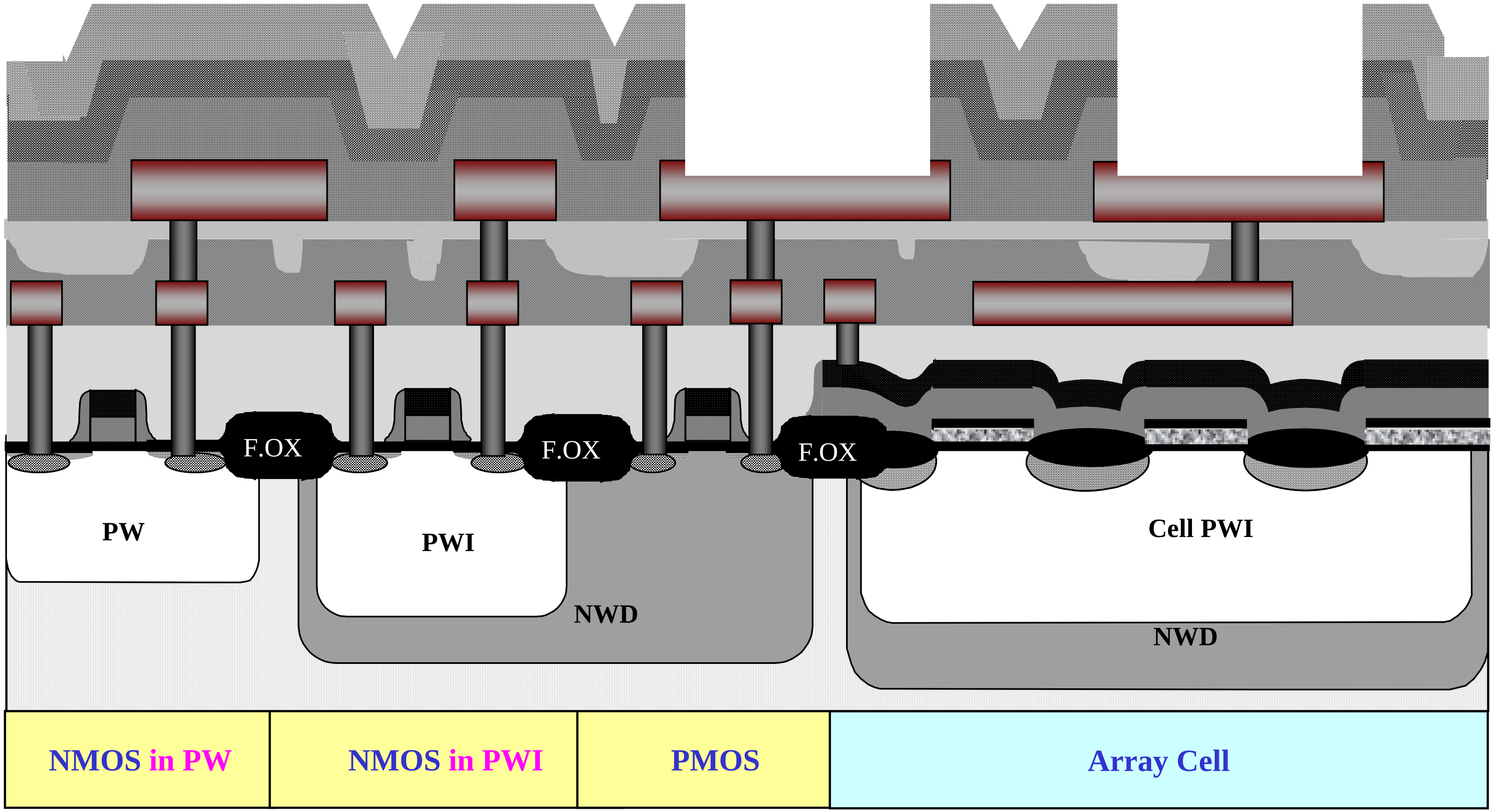


Figure 18 NROM device fabrication flow – after pad window opening

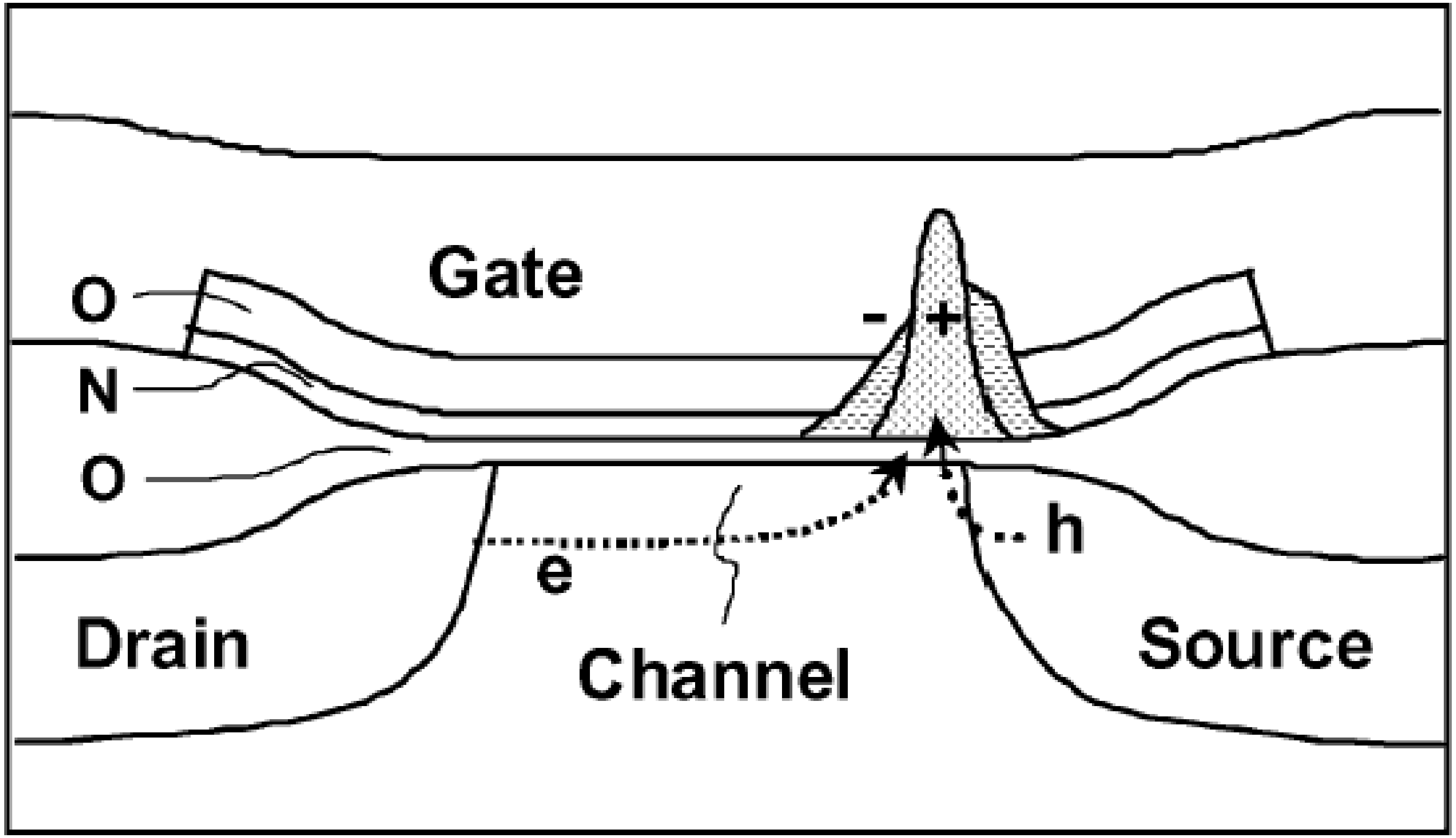


Figure 19 Schematics illustration of cross section of NROM cell and the program

and erase injected charge distributions

Reference from “Data Retention Reliability Model of NROM Nonvolatile Memory Products”

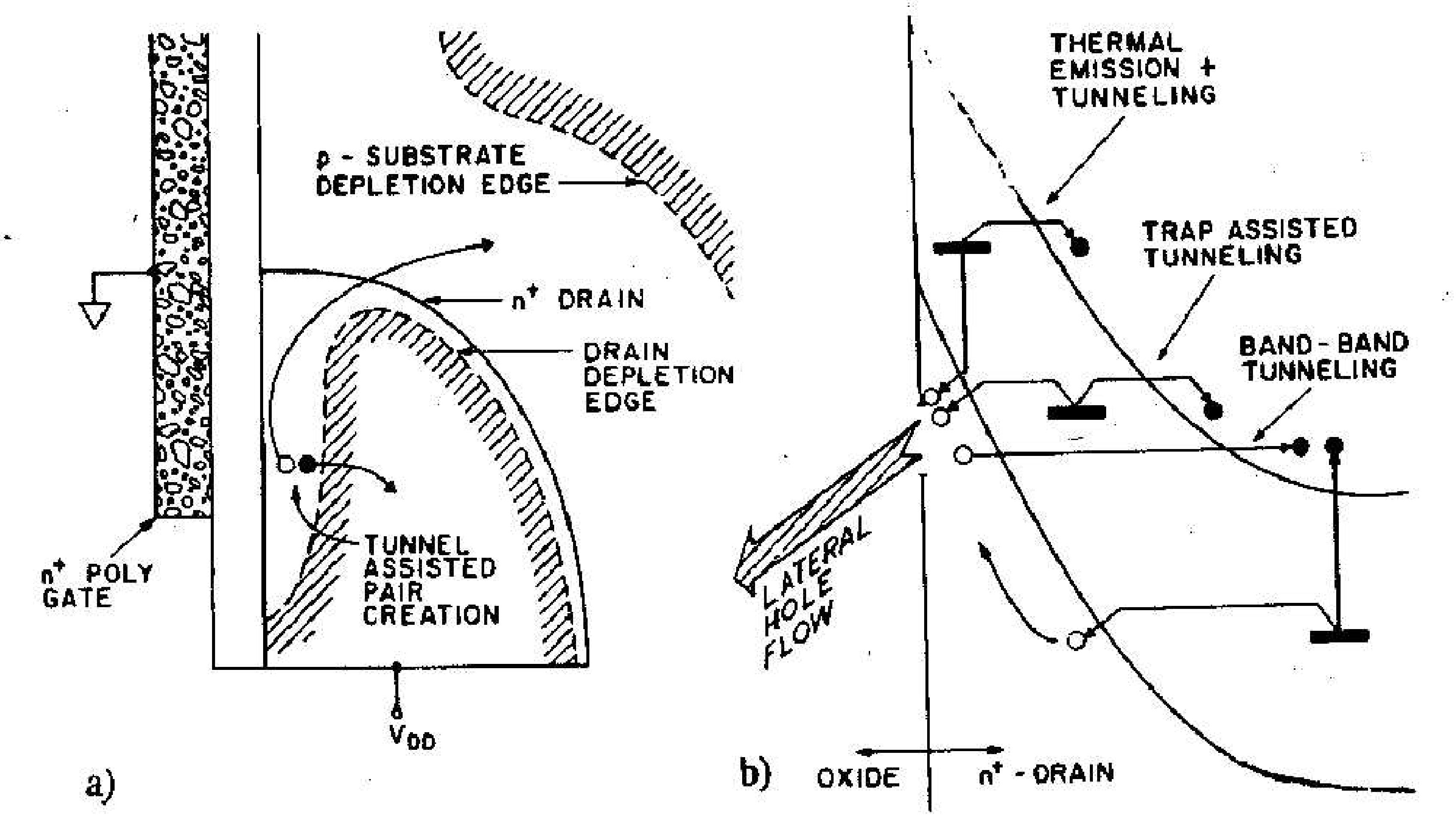


Figure 20 Illustration of hot hole generation mechanism

Reference from “The Submicron MOSFET,” Chap.3, in *High-Speed Semiconductor Device*, Ed. Sze.

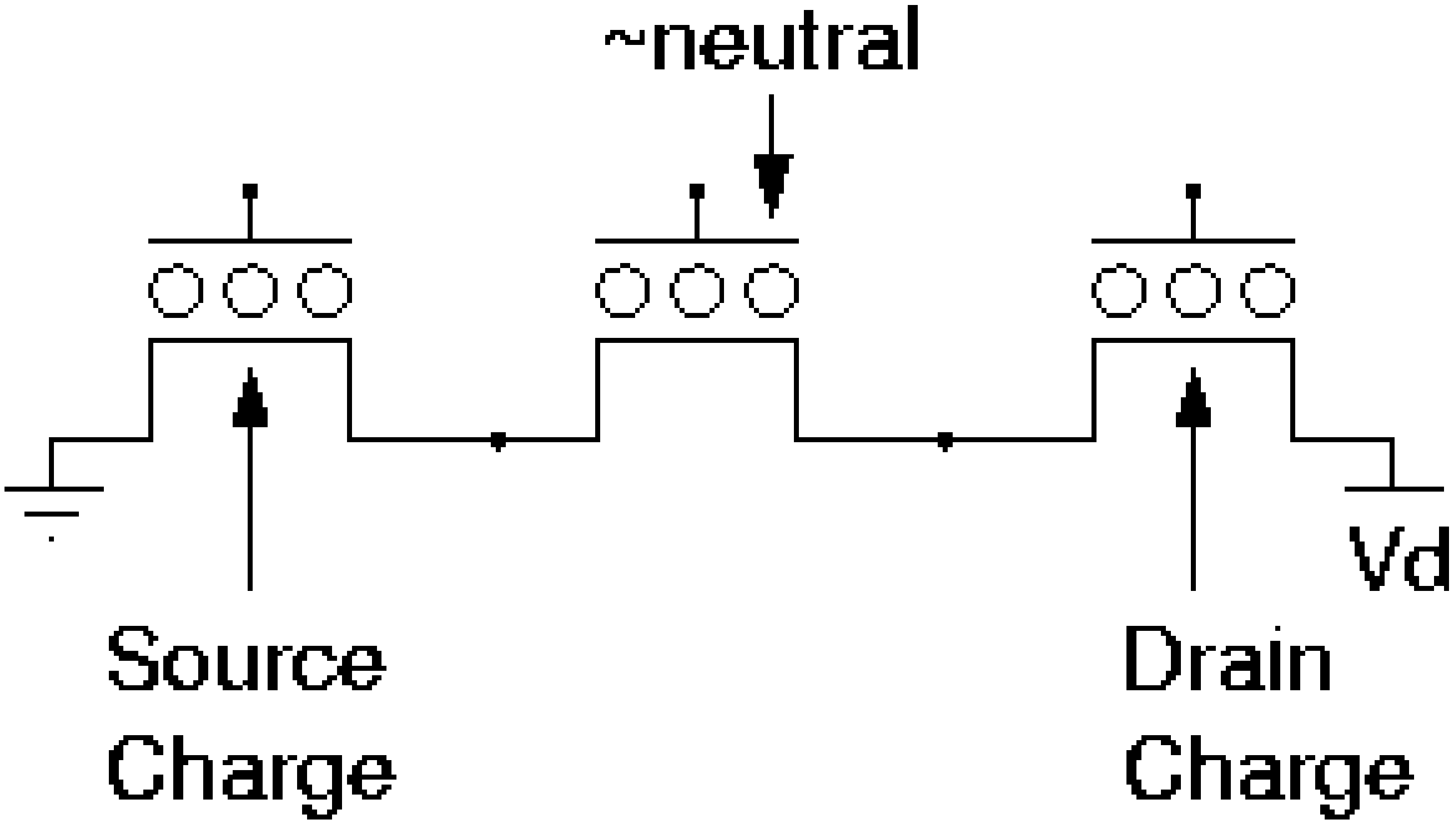


Figure 21 Equivalent device structure of NROM memory cell

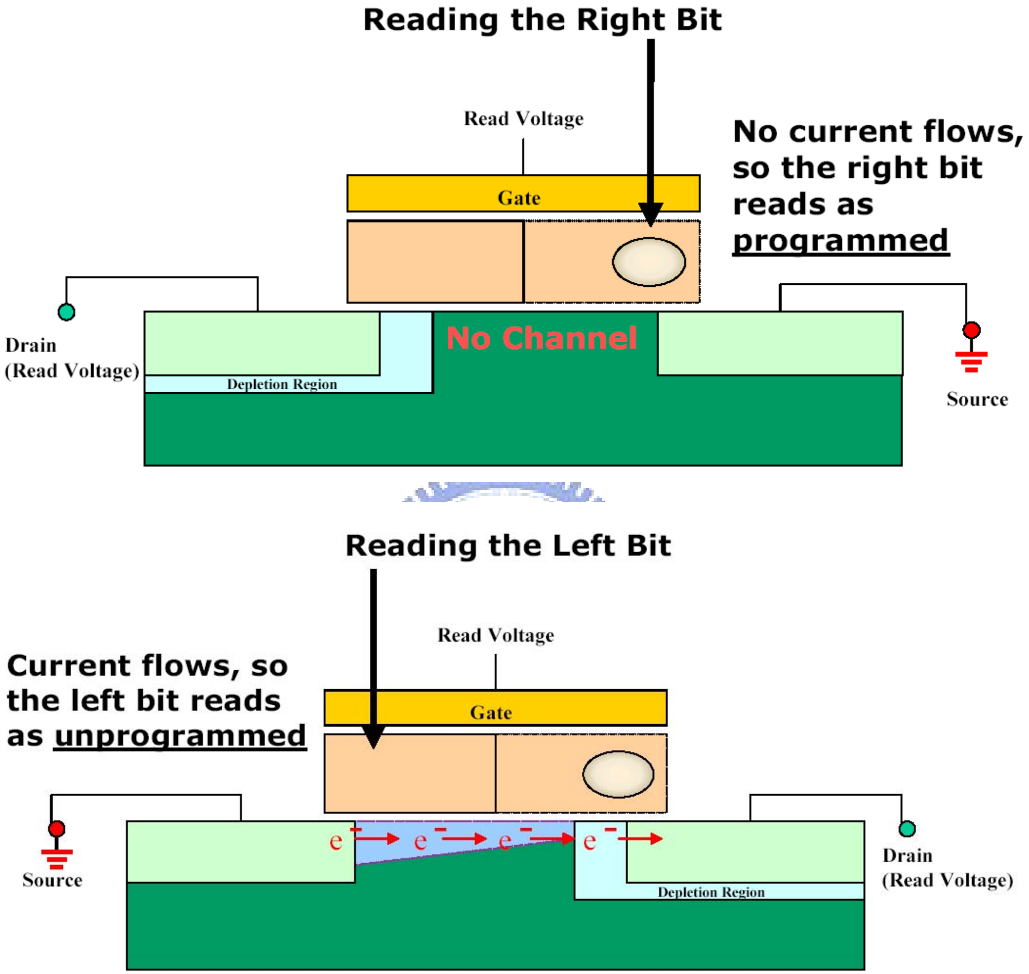


Figure 22 Illustration of NROM cell in read operation

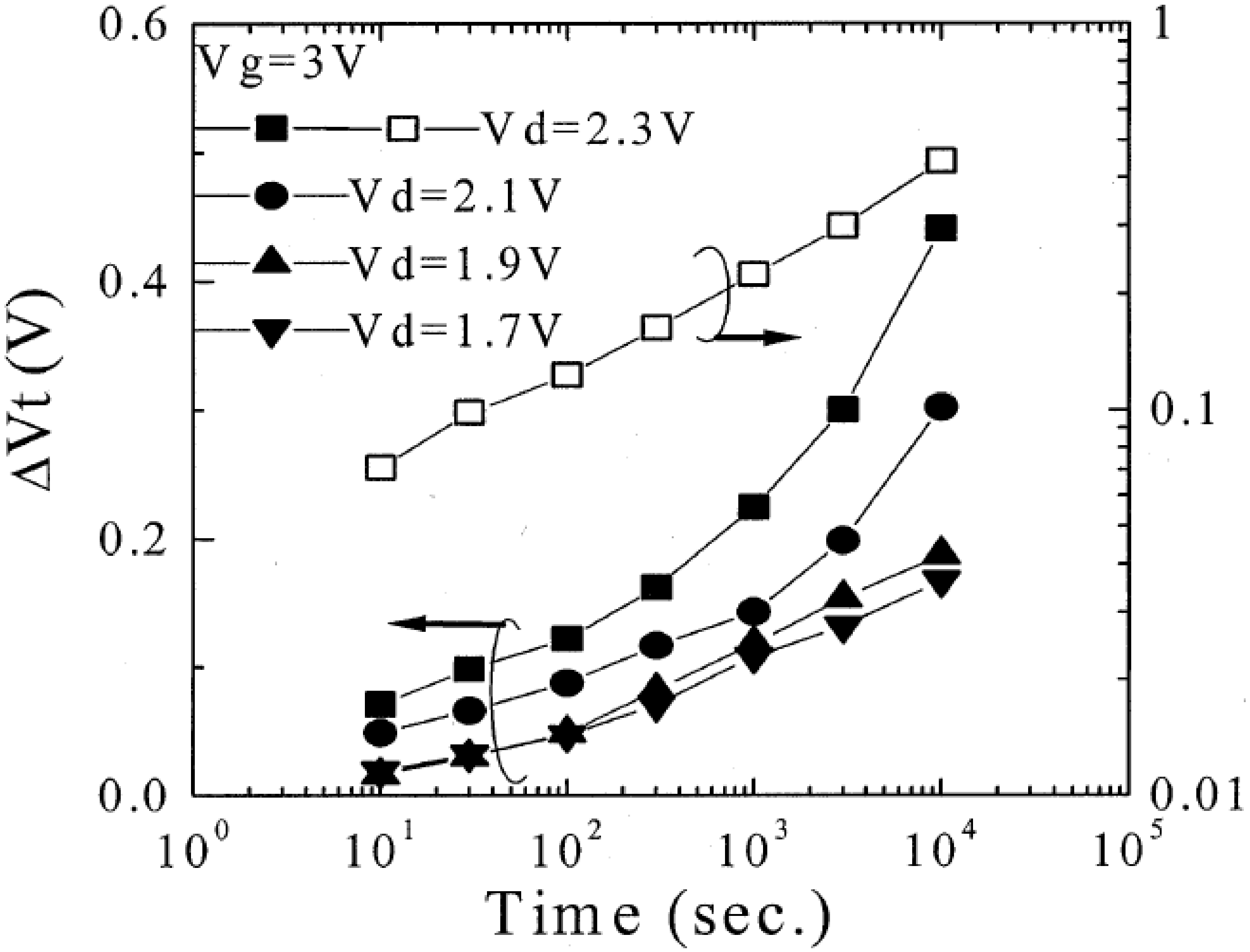


Figure 23 Vt shift versus disturb time of a 10-K P/E cycled cell at various drain biases.

Reference from “Positive oxide charge-enhanced read disturb in a localized trapping storage flash memory cell,” *IEEE Trans. Electron Devices*, no. 4, pp. 434–439, Apr. 2004

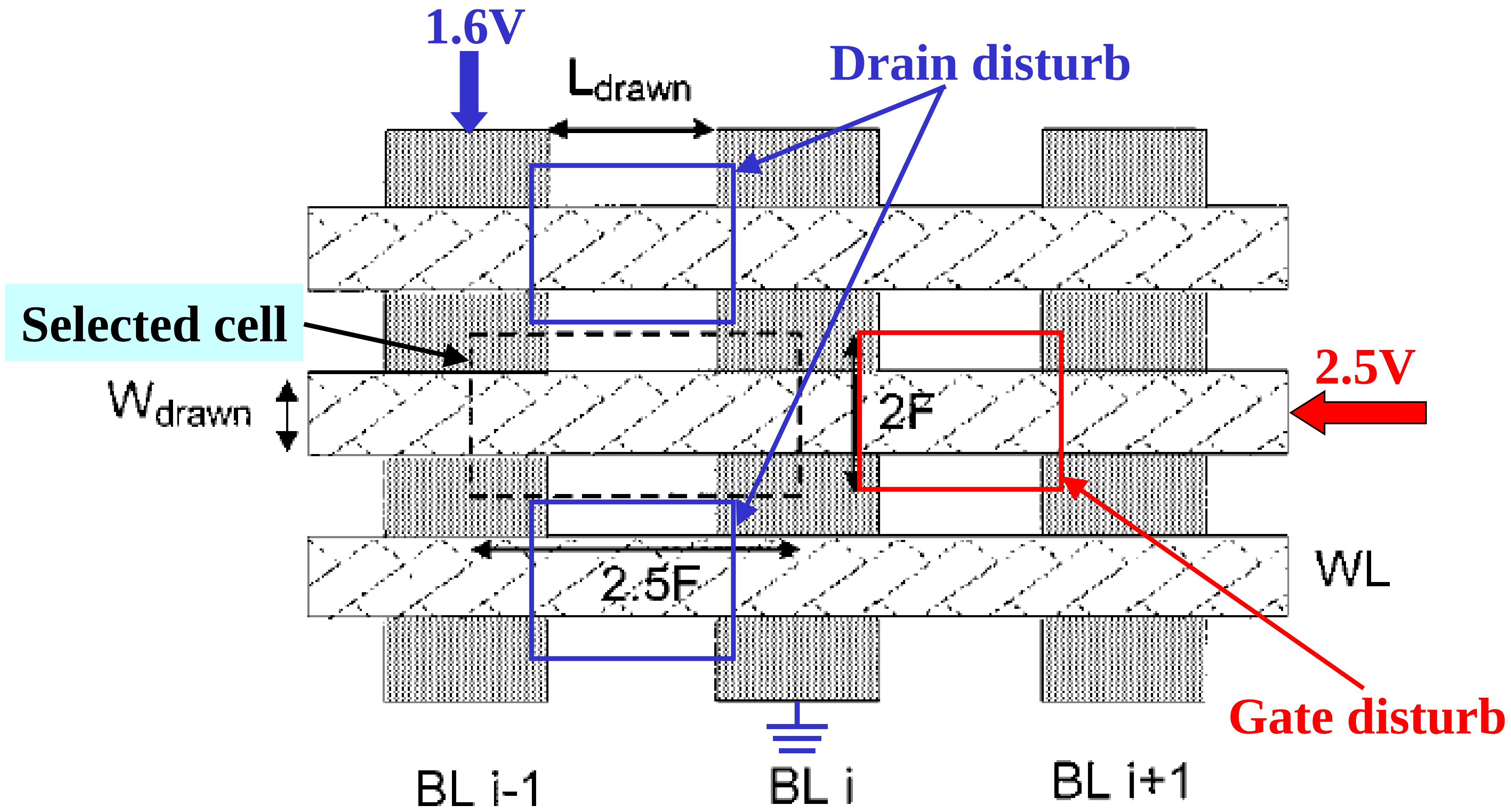


Figure 24 various disturb of NROM device during read operation

Reference from “NROM: A novel localized trapping, 2-bit nonvolatile memory cell,” *IEEE Electron Device Lett.*, no. 6, pp. 543–545, Jun. 2000

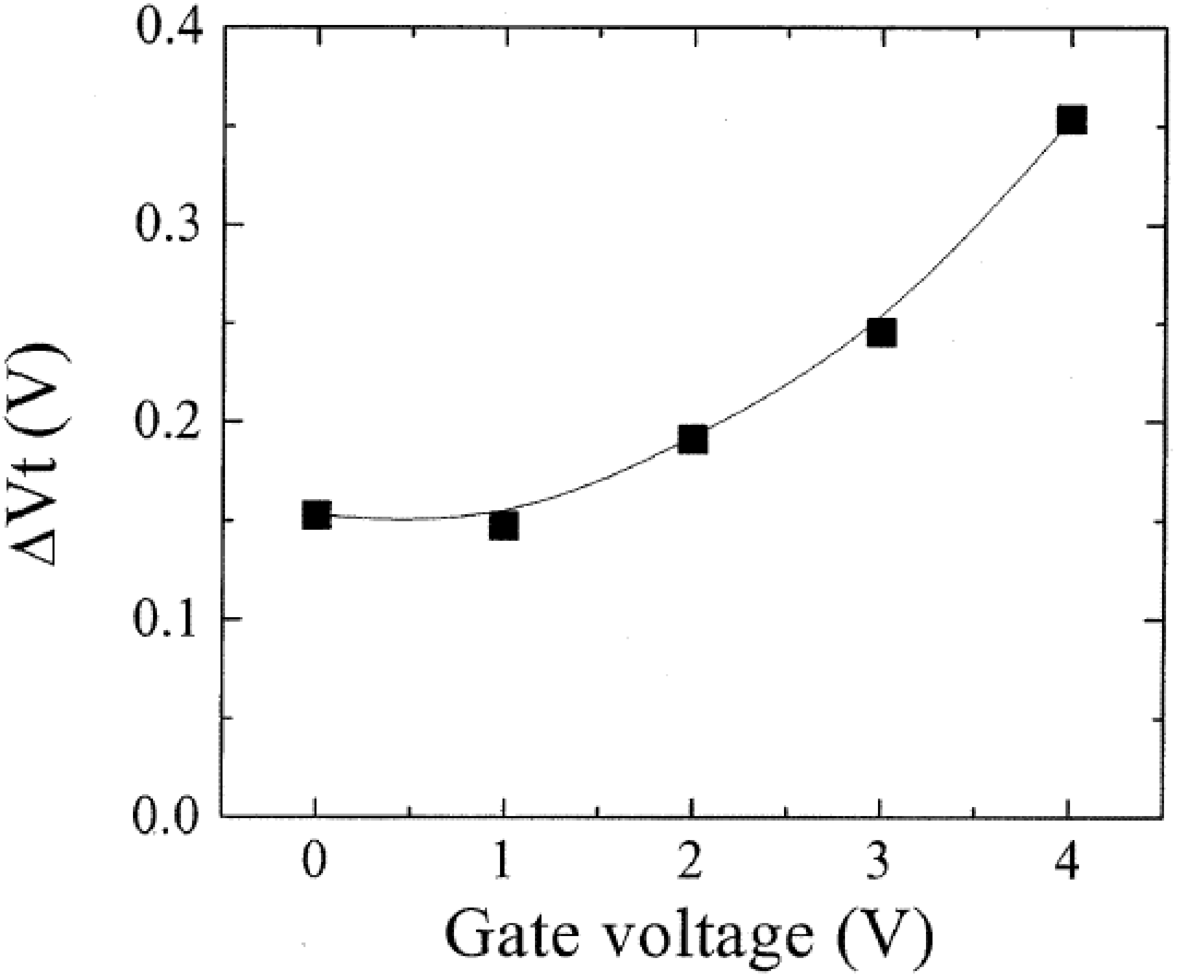


Figure 25 Vt shift versus applied gate bias of a 10-K P/E cycled cell

Reference from “Positive oxide charge-enhanced read disturb in a localized trapping storage flash memory cell,” *IEEE Trans. Electron Devices*, no. 4, pp. 434–439, Apr. 2004

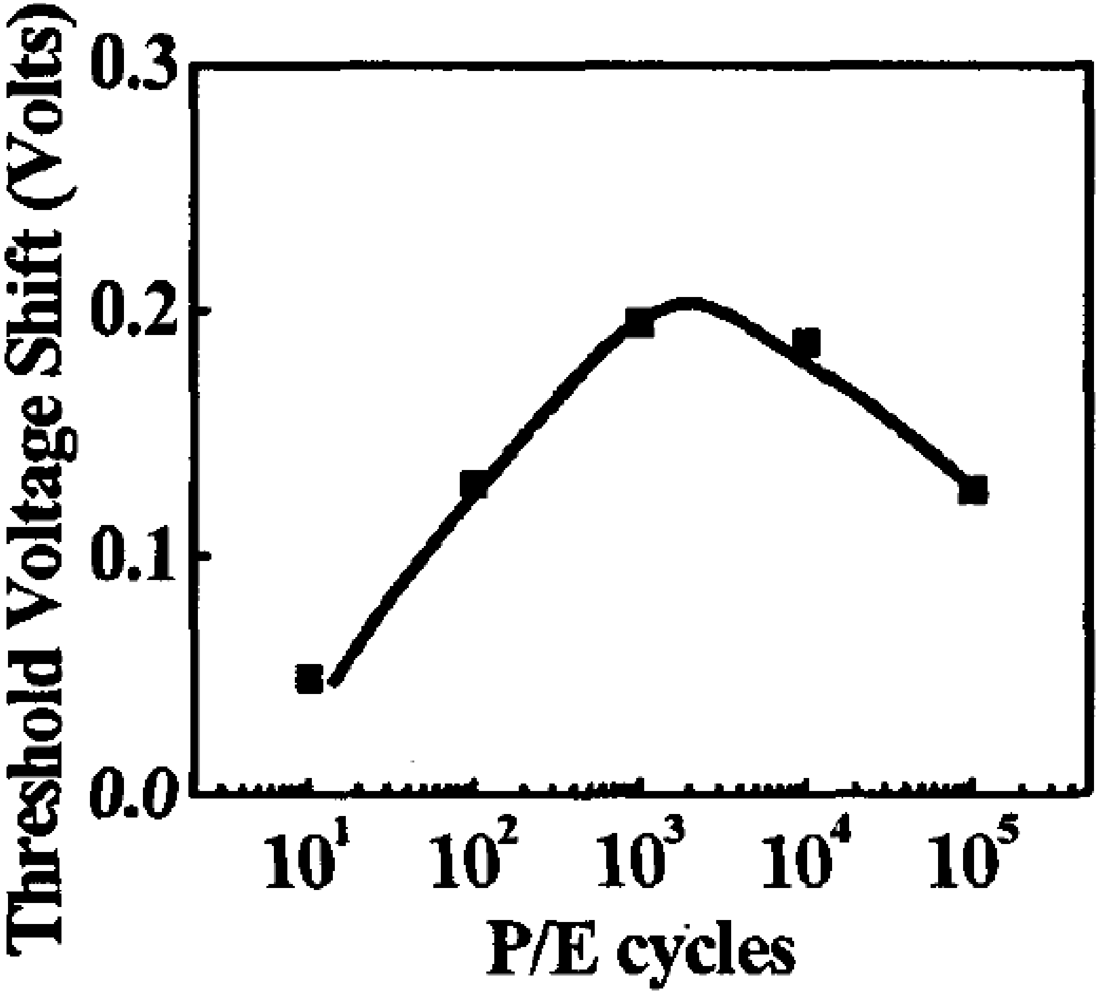


Figure 26 P/E cycle dependence of erase-state Vt drift after 10^4 sec storage

Reference from “Data retention behavior of a SONOS type two-bit storage Flash memory cell,” in *IEDM Tech. Dig.*, 2001, pp. 32.6.1–32.6.4.

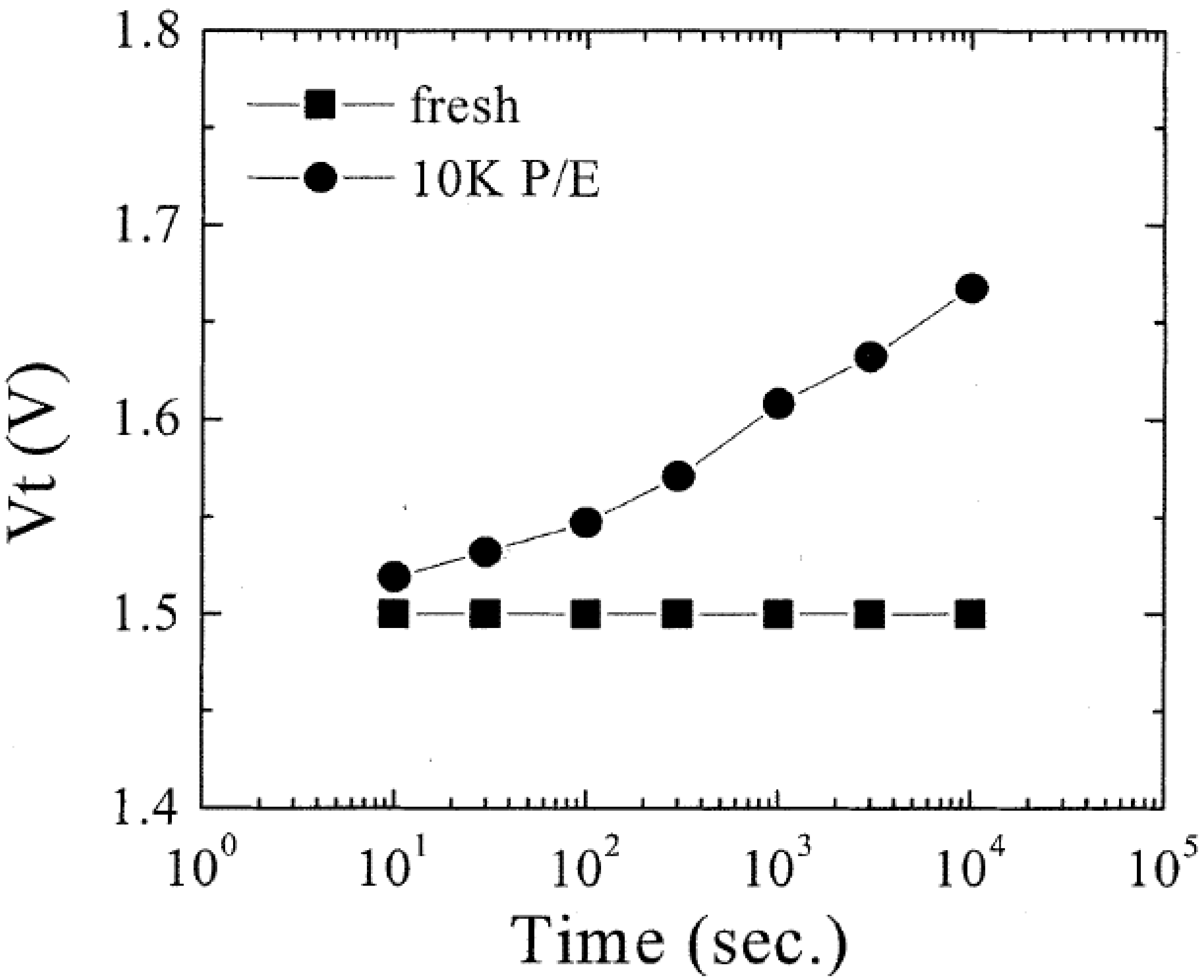


Figure 27 Read disturb characteristics of a fresh cell and a 10-K P/E cycled cell

Reference from “Positive oxide charge-enhanced read disturb in a localized trapping storage flash memory cell,” *IEEE Trans. Electron Devices*, no. 4, pp. 434–439, Apr. 2004

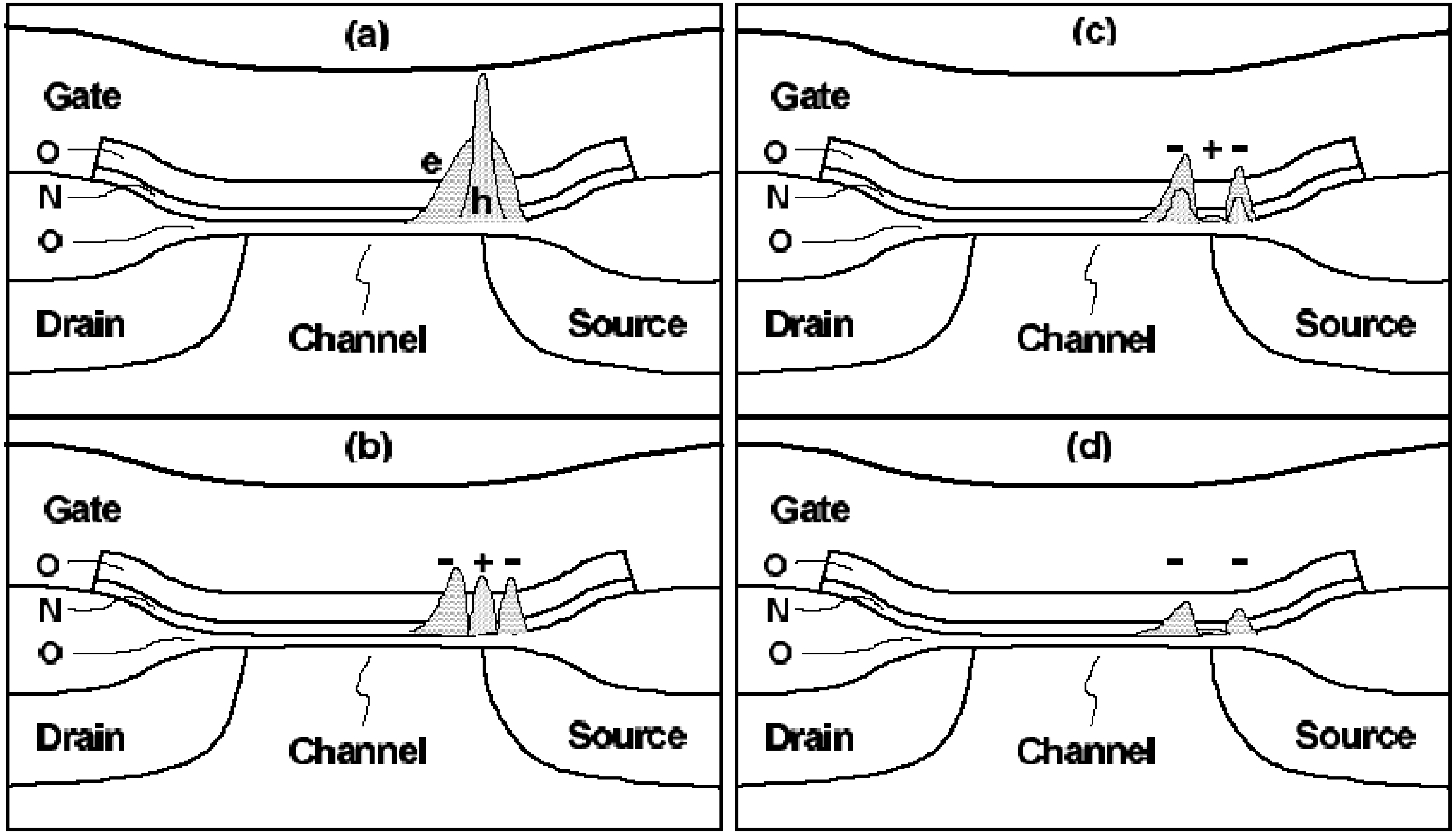


Figure 28 Schematic illustration of the cross section of the spatial distribution of the charge before ((a),(b)) and after ((c),(d)) retention bake

Reference from "Data Retention Reliability Model of NROM Nonvolatile Memory Products"

	A	***B***	***C***	***D***	***E***	***F***	***G***
First passivation layer	LPPEOX (2K)	LPPEOX (2K)	LPPEOX (1K)	LPPEOX (3K)	PESIN (2K)	SION (2K)	LPPEOX (2K)
Second passivation layer	SAUSG	HDP	HDP	HDP	SAUSG	SAUSG	SAUSG
Post annealing after second passivation film	NA	NA	NA	NA	NA	NA	YES
Third passivation layer	PESIN	PESIN	PESIN	PESIN	PESIN	PESIN	PESIN

Table 2 Passivation layer experiment condition (A is standard condition)

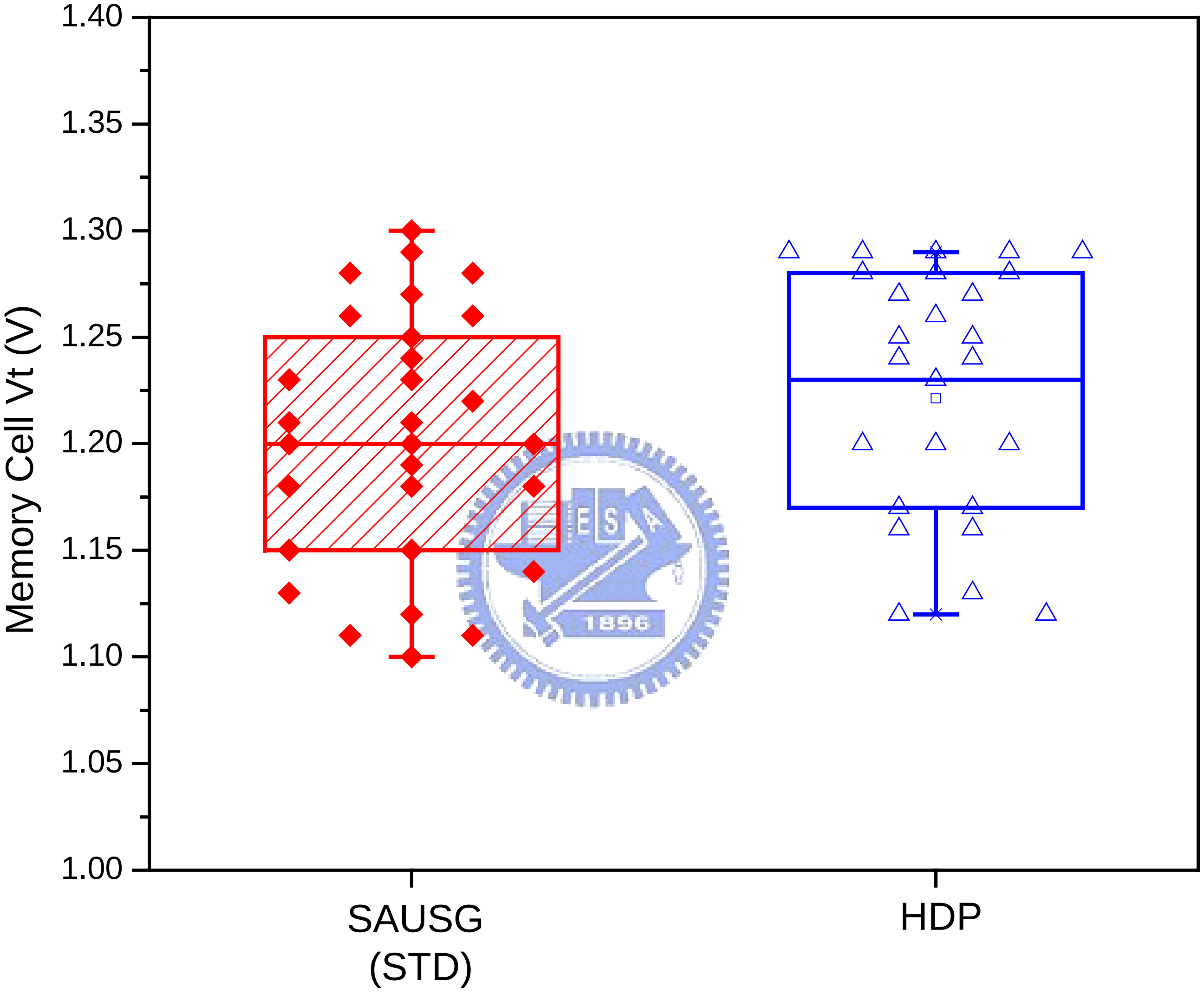


Figure 29 Vt compare of SAUSG and HDP experiment in WAT test key

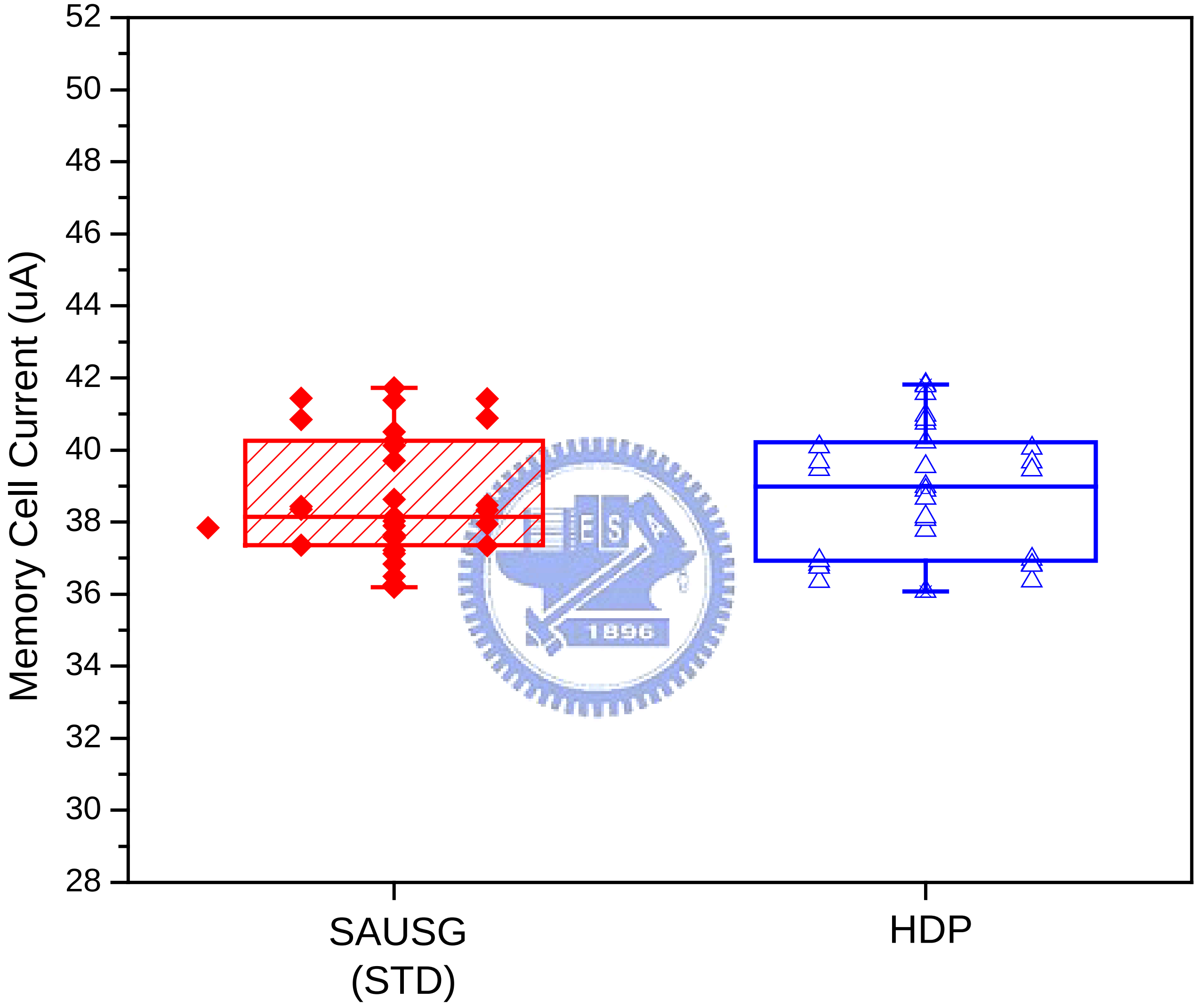


Figure 30 Cell current compare of SAUSG and HDP experiment in WAT test key

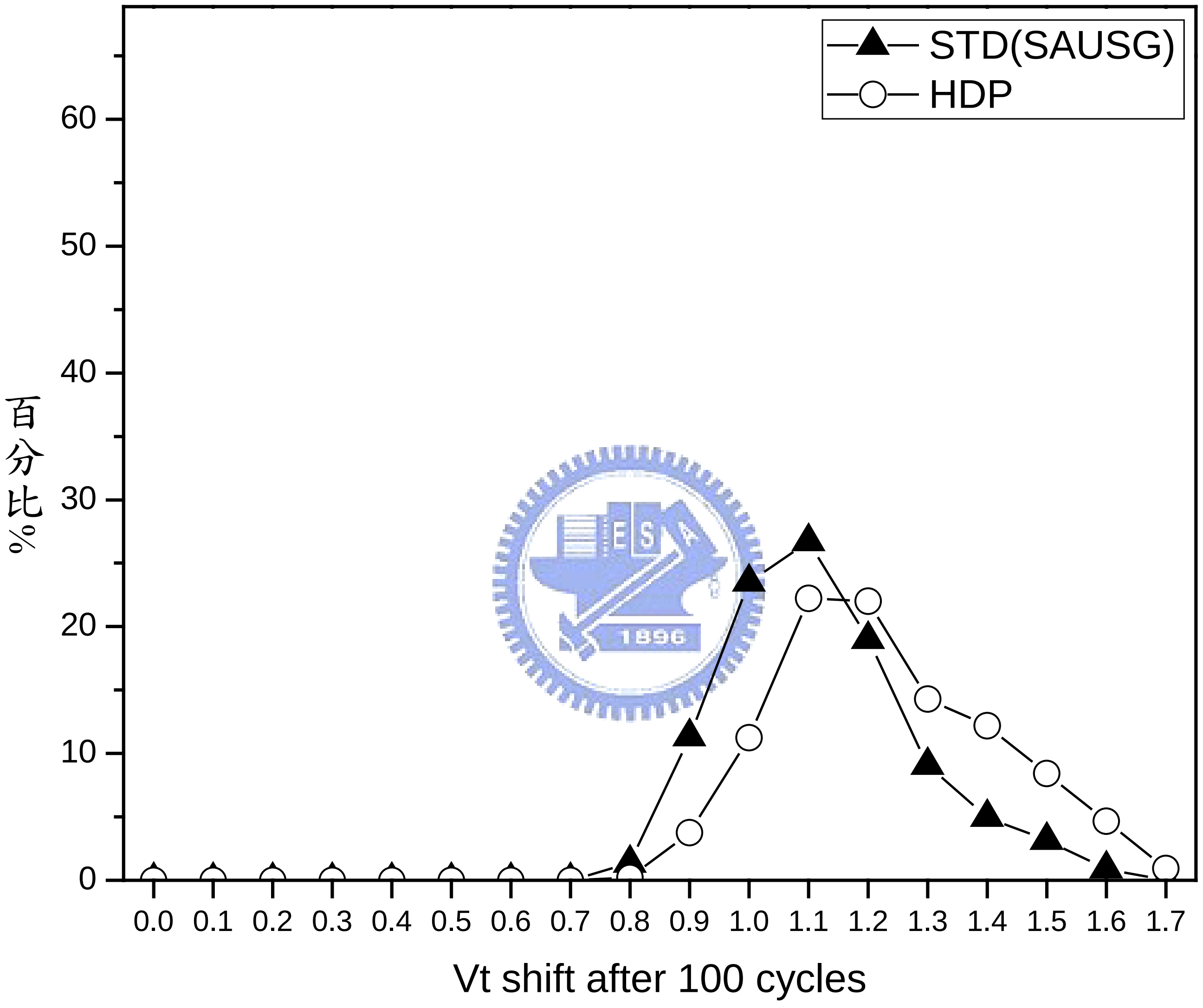


Figure 31 Vt shift distribution of SAUSG and HDP experiment after 100 cycles

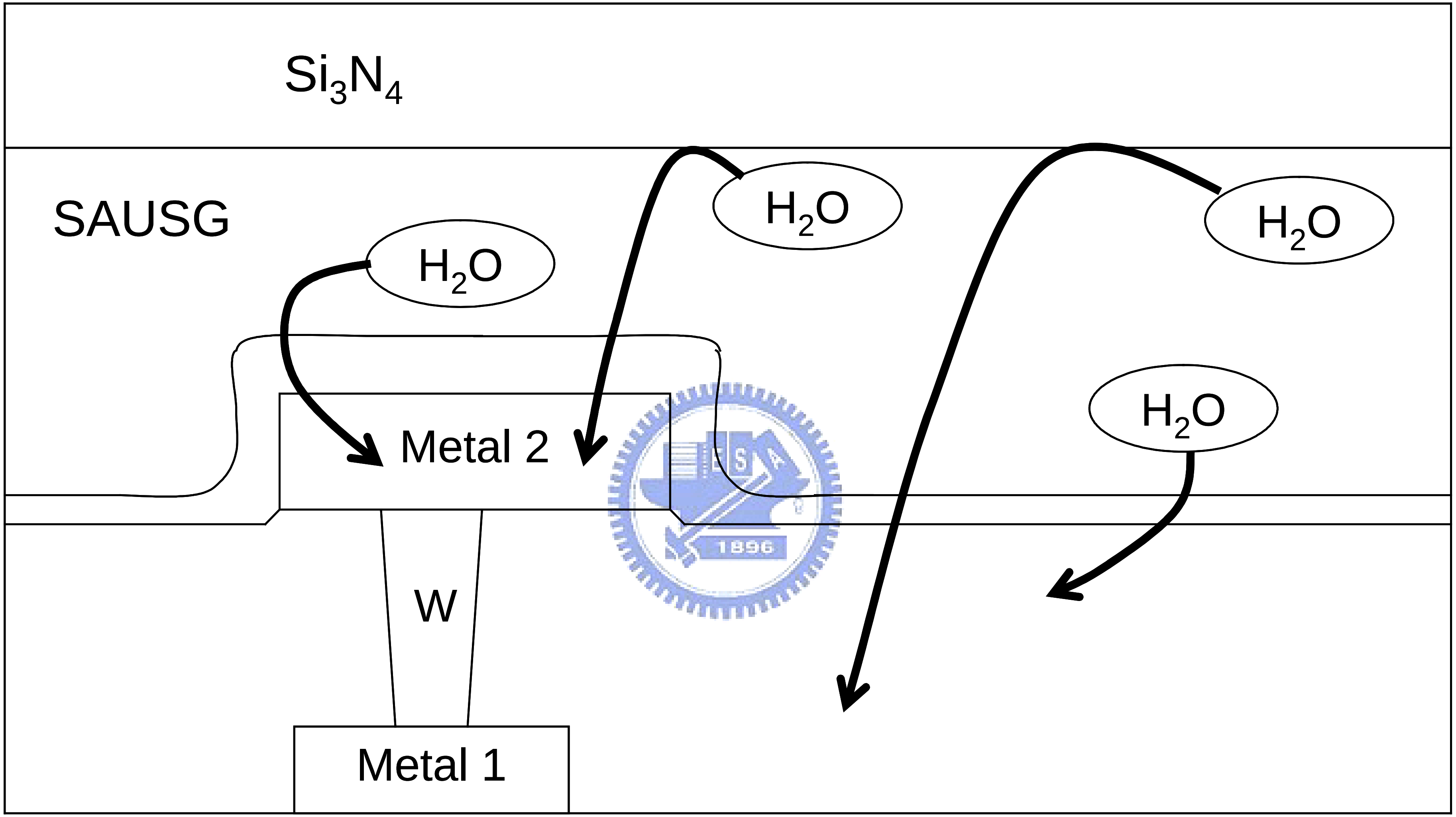


Figure 32 Illustration of moisture diffusion with first passivation film using LP-PEOX

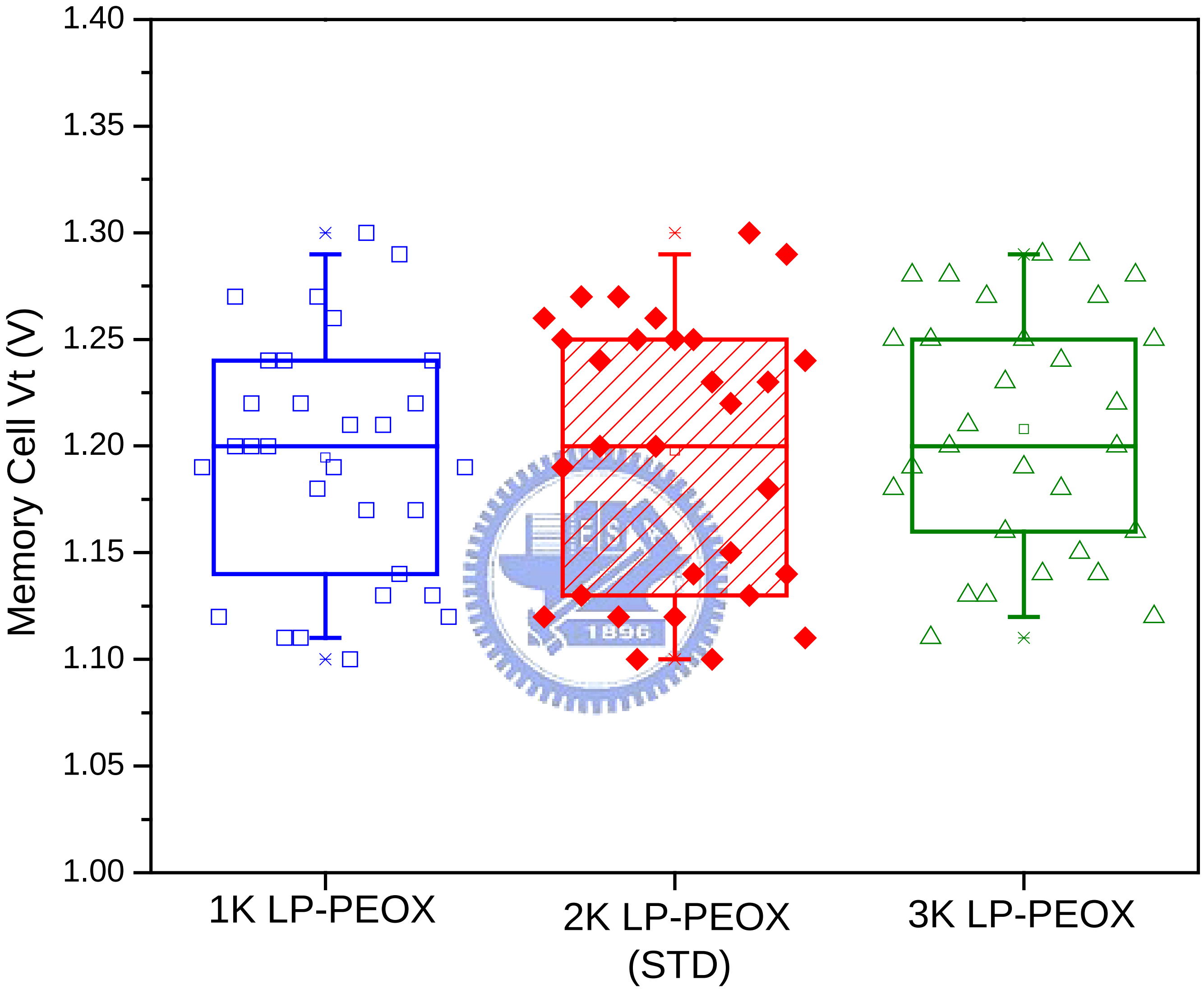


Figure 33 Vt compare of different LP-PEOX thickness experiment in WAT test key

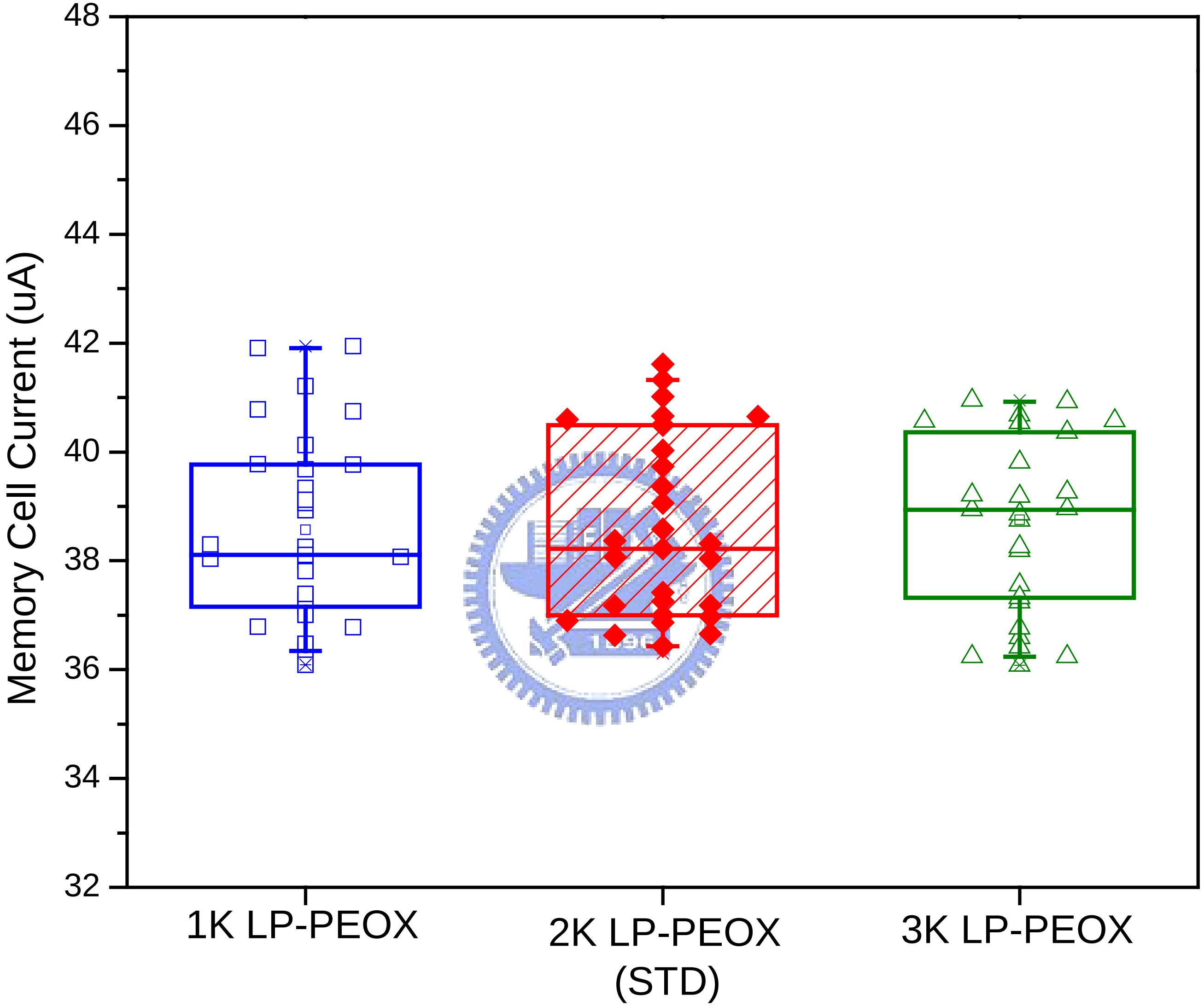


Figure 34 Cell current compare of different LP-PEOX thickness experiment in WAT test key

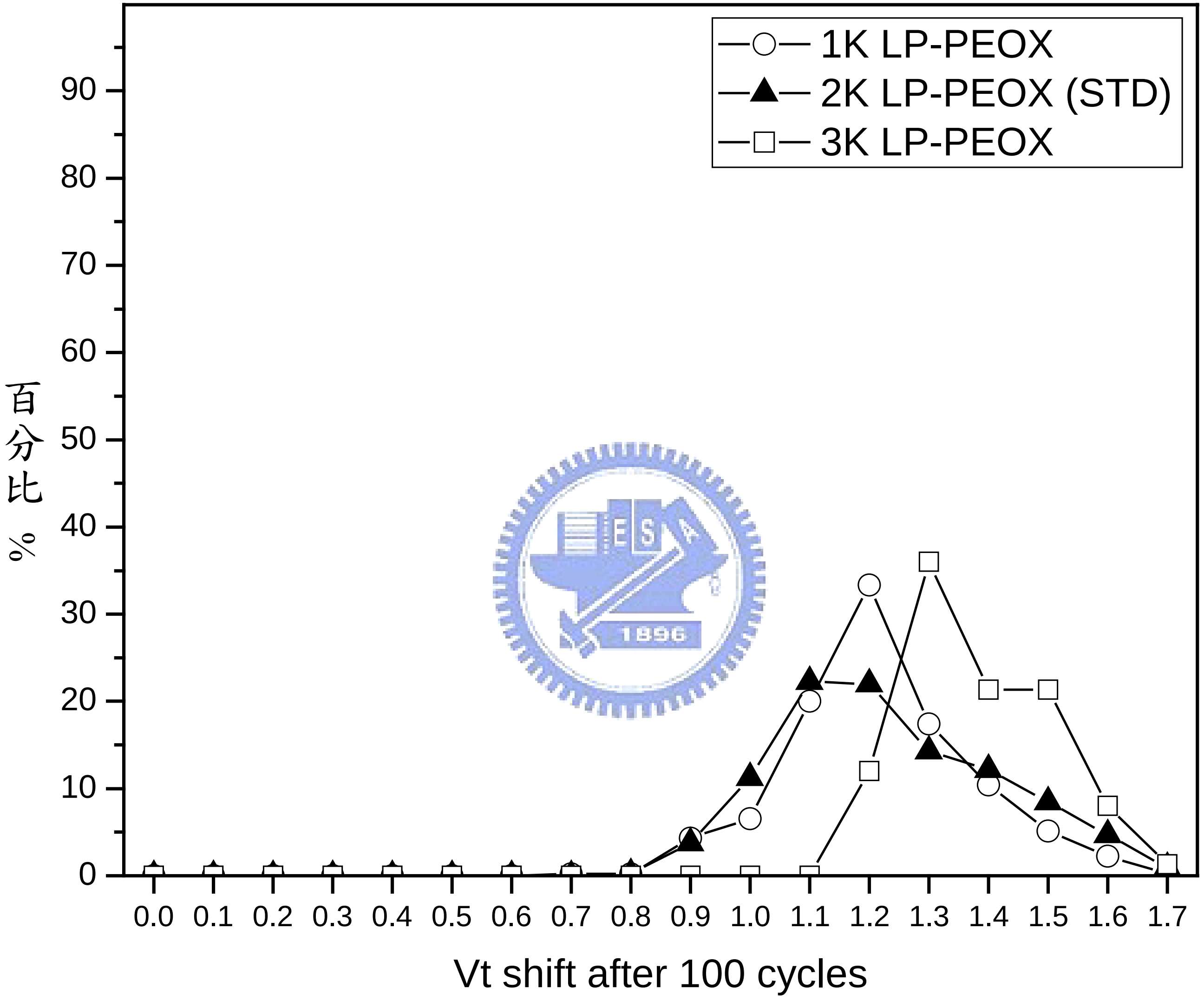


Figure 35 Vt shift distribution of dfferent LP-PEOX thickness experiment after 100 cycles

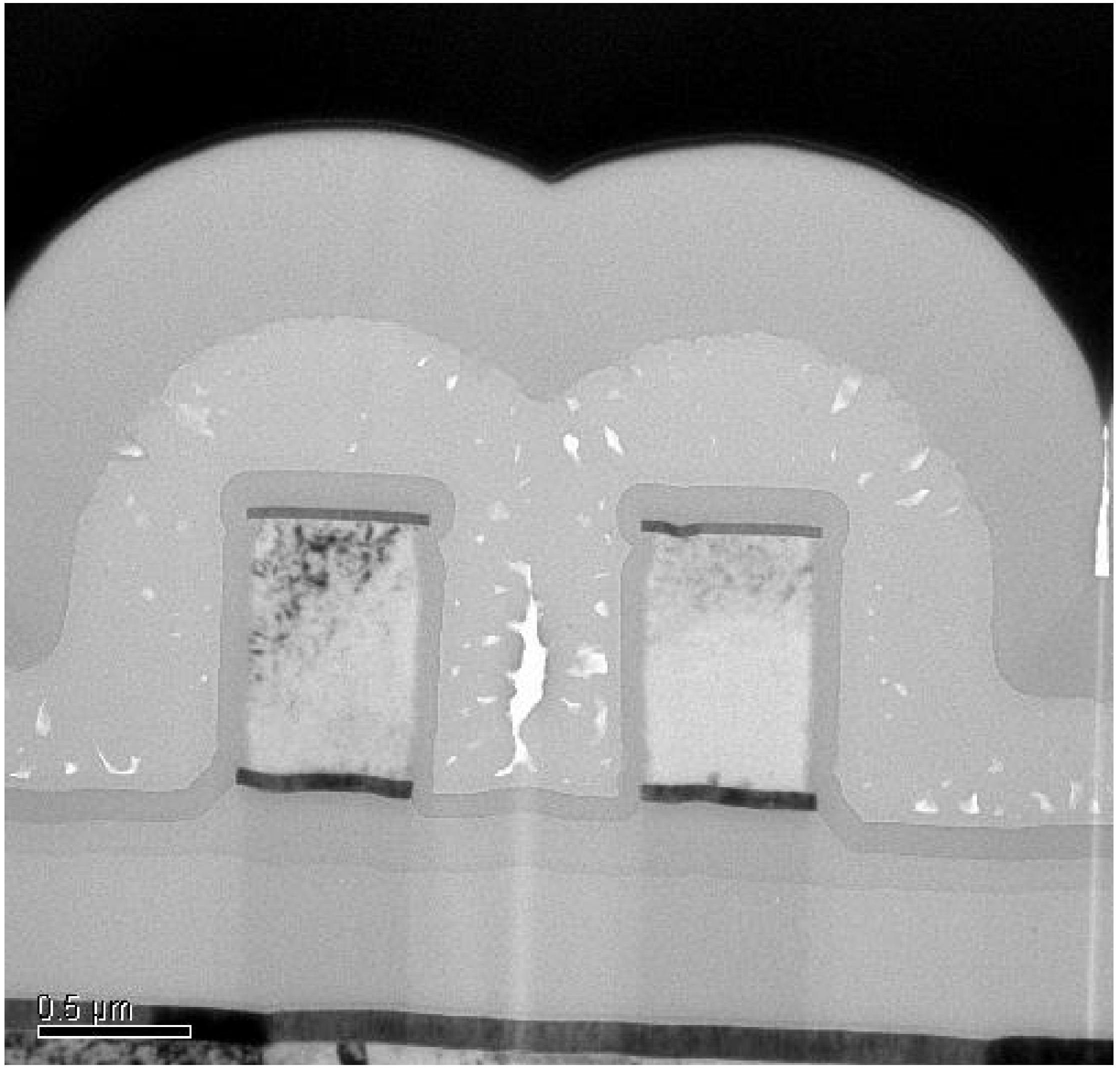


Figure 36 TEM of passivation film structure

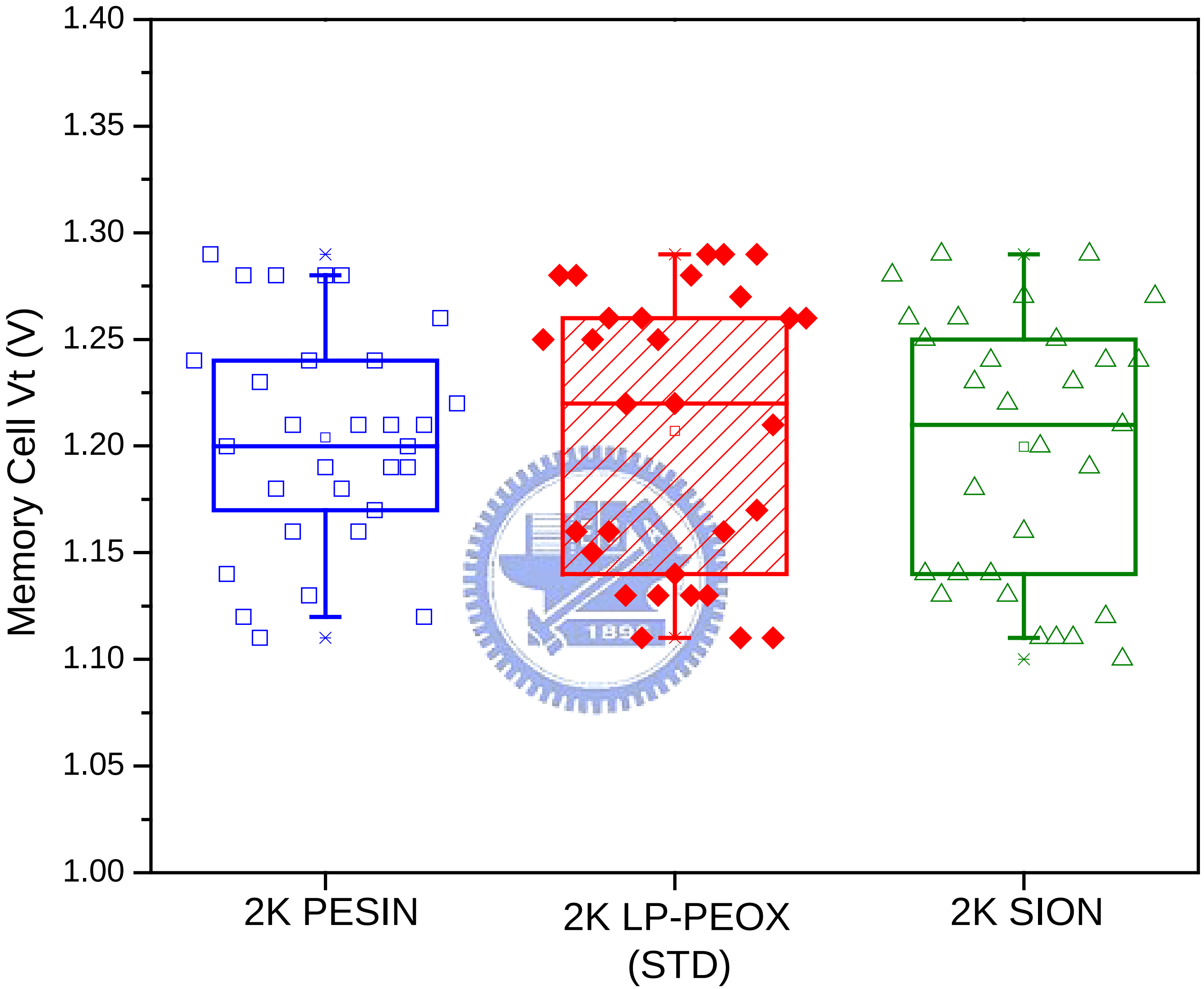


Figure 37 Vt compare of different passivation film material experiment in WAT test key

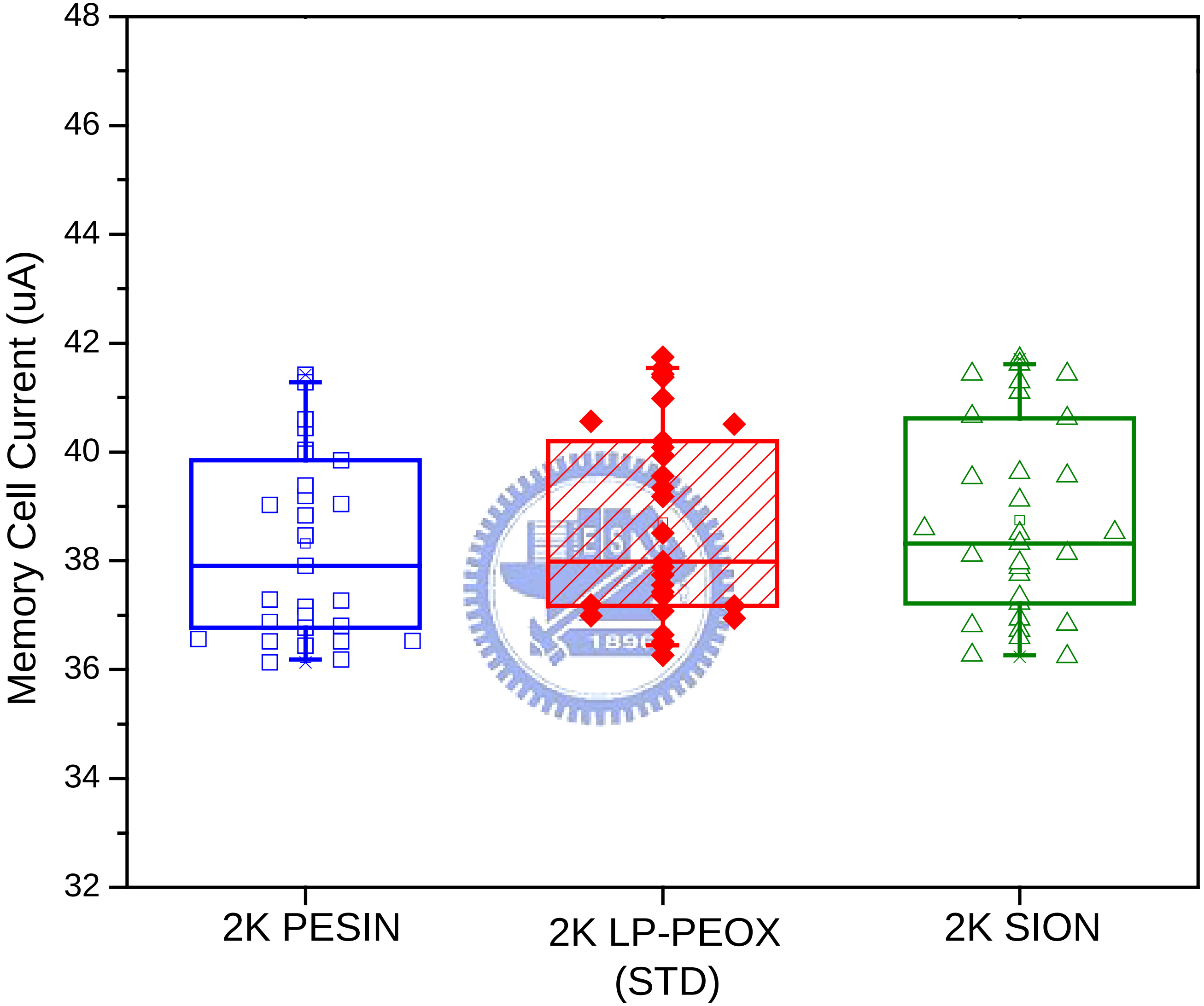


Figure 38 Cell current compare of different passivation film material experiment in WAT test key

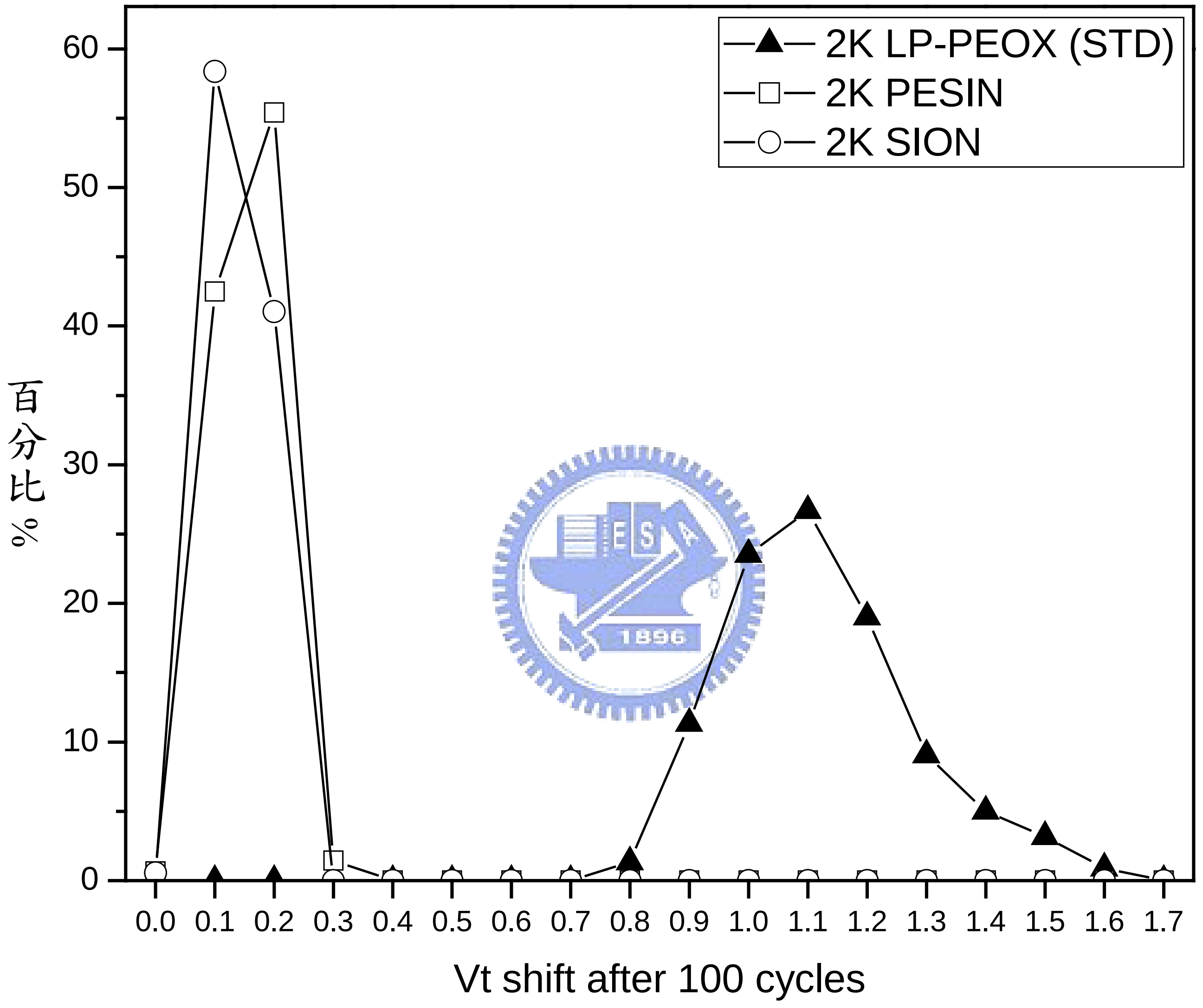


Figure 39 Vt shift distribution of different passivation film material experiment after 100 cycles

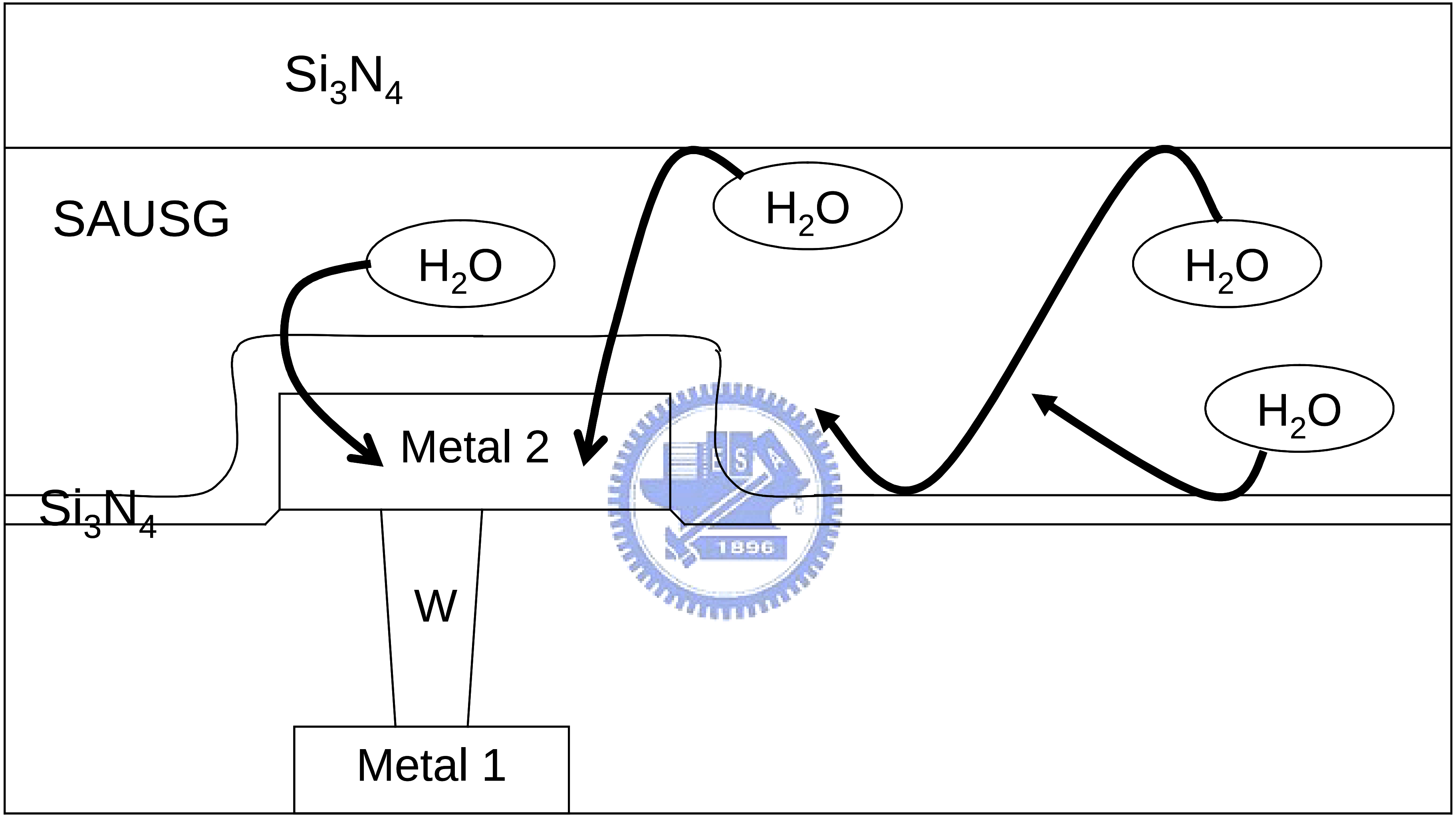


Figure 40 Illustration of moisture diffusion with first passivation film using Si_3N_4

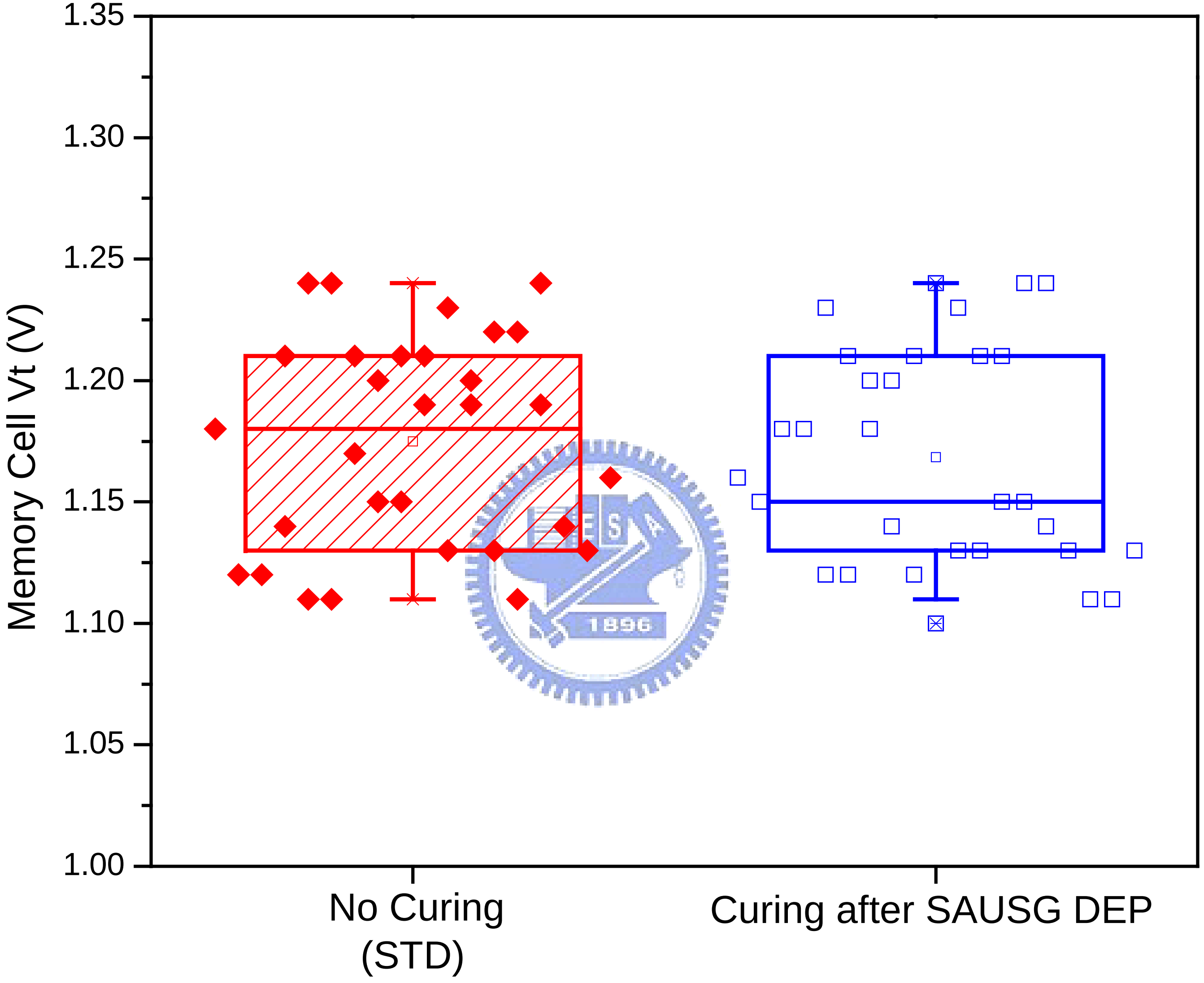


Figure 41 Vt compare of curing after SAUSG DEP experiment in WAT test key

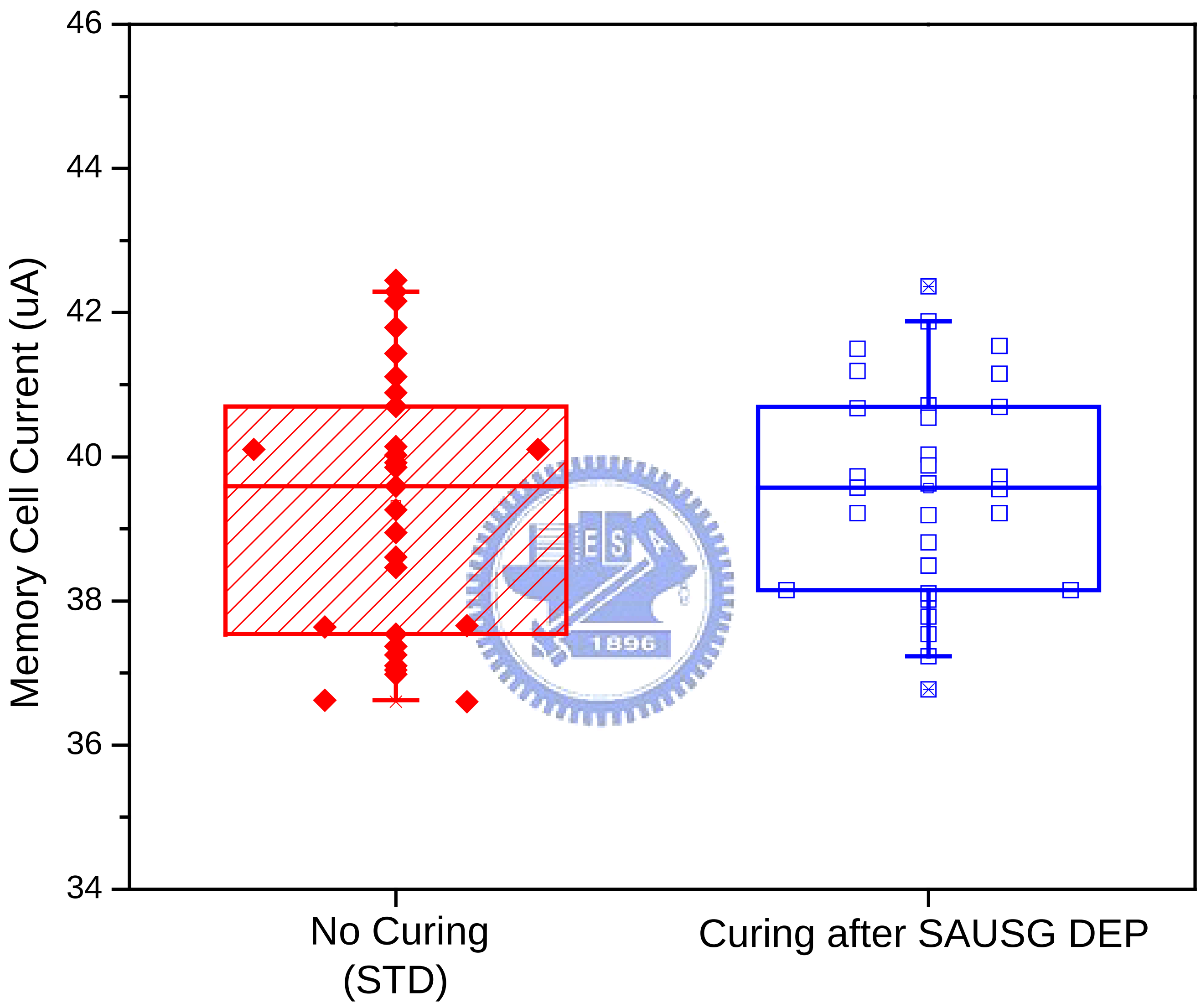


Figure 42 Cell current compare of curing after SAUSG DEP experiment in WAT test key

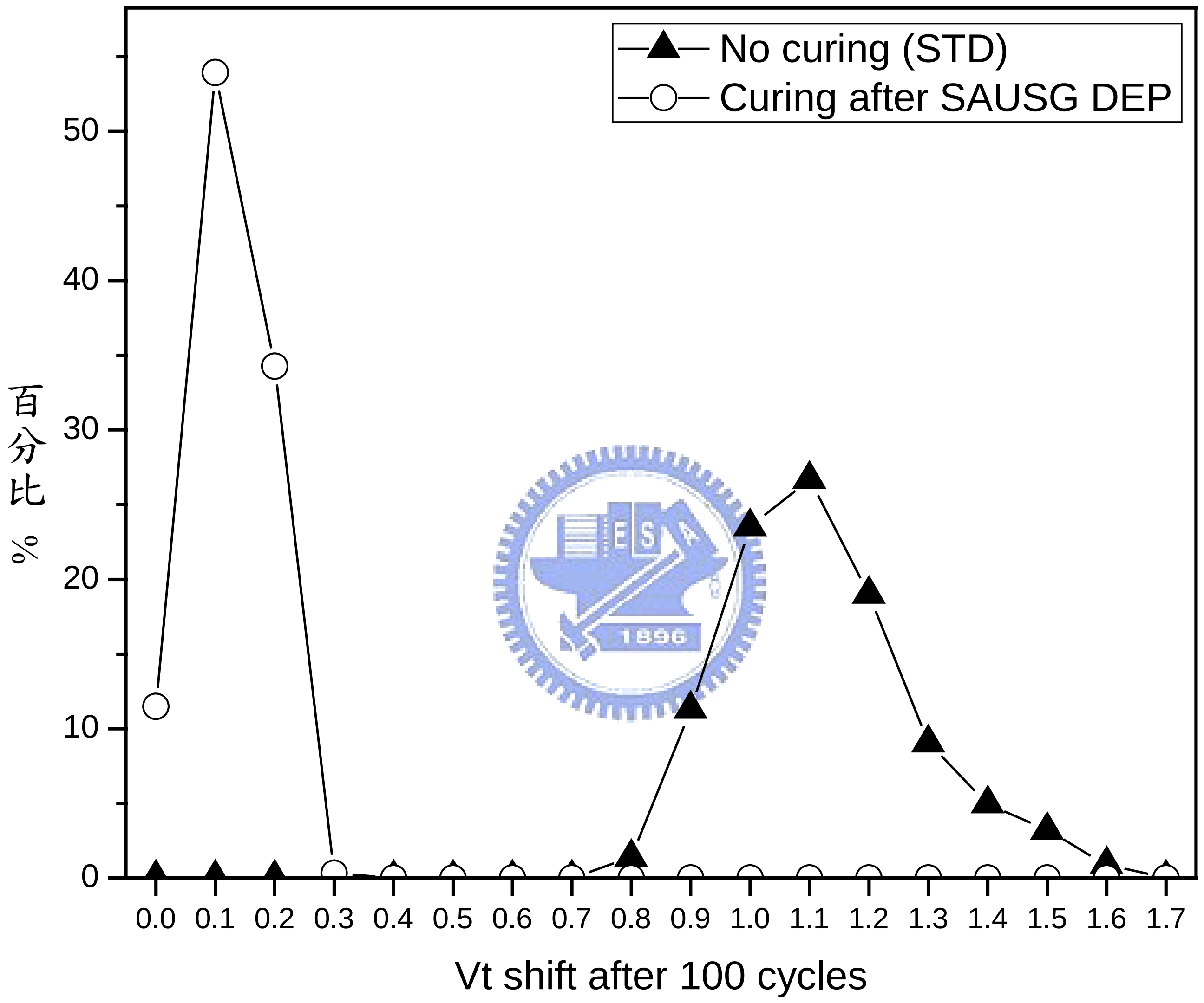


Figure 43 Vt shift distribution of curing after SAUSG DEP experiment after 100 cycles

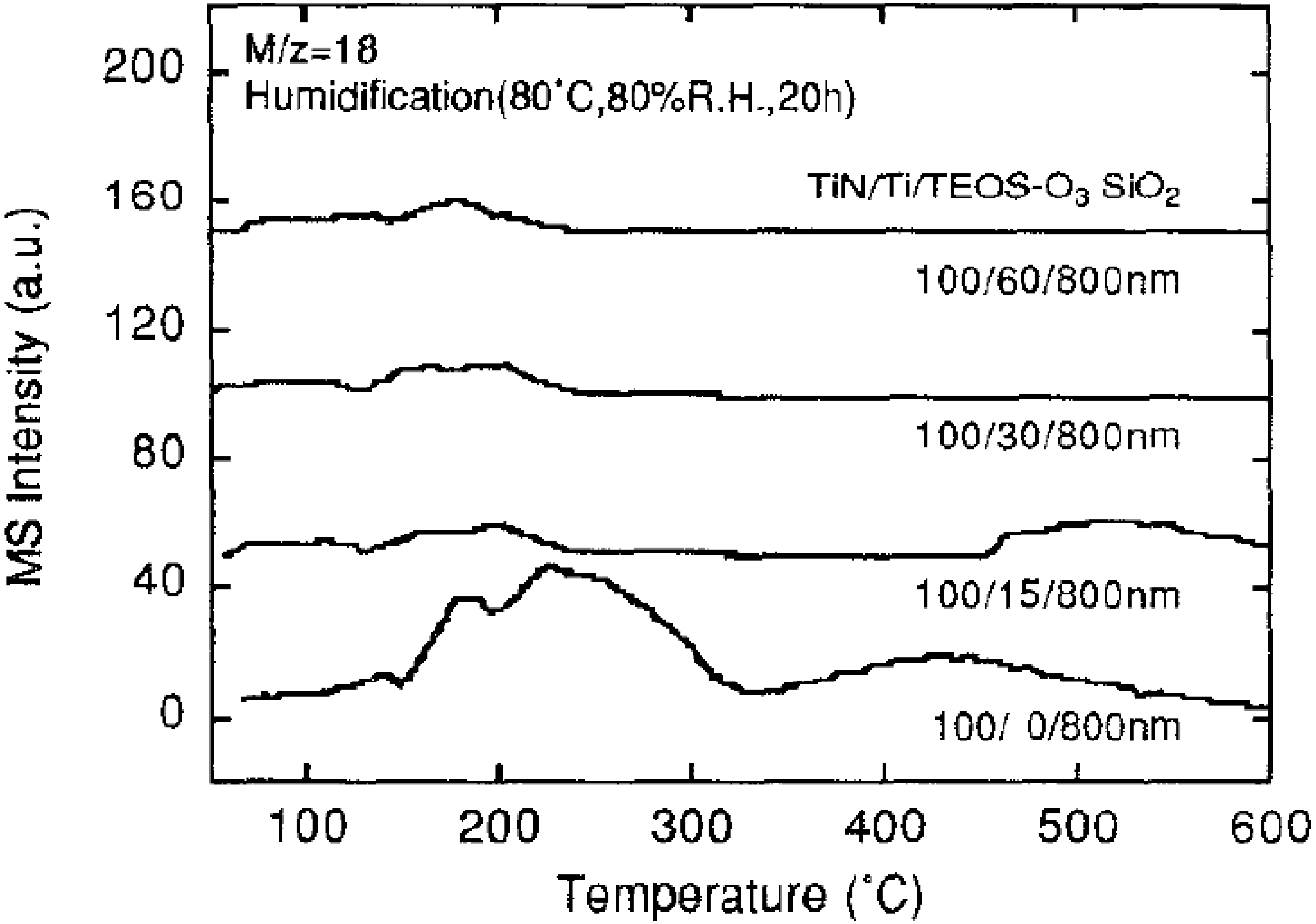


Figure 44 TDS spectra of water desorbed from TiN/Ti/TEOS-O_3 SiO_2, with various Ti thickness.

Reference from “Deoxidization of Wafer Desorbed from APCVD TEOS-O_3 SiO_2 by Titanium Cap Layer,” *Reliability Physics Symposium, 1995. 33rd Annual Proceedings., IEEE International 4-6 April 1995*

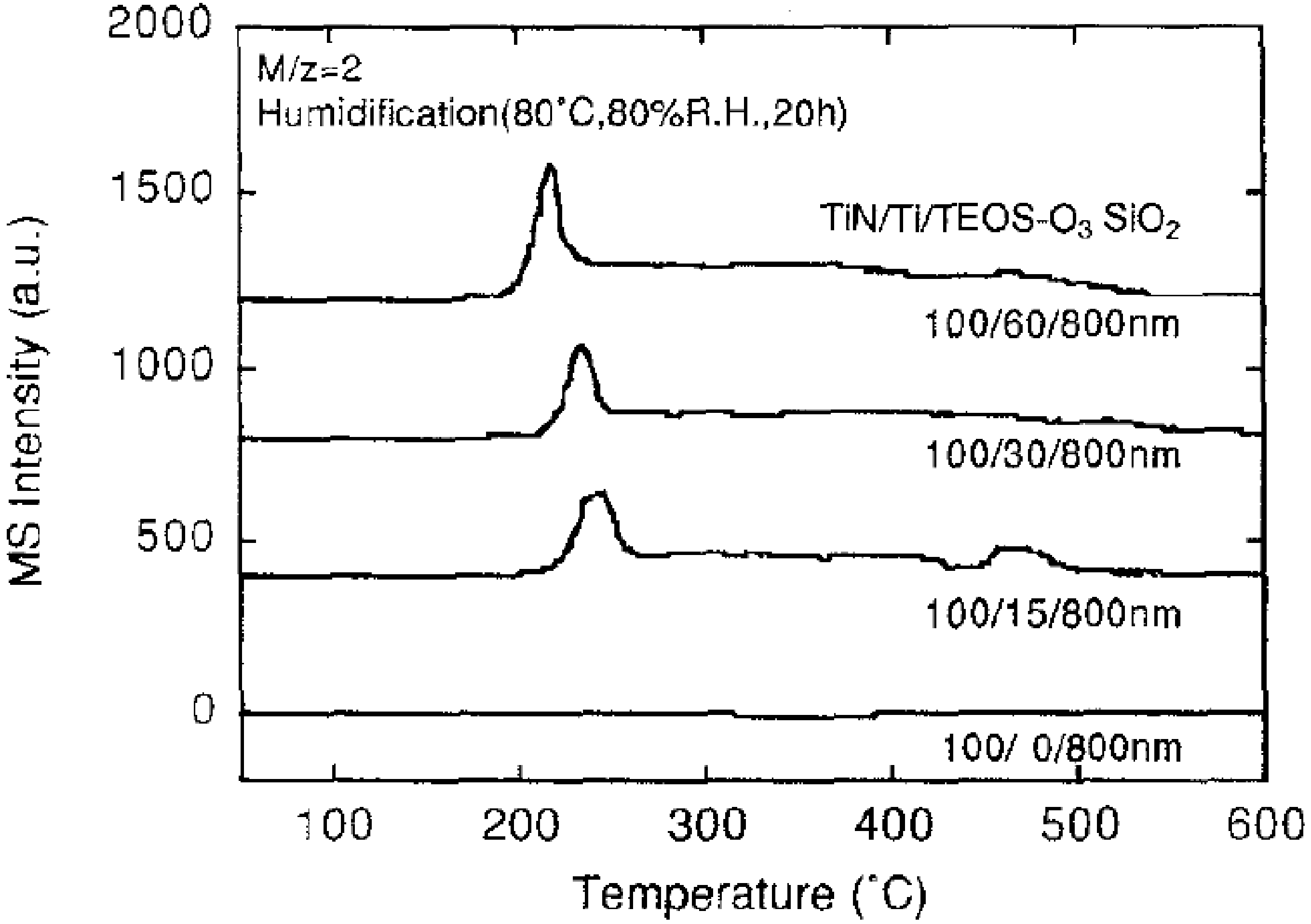
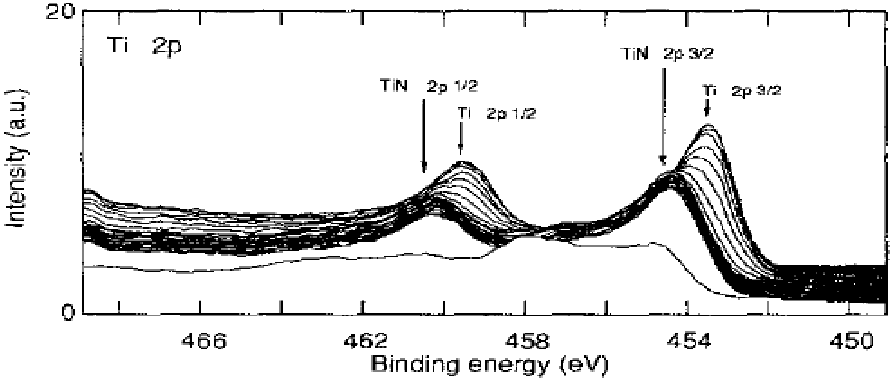
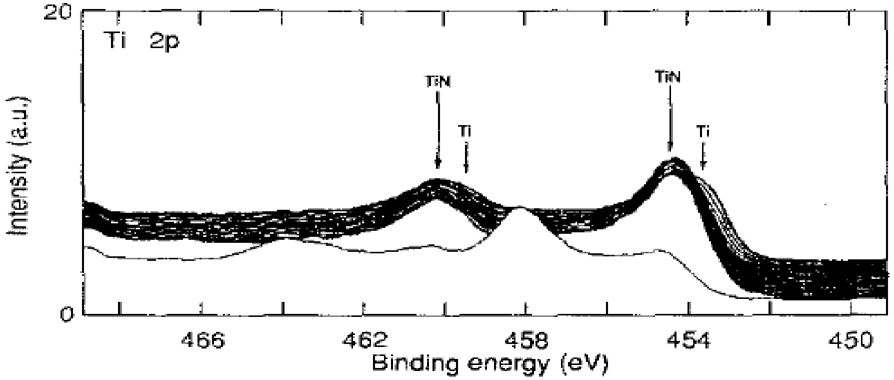


Figure 45 TDS spectra of hydrogen desorbed from TiN/Ti/TEOS-O_3 SiO_2, with various Ti thickness.

Reference from “Deoxidization of Wafer Desorbed from APCVD TEOS-O_3 SiO_2 by Titanium Cap Layer,” *Reliability Physics Symposium, 1995. 33rd Annual Proceedings., IEEE International 4-6 April 1995*



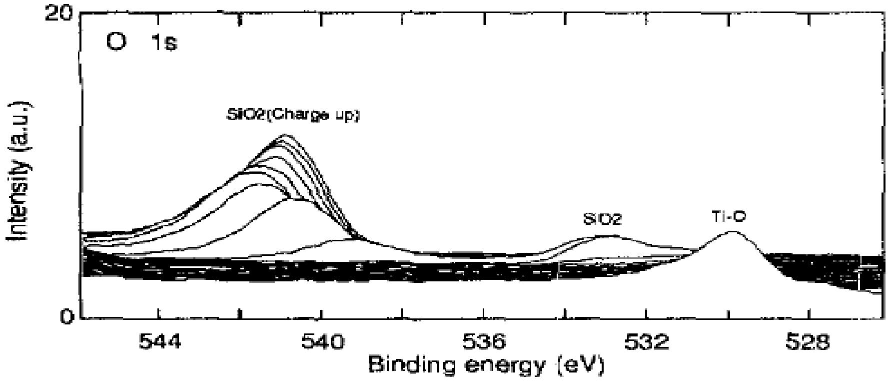
(a) Before TDS measuremen



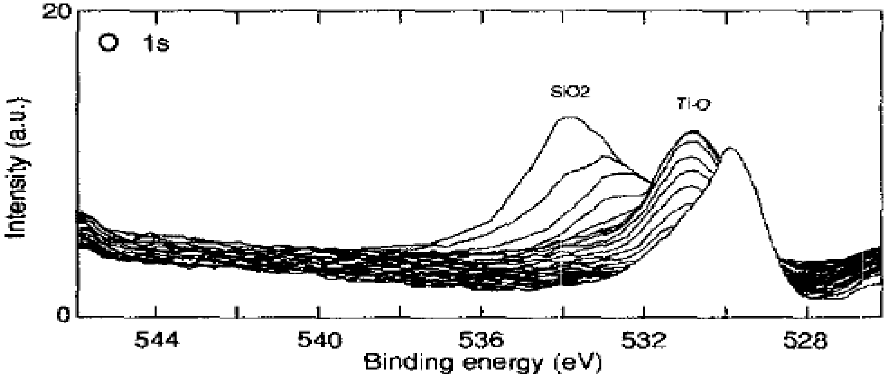
(b) After TDS measurement

Figure 46 Depth profiles of Ti 2p XPS-spectra for TiN/Ti/TEOS-O_3 SiO_2, before and after TDS Measurment, (a)before TDS measurement, (b)after TDS measurement

Reference from “Deoxidization of Wafer Desorbed from APCVD TEOS-O_3 SiO_2 by Titanium Cap Layer,” *Reliability Physics Symposium, 1995. 33rd Annual Proceedings., IEEE International 4-6 April 1995*



(a) Before TDS measurement



(b) After TDS measurement

Figure 47 Depth profiles of O 1s XPS-spectra for TiN/Ti/TEOS-O_3 SiO_2, before and after TDS Measurment, (a)before TDS measurement, (b)after TDS measurement

Reference from “Deoxidization of Wafer Desorbed from APCVD TEOS-O_3 SiO_2 by Titanium Cap Layer,” *Reliability Physics Symposium, 1995. 33rd Annual Proceedings., IEEE International 4-6 April 1995*

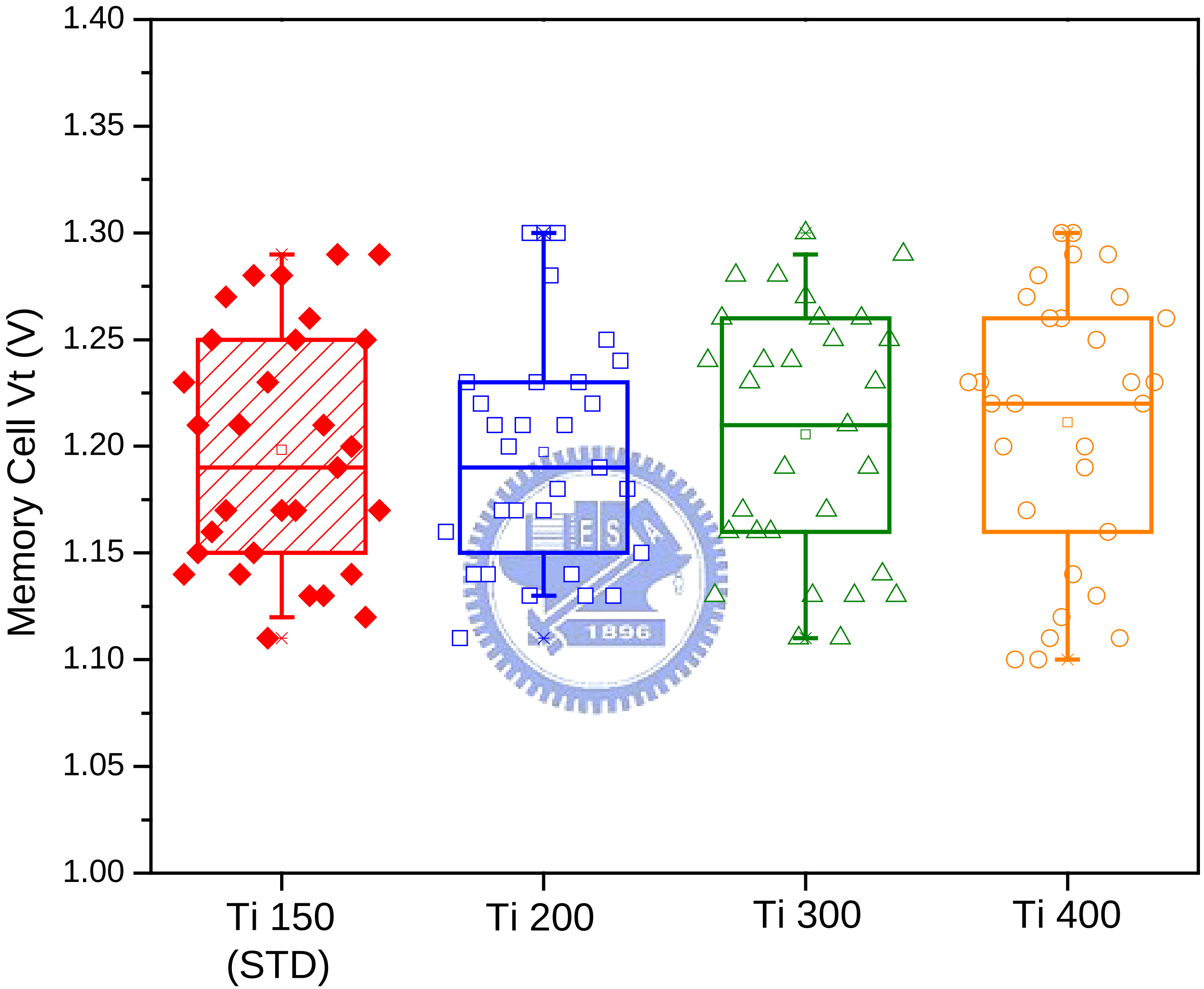


Figure 48 Vt compare of different Ti thickness experiment with old passivation film in WAT test key

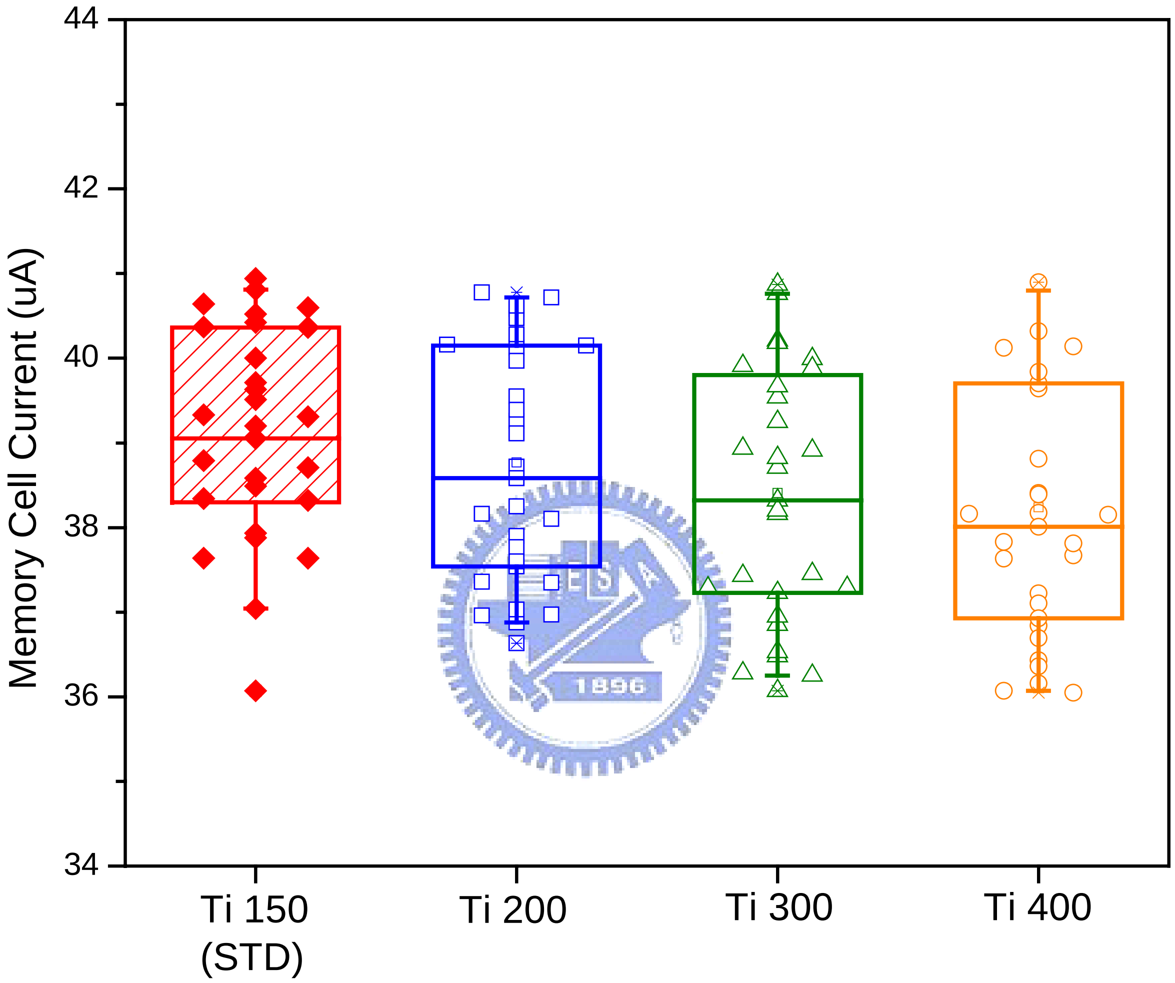


Figure 49 Cell current compare of different Ti thickness experiment with old passivation film in WAT test key

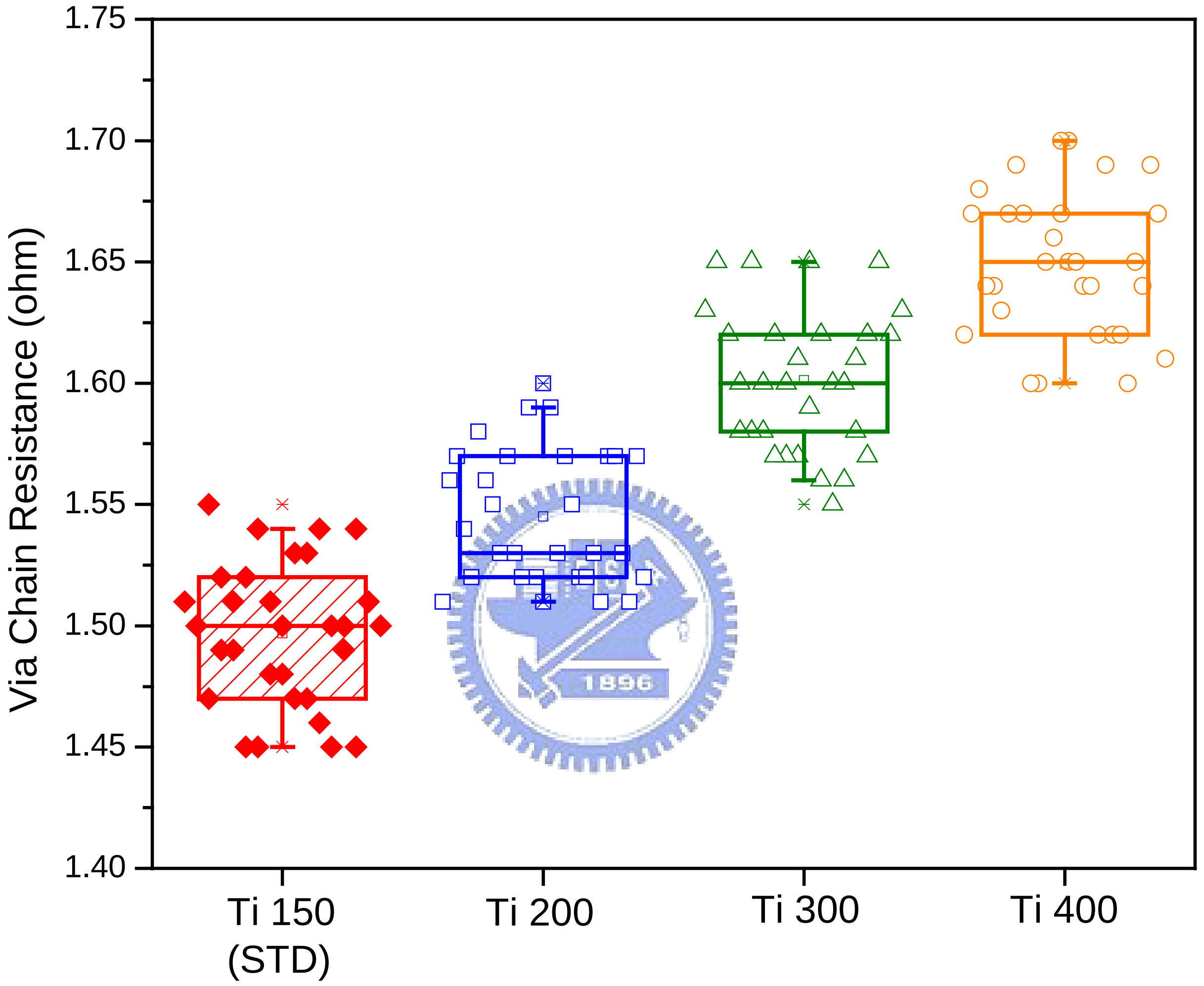


Figure 50 Via chain resistance compare of different Ti thickness experiment with old passivation film in WAT test key

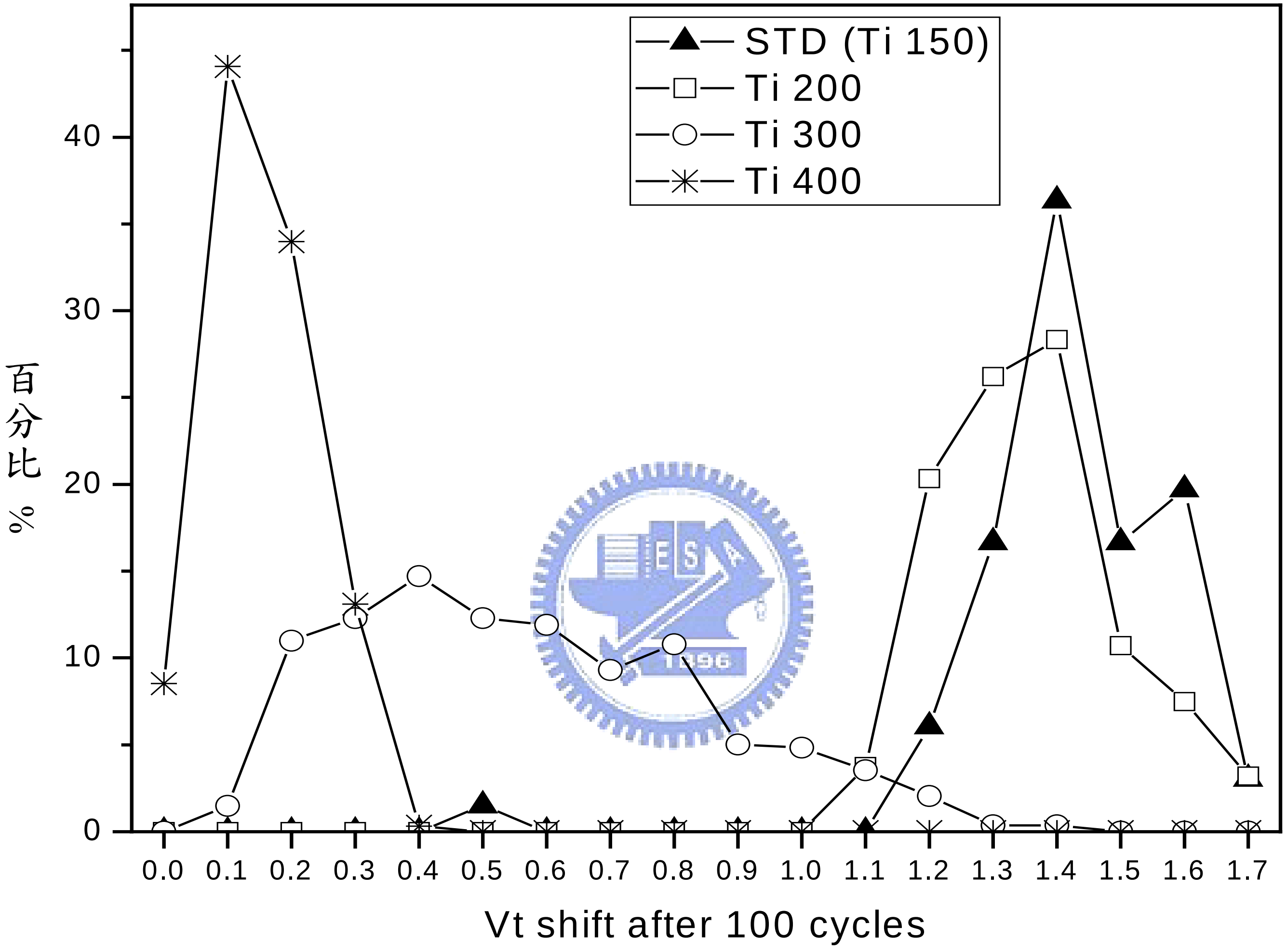


Figure 51 Vt shift distribution of different Ti thickness experiment with old passivation film after 100 cycles

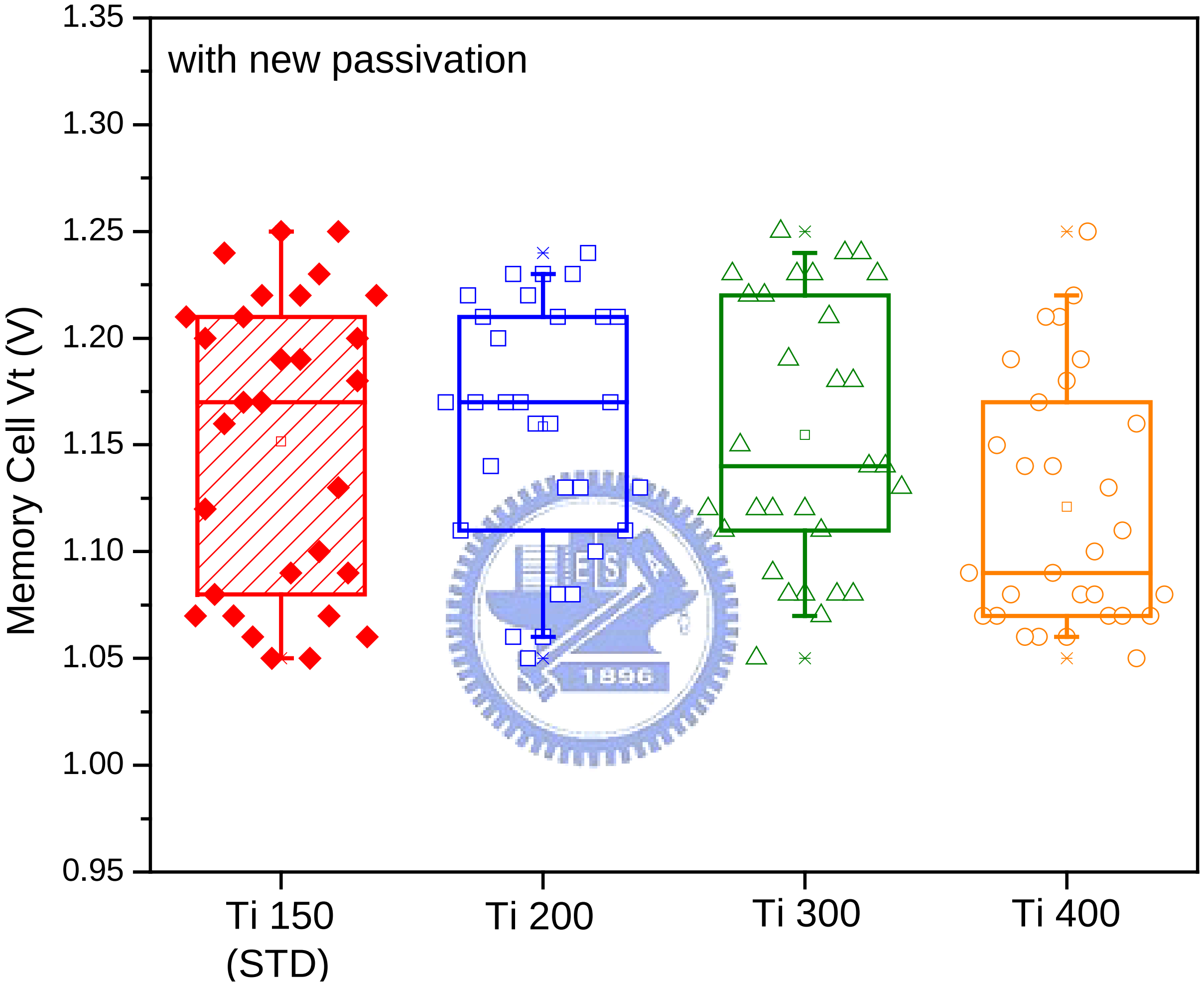


Figure 52 Vt compare of different Ti thickness experiment with new passivation film in WAT test key

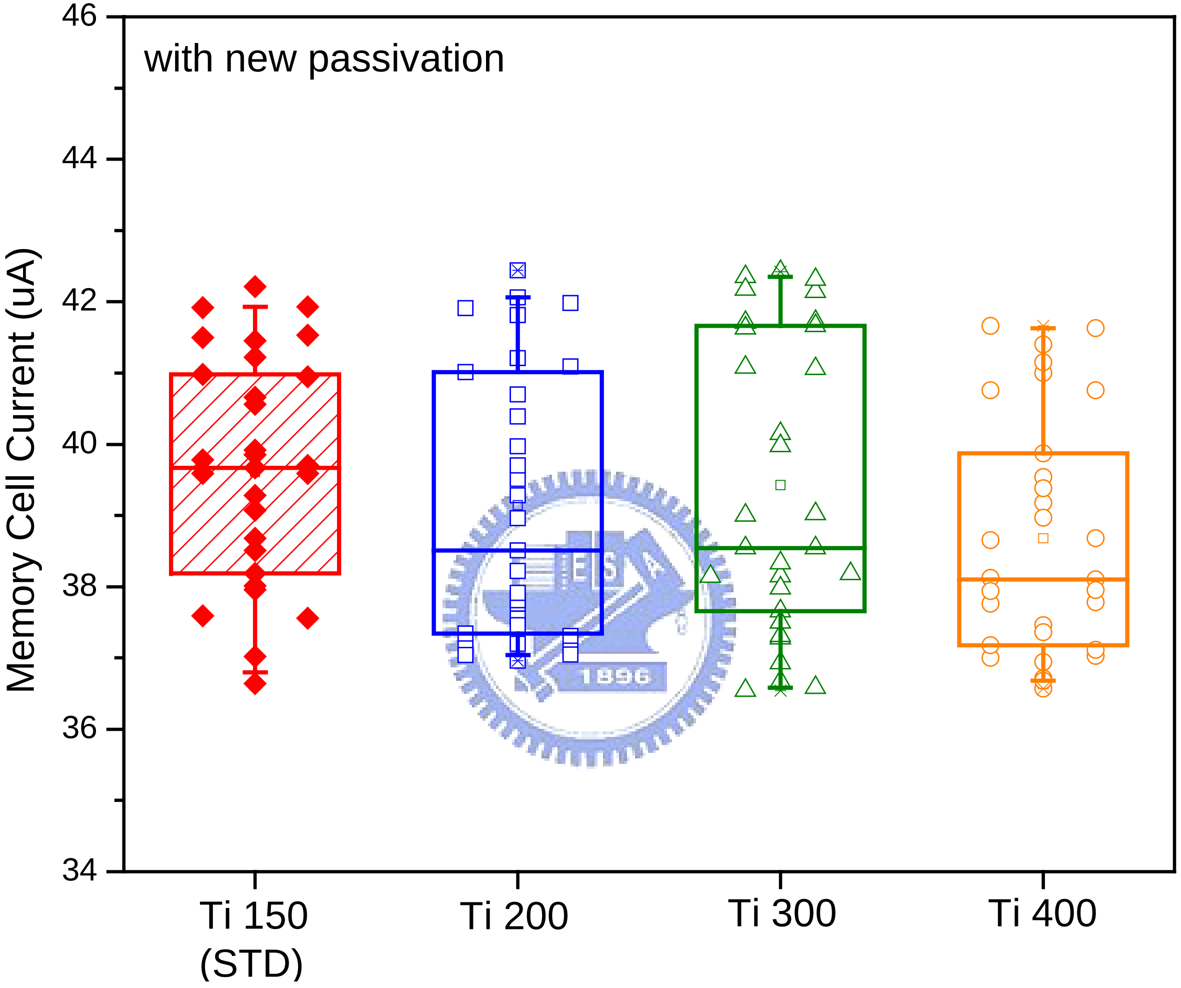


Figure 53 Cell current compare of different Ti thickness experiment with new passivation film in WAT test key

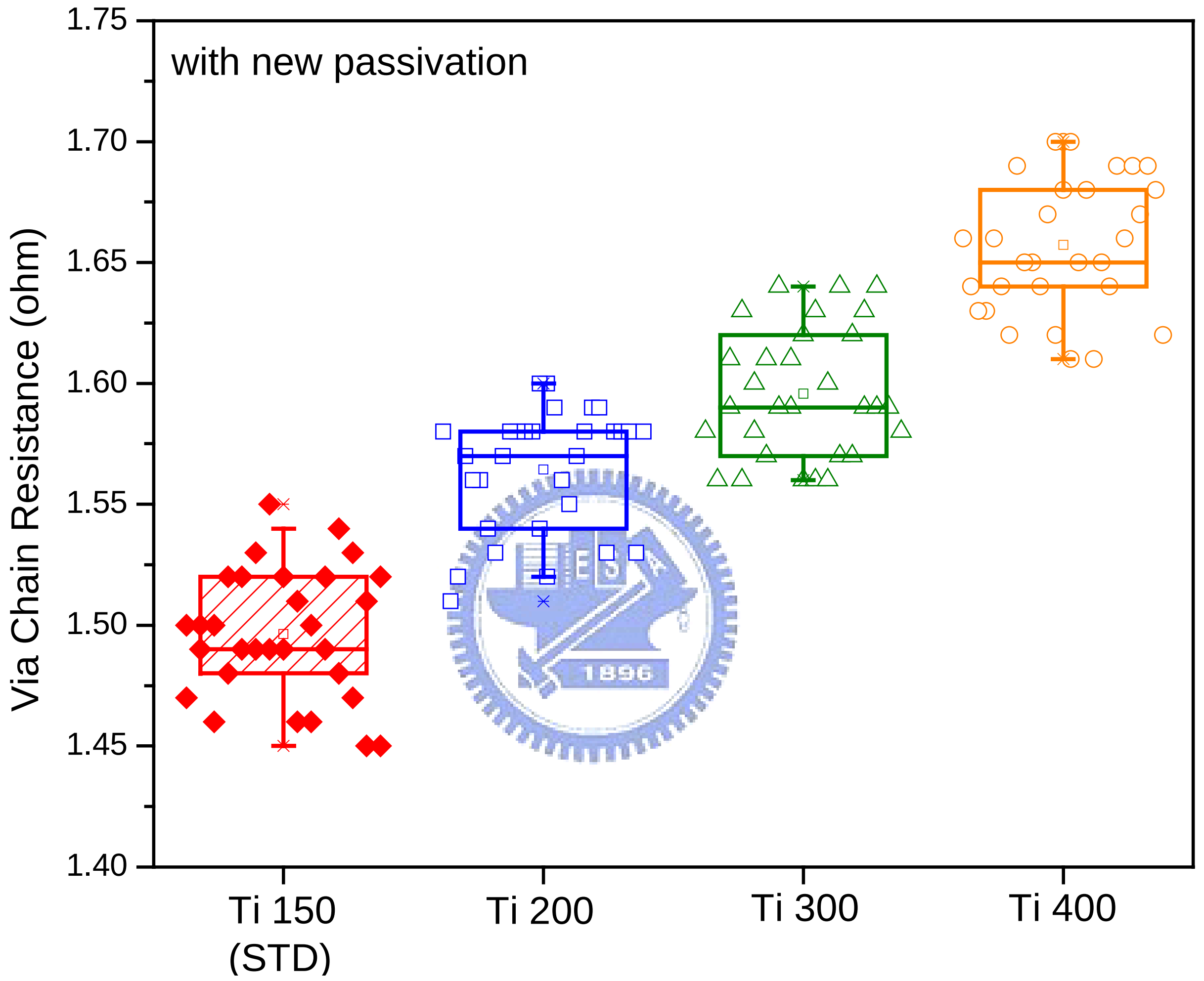


Figure 54 Via chain resistance compare of different Ti thickness experiment with new passivation film in WAT test key

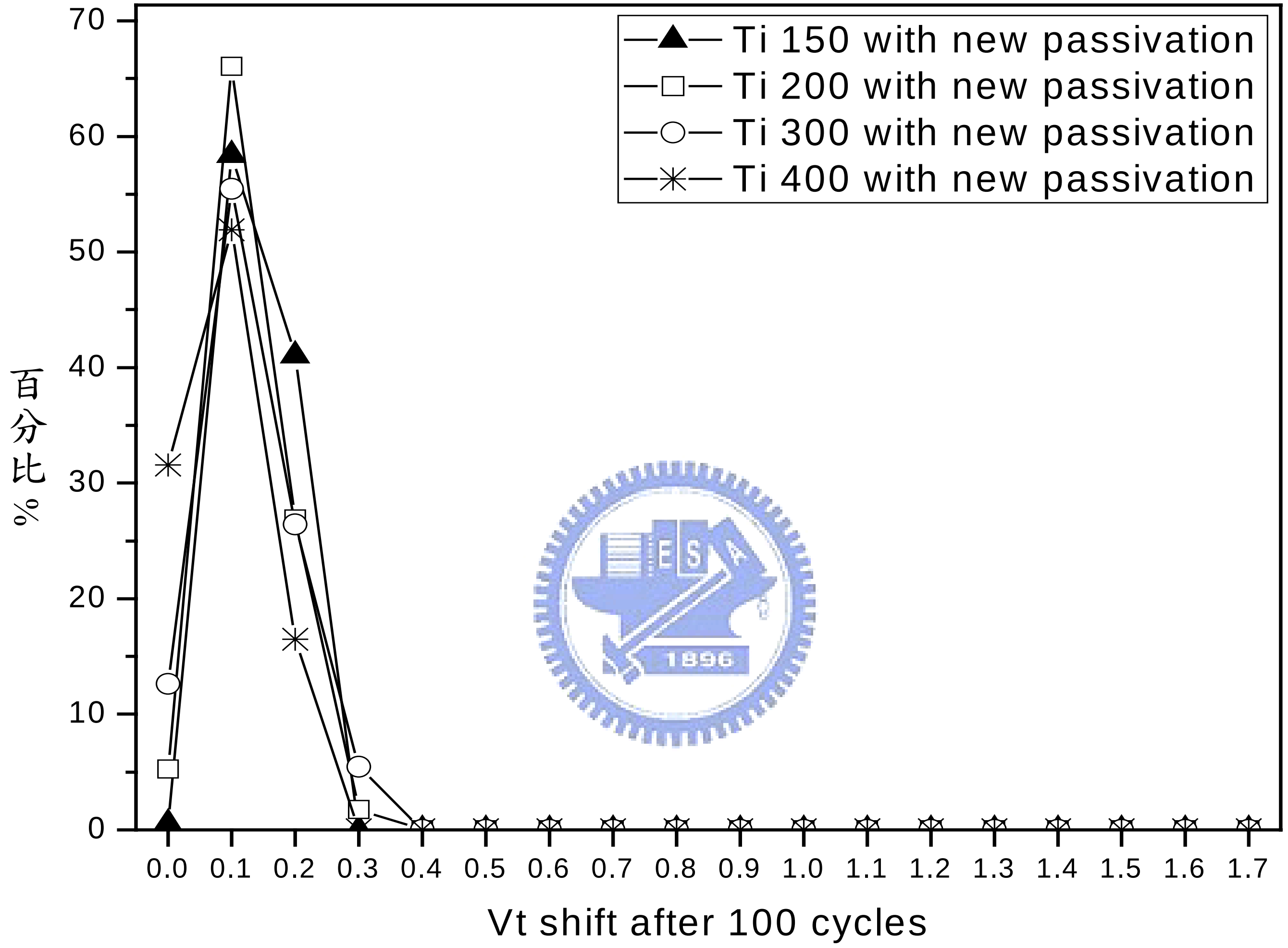


Figure 55 Vt shift distribution of different Ti thickness experiment with new passivation film after 100 cycles

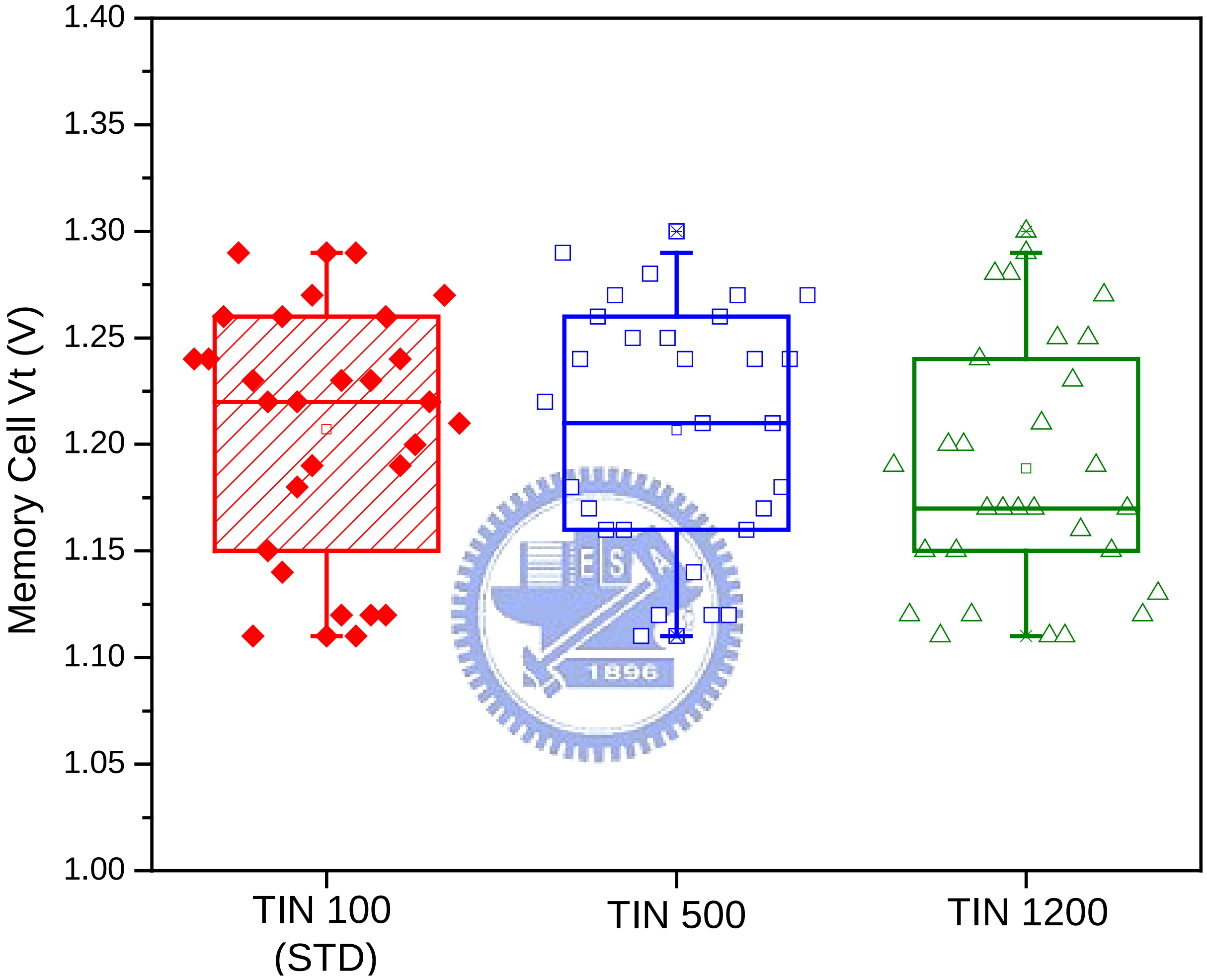


Figure 56 Vt compare of different TiN thickness experiment with old passivation film in WAT test key

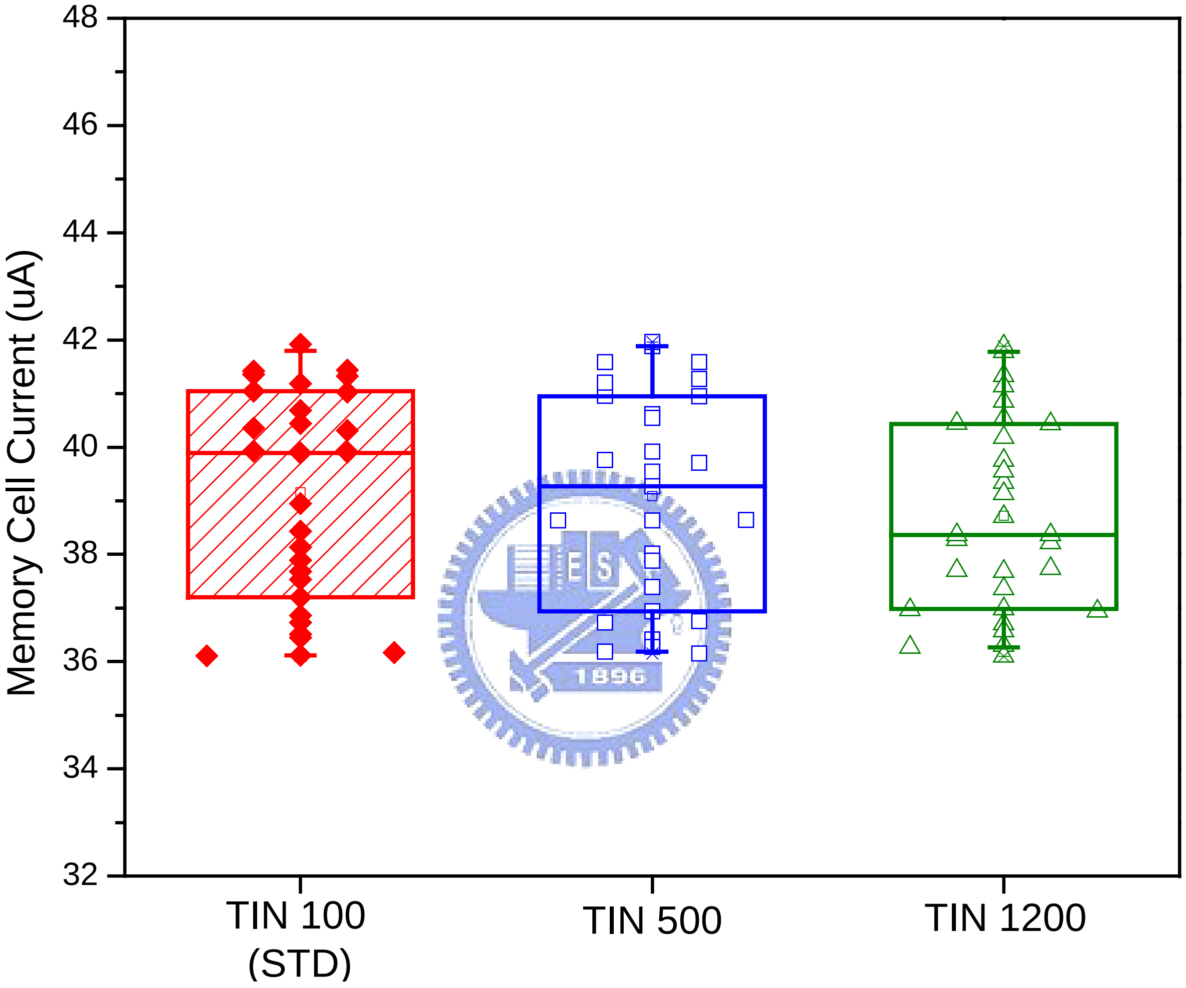


Figure 57 Cell current compare of different TiN thickness experiment with old passivation film in WAT test key

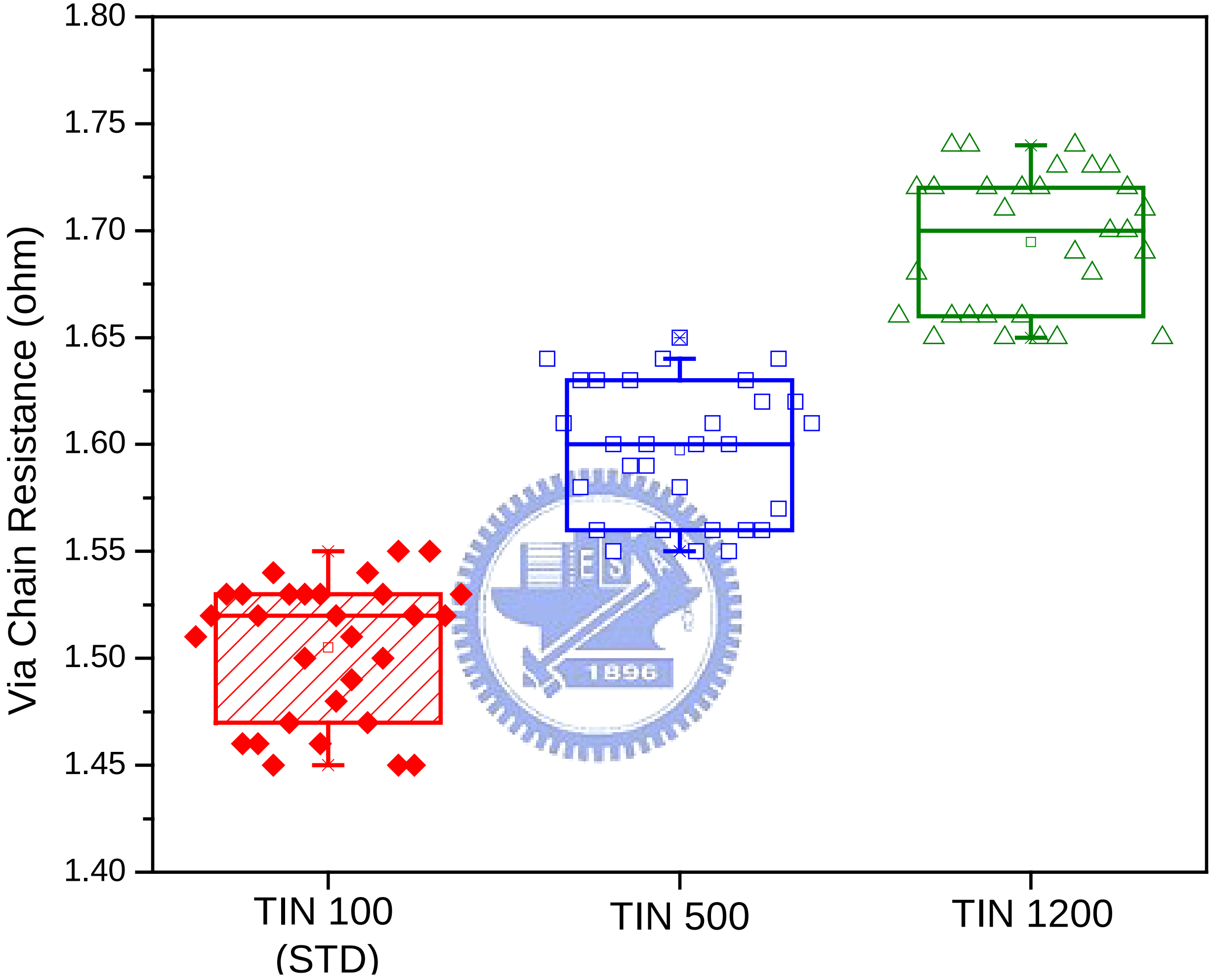


Figure 58 Via chain resistance compare of different TiN thickness experiment with old passivation film in WAT test key

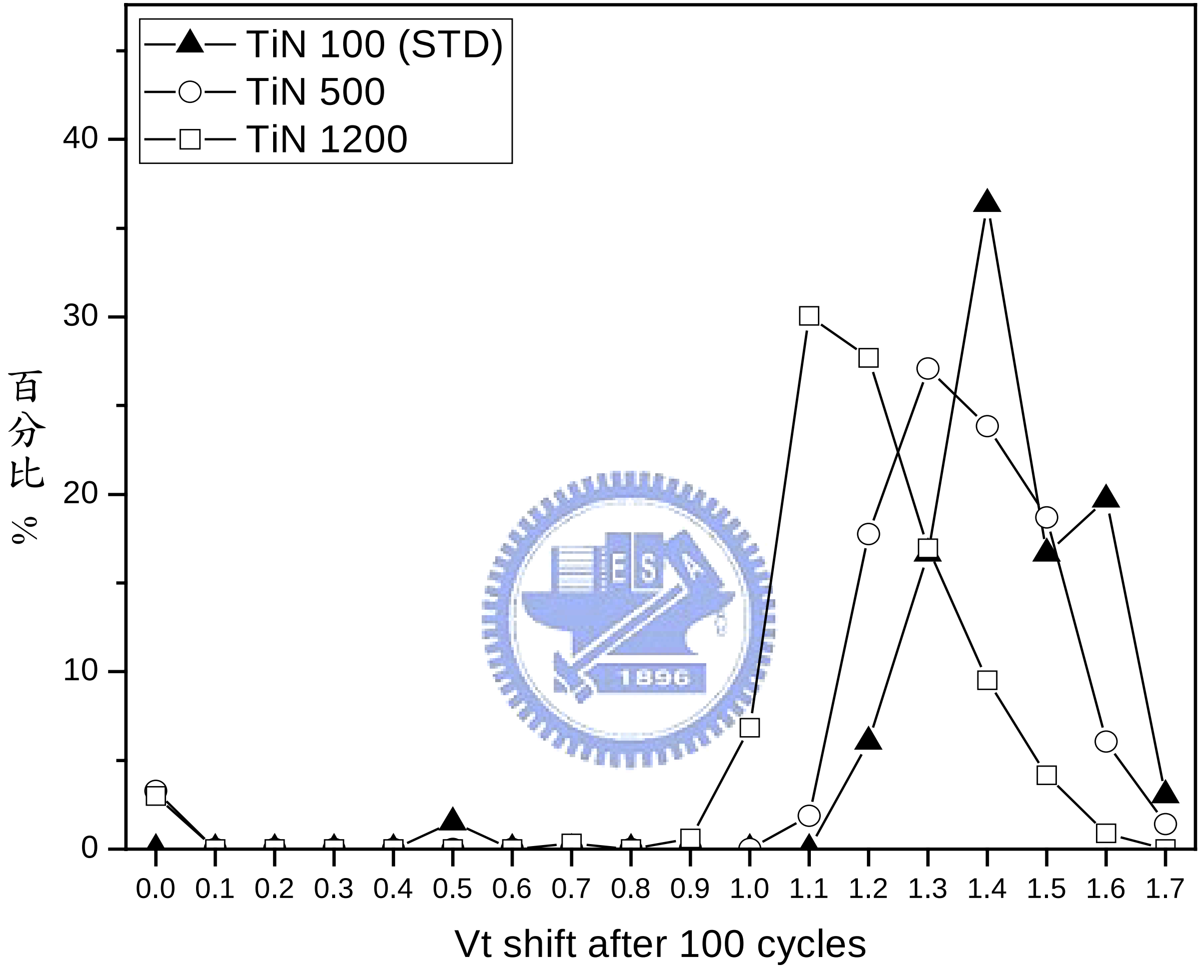


Figure 59 Vt shift distribution of different TiN thickness experiment with old passivation film after 100 cycles

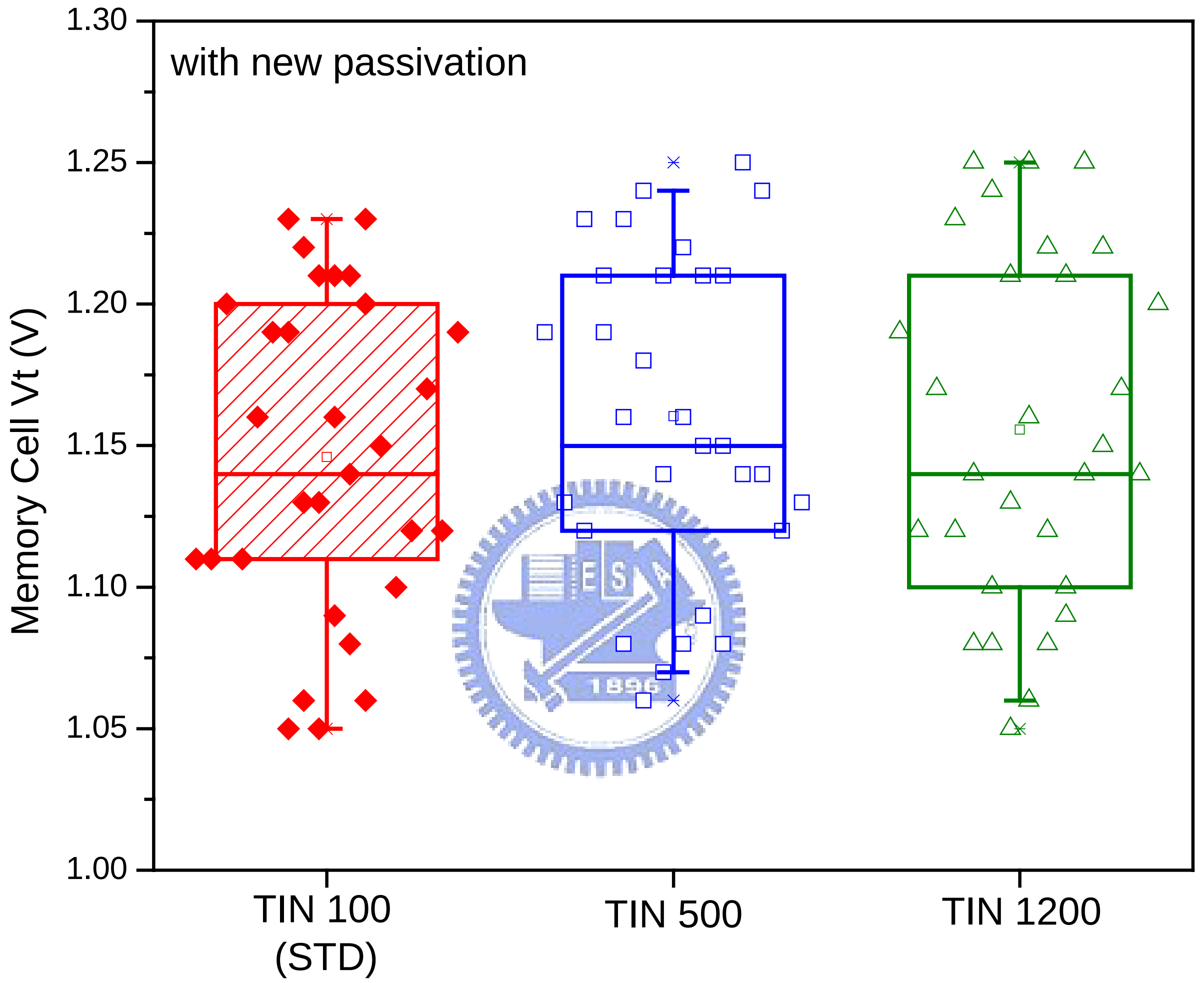


Figure 60 Vt compare of different TiN thickness experiment with new passivation film in WAT test key

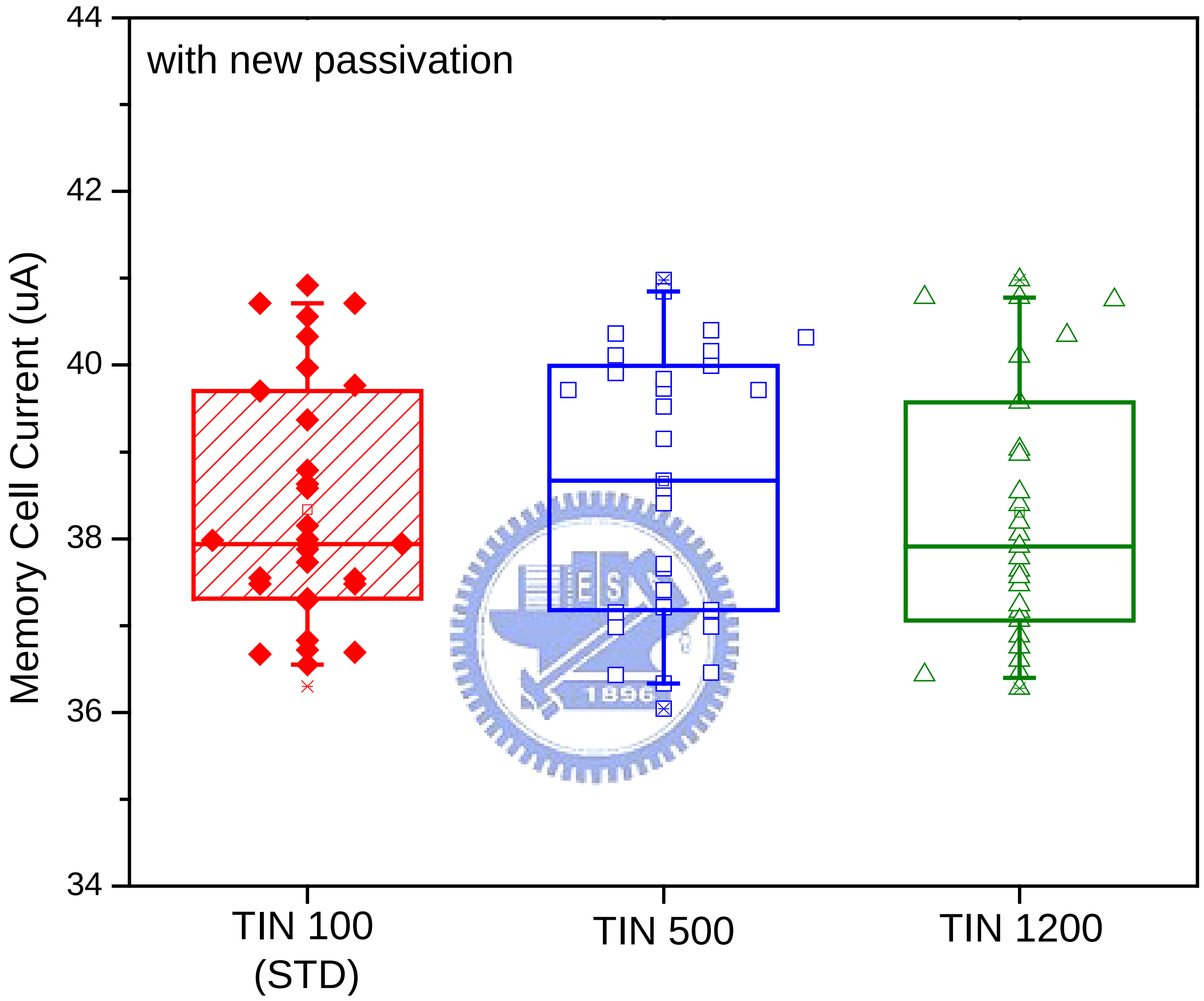


Figure 61 Cell current compare of different TiN thickness experiment with new passivation film in WAT test key

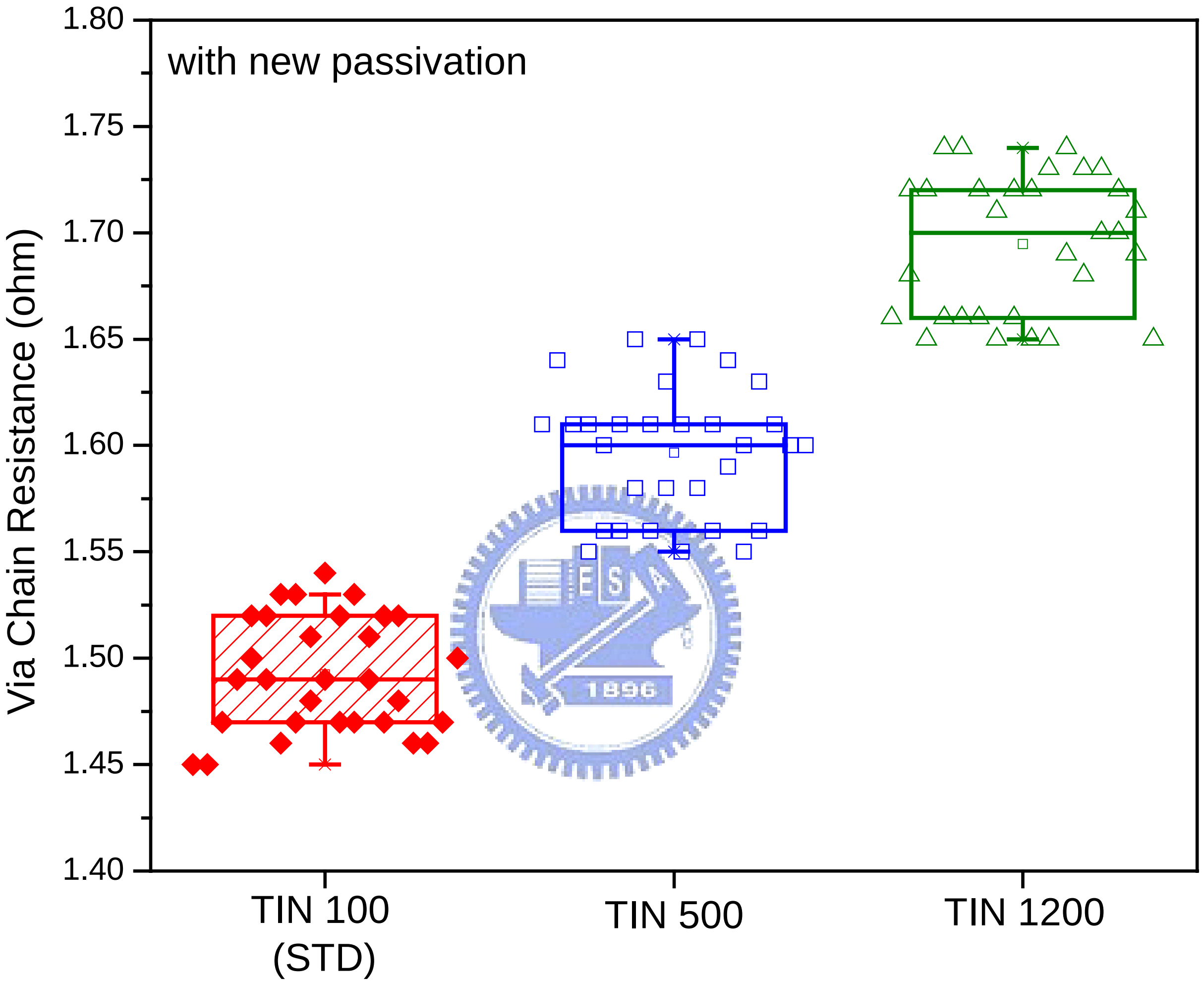


Figure 62 Via chain resistance compare of different TiN thickness experiment with new passivation film in WAT test key

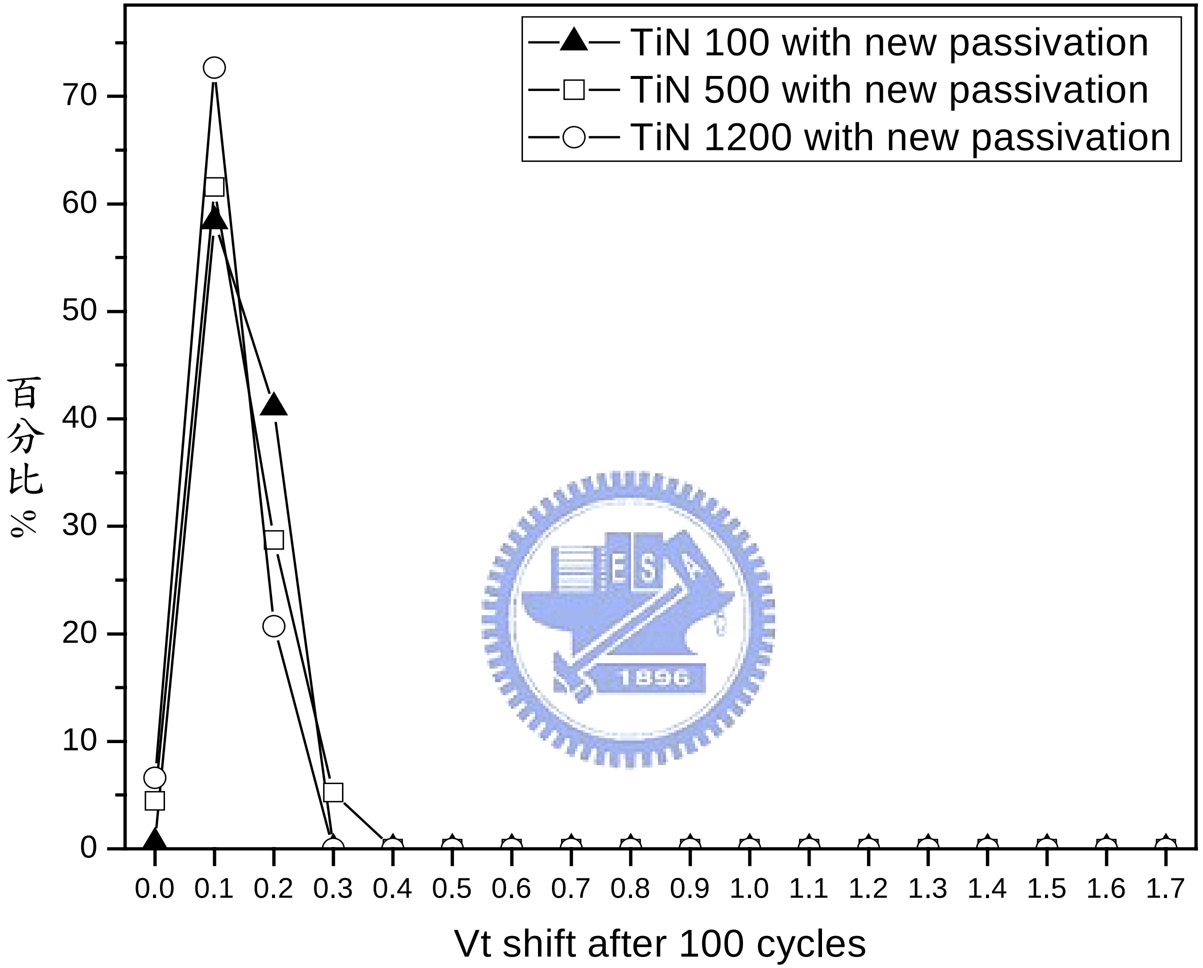


Figure 63 Vt shift distribution of different TiN thickness experiment with new passivation film after 100 cycles

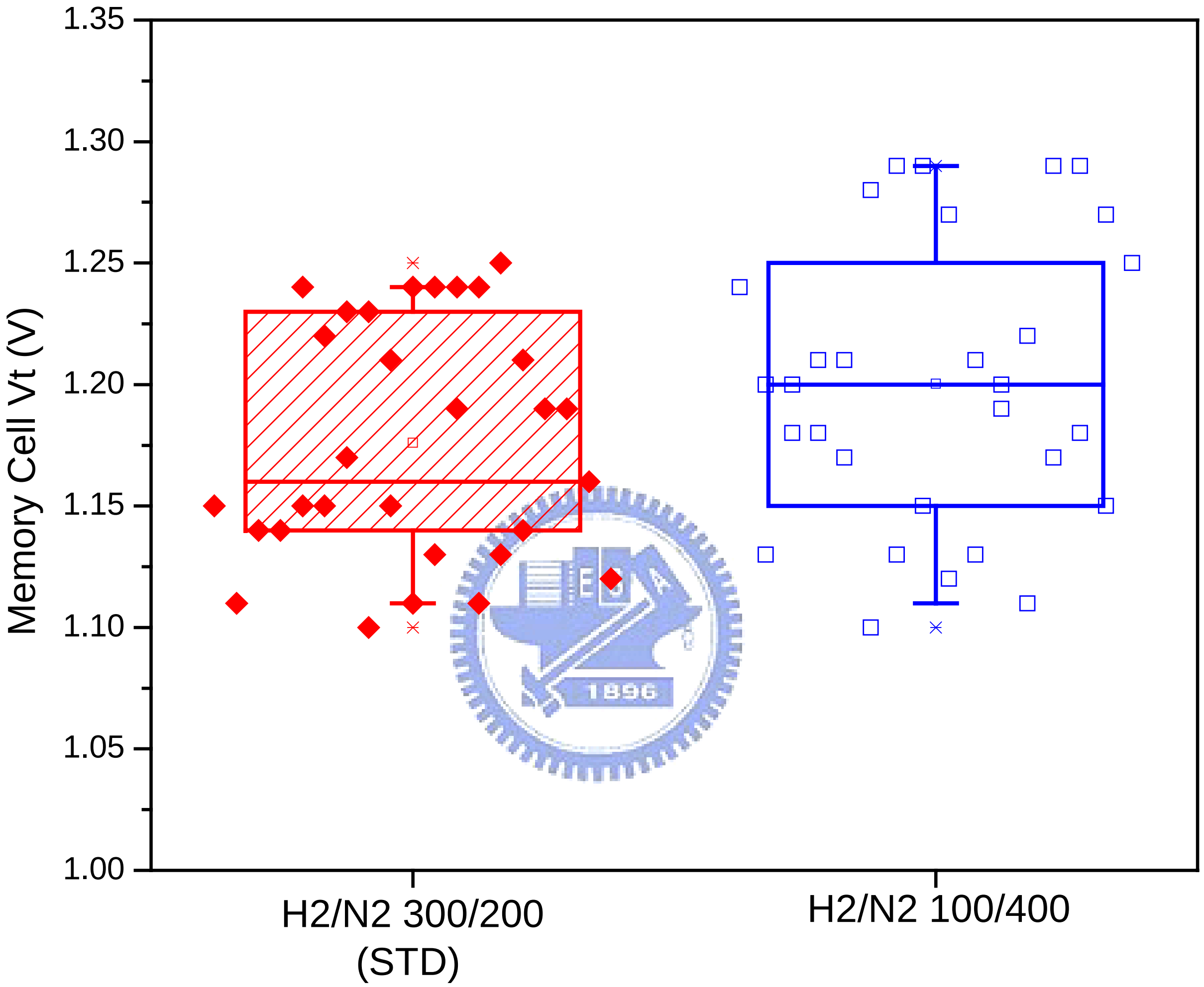


Figure 64 Vt compare of plasma treatment gas partial pressure experiment with old passivation film in WAT test key

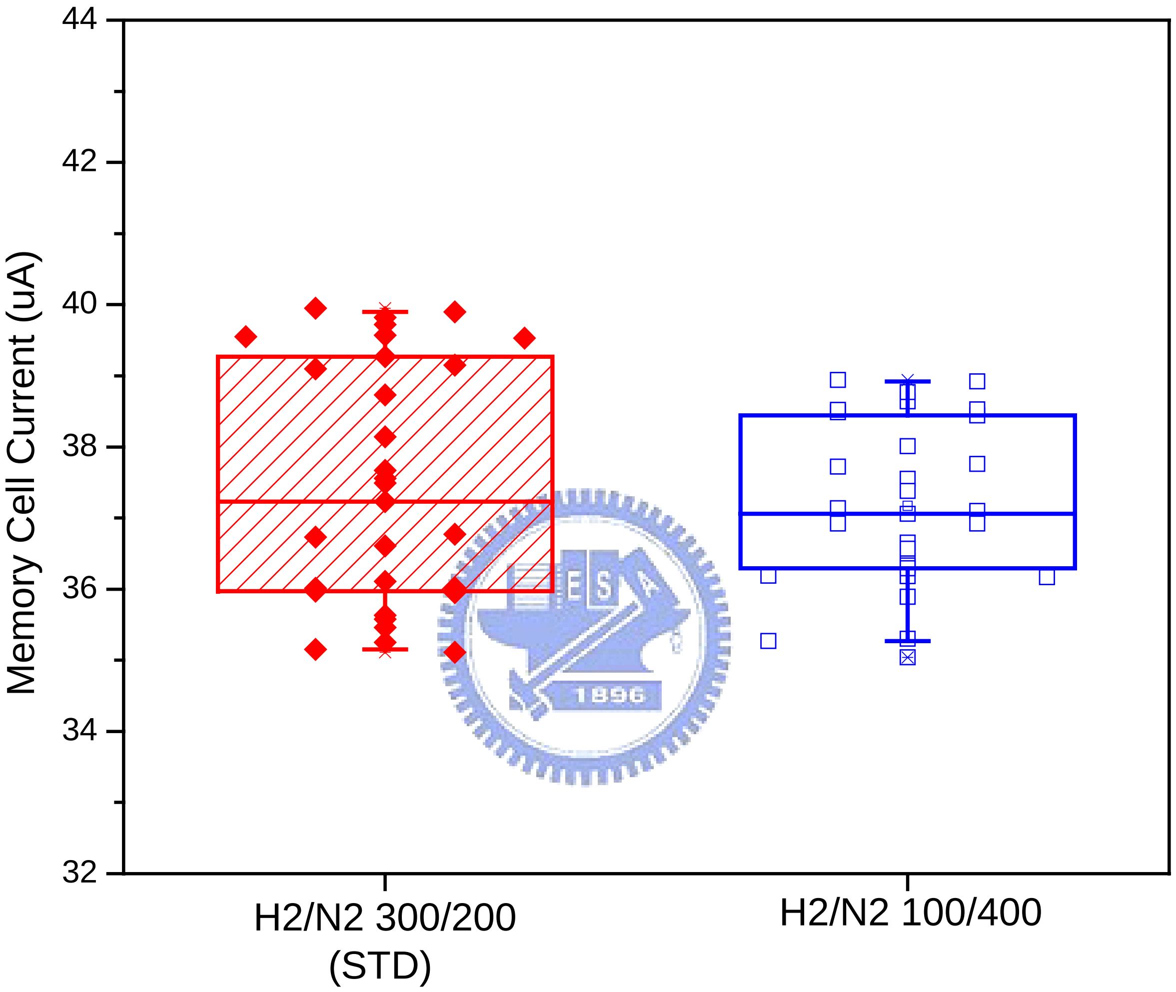


Figure 65 Cell current compare of plasma treatment gas partial pressure experiment with old passivation film in WAT test key

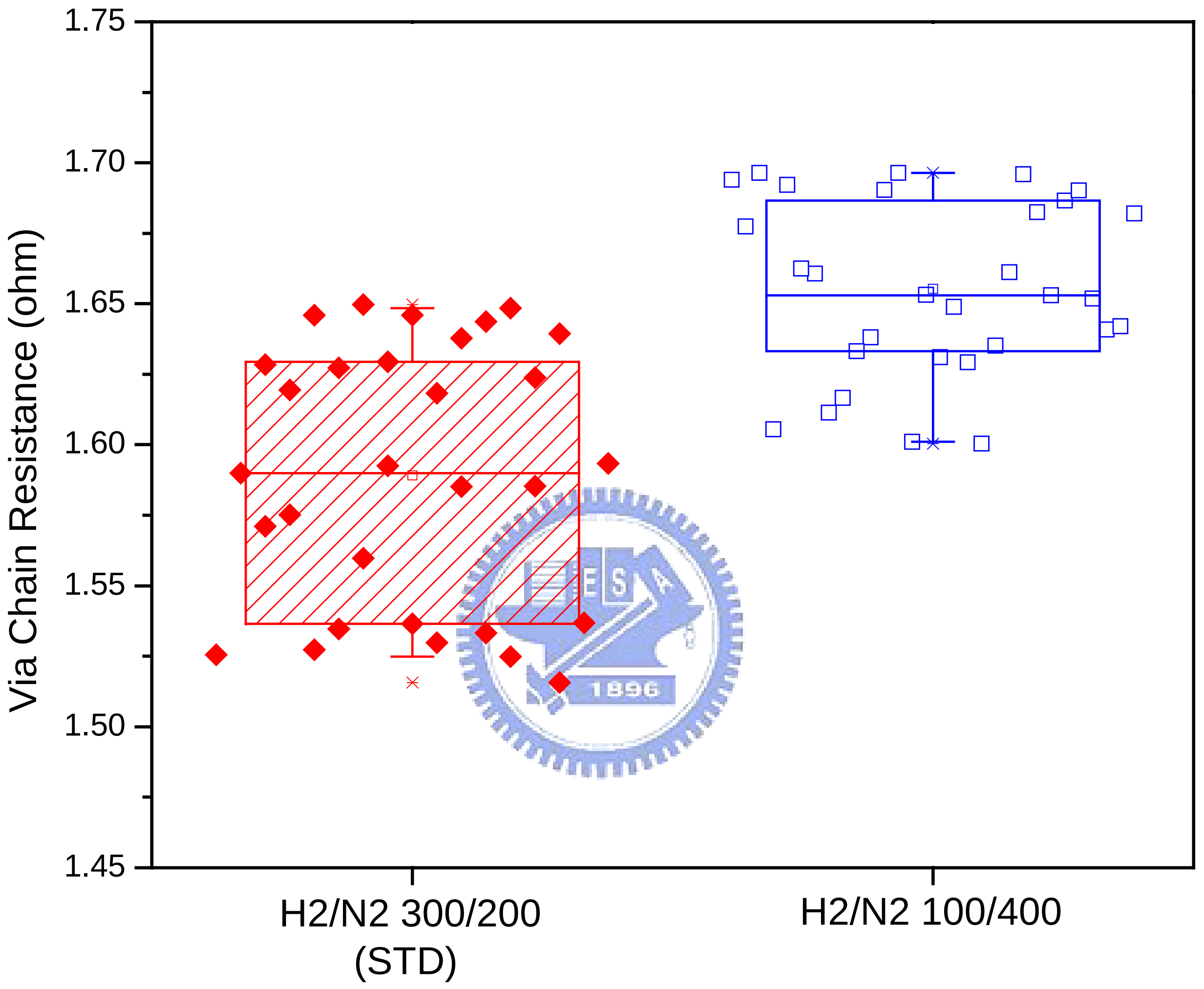


Figure 66 Via chain resistance compare of plasma treatment gas partial pressure experiment with old passivation film in WAT test key

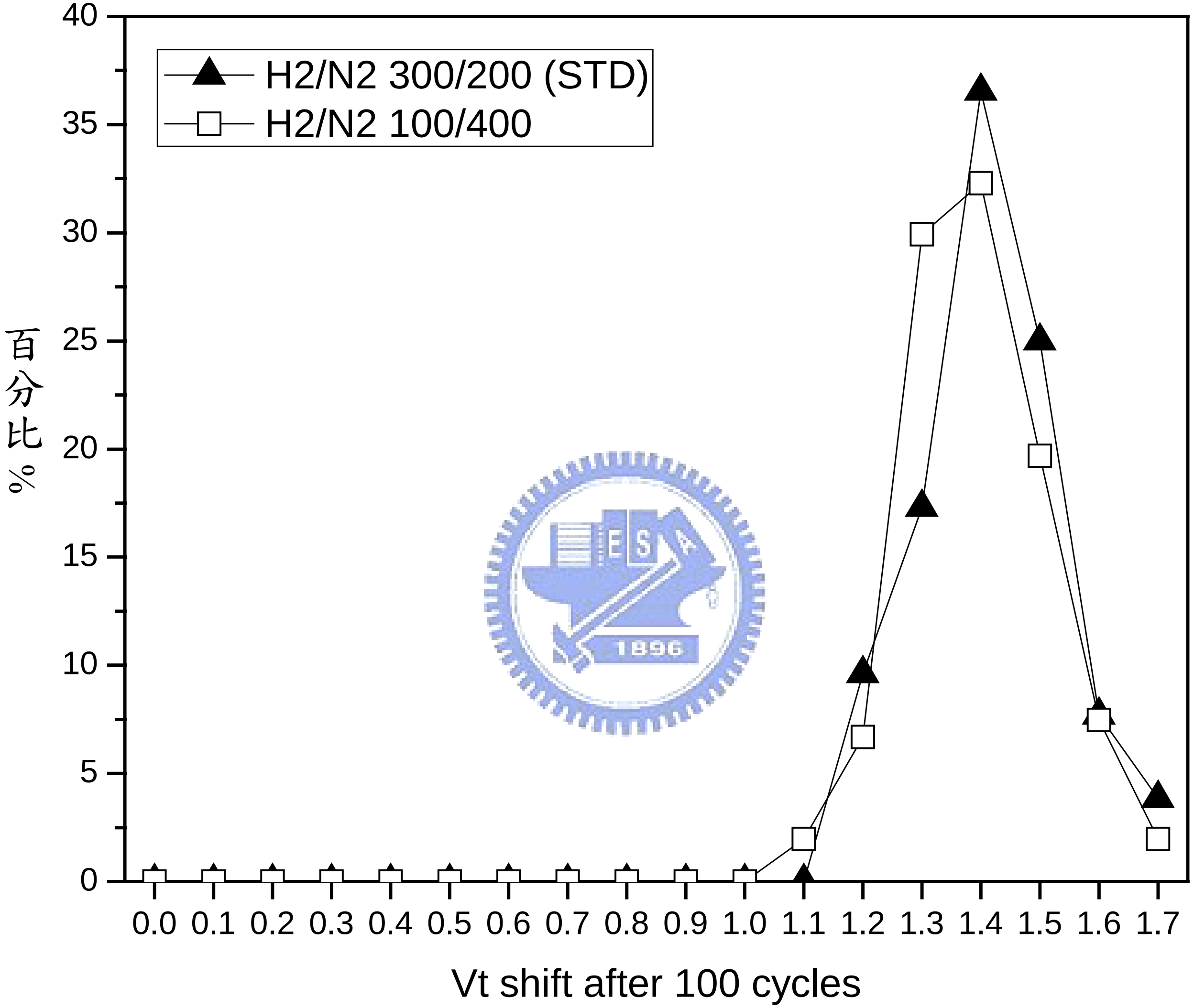


Figure 67 Vt shift distribution of plasma treatment gas partial pressure experiment after 100 cycles