

References

- [1] D. Kahng and S.M. Sze, "A Floating Gate and its Application to Memory Devices," *Bell Syst. Tech. J.*, vol. 46, p. 1288, 1967.
- [2] S. Aritome, "Advanced Flash Memory Technology and Trend for File Storage Application," *Electron Devices Meeting, 2000. IEDM Technical Digest. International 10-13 Dec. 2000*, pp. 763-766
- [3] B. Eitan et al., "Multilevel Flash cells and their Trade-offs," in *IEDMTech. Dig.*, 1996, pp. 169–172.
- [4] M. Bauer, R. Alexis, G. Atwood, B. Baltar, A. Fazio, K. Frary, M. Hensel, M. Ishac, J. Javanifard, M. Landgraf, D. Leak, K. Loe, D. Mills, P. Ruby, R. Rozman, S. Sweha, S. Talreja and K. Wojciechowski, "A Multilevel-Cell 32Mb Flash Memory," *Multiple-Valued Logic, 2000. (ISMVL 2000) Proceedings. 30th IEEE International Symposium on 23-25 May 2000*, pp. 367-368
- [5] B. Eitan, P. Pavan, I. Bloom, E. Aloni, A. Frommer, and D. Finzi, "NROM: A Novel Localized Trapping, 2-Bit Nonvolatile Memory Cell," *IEEE Electron Device Lett.*, no. 6, pp. 543–545, Jun. 2000.
- [6] B. Eitan, P. Pavan, I. Bloom, E. Aloni, A. Frommer, D. Finzi, "Can NROM, a 2 Bit, Trapping Storage NVM cell, Give a Real Challenge to Floating Gate Cells?" *Ext. Abst. 1999 Conf. Solid State Devices and Materials*, p.522, 1999.
- [7] C.C. Yeh, W.J. Tsai, T.C. Lu, Y.Y. Liao, N.K. Zous, H.Y. Chen, T. Wang, W. Ting, J. Ku and C.Y. Lu, "RELIABILITY AND DEVICE SCALING CHALLENGES OF TRAPPING CHARGE FLASH MEMORIES," *Physical and Failure Analysis of Integrated Circuits, 2004. IPFA 2004. Proceedings of the 11th International Symposium on the 5-8 July 2004*, pp. 247-250

- [8] W. J. Tsai, C. C. Yeh, N. K. Zous, C. C. Lin, S. K. Cho, T. Wang, S. C. Pan, and C. Y. Lu, "Positive Oxide Charge-Enhanced Read Disturb in a Localized Trapping Storage Flash Memory Cell," *IEEE Trans. Electron Devices*, no. 4, pp. 434–439, Apr. 2004.
- [9] C. C. Yeh, W. J. Tsai, T. C. Lu, H. Y. Chen, H. C. Lai, N. K. Zous, G. D. You, S. K. Cho, C. C. Liu, F. S. Hsu, L. T. Huang, W. S. Chiang, C. J. Liu, C. F. Cheng, M. H. Chou, C. H. Chen, T. Wang, W. Ting, S. Pan, and C. Y. Lu, "Novel Operation Schemes to Improve Device Reliability in a Localized Trapping Storage SONOS-type Flash Memory," in *IEDM Tech. Dig.*, 2003, pp. 7.5.1–7.5.4.
- [10] W. J. Tsai, N. K. Zous, C. J. Liu, C. C. Liu, C. H. Chen, T. H. Wang, S. Pan, C. Y. Lu, and S. H. Gu, "Data Retention Behavior of a SONOS Type Two-Bit Storage Flash Memory Cell," in *IEDM Tech. Dig.*, 2001, pp. 32.6.1–32.6.4.
- [11] W. J. Tsai, S. H. Gu, N. K. Zous, C. C. Yeh, C. C. Liu, C. H. Chen, T. Wang, S. Pan, and C. Y. Lu, "Cause of Data Retention Loss in a Nitride Based Localized Trapping Storage Flash Memory Cell," in *Proc. IRPS*, 2001, pp. 34–38.
- [12] E. Lusky, Y. Shacham-Diamand, A. Shappir, I. Bloom, G. Cohen, and B. Eitan, "Retention Loss Characteristics of Localized charge trapping devices," in *Proc. IEEE Int. Reliability Physics Symp.*, vol. 42, Apr. 2004.
- [13] E. Lusky, Y. S. Diamand, I. Bloom and B. Eitan, "Electrons Retention Model for Localized Charge in Oxide-Nitride-Oxide (ONO) Dielectric," *Electron Device Letters, IEEE Volume 23, Issue 9, Sept. 2002*, pp. 556-558
- [14] L. Larcher, P. Pavan and B. Eitan, "On the Physical Mechanism of the NROM Memory Erase," *Electron Devices, IEEE Transactions on Volume 51, Issue 10, Oct. 2004*, pp. 1593-1599
- [15] M. Jannai, "DATA RETENTION, ENDURANCE AND ACCELERATION

- FACTORS OF NROM DEVICES,” in *Proc. Int. Reliabil. Phys. Symp.*, 2003, pp. 502–505.
- [16] A. Brand, K. Wu, S. Pan and D. Chin, “Novel Read Disturb Failure Mechanism Induced By FLASH Cycling,” *Reliability Physics Symposium, 1993. 31st Annual Proceedings. ,International 23-25 March 1993*, pp. 127-132
- [17] M. Janai, B. Eitan, A. Shappir, E. Lusky, I. Bloom and G. Cohen, “Data Retention Reliability Model of NROM Nonvolatile Memory Products”, in *IEEE Transactions on Device and Materials Reliability*, 2004, pp. 404-415
- [18] S. S. Chung, C. M. Yih, S. M. Cheng, and M. S. Liang, “A New Technique for Hot Carrier Reliability Evaluations of Flash Memory Cell After Long-Term Program/Erase Cycles,” *Electron Devices, IEEE Transactions on Volume 46, Issue 9, Sept. 1999*, pp. 1883-1889
- [19] Reply by B. S. Doyle, K. R. Mistry, M. Bourcerie, C. Bergonzoni, R. Benecchi, A. Bravis and A. Boudou, “Comments on ‘The generation and characterization of electron and hole traps created by hole injection during low gate voltage hot-carrier stressing of n-MOS transistors’ [with reply],” *Electron Devices, IEEE Transactions on Volume 39, Issue 2, Feb. 1992*, pp. 458-464
- [20] S. Shuto, M. Tanaka, M. Sonoda, K. Sasaki, and S. Mori, “Impact of passivation film deposition and post-annealing on the reliability of flash memories,” *Reliability Physics Symposium, 1997. 35th Annual Proceedings., IEEE International 8-10 April 1997*, pp. 17-24
- [21] M. Shimaya, “Water Diffusion Model for the Enhancement of Hot Carrier Induced Degradation Due to Silicon Nitride Passivation in Submicron MOSFET’s,” *IEEE Proc. of IRPS, 1995*, pp. 292-296
- [22] S. Tokitoh, H. Uchida, K. Shibusawa, N. Murakami, T. Nakamura, H. Aoki, S. Yamamoto and N. Hirashita,” Enhancement of Hot-Carrier Induced

- Degradation under Low Gate Voltage Stress due to Hydrogen for NMOSFETs with SiN Films,” *Reliability Physics Symposium, 1997. 35th Annual Proceedings., IEEE International 8-10 April 1997*, pp. 307-311
- [23] S. Ito, K. Noguchi, T. Horiuchi and J. Clemens, “Limitation of Post-Metallization Annealing Due to Hydrogen Blocking Effect of Multilevel Interconnect,” *VLSI Technology, 1998. Digest of Technical Papers. 1998 Symposium on 9-11 June 1998*, pp. 182-183
- [24] S. Yoshida, K. Okuyama, F. Kanai, Y. Kawate, M. Motoyoshi and H. Katto, “IMPROVEMENT OF ENDURANCE TO HOT CARRIER DEGRADATION BY HYDROGEN BLOCKING P-SiO₂,” *IEEE IEDM Tech. Dig 1988*, pp. 22-25
- [25] M. T. Takagi, I. Yoshii and K. Hashimoto, ”Characterization of Hot Carrier Induced Degradation of MOSFET’s Enhanced by H₂O Diffusion for Multilevel Interconnection Processing,” *IEEE IEDM Tech. Dig. 1992*, pp. 703-706
- [26] E. Sakagami, N. Arai, H. Tsunoda, H. Egawa, Y. Yamaguchi, E. Kamiya, M. Takebuchi, K. Yamada, K. Yoshikawa and S. Mori, “The impact of intermetal dielectric layer and high temperature bake test on the reliability of nonvolatile memory device,” *IEEE Proc. of IRPS 1994*, pp. 359-367
- [27] S. Wolf, *Silicon Processing for the VLSI Era*. Sunset Beach, CA: Lattice, vol.2, ch. 11, pp. 333-333
- [28] M. Yoshimaru, T. Yoshie, M. Kageyama, K. Shimokawa, Y. Fukuda, H. Onoda and M. Ino, “Deoxidization of Wafer Desorbed from APCVD TEOS-O₃ SiO₂ by Titanium Cap Layer,” *Reliability Physics Symposium, 1995. 33rd Annual Proceedings., IEEE International 4-6 April 1995*, pp. 359-364

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