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懸浮閘和 SONOS 非揮發性記憶體元件特性及可靠度分析之研究

Study of Characteristics and Reliability of Floating-gate and SONOS Nonvolatile Memory Devices

研 究 生：林欣逸

指導教授：林鴻志　博士

黃調元　博士

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研 究 生：林欣逸　　Student：Hsin-I Lin

指導教授：林鴻志　博士　　Advisors：Dr. Horng-Chih Lin

黃調元　博士　　Dr. Tiao-Yuan Huang

國 立 交 通 大 學

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摘要

在本研究中，我們製作和描述 n 型通道的懸浮閘與 SONOS 非揮發性快閃記憶體元件特性。這篇論文主要著重致力於懸浮閘和 SONOS 元件的操作特性分析，如寫入與抹除操作以及相關的可靠性之議題。

由於閘極到汲極之間的藕合效應問題，所以懸浮閘元件被觀察到有嚴重的短通道效應。所幸這是可以使用介於控制閘與元件通道之間薄的 ONO 層之 SONOS 元件結構來緩和這個現象。在本篇論文中，我們也探討在熱應力下資料保存的影響與相關儲存電荷流失的路徑。再者我們觀察到 SONOS 元件 ONO 層頂端較薄的矽氧化層所引發的可靠性議題，其中又以影響最顯著的直接穿隧電荷流失效應為最。在另外一方面，隨著寫入/抹除的次數增加，懸浮閘元件會產生重要的電子的捕捉現象而導致縮小臨界電壓的操作範圍。此外我們觀察到兩種記憶體元件寫入方法所引發的界面缺陷現象，尤其是 SONOS 元件。雖然 SONOS 元件的通道初始二次電子(CHISEL)寫入方式會大量地增加界面狀態密度和導致次臨界電壓擺幅與跨導的退化，然而我們從結果可以看出既使在多次重覆寫入/抹寫狀態後，一個可以接受的臨界電壓操作範圍是得以維持。

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Student：Hsin-I Lin　　Advisors：Dr. Horng-Chih Lin

Dr. Tiao-Yuan Huang

Degree Program of Electrical and Computer Engineering

National Chiao Tung University

ABSTRACT

In this work, we fabricated and characterized n-channel floating-gate (FG) and silicon-oxide-nitride-oxide-silicon (SONOS) flash non-volatile memory devices. Major focus is paid on operation characteristics like programming and erasing, as well as the associated reliability issue.

Worse short-channel effect (SCE) is observed for the FG devices, owing to gate-to-drain coupling issues. This phenomenon could be relaxed using the SONOS structure, thanks to the thin ONO layer between the control gate and the channel. We also investigated the impact of thermal stress on the data retention and the related charge loss paths. Furthermore, significant direct tunneling (DT) charge loss effect from the thinner top oxide of the ONO layer of the SONOS devices is observed. On the other hand, as P/E cycle number increases, significant electron trapping events occur in the FG devices, resulting in shrinkage of threshold voltage window. In addition, interface states generated during programming procedure are observed for the two types of devices, especially for the SONOS devices. Although channel initiated secondary electron (CHISEL) programming of the SONOS

devices would greatly increase interface state density, and result in subthreshold swing (SS) and transconductance (GM) degradation, our results indicate that an acceptable threshold voltage window retains even after a great number of P/E cycles.

誌謝

時間很快就過去了，轉眼間又要到畢業的日子，在研究所這幾年來學到許多正確學習觀念和課本學不到的一些元件物理概念與想法，而這些都要感謝指導教授黃調元博士和林鴻志博士細心和嚴格的教導，讓我在研究的過程更加嚴謹以致發掘更多想法與觀念，每次都能突破一些瓶頸與困難，使得論文更加完整。林博常說要有正確的觀念與想法才不會做許多白功，而因自己已在業界工作多年，蠻能體會這句話，因自己以前就因缺少正確的觀念而常常走錯很多冤枉路，浪費自己的時間和公司的成本，如今有兩位指導教授的指導與教誨能讓我順利完成學業，也讓我在這次的學習中獲益良多，相信這會讓我往後在業界的發展將會很有幫助。

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林 欣 逸

誌于風城交大 2007

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Chapter 1
Introduction

1-1 General Background and Motivation

1-1.1 Overview of Non-volatile Memory Development

Nonvolatile semiconductor memories (NVSMs) are widely used as an important component in a number of modern electronic systems, including personal computers, cellular phones, digital cameras, automotive system and so forth. After decades of development with device scaling, several technologies have been employed for product manufacturing, including earlier metal-nitride-oxide-semiconductor (MNOS), electrical programmable read-only-memory (EPROM), and more recently Flash [1, 2].

Because of mass data storage requirement in electronic products, Flash device has become the mainstream in non-volatile semiconductor memory products nowadays [3]. An indispensable trend for technology development is to shrink the channel length for a higher storage capacity. Moreover, lowering the voltage for writing/erasing operations is essential for lower power consumption, while high speed access is required to shorten mass data storage time. Of course there is no free lunch and a number of challenges is lying ahead hindering the development of device technology. In this thesis we will focus on issues of reliability and operation performance for two different flash memory devices.

1-1.2 Floating Gate and SONOS Memory Device physics

Figure 1.1 shows that it is necessary to extend the actual flash memory device technology lifetime as much as possible. Through decades of development, flash devices are categorized into two types of structures, namely, FG [4] and charge trapping structures, as illustrated in Figure1.2. For FG devices, owing to the high topography of the gate structure, the interference between neighboring cells by gate coupling becomes an almost unsolvable issue

beyond 45nm-node. As a consequence charge trapping flash memory devices such as SONOS is revisited as the succeeding technology to avert interference between neighboring cells

FG structure is composed of a POLY1 floating gate inserted between an underlying tunnel oxide and a stacked ONO (oxide-nitride-oxide) layer. The ONO is used to increase the gate coupling ratio and to reduce charge emission loss. A POLY2 layer is deposited on top of the ONO to serve as the control gate [5].

In SONOS structure, a carrier-trapping layer made up of nitride is inserted between two silicon oxide layers to prevent charge loss. Such flash cells resemble a standard MOS transistor except that the gate oxide is replaced by an oxide-nitride-oxide dielectric stack [6].

The storage material is typically a degenerately doped poly-Si for floating-gate devices and a nitride layer for SONOS devices. The mechanisms of charge storage are different between the two types of devices due to the different storage materials. Since the floating gate is made up of a conducting material, the stored electrons flow freely inside the floating gate. This raises a reliability issue in that if certain paths for stress induce leakage current (SILC) are created in the tunnel oxide during operation, the stored charges may easily find the path to leak out which in turn lead to poor retention and endurance characteristics. On the other hand, the nitride storage layer in SONOS device contains discrete traps serving as the charge storage sites. The injected electrons are trapped in deep level of the nitride layer and become immobile, so the aforementioned SILC issue can be avoided and better retention and endurance are expected [7].

Programming operation can be achieved by injecting charges into the storage layer, a nitride for the SONOS or a poly layer for the FG type. Channel or substrate hot carrier injections are usually employed for this purpose. On the other hand, erasing mechanism could be implemented via band-to-band hot holes injection from drain side. For efficiency, both programming and erasing operations need high biases on the gate and drain. The high electric field may provoke potential reliability concerns such as oxide breakdown and generation of

excessive SILC. Moreover, high power consumption while the devices are under programming and erasing operations is inevitable [8].

The difference between FG and SONOS-type devices lies in the method of charge storage, which is fundamental to issues such as scaling and radiation hardness. The concept of nonvolatile data storage based on a shift in the threshold voltage of the nonvolatile semiconductor memory (NVSM). The threshold voltage has the following expression [9]

$$V_{th} = \Phi_{GS} + 2\Phi_F - (Q_{SS} + Q_S)/C_I - Q_T/\varepsilon_I \tag{1-1}$$

where Qss is the fixed charge at Si-SiO_2 interface, Qs is the charge in silicon semiconductor, Q_T is the charge stored in the gate insulator, C_I and ε_I are the capacitance per unit area and dielectric constant of the gate insulator layer, respectively. Based on Eq.(1-1), threshold voltage increases when more electrons are trapped. On the contrary, threshold will be decreased, if Qs quantities are reduced. Therefore we can control Qs by means of varying the substrate doping concentration to adjust the threshold voltage of flash devices. The threshold voltage window (Write Vth – Erase Vth) should be maintained at least 1.5V to easily distinguish between “1” and “0” states by peripheral sense amplifier circuits [10].

The storage charges will gradually leak away as the storage time progresses because of the existence of different leakage mechanisms. The capability of preserving the charge storage is directly related to the data retention and device life time. Therefore the FG device has added ONO (oxide-nitride-oxide) layer above POLY1 to reduce charge loss through the top side while keeping the gate coupling ratio. On the other hand, SONOS must maintain a tunneling oxide thickness of around 2nm or above to prevent the excessive direct tunneling of charges from nitride layer to substrate. High temperature data retention analysis is usually performed to monitor the variation of programmed threshold voltage as a function of the elapsing time. The measurements are typically performed between 150 ^{o}C and 250 ^{o}C to ensure 10-year data retention time.

Both programmed and erased operations affect the endurance capability of flash devices. These procedures should thus be carefully designed and optimized to improve the endurance characteristics. Conventionally for floating-gate devices, channel hot electron injection (CHEI) and hot hole injection (HHI) mechanism are employed to program and erase the device, respectively. CHEI has better speed performance. Nevertheless, the hot electrons are injected into POLY1 layer from the channel region near the drain, and may cause defects like trapped charges in the oxide and interface states, so the threshold voltage window narrows with program/erase (P/E) cycles.

For SONOS devices, channel induced secondary electron injection (CHISEL) can be an alternative approach for programming, while HHI is used for erasing [11]. CHISEL programming method proceeds by negatively biasing the substrate. As a result, more hot electrons and secondary electrons are generated and the programming speed is effectively improved. CHISEL thus provides better programming efficiency than CHEI. However, CHISEL will also result in interface state damage, so that subthreshold swing (SS) and mobility (Gm) are degraded after P/E cycling.

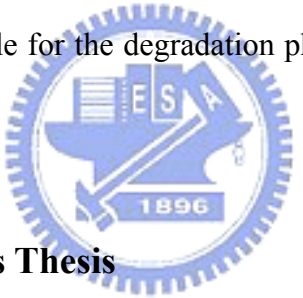
NVSMs are required to withstand up to 10K-100K program/erase cycles (endurance) with 10-year lifetime at temperatures as high as 125 ^{o}C. In practical applications radiation hardness is another issue. In certain applications, it may require radiation-hardened field oxide processes to reduce the build up of radiation induced parasitic leakage in advanced flash memory technology.

1-1.3 Motivation

The FG memory device has been implemented by the industry to preserve mass data for a long time. However, scaling of this technology is limited by the coupling issues which may result in the interference between neighboring cells in deep sub-micro NVMs and beyond. In this study we investigate and discuss the impact of new storage material (silicon nitride) and

the effectiveness of the associated SONOS structure on resolving this issue. The implementation of the SONOS devices in a chip is compatible with current manufacturing technology and thus represents a viable candidate for NVSMs scaling [12].

Data retention and endurance represent the most critical reliability concerns in NVSMs. The physical mechanisms and reliability characteristics have been extensively examined. The reliability parameters in terms of threshold voltage shift (△Vth), charge loss (△Q), and subthreshold swing degradation (△SS) after programming/erasing cycles, have been monitored and studied by using different stress test schemes. However, there seems few works devoting to identify and compare the difference in reliability performance between the FG and SONOS devices. This motivates us to carry out this study on understanding the impacts of the programming/ erasing methods on the reliability of the two types of memory devices. Mechanisms responsible for the degradation phenomena are also investigated in this work.



1-1.4 Organization of This Thesis

In addition to this chapter, this thesis is divided into the following three chapters.

In Chapter 2, we briefly describe the process flow, layouts, and structures for fabricating the test devices. We also present the characterization method, measurement setup, equipment, and conditions for P/E cycling stressing.

In Chapter 3, results regarding the impacts of programming and erasing schemes on the characteristics of FG and SONOS devices are presented. Moreover, the coupling issues of the FG structures and effectiveness of SONOS devices in addressing the issue are examined and discussed. Reliability performance of the devices is also discussed.

In the Chapter 4, important conclusions generated from this work are summarized.

Chapter 2
Device Fabrication and Measurement Setup

2-1 Device Fabrication

2-1.1 Fabrication of Non-Volatile Memory

In this study two types of devices, namely, conventional floating-gate (FG) flash and silicon-oxide-nitride-oxide-silicon (SONOS) flash, were fabricated and characterized [13]. The process flows are described in Fig. 2-1. Briefly, the fabrication began with 6-inch p-type (100) silicon wafers with resistivity of 8-25Ω-cm and thickness of around 655~695μm. The active area of the memory cell is defined by a p-type well implantation. Next, a standard field oxidation (FOX) or local oxidation of silicon (LOCOS) process with channel stop implant before drive-in was used for isolation between cell devices. Implantation to adjust the threshold voltage of memory cells (EPROM IMP) was done by implanting BF_2^+ at 55keV. A 15nm-thick tunneling oxide was grown by thermal oxidation, a 200nm undoped polycrystalline silicon layer (poly1) was deposited by low pressure chemical vapor (LPCVD), followed by implantation of phosphorous ions into the poly1 gate with a dosage of 5×10^{13} cm-^{2} at 30keV. An oxide-nitride-oxide (ONO) stack layer was then deposited on ploy1 by LPCVD. Thickness of the bottom oxide, nitride, and top oxide is 7nm, 12nm and 3nm, respectively. An undoped poly2 of 200nm was then deposited on ONO to serve as the control gate. Afterwards, doping of phosphorous (P^+) in poly2 was done with implant conditions identical to that for poly1, followed by cell gate etch process. The source/drain (S/D) extension regions were then formed by arsenic (As^+) implantation, and 200nm spacers were subsequently formed by atmospheric pressure chemical vapor deposition (APCVD). Inter layer dielectric (ILD) of

boron phosphorous silicon glass (BPSG) film was deposited. After contact hole etching, normal metallization scheme was carried out. Finally, 500nm passivation oxide and 700nm nitride were deposited by PECVD to prevent undesirable particles contamination.

The SONOS process flow was almost the same as that of FG flash, except the deposition of two layers, poly1 and subsequent 7nm-thick oxide, required in the floating gate process, was skipped. In addition, because UMC 6 inch Fab was harder to fine tune thinner FG gate oxide thickness recipes and parameters, 15nm-thick tunneling oxide of the SONOS device was unsage production in flash industry due to follow FG process.

2-1.2 Device layout and Structure

The structure and layout of devices are shown in Fig. 2.2. Two cells sharing a common source were shown. Note that polycide was stacked on poly2 gate in order to reduce the gate resistance. The length and width (L/W) of a single cell are 0.65um and 0.5um, respectively. Cross-section views of the fabricated FG and SONOS memory devices are shown in Fig. 2.3.

2-2 Measurement Setup

2-2.1 Electrical Measurement Setup

Electrical characteristics of the fabricated flash memory device were measured by an HP 4156A-Precision Semiconductor Parameter Analyzer. Methods of parameter extraction used in this study are described in this section. Temperature-regulated hot chuck was used to keep the device under test at a fixed temperature of 25^{o} C.

Charge pumping measurements are popular and widely used to characterize density

of interface states and endurance analysis in flash memory devices. Figure 2.4 shows the characterization equipment, including semiconductor parameter analyzer (HP4156A), dual channel pulse generator (HP8110A), low leakage switch mainframe (HP E5250A), cascade guarded thermal probe station and thermal controller, providing an adequate capability for measuring the device I-V characteristics. In addition, the PC programs (VEE software) were used to control the measurement procedure. This provides a very effective way to extract the interface state densities after programming/erasing (P/E) cycling of flash memory stress. To accurately analyze interface state densities in the oxide dielectric from charge pumping measurement results, it is necessary to pay attention to the leakage current phenomenon. Moreover, it excludes the contribution of gate leakage to the calculation of interface state densities presented in gate oxides at lower frequencies. The basic charge pumping measurement technology includes the measurement of the substrate current when a series of voltage pulses with fixed amplitude voltage, rise time, fall time, and duty cycle is being applied to the gate of the flash memory device as Figure 2.5. The source and drain are connected to a small reverse bias around 50mV and the substrate connected to ground and the HP81110A pulse generator is connected to the gate through the switch equipment. After the P/E cycling of interface state density extraction, we use “fixed amplitude sweep method” to calculate interface state density. Square-wave waveforms are applied to the gate with a frequency of 1MHz, and the base voltage is varied to change the surface condition from inversion to accumulation, Figure 2.6 shows the operation principles of the measurements. In this scheme, an HP4156A measures source and drain current (I1, I2) and substrate current (I3, I4) while keeping the pulse amplitude at a fixed voltage (e.g., 1.5V). The charge pumping current is obtained with the

relation $I_{CP} = I_1 - I_2 = I_3 - I_4$. It can also be expressed using the following equation:

$$I_{CP} = qfA_G \int_{E_{em,h}}^{E_{em,e}} D_{it}(E)dE \approx qfA_G \overline{D_{it}}\left(E_{em,e} - E_{em,h}\right) \approx qfA_G \overline{D_{it}} \Delta\psi_s \quad (2\text{-}1)$$

where A_G is the gate area and f is pulse frequency. The interface trap density Dit (Nit) could be extracted based on this formula.

2-2.2 Setup for Data Retention Measurements

We used temperature-regulated hot chuck with temperature ranging from 25°C to 125°C for data retention and device life time analysis. The measurement was performed after data was written into the cell. Characteristics of charge loss [14] were explored by probing the shift in threshold voltage of the flash device at 25°C, 85°C or 125°C. Based on the measured data and time, charge loss was calculated using the following equation:

$$\Delta V_t = \frac{t_{control}}{\varepsilon_{ox}} \cdot Q_t \quad (2\text{-}2)$$

where $t_{control}$ is tunneling oxide thickness and ε_{ox} is oxide dielectric constant

2-2.3 Procedure for Nit Extraction

The programming and erasing time are around 0.001 and 0.1 seconds for FG devices, and 0.4 and 0.1 seconds for SONOS devices. The method to extract interface state density (Icp maximum) after P/E cycling stress and the measurement setup are shown in Figure 2.7. Procedures of the measurements with fixed amplitude are described as below

1. During the Icp measurement, the gate was applied with a bias having a fixed amplitude magnitude ($\triangle V_A$) of 1.5V with V_{base} increasing from -1V to 1V by step 0.1V. Rise and fall times of the pulse are both 80 nano-second.
2. Maximum Icp value was recorded before and after programming and erasing cycling.
3. Interface state densities (Nit) were extracted from the Icp data. Endurance of the flash devices was analyzed based on the extracted Nit.

Chapter 3
Results and Discussion

3-1 Electrical Characteristics of Floating-Gate and SONOS Flash Devices

Figure 3.1 shows subthreshold characteristics of the floating-gate (FG) and SONOS devices with channel length/width = 0.65μm/0.5μm, measured at drain voltage of 0.1V and 2.0V. The coupling issue associated with the FG device is clearly observed in the figure. Such effect is apparent from the shift of the threshold voltage with increasing drain voltage in the FG device [15]. As a comparison, it is noted that the SONOS device does not exhibit this phenomenon. The same effects can also be observed in I_D saturation regime. Figure 3.2 shows I_D-V_D characteristics of both flash memory devices. From the figure, the FG device obviously shows more pronounced short-channel effect. In the saturation region (V_{DS}>V_{GS}-V_{TH}), the drain current can be expressed as follows [16].

$$I_{DS} = \frac{1}{2}\mu_{FE} C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2 \qquad 3\text{-}1$$

The higher shift in threshold voltage with increasing drain voltage for FG device is attributed to the worse charge-sharing effects of the depletion region, owing to the FG structure. As the gate and drain voltage are raised, a fraction of voltage drop develops across the floating gate (Poly 1), resulting in a reduction in gate controllability as well as the punchthrough voltage of the device [17]. Therefore, we found a larger saturation current and slope in FG device shown in Fig. 3.2. In contrast, SONOS device with charge storage in discrete traps is less susceptible to this issue owing to the low gate structure [18].

3-2 Program and Erase Characteristics

3-2.1 Program and Erase Schemes

To promote the injection efficiency of electrons, the feasibility of using channel-initiated secondary electron (CHISEL) programming has been demonstrated in the SONOS devices [19]. CHISEL programming conditions and mechanisms are shown in Figure 3.3(a). The hot holes generated near the drain mainly drift toward the substrate and contribute to the substrate current (I_B). Some of these hot holes create electron-hole pairs by secondary impact ionization, which are greatly enhanced under a high electric field by the applying of a reverse substrate bias (V_B <0). As a result, the hot electrons caused by the secondary impact ionization tend to be injected into the SONOS structure and result in a wide distribution of trapped electrons, compared with the case of channel hot electron injection (CHEI) [20]. Figure 3.3(b) illustrates the energy band diagram for CHISEL programming operation. Owing to the reverse substrate bias, the conduction band (E_C) of the substrate is raised, and the substrate hot electrons can more easily tunnel through the oxide energy barrier (i.e., 3.1eV).

Discrete charge storage memories (e.g., SONOS and nanocrystal) are typically erased using hot holes injection (HHI) [21], generated by band-to-band tunneling (BBT) in the channel and drain side overlap region. The HHI erasing conditions and mechanisms are shown in Figure 3.4(a). During the HHI erasing operation, the n-type SONOS device is turned off while maintaining a negative gate bias with positive drain and substrate biases. The energy band diagram [22] during the HHI erasing operation is shown in Figure 3.4(b). The increased positive bias in substrate causes a downward shift of valance band of the substrate and also helps promote charge trapping efficiency of the nitride layer [23].

As a result, electron-hole pairs created from BBT tunneling in the channel/drain

overlap region are accelerated by the drain lateral electric field and are injected into the nitride layer assisted by the substrate vertical electric field to complete the HHI erasing operation [24].

3-2.2 Program and Erase efficiency

Figure 3.5(a) shows the I_D-V_D characteristics of a SONOS device under CHISEL programming mode. For comparison, the characteristics of a FG device under CHEI programming mode are shown in Figure 3.5(b). It indicates that the V_D range is between 4V and 6V in CHISEL programming, while it is between 3V and 6V in CHEI programming. Therefore, 5V drain voltage is selected in this work to measure and compare CHISEL and CHEI programming characteristics of the two types of memory devices. It was observed that the programming efficiency of the FG device is better than that of the SONOS device. This is mainly ascribed to the use of a thicker tunneling oxide in the SONOS device, resulting in a greatly reduced programming current [25].

The efficiency of electron injection into the tunnel oxide can be estimated by I_G/ I_D, the ratio between electron injection current and the total channel current [26]. The electron injection efficiency characteristics with 5V drain voltage for the SONOS device are shown in Figure 3.6. Hot carrier generation and injection at V_B=0V and V_B<0V are generally referred to as CHEI and CHISEL programming operation, respectively. It can be seen that the programming efficiency of CHISEL (V_B<0V) is higher than that of CHEI (V_B=0V) in the SONOS memory devices. The reason is that CHISEL programming generates and injects more secondary electrons into the nitride layer. The high I_G/ I_D ratio implies higher injection efficiency in terms of faster programming speed, as shown in Figure 3.7(a). It is also clearly seen that the largest threshold voltage shift ($\triangle V_{th}$ =3.5V) is obtained after 10ms programming time.

Figure 3.7(b) shows I_D-V_G characteristics of CHISEL programming with V_B=-4V at various programming times for the SONOS device. It appears that excellent subthreshold characteristics are retained after programming with a 3.5V threshold voltage window.

HHI erasing characteristics of the SONOS device are shown in Figure 3.8(a). It is seen that the erasing speed is improved when a higher drain voltage is applied. Note that no over-erase symptoms during a long erasing duration (10sec) are observed in the SONOS device [27]. This could be explained by the fact that discrete traps in deep level bandgap memories are harder to be detrapped in the erasing operation. The characteristics of I-V curves after the HHI erasing are shown in Figure 3.8(b). Compared with CHISEL programming characteristics shown in Fig. 3.7(b), the range of threshold voltage shift is still narrower for the best HHI erasing condition (V_D=8V, V_G=-15V and V_B=5V) [28].

Furthermore, we summarize the program/erase (P/E) operation speed and V_{th} window characteristics for the SONOS device in Figs. 3.9 and 3.10. It can be seen that a 1.86V V_{th} window is achieved with 100ms P/E duration. Figure 3.10 shows the subthreshold characteristics of the two types of devices at different stage of operations. It is seen that good subthreshold slope is retained for these devices after operations.

3-2.3 Forward Read Performance after Programming and Erasing

For read operation in general, a voltage larger than 1.5V is applied to V_D. Hence, we measured the I-V curves biased at V_D= 1.5V for both memory devices in erased and programmed states. Typical results are shown in Fig. 3.11. In the figure, the threshold voltage difference is slightly larger for the FG device. The erased state and programmed states have a low reading current (ON-STATE current<8uA and OFF-STATE current <1pA) and 164 mV/decade of the subthreshold swing (SS) at

V_G=3V for both memory devices. During the data read-out operation, such low reading currents are helpful for reducing the power consumption.

Figure 3.12 shows the threshold voltage of programmed and erased states as a function of V_D for the two types of devices [29]. It is clearly seen that the threshold voltage decreases with increasing V_D for the FG device, although the difference between the two states remains roughly a constant. Such phenomenon, dubbed the drain turn-on effect, appears frequently in conventional FG devices. It is widely believed that the degradation is caused by the drain-to-gate coupling effect of the FG device [30]. In contrast, the SONOS device is not vulnerable to this effect, because such coupling effect is effectively eliminated in the discrete-trap storage structure, as mentioned in the previous section [31].

As listed in Table 3.1, we compare program/erase conditions and the speed performances for both flash memory devices. Despite the fact that the SONOS device has a poor P/E speed, it can be improved by further thinning down the tunneling oxide.

3-3 Reliability Analysis

3-3.1 Drain Side Stress

High-field carrier injection into the oxide during P/E operation is usually considered the main mechanism responsible for reliability degradation. Because of the array organization of the memory, however, several other parasitic processes may also contribute. The situation is shown in Fig. 3.13(a), in which a memory cell (e.g., cell #1) is programmed, while all the other cells sharing the same bitline (such as cell #2) are subjected to a high drain bias. BBT current may occur in these cells (Fig. 3.13(a)) and leads to undesirable threshold voltage shift. Such phenomenon is called program

(or drain) disturb [32] [33]. In this work we examined the data conservation ability under such drain side stress in the two types of memory devices. After the stress, we evaluated the threshold voltage degradation caused by the holes BBT injection. Devices were stressed at a high drain voltage, while V_G, V_S and V_B were all grounded. The results are shown in Figs. 3-14(a) and 3-14(b). In Fig. 3.14(a), it is clearly seen that the threshold voltage shifts significantly for FG devices under V_D of 7V. On the contrary, despite the fact that the device is operated under higher V_D read/write/erase conditions, the SONOS memory device still maintains better data conservation ability.

3-3.2 Data Retention under Thermal Stress

Nonvolatility implies at least ten years of charge retention. In other words, the data state should be maintained over such a long period of time whether the device is powered ON or OFF. The confidence in flash reliability has grown together with the understanding of reliability mechanisms in the memory devices [34].

High temperature data retention analysis has been performed by monitoring the programmed threshold voltage as a function of the elapsed time. The measurements were performed at 50 ^{o}C, 85 ^{o}C, and 125 ^{o}C. Retention characteristics of both memory devices are shown in Fig. 3.15. The results clearly indicate that the FG device is subject to small threshold voltage degradation under the high temperature stress. On the other hand, for SONOS devices, much worse retention characteristics are observed regardless of the program methods (CHISEL or CHEI). It is also interesting to note that the retention extrapolation shows the charge loss results in approximately 1.4 V of threshold voltage shift in the SONOS device after ten years under stress temperature of 125 ^{o}C. The charge loss mechanisms and paths are schematically shown in Figure 3.16(a). There are two major leakage current components relating to the charge loss: one is the thermionic emission, the other is the direct tunneling (DT)

through either top or tunnel oxide. Accordingly, it is reasonable to assume that the degradation is mainly caused by the thinner top oxide induced DT charge loss in the SONOS device. We can directly calculate the effective oxide thickness t_{eff} of ONO and total charge loss (△Q) [35] by the following relationships,

$$t_{eff} = A\varepsilon_{ox} / C_{eff} \quad \text{3-2}$$

$$\Delta Q = \Delta V_{th} \cdot \frac{A\varepsilon_{ox}}{t_{eff} - t_{ox} - t_N \cdot \varepsilon_{ox}/\varepsilon_N} \quad \text{3-3}$$

where t_N is the distance between the charge centroid and SiN/bottom-oxide interface. The △Q plots of the SONOS device are obtained by assuming that the charge centroid is located at the SiN/bottom-oxide interface, as shown in Figure 3.16(b). It reveals that two different dominant leakage components can be observed in a SONOS device. Specifically, the leakage behavior of the SONOS device is governed by DT via top oxide in the early stage, followed by the thermionic emission for which trapped charges are thermally excited, as shown with path 1 (Figure 3.16(a)). Compared with the FG device which exhibits few DT charge loss (Figure 3.15(a)), one important implication from the SONOS device retention data is that the leakage is dominated by DT in the early stage of stress, and later by thermionic emission when the stress time is sufficiently long. In order to prevent DT charge loss in the SONOS device, thicker top and tunneling oxides are necessary. However, a thicker oxide results in higher operation voltage. Trade-off should thus be carefully made in terms of optimized device performance, reliability, and power consumption.

3-3.3 Endurance

For conventional flash memory the minimum number of program/erase (P/E) cycles that the device must sustain is 100K, regardless of the P/E mechanisms.

Typical cycling is known to cause a fairly uniform deterioration of device performance, eventually limiting the endurance of flash memory. The P/E cycling conditions are summarized in Table 3.2.

To study the behavior of the cycling, 5,000 P/E cycles are applied to both FG and SONOS devices which are programmed by CHEI or CHISEL mechanisms, respectively; and are erased by using FN tunneling and HHI, respectively. Endurance characteristics of the two types of devices are shown in Fig. 3.17. We can see that the SONOS device maintains a wide and stable window of around 3V even after 5,000 P/E cycles. By contrast, the FG device exhibits window shrinkage with the evolution of P/E cycling. To understand the characteristics more clearly, we measured I_D-V_G characteristics of both devices before and after 5,000 P/E cycles. The results are shown in Fig. 3.18. For FG device, the positive V_{th} shift of the erased state is ascribed to electron-trapping in the tunnel oxide. Furthermore, the increased V_{th} in the erased state tends to reduce the CHEI programming current and thus leads to the decrease in V_{th} of the programmed states, resulting in a narrowing of the V_{th} window ($\triangle V_{th}$=2V) after 5,000 P/E cycles, as observed in the FG device. Nevertheless, these effects do not cause serious degradation in Gm and I_d of the device. On the other hand, although the window does not shrink, the SONOS device exhibits degradation in subthreshold swing (SS) after 5,000 P/E cycles, as shown in Fig. 3.18(b). This is ascribed to the generation of additional interface states during the programming and erasing operations [36].

Actually a slight transconductance (Gm) degradation is observed after 1, 1,000 and 5,000 P/E cycles for the FG device, as shown in Fig. 3.19. In contrast, Figs. 3.20(a) and 20(b) show that the SONOS device encounters degradation in SS and Gm after the P/E cycles. We compare SS and Gm degradation for the two types of devices in Figure 3.21(a) and Figure 3.21(b), respectively. It is obviously seen that SS and Gm

degradation of the SONOS device are worse than those of the FG device. This phenomenon will be discussed and investigated in more detail in Section 3-3.4.

3-3.4 Charge Pumping Analysis

It is well known that a considerable amount of interface states and traps in the oxide are generated during program/erase cycles. In order to fully comprehend the cause for the degradation mechanisms of endurance, a complete understanding of the interface states of both memory devices with P/E cycling operation is necessary. To clarify the relation between the degradation and oxide damage such as interface states and oxide charges, we employed a novel charge pumping (CP) measurement [37], which proceeds with a fixed amplitude (V_h). The measurement scheme presented in Section 2-2.3 was used to extract interface trap state in both memory devices.

To detect the interface states, the voltage pluses applied during measurement must undergo alternate accumulation and inversion cycles. Here the plus base level (V_{base}) varies from -1V to 1V, while the amplitude of the pulse is kept at 1.5V with 1MHz in frequency. However, since V_h is set larger than the highest V_{th} along the whole channel, charge pumping current (I_{cp}) will begin to grow while V_h starts to exceed the local V_{th} in the channel.

First, we choose a FG device and a SONOS device and measure the incremental charge pumping current ($\triangle I_{cp}$) at 1, 1,000 and 5,000 P/E cycles. The results are shown in Fig. 3.22 and 3.23, respectively. We speculate that the different outcomes in the two figures correspond to the use of different programming operations, namely, CHEI and CHISEL schemes [38]. When the SONOS device is programmed by the CHISEL method, numerous secondary or hot electrons are injected into the nitride from across the substrate. It means that such mechanism may generate a uniform distribution of numerous interface states at the channel/oxide interface in the SONOS

device [39]. As a result, the subthreshold slope is severely degraded by the generated interface defects. On the other hand, the FG device is programmed by the CHEI method, and the charge injected by CHEI stays localized near the drain region. This contributes to the fact that the I_{cp} current only slightly increases by the generated interface states in the neighboring drain side region [40]. As the interface state density (N_{it}) is assumed to be spatially uniform along the channel, the charging pumping current can be expressed with the following form:

$$I_{cp,max} = q f Nit WL, \qquad 3\text{-}4$$

where f is the gate pulse frequency, W is the channel width, and L is the channel length. From $I_{cp,max}$ measurement and Equation 3-4, we can calculate the effective N_{it} of both memory devices after 1,000 and 5,000 P/E cycle stresses, and the results are shown in Fig.3.24. Compared with the figures, it agrees with the aforementioned inference that the interface trap states of floating-gate device are less than those of the SONOS device after P/E cycling. These results indicate good correlation between the interface state density characteristics and the degradation of SS and Gm behaviors after P/E cycling.

Form a reliability standpoint, although the CHISEL programming of the SONOS device will cause numerous interface states and degrade SS and Gm, it is still acceptable in terms of meeting the demand of operation window after P/E cycling. The FG devices do not suffer from the interface degradation, but significant window shrinkage is observed. Such finding is attributed to the electron trapping events in the tunneling oxide after P/E cycles.

Chapter 4
Summary and Conclusions

Semiconductor flash memory device technology will continue to play an important role in the electronics industry, although its development has been facing a lot of challenges. Conventional FG structure suffers from serious coupling issues that degrade the device characteristics and may eventually limit further device scaling. It thus faces fierce competition from a number of new types of devices, including the SONOS.

In this thesis, we fabricate, characterize, and compare the characteristics of FG and SONOS flash non-volatile memory device using a conventional process with LOCOS isolation. Fundamental electrical characteristics, program/erase (P/E) speed, and the associated reliability were investigated. Several important phenomena were observed and summarized as follows.

First, we found that the gate coupling effect indeed hinders the operation of FG devices. Aggravated short-channel effect (SCE) is observed for FG devices scaling because of the gate-to-drain parasitical coupling effect. Such situation could be effectively relaxed with the SONOS devices, owing to the use of an ultra-thin charge storage layer which could help reduce the height of the gate structure.

Secondly, although the SONOS devices exhibit slower programmed speed over the FG ones, it can be improved by using a thinner tunneling oxide. It also reveals that good subthreshold characteristics could be retained for these devices after write/erase cycles.

Thirdly, interface trap generation is mainly responsible for the threshold voltage shift of SONOS devices after a large number of P/E cycles. Such effect, however, may not result in Vt window narrowing. In contrast to this, trapping of electrons in the

tunnel oxide is identified as the major mechanism for FG devices, causing a shrinkage of Vt window with increasing number of P/E cycles.

New materials and novel device structure are always indispensable for flash memory scaling and device performance improvement. From the results obtained in this work, it is confirmed that discrete trap-based flash memory is more scalable than FG memory device. Besides, the fabrication of SONOS devices is compatible with current CMOS processing and is thus a suitable candidate for embedded memory applications. In order to achieve better chip performance and low cost, however, more efforts are required to further optimize the device performance, especially the reduction of P/E speed and better reliability.

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Tables

Performance Comparison Table		
Item \ Device	Floating Gate	Single Gate SONOS
PGM	CHEI	CHISEL
ERS	HHI/BTBT FN	HHI
PGM V_D Range	3~5.8V	4.1~6.3V
ERS V_D Range	<6.5V	<11V
PGM Voltage	V_G =10V V_D =5V V_B =0	V_G =10V V_D =5V V_B =-4V
ERS Voltage	V_G =-15 V_D =5V V_B =0V	V_G =-15V V_D =8V V_B =5V
PGM Speed	0.5m sec	10m~100m sec
ERS Speed	100m sec	100m ~1 sec
Forward Read	V_D =0.1~2V	V_D =0.1~5V

Table 3.1 Performance and operation window between the FG and the SONOS memory devices.

#	SONOS		Floating gate	
	Program	Erase	Program	Erase
Method	CHISEL	HHI	CHEI	BBT-FN
V_D (V)	5	8	5	5
V_G (V)	10	-15	10	-15
V_S (V)	0	0	0	0
V_B (V)	-4	5	0	0
Time(Sec)	400m	100m	1m	100m

Table 3.2 Endurance operation conditions in the FG and the SONOS memory devices.

Figures

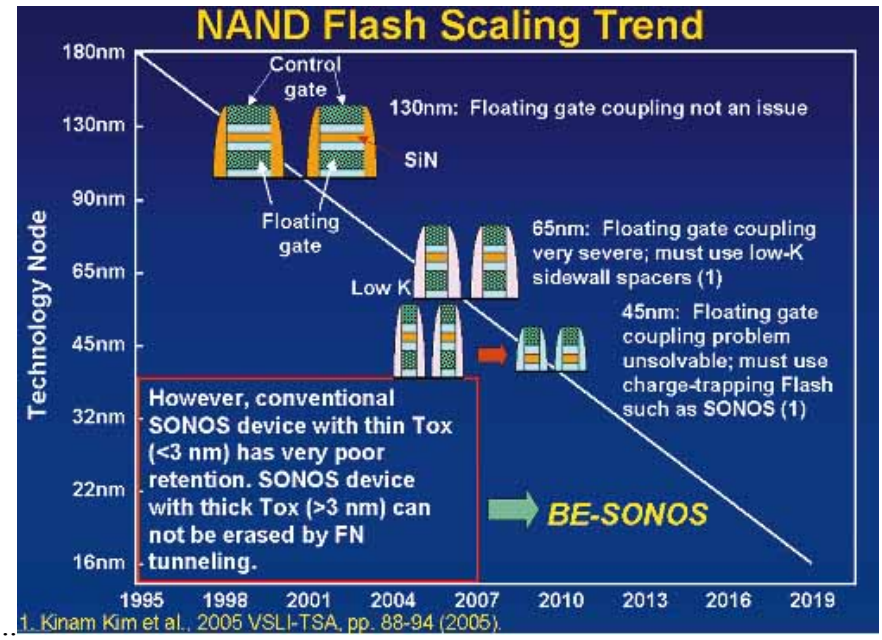


Fig 1.1 Scaling trend for flash memory device development [13]

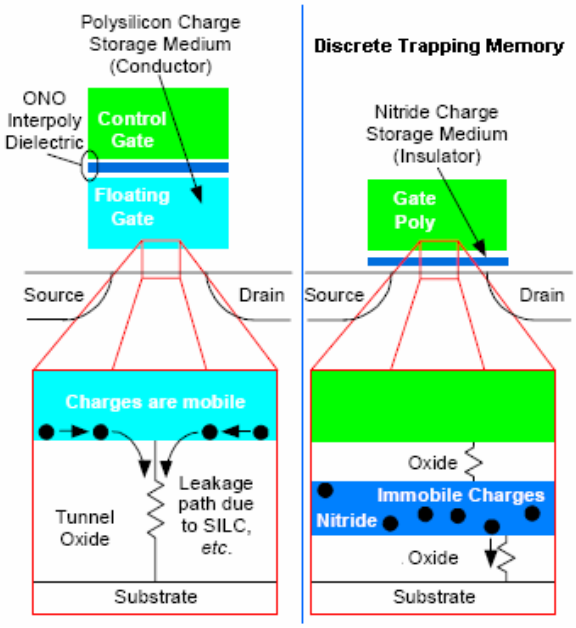


Fig 1.2 Diagrams illustrating physical structures of floating-gate and discrete trapping (SONOS) devices [7]

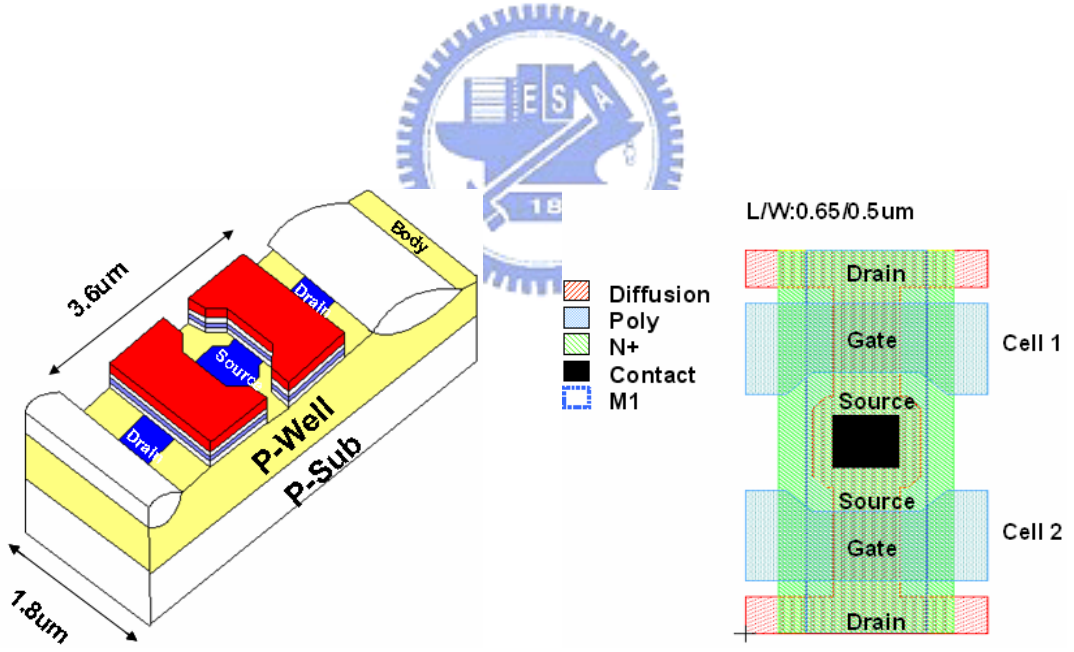
ACTIVE	PAD OXIDATION
	SIN DEP
	ACTIVE ETCH
WELL	P-WELL IMP
FOX	FOX & DRIVE-IN
	SIN REMOVE
VT	VT IMP
GOX	GOX(2)
POLY1	POLY(1) DEP
	N+ DOPING
ONO	OXIDATION
	THIN SIN DEP
	OXIDATION
POLY2	POLY(2) DEP
	N+ DOPING
S/D IMP	N+ S/D IMP
ILD	BPSG DEP
CONT	W-CONT ETCH
M1	ARC-ALCU SPUTTER

(a)

ACTIVE	PAD OXIDATION
	SIN DEP
	ACTIVE ETCH
WELL	P-WELL IMP
FOX	FOX & DRIVE-IN
	SIN REMOVE
VT	VT IMP
GOX	GOX(2)
Nitride	THIN SIN DEP
	OXIDATION
POLY2	POLY(2)
	N+ DOPING
S/D IMP	P+S/D IMP
ILD	BPSG DEP
CONT	W-CONT ETCH
M1	ARC-ALCU SPUTTER

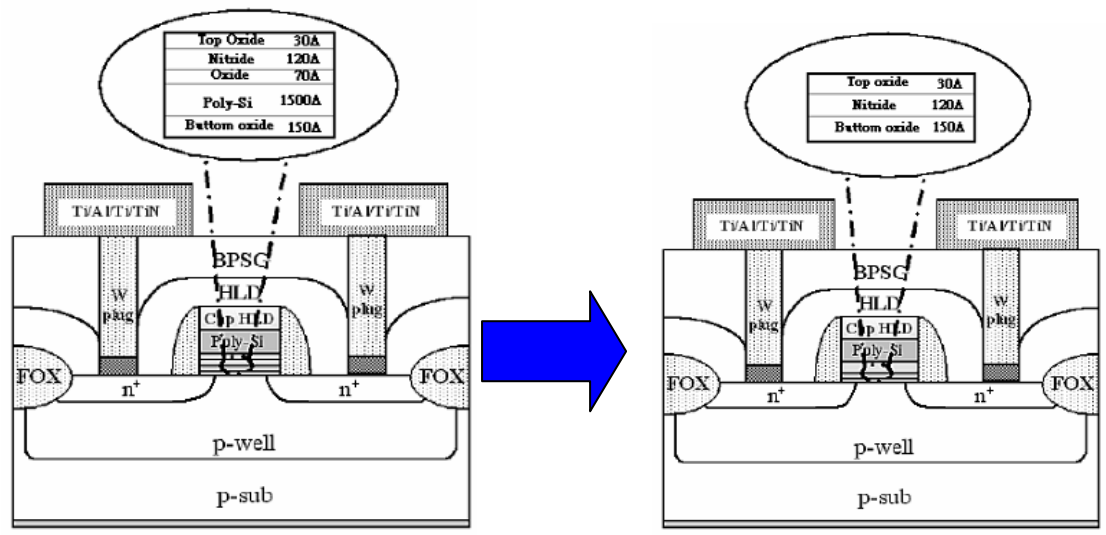
(b)

Fig 2.1 Flash memory device process flows: (a) conventional floating gate flash and (b) silicon-oxide-nitride-oxide-silicon (SONOS) stacked gate flash.



(a) (b)

Fig 2.2 Flash memory device structure (a) Cross-sectional view and (b) Layout.



(a) **(b)**

Fig 2.3 Cross-section view of flash memory devices with (a) Floating gate and (b) SONOS stacked gate.

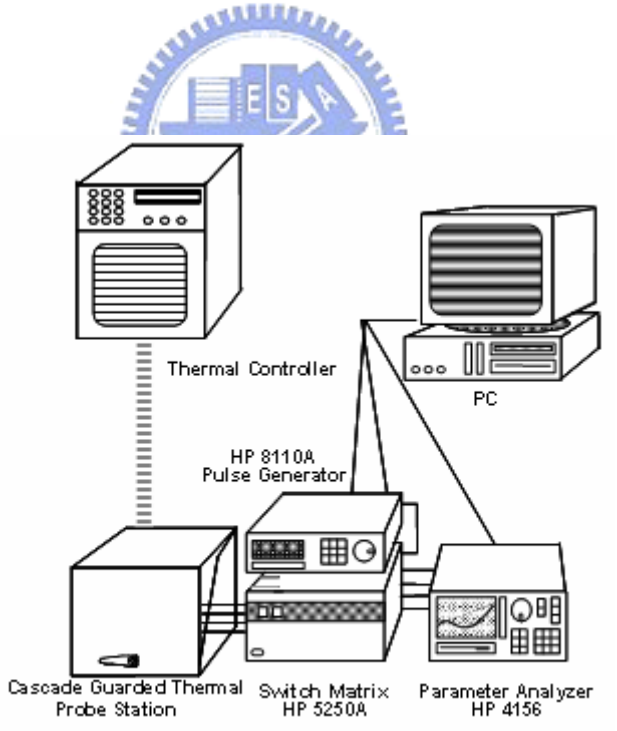


Fig 2.4 Experimental setup for basic charge pumping measurements.

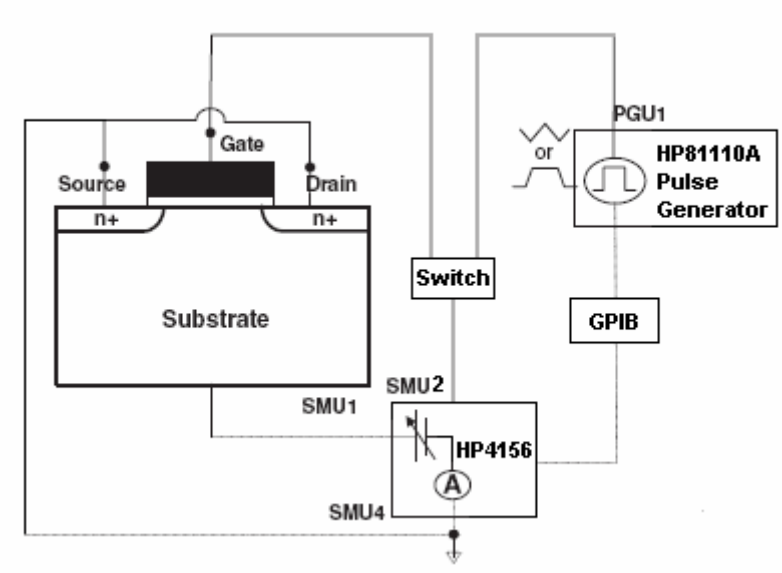


Fig 2.5 Detailed schematic for charge pumping measurement setup.

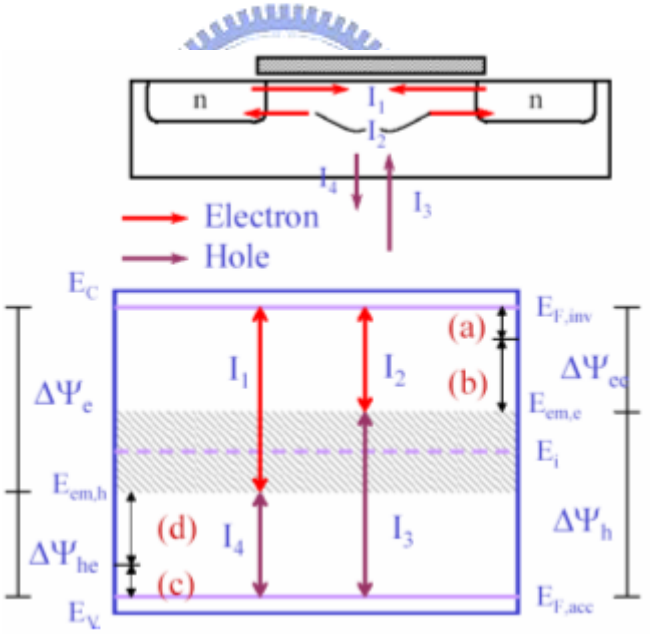


Fig 2.6 Principles of Icp current measurements.

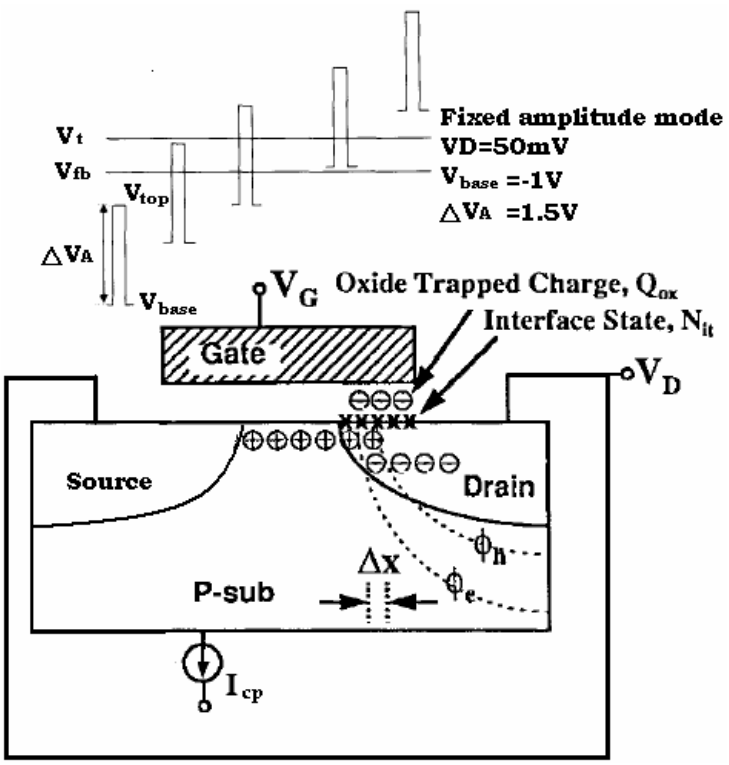


Fig 2.7 Schematic illustration of charge pumping measurements with fixed amplitude.

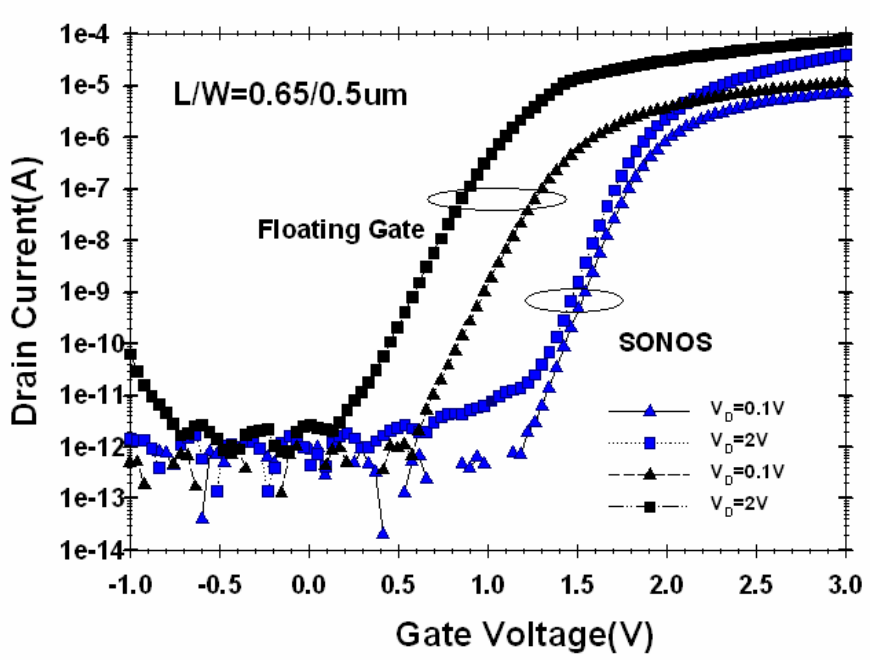


Fig 3.1 I_D–V_G Characteristics of N-channel FG and the SONOS memory devices. Channel length/width = 0.65μm /0.5μm.

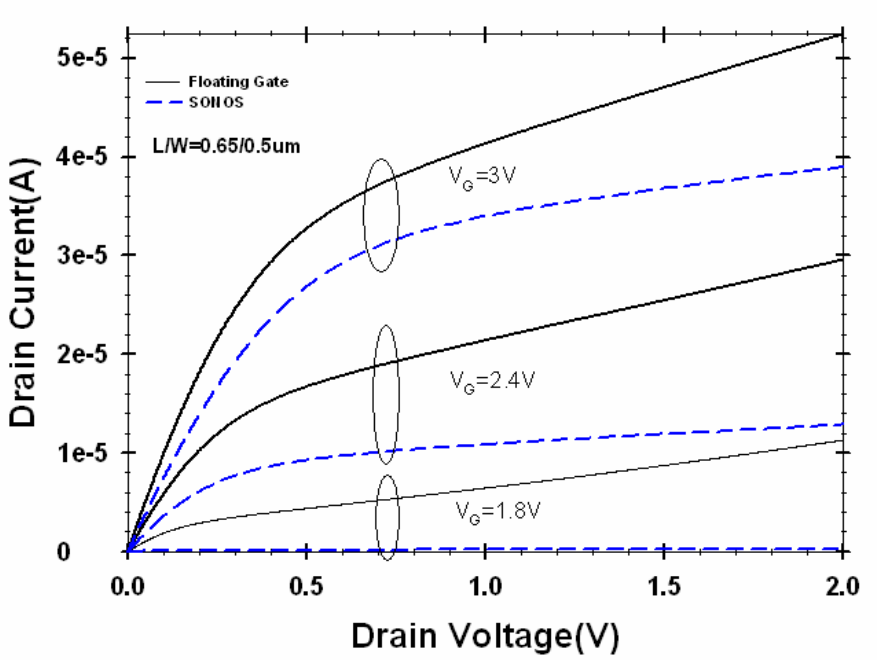
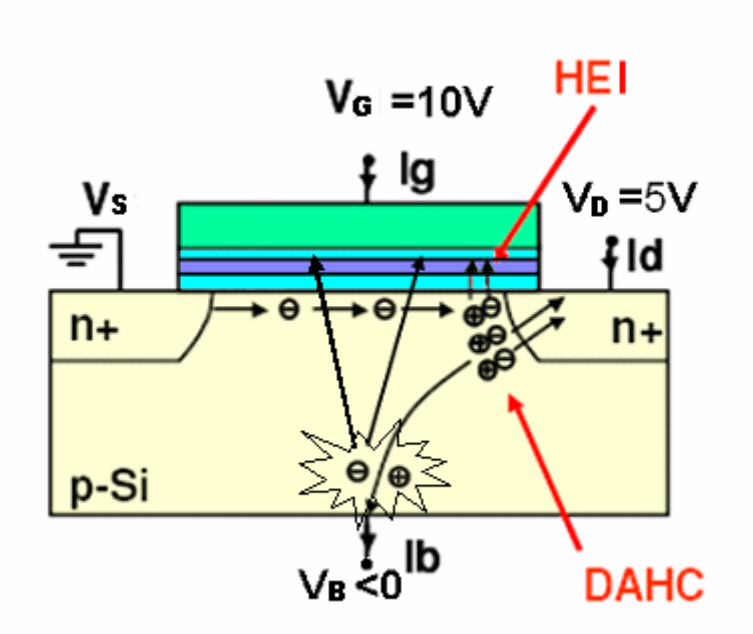
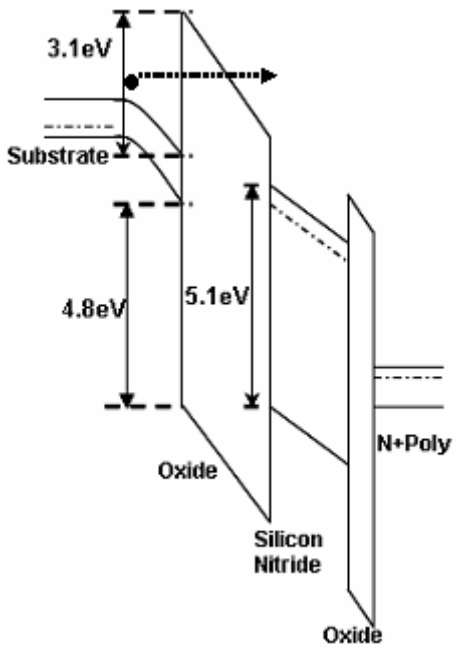


Fig 3.2 I_D–V_D Characteristics of N channel FG and the SONOS memory devices. Channel length/width = 0.65μm /0.5μm.

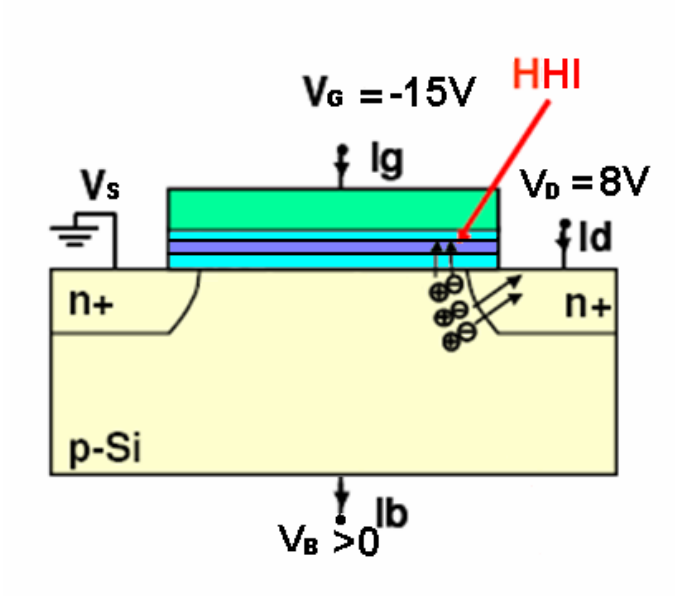


(a)

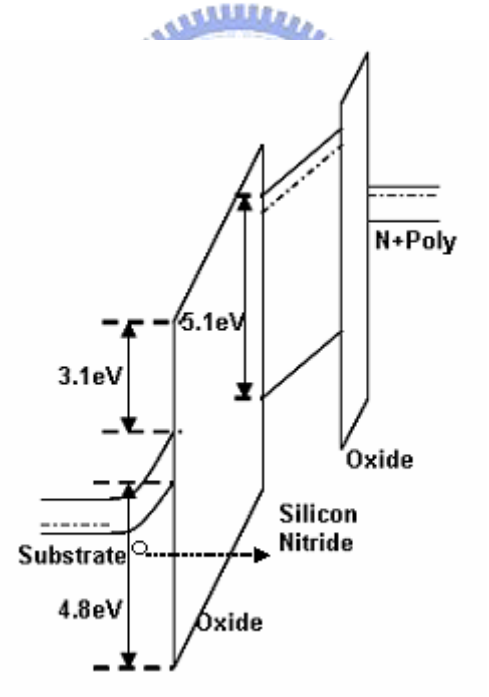


(b)

Fig 3.3 Channel-initiated secondary electron (CHISEL) programming mechanism for n-channel SONOS memory device. (a) Programming conditions and related events inside the substrate. (b) Band gap diagram for the programming.

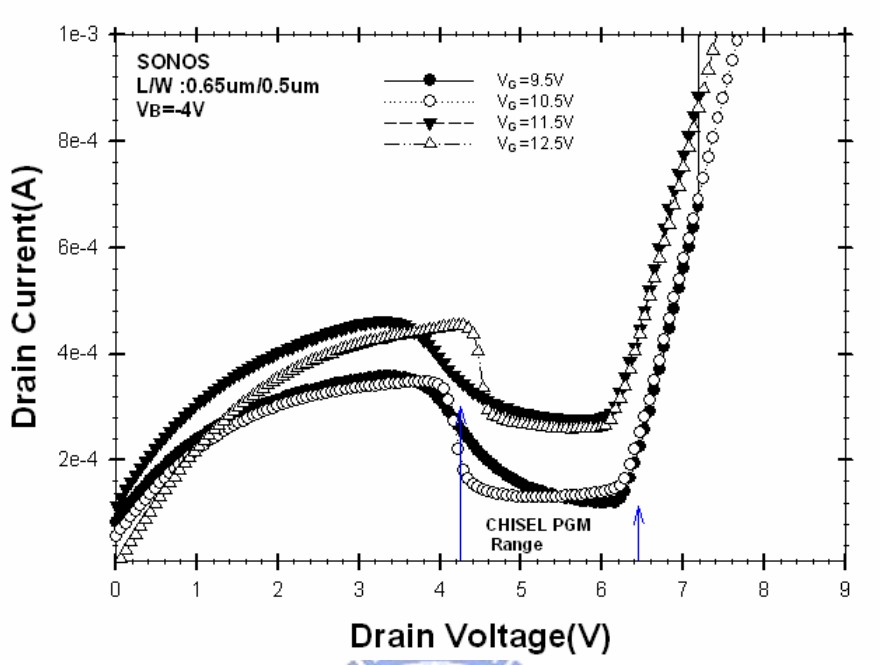


(a)

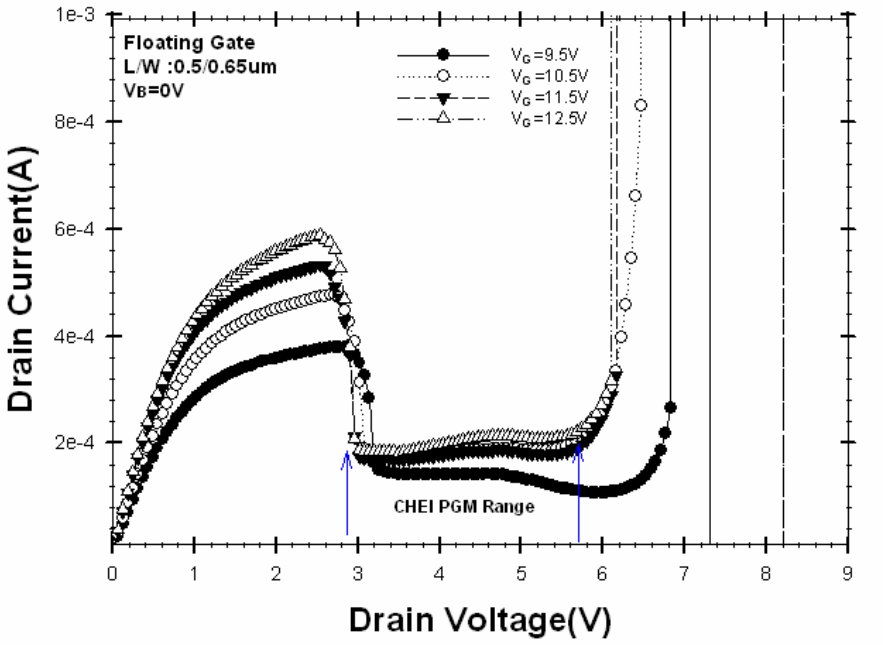


(b)

Fig 3.4 Hot holes injection (HHI) erasing characteristics of N channel SONOS memory device. (a) Erasing conditions and mechanisms. (b) Erasing band gap diagram.



(a)



(b)

Fig 3.5 V_D operation range of programming. (a) CHISEL programming for SONOS devices. (b) CHEI programming for FG devices..

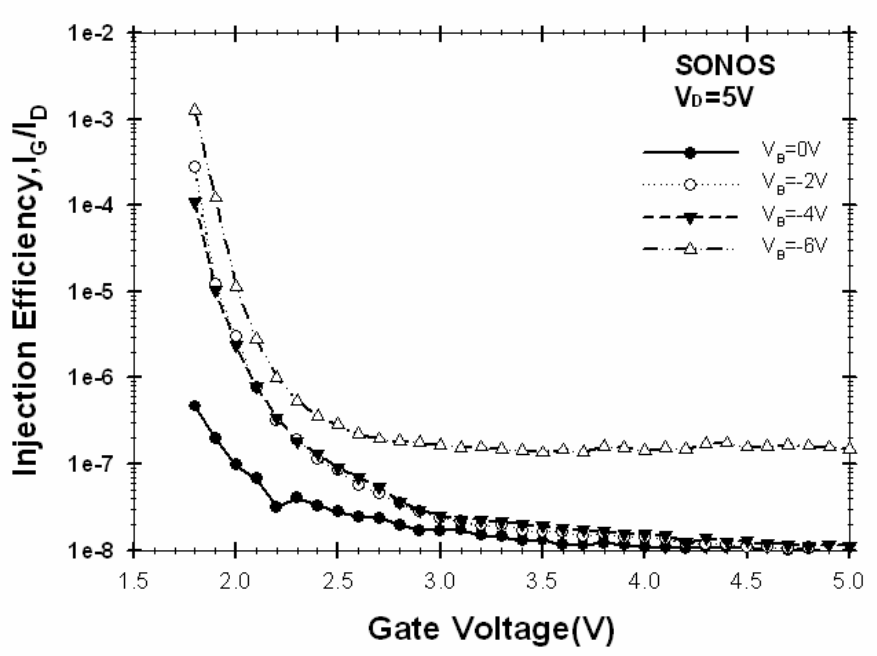
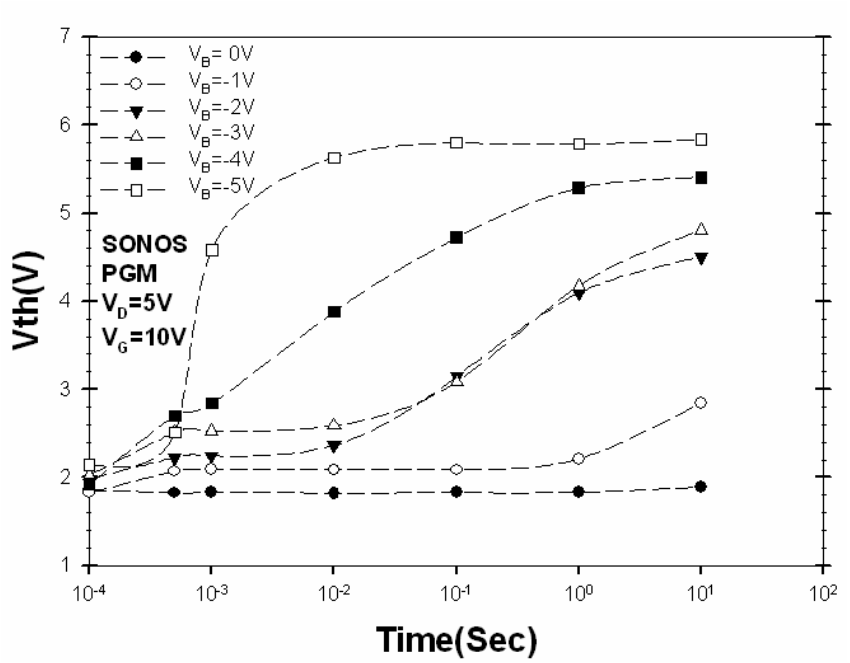
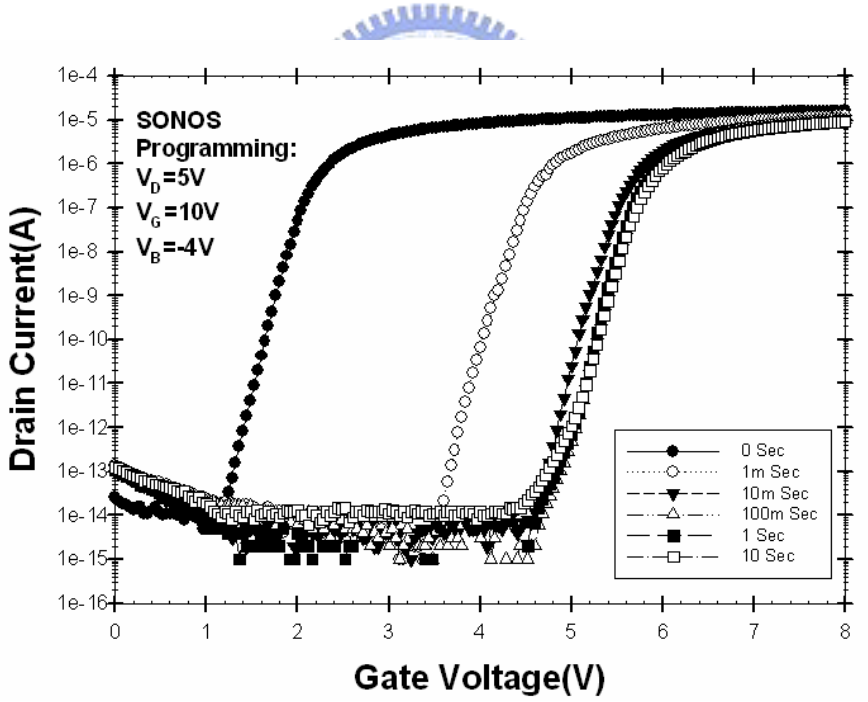


Fig 3.6 CHEI (V_B=0) and CHISEL (V_B<0) programming efficiency (I_G/ I_D) of carries injection for the SONOS memory devices with channel length/width = 0.65μm /0.5μm.

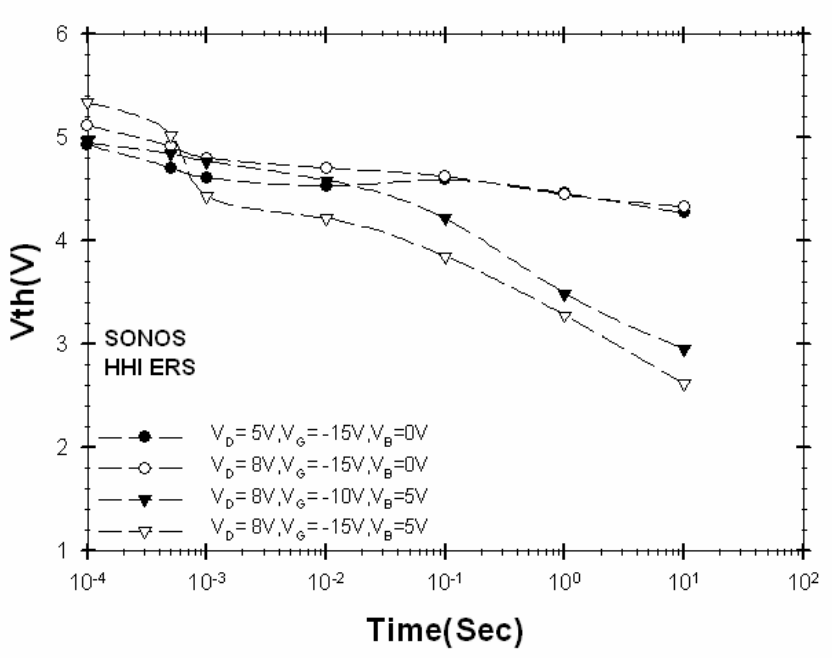


(a)

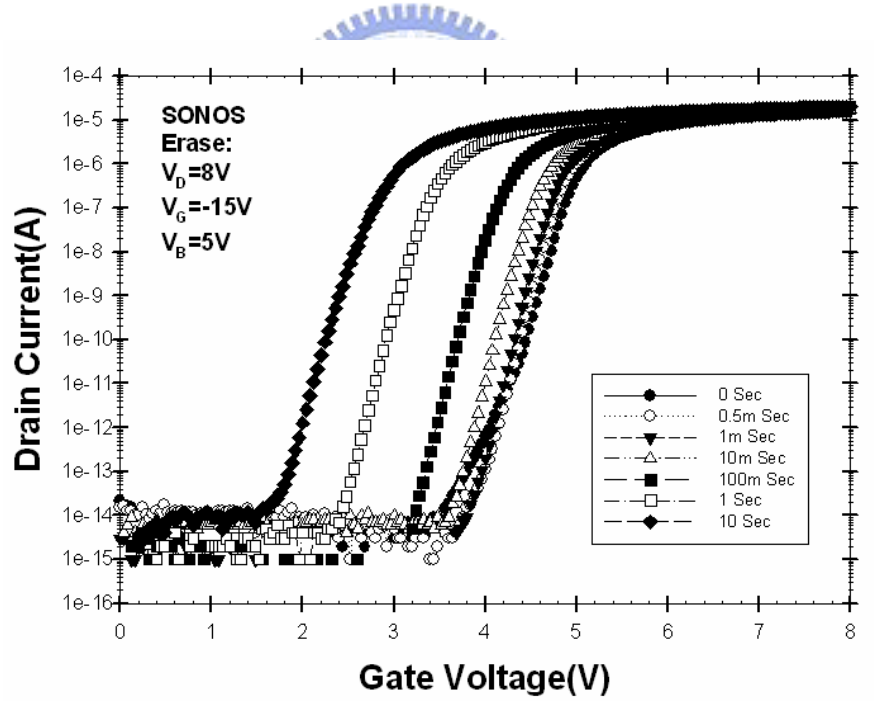


(b)

Fig 3.7 Programming characteristics of the SONOS memory devices. (a) Programming speed performance for different substrate bias (b) I_D–V_G curves in different CHISEL programming time with V_B=-4V.



(a)



(b)

Fig 3.8 Hot hole injection (HHI) erasing characteristics of the SONOS memory device. (a) Threshold voltage shift window and erasing speed. (b) I_D–V_G curves under different HHI erase time with V_B=5V.

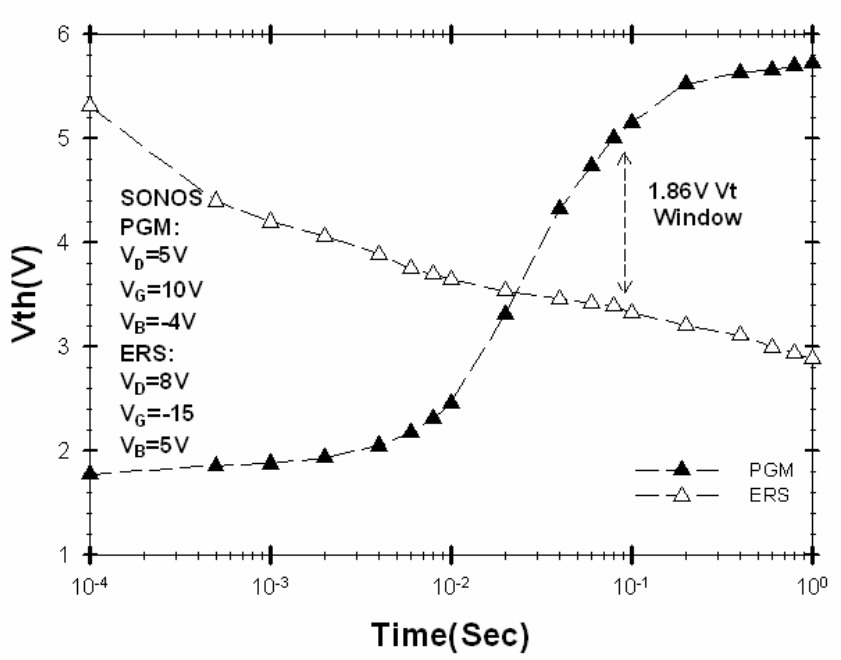


Fig 3.9 Threshold voltage window of the SONOS memory device between CHISEL programming and HHI erasing.

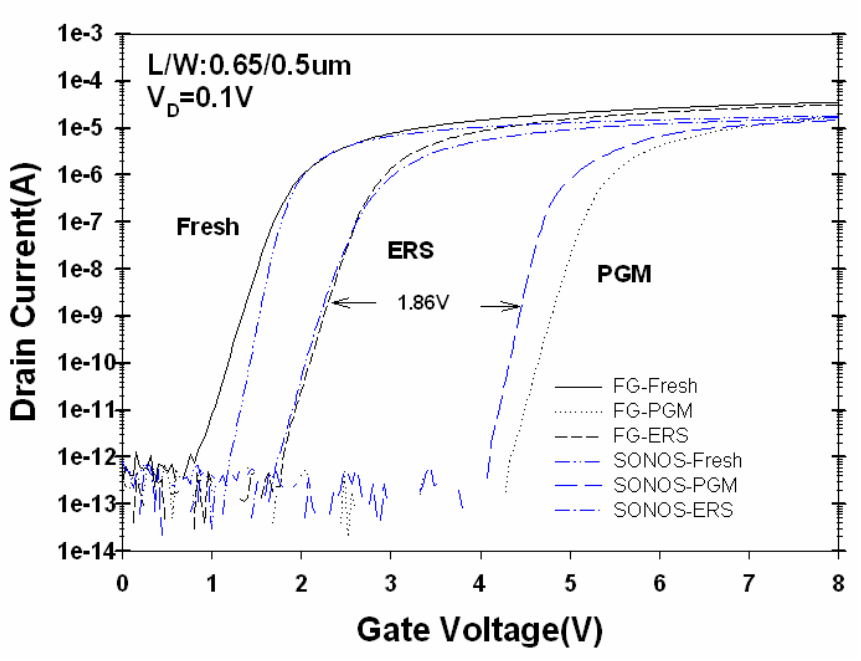


Fig 3.10 Subthreshold characteristics of FG and SONOS memory devices at different stage of operations.

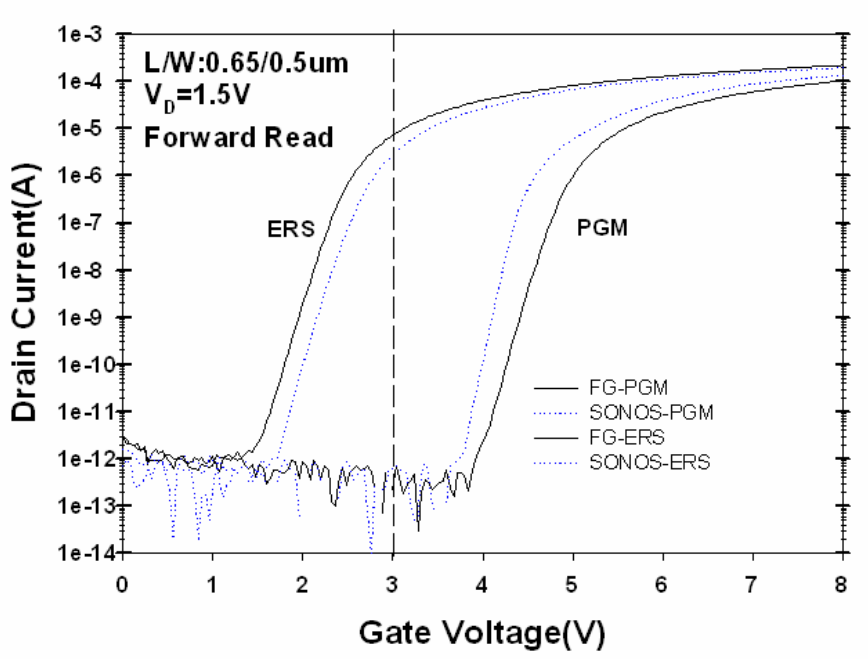


Fig 3.11 I_D–V_G **characteristics of forward read (V_D =1.5V) after programming and erasing in the floating gate and the SONOS memory devices.**

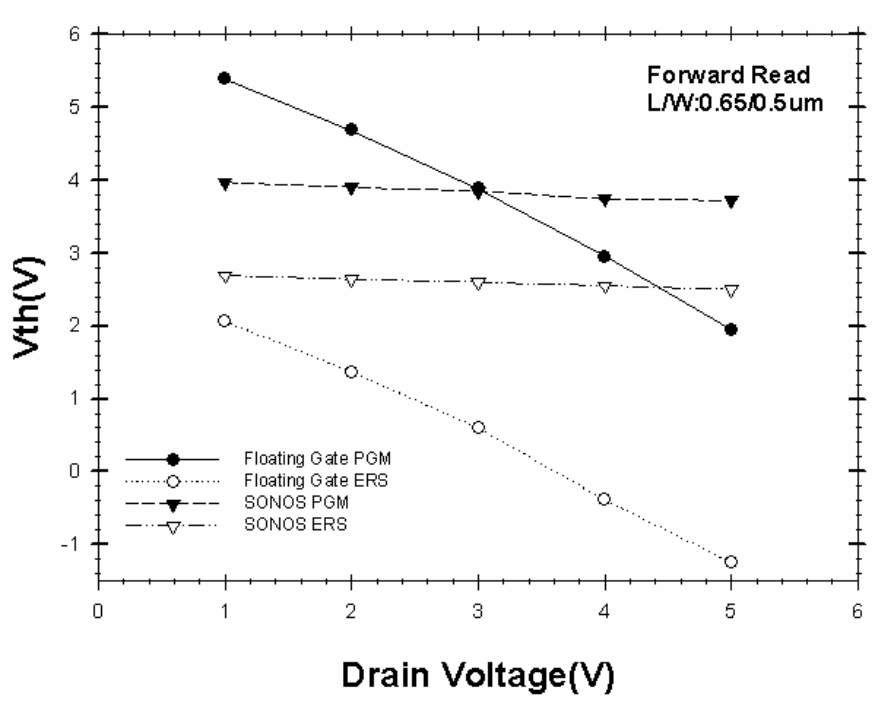
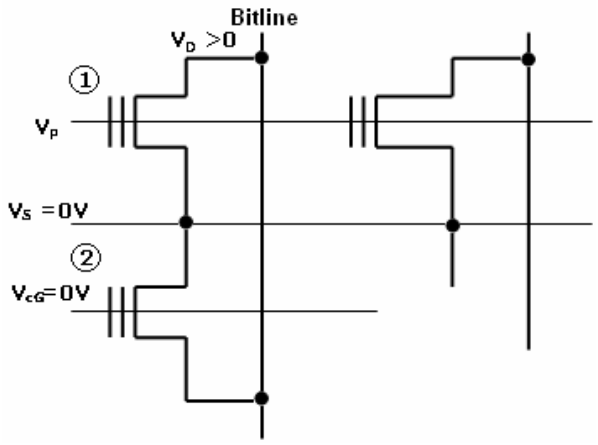
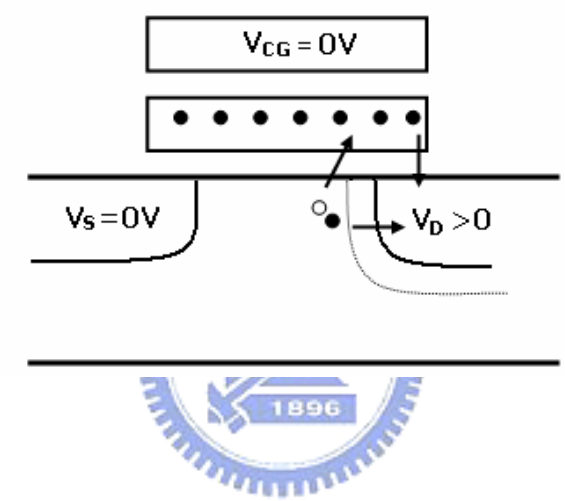


Fig 3.12 Threshold voltage of programmed and erased states as a function of V_D for the two types of devices.

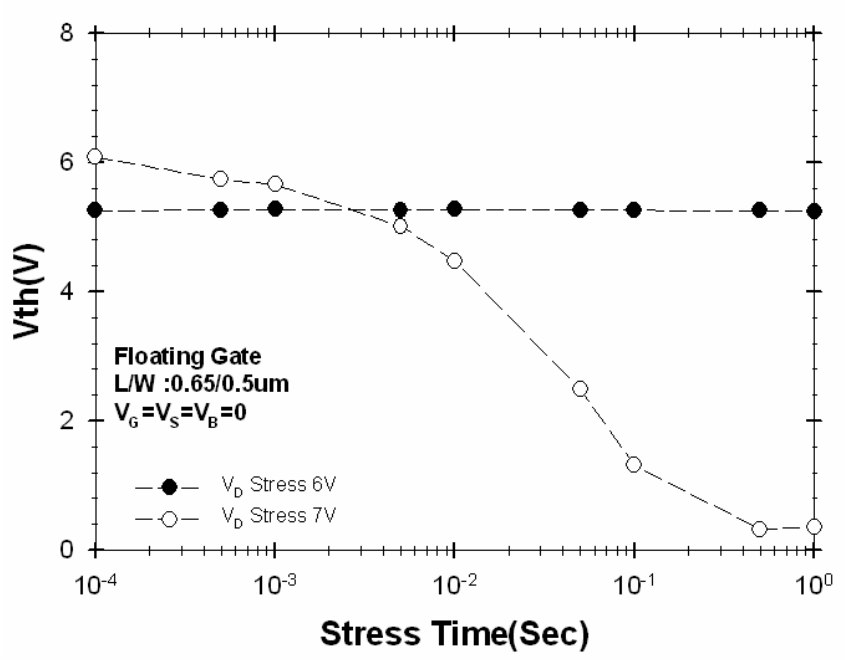


(a)

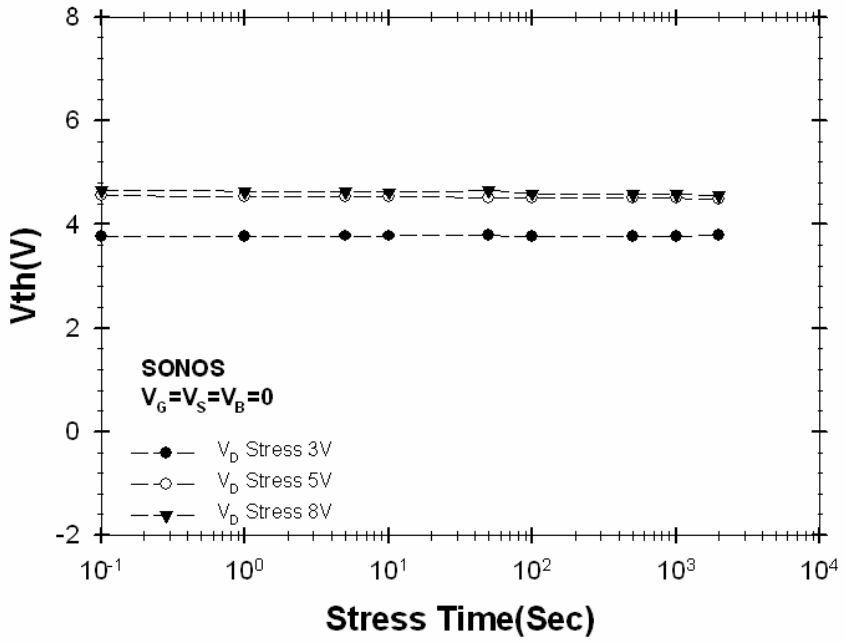


(b)

Fig 3.13 Schematic of parasitic carrier injection mechanisms under drain disturb on programmed cells. (a) Drain disturb in flash array circuit. Cell #1 is programmed and cell #2 is not programmed but sharing the same bitline (b) Hole BBT tunneling current may incur in the drain overlap region of the Cell #2 devices [32].

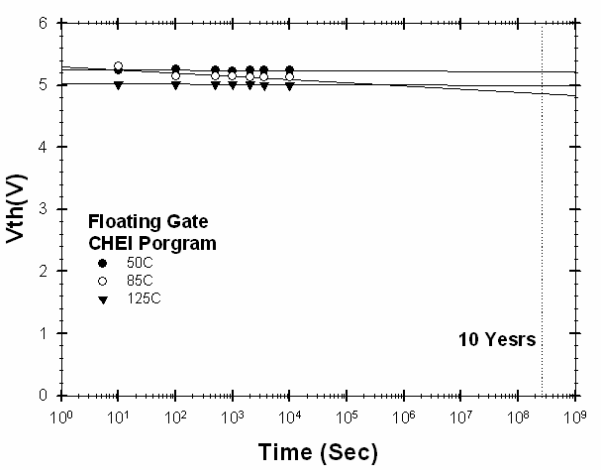


(a)

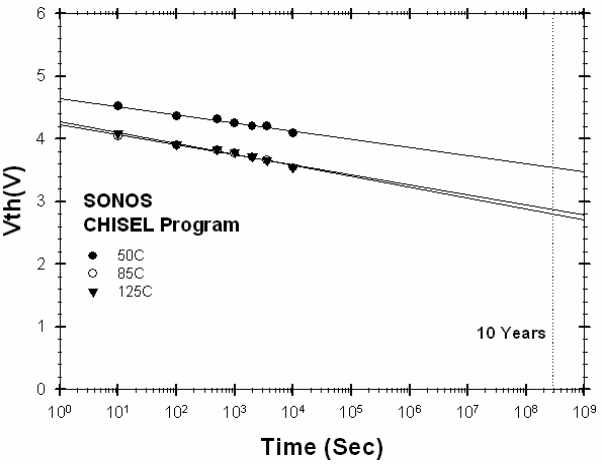


(b)

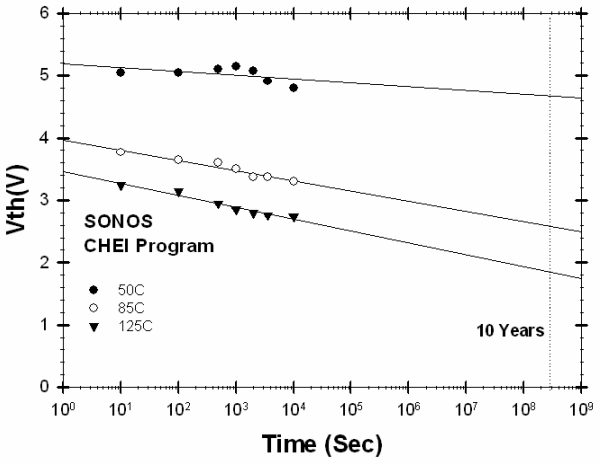
Fig 3.14 V_D Stress versus threshold voltage shift. (a) The floating gate devices. (b) The SONOS devices.



(a)

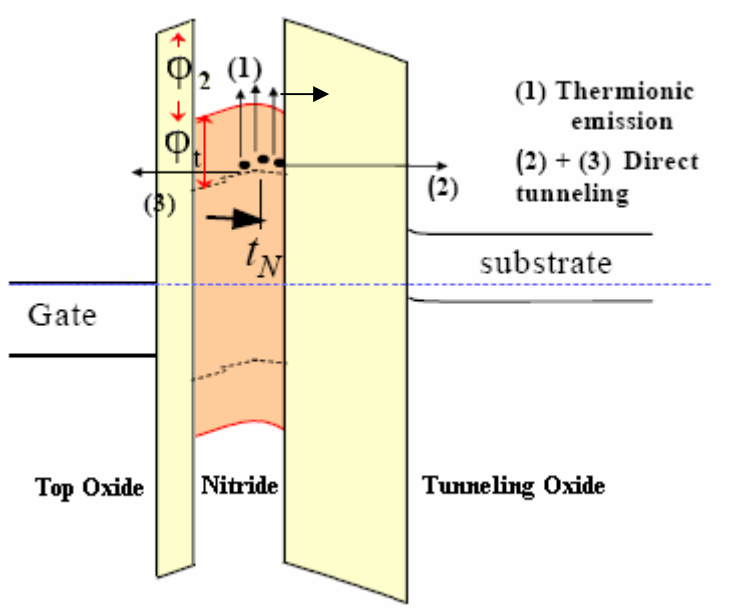


(b)

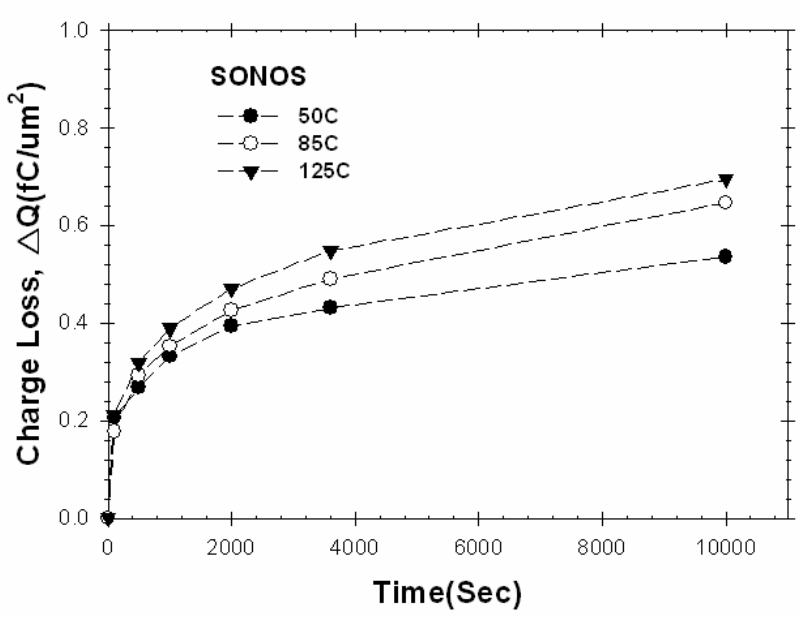


(c)

Fig 3.15 Data retention characteristics under elevated temperature stress at 50 °C, 85 °C and 125 °C. (a) CHEI program for FG devices. (b) CHISEL program for SONOS devices. (c) CHEI program for SONOS devices

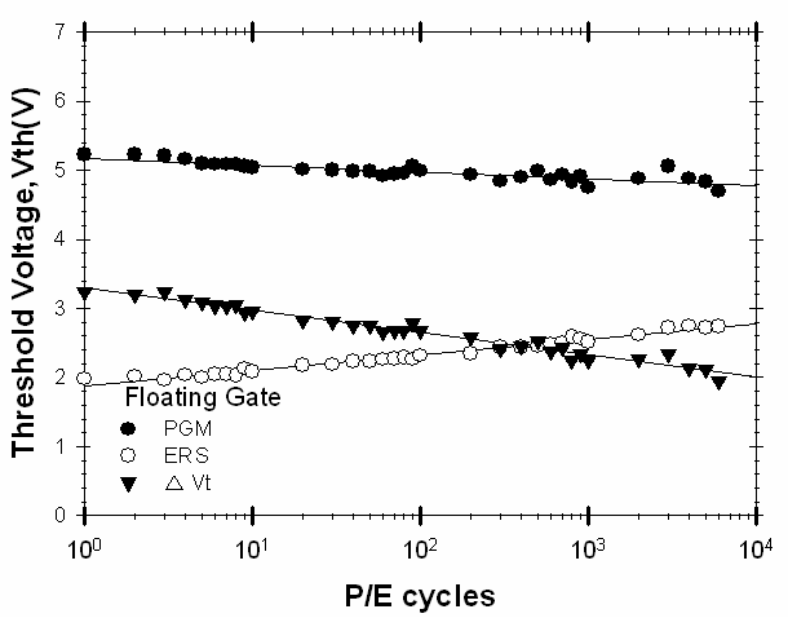


(a)

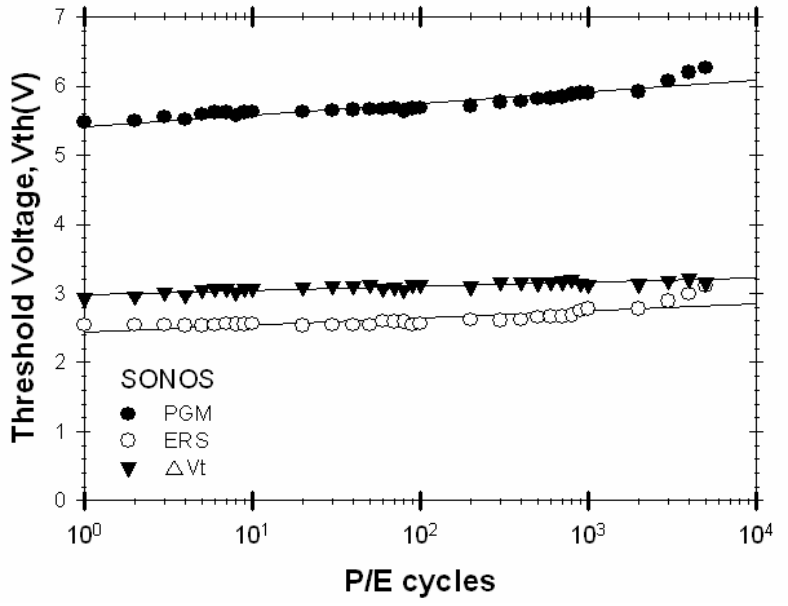


(b)

Fig 3.16 (a) The charge loss paths and the various leakage current components in an SONOS device [35]. (b) Charge loss performed at difference thermal stress for the SONOS memory device with channel length/width = 0.65μm /0.5μm.

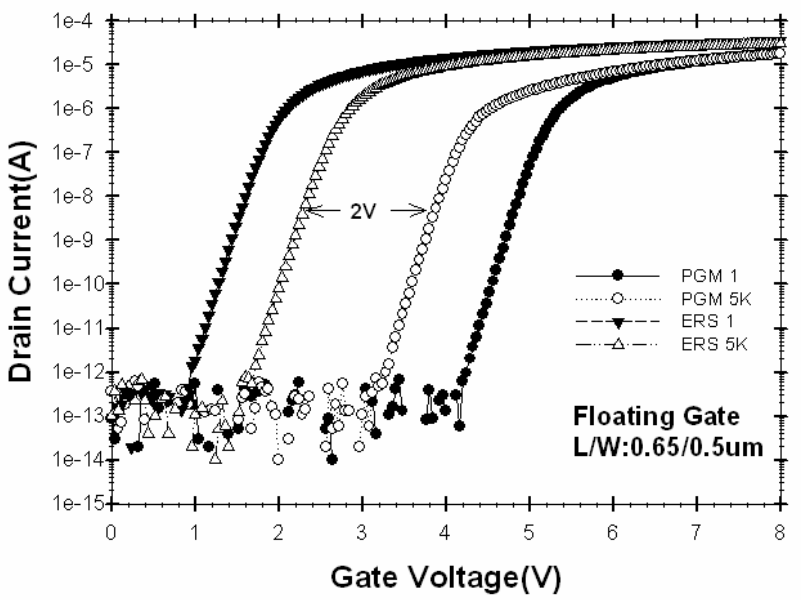


(a)

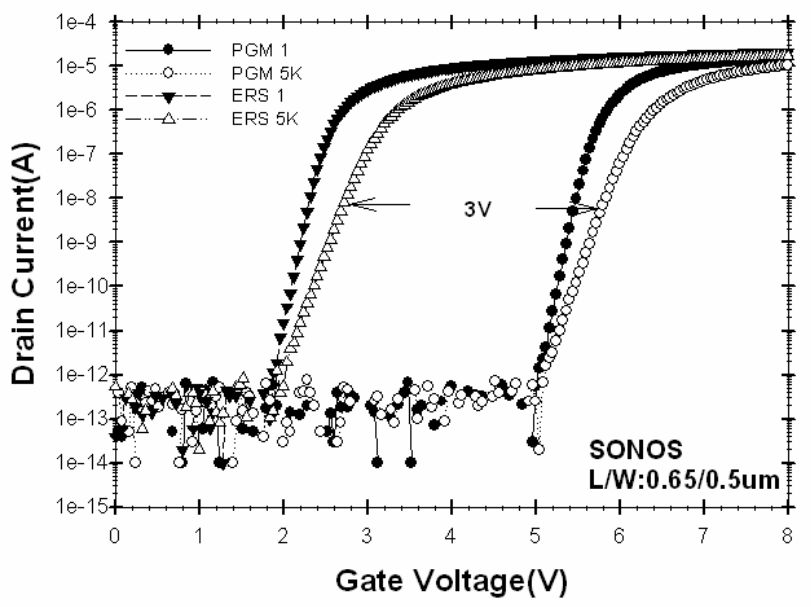


(b)

Fig 3.17 Endurance characteristics after program/erase (P/E) cycling stress. (a) The FG device. (b) The SONOS device.

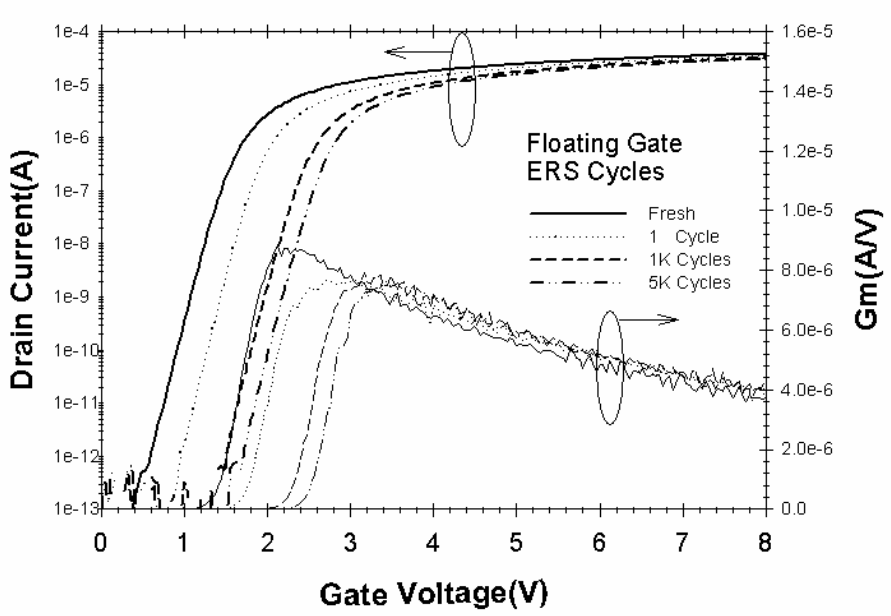


(a)

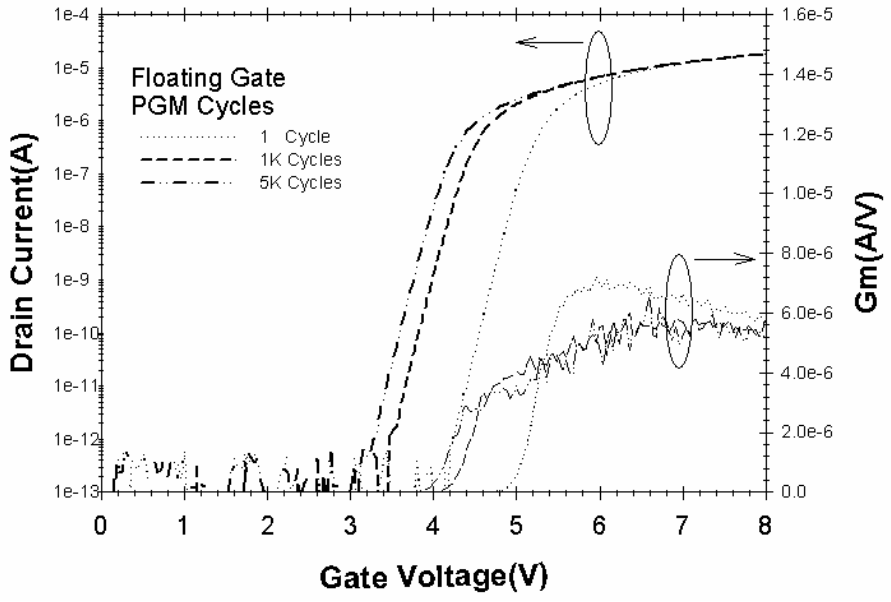


(b)

Fig 3.18 Subthreshold characteristics after 1 and 5000 times P/E cycles. Channel length/width = 0.65μm /0.5μm. (a) The FG device. (b) The SONOS device.

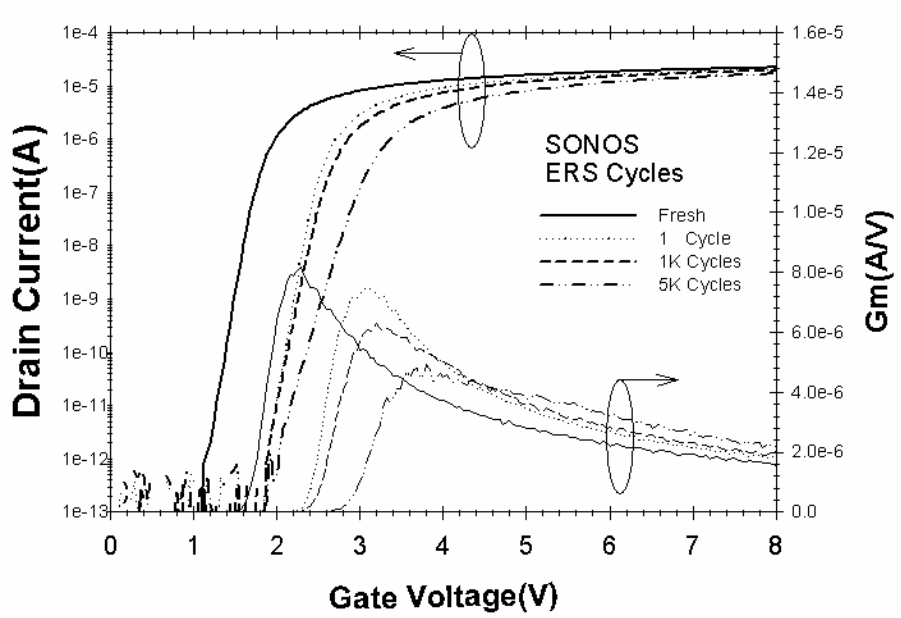


(a)

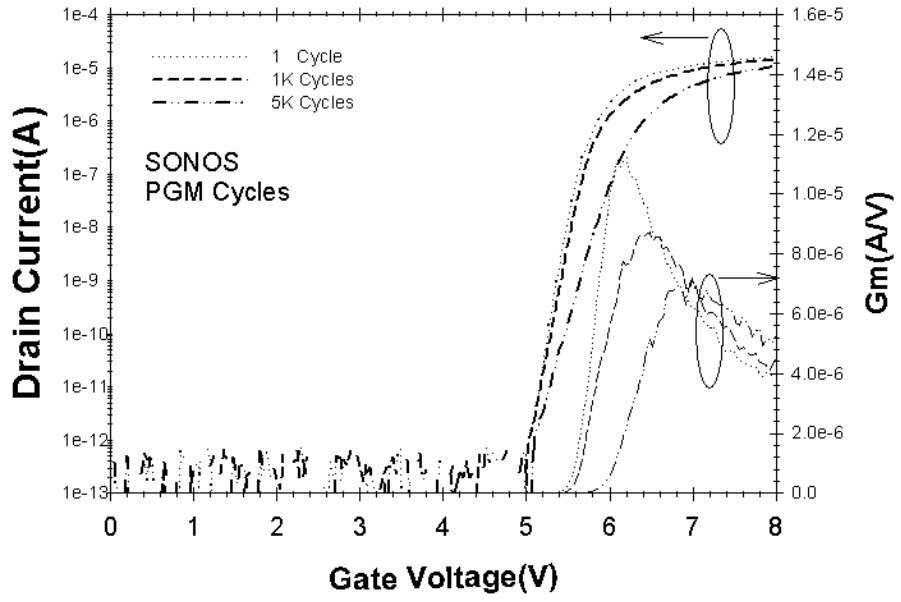


(b)

Fig 3.19 Subthreshold characteristics and transconductances of the FG memory device with length/width = 0.65μm /0.5μm. (a) Erasing and (b) programming operations.

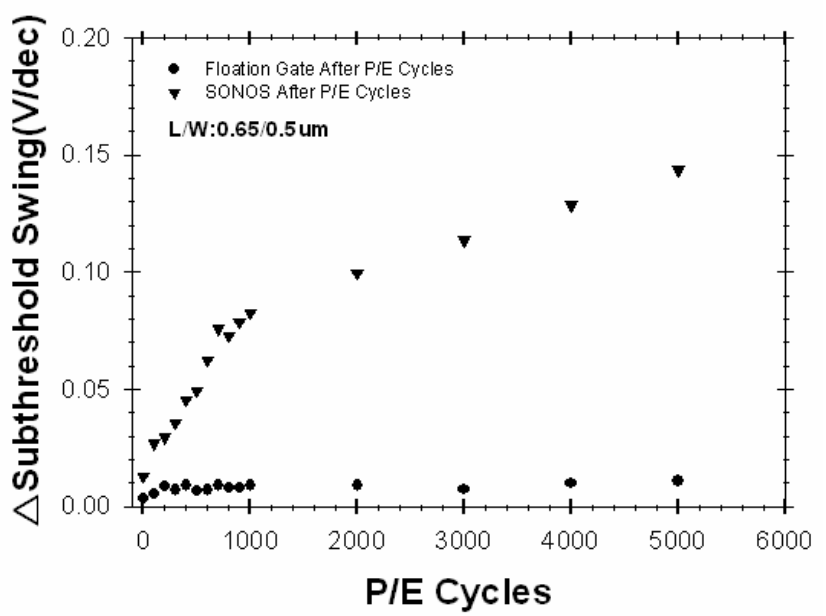


(a)

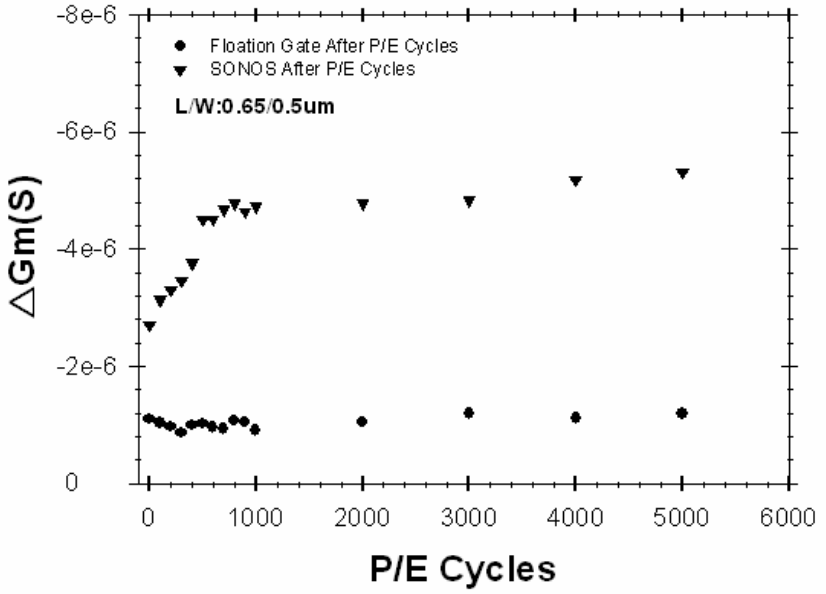


(b)

Fig 3.20 Subthreshold characteristics and transconductances of an n-channel SONOS memory device with length/width = 0.65μm /0.5μm. (a) Erasing and (b) programming operations.

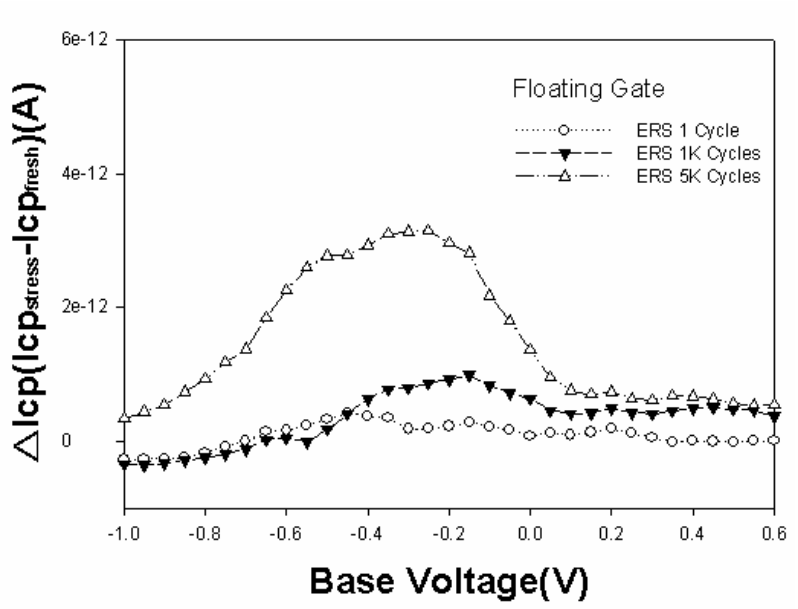


(a)

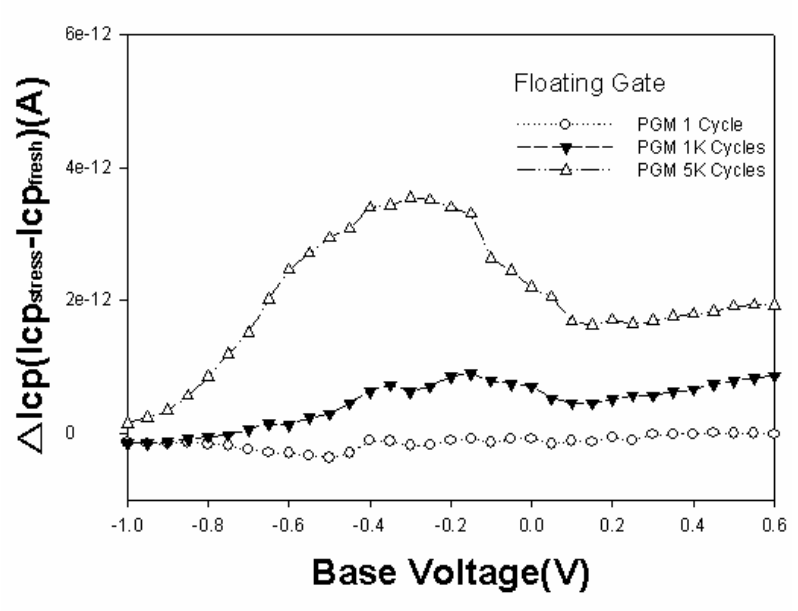


(b)

Fig 3.21 Degradation of (a) Subthreshold swing and (b) transconductance of the FG and the SONOS memory devices as a function of P/E cycles.

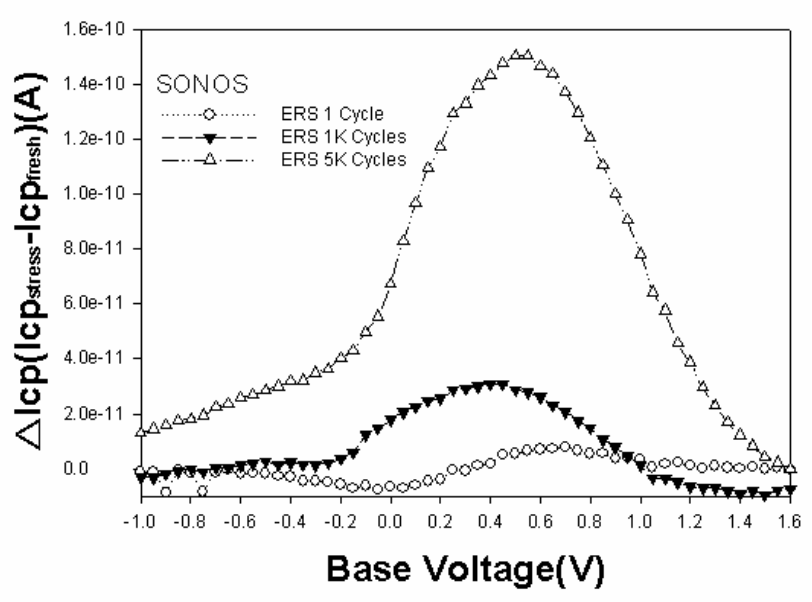


(a)

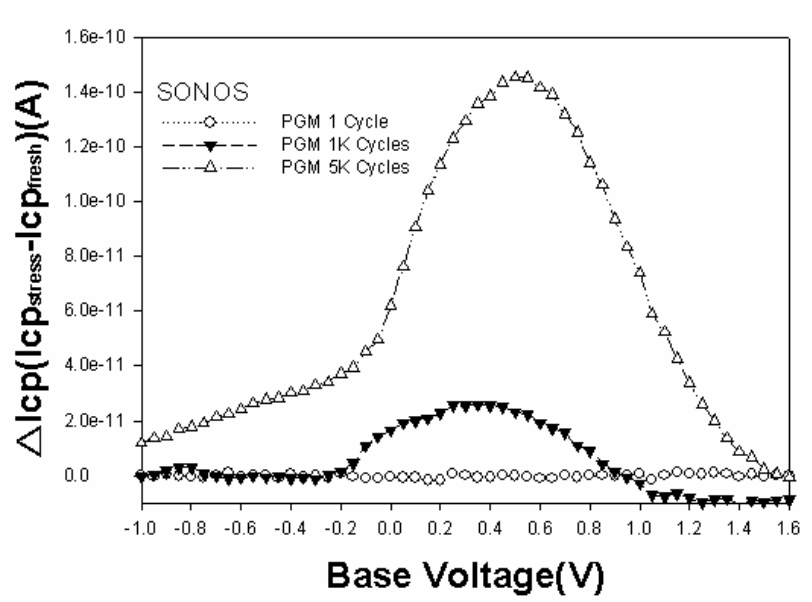


(b)

Fig 3.22 Increase in charge pumping current (△Icp) after 1000 and 5000 P/E cycles for an FG device. The measurements were performed under fixed amplitude of 1.5V and frequency of 1MHz. (a) Erasing state. (b) Programming state.

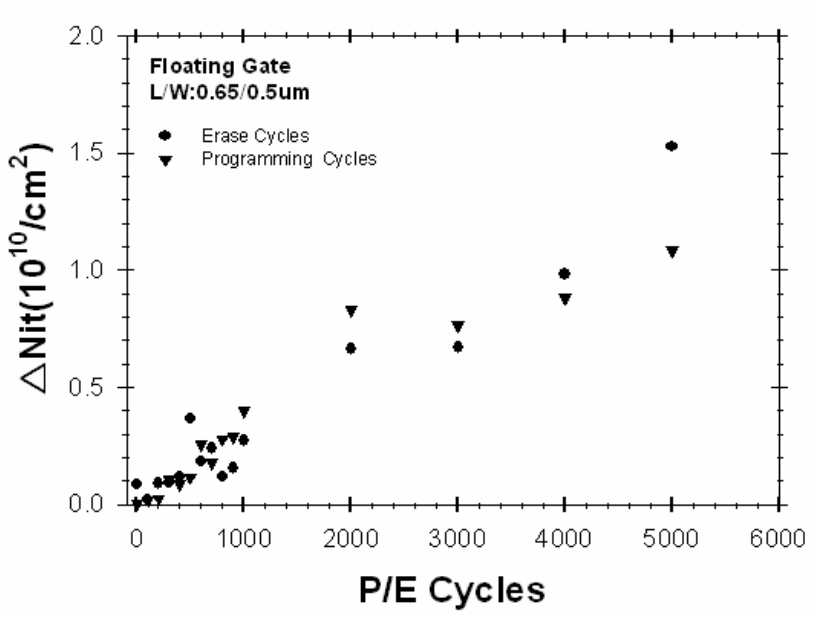


(a)

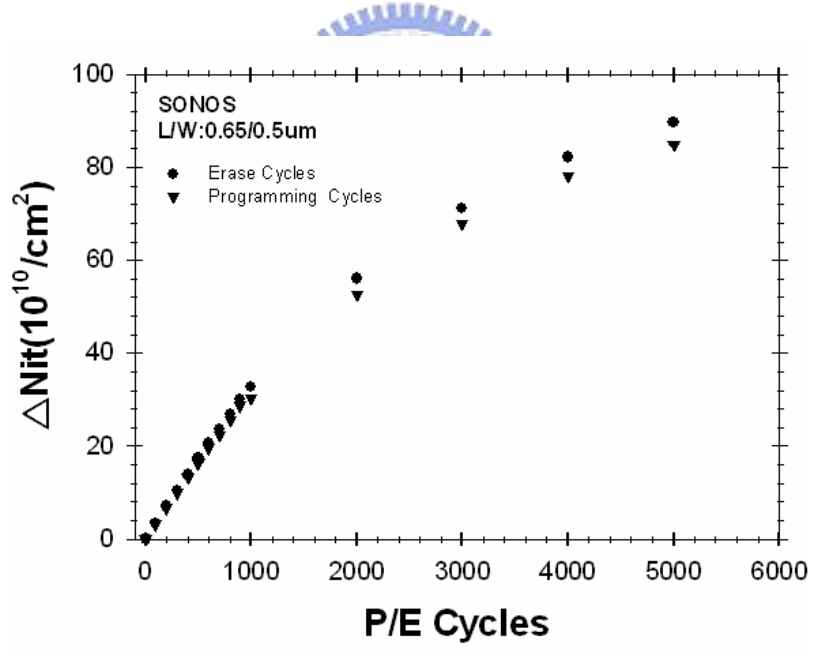


(b)

Fig 3.23 Increase in charge pumping current (△Icp) after 1000 and 5000 P/E cycles for an SONOS device. The measurements were performed under fixed amplitude of 1.5V and frequency of 1MHz. (a) Erasing states. (b) Programming states.



(a)



(b)

Fig 3.24 Interface state generation after P/E cycling of both flash memory devices with channel length/width = 0.65μm /0.5μm. (a) The FG device (b) The SONOS device.

作者簡歷

姓名：林欣逸　Hsin-I Lin

姓別：男

生日：西元 1975 年 4 月 29 日

籍貫：台灣省 高雄縣

現址：高雄縣路竹鄉中和街 310 號

學歷：南台工商專校計算機工程組　1990.9 ~ 1995.6

大葉大學電機工程學系　1995.9 ~ 1998.6

國立交通大學電機與資訊學院專班電子與光電組　2005.9 ~ 2007.9

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