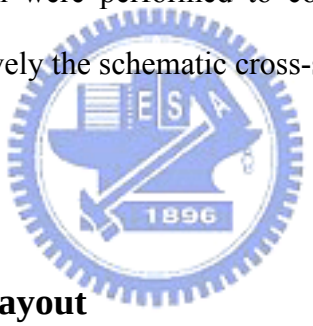
Chapter 3

Implementation of Ring Oscillator with LTPS TFTs

3-1. Device Fabrication

The process flow of fabricating LTPS TFTs is described as follows. Firstly, the buffer oxide and a-Si:H films were deposited on glass substrates; then XeCl excimer laser was used to crystallize the a-Si:H film, followed by poly-Si active area definition. Subsequently, a gate insulator was deposited. Then, the metal gate formation and source/drain doping were performed. A lightly doped drain (LDD) structure was used on the n-type TFTs. Dopant activation and hydrogenation were carried out after interlayer deposition. Finally, contact holes formation and metallization were performed to complete the fabrication work. The Fig.3-1 and Fig.3-2 show respectively the schematic cross-section structure of the N-type TFT and P-type TFT.



3-2. Testkey Design and Layout

The ring oscillator testkey is composed of two blocks: ring oscillator and buffer as shown on Fig.3-3. The ring oscillator consists of an odd number of inverters in a chain, in this case 105 stages. A two input nand gate X1 with one of the inputs connected to an enable signal is equivalent to an inverter in the chain. If the RO is enabled, the nand gate works just as any other inverter. The chain inverter gate X2 and X3 are served as 74 chain inverters with identical aspect ratio. The buffer block has four invert gates X4 to X7 and its supply power is independent from ring oscillator in order to measure the input current exactly consumed by ring oscillator. The main objective of the buffer is to enlarge the driving ability of ring oscillator output signal so that the probe loading has little influence on measurement result.

The testkey layout is composed of three blocks: ring oscillator buffer and probing pad as shown on Fig.3-4 to Fig.3-6 respectively. The layout of ring oscillator is folded by half symmetrically in order to keep one sampling testkey being in short range. There are six probing pads in one sampling testkey which are XVDD, VSS, IN, OUT, VVDD, and VVSS. XVDD and VSS serve as supply power and ground respectively for ring oscillator, while VVDD and VVSS are power and ground respectively for buffer. IN and OUT are enable and output signal for ring oscillator respectively. The width and pitch for probing pad are 200um and 100um respectively owing to matching the request from the probe card.

3-3. Measurement and Device Parameter Extraction Method

3-3-1. Measurement Method

The block diagram for measurement method is shown on Fig.3-7. There are four fundamental components: DUT (device under test equivalent to ring oscillator test-key here), power supply, probe card and oscilloscope during our measurement. The procedure for measurement is described as below:

(1) The DUT is placed on stage. Insert probe card into the probe card holder which will set the probe card position just above the DUT. The stage can adjust up and down to make the connection and disconnection between them.

(2) The IN, enable signal of ring oscillator, is initially set to “low” (ground level).

(3) Supply the XVDD and VVDD from power supply, both values is set to 5V and 15V step by step.

(4) Switch the IN to “High”(5V or 15V), then measure the output frequency and input current from oscilloscope and current meter respectively.

(5) The Id-Vg characteristics of nearest N-type and P-type TFT are also measured and recorded.

Since the measurement is done, our next step is to extract the device parameter from the N-type and P-type TFT Id-Vg characteristic just measured.

3-3-2. Parameter Extraction

a. Determination of the threshold voltage

In most of the researches on TFT, the constant current method is widely-adopted to determine the threshold voltage (Vth). In this work, the threshold voltage is determined from this method, which extracts Vth from the gate voltage at the normalized drain current $I_N = I_D/(W_{eff}/L_{eff}) = 10$ nA for $V_D = 0.1$V.

b. Determination of the field-effect mobility

The field effect mobility (μ_{FE}) is derived from the transconductance gm at low drain voltage. Since the transfer characteristics of poly-Si TFTs are similar to those of conventional MOSFETs, the first order I-V relation in the bulk Si. can be applied to the poly-Si TFTs, which can be expressed as

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}[(V_G - V_{th})V_D - \frac{1}{2}V_D{}^2] \quad (3\text{-}1)$$

Where

C_{ox} is the gate oxide capacitance per unit area,

W is channel width,

L is channel length,

V_{th} is the threshold voltage.

If the drain voltage V_D is much smaller compared with V_G-V_{th}, then the drain current can be approximated as:

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}(V_G - V_{TH})V_D \quad (3\text{-}2)$$

And the transconductance is defined as:

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=const.} = \frac{WC_{ox}\mu_{FE}}{L}V_D$$

Therefore, the field effect mobility can be expressed as:

$$\mu_{FE} = \frac{L}{C_{ox}WV_D}\mathrm{g_m} \qquad (3\text{-}3)$$

In this thesis, we extract the field-effect mobility by taking the maximum value of the g_m into (3-2) when $V_D = 0.1V$.

3-4. Results

We will begin this section with ring oscillator delay time and its direct relationship with device parameter. And, finally, we conclude this section with the analysis of measured delay time of ring oscillator.

The output frequency of ring oscillator has direct relationship with the inverter delay time which can be expressed as:

$$f_{RO}=1/(2NTd) \qquad (3\text{-}4)$$

where f_{RO} is the ring oscillator output frequency, N is number of stage, Td is inverter delay time. We can also refer to Fig. 3-8 to look more insight to this formula. As the figure shown, we take a three stages ring oscillator for example. And every composed inverter of ring oscillator has a delay time Td. Let us now assume the circuit begins with Vx = Vdd. Under this condition, Vy = 0 and Vz = Vdd. Thus, when the circuit is released, Vx begins to fall to zero (because the first inverter senses a high input), forcing Vy to rise to Vdd after one inverter delay, Td, and Vz to fall to zero after another inverter delay. The circuit therefore oscillates with a delay of Td between consecutive node voltages, yielding a period of 6Td.

Finally, we conclude with the output frequency of a three stages ring oscillator is 1/(6Td) which matches with our formula.

It is, then, important to derive the delay time expression of inverter. Therefore, we fall back to the simplified switch model of the inverter introduced in Fig. 3-8 to derive a reasonable approximation of the propagation delay adequate for our analysis. The voltage dependencies of the "on" resistance and the load capacitor are addressed by replacing both by a constant linear element with a value averaged over the interval of interest. Deriving the propagation delay of the resulting circuit is now straightforward. It is nothing more than the analysis of a first-order linear RC network. As we known, the propagation delay of such a network, excited by a voltage step, is proportional to the time constant of the network, formed by pull-down and load capacitance. Hence,

$$t_{pHL} = \ln(2)ReqnCL = 0.69ReqnCL \quad (3\text{-}5)$$

where CL is load capacitance of inverter, Reqn is the equivalent "on" resistance of N channel thin film transistor over the interval of interest. Similarly, we can obtain the propagation delay for the low-to-high transition. We write

$$t_{pLH} = \ln(2)ReqpCL = 0.69ReqpCL \quad (3\text{-}6)$$

where Reqp is the equivalent "on" resistance of P channel thin film transistor over the interval of interest. The overall propagation delay of the inverter is defined as the average of the two values:

$$Td = 0.69\ CL\ (Reqn+Reqp)/2 \quad (3\text{-}7)$$

where CL is load capacitance of inverter, Reqn and Reqp is the "on" resistance of N channel and P channel thin film transistor respectively. The TFT "on" resistance can be expressed as the below equation:

$$Req=1/\mu_{n,p}C_{ox}(W/L)(V_{GS}-|V_{TH(n,p)}|)= 1/\mu_{n,p}C_{ox}(W/L)OD_{n,p} \quad (3\text{-}8)$$

where $\mu_{n,p}$ is mobility of electron or hole, C_{ox} is the gate oxide capacitance per unit area, W is effective channel width, L is effective channel length, $(V_{GS}-|V_{TH(n,p)}|)$ is the "overdrive voltage" of N channel and P channel thin film transistor respectively and we replace it with

$OD_{n,p}$ for simplify. With the aid of equation 3-8, we conclude our discussion with delay time of ring oscillator is inverse proportion to $\mu_{n,p}$ and $OD_{n,p}$.

With the concept of delay time and its direct relationship with device parameter, we will begin the analysis with delay time histogram. And, by next, we will do further analysis with error bar char of both ring oscillator power consumption and delay time. Finally, we will conclude our discussion with the relationship between delay time, operating voltage and number of stages. Fig. 3-10 shows the measured ring oscillator delay time histogram chart. It is arranged with respect to operating voltage by columns and number of stages by rows. At the first glance to the histogram chart, we find the shape of distribution is almost normal type in all cases. So we can proceed with our analysis by using statistical parameter such as average and standard deviation.

Error bar graph is a good tool to shows the trend of average and standard deviation between several conditions. Fig. 3-11 shows ring oscillator power consumption error bar chart which points out that the average and standard deviation of power are independent of the stage number of ring oscillator. Furthermore, it tells us that the average and standard deviation of power are proportional to operating voltage. In order to check the validity of our measurement, we will find out the correlation between measurement result and theory.

To begin our analysis on ring oscillator power consumption measurement result, one thing we should keep in mind is that the ring oscillator is composed of chain inverters. And inverter hardly consumes any “DC” power. The “AC” power can be expressed by below formula:

$$P_{AC} = C_L Vdd^2 f \qquad (3\text{-}9)$$

where C_L represents the load capacitance, Vdd is operating voltage and f stands for operating voltage. With the aid of power consumption equation (3-9), we can make sure that the average of power is linear relative to square of supply voltage. We show our analysis result on

figure 3-12 which matches with the prediction of theory and confirms the validity of our measurement.

Similarly, the C_L and Vdd of equation (3-8) are assumed to be constant. And we will find out that the variation of frequency will have direct influence on power consumption. In other words, the standard deviation of frequency will have linear relationship with power distribution range. Our analysis result is presented on figure 3-13 which verifies the correctness of our measurement.

Fig. 3-14 is the error bar chart of ring oscillator delay time when operating voltage is 5V, 10V and 15V respectively. Based on the results shown on fig. 3-14, we have two conclusions. The first conclusion is the average and standard deviation of delay time is independent of the stage number of ring oscillator. The second conclusion is the average and standard deviation of delay time is inversely proportional to operating voltage.

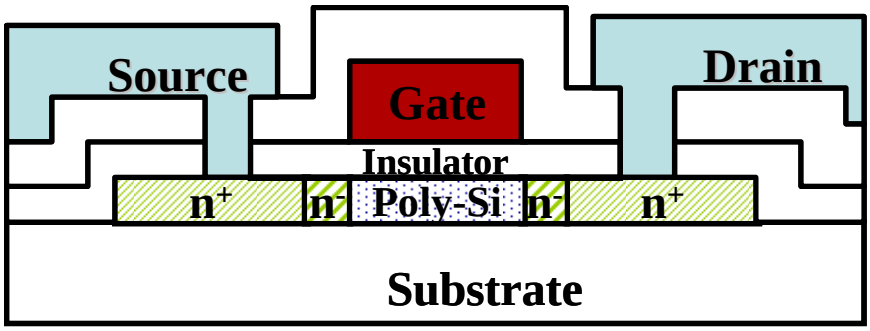


Fig. 3-1 The schematic cross-section structure of the n-type TFT

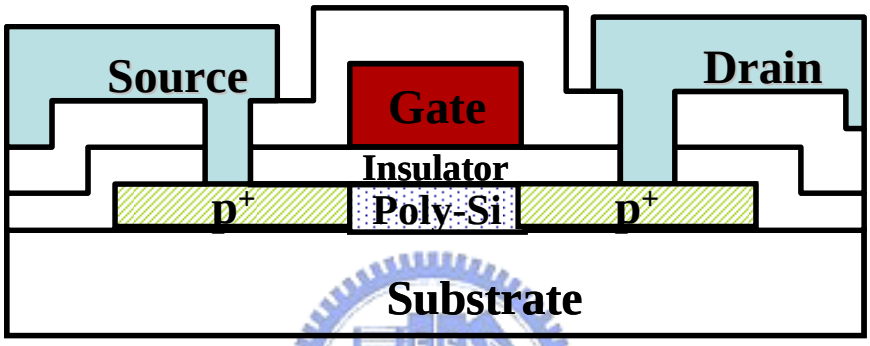


Fig. 3-2 The schematic cross-section structure of the p-type TFT

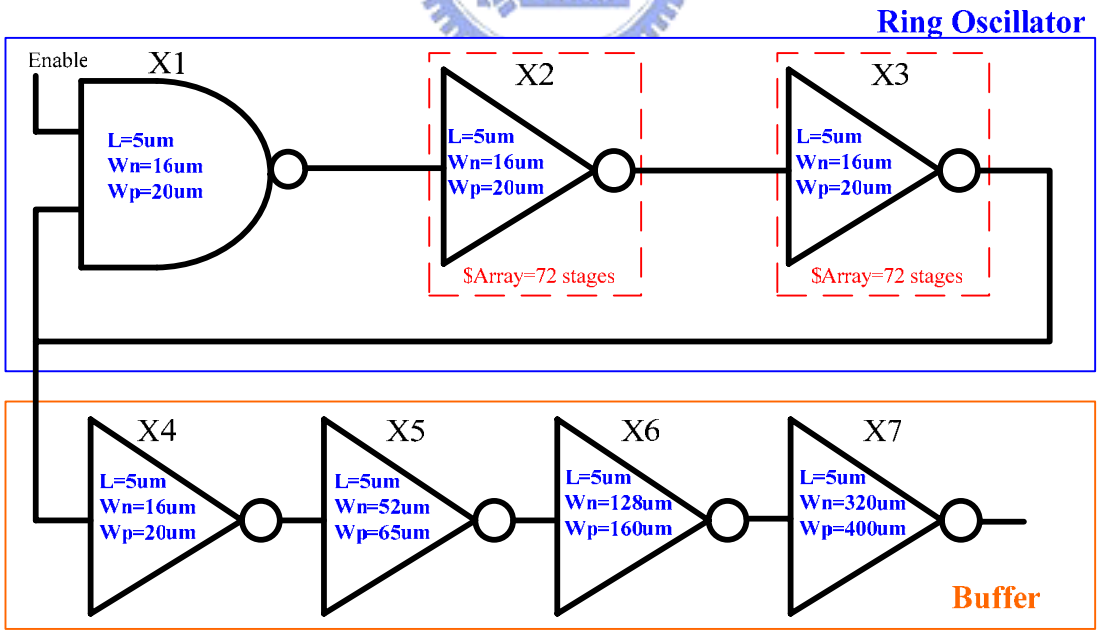


Fig. 3-3 The schematic of ring oscillator testkey

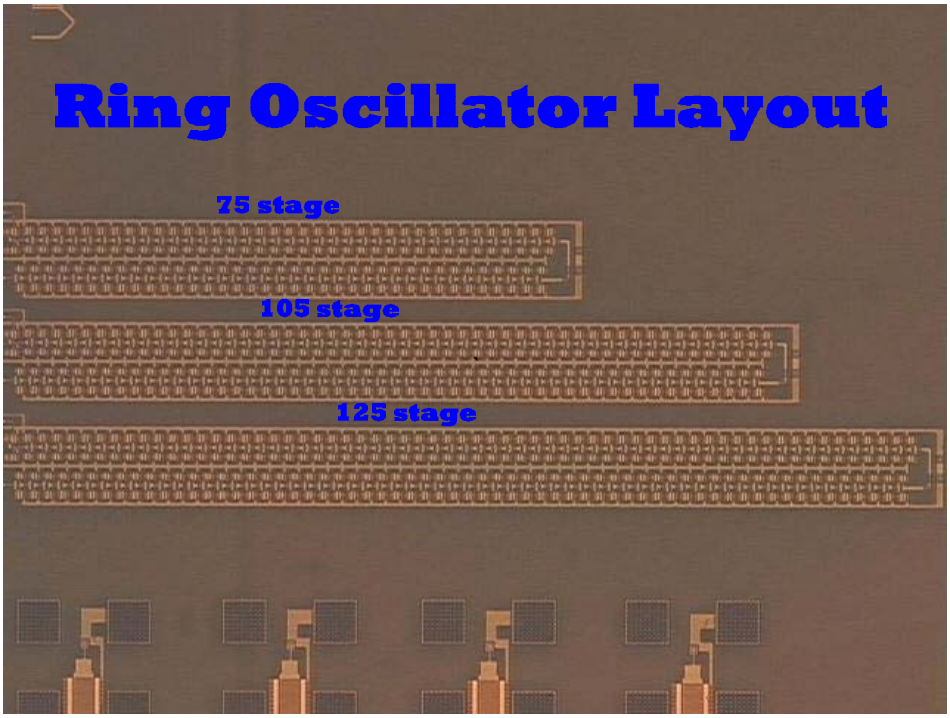


Fig. 3-4 The layout picture of ring oscillator testkey

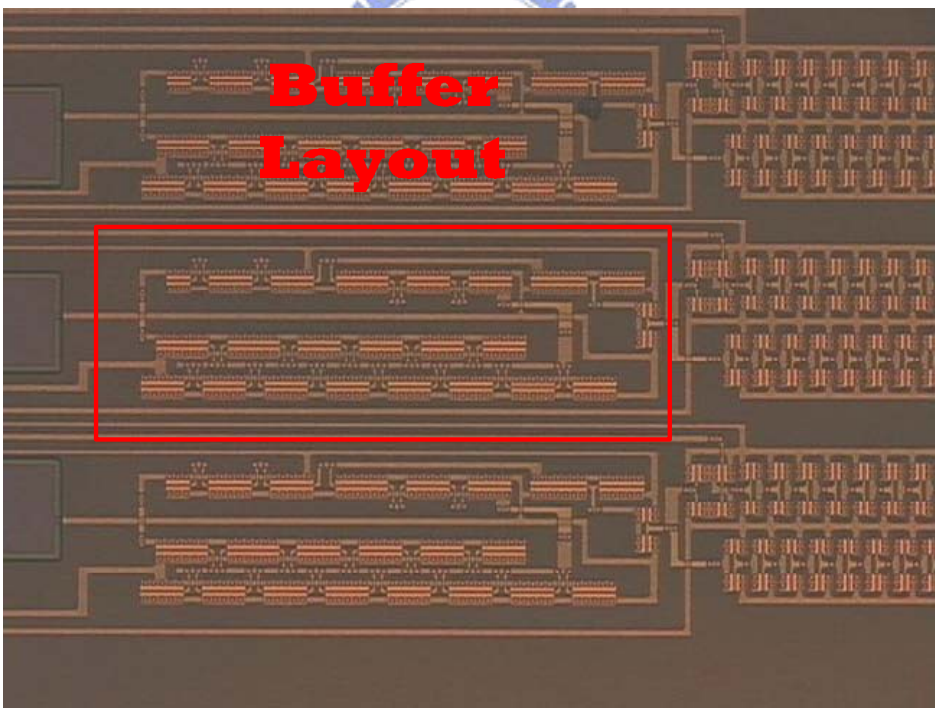


Fig. 3-5 The layout picture of buffer block in ring oscillator testkey

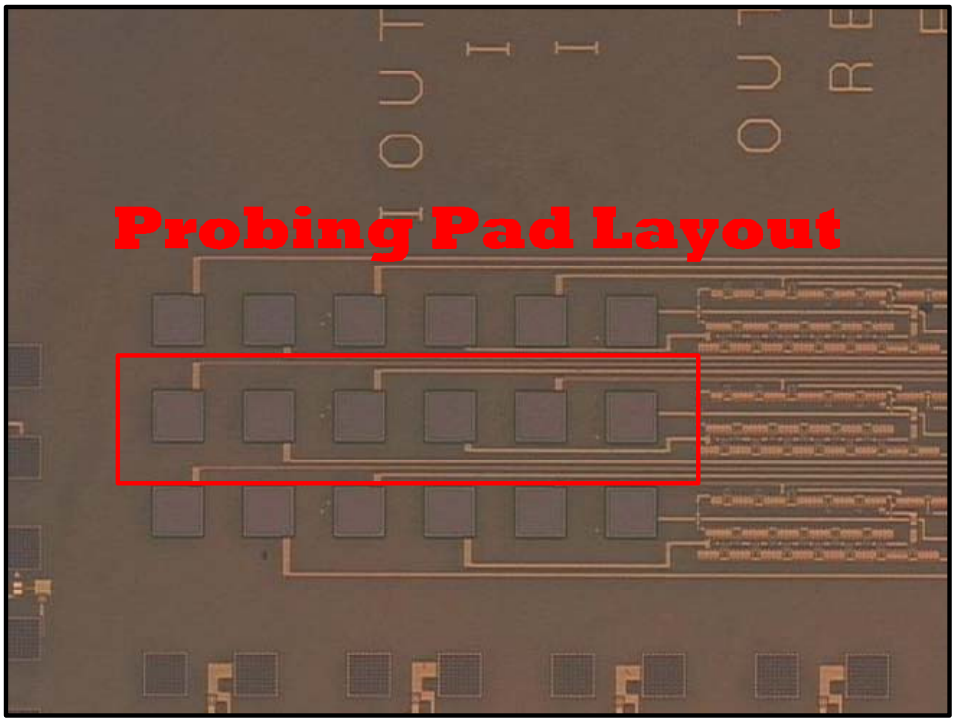


Fig. 3-6 The layout picture of probing pad block in ring oscillator testkey

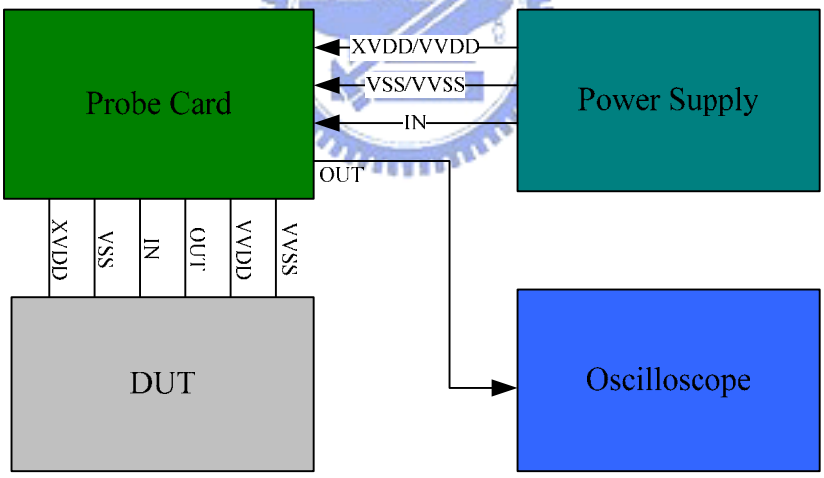


Fig. 3-7 The block diagram of measurement method for ring oscillator testkey

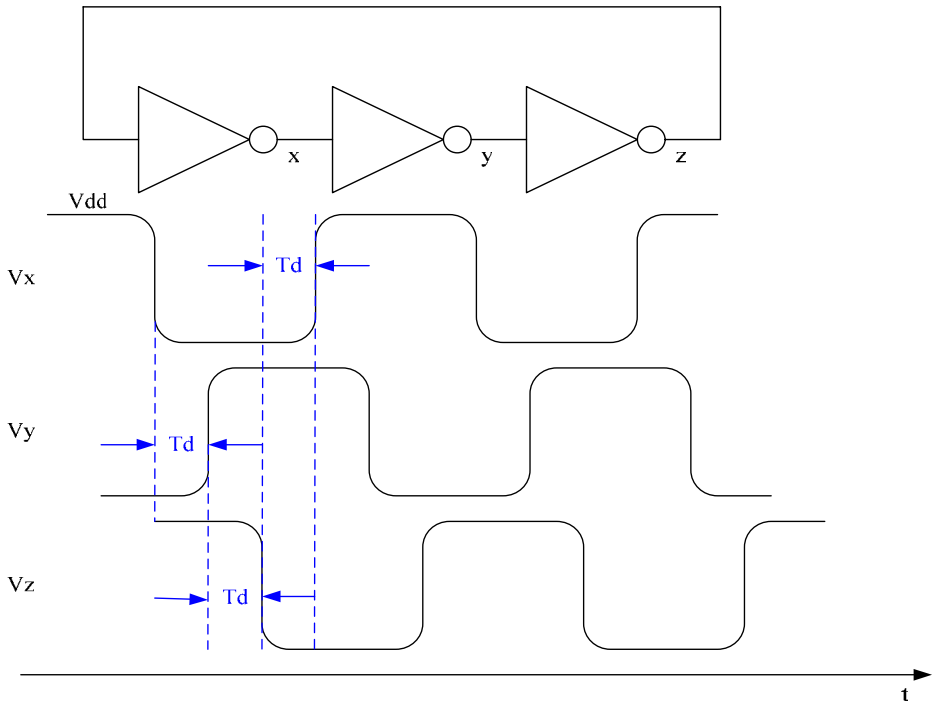


Fig. 3-8 The relationship between output frequency of three stages ring oscillator and inverter delay time Td

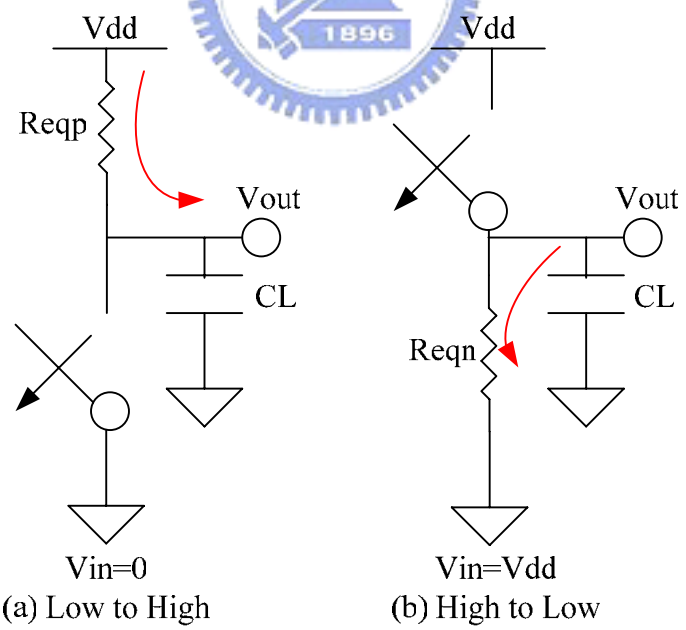


Fig. 3-9 Switch model of dynamic behavior of static inverter

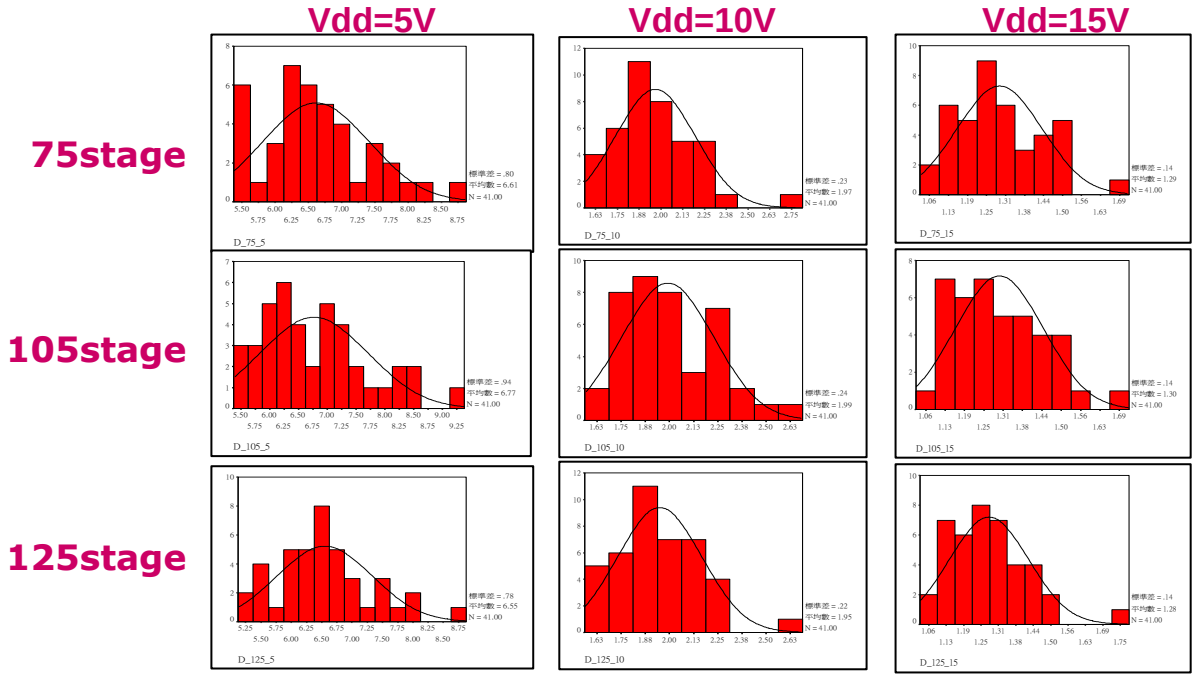


Fig. 3-10 Ring oscillator delay time histogram chart

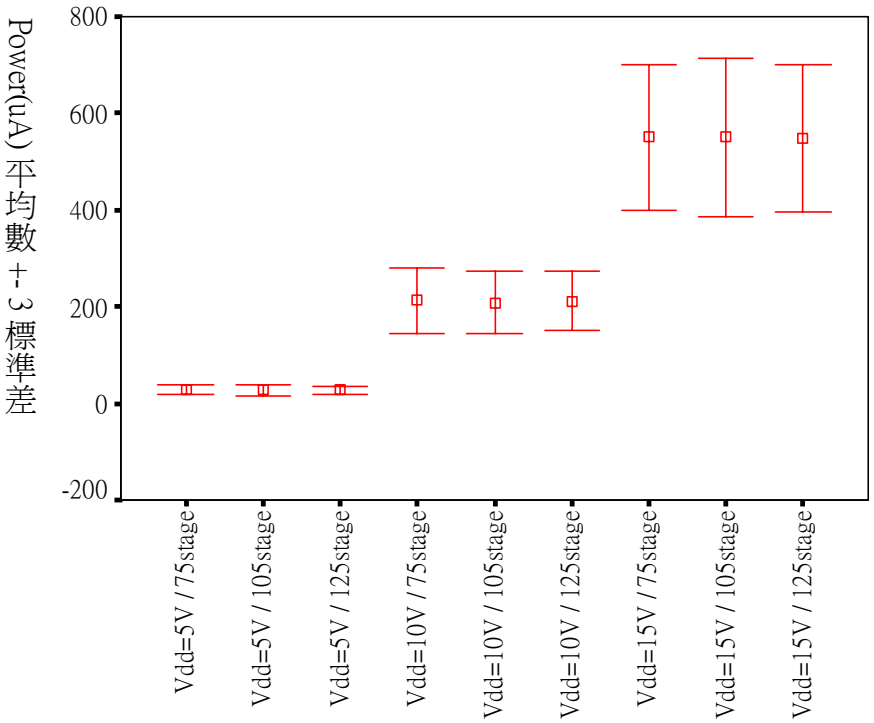


Fig. 3-11 ring oscillator power consumption error bar chart

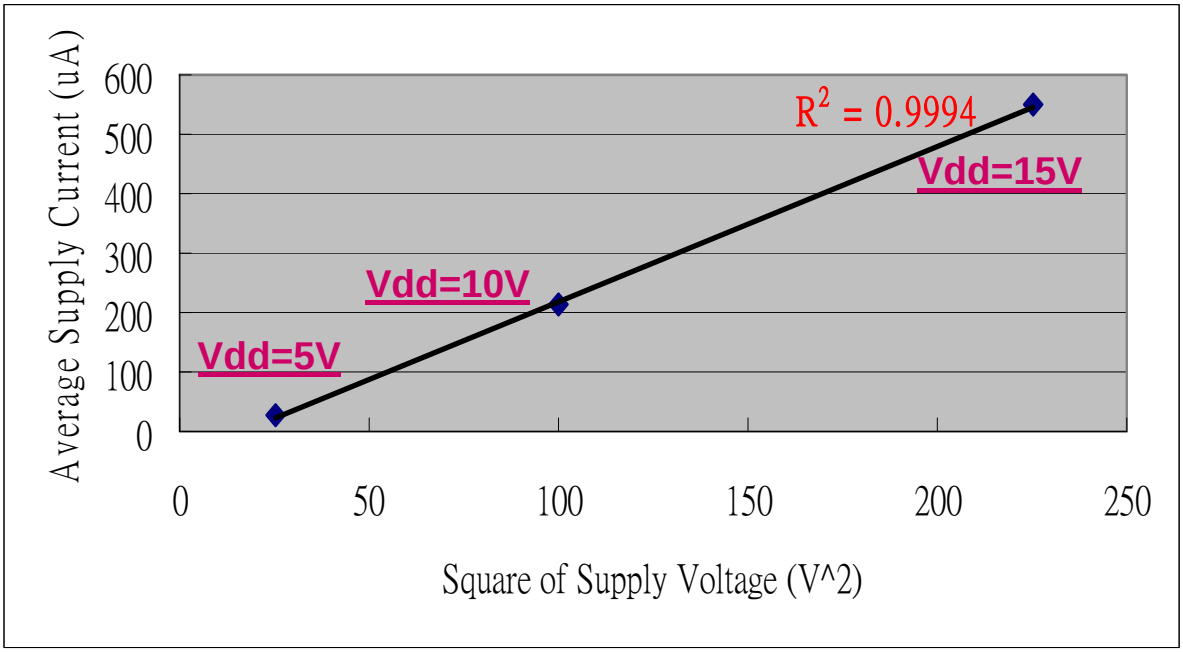


Fig. 3-12 the distribution chart of ring oscillator supply current and square of supply voltage

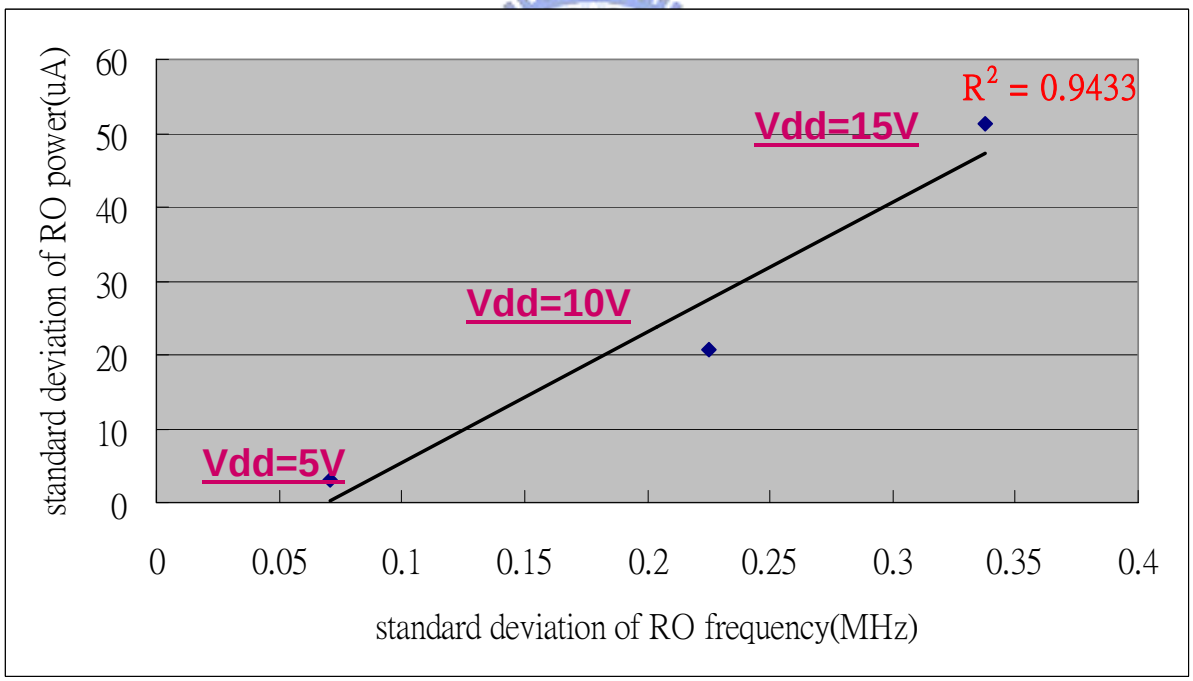


Fig. 3-13 the distribution chart for standard deviation of RO power and frequency

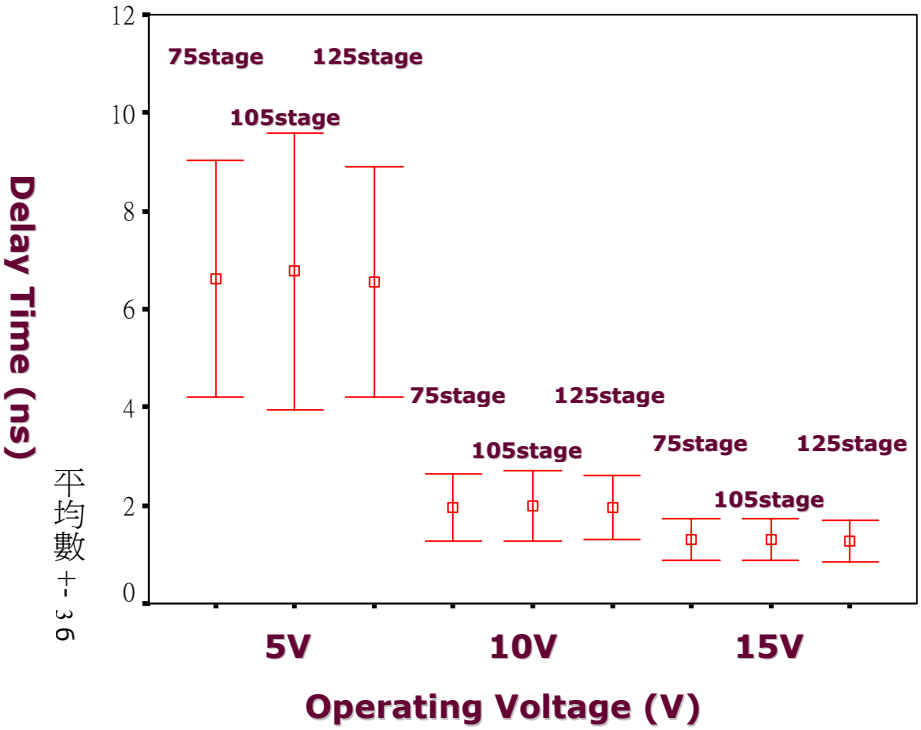


Fig. 3-14 Ring oscillator delay time error bar chart

Chapter 4

Device Variation Effects on Ring Oscillator

4-1. Microscopic Device Variation Effect on Ring Oscillator

In this section, we will begin our discussion with the plan of experiment. And then, based on the previous study result introduced in section 2-3, we will do simulation to predict the variation range of microscopic device variation on ring oscillator. Finally, we conclude this section with the consistence between measurement and simulation results.

As mentioned in the beginning of chapter 2, the microscopic device variation can be observed in short range. It means if we want to make sure the microscopic device variation effect on ring oscillator, we should consider the variation within a ring oscillator but not the mutual variation among them. We begin our experiment with the measurement on the output frequency of a set of ring oscillators, and then we extract the device parameters from only one test-key right beside each ring oscillator. Finally, we proceed with the simulation by using the device parameters just being extracted out. The question arises here is that does only one measured test-key device can represent the whole ring oscillator composed of hundreds of LTPS TFT? In fact, the difference between measured and simulated output frequency of ring oscillator is equivalent to microscopic device variation. And our goal in this section is to prove this difference will be within the predicted range.

We will then put our emphasis on how to define the variation range of microscopic device variation. Since we don't know where the only one measured device parameter will locate in the distribution range, we define the variation range by assuming 99% of distribution range is included. Based on previous study result mention in chapter 2, we can predict device parameter error (Δ) at the 0.5% and 99.5% of the distribution shown as below table 4-1, respectively.

	0.50%	99.50%
ΔMun (cm2/Vs)	-10.223	9.723
ΔVthn (V)	-0.147	0.142
ΔMup (cm2/Vs)	-9.216	8.716
ΔVthp (V)	-0.155	0.150

Table 4-1 Predicted ΔMun, ΔVthn, ΔMup and ΔVthp at the 0.5% and 99.5% of the distribution respectively

The simulation will be done by three steps called sim_typ, sim_ff and sim_ss. The sim_typ is simulated with the measured device parameter directly. Sim_ff is simulated with the possibly high mobility and low threshold voltages of both N-TFT and P-TFT at 99.5% and 0.5% of the distribution respectively. On the contrast, sim_ss is with the possibly low and high mobility and threshold voltages at 0.5% and 99.5% of the distribution respectively. Fig 4-1 to 4-3 show the simulation results of microscopic device variation effect on 105 stage ring oscillator when operating voltage is 5V, 10V and 15V, respectively. In these figures, the data are sorted by measured frequency. We will demonstrate the simulation results by separating it into three cases. Firstly, if the measured value closes to sim_typ, it represents the measured device parameter closes to the average of whole devices in corresponding ring oscillator. Secondly, if the measured value closes to sim_ff, it means the measured device parameter performs much worst than the average. Finally, if the measured value closes to sim_ss, it corresponds to the measured device parameter overestimates the circuit performance. As a result, the measured values are all within the range between overestimation and underestimation.

Since the 75, 105 and 125 stage ring oscillators are placed in a short range, the difference of measured delay time between them is also equivalent to microscopic device variation. Fig. 4-4 to Fig.4-6 show the measured microscopic device variation effect on delay time with respect to operating voltage is 5V, 10V and 15V, respectively. In these figures, the data are sorted by the delay time of 75 stage ring oscillator. Despite of a few abnormal high variation data, almost all the measured data is consistent with our simulation prediction.

Finally, we conclude this section with the answer of the question mentioned in the beginning of this section "Can only one measured test-key device parameter represent the whole ring oscillator composed of hundreds of LTPS TFT". Our reply is "Not exactly, but it will very close to the actual performance". Furthermore, we also define how close it will be. Obviously, the reason why it can't represent the whole circuit is owing to the microscopic device variation effect.

4-2. Macroscopic Device Variation Effect on Ring Oscillator

As mentioned in chapter 1, there are two major types of simulation, called "Worst-Case" and "Monte-Carlo" when macroscopic device variation effect on ring oscillator is considered. In this section, we begin with quick review of previous study results on these two types of simulation. And then we will follow its conclusion and run Monte-Carlo simulation to predict macroscopic device variation effect on ring oscillator performance. We will verify the simulation by comparing the average and standard deviation of delay time between the simulated and measured results. The comparison shows the standard deviation of simulated delay time is smaller than the measured value. We will then point out two possibilities leads to the poor prediction. Firstly, we will modify the simulation by including microscopic device variation and check its effect on standard deviation of delay time. Secondly, we will modify the simulation by taking the collocation of device parameters into

consideration. Finally, we will share our improvement on simulation method by pointing out the worst case condition of Monte Carlo method. Furthermore, we also prove there is no need to consider the microscopic device variation on LTPS TFT digital circuits.

From previous study [8], fig. 4-7 shows a distribution of gate delay calculated by the Monte Carlo analysis with 1000 SPICE simulations. Two worst-case values calculated by Worst-Case and Monte Carlo analysis are indicated as “corner” and “MC”, respectively. Previous study pointed out the worst-case rang of the Worst-Case simulation is 19% wider than the range of the Monte Carlo analysis.

The behavior of macroscopic device variation effect on ring oscillator, as mentioned in the beginning of chapter 2, is common variation. So we assume the device parameter distribution is Gaussian type generated from the measured device parameter average and standard deviation as below table 4-2.

	Mun (cm2/Vs)	**Mup (cm2/Vs)**	**Vthp (V)**	**Vthn (V)**
Average	**72.47**	**117.4**	**-1.88**	**1.66**
std dev	**6.70**	**7.91**	**0.17**	**0.11**

Table 4-2 the measured device parameter average and standard deviation from the uniformly distributed sample device on the same glass substrate

At first, we assume the correlation among device parameters is independent. Here, we also neglect the microscopic device variation effect which means the whole device inside the corresponding ring oscillator will have identical device parameters. When simulation is done, we can plot the histogram as fig 4-8. By compare with the measurement result shown as fig. 3-10, we find out that the average of simulation is close to measurement result owing to the device parameter of simulation is generated from the same measured database. However

the standard deviation of simulation is much smaller than measurement result which will lead to wrong estimation on circuit performance variation range and low production yield.

We will then modify the simulation by including microscopic device variation and check its effect on standard deviation of delay time. Based on the previous study result introduced in section 2-3 again, the device parameter error(Δ) can be generated. We simply add the device parameter error(Δ) into every device inside the corresponding ring oscillators and then run simulation again. The simulation results are shown by plotting the histogram of delay time as fig 4-9. By compare with the simulation results shown as fig 4-8 which do not consider the microscopic device variation effect, the standard deviation with microscopic device variation will be slightly smaller. This tells us the truth that the microscopic device variation has little influence on the long range ring oscillator simulation result. Furthermore, we also find out the dominator factor of ring oscillator circuit performance is the average of whole device parameters inside it. In other words, the corner of device parameter will not be the bottleneck of ring circuit performance. Besides, the comparison of variation level between microscopic and macroscopic device variation will be meaningless owing to the microscopic effect will be averaged.

The correlation among the device parameters mentioned in table 4-2 will have direct influence on simulation result. For example, a high mobility collocates with small threshold voltage will lead to much higher ring oscillator output frequency than the average. This tells us a fact that if there exists a negative relation between mobility and threshold voltage, a much higher and lower ring oscillator output frequency than average will therefore occur which will rise up its standard deviation without doubt. Since a discussion about correlation among device parameters and its influence on standard deviation of ring oscillator frequency is presented, our next step is to define a clear representation for correlation among device parameters. Three types of correlation among device parameters are chosen out here as explanation examples shown as fig. 4-10. The first type being chosen out here is called as

“(N,N,P)”, where the “N” in first column denotes for the “negative relation” between Mun and Vthn, and the “N” in second column represents the “negative relation” between Mup and Vthp, and the “P” in last column sets the “positive relation” between Mun and Mup. The “(P,P,N)” type stands for the same definition with “(N,N,P)”, the only difference is the different values in three columns. And random just means random collocation with each other.

Since each column has three conditions, we will have total 27 types of simulation need to be checked. Fig 4-11 shows the error bar chart of 27 simulation results of macroscopic device variation effect. Here, the “(I,I,I)” is equivalent to the random type collocation. At the first glance on it, we find the collocation of device parameter will have direct influence on the standard deviation of delay time without doubt. And, obviously, the (N,N,P) collocation will be the worst case among all Monte Carlo simulation results. Besides, the (N,N,P) collocation is also the closest result with measured data. Meanwhile, we also find the average of delay time in all the 27 types of simulation results close to the measured value. This tells us the fact if the average of device parameters are determined, the average of delay time will also be determined. Figure 4-12 shows the histogram chart of (N,N,P) collocation for comparison with measured histogram shown on fig. 3-10. Finally, the concept here is a precise prediction for macroscopic device variation effect on LTPS TFT circuit performance is difficult owing to unknown correlation among device parameters. And from point view of production yield, which always have direct relationship with cost, we recommend using (N,N,P) type Monte Carlo simulation to predict the worst case distribution of circuit performance. Because the general (I,I,I) type Monte Carlo simulation will sometimes underestimate the macroscopic device variation effect on LTPS TFT circuit performance owing to the correlation among device parameters is not supposed to be random type.

4-3. Summary

This chapter has described the device variation effect on LTPS TFT circuit performance. On the microscopic device variation aspect, we predict its variation range and furthermore the consistence between measurement and simulation results is also presented. On the macroscopic device variation aspect, we confirm the microscopic variation is negligible owing to its effect on LTPS TFT circuit performance will be averaged. Furthermore, we demonstrate a new concept about the collocation of device parameters and its effect on standard deviation of delay time. After correlating the results between simulation and measurement, we conclude our discussion with using the worst case condition of Monte Carlo method to predict the variation range of circuit performance which will be beneficial on achieving a high yield design.

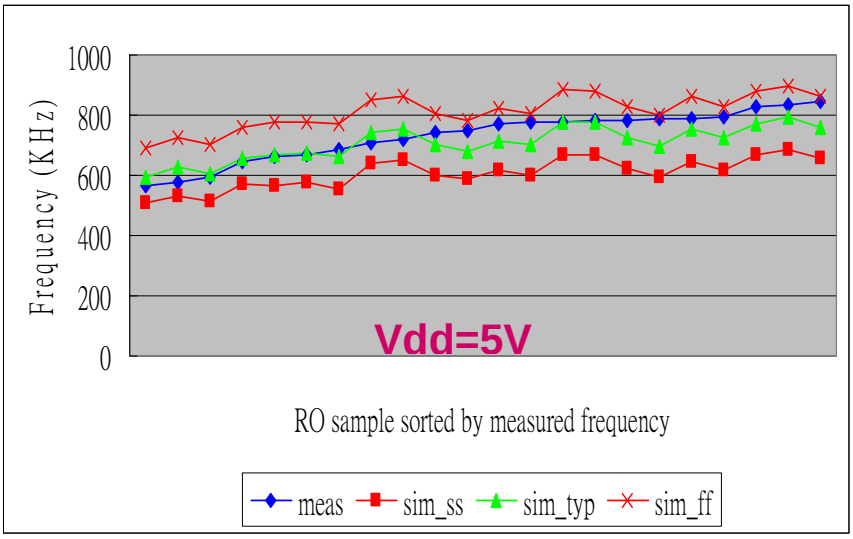


Fig. 4-1 Simulation result of microscopic device variation effect on ring oscillator when operation voltage is 5V

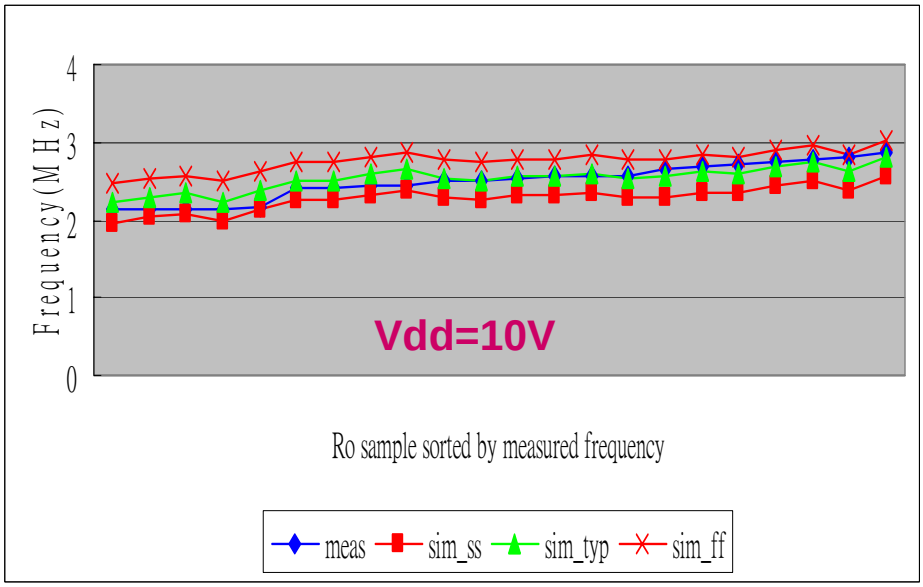


Fig. 4-2 Simulation result of microscopic device variation effect on ring oscillator when operation voltage is 10V

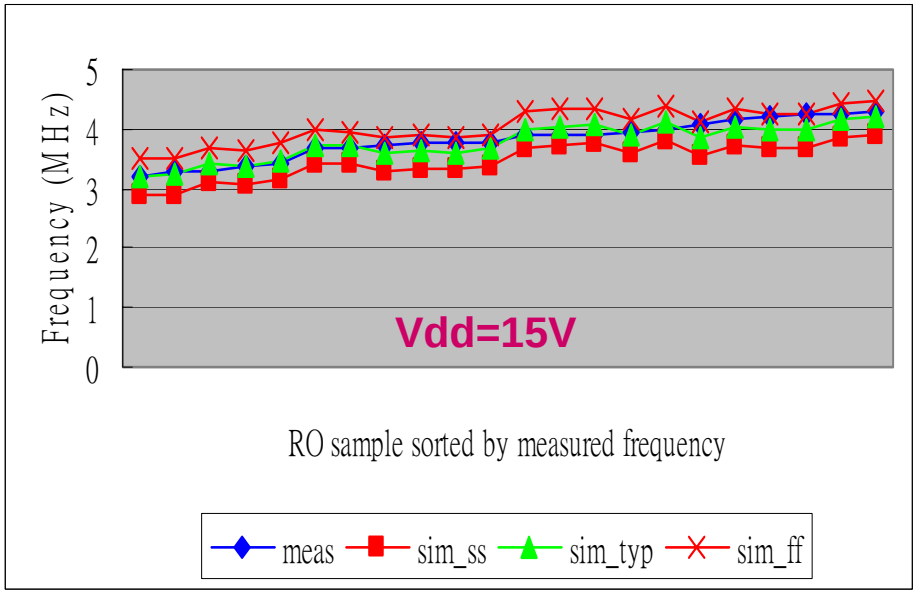


Fig. 4-3 Simulation result of microscopic device variation effect on ring oscillator when operation voltage is 15V

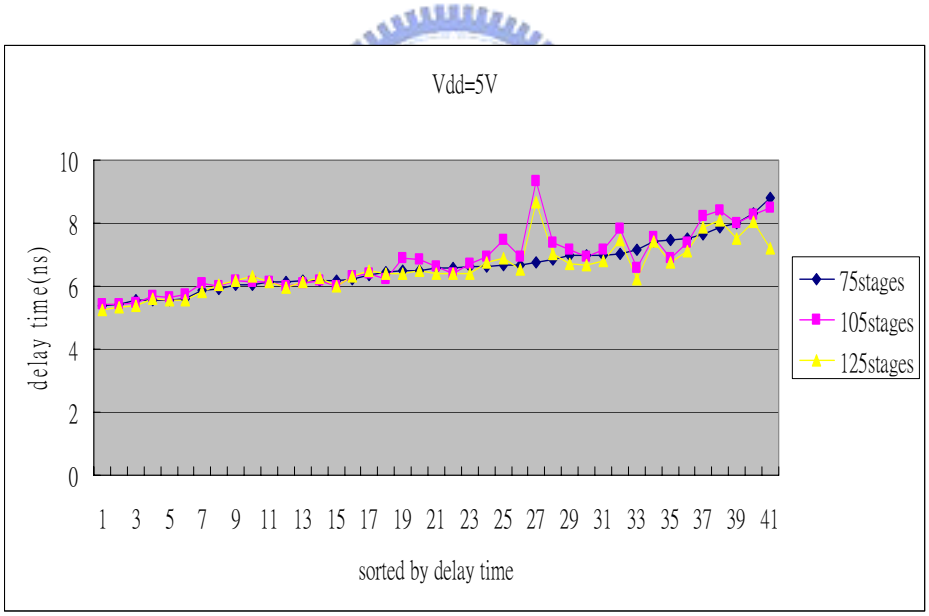


Fig. 4-4 the measured microscopic device variation effect on delay time with respect to operating voltage is 5V

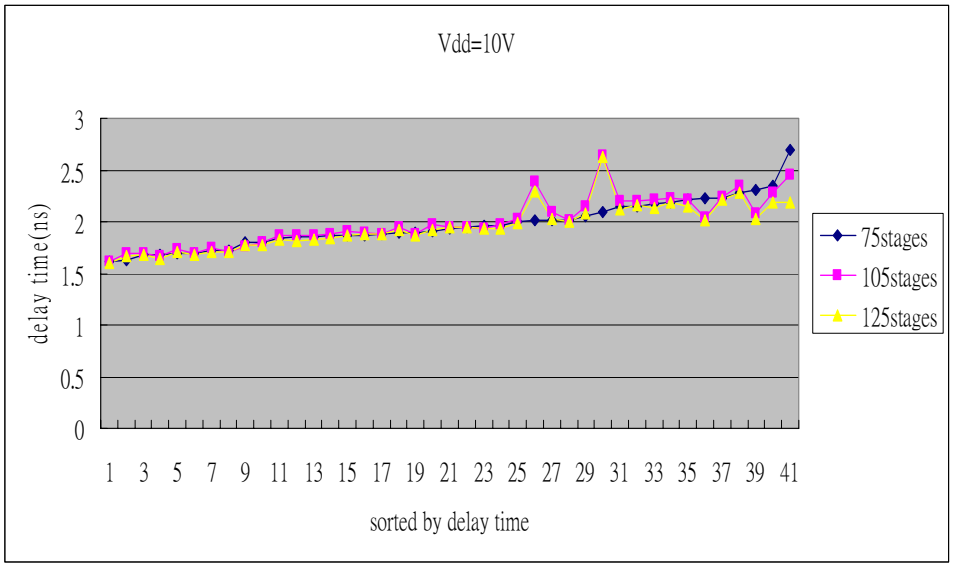


Fig. 4-5 the measured microscopic device variation effect on delay time with respect to operating voltage is 10V

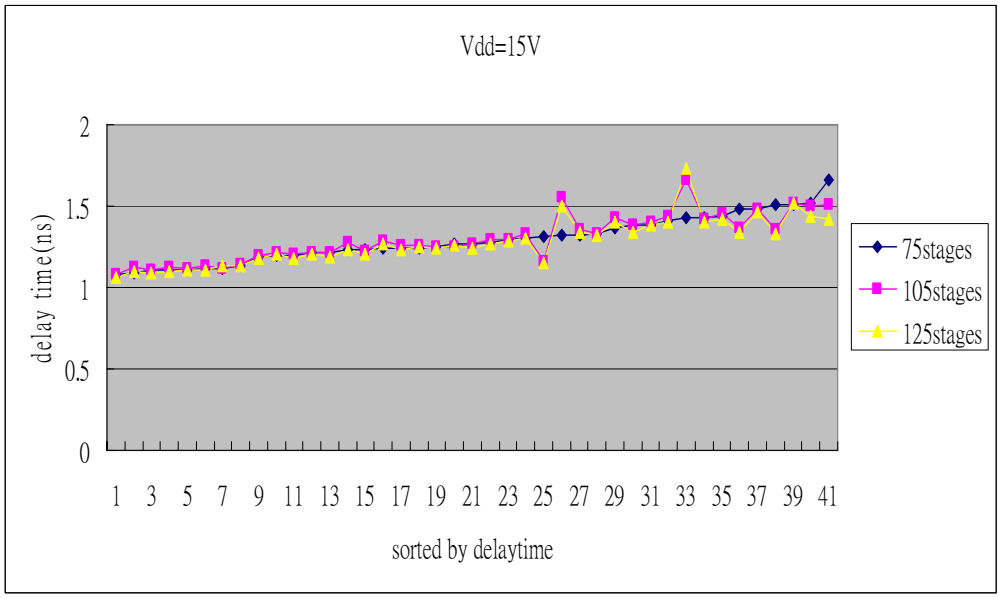


Fig. 4-6 the measured microscopic device variation effect on delay time with respect to operating voltage is 15V

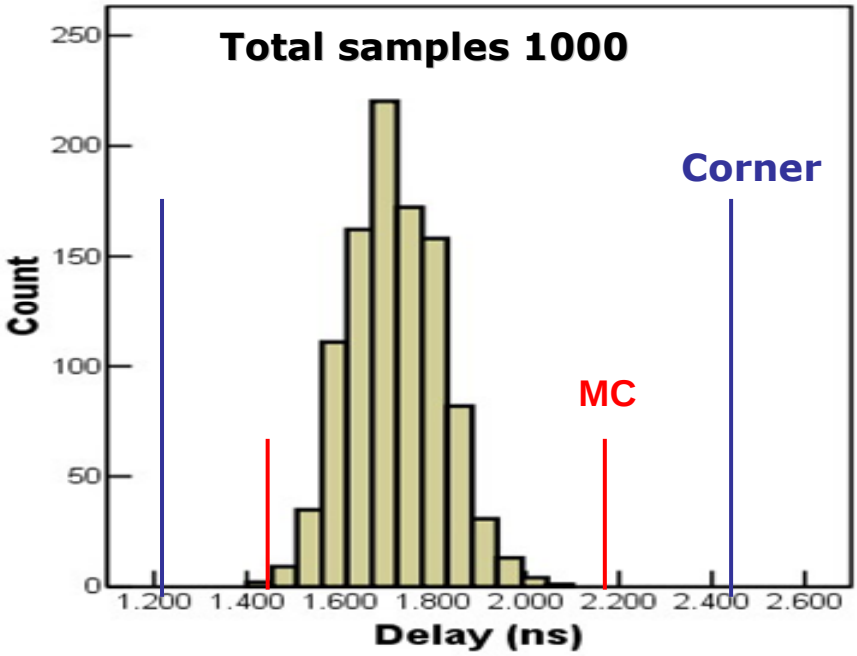


Fig. 4-7 Histogram of an inverter circuit carries delay and its worst-case values

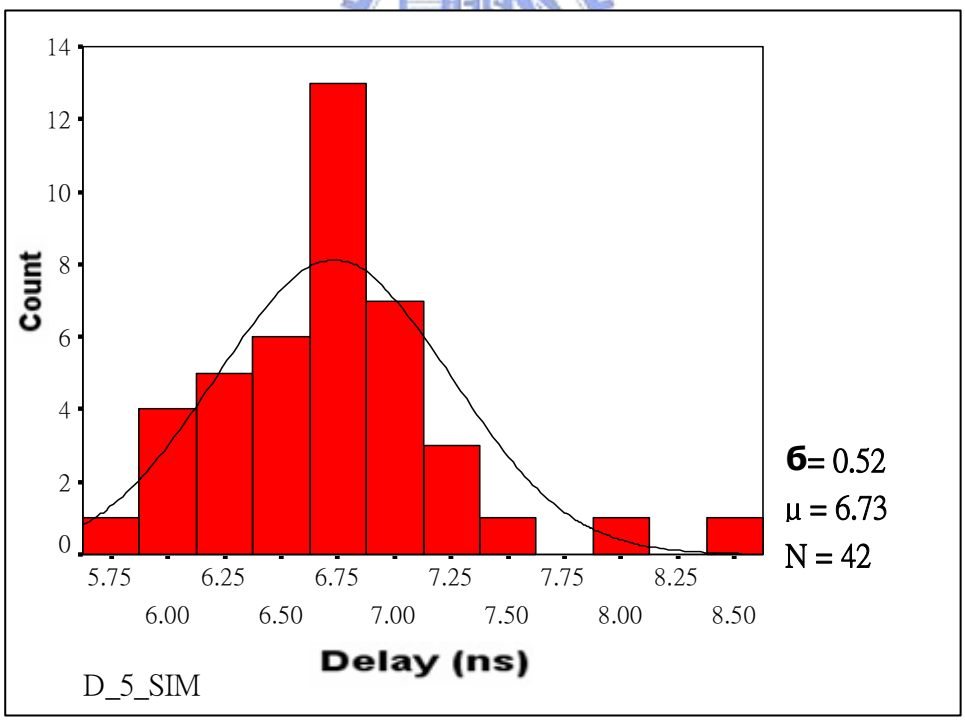


Fig. 4-8 the simulated delay time histogram of ring oscillator when operating voltage is 5V.

Device parameter combination is assumed to be random type, and

the microscopic effect is neglected

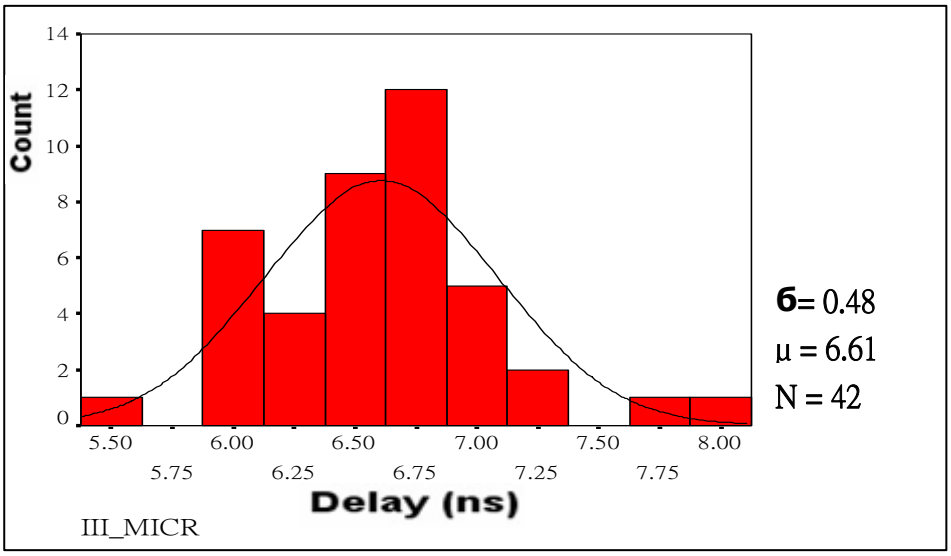


Fig. 4-9 the simulated delay time histogram of ring oscillator when operating voltage is 5V.

Device parameter combination is assumed to be random type, and

the microscopic device effect is included.

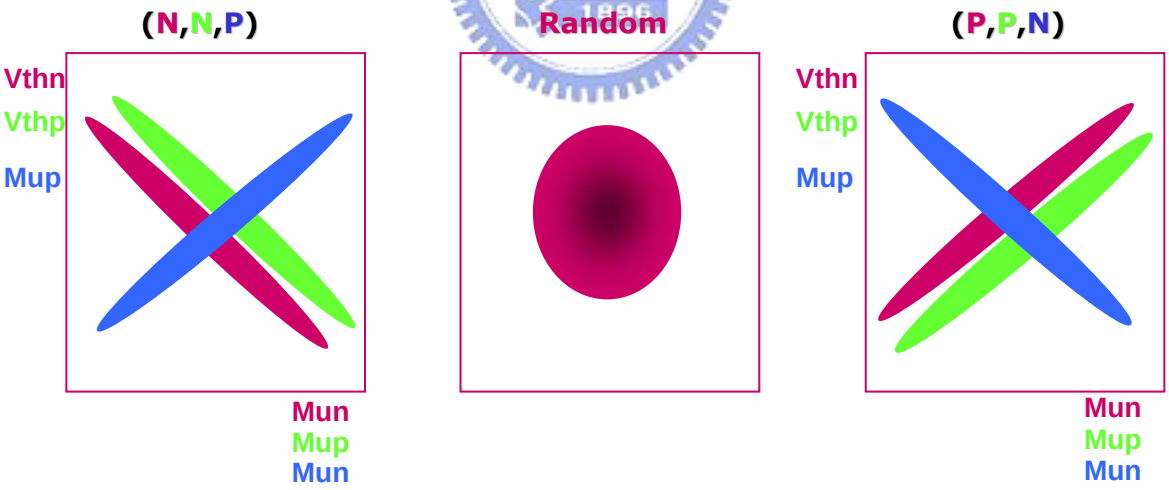


Fig. 4-10 Three types of combination between device parameters known as (N,N,P), random and (P,P,N), respectively.

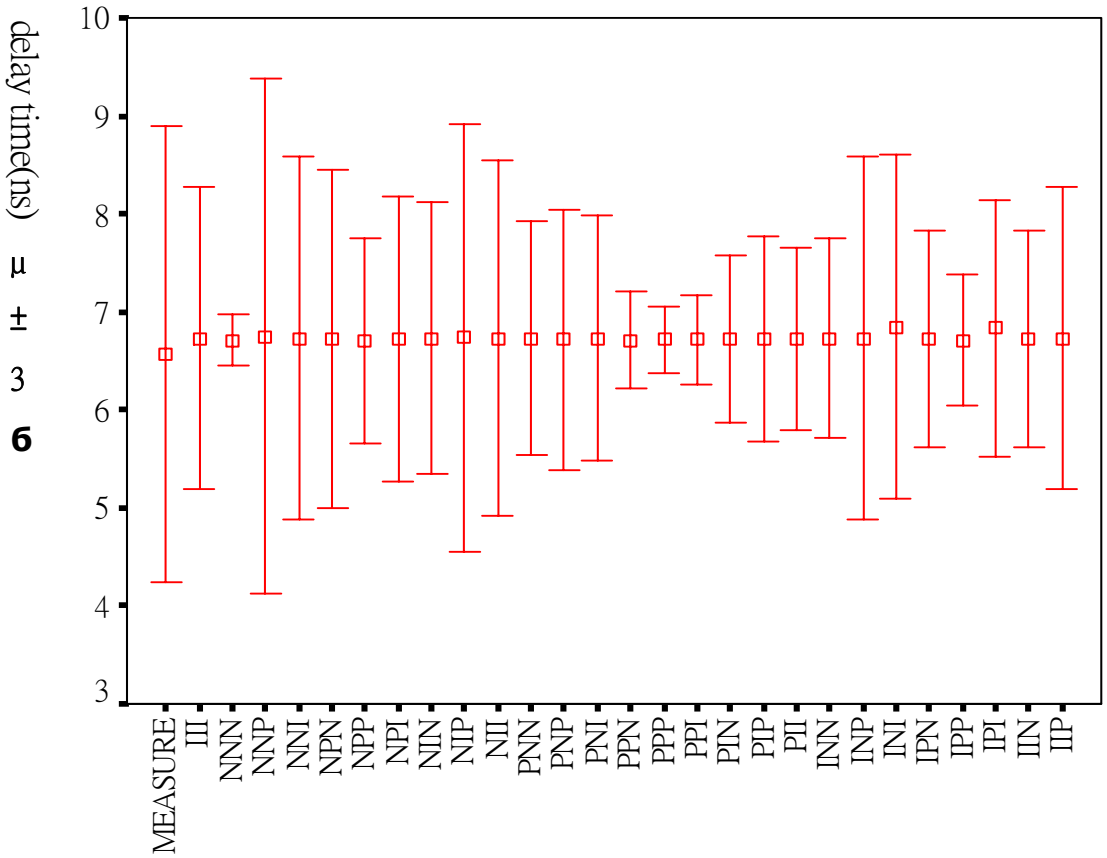


Fig. 4-11 the error bar graph of measured and simulated delay time for 27 sets combination between device parameters

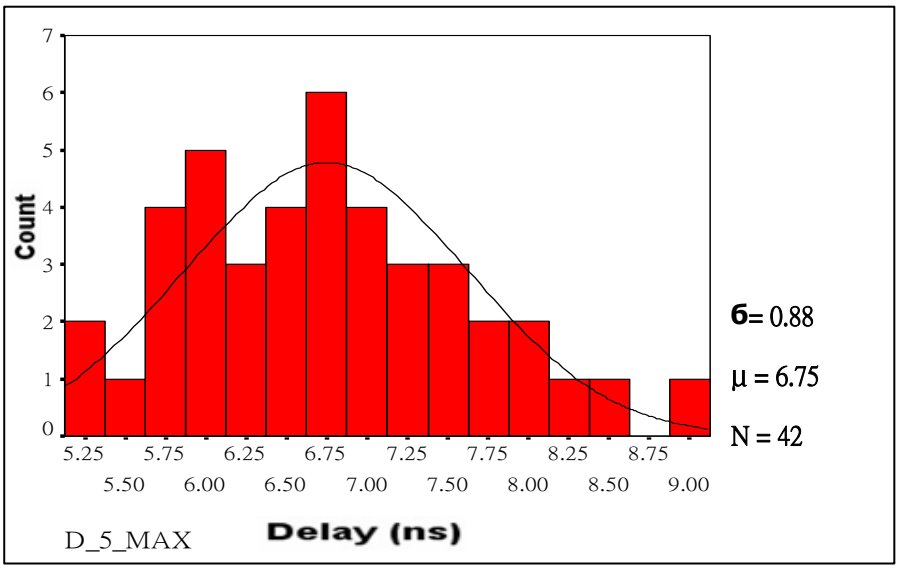


Fig. 4-12 the simulated delay time histogram of ring oscillator when operating voltage is 5V and device parameter combination is assumed to be (N,N,P)

Chapter 5

Conclusion and Future Work

In this thesis, we investigate the device variation issue in the LTPS TFT digital circuit. We aim at the major two types of device variation effect, known as microscopic and macroscopic device variation, on LTPS TFT circuit performance. A propagation delay is one of the most important performances, so that it is necessary to analyze the variability of the propagation delay. By implementing with ring oscillator test-key this makes it possible to do the correlation between measurement and simulation.

Firstly, we deal with the microscopic device variation effect on LTPS TFT circuit performance. With the aid of previous study on the distribution of initial parameter difference, the variation range of microscopic device variation is verified. Furthermore, the measurement result is consistent with our simulation result. More importantly, those researches proceeded independently, but they all point out the same conclusions. This definitely rises up the confidence level on our conclusion greatly.

Secondly, we aim at the macroscopic device variation effect on LTPS TFT circuit performance. We successfully proposed a new concept when dealing with macroscopic device variation effect. The original of our concept is the major difficulty when facing macroscopic device variation is unknown correlation of device parameter. The well-known concept for correlation of device parameter is random type. But after our verification by comparing the simulated and measured results, the random type correlation will underestimate the effect of macroscopic device variation on circuit performance which will lead to bad production yield without doubt. We conclude our discussion on macroscopic device variation with running

worst case condition of Monte Carlo simulation will get a more reliable prediction on variation range of circuit performance.

Finally, the microscopic variation effect on site-to-site circuit performance is evaluated. The conclusion here is micro variation is negligible when compared to macro. So the micro variation needs to be taken into consideration only when the matched TFT is used or specialized application such as current mirror, differential pair and etc.

In this work, we have classified and quantitatively distinguished macro and micro variation. This would be helpful for designers in predicting the circuit performance. In the future, we have to investigate the correlation between ring oscillator and more practical circuit such as shift register. And for the low voltage digital circuit requirement in future, study on the improvement of macroscopic device variation is urged.

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碩士班論文題目:

利用環型震盪器探討元件變異對低溫多晶矽薄膜電晶體電路效能之研究

Study on the Device Variation Effect on LTPS TFT Circuit Performance Using Ring Oscillator