國立交通大學

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碩 士 論 文

具辨識車輛方向功能之都卜勒雷達收發機

A Direction Sensitive Doppler Radar Transceiver For Vehicle Applications

研 究 生：昌任為

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中 華 民 國 九 十 五 年 九 月

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摘　　要

本篇論文提出一個 I/Q 分合混波器的架構且使用單一天線來發射與接收信號，此 I/Q 分合混波器可提供移動目標物的方向及速度，其功能如下 ： 一則可將本地振盪器的信號傳送到天線端後發射出去 ； 二則可將接收到之反射信號與本地振盪器信號混波後分成兩個(I/Q)中頻信號。另外，利用 DGS 的特性改善了振盪器離載波信號 100KHz 遠的相位雜訊大約 10-16dB.

本篇論文設計一個 10.5GHz 之都卜勒雷達收發機，包括 5.25GHz 鎖相頻率合成器、5.25GHz 至 10.5GHz 之頻率乘法器、10.5GHz 帶通濾波器、I/Q 分合混波器、中頻放大器等，接著使用一個 X-Band 標準天線和數位信號處理來量測此收發機的特性，量測結果顯示可正確的判斷出目標物是接近或遠離以及目標物的移動速度，此收發機可應用於智慧型運輸系統。

A Direction Sensitive Doppler Radar Transceiver For Vehicle Applications

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Abstract

In this thesis, an I/Q hybrid mixer with particular characteristic of passing LO power to antenna port is proposed to provide the direction and velocity for a moving target, which the transmitted radar signal and the received echo signal pass through the same antenna with no circulator. In addition, the phase noise of oscillator has been reduced by 10-16dB at 100KHz offset from carrier using the Defected Ground Structure (DGS).

A 10.5GHz Doppler radar transceiver consists of 5.25GHz PLL frequency synthesizer, 5.25GHz to 10.5GHz frequency doubler , 10.5GHz band pass filter (BPF) , I/Q hybrid mixers and IF amplifiers which has been designed , fabricated and integrated for above each component. The designed Doppler radar transceiver is then measured using an X-band standard horn antenna and Digital Signal Processing(DSP) that shows the validity of distinguishing a receding target or an approaching target and the related moving velocity for the applications of Intelligent Transportation Systems (ITS).

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Chapter 1 Introduction

1.1 Motivation and Objective

With the increase of traffic density and car accident on today's road, Intelligent Transportation Systems (ITS) have been adopted to monitor and manage traffic flow, relieve traffic congestion, provide alternate routes to travelers, and improve transportation safety and efficiency. An ITS consists of smart roads and routs, smart cars, smarts buses, smart trains, smart cargo, smart baggage, and smart travelers all working together in a cohesive system. The ITS market areas have been divided into nine sections as shown in Fig.1.1 [1]. The sensor in ITS technology is able to sense and measure the current state of the traffic on the highway and the status of the transportation system as a whole.

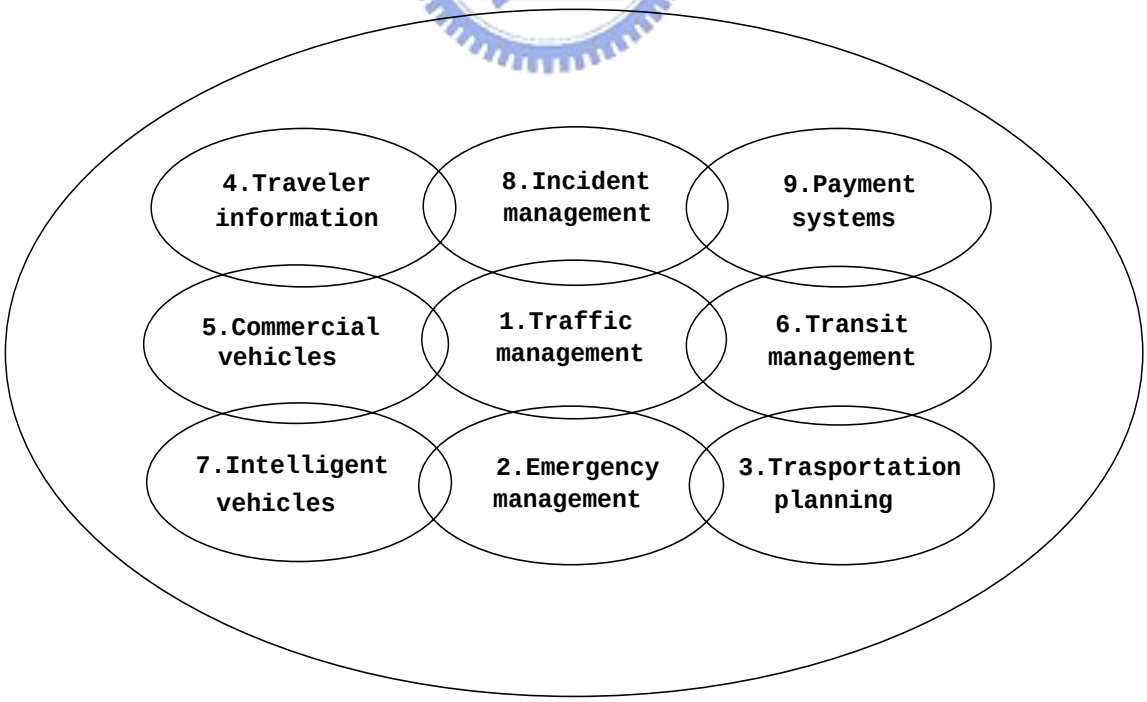


Figure 1.1 The ITS market areas

Currently there are three kinds of vehicles sensors on markets: circular loop sensors, infrared sensors and radar sensors .And radar sensors will replace circular sensors and infrared sensors in the future [2]. Radar sensor has two types: continual wave (CW) radar sensor and linear frequency modulation continual wave (LFMCW) radar sensor. CW radar utilizes the theory of measuring speed to detect traffic and speed of moving vehicle. LFMCW radar utilizes the theory of measuring distance which is usually used when vehicle are static or moving in very slow speed [3].

A Doppler radar sensor can easily measure both the true ground-speed of vehicles and the relative speed between a car and an obstacle so that it can be used to reduce reaction times in avoiding accidents or simply to monitor a high density traffic road [4]. However, for the applications of traffic monitoring systems, motion sensors and automotive Doppler navigation aids, it is of interest to know whether the target is approaching or receding. In order to obtain the velocity sign information, an I/Q mixer has been adopted and demonstrated using two antennas to transmitting and receiving respectively [5].

The purpose of this thesis is to design a Doppler radar transceiver which is able to provide the direction and speed for a moving target using an I/Q hybrid mixer with single antenna.

1.2 Radar System

Radar (Radio Detection And Ranging) detects the presence of objects and locates their position in space by transmitting electromagnetic and observing the returned signal.

A. Simple Doppler Radar [6]

If the target has a velocity component along the line-of-sight of the radar, the returned signal will be shifted in frequency relative to the transmitted frequency, due to doppler effect. If the transmitted frequency is f_0, and the radial velocity is v, then the doppler frequency shift will be

$$f_d = \frac{2vf_0}{c} \tag{1.1}$$

where c is the velocity of light. The received frequency is then $f_0 \pm f_d$, where the plus sign corresponds to an approaching target and the minus sign corresponds to a receding target. Fig. 1.2 shows a basic doppler radar system. The oscillator signal f_0 can be used as the transmitted signal, and the oscillator signal f_0 can also be used as a local oscillator for receiver mixer, because the received echo signal is frequency offset by the doppler frequency. The filter following the mixer should have a pass band corresponding to the expected minimum and maximum target velocities. It is important that the filter have high attenuation at zero frequency, to eliminate the effect of clutter return and transmitter leakage at frequency f_0, as these signals would down-convert to zero frequency. This type of filter response also helps to reduce the effect of 1/f noise.

The major drawback of the above radar is, can not distinguish between approaching and receding targets, as the sign of f_d is lost in the detection process.

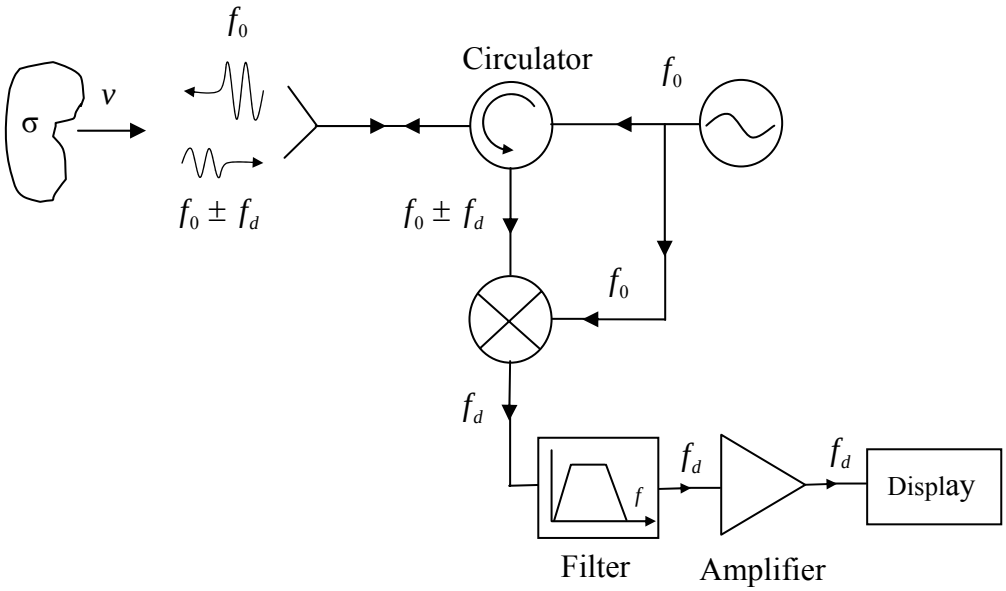


Figure 1.2 Simple Doppler Radar

B. Direction Sensitive Doppler Radar [7]

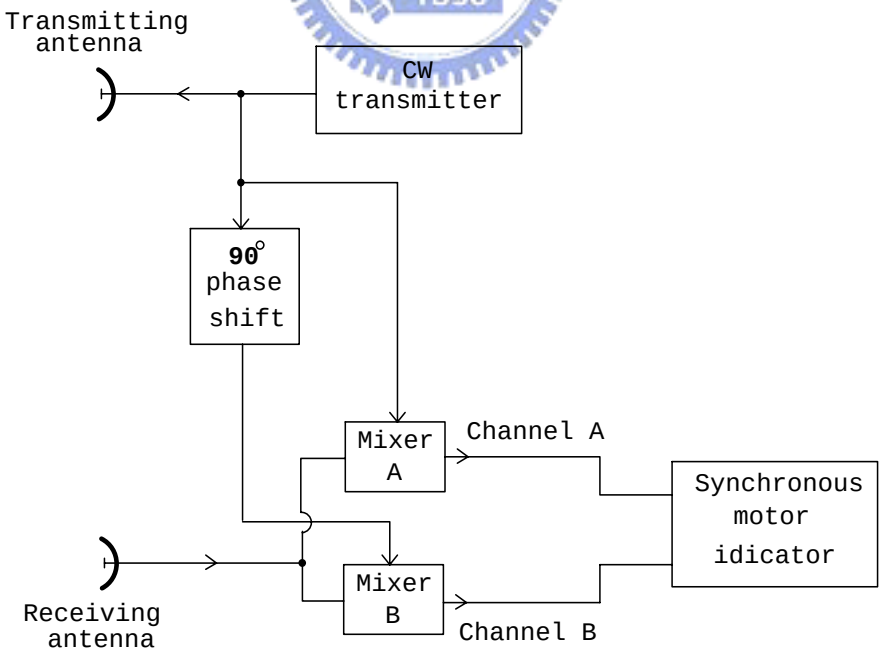


Figure 1.3 The classic Doppler radar for obtaining the velocity sign information

The sign of the doppler frequency, and therefore the direction of target motion, may be found by splitting the received signal into two channels as shown in Fig. 1.3.

If the transmitter signal is given by

$$E_t = E_0 \cos \omega_0 t \tag{1.2}$$

the echo signal from a moving target will be

$$E_r = k_1 E_0 \cos[(\omega_0 \pm \omega_d)t + \phi] \tag{1.3}$$

where E_0 = amplitude of transmitter signal

k_1 = a constant determined from radar equation

ω_0 = angular frequency of transmitter, rad/s

ω_d = doppler angular frequency shift

ϕ = a constant phase shift, which depends upon range of initial detection

The received signal and a portion of the transmitter heterodyne in the detector (mixer) to yield a difference signal

$$E_A = k_2 E_0 \cos(\pm\omega_d t + \phi) \tag{1.4}$$

The other channel is similar, except for a 90° phase delay introduced in the reference signal. The output of the channel B mixer is

$$E_B = k_2 E_0 \cos(\pm\omega_d t + \phi + \frac{\pi}{2}) \tag{1.5}$$

If the target is approaching (positive doppler), the outputs from the two channels are

$$E_A(+) = k_2 E_0 \cos(\omega_d t + \phi) \qquad E_B(+) = k_2 E_0 \cos(\omega_d t + \phi + \frac{\pi}{2}) \tag{1.6a}$$

On the other hand, if the target is receding (negative doppler) ,

$$E_A(-) = k_2 E_0 \cos(\omega_d t - \phi) \qquad E_B(-) = k_2 E_0 \cos(\omega_d t - \phi - \frac{\pi}{2}) \tag{1.6b}$$

The sign of ω_d and the direction of the target's motion may be determined according to whether the output of channel B leads or lags the output of channel A .

1.3 Overview of this Thesis

There are five chapters in this thesis as follows:

Chapter 1 presents the difference between simple Doppler radar and direction sensitive Doppler radar.

Chapter 2 describes the architecture of the designed 10.5GHz Doppler radar transceiver. And presents the basic theory.

Chapter 3 shows the results of the simulation and measurement for each component including the I/Q hybrid mixer, 5.25GHz PLL frequency synthesizer, 5.25GHz to 10.5GHz frequency doubler and 10.5GHz band pass filter.

Chapter 4 shows the measurement results of the designed 10.525GHz Doppler radar transceiver for the phase noise and output power, then is measured using an X-band standard horn antenna and Digital Signal Processing (DSP) for a moving target.

Chapter 5 describes the conclusion and future study.

Chapter 2 Transceiver Architecture and Basic Theory

2.1 Transceiver Architecture

In this thesis, an I/Q hybrid mixer with particular characteristic of passing LO power to antenna port is proposed to provide the direction and velocity for a moving target, which the transmitted radar signal and the received echo signal pass through the same antenna with no circulator. There are two phase shifts of 45° in the I/Q hybrid mixer which are located between 90° hybrid A and hybrid mixer I , and between hybrid mixer Q and 90° hybrid B respectively. The designed doppler radar transceiver consists of 5.25GHz PLL frequency synthesizer, 5.25GHz to 10.5GHz frequency doubler, 10.5 10.5GHz band pass filter (BPF) , I/Q hybrid mixers and IF amplifiers as shown in Figure 2.1.

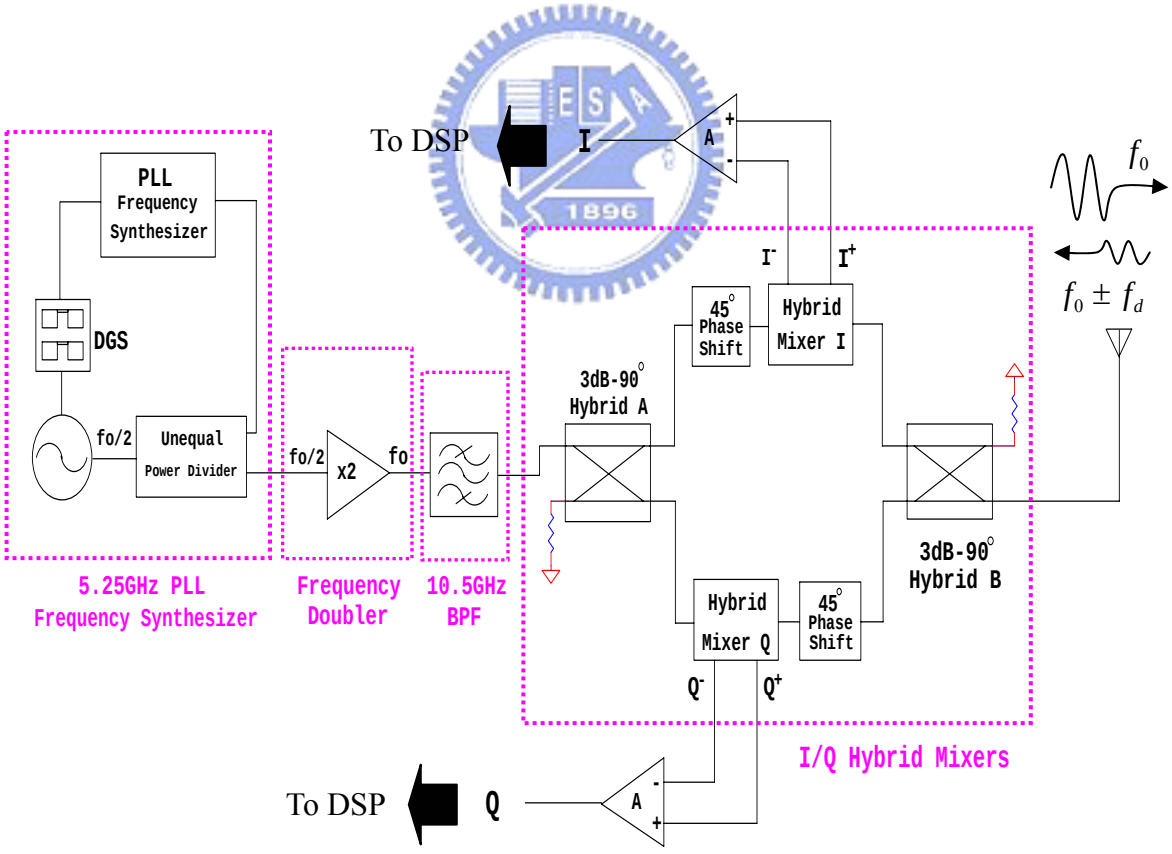


Figure 2.1 Architecture of the designed 10.5GHz Doppler radar transceiver

2.2 Hybrid Mixer

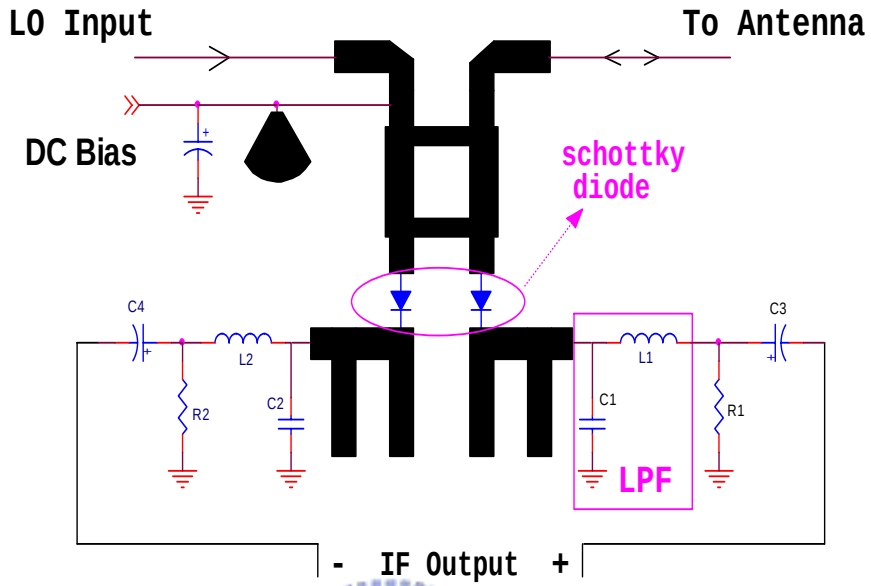


Figure 2.2 Schematic of the hybrid mixer

Fig.2.2 shows the schematic of the hybrid mixer. It consists of a quadrature hybrid and two schottky diodes, which has the symmetrical structure with differential IF output to compensate the AM noise. The quadrature hybrid is designed using microstrip branch line circuitry in the frequency of 10.5GHz. Since the LO signal is connected to the input of the 90° hybrid , the schottky diodes are connected to the through port and coupler port respectively, and the antenna is connected to isolation port. The quarter-wavelength open stubs have been adopted to avoid directly short circuit between the IF output and ground with respect to using via holes which act as RF ground to the schottky diodes. RF chokes and LC low pass filters with stop frequency of 100 KHz are connected to the IF outputs. Another RF choke is connected to the hybrid for DC biasing. The parallel resistors of several hundred ohms to ground are required to discharge the static charge at IF outputs.

In operation, the 90° hybrid splits the LO signal with equal amplitude and phase difference of 90° . These split signals drive the mixer diodes and then reflected from the diodes with little attenuation. These reflected signals enter the hybrid again and will cancel at the LO port and combine at the antenna port. The insertion loss from LO to antenna is the summation of the reflection loss from diodes and twice of the hybrid transmission loss. Since the diodes are connected to a virtual short, the reflection loss is quite small and the hybrid loss is also negligible. Thus most of the input LO power is bypassed to the antenna for transmitting signal. Once the echo signal is received from the antenna, it is split and enters the mixer diodes. The IF output of the hybrid mixer is a differential format wit phase difference of 180° which is able to eliminate several noises from RF source. The major noise from RF source such as AM noise and flick (1/f) noise will appear in the common mode of the mixer output. This term will be rejected after the following differential amplifier. Since the diodes are placed in parallel, DC bias can be added to make the mixer work properly when LO power is low. The added DC bias will influence the insertion loss and the conversion loss of the mixer. The total loss can be calculated as the summation of the insertion loss and conversion loss. Thus, an optimum performance can be achieved by fine tuning the bias voltage for various LO power [8].

2.3 Defected Ground Structure (DGS)

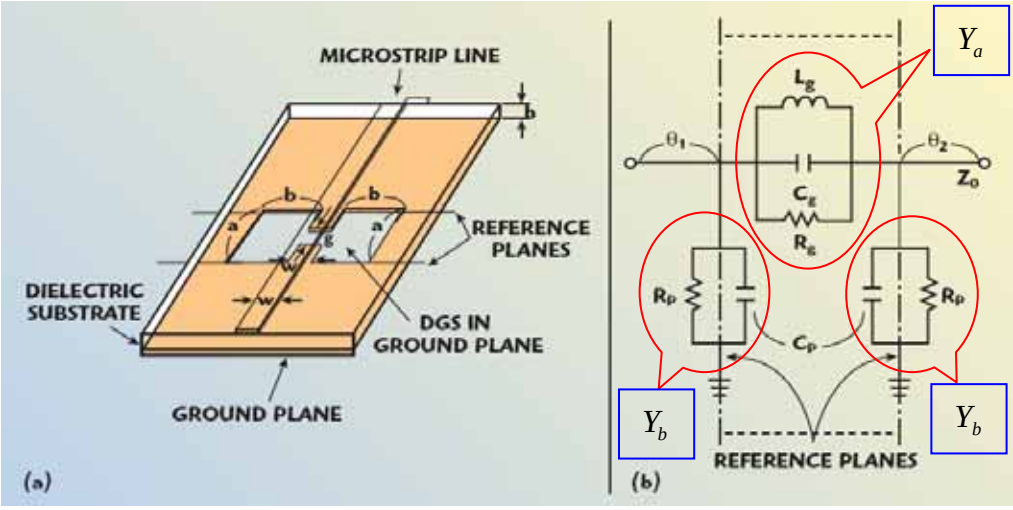


Figure 2.3 (a) 3-Dimensinal view of the DGS unit section. (b) Equivalent circuit

Defected Ground Structure (DGS) consists of narrow and wide etched areas in backside metallic ground plane as shown in Figure 2.3(a). An etched defect in ground plane disturbs the shield current distribution in the ground plane. This disturbance can change characteristics of a transmission line such as line capacitance and inductance.

A DGS unit has a cutoff frequency at a certain frequency due to the increase of the effective series inductance of the transmission line. It also has an attenuation pole above the cutoff frequency. Thus , the equivalent circuit of the DGS can be modeled as a parallel LC resonant circuit with a parallel conductance and include the parallel capacitance due to the relatively large fringing field at the step discontinuity plane on metallic ground surface as shown in Figure 2.3(b) . In order to derive the equivalent circuit parameters, the S-parameters of a DGS unit cell at the reference plane are calculated by EM-simulation. Once the S-parameters are calculated at the cutoff frequency, the equivalent circuit parameter can be extracted by using the relation between the S-parameters and ABCD-parameters as the following [9]:

$$A = \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{2S_{21}} = 1+\frac{Y_b}{Y_a} \tag{2.1}$$

$$B = \frac{(1+S_{11})(1+S_{22})-S_{12}S_{21}}{2S_{21}} = \frac{1}{Y_a} \tag{2.2}$$

$$C = \frac{1}{Z_0}\frac{(1-S_{11})(1-S_{22})-S_{12}S_{21}}{2S_{21}} = 2Y_b + \frac{Y_b^2}{Y_a} \tag{2.3}$$

$$D = \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{2S_{21}} = 1+\frac{Y_b}{Y_a} \tag{2.4}$$

where Y_a = series susceptance of the the π-type symmetrical two-port circuit

Y_b = parallel susceptance of the the π-type symmetrical two-port circuit

Then, the ABCD parameters of the π-type symmetrical circuit are represented by these equivalent circuit parameters. The resulting relations between the equivalent circuit parameters of the π-type symmetrical two-port circuit and the equivalent circuit parameters of the DGS circuit are given by

$$Y_a = \frac{1}{B} = \frac{1}{R_g} + jB_r \tag{2.5}$$

$$Y_b = \frac{A-1}{B} = \frac{-1\pm\sqrt{1+BC}}{B} = \frac{D-1}{B} = \frac{1}{R_p} + jB_p \tag{2.6}$$

From these relations, the equivalent circuit parameters of the DGS circuit are given by

$$C_g = \frac{B_r}{\omega_2\left[\frac{\omega_1}{\omega_2}-\frac{\omega_2}{\omega_1}\right]} \tag{2.7}$$

$$L_g = \frac{1}{\omega_2^2 C_g} \tag{2.8}$$

$$C_p = \frac{B_p}{\omega_1} \tag{2.9}$$

$$R_g = \frac{1}{\mathrm{Re}[Y_a]} \tag{2.10}$$

$$R_p = \frac{1}{\mathrm{Re}[Y_b]} \tag{2.11}$$

where ω_1 = cutoff frequency of the EM-simulated resulted for the unit DGS circuit

ω_2 = attenuation pole of the EM-simulated resulted for the unit DGS circuit

$\mathrm{Re}[Y_a]$ = real parts of Y_a

$\mathrm{Re}[Y_b]$ = real parts of Y_b

The frequency characteristic of the DGS section can be described by two parameters: the etched lattice dimension and gap distance [10].

A. Influence of the Square Lattice Dimension

In order to investigate the influence of the square lattice dimension, the etched gap(g) was kept constant to 0.2mm for all three lattice dimension cases: a = b =1.3mm, a = b =2.5mm , a = b =4.6mm as shown in Fig. 2.3(a). The substrate with 62-mil thick and a dielectric constant of ten was used for all simulations. The simulation results are illustrated in Fig. 2.4. There are attenuation poles in simulation results on the etched unit lattices. These attenuation poles can be explained by parallel capacitance with the series inductance. These capacitance values depend on the etched gap below the conductor line, which are identical for all cases due to the identical gap distance. As the etched area of the unit lattice is increased, the effective series inductance increases, and increasing the series inductance gives rise to a lower cutoff frequency and a lower attenuation pole as seen in Fig. 2.4.

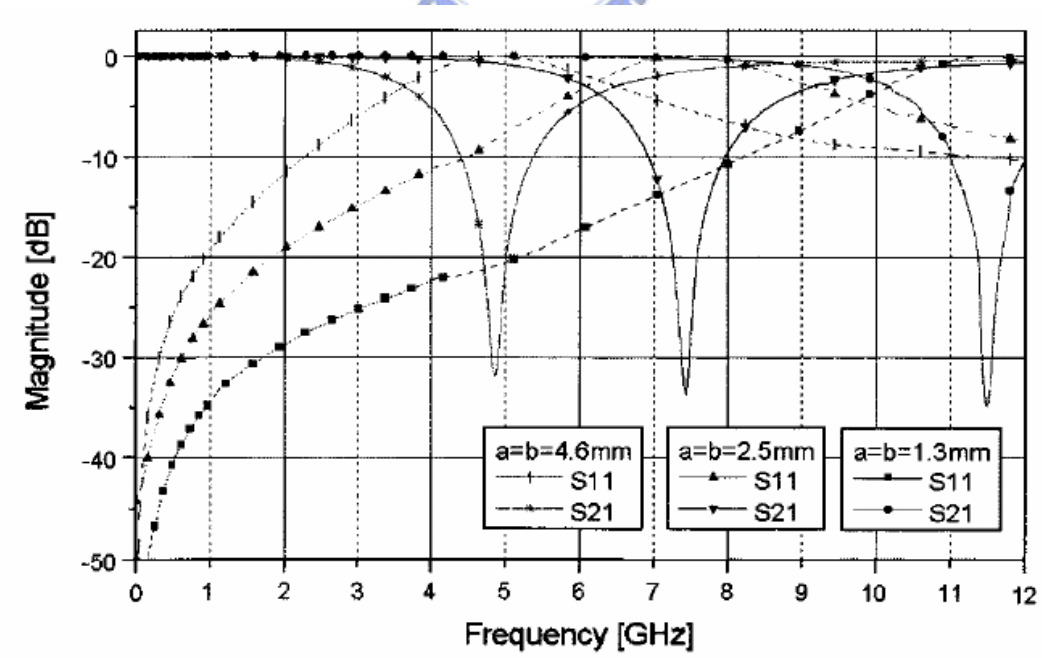


Figure 2.4 Three DGS unit lattices simulation for varying the square lattice dimension

B. Influence of the Gap Distance

The lattice dimension a×b was kept constant to 2.5 mm×2.5 mm for all three gap distance cases : g = 0.2mm , g = 0.4 mm , g = 0.6 mm. The simulation results are shown in Fig. 2.5. The effective series inductances are constant due to the constant lattice dimensions. Unlike the influence of lattice dimension, there is no change in cutoff frequency despite the variation of the gap distance. This means that the gap distance does not affect the effective series inductance of a microstrip line. Variation of the effective capacitance only affects the attenuation pole location. As the etched gap distance increases, the effective capacitance decreases so that the attenuation pole location moves up to higher frequency as seen in Fig.2.5.

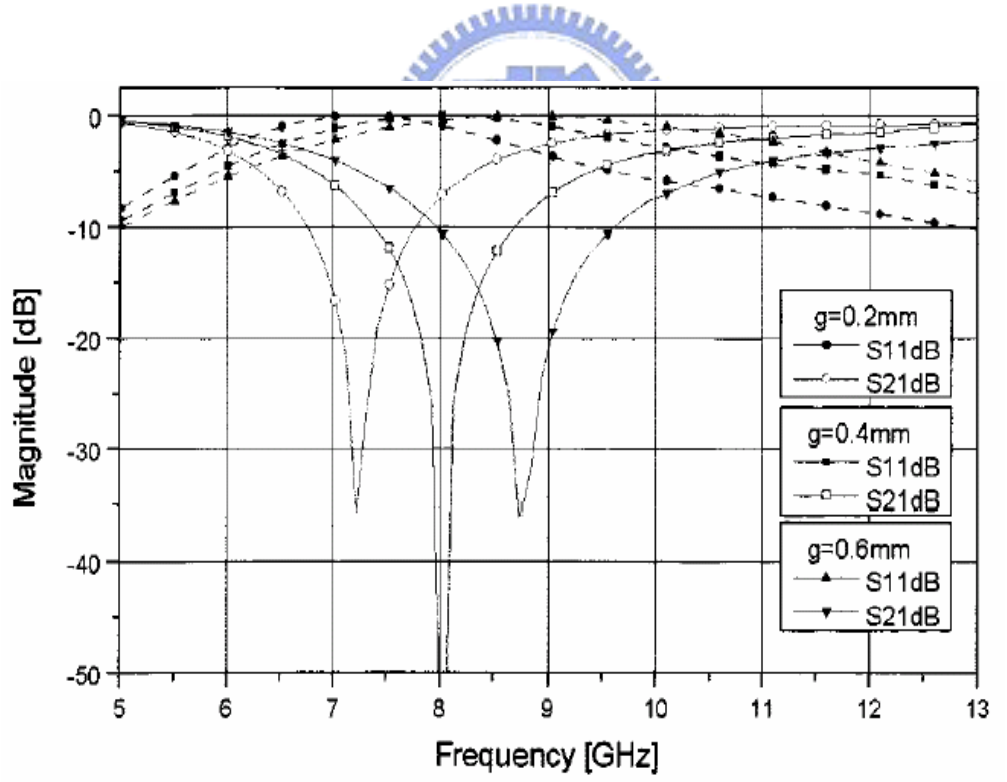


Figure 2.5 Three DGS unit lattices simulation for varying the gap distance

2.4 Fundamental of Oscillators

2.4.1 Feedback Oscillators [11]

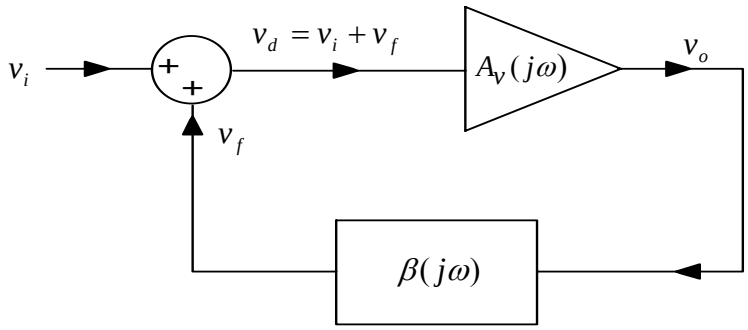


Figure 2.6 The basic feedback circuit.

Fig.2.6 shows a basic feedback oscillator. The amplifier's voltage gain is $A_v(j\omega)$, and the voltage feedback network is described by the transfer function $\beta(j\omega)$.Positive feedback occurs when the feedback signal (v_f) adds from input signal (v_i). The phase of v_f determined if v_f adds or subtracts from v_i and is determined by the closed-loop circuit in Fig.2.6. For positive feedback the total phase shift associated with the closed loop must be 0° or a multiple of 360°. The closed-loop voltage gain $A_{vf}(j\omega)$ can be found to be

$$A_{vf}(j\omega) = \frac{v_o}{v_i} = \frac{A_v(j\omega)}{1-\beta(j\omega)A_v(j\omega)} \qquad (2.12)$$

For oscillations to occur, an output signal must exist with no input signal applied. With v_i=0 in equation (2.12), it follows that a finite v_0 is possible only when denominator is zero. That is, when

$$1-\beta(j\omega)A_v(j\omega) = 0 \quad \text{or} \quad \beta(j\omega)A_v(j\omega) = 1 \qquad (2.13)$$

Equation (2.13) expresses the fact that for oscillator to occur, the loop gain [$\beta(j\omega)A_v(j\omega)$] must be unity. This relation is known as the Barkhausen criterion.

With $A_v(j\omega) = A_{vo}$ and letting $\beta(j\omega) = \beta_r(\omega) + j\beta_i(\omega)$

where $\beta_r(\omega)$ and $\beta_i(\omega)$ are the real and imaginary parts of $\beta(j\omega)$, then (2.13) can be rewritten as $\beta_r(\omega)A_{vo} + j\beta_i(\omega)A_{vo} = 1$

Equating the real and imaginary parts on both sides of the equation gives

$$\beta_r(\omega)A_{vo} = 1 \quad \Rightarrow \quad A_{vo} = \frac{1}{\beta_r(\omega)} \tag{2.14}$$

and

$$\beta_i(\omega)A_{vo} = 0 \quad \Rightarrow \quad \beta_i(\omega) = 0 \tag{2.15}$$

since $A_{vo} \neq 0$. The condition (2.14) is known as the gain condition, and (2.15) as the frequency of oscillation condition. The frequency of oscillation condition gives the frequency at which the phase shift around the closed loop is 0° or a multiple of 360°. From the circuit theory we know that oscillation occurs when a network has a pair of complex conjugate poles on the imaginary axis. Most importantly, the gain condition should be modified to be $\beta_r(\omega)A_{vo} > 1$ to put the transfer-function pole in the right half plane, to allow the oscillation to commence. Then, as the oscillation builds, the amplifier saturates, the gain decreases, and the oscillation stabilizes at $\beta_r(\omega)A_{vo} = 1$.

In a feedback oscillator, it is relatively easy to avoid spurious resonance, which could cause the oscillator to oscillate at an undesired frequency. As long as the resonator has transmission only at resonant frequency, the oscillator can oscillate only at the desired frequency. Unfortunately feedback oscillator can be difficult to design at high frequencies due to the phase shift in the long connection from the amplifier output to the resonator, so high-frequency oscillators are usually designed by means of a negative-resistance theory.

2.4.2 Negative Impedance Oscillators [12]

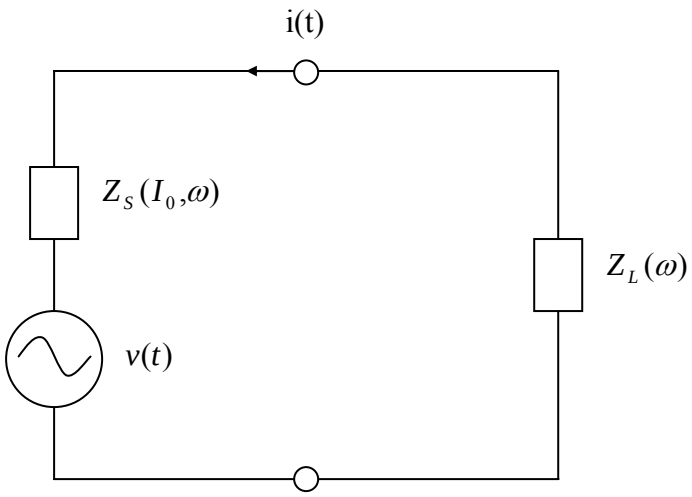


Figure 2.7 The classical model of a negative-resistance oscillator

An oscillator is an energy conversion device that transforms dc power into ac power. A microwave oscillator can be modeled as a one-port in which the real part of the port impedance is negative as shown in Fig.2.7. The load impedance $Z_L(\omega)$ is linear, but the source impedance $Z_S(I_0,\omega)$ (the output impedance of the oscillator) is a function of I_0, the magnitude of the fundamental frequency component of the output current. The real part of Z_S is negative and decrease with an increase in I_0.The voltage source $v(t)$ in Fig.2.7 provides a perturbation necessary to start oscillation in the unstable circuit.In practical circuits it represents noise, an injection-locking signal, or the turn-on transient of the circuit.

Kurokawa proved that the conditions for oscillation are

$$Z_S(I_0,\omega)+Z_L(\omega)=0 \qquad (2.16)$$

that is, the real parts of the impedances cancel and the imaginary parts resonant. Then, if an infinitesimal perturbation $v(t)$ exists, the magnitude of the response $i(t)$ increases exponentially with time and becomes sinusoidal at some frequency ω_p where

$$\mathrm{Im}\{Z_S(\omega_P)\}=-\mathrm{Im}\{Z_L(\omega_P)\}$$

The source could also be described by a nonlinear conductance $Y_S(V_0,\omega)$; then, the oscillation condition is

$$Y_S(V_0,\omega)+Y_L(\omega)=0 \tag{2.17}$$

This is the case of a parallel resonance having a total negative conductance, in which the transient perturbation comes from a shunt small-signal current source, and V_0 is the magnitude of the shunt voltage. The oscillation begins when real part of the shunt conductance is negative and $\mathrm{Re}\{Y_S\}$ decreases as the oscillation increases until (2.17) is satisfied. If a transistor oscillator circuit includes a high-Q resonator, the high-Q resonator will dominate in establishing the frequency. In a high-Q resonator, $\mathrm{Im}\{Y_L\}$ varies rapidly with frequency close to resonance, so changes in $\mathrm{Im}\{Y_S\}$ do not cause much frequency deviation.

The oscillation is stable if the sinusoidal voltage or current returns to its steady-state value after it is perturbed. Kurokawa derived a condition for stable oscillation; in terms of impedance, the condition is

$$\frac{\partial R_S}{\partial I}\frac{\partial X_L}{\partial \omega}-\frac{\partial X_S}{\partial I}\frac{\partial R_L}{\partial \omega} > 0 \tag{2.18}$$

where $R_S=\mathrm{Re}\{Z_S\}$, $X_S=\mathrm{Im}\{Z_S\}$, $R_L=\mathrm{Re}\{Z_L\}$, $X_L=\mathrm{Im}\{Z_L\}$, and the derivatives are evaluated at $I=I_0$ and $\omega=\omega_P$. In a simple case where X_S is independent of I and the load is a simple series RL or RC circuit, (2.18) is always satisfied.

2.5 PLL Frequency Synthesizer

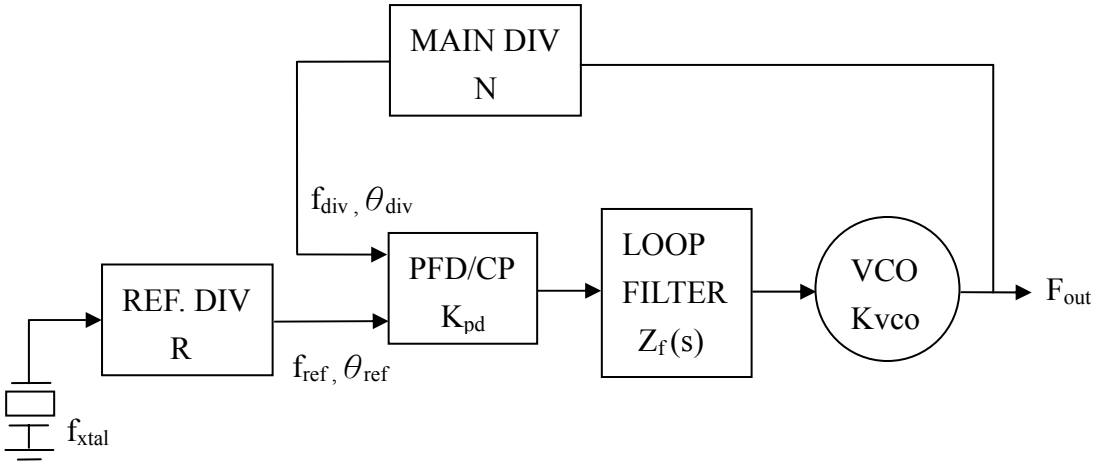


Figure 2.8 Block diagram of a single-loop PLL frequency synthesizer

A phase-locked loop (PLL) is used primarily in communication system. The architecture of a single-loop integer-N PLL is shown in Fig.2.8 which consists of a voltage-controlled oscillator (VCO), a programmable frequency divider with a divider N, a phase-frequency detector/charge pump combination (PFD/CP) and a loop filter. In addition, the architecture also comprises a reference crystal oscillator and a reference frequency divider of ratio R. When the loop is locked the phase of the divided output signal f_{div} accurately tracks the phase of the reference signal f_{ref}. The phase-lock process forces the frequencies of f_{div} and f_{ref} to be equal.

Relating F_{out} to f_{div} and f_{ref} can be obtained as

$$F_{out}=N\cdot f_{ref}=N\cdot\frac{f_{xtal}}{R} \tag{2.19}$$

If the division ratio N is programmable in steps of 1, then F_{out} can be stepped with a minimum step size equal to f_{ref}.

In the basic PLL configuration of Fig. 2.8, the frequency range of the VCO must be covering the total tuning range of the intended application [13].

.2.5.1 Phase-Frequency Detector / Charge-Pump

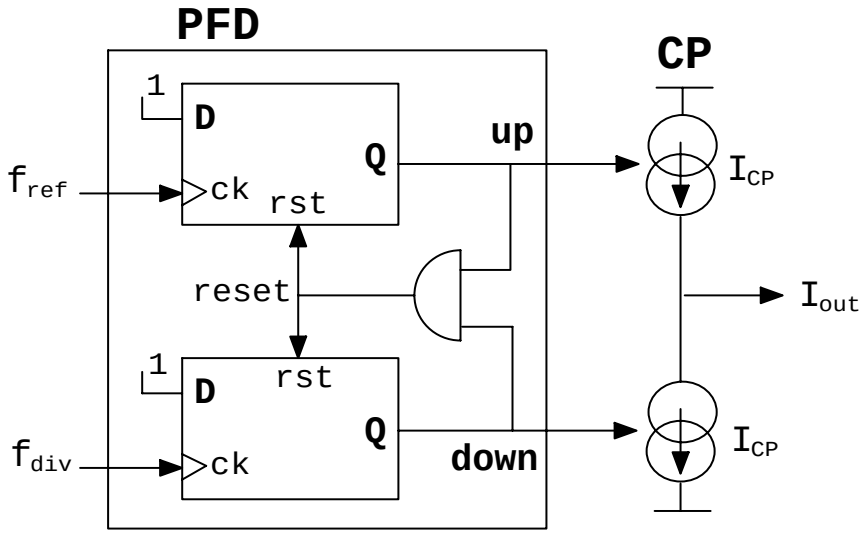
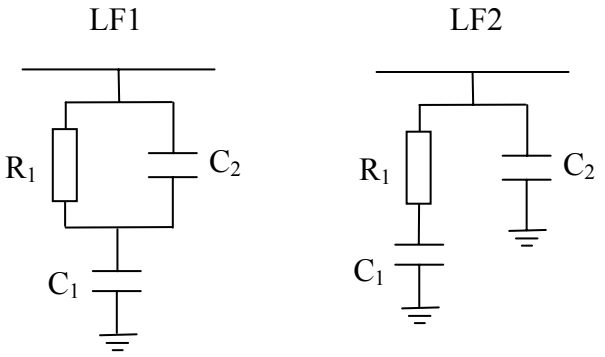


Figure 2.9 Sequential phase-frequency detector combined with single-ended charge-pump

The block diagram of a common implementation of the phase-frequency detector is presented in Fig. 2.9.It consists of two D-type flip-flops (D-FF)which have their D inputs connected to the active level. The upper D-FF, which is clocked by f_{ref}, generates the up signal. The lower D-FF, which is clocked by f_{div}, generates the down signal. The AND gate monitors the up and down signals and generate the reset signal for the D-FFs at the moment both outputs become active. The up and down signals are used to switch the current sources in the charge-pump CP. When up is active, a current with magnitude of I_{CP} is sourced by the charge-pump; conversely, when down is active, current is sunk into the charge-pump. When both up and down are inactive, no current flows into or out the output node of the charge-pump. The output is a high impedance node, under all circumstances.

2.5.2 Loop Filter



Parameter	LF1	LF2
τ_2	$R_1(C_1+C_2)$	R_1C_1
τ_3	R_1C_2	$R_1\frac{C_1C_2}{C_1+C_2}$
k	$\frac{1}{C_1}$	$\frac{b-1}{b}\cdot\frac{1}{C_1}$
$b(\tau_2/\tau_3)$	$1+\frac{C_1}{C_2}$	$1+\frac{C_1}{C_2}$

Figure 2.10 Two common passive loop filter topologies and corresponding relationships design parameters and component values.

The loop filter provides the current-to-voltage conversion from the charge-pump signal to the tuning voltage input of the VCO. The purity of the tuning voltage determines to a great extent the spectral components of the VCO output signal. The trans-impedance transfer function of the loop filter as

$$Z_f(s)=\frac{k}{s}\frac{1+s\tau_2}{1+s\tau_3}=\frac{k}{s}\frac{1+s\tau_2}{1+s\tau_2/b} \tag{2.20}$$

where k is a gain factor which depends on the specific configuration of the loop filter , τ_2 is the time constant of the "stabilizing" zero, τ_3 is the time constant of the pole which is used to attenuate the reference frequency and its harmonics and b is the ratio of the time constants τ_2/τ_3 .

Two passive loop filter configurations which comply to (2.20) are shown in Fig. 2.10. The trans-impedance transfer functions $Z_{f1}(s)$ and $Z_{f2}(s)$ for loop filters LF1 and LF2 respectively, are given as follows:

$$Z_{f1}(s)=\frac{1+s(R_1(C_1+C_2))}{sC_1(1+sR_1C_2)} \tag{2.21}$$

$$Z_{f2}(s)=\frac{1+s(R_1C_1)}{s(C_1+C_2)(1+(sR_1\frac{C_1C_2}{C_1+C_2})} \tag{2.22}$$

The purpose of the capacitor (C_2) is to decrease the loop filter trans-impedance at high frequencies, and therefore to decrease the magnitude of the voltage ripple of a given value of DC leakage current.

2.6 Active Frequency Multiplier

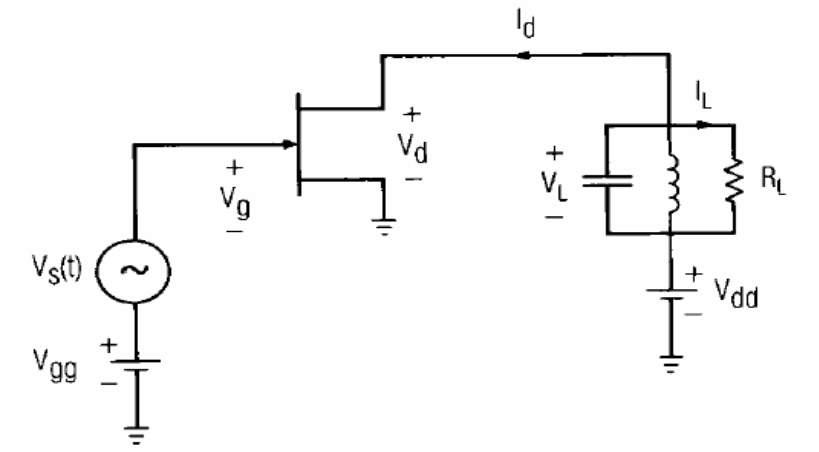


Figure 2.11 Circuit of an ideal FET frequency multiplier

The circuit of a frequency multiplier with an ideal FET is as shown in Fig.2.11. The output resonator is tuned to the nth harmonic of the excitation frequency, so it short circuits the FET's drain at all other frequencies, especially the excitation frequency, ω_P. The gate-bias voltage in an efficient FET multiplier must be equal to or less than (more negative than) the threshold voltage V_t. Thus, the FET's channel conducts only during the positive half of the excitation cycle, and the drain conducts in pulses; the shape of the pulses is approximately a rectified cosine. The duty cycle of the pulses varies with the dc gate voltage: if $V_{gg} = V_t$, the duty cycle is 50%, but if $V_{gg} < V_t$, the FET is turned off over most of the excitation cycle. The duty cycle then is less than 50% [14].

Fig.2.12 shows the voltage and current waveforms of an ideal FET used as a frequency doubler. Due to the output resonator eliminates all voltage components except the one at the nth harmonic, the drain voltage $V_d(t)$ is a sinusoid at radian frequency $n\omega_p$. For best efficiency and output power, the drain voltage must vary between V_{max} and V_{min}. The drain current peaks at the value I_{max}, and the current pulses have the time duration t_0; $t_0 < T/2$, where T is the period of the excitation.

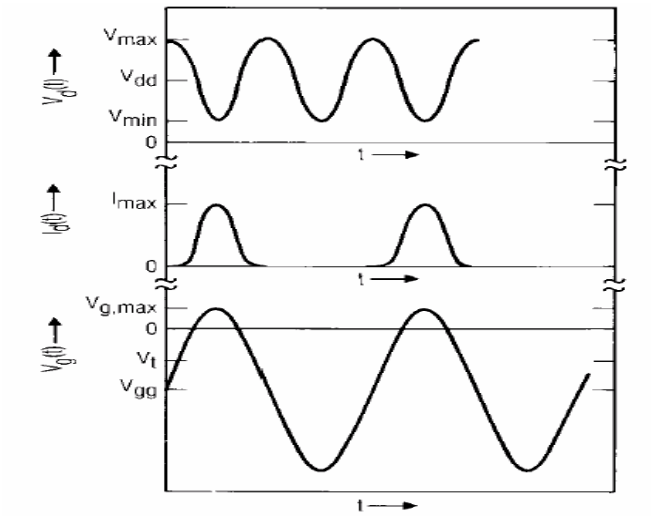


Figure 2.12 Voltage and current waveforms in an ideal FET frequency multiplier

Assuming that the current is maximum at t=0, the Fourier-series representation of the current has only cosine components:

$$I_d(t)=I_0+I_1\cos(\omega_p t)+I_2\cos(2\omega_p t)+..... \tag{2.23}$$

When $n \geq 1$, the coefficients are

$$I_n=I_{\max}\frac{4\cdot t_0}{\pi\cdot T}\left|\frac{\cos(n\pi\cdot t_0/T)}{1-(2n\cdot t_0/T)^2}\right| \tag{2.24}$$

and when n = 0 ,

$$I_n=I_{\max}\frac{2\cdot t_0}{\pi\cdot T} \tag{2.25}$$

When $t_0 / T = 0.5/n$, $n \neq 0$, (2.24) is indeterminate. Then, I_n is

$$I_n=I_{\max}\frac{t_0}{T} \tag{2.26}$$

Equation (2.24) shows that the FET multiplier has only means to maximize I_n , namely adjusting t_0 / T for achieving maximum output power and efficiency. Fig.2.13 shows a plot of I_n / I_{max} as a function of t_0 / T when n = 2 through n = 4; each of these curves has a clear maximum below $t_0 / T = 0.5$. It appears that, in order to achieve the optimum value of I_n , V_{gg} can be adjusted so that $I_d(t)$ has the desired period of conduction, t_0 .

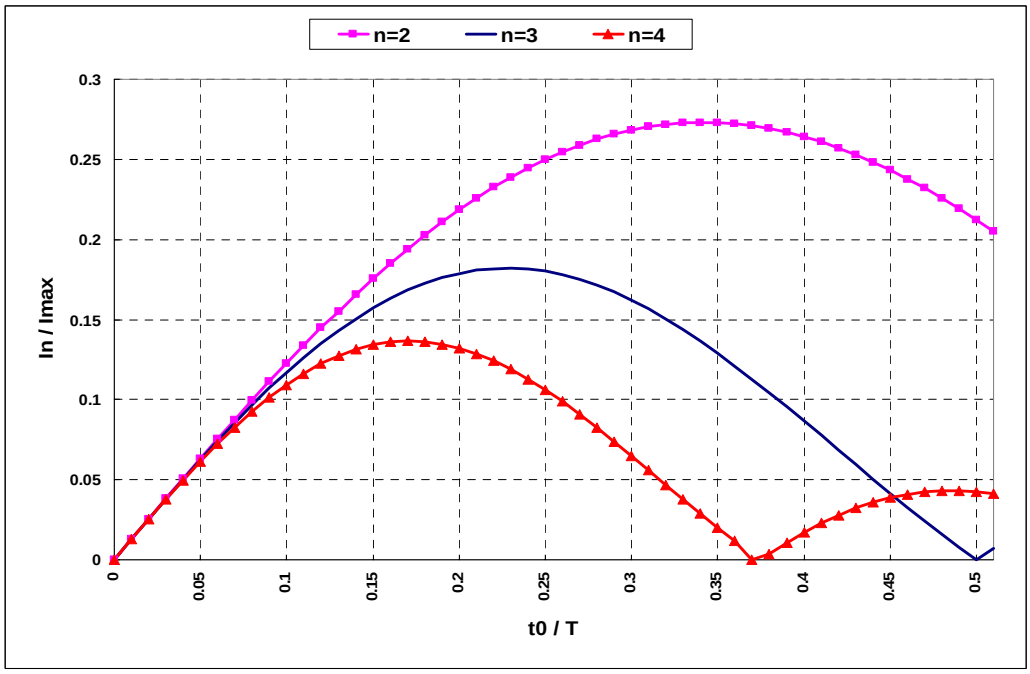


Figure 2.13 Harmonic drain-current components as a function of t_0 / T when the drain-current waveform is a half-sinusoidal pulse train

If the gate voltage varies between $V_{g,\max}$ and the peak reverse voltage $V_{g,\min}$, the phase angle θ_t, over which $V_g(t) > V_t$ is

$$\theta_t = 2a\cos\left(\frac{2V_t - V_{g,\max} - V_{g,\min}}{V_{g,\max} - V_{g.\min}}\right) \tag{2.27}$$

The bias voltage that achieves this value of θ_t is

$$V_{gg} = \frac{V_{g,\max} + V_{g,\min}}{2} \tag{2.28}$$

θ_t is sometimes called the conduction angle of the device.

Equation (2.27) shows that a large negative value of $V_{g,\min}$ decreases the conduction angle. It also shows that decreasing $V_{g,\max}$ has the same effect.

Chapter 3 Design and Measurement of Components

3.1 Design and Measurement of the I/Q Hybrid Mixer

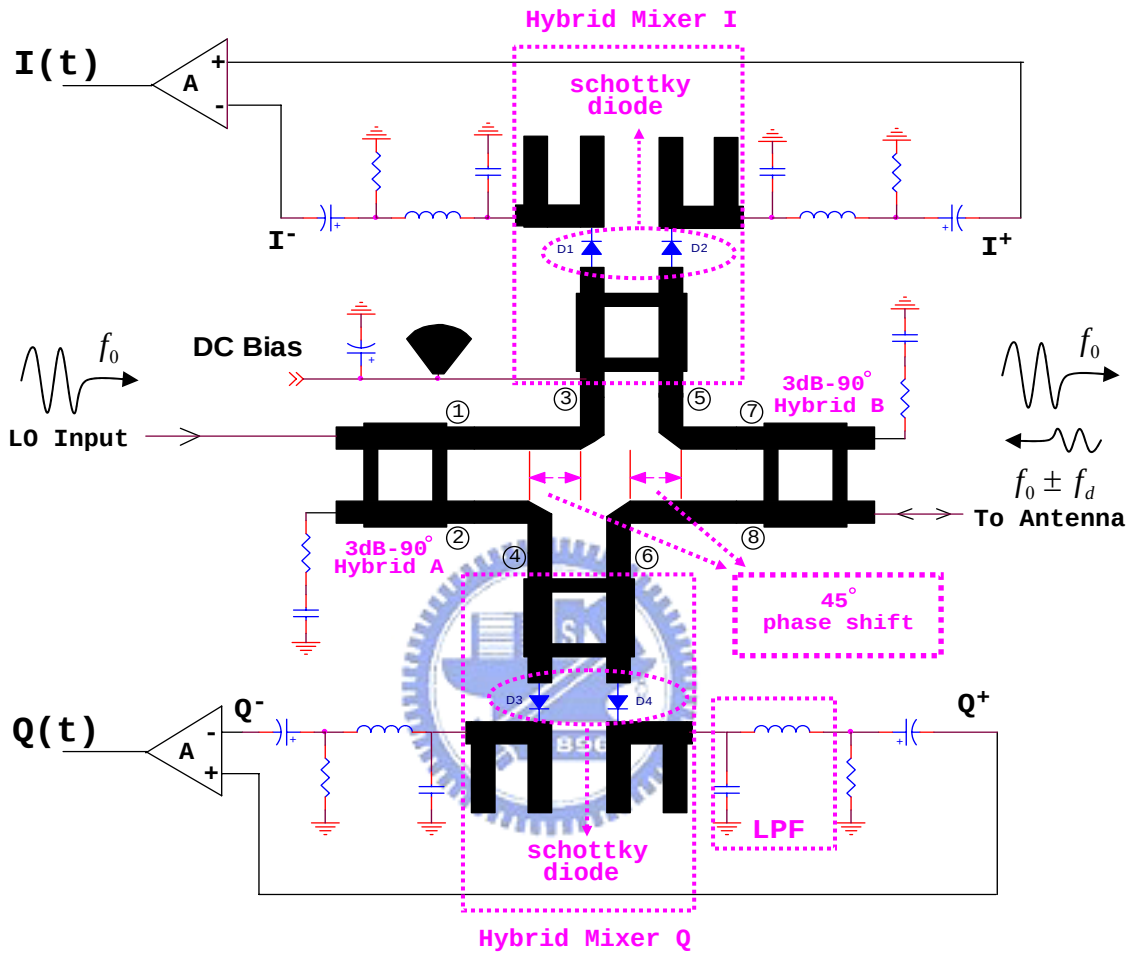


Figure 3.1 Schematic of the I/Q hybrid mixer using the MA4E2054-1141T

The I/Q hybrid mixer consists of two 90° hybrids, two hybrid mixers and two phase shifts of 45° in which are located between 90° hybrid A and hybrid mixer I ,and between hybrid mixer Q and 90° hybrid B respectively as shown in Fig.3.1. There are four 90° hybrids designed in the I/Q hybrid mixer using microstrip branch line circuitry in the frequency of 10.5GHz.M/A-COM MA4E2054-1141T schottky diode is used on the I/Q hybrid mixer and its configuration, spice model and circuit model are shown in Fig.3.2. The amplification of IF amplifiers is assumed to be 1000 using ADI OP213.

Let LO input voltage be a cosine wave of frequency f_0 :

$$v_{LO}(t)=V_{LO}\cos(2\pi\cdot f_0 t) \tag{3.1}$$

In operation, the I/Q hybrid mixer can be analyzed by transmitting signal path and receiving signal path as follows:

(1) Transmitting signal path

Since LO signal is connected to the input of the 90° hybrid A , the hybrid A will split LO signal into two equal amplitude with phase difference of 90° between point ① and point ② , and will be phase difference of 45° between point ③ and point ④ due to the phase shift of 45° as

$$\text{point ③ : } v_{LOI}(t)=V_{LOI}\cos(2\pi\cdot f_0 t-45^\circ+\phi_1) \tag{3.2}$$

$$\text{point ④ : } v_{LOQ}(t)=V_{LOQ}\cos(2\pi\cdot f_0 t-90^\circ+\phi_1) \tag{3.3}$$

, then pass through I/Q hybrid mixers with little attenuation and will be phase difference of 90° between point ⑦ and point ⑧ due to the phase shift of 45° as

$$\text{point ⑦ : } v_{LOI}(t)=V_{LOI}\cos(2\pi\cdot f_0 t-45^\circ+\phi_2) \tag{3.4}$$

$$\text{point ⑧ : } v_{LOQ}(t)=V_{LOQ}\cos(2\pi\cdot f_0 t-135^\circ+\phi_2) \tag{3.5}$$

Finally these two LO signals will be combined in-phase at the output of the hybrid B (antenna port) for radiation as

$$v_t(t)=V_0\cos(2\pi\cdot f_0 t+\phi_3) \tag{3.6}$$

(2) Receiving signal path

If the transmitter signal is given by (3.6)

the echo signal from a moving target will be

$$v_r(t) = k_1 V_0 \cos[(2\pi(f_0 \pm f_d)t + \phi] \tag{3.7}$$

where V_0 = amplitude of transmitter signal

k_1 = a constant determined from radar equation

f_0 = transmitter frequency, Hz

f_d = doppler frequency shift, Hz

ϕ = a constant phase shift, which depends upon range of initial detection

Once the echo signal is received from the antenna , the hybrid B will split the echo signal into two equal amplitude with phase difference of 90° between point ⑦ and point ⑧ , and will be phase difference of 45° between point ⑤ and point ⑥ due to the phase shift of 45° as

$$\text{point ⑤ :} \quad v_{RFI}(t) = V_{RFI}\cos[(2\pi(f_0 \pm f_d)t - 90^\circ + \phi_4] \tag{3.8}$$

$$\text{point ⑥ :} \quad v_{RFQ}(t) = V_{RFQ}\cos[(2\pi(f_0 \pm f_d)t - 45^\circ + \phi_4] \tag{3.9}$$

The received echo signal ($f_0 \pm f_d$) and the transmitter signal (f_0) heterodyne in the schottky diode to yield a difference signal and using differential amplifiers to produce I/Q channels respectively as

$$I(t)=V_{IFI}\cos(\pm 2\pi \cdot f_d t+\phi_5) \tag{3.10}$$

$$Q(t)=V_{IFQ}\cos(\pm 2\pi \cdot f_d t+90^\circ+\phi_5) \tag{3.11}$$

If the target is approaching (positive doppler), the outputs from I/Q channels are

$$I^+(t)=V_{IFI}\cos(2\pi \cdot f_d t+\phi_5) \qquad Q^+(t)=V_{IFQ}\cos(2\pi \cdot f_d t+90^\circ+\phi_5) \tag{3.12}$$

It means **I channel lag to Q channel for an approaching target.**

If the target is receding (negative doppler), the outputs from I/Q channels are

$$I^-(t)=V_{IFI}\cos(2\pi \cdot f_d t-\phi_5) \qquad Q^-(t)=V_{IFQ}\cos(2\pi \cdot f_d t-90^\circ-\phi_5) \tag{3.13}$$

It means **I channel lead to Q channel for a receding target**

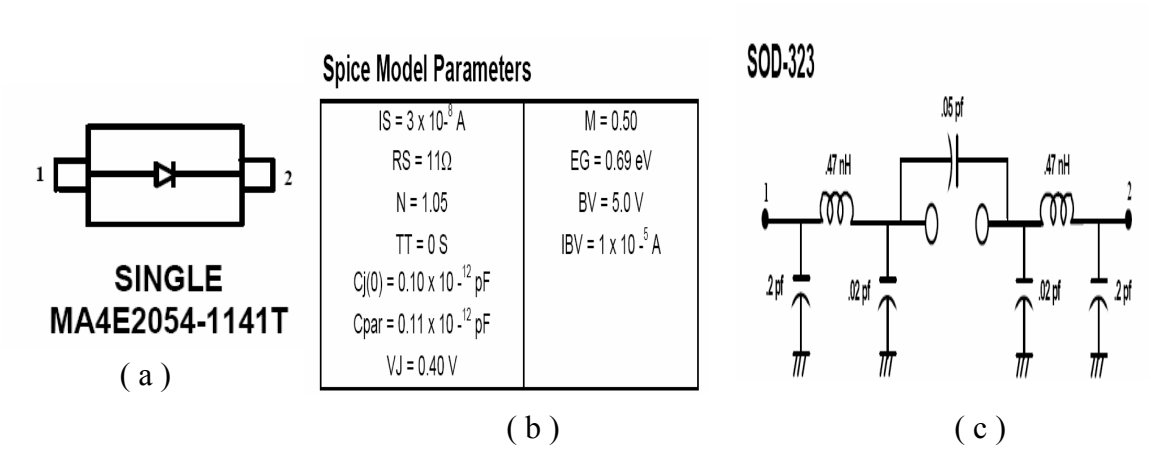


Figure 3.2 M/A-COM MA4E2054-1141T schottky diode for (a) configuration (b) spice model (c) circuit model

The MA4E2054-1141T schottky diode using spice model and circuit model is used on the simulation circuit of the I/Q hybrid mixer as shown in Fig.3.3. The simulation result of the insertion loss for the I/Q hybrid mixer is shown in Fig.3.4 that LO signal was set as frequency of 10.525GHz with power of 0dBm. Fig.3.5 shows the simulation result of the conversion loss for the I/Q hybrid mixer that RF, LO and relative IF signal was set as 10.535GHz with power of -30dBm , 10.525GHz with power of 0dBm and 10MHz respectively. The simulated conversion loss is the single-ended output from one of the IF outputs.

The measurement results of the insertion loss and conversion loss for various LO power are shown in Table 3.1 and Fig.3.6. The total loss has been calculated as the summation of the insertion loss and conversion loss. The measured conditions of the insertion loss and conversion loss are the same as the simulation conditions except that the LO power is variable from -4dBm to 14dBm. For measurement convenience, the measured conversion loss is the single-ended output from one of the IF outputs. The IF differential output has a theoretically 3dB improvement in the conversion loss.

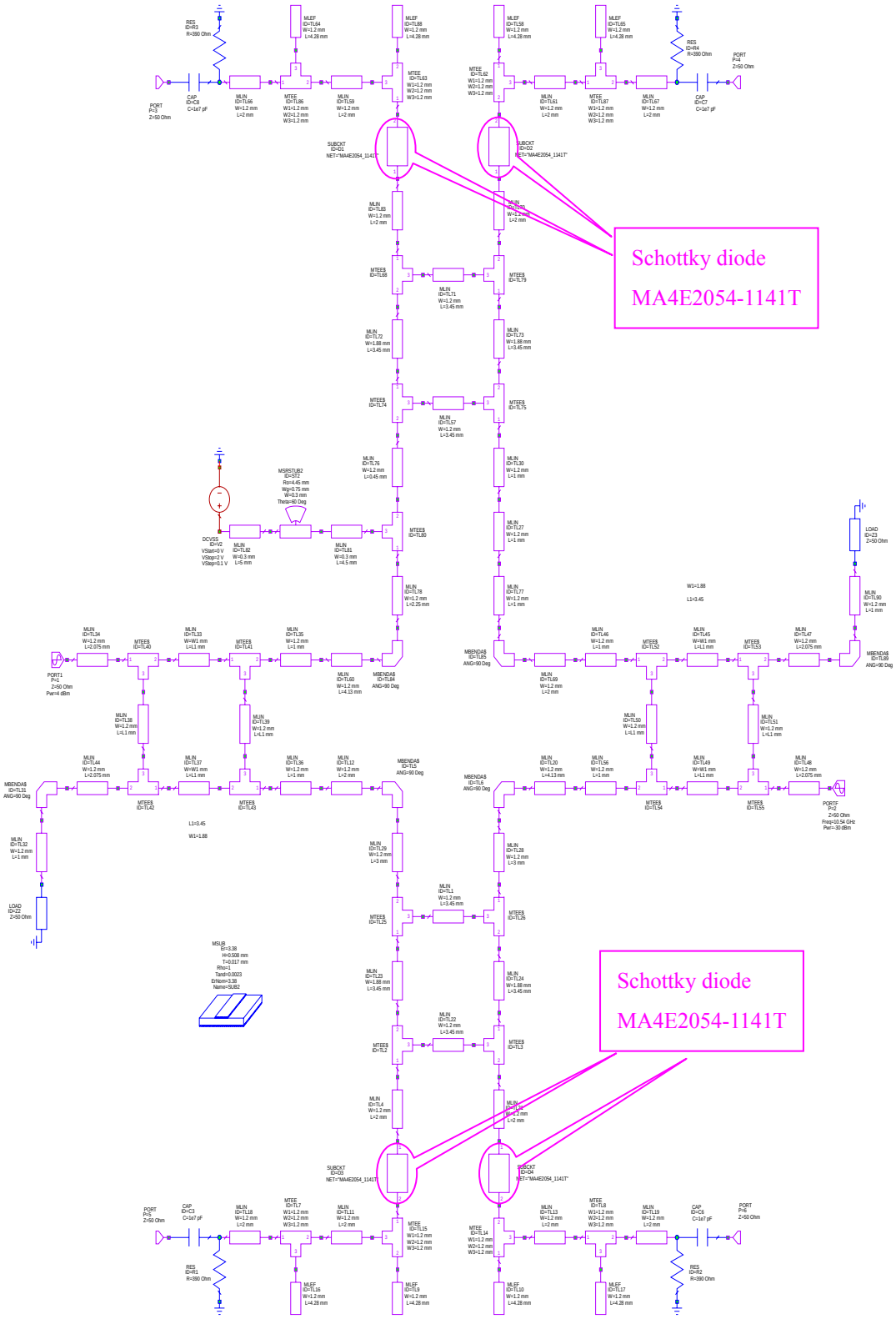


Figure 3.3 Simulation circuit of the I/Q Hybrid Mixer

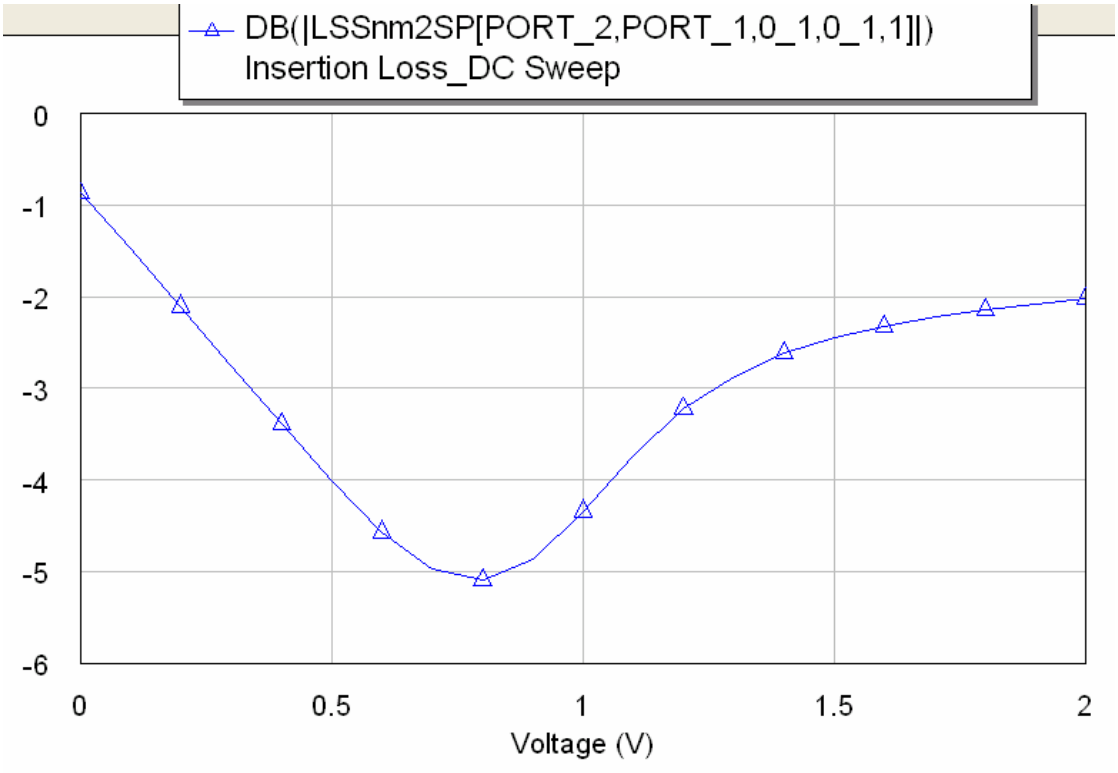


Figure 3.4 Simulation result of the insertion loss for the I/Q hybrid mixer with LO power of 0dBm

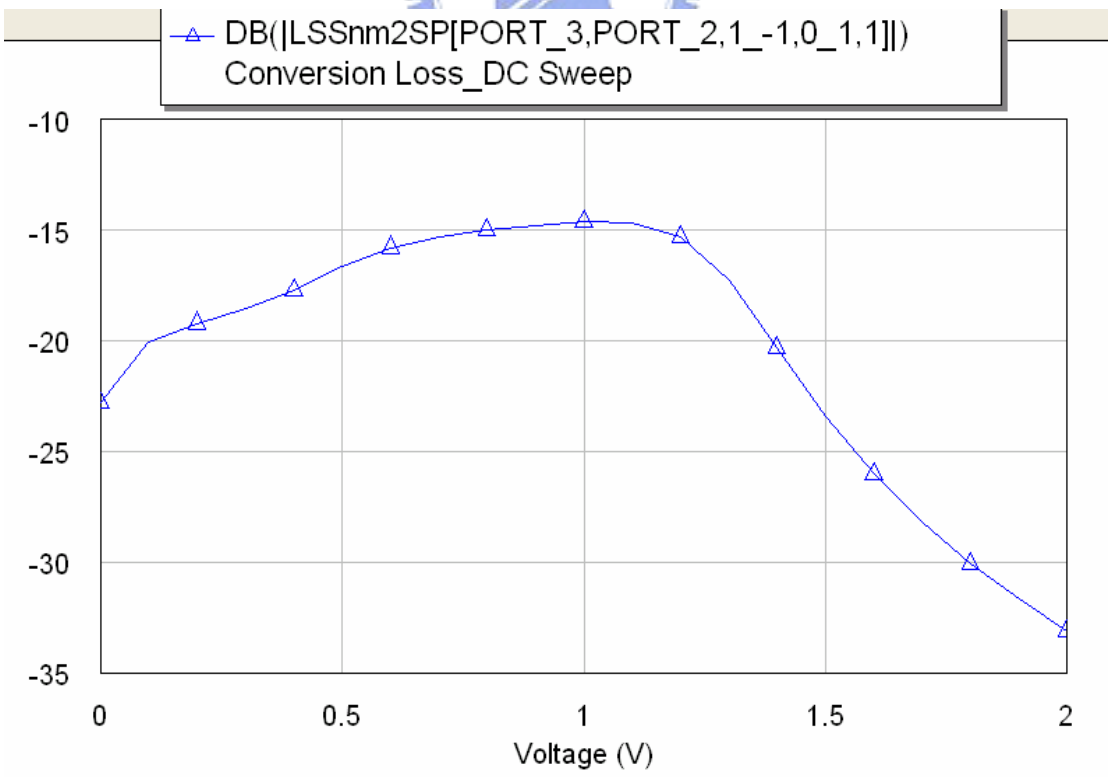
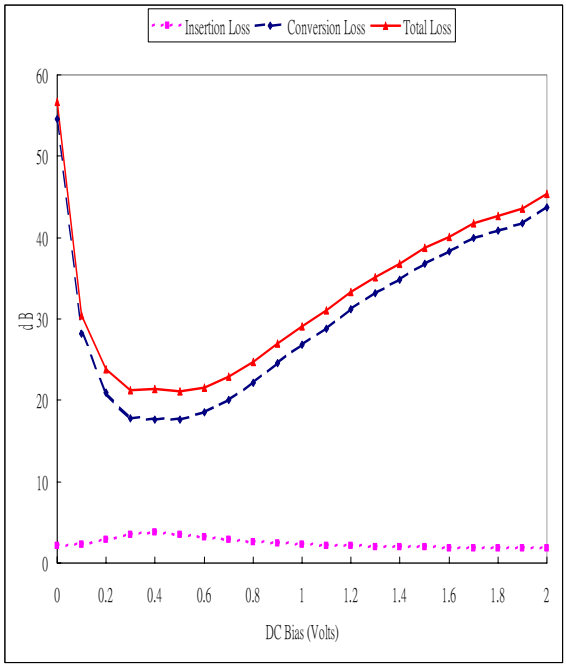


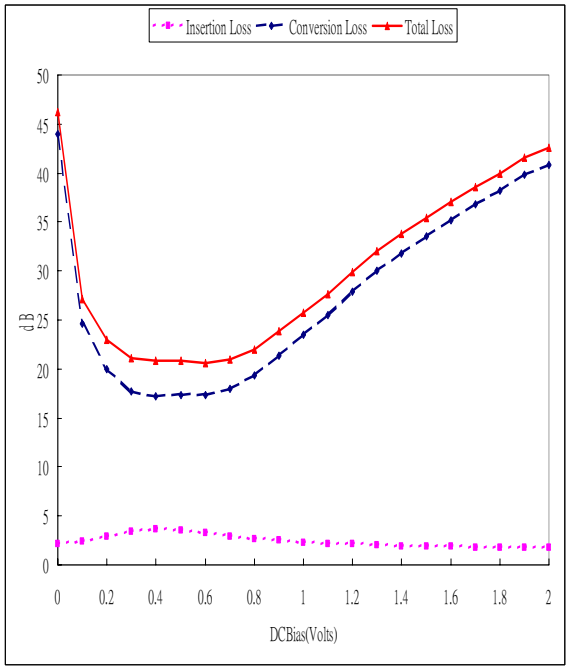
Figure 3.5 Simulation result of the conversion loss for the I/Q hybrid mixer with LO power of 0dBm

Table 3.1 Measurement results of the I/Q hybrid mixer for various LO power

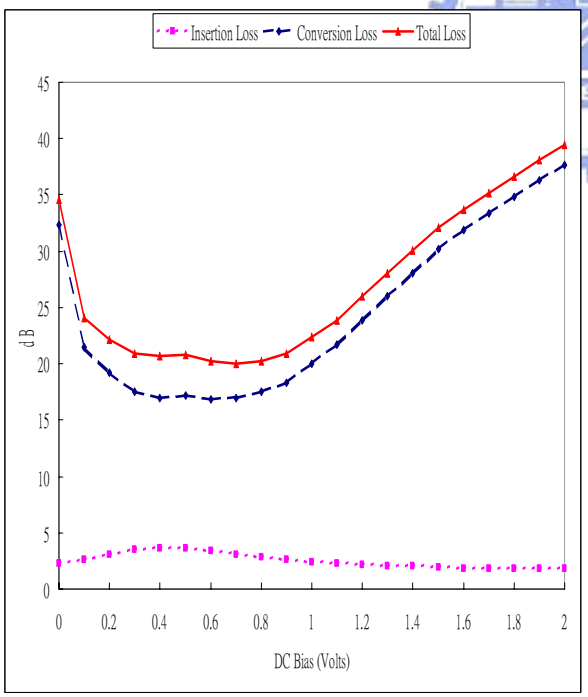
The Summary of I/Q Hybrid Mixer measurement results												
LO Power	Loss (dB)	DC Bias (V)										
		0	0.2	0.4	0.6	0.8	1	1.2	1.4	1.6	1.8	2
-4	Insertion Loss	2.15	2.83	3.7	3.12	2.6	2.28	2.1	1.93	1.83	1.76	1.77
	Conversion Loss	54.5	21	17.67	18.5	22.17	26.83	31.17	34.83	38.33	40.83	43.67
	Total Loss	56.65	23.83	21.37	21.62	24.77	29.11	33.27	36.76	40.16	42.59	45.44
-2	Insertion Loss	2.18	2.93	3.67	3.26	2.66	2.31	2.12	1.94	1.83	1.76	1.76
	Conversion Loss	44	20	17.17	17.33	19.33	23.5	27.83	31.83	35.17	38.17	40.83
	Total Loss	46.18	22.93	20.84	20.59	21.99	25.81	29.95	33.77	37	39.93	42.59
0	Insertion Loss	2.25	3.03	3.64	3.37	2.78	2.37	2.16	2.09	1.85	1.79	1.82
	Conversion Loss	32.33	19.17	17	16.83	17.5	20	23.83	28	31.83	34.83	37.67
	Total Loss	34.58	22.2	20.64	20.2	20.28	22.37	25.99	30.09	33.68	36.62	39.49
2	Insertion Loss	2.39	3.14	3.61	3.51	2.96	2.48	2.23	2.12	1.89	1.81	1.84
	Conversion Loss	24.5	18.67	17	16.83	16.5	17.5	19.67	23.33	27.5	31	34.67
	Total Loss	26.89	21.81	20.61	20.34	19.46	19.98	21.9	25.45	29.39	32.81	36.51
4	Insertion Loss	2.58	3.23	3.59	3.59	3.17	2.65	2.35	2.18	1.93	1.83	1.82
	Conversion Loss	21.17	18.17	17.17	16.83	16.33	16.33	17.17	18.83	22	25.67	29.5
	Total Loss	23.75	21.4	20.76	20.42	19.5	18.98	19.52	21.01	23.93	27.5	31.32
6	Insertion Loss	2.8	3.29	3.56	3.63	3.36	2.88	2.55	2.29	2.05	1.9	1.87
	Conversion Loss	19.67	18	17	16.83	16.33	16.17	16.5	16.67	17.83	19.83	23
	Total Loss	22.47	21.29	20.56	20.46	19.69	19.05	19.05	18.96	19.88	21.73	24.87
8	Insertion Loss	2.97	3.34	3.55	3.63	3.54	3.1	2.77	2.5	2.23	2.05	2
	Conversion Loss	19	17.83	17	16.83	16.5	16.17	16.17	16.17	16.33	16.83	18
	Total Loss	21.97	21.17	20.55	20.46	20.04	19.27	18.94	18.67	18.56	18.88	20
10	Insertion Loss	3.12	3.39	3.53	3.64	3.54	3.3	3.03	2.75	2.48	2.26	2.18
	Conversion Loss	18.5	17.67	17	16.83	16.67	16.33	16.17	16.17	16.17	16	16.33
	Total Loss	21.62	21.06	20.53	20.47	20.21	19.63	19.2	18.92	18.65	18.26	18.51
12	Insertion Loss	3.21	3.41	3.51	3.63	3.59	3.42	3.25	3.03	2.78	2.54	2.45
	Conversion Loss	18.17	17.67	17.17	17	16.67	16.5	16.33	16.17	16.17	16	16
	Total Loss	21.38	21.08	20.68	20.63	20.26	19.92	19.58	19.2	18.95	18.54	18.45
14	Insertion Loss	3.27	3.4	3.48	3.58	3.61	3.48	3.38	3.23	3.04	2.84	2.76
	Conversion Loss	18	17.67	17.17	17.17	16.83	16.67	16.5	16.5	16.33	16.17	16
	Total Loss	21.27	21.07	20.65	20.75	20.44	20.15	19.88	19.73	19.37	19.01	18.76



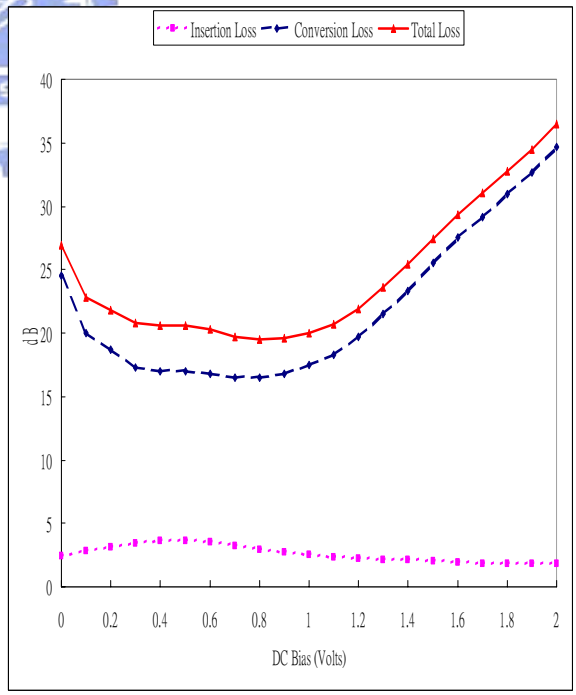
(a) LO = -4dBm



(b) LO = -2dBm

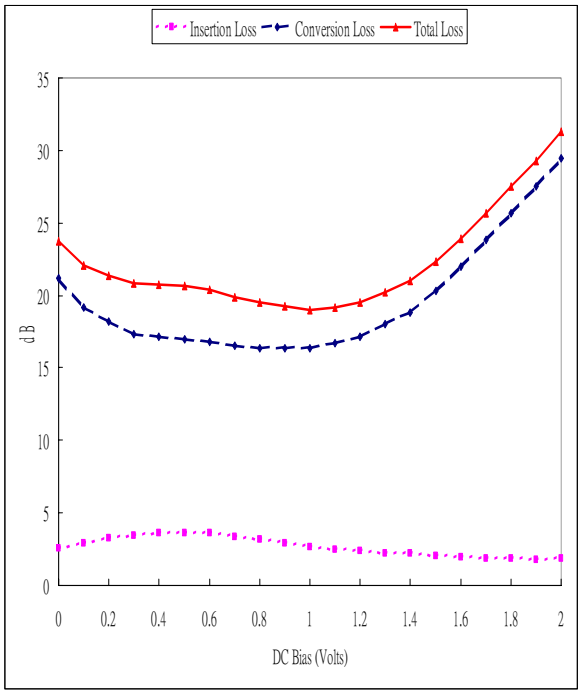


(c) LO = 0dBm

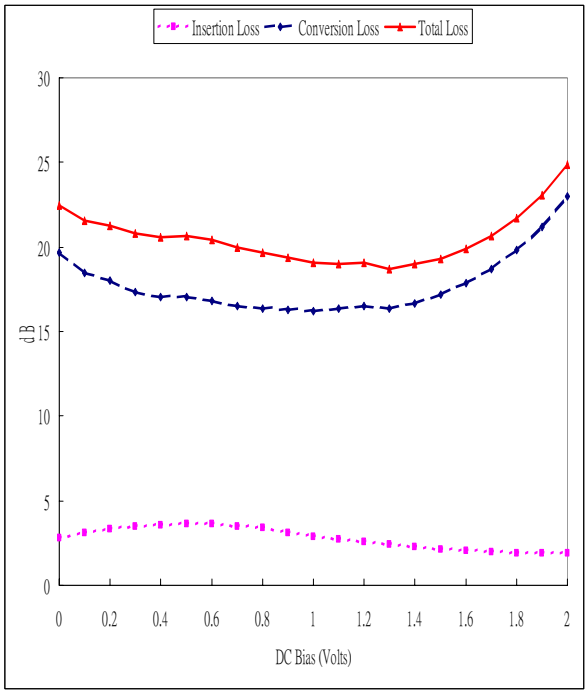


(d) LO = 2dBm

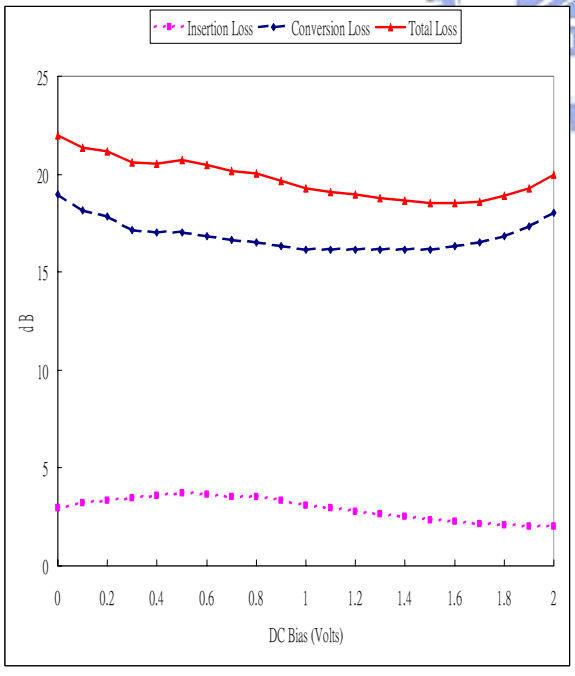
Figure 3.6 Measurement results of the I/Q hybrid mixer for various LO power



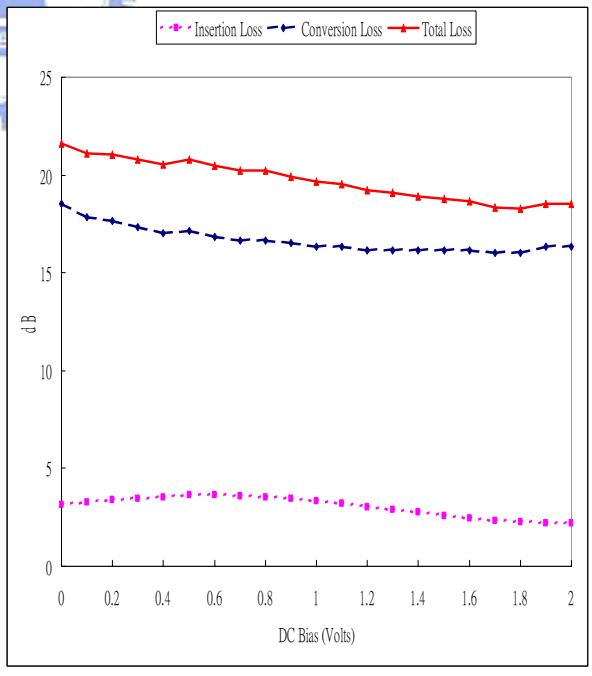
(e) LO = 4dBm



(f) LO = 6dBm

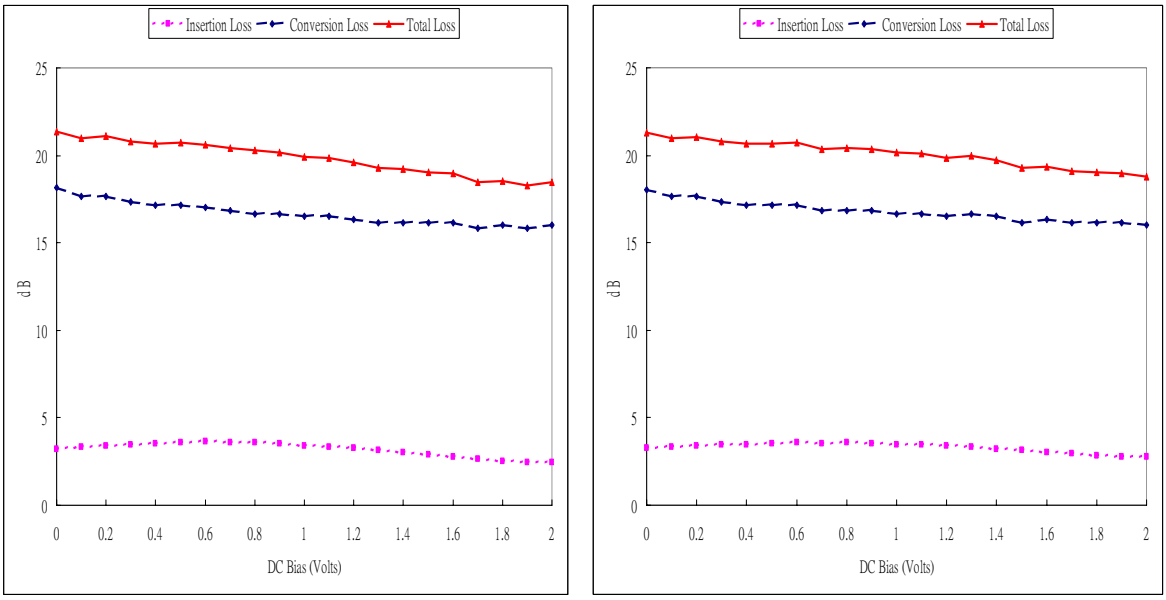


(g) LO = 8dBm



(h) LO = 10dBm

Figure 3.6(continued)



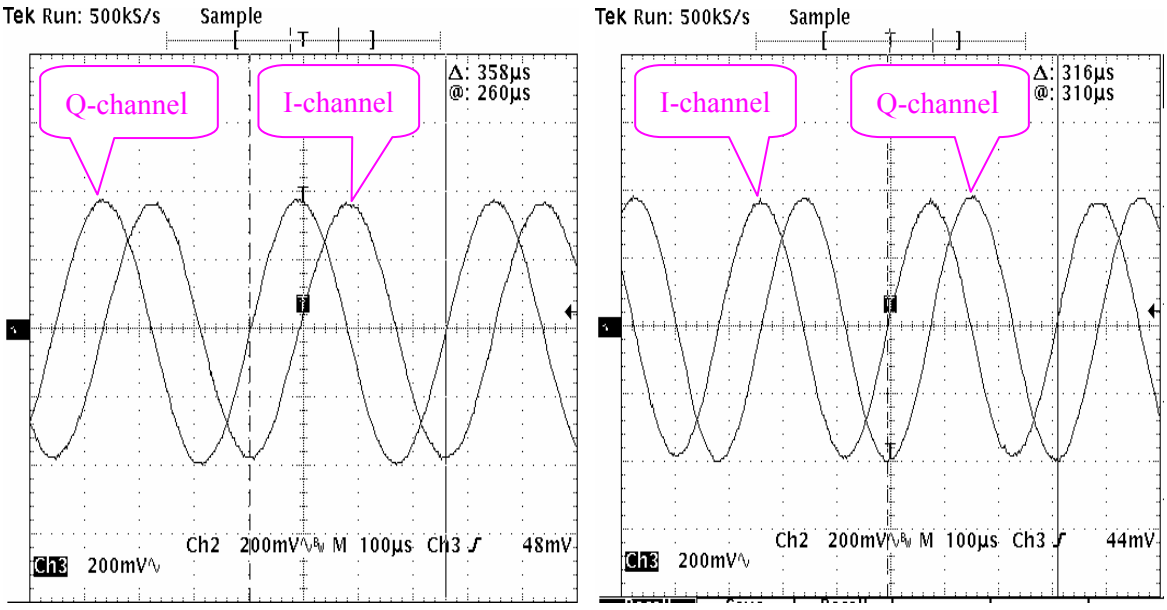
(i) LO =12dBm (j) LO = 14dBm

Figure 3.6(continued)

Table 3.2 The optimized results of the I/Q hybrid mixer for various LO power

LO Power (dBm)	Optimal DC bias (volts)	Conversion loss (dB)	Insertion loss (dB)	Total loss (dB)
-4	0.5	17.7	3.49	21.19
-2	0.6	17.33	3.26	20.59
0	0.7	17	3.05	20.05
2	0.8	16.5	2.96	19.46
4	1	16.33	2.65	18.98
6	1.3	16.33	2.38	18.71
8	1.5	16.17	2.34	18.51
10	1.8	16	2.26	18.26
12	1.9	15.83	2.83	18.66
14	2	16	2.76	18.76

The optimal performance can be obtained by minimizing the total loss for the hybrid I/Q mixer. Table3.2 shows the optimized result of the I/Q hybrid mixer for various LO power.



(a) Positive Doppler frequency (b) Negative Doppler frequency

Figure 3.7 Measurement results of I/Q channels

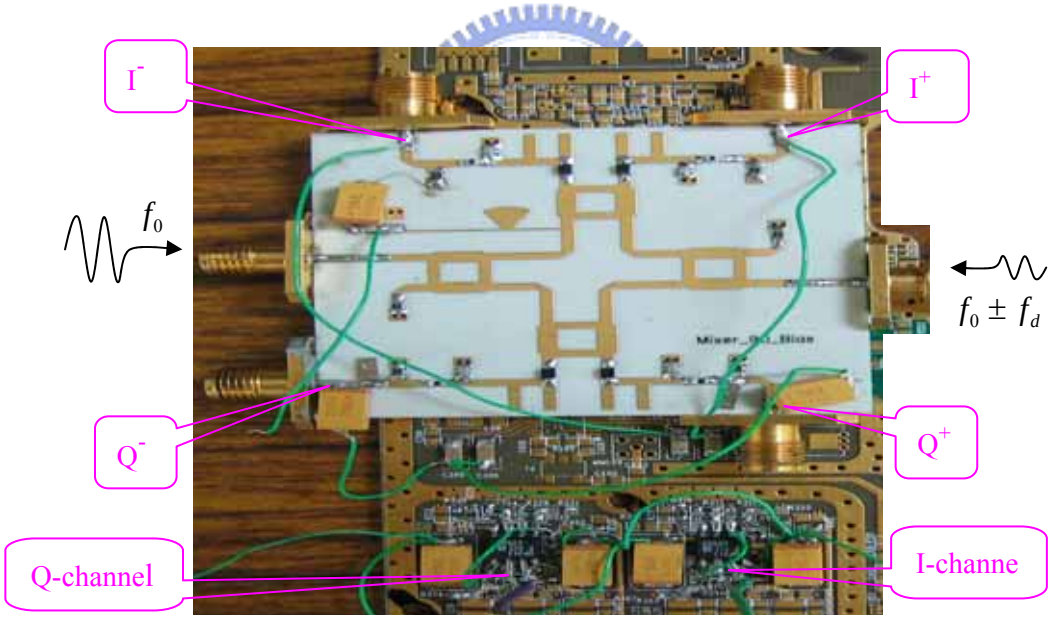
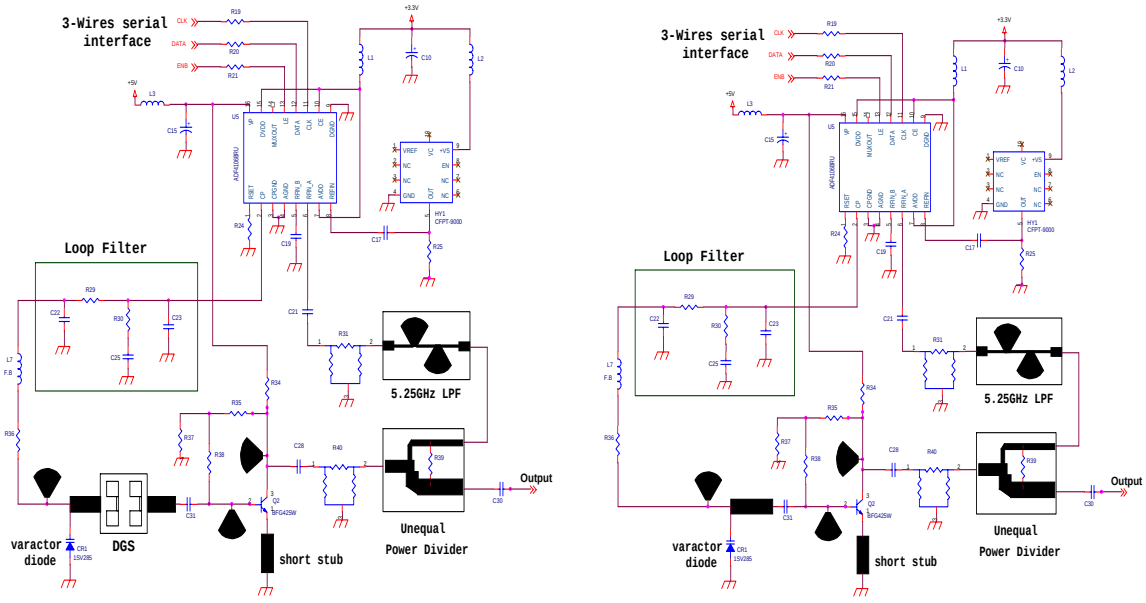


Figure 3.8 Photograph of the I/Q hybrid mixer

In order to manifest the performance of I/Q channels , LO signal (f_0) was set as 10.525GHz with power of 0 dBm , RF signal ($f_0 \pm f_d$) was set as 10.525GHz +/- 3KHz with power of -50 dBm and DC bias was 0.4 volts. Fig.3.7 shows the measurement results of I/Q channels. It appears that Q channel lead to I channel for positive Doppler shift (an approaching target) ; conversely, I channel lead to Q channel for negative Doppler shift (a receding target) . Fig.3.8 shows the photograph of the I/Q hybrid mixer.

3.2 5.25GHz PLL Frequency Synthesizer with and without DGS



(a) with DGS (b) without DGS

Figure 3.9 Schematic of 5.25GHz PLL Frequency Synthesizer

Defected Ground Structure (DGS) has been proposed and demonstrated to reduce the phase noise of oscillators [15]. Fig.3.9 shows the schematic of 5.25GHz PLL frequency synthesizer with and without DGS which both of them have been fabricated and measured simultaneously to verify the performance of the DGS. The 5.25GHz PLL frequency synthesizer consists of a Voltage Controlled Oscillator (VCO), an unequal power divider, a low pass filter (LPF), a synthesizer IC and a loop filter. The ADF4106 integer-N frequency synthesizer is the form of current output and is controlled by 3-wire serial interface. The loop bandwidth of the loop filter is assumed to be 2.5 KHz.

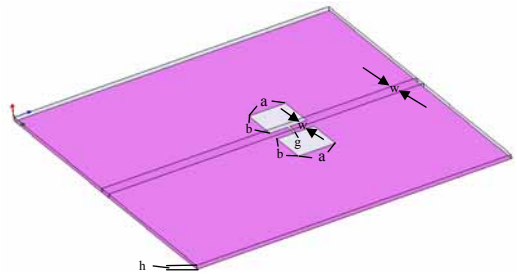
Section 3.2.1 shows the photographs and the results of simulation and measurement for the one-section, two-section and three-section DGS respectively that the 3dB cut-off frequency is designed as around 5.2GHz. In this thesis, two-section DGS has been adopted to reduce the phase noise of oscillator that is a compromise between the electric performance and the circuit size.

3.2.1 Simulation and Measurement of the DGS

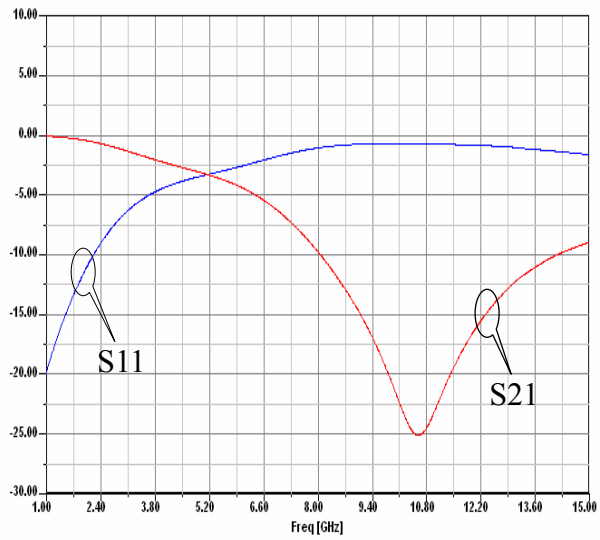
A. One-section DGS

a=b=3.5mm ; g=0.2mm ; W=1.15mm

RO4003 ε_r =3.38 ; h=0.508mm



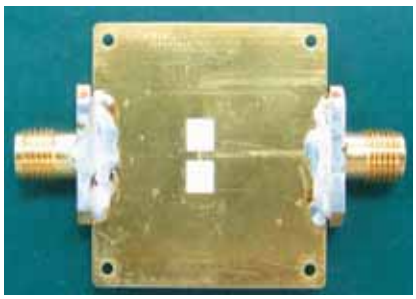
(a)



(b)

Figure 3.10 EM-simulation of the one-section DGS (a) 3-D view; (b) result

(a) Top side



(b) Bottom side

Figure 3.12 Photograph of the one-section DGS

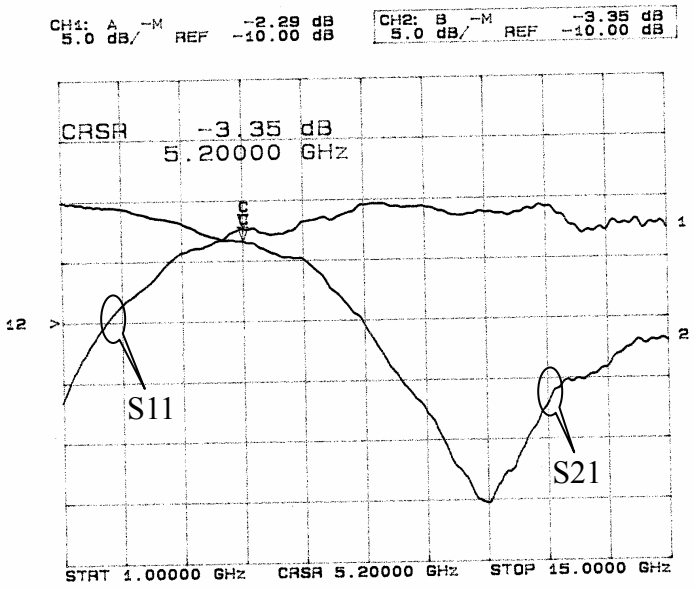
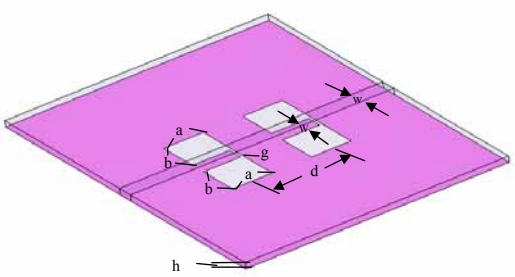
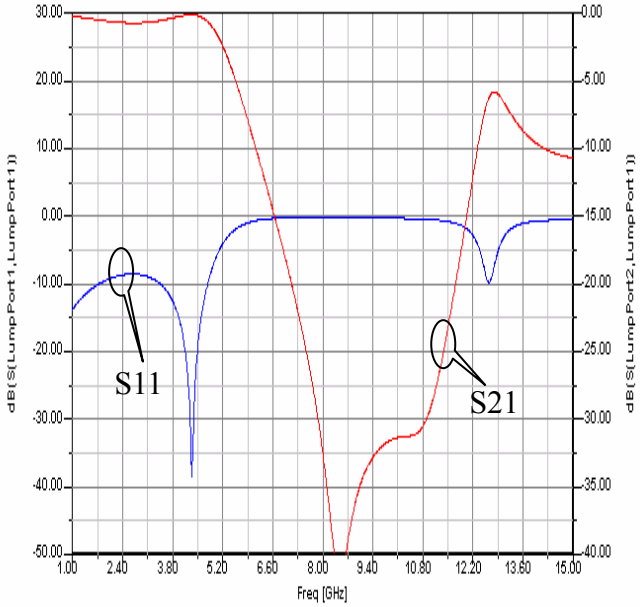


Figure 3.11 Measurement result of the one-section DGS

B. Two-section DGS

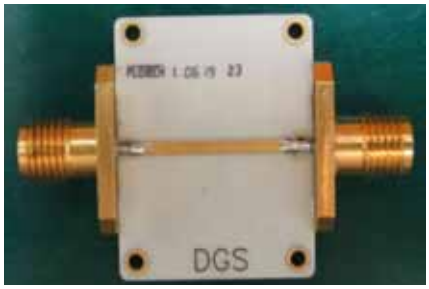
a=b=3mm ; g=0.2mm ; W=1.15mm
d=6mm ; h=0.508mm
RO4003 ε_r =3.38



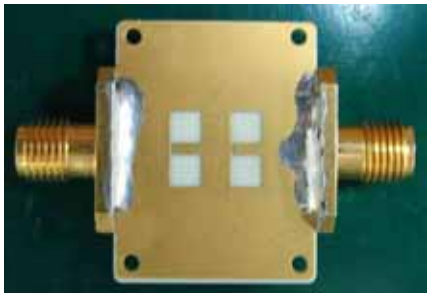


(a) (b)

Figure 3.13 EM-simulation of the two-section DGS (a) 3-D view; (b) result



(a) Top side



(b) Bottom side

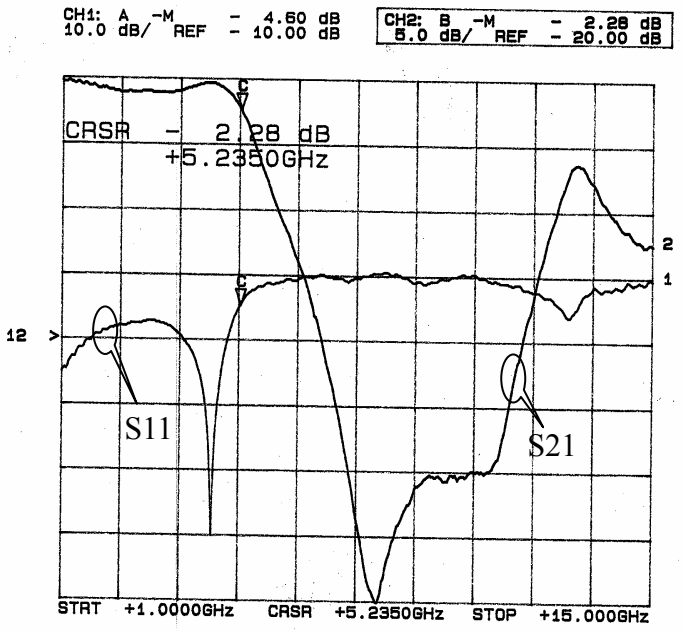


Figure 3.14 Measurement result of the two-section DGS

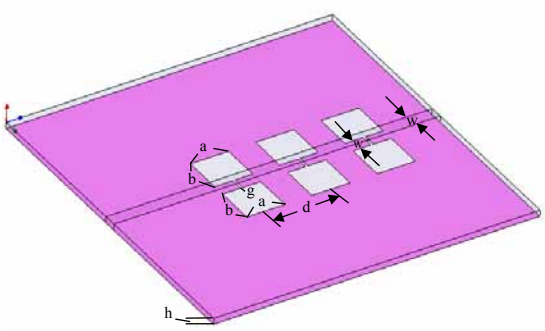
Figure 3.15 Photograph of the two-section DGS

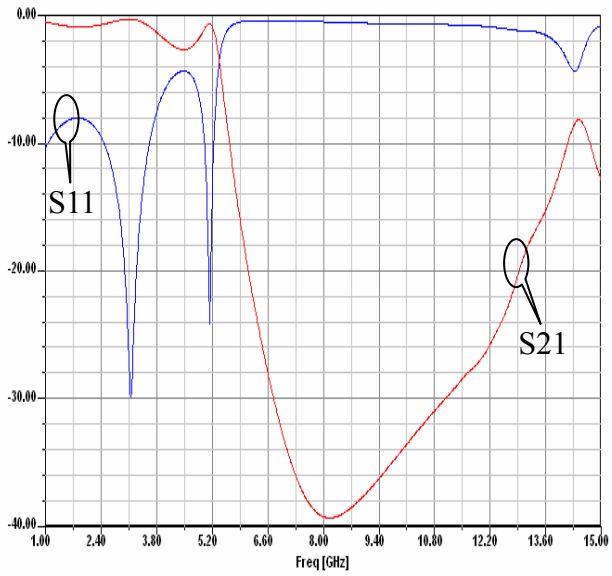
C. Three-section DGS

a=b=3.5mm ; g=0.2mm ; W=1.15mm

d=6mm ; h=0.508mm

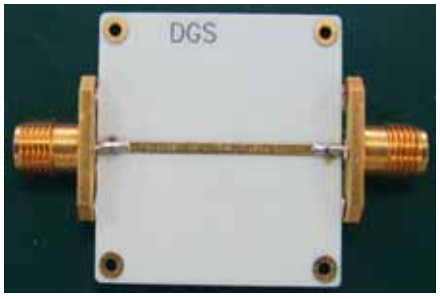
RO4003 ε_r=3.38



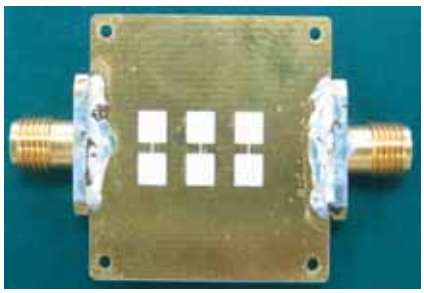


(a) (b)

Figure 3.16 EM-simulation of the three-section DGS (a) 3-D view; (b) result



(a) Top side



(b) Bottom side

Figure 3.18 Photograph of the three-section DGS

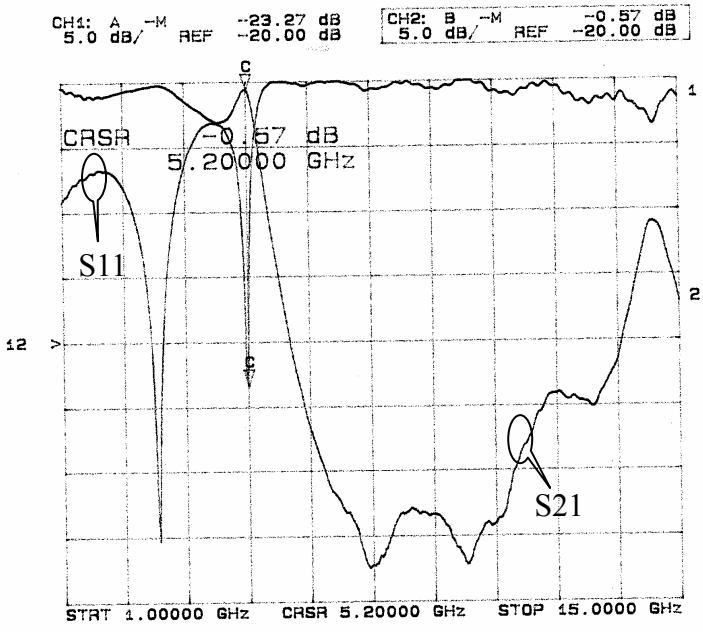


Figure 3.17 Measurement result of the three-section DGS

The method of modeling the DGS had been presented in section 2.3. Following up this method, the equivalent circuit of the two-section DGS can be modeled as the π-type symmetrical two-port circuit as shown in Fig.3.19.

Fig.3.20 shows the simulation result for the equivalent circuit of the two-section DGS that is very similar to EM-simulation result as shown in Fig. 3.13(b).

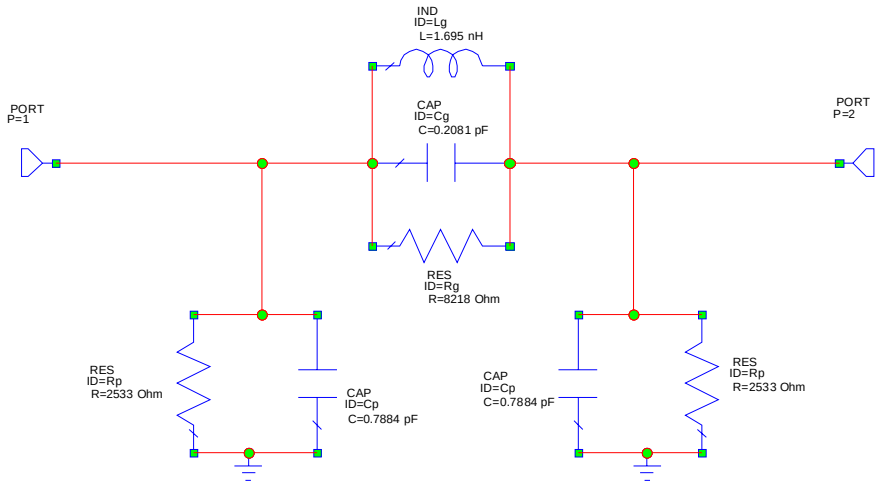


Figure 3.19 The equivalent circuit of the two-section DGS

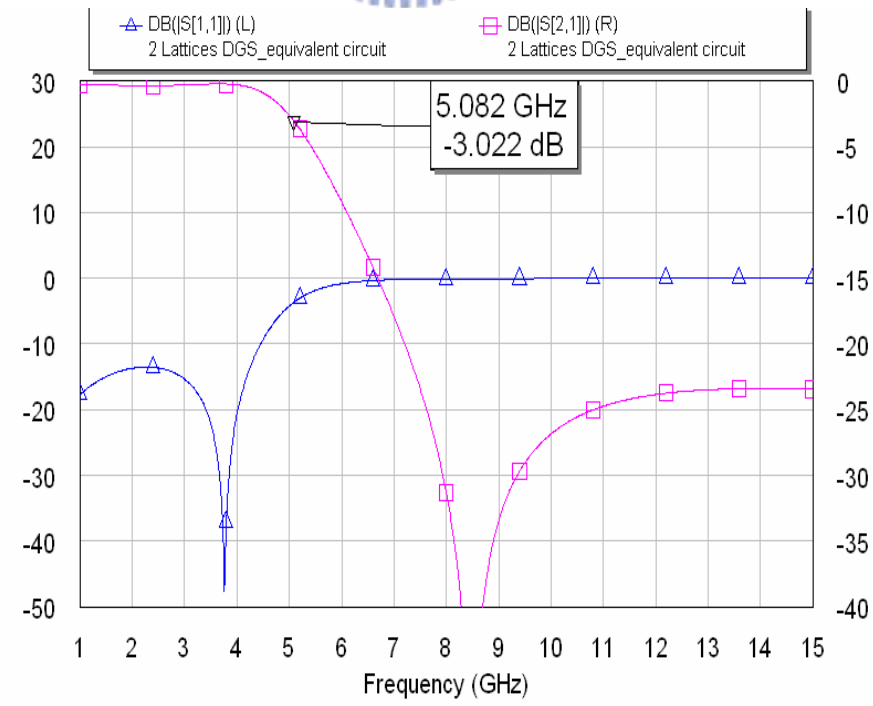
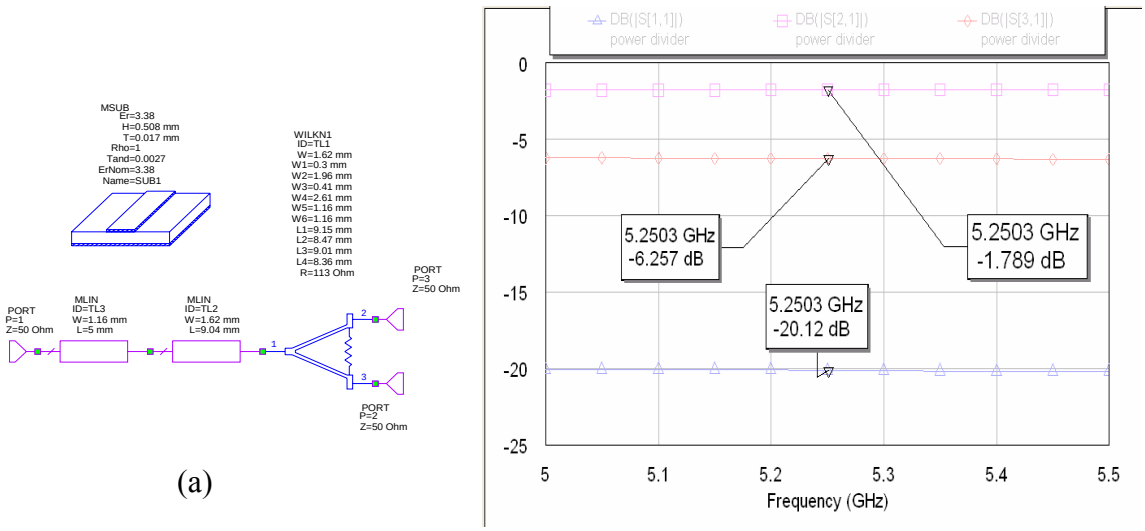


Figure 3.20 Simulation result for the equivalent circuit of the two-section DGS

3.2.2 Simulation and Measurement of 5.25GHz Unequal Power Divider



(a) (b)

Figure 3.21 Simulation of 5.25GHz unequal power divider (a) schematic; (b) result

Figure 3.22 Photograph of 5.25GHz unequal power divider

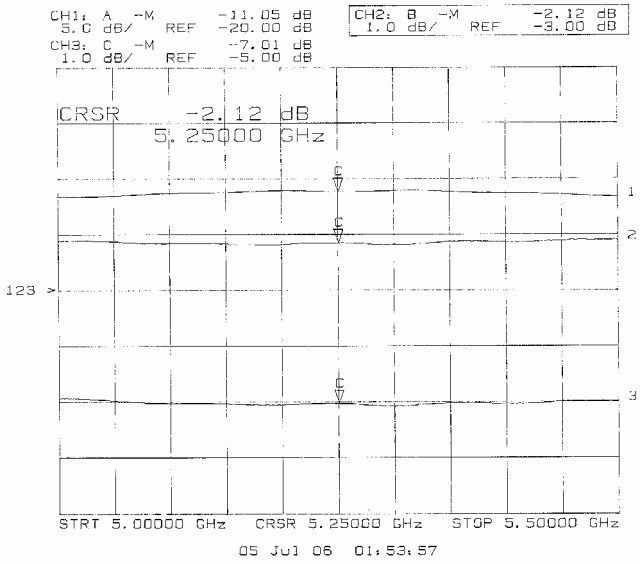


Figure 3.23 Measurement result of 5.25GHz unequal power divider

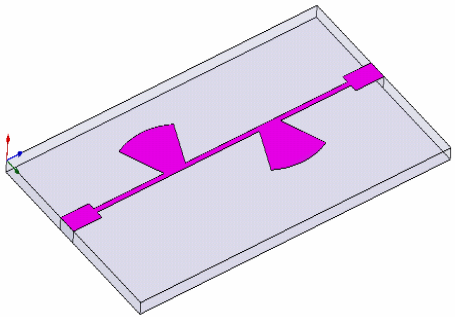
An unequal power divider can be designed using the factor k^2-output power ratio [16]. In this thesis, the output power ratio of 5.25GHz unequal power divider is assumed to be 3:1. The simulation and measurement results of the S-parameters S_{21}, S_{31} of show as 1.78dB, 6.25dB and 2.12dB, 7.01dB as shown in Fig.3.21 and Fig3.23 respectively.

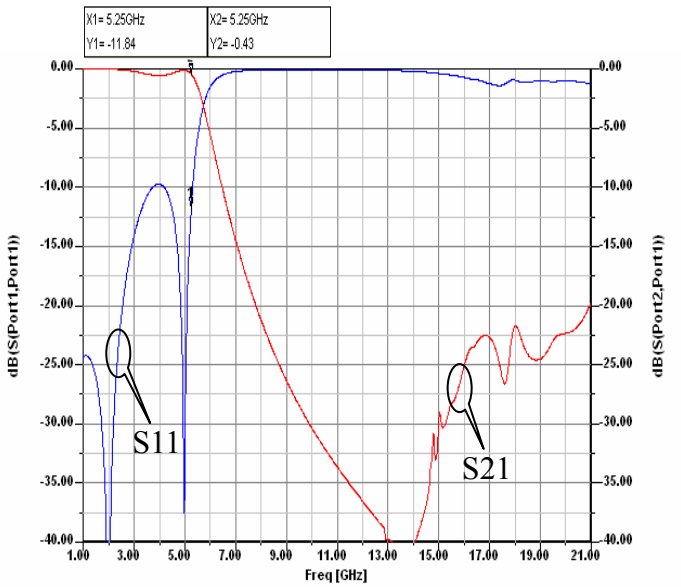
3.2.3 Simulation and Measurement of 5.25GHz Low Pass Filter

PCB :

RO4003 ε_r=3.38 with

0.508 mm thickness





(a) (b)

Figure 3.24 EM-simulation of 5.25GHz LPF (a) 3-D view; (b) result

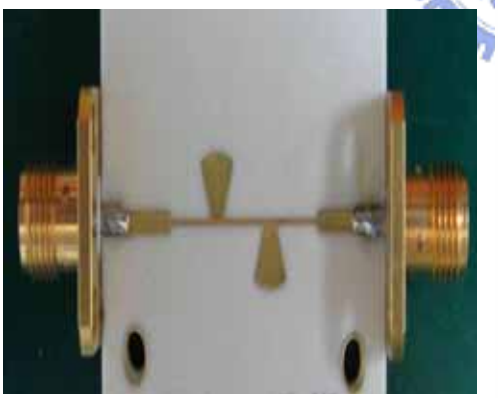


Figure 3.25 Photograph of 5.25GHz LPF

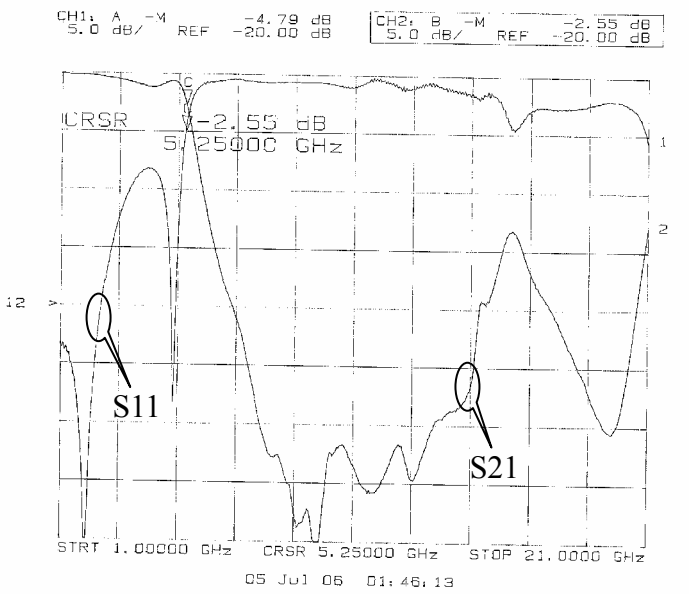


Figure 3.26 Measurement result of 5.25GHz LPF

5.25GHz Low Pass Filter (LPF) using microstrip line circuitry was used in order to obtain a pure signal at the RF input of ADF4106. The results of EM-simulation and measurement for 5.25GHz LPF are shown in Fig.3.24 and Fig.3.26 respectively.

3.2.4 Simulation and Measurement of 5.25GHz VCO with and without DGS

A. Simulation of the negative-impedance circuit

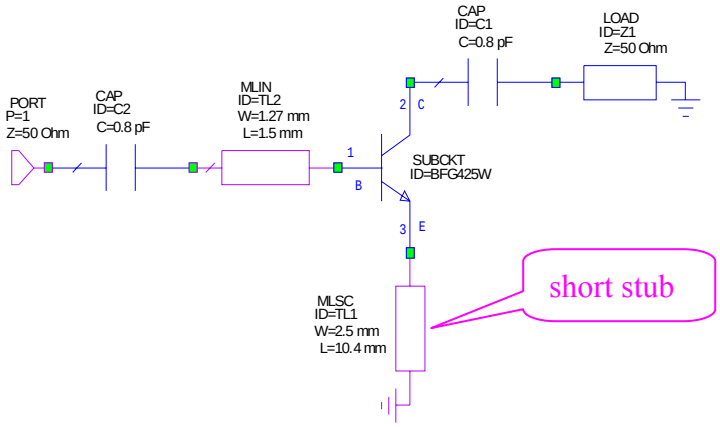


Figure 3.27 Schematic of the negative-impedance using the BFG425W

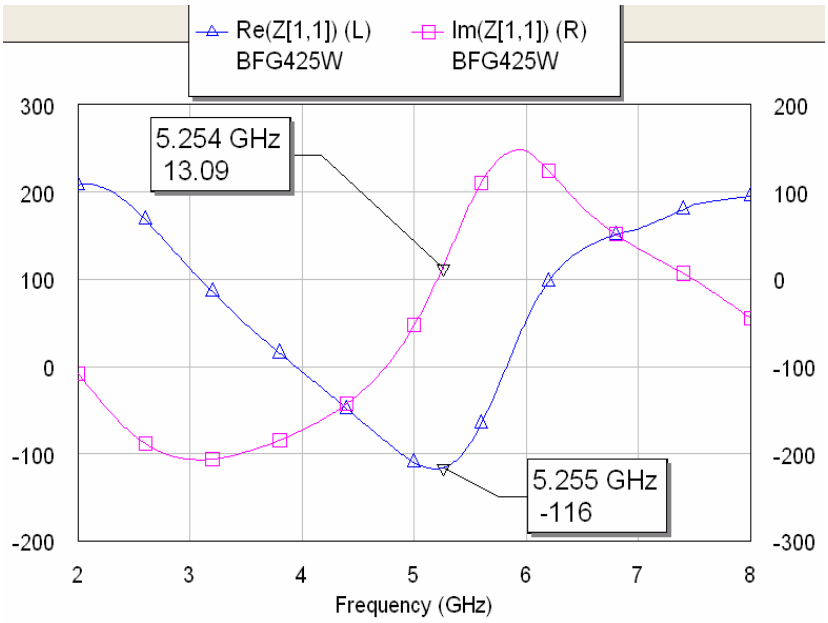


Figure 3.28 Simulation result of the negative-impedance circuit

The bipolar transistor BFG425W (Philips) is used to act as the active device on the circuit of 5.25GHz VCO.A short stub was connected to the emitter of the BFG425W in order to obtain a negative real part of input impedance as shown in Fig.3.27. Simulation result of the negative-impedance circuit is shown in Fig.3.28.

B. Simulations of the resonator with and without DGS

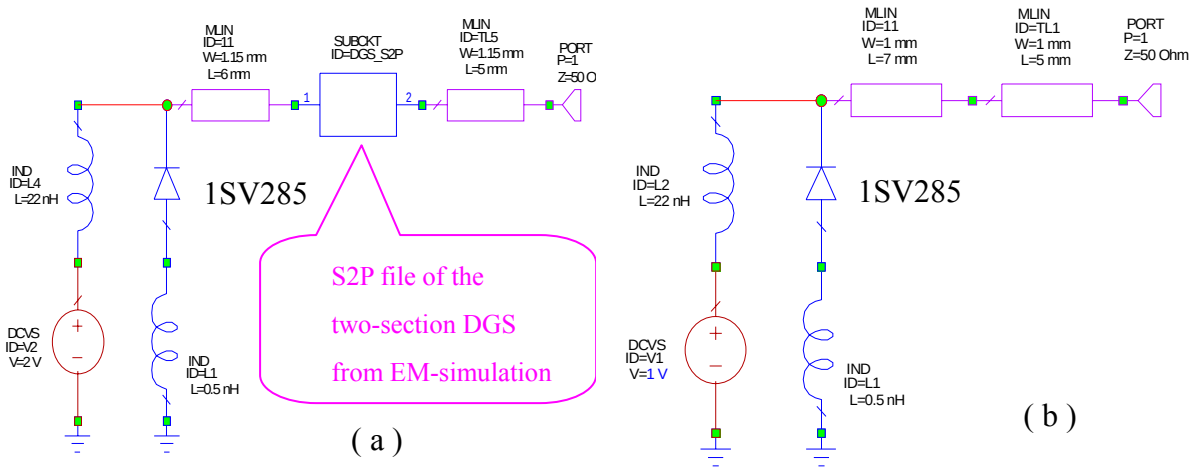
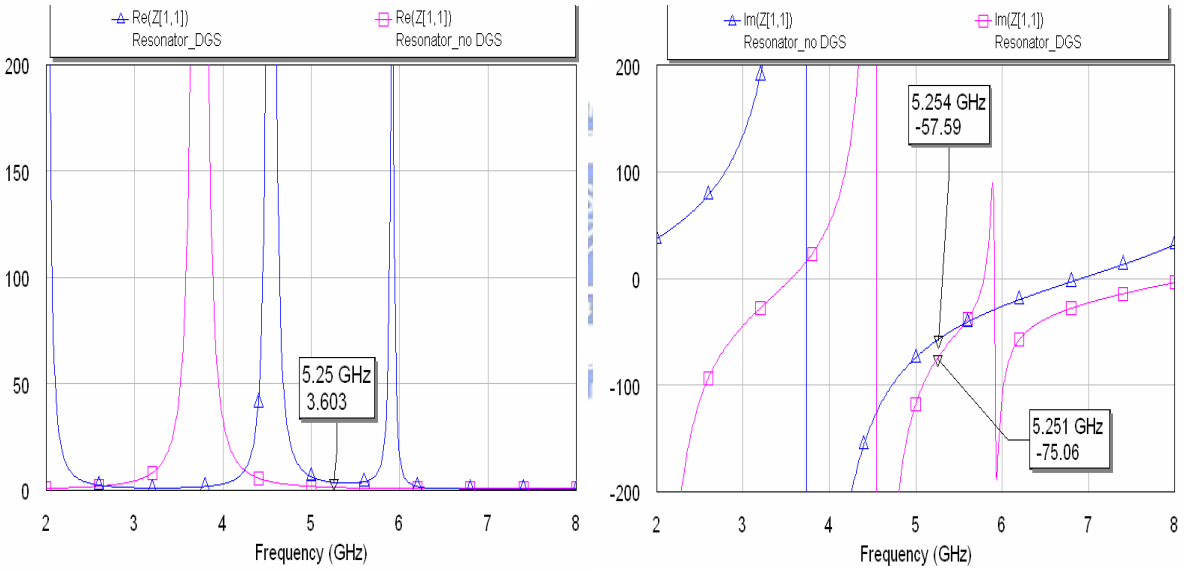


Figure 3.29 Schematic of the resonator (a) with DGS (b) without DGS



(a) real part of input impedance (b) imaginary part of input impedance

Figure 3.30 Simulation results of the resonator with and without DGS

TOSHIBA 1SV285 varactor diode is used on the resonator of 5.25GHz VCO as shown in Fig.3.29 In the circuit of the resonator with DGS, the S2P file of the two-section DGS is extracted from EM-simulation. Fig.3.30 shows the simulation results of the resonator with and without DGS that the imaginary part of the resonator with DGS has higher slope than the imaginary part of the resonator without DGS. It implies that the resonator with DGS has a higher quality factor.

C. Measurement result of 5.25GHz VCO with DGS

Table 3.3 Measurement result of 5.25GHz VCO with DGS

Vt (V)	f0 (MHz)	outptu power(dBm)	Sensitivity(MHz/V)	
0	5181	5.5	44	
0.5	5204	5.5		
1	5225	5.5		47
1.5	5248	5.67		
2	5272	5.67	54	
2.5	5297	5.67		
3	5326	5.83		64
3.5	5357	6		
4	5390	6.33	59	
4.5	5423	6.5		
5	5449	6.67		

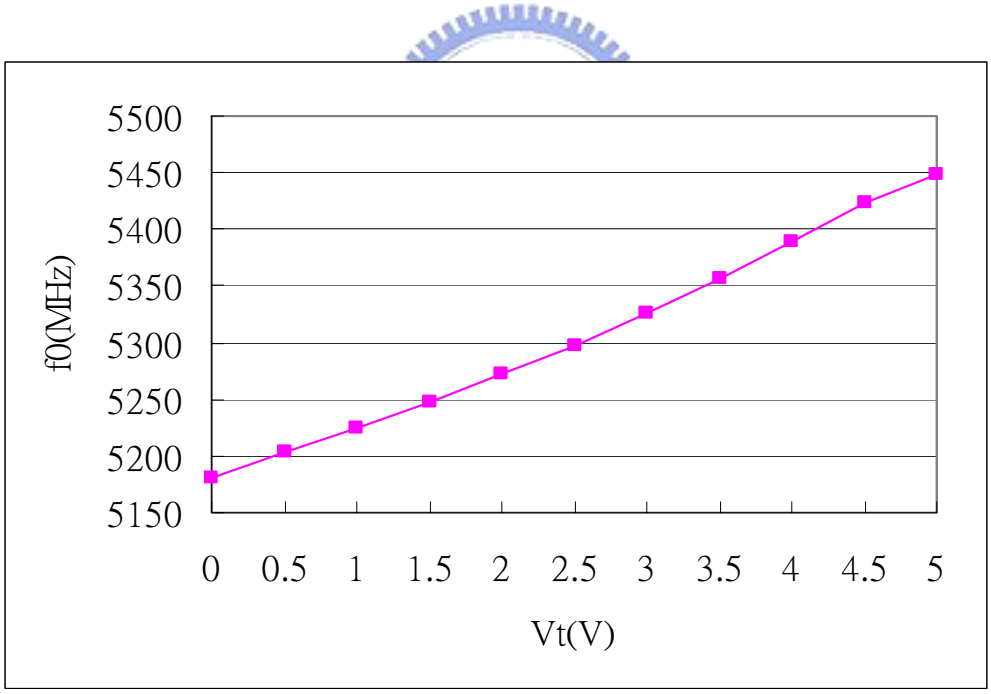


Figure 3.31 The curve of Frequency vs. Tuning Voltage for 5.25GHz VCO with DGS

The performance of 5.25GHz VCO with DGS has been measured as shown in Table3.3. Fig.3.31 shows the curve of Frequency vs. Tuning Voltage for 5.25GHz VCO with DGS.

D. Measurement result of 5.25GHz VCO without DGS

Table 3.4 Measurement result of 5.25GHz VCO without DGS

Vt (V)	f0 (MHz)	outptu power(dBm)	Sensitivity(MHz/V)	
0	5189	5	31	
0.5	5205	5.33		
1	5220	5.33		30
1.5	5235	5.33		
2	5250	5.5	33	
2.5	5266	5.5		
3	5283	5.5		39
3.5	5302	5.5		
4	5322	5.5	40	
4.5	5344	5.67		
5	5362	5.67		

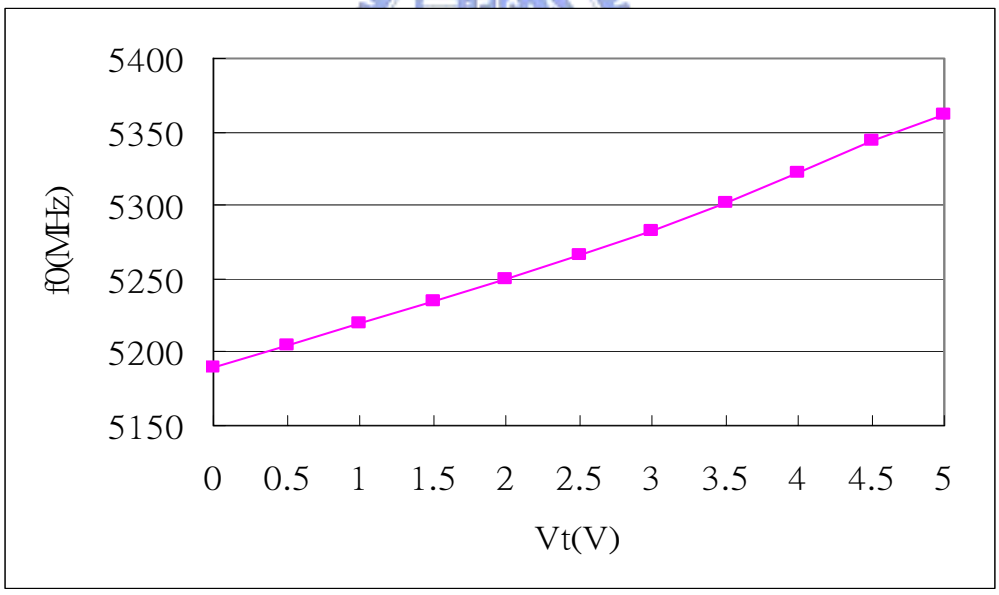
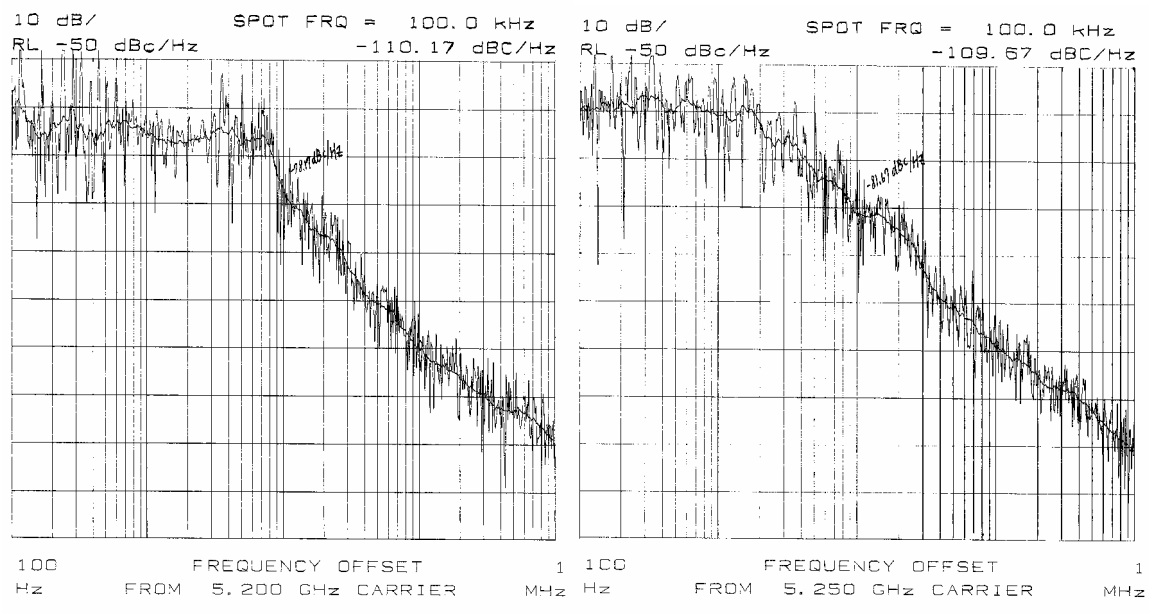


Figure 3.32 The curve of Frequency vs. Tuning Voltage for 5.25GHz VCO without DGS

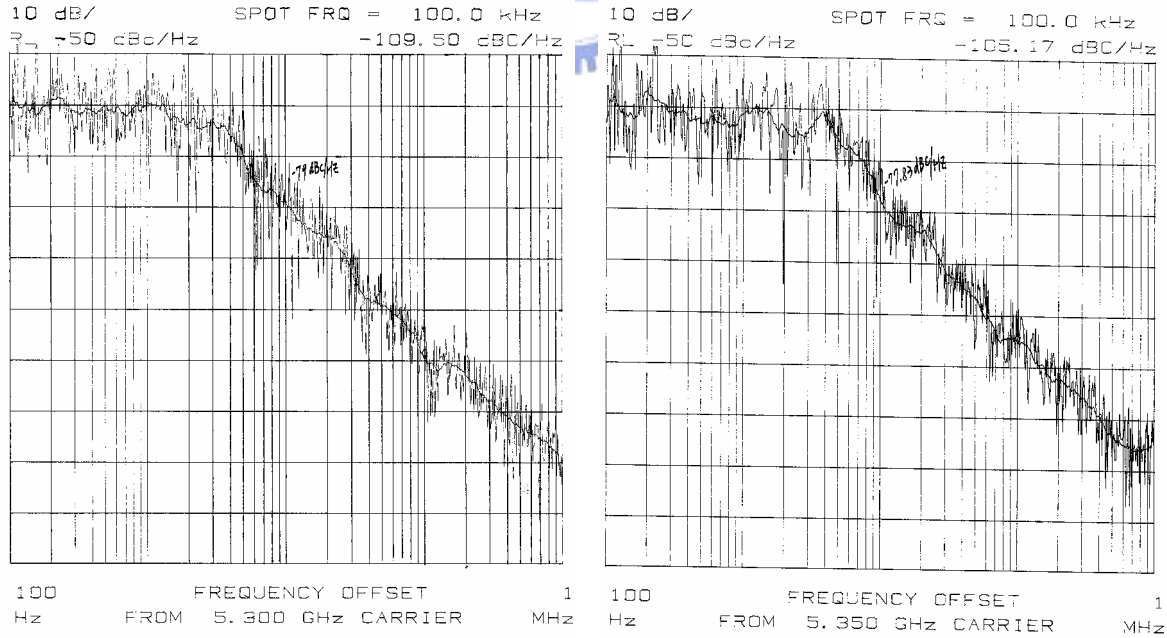
The performance of 5.25GHz VCO without DGS has been measured as shown in Table3.4. Fig.3.32 shows the curve of Frequency vs. Tuning Voltage for 5.25GHz VCO without DGS.

3.2.5 Measurement of 5.25GHz PLL Frequency Synthesizer with and without DGS

A. Measurement results of 5.25GHz PLL Frequency Synthesizer with DGS

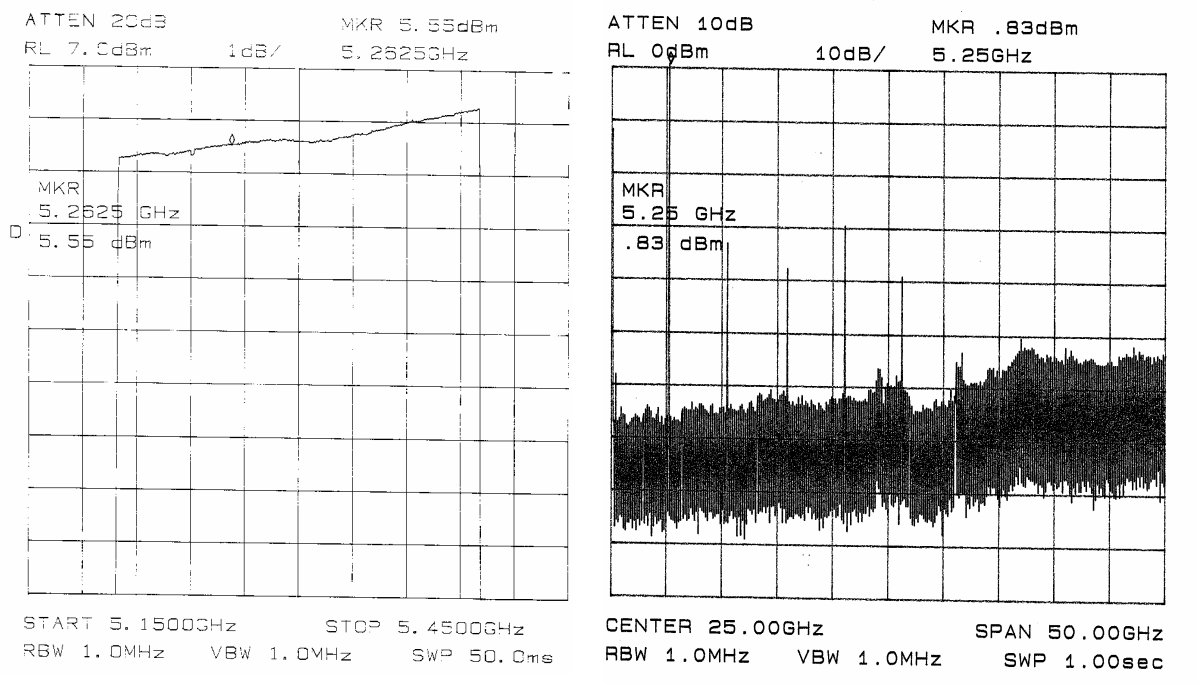


(a) f_0 = 5200MHz (b) f_0 = 5250MHz



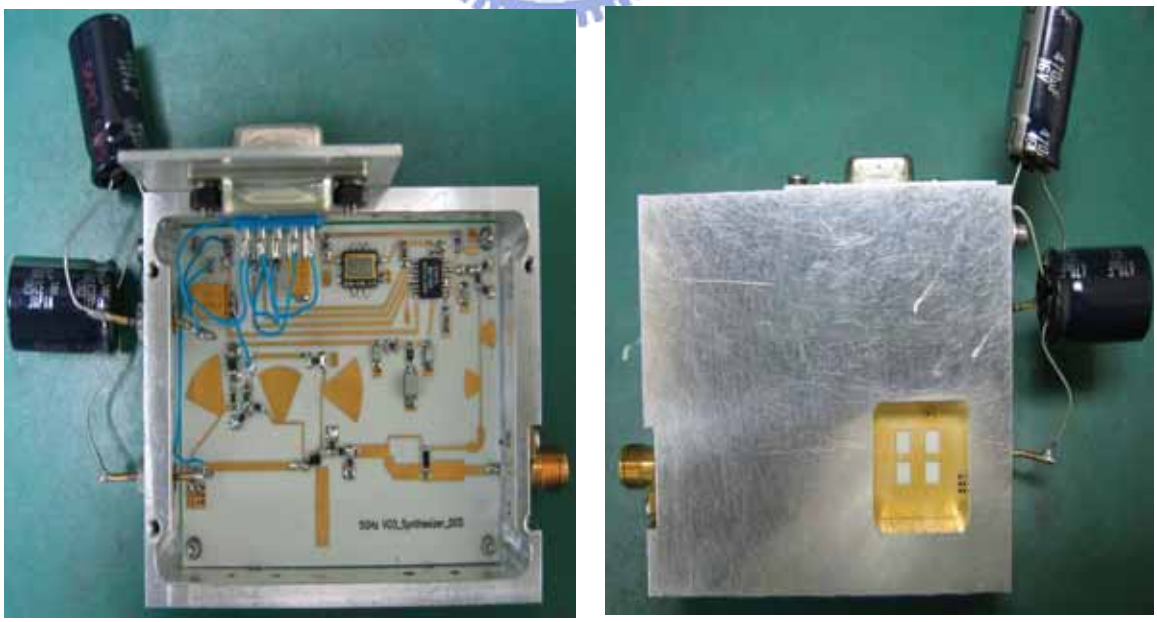
(c) f_0 = 5300MHz (d) f_0 = 5350MHz

Figure 3.33 Measurement results of the phase noise with DGS



(a) (b)

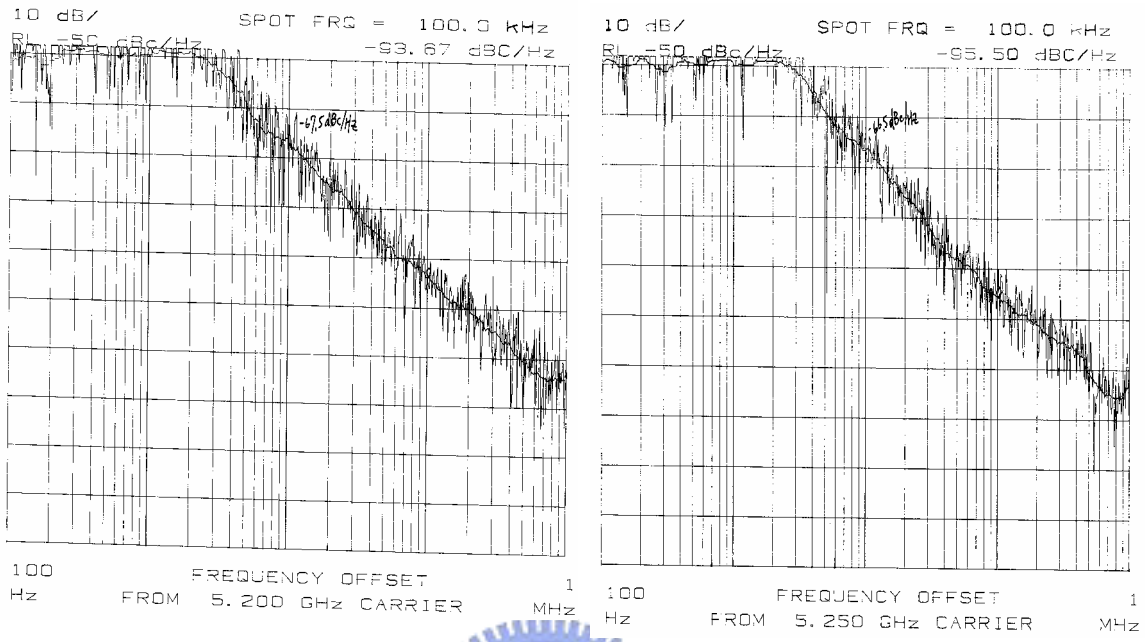
Figure 3.34 Measurement results with DGS (a)tuning range; (b) spectrum



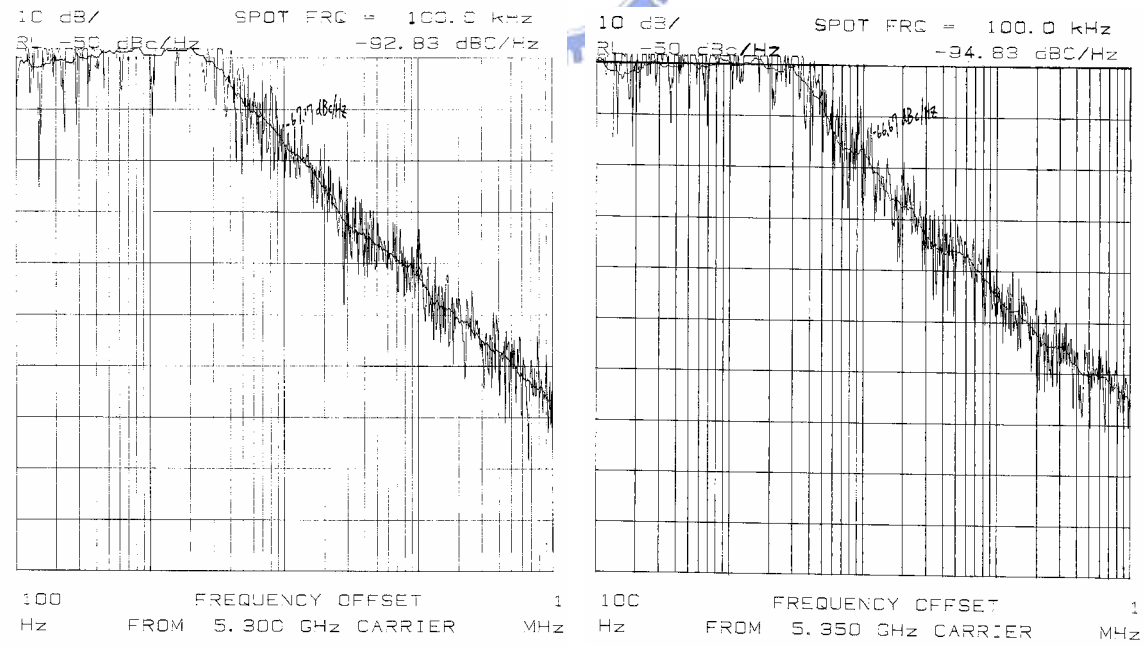
(a) Top side (b) Bottom side

Figure 3.35 Photograph of 5.25GHz PLL frequency synthesizer with DGS

B. Measurement results of 5.25GHz PLL Frequency Synthesizer without DGS

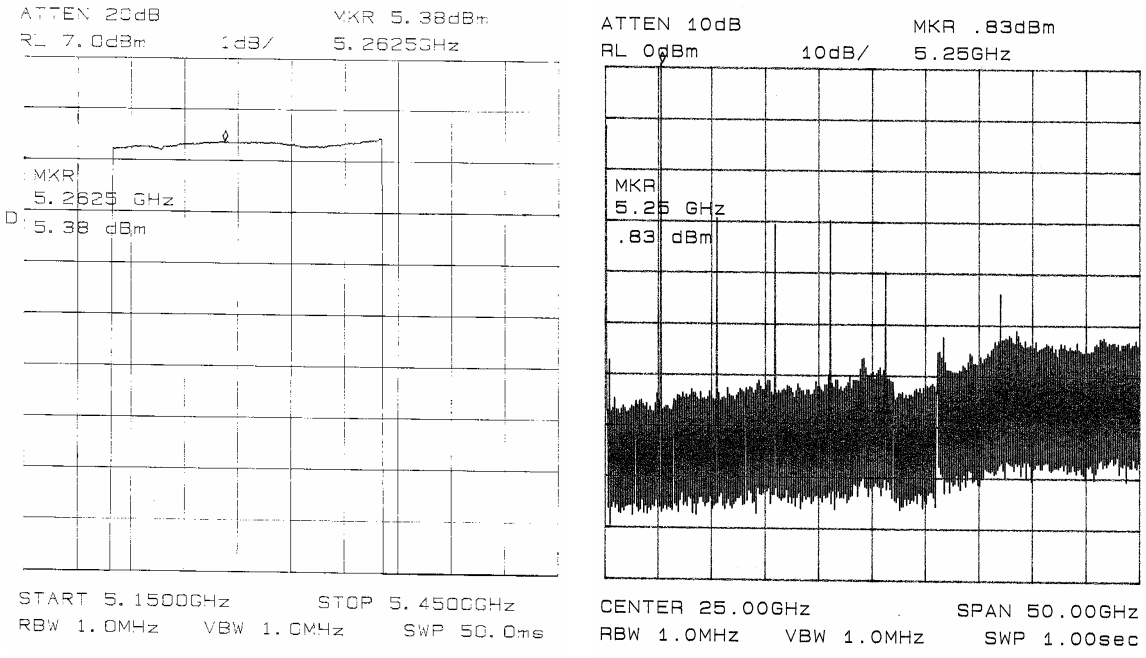


(a) f_0 = 5200MHz (b) f_0 = 5250MHz



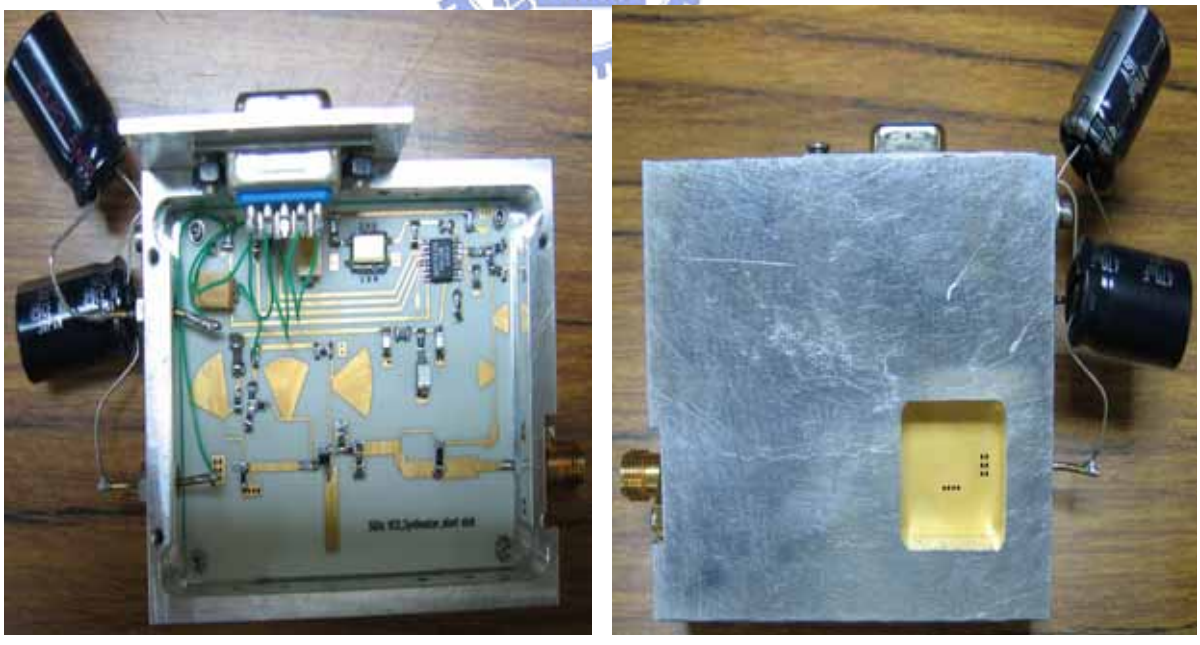
(c) f_0 = 5300MHz (d) f_0 = 5350MHz

Figure 3.36 Measurement results of the phase noise without DGS



(a) (b)

Figure 3.37 Measurement results without DGS (a)tuning range ; (b) spectrum

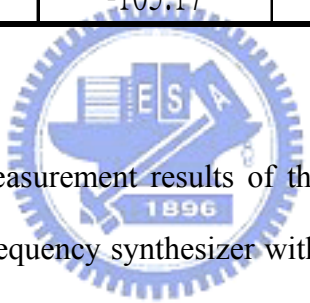


(a) Top side (b) Bottom side

Figure 3.38 Photograph of 5.25GHz PLL frequency synthesizer without DGS

Table 3.5 Summary of the measured phase noise with and without DGS

	The phase noise With DGS		The phase noise Without DGS	
Frequency (MHz)	@10KHz offset (dBc/Hz)	@100KHz offset (dBc/Hz)	@10KHz offset (dBc/Hz)	@100KHz offset (dBc/Hz)
5200	-78.17	-110.17	-67.5	-93.67
5250	-81.67	-109.67	-66.5	-95.5
5300	-79.0	-109.5	-67.17	-92.83
5350	-77.83	-105.17	-66.67	-94.83



Section 3.2.5 shows measurement results of the phase noise, tuning range and spectrum for 5.25GHz PLL frequency synthesizer with and without DGS. Fig.3.35 and Fig.3.38 show the photographs of 5.25GHz PLL frequency synthesizer with and without DGS respectively.

Table 3.5 shows a summary of the measured phase noise for 5.25GHz PLL frequency synthesizer with and without DGS. It appears that using the two-section DGS can reduced the phase noise by 10-16dB at 100 KHz offset from carrier. Thus, a higher quality factor can be obtained using the two-section DGS.

3.3 Simulation and Measurement of the Frequency Doubler

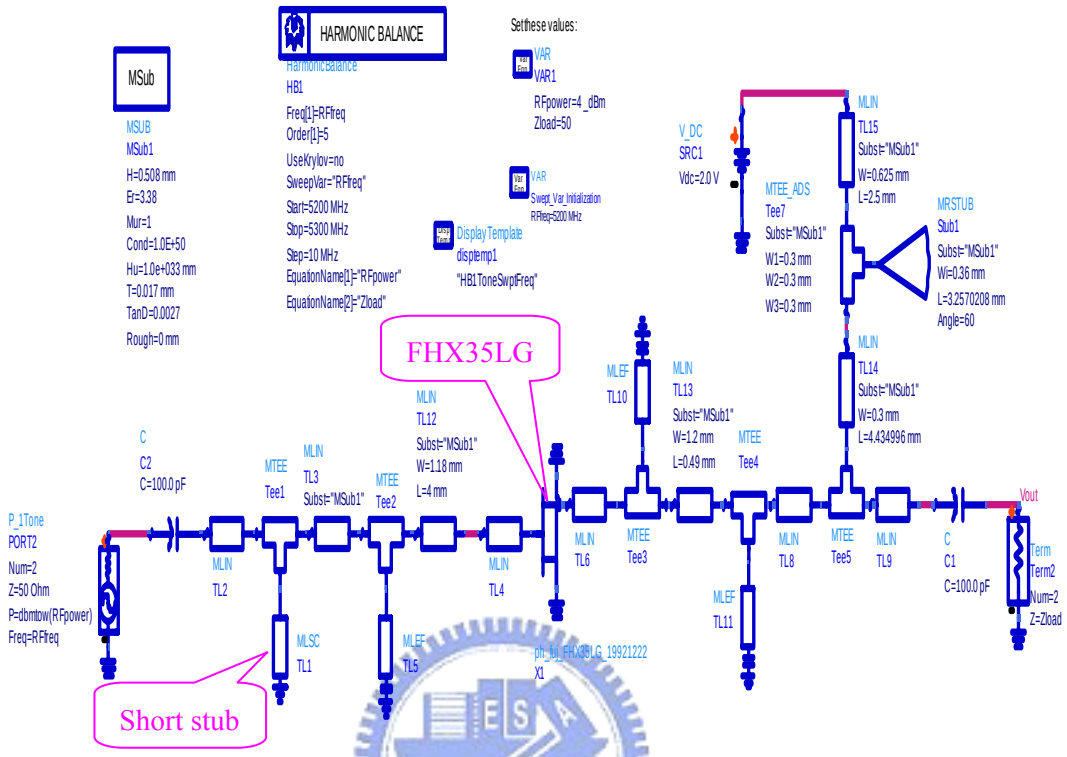


Figure 3.39 Schematic of the frequency doubler using the FHX35LG

The FHX35LG is used on the circuit of 5.25GHz to 10.5GHz frequency doubler to act as the active device as shown in Fig.3.39. The gate voltage is set as zero volts by means of using a short stub that can minimize the required circuit size with a simple bias condition, namely no requirement for RF choke and negative voltage at the gate terminal. The results of the simulation and measurement for 5.25GHz to 10.5GHz frequency doubler with input power of 4dBm are shown in Fig.3.40 and Fig.3.41 respectively.It appears that the conversion gain of the measurement result is better than the simulation result about 5.9dB at input power of 4dBm.The photograph of 5.25GHz to 10.5GHz frequency doubler is shown in Fig.3.42. The conversion gain of 5.25GHz to 10.5GHz frequency doubler has been measured for various input power as shown in Table3.6. Fig.3.43 shows the conversion gain and output power vs. input power curve for 5.25GHz to 10.5GHz frequency doubler.

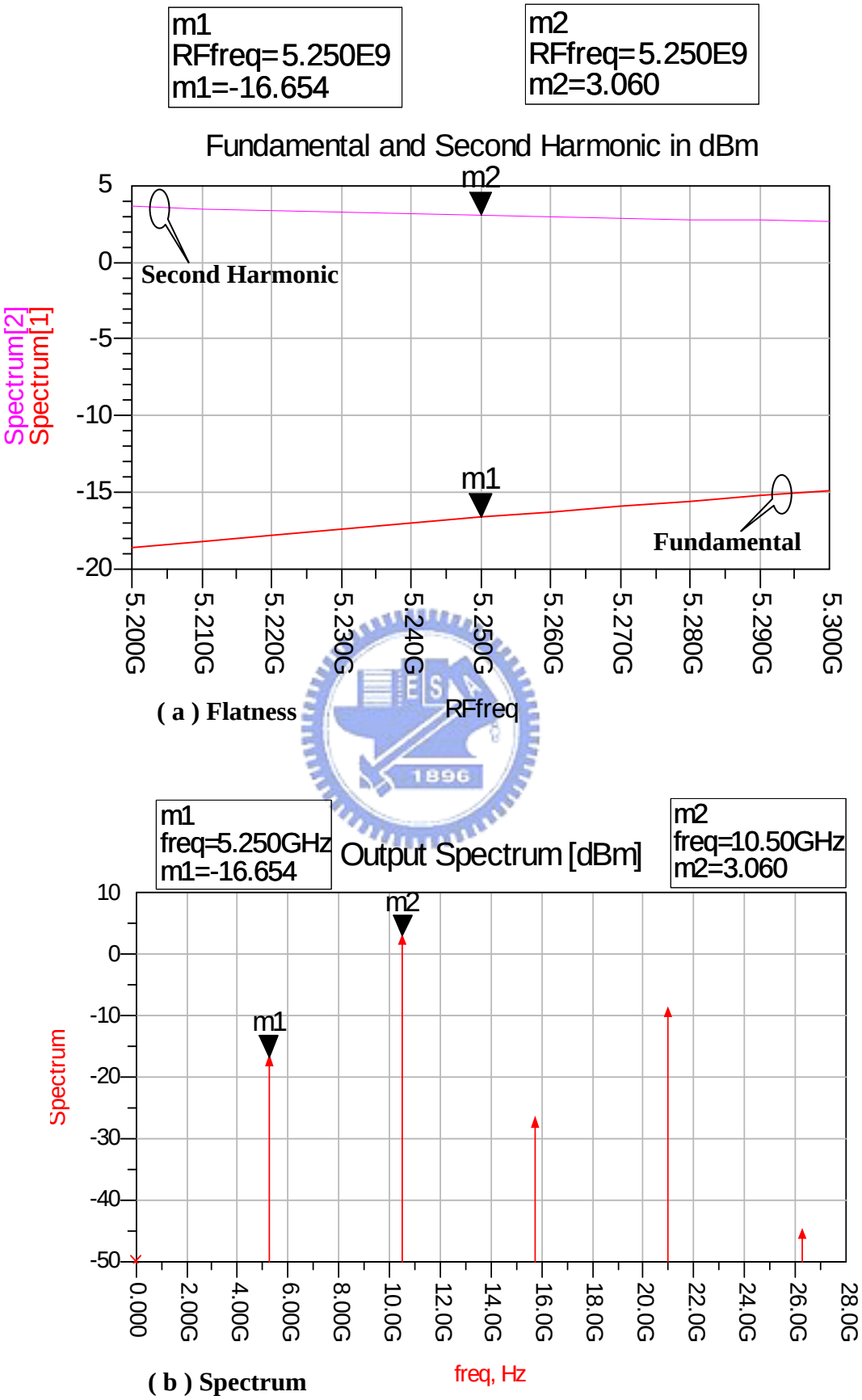
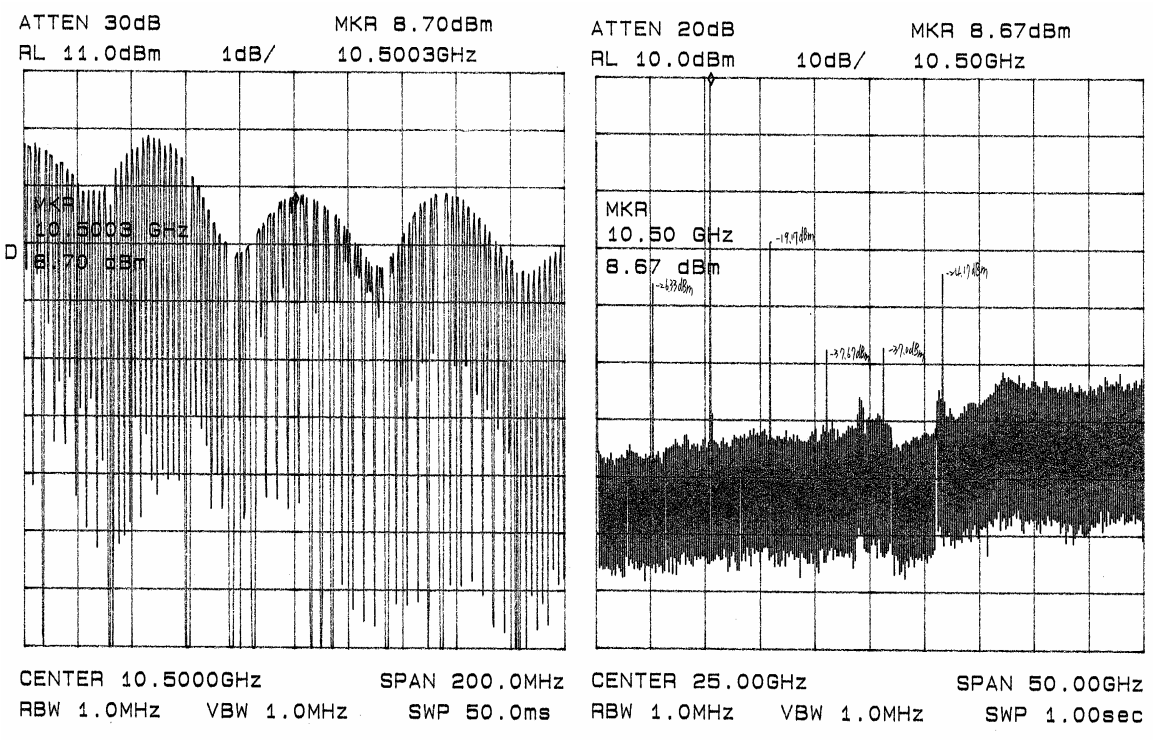


Figure 3.40 Simulation results of the frequency doubler with input power of 4dBm



(a) Flatness **(b) Spectrum**

Figure 3.41 Measurement results of the frequency doubler with input power of 4dBm

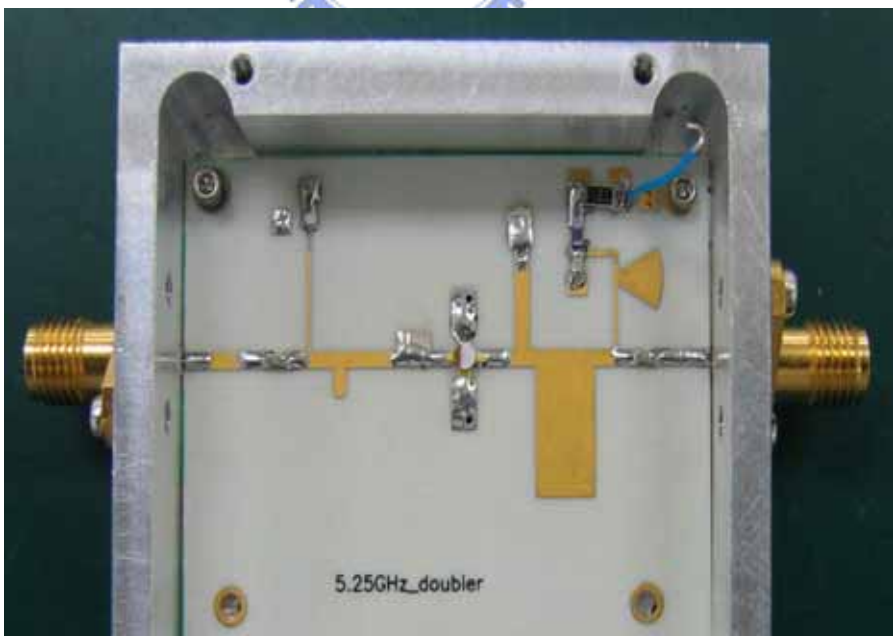


Figure 3.42 Photograph of 5.25GHz to 10.5GHz Frequency Doubler

Table 3.6 Measurement results of the frequency doubler with various input power

Input power @5.25GHz (dBm)	Output power(dBm)@10.5GHz	Conversion Gain(dB)
-10	-5.83	4.17
-9	-4.17	4.83
-8	-2.83	5.17
-7	-1.67	5.33
-6	-0.33	5.67
-5	0.67	5.67
-4	1.83	5.83
-3	3	6
-2	4	6
-1	5	6
0	5.9	5.9
1	6.85	5.85
2	7.67	5.67
3	8.42	5.42
4	8.92	4.92
5	9.33	4.33
6	9.67	3.67
7	9.83	2.83
8	10.08	2.08
9	10.42	1.42
10	10.83	0.83

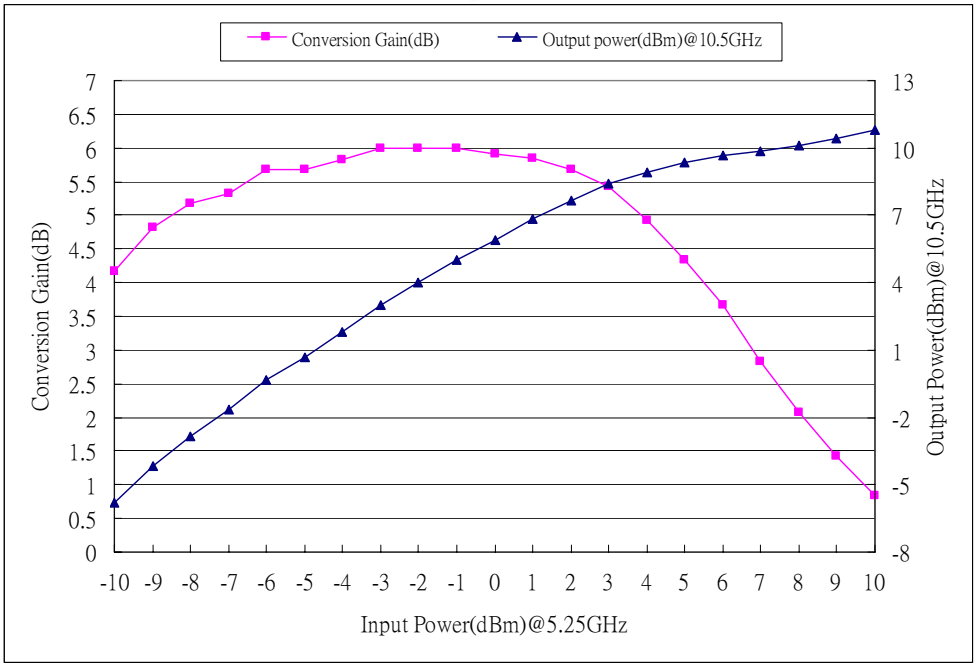


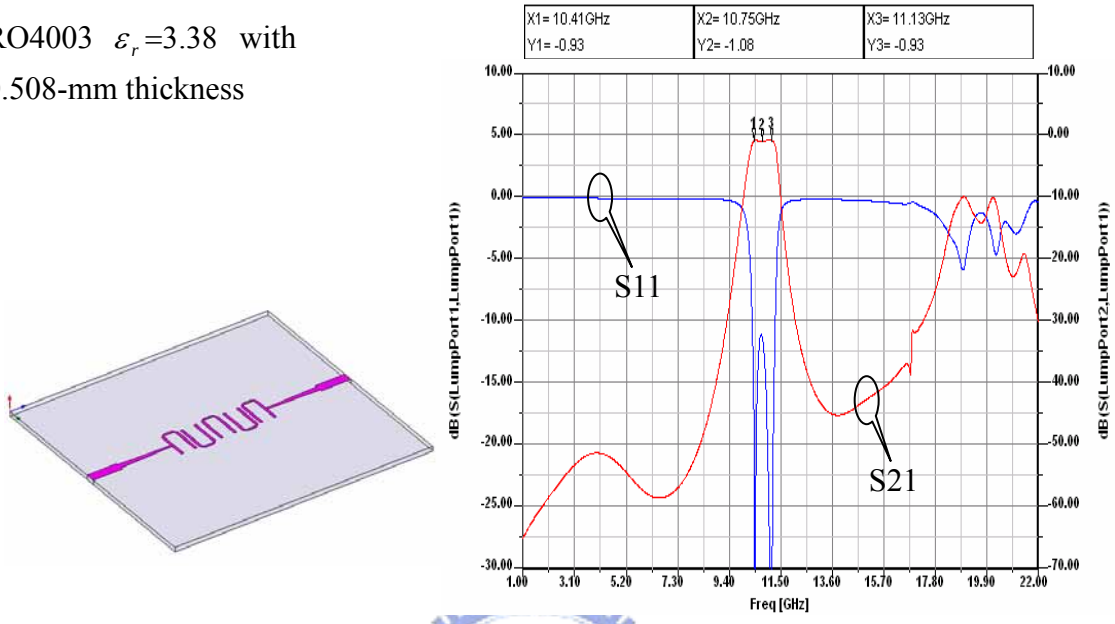
Figure 3.43 The conversion Gain vs. input power curve for the Frequency Doubler

3.4 Simulation and Measurement of 10.5GHz Band Pass Filter

A. 10.5GHz Hairpin Band Pass Filter with N=5

PCB :

RO4003 ε_r=3.38 with 0.508-mm thickness



(a) (b)

Figure 3.44 EM-simulation of 10.5GHz Hairpin BPF (N=5) (a) 3-D view; (b) result

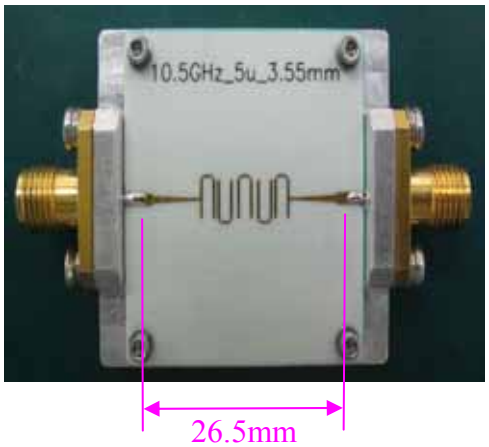


Figure 3.45 Photograph of 10.5GHz BPF(N=5)

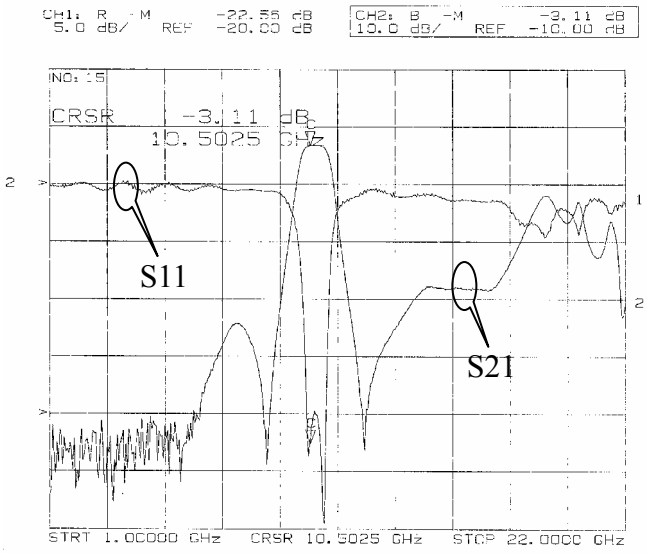
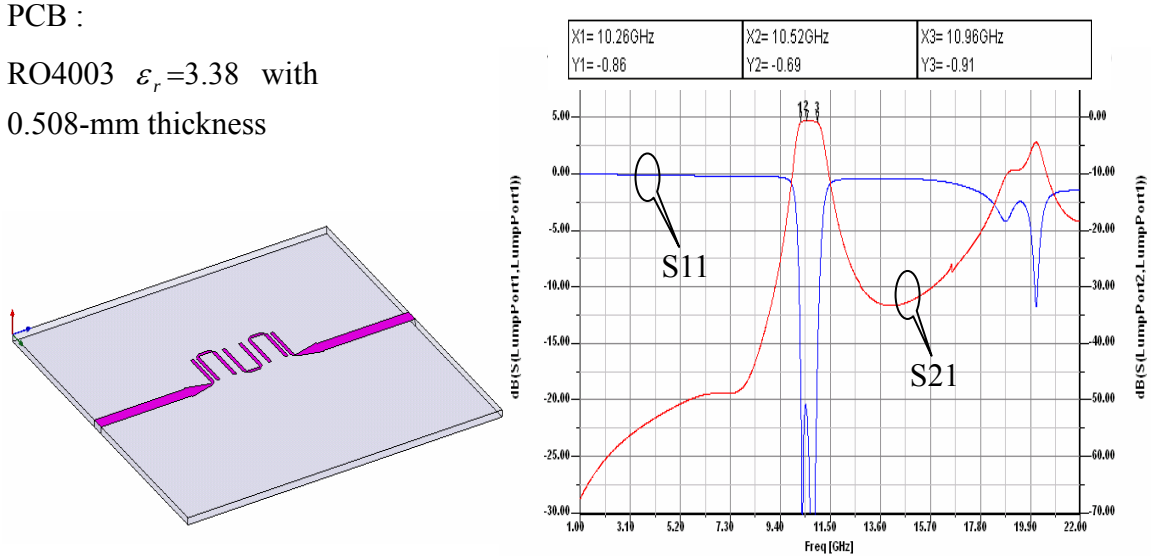


Figure 3.46 Measurement result of 10.5GHz BPF(N=5)

B. 10.5GHz Hairpin Band Pass Filter with N=3

PCB :

RO4003 ε_r=3.38 with 0.508-mm thickness



(a) (b)

Figure 3.47 EM-simulation of 10.5GHz Hairpin BPF (N=3) (a) 3-D view; (b) result

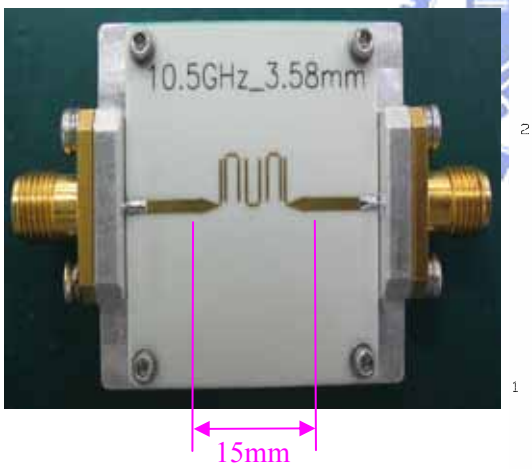


Figure 3.48 Photograph of 10.5GHz BPF(N=3)

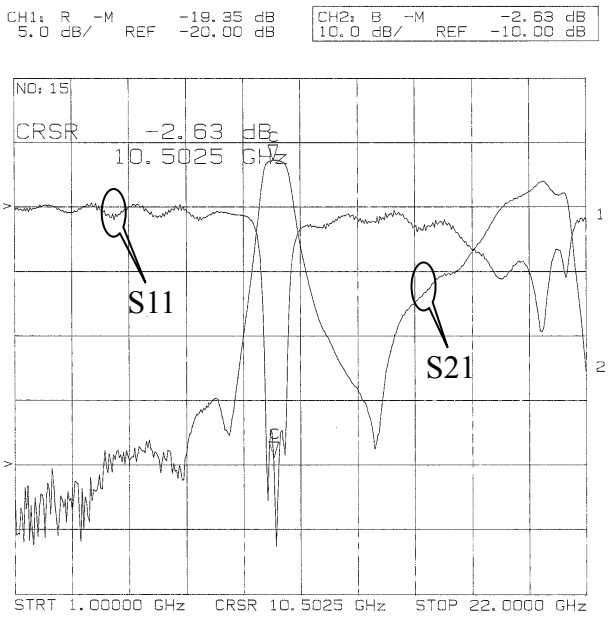


Figure 3.49 Measurement result of 10.5GHz BPF(N=3)

Section 3.4 shows the results of simulation and measurement for 10.5GHz hairpin BPF with N=3 and N=5 respectively. It appears that the rejection of 10.5GHz hairpin BPF with N=5 was deeper than 10.5GHz hairpin BPF with N=3 obviously. But in this thesis, 10.5GHz hairpin BPF with N=3 had been adopted due to its small size.

Chapter 4 Integration and Measurement of the Transceiver

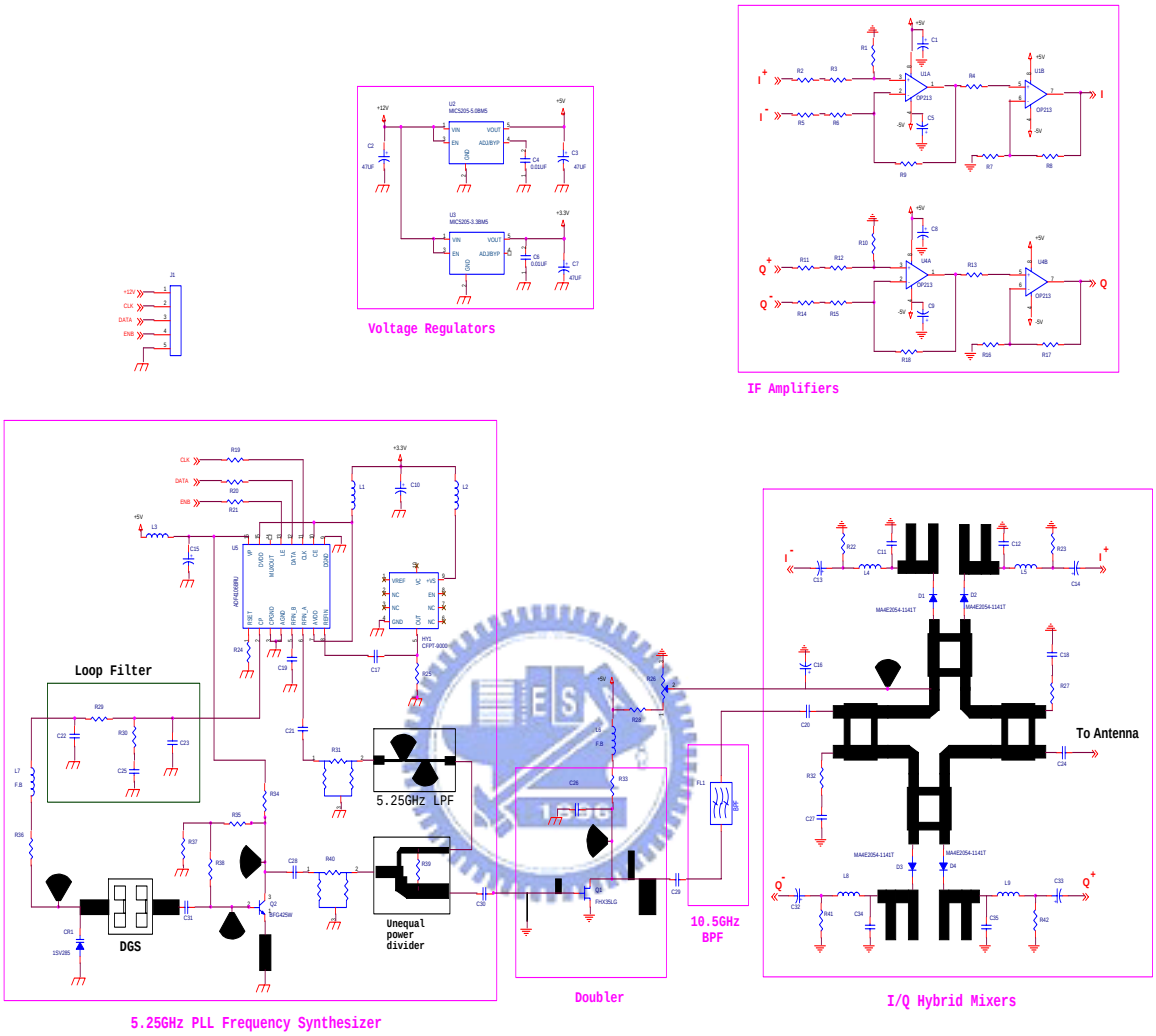


Figure 4.1 Schematic of the designed Doppler radar transceiver

Since the performance of each component had been demonstrated in the chapter 3, these components are then integrated as a Doppler radar transceiver. Fig.4.1 shows the schematic of the designed 10.5GHz Doppler radar transceiver which consists of 5.25GHz PLL frequency synthesizer with DGS, 5.25GHz to 10.5GHz frequency doubler, 10.5GHz Band Pass Filter (BPF), I/Q hybrid mixers, IF amplifiers and voltage regulators.

The designed Doppler radar transceiver has been integrated and fabricated as shown in Fig.4.2. The measurement results of the designed transceiver for the output power of 6dBm and 0dBm are shown in Fig.4.3 and Fig.4.4 respectively. Figure 4.3 (c) shows the output frequency range is from 10.4GHz to 10.8GHz.

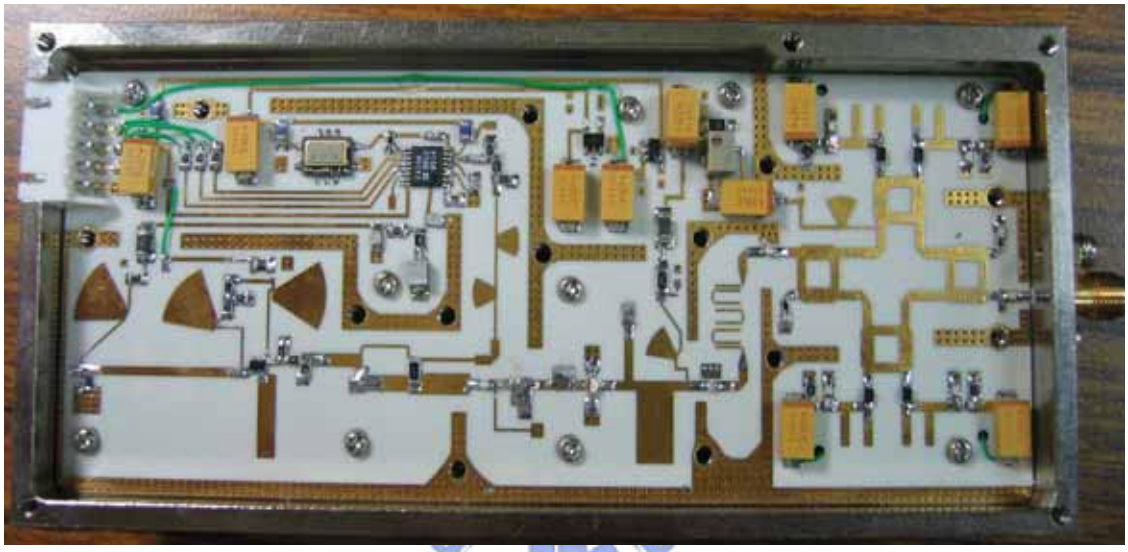
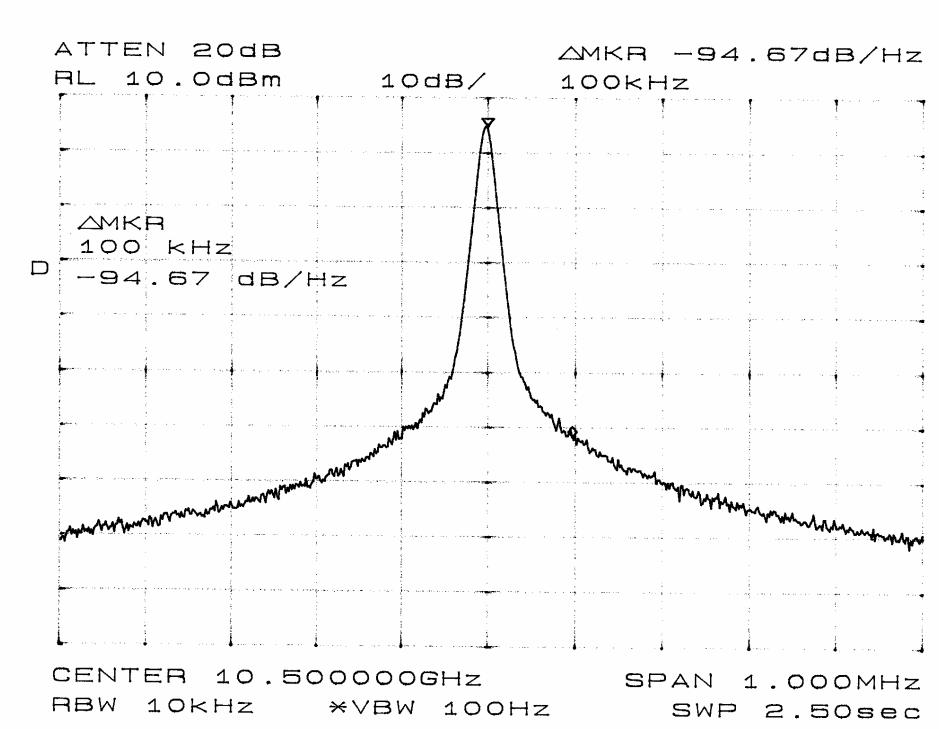
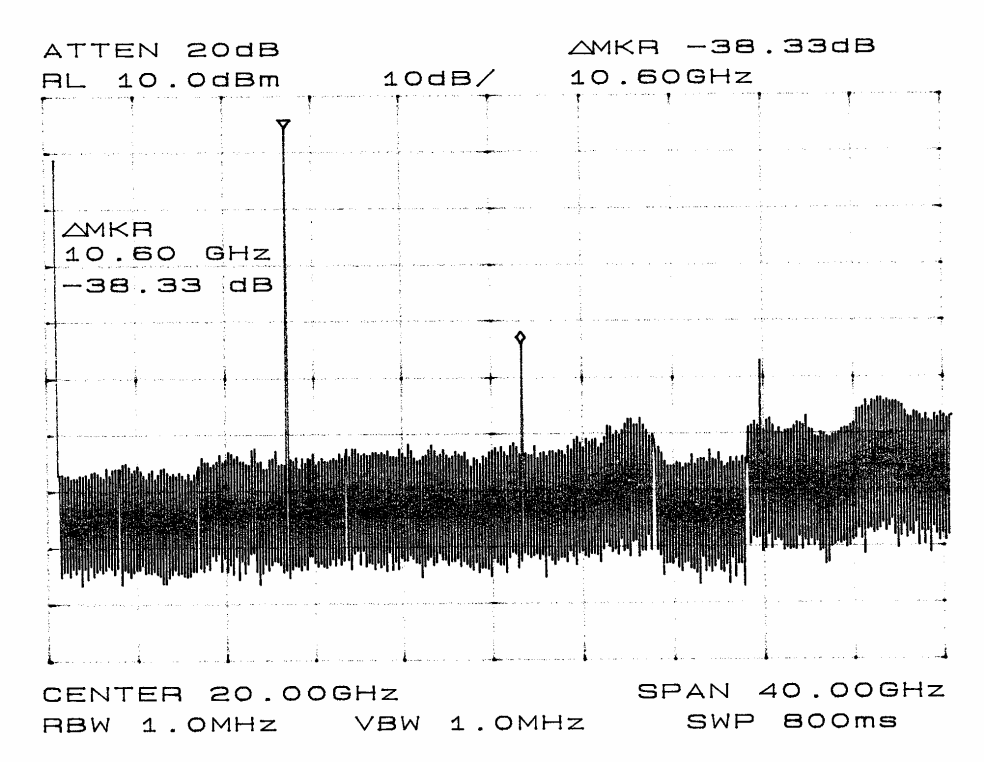


Figure 4.2 Photograph of the designed Doppler radar transceiver

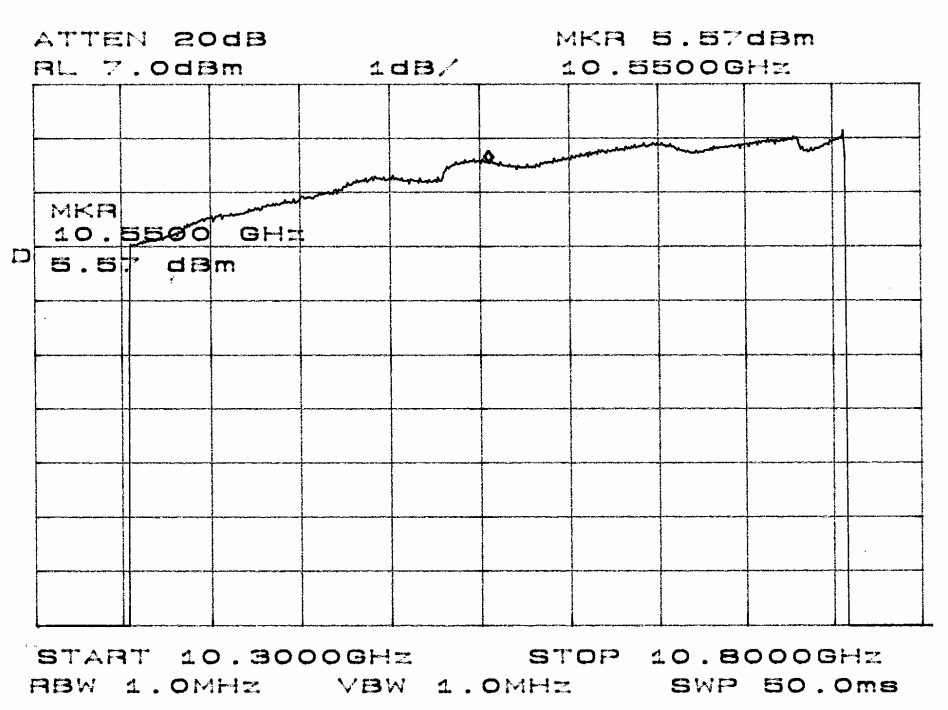


(a) Phase noise

Figure 4.3 Measurement results of the designed transceiver with output power of 6 dBm

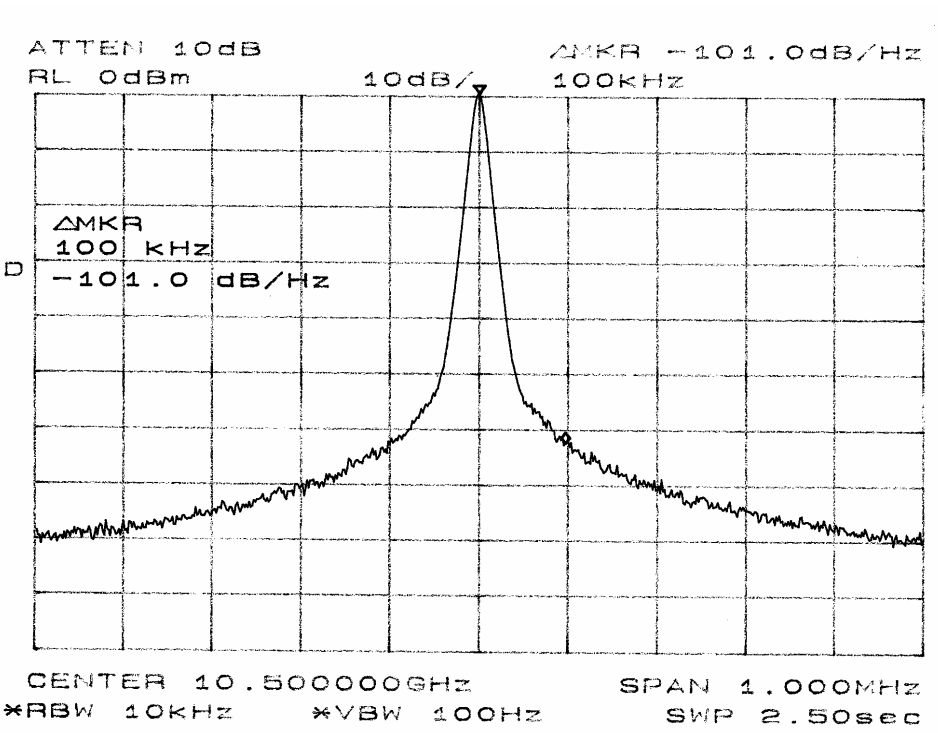


(b) Spectrum

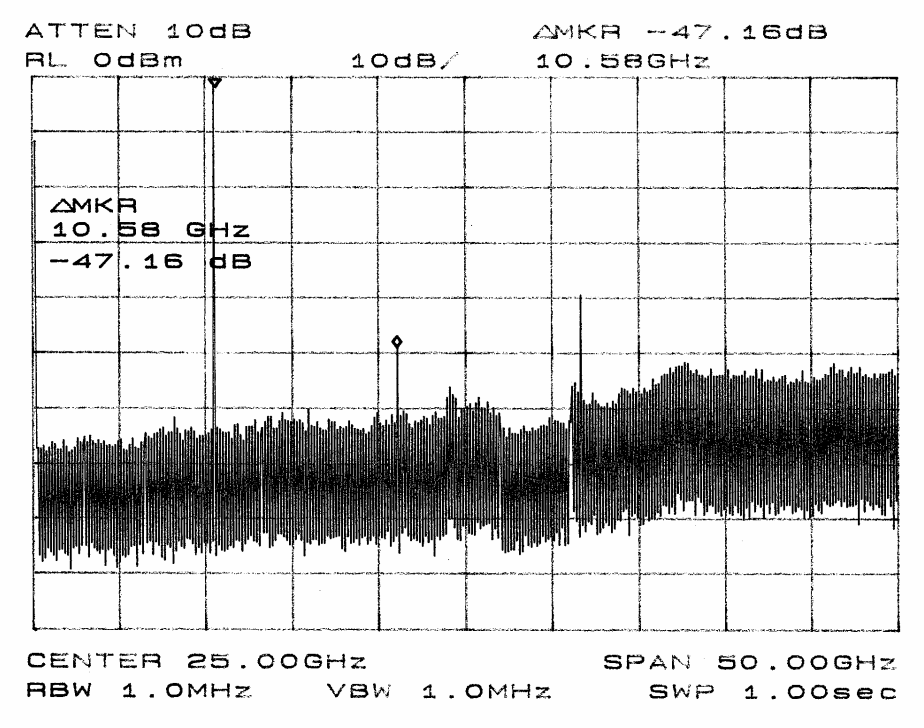


(c) Flatness

Figure 4.3 (continued)



(a) phase noise



(b) spectrum

Figure 4.4 Measurement results of the designed transceiver with output power of 0 dBm

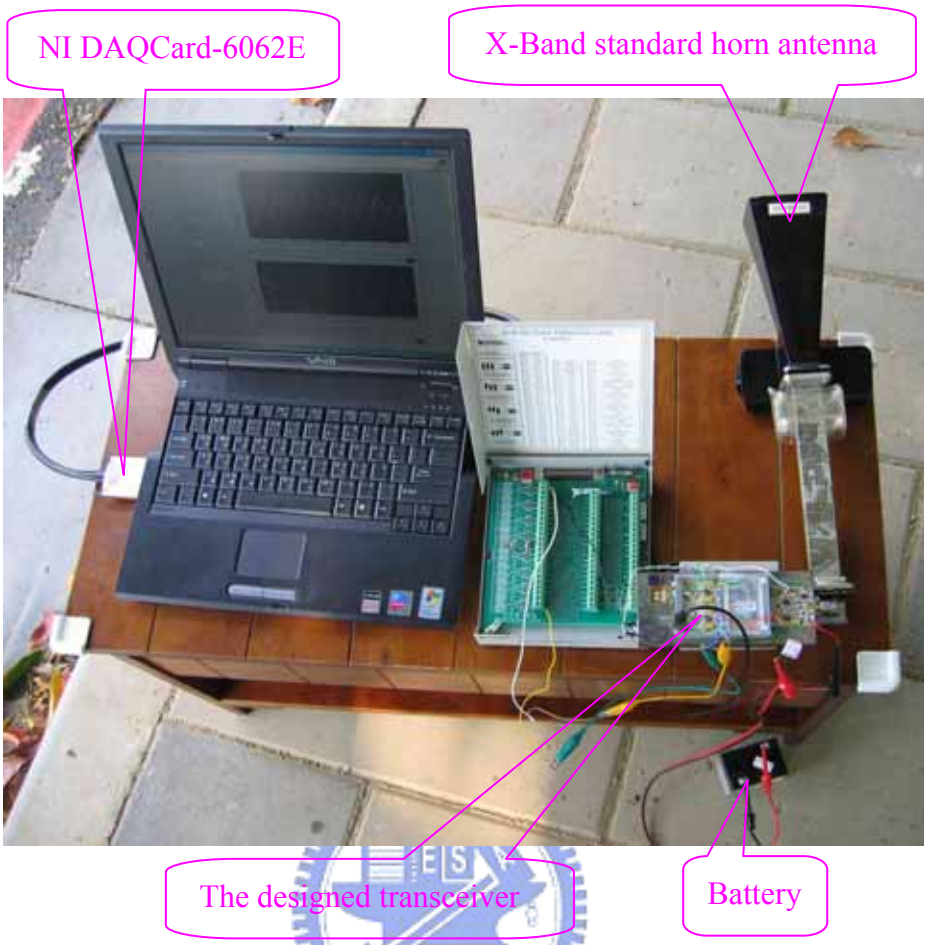


Figure 4.5 Photograph of the Doppler radar sensor

The Doppler radar sensor consists of the designed transceiver, an X-Band standard horn antenna, NI DAQCard-6062E with Digital Signal Processing (DSP) and a battery as shown in Fig.4.5 which has been measured for an approaching vehicle at the velocity of 60km/hr and a receding vehicle at the velocity of 45km/hr respectively. The sample rate is assumed to be 50k samples/sec. Fig.4.6 shows Q channel lead to I channel for an approaching vehicle at the velocity of 60km/hr.Fig.4.7 shows Q channel lag to I channel for a receding vehicle at the velocity of 45km/hr. Fig.4.8 shows the Doppler frequency shift is about 1172Hz and the image rejection is about 29dB for an approaching vehicle at the velocity of 60km/hr. Fig.4.9 shows the Doppler frequency shift is about -878Hz and the image rejection is about 25dB for a receding vehicle at the velocity of 45km/hr.

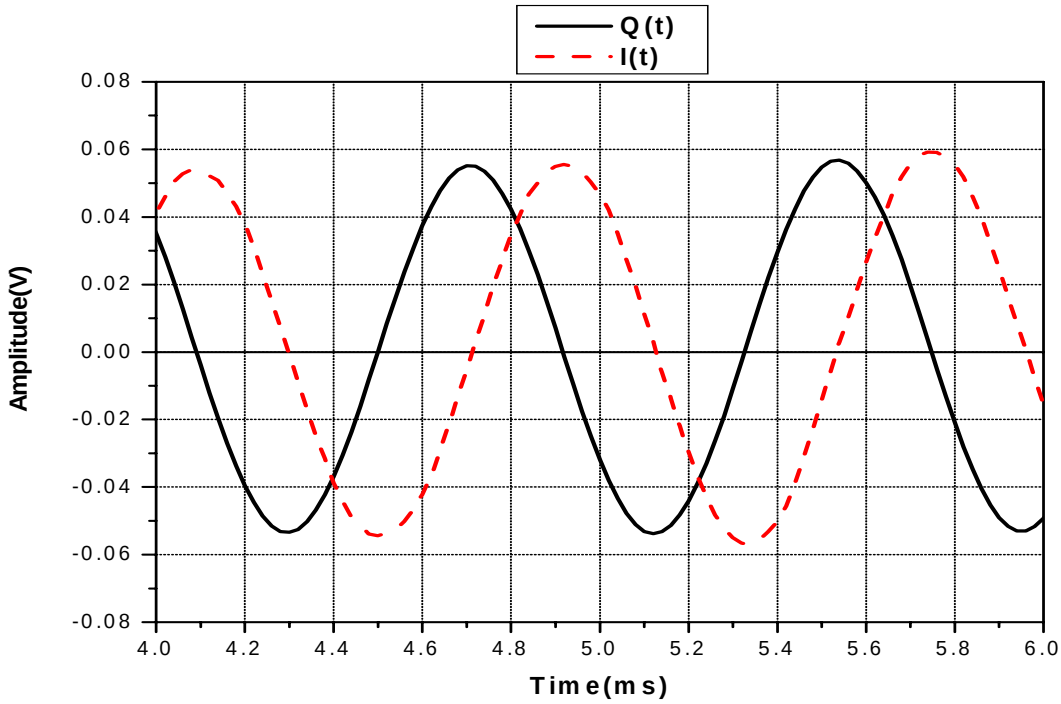


Figure 4.6 Measurement result of I/Q channels for an approaching vehicle at the velocity of 60km/hr

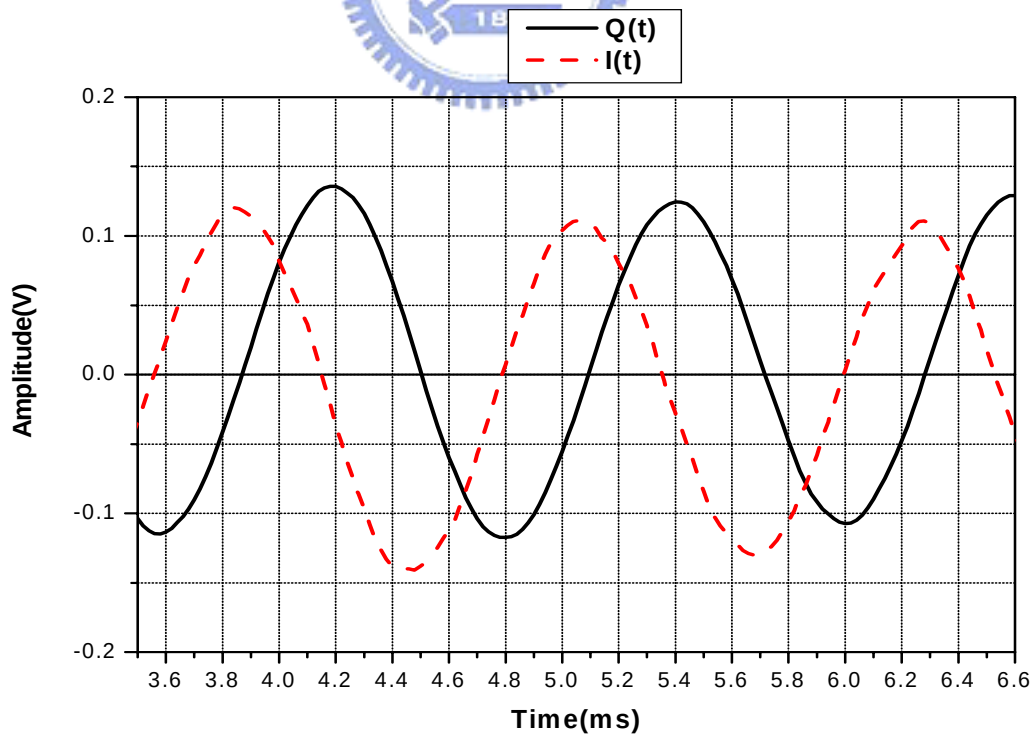


Figure 4.7 Measurement result of I/Q channels for a receding vehicle at the velocity of 45km/hr

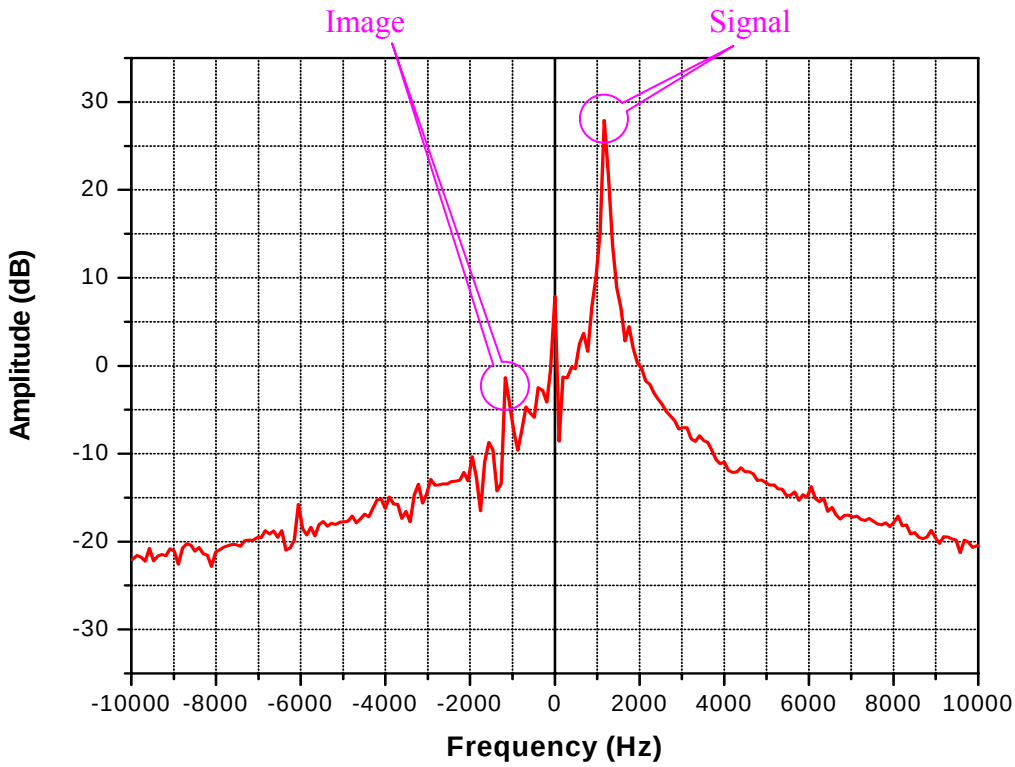


Figure 4.8 Measurement result of the Doppler spectrum (image rejection) for an approaching vehicle at the velocity of 60km/hr

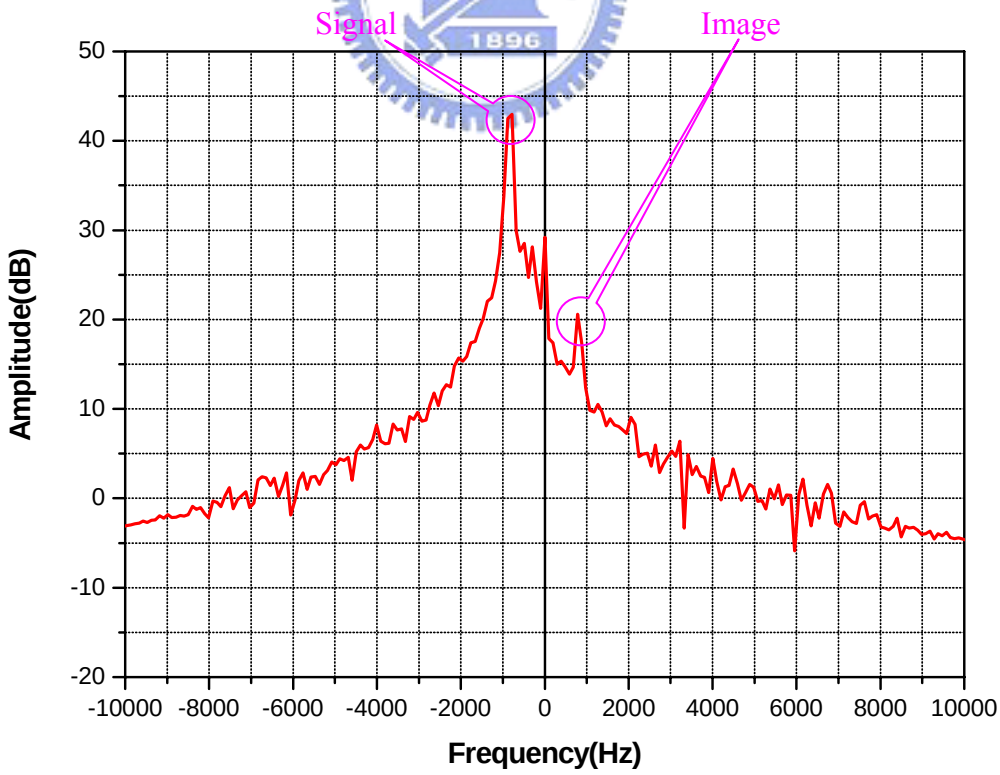


Figure 4.9 Measurement result of the Doppler spectrum (image rejection) for a receding vehicle at the velocity of 45km/hr

Chapter 5 Conclusion and Future Study

An I/Q hybrid mixer is proposed and demonstrated in this thesis which the transmitted signal and the received echo signal pass through the same antenna with no circulator. In addition, the phase noise of oscillator can be reduced by 10-16dB at 100KHz offset from carrier using the DGS. Finally, the designed Doppler radar transceiver has been measured using an X-band standard horn antenna and NI DAQCard-6062E with Digital Signal Processing (DSP) for an approaching vehicle and a receding vehicle. The measurement result shows the validity of distinguishing an approaching vehicle or a receding vehicle and the related velocity.

Due to the 400MHz tunable synthesizing frequency, the designed transceiver can be used with the frequency-scanning antenna for the application of multi-path sensors.

The drawback of the designed transceiver is its big circuit size. It is necessary to reduce the circuit size. In the future, it is worth considering that the designed transceiver with Digital Signal Processing (DSP) can be realized in the MMIC to minimize the circuit size.

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