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電機學院與資訊學院 資訊學程

碩 士 論 文

液晶平面顯示器時序控制與影像品質之改善

The Improvement of TFT-LCD Timing Control and Image Quality

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中華民國九十五年六月

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摘要

TFT-LCD顯示器具有體積小，重量輕，低輻射和省電等優點，非常適合應用在行車裝置、個人隨身裝置、筆記型電腦、桌上型顯示器以及大尺吋的家庭電視。此篇論文我們以液晶的光電轉換特性切入並瞭解液晶應用於顯示科技上的原理，並且使用非揮發性記憶體存取時序控制設定值於時序控制器內，此設計可彈性化的應用於不同製程的液晶顯示器面版，以因應不同的時序控制時間。

在影像品質提升上，為配合六位元的驅動晶片往往影像品質就會變差，故此論文使用影像演算法在空間與時間上將影像品質延伸至近乎八位元的影像品質。

最後將時序控制器和影像演算法實現於XILINX FPGA 上並且在液晶顯示器上做影像演算法的驗證。

The Improvement of TFT-LCD Timing Control and Image Quality

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ABSTRACT

TFT-LCD is a lighter weight, lower power, no radiation and thinner display than bulky display. In virtue of these characteristics, it is convenient to deploy TFT-LCD in car, PDA, notebook, monitor and TV etc. In this thesis, we describe TFT-LCD panel operation, driving methods from system view, and use Verilog HDL to implementation flexible TFT-LCD timing controller.

Due to that different panel module implementations have different characteristics, panel module will affect designs on timing control signals. In early timing controllers the constant timing value was used for a specific TFT-LCD panel. If we want to implement a new panel module we have to design new timing controller.

In this thesis we use external EEPROM memory to save associated control timing value, it can reuse timing controller for different panel modules and reduce design cycle for panel system designer.

The image data in TFT-LCD panel need to be harmony with 6-bits driver IC, therefore it has low image quality. In this thesis we use frame rate control algorithm to improve it becoming almost 8-bits image quality.

Finally, we use XILINX FPGA to verify control timing and use TFT-LCD panel to verify frame rate control algorithm.

Acknowledgments

I am so very appreciative of:

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Chap 1 Introduction

1.1 TFT-LCD Panel Industry Profile

The TFT-LCD, an abbreviation of thin-film-transistor-addressed liquid crystal display, is a flat-panel display in which the display medium is liquid-crystal and each picture element (pixel) is controlled by a thin film transistor. The TFT-LCD is creating a whole new world of technology in consumer electronics, computer and communication systems. The market for TFT-LCD products is now growing much faster than expected and also impacting new application fields, for examples, LCD-TV, LCD monitor, PDA, cellular phone, camera and GPS as well as conventional fields.

From 2003 to 2008, the LC displays market share will be grow up 16% and the output value will rise to USD 113.2 billion. See Figure 1.

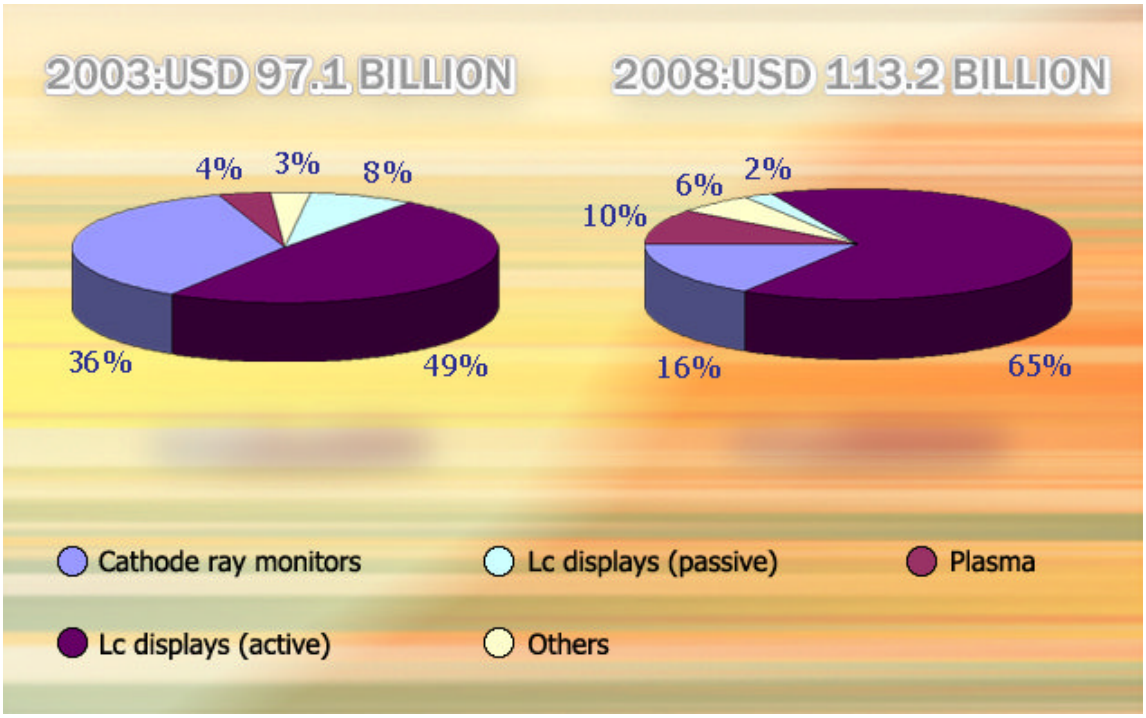


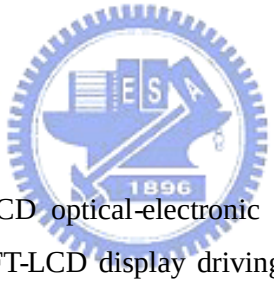
Figure 1. Market volume of all display types [3]

1.2 Motivation

In the past, the timing controller of the thin film transistor liquid crystal displays (TFT-LCD) is used for specific panel process. Therefore TFT-LCD system designer needs to create many specific for timing control in different panel process, it's become more effort on system design cycle.

If we can design flexible timing controller for different panel model using, it's convenient for panel system engineer and shorter develop cycles to achieve time to market.

Furthermore in early TFT-LCD timing controller is using TTL level to transmission image stream for column driver, but it usually has EMI emissions issue and large wire trace on print circuit board. Therefore by reducing image data stream can reduce large wire trace and EMI emissions issue, so normally we use 6-bits image data format for display, in that case, we can know that reduce image data format will affect on image quality. In this thesis we will improve these problems.



1.3 Organization

In this thesis we study TFT-LCD optical-electronic character in section 2.2 and then, in section 2.4 we will describe TFT-LCD display driving method. After that we will illustrate color image operation principle in TFT-LCD panel in section 2.5. After we know about the TFT-LCD operation principle, we will describe design of TFT-LCD timing controller and frame rate control algorithm to improve 6-bit image data extended to 8-bit image data quality in section 3. In section 4 we use FPGA-based platform to verify our timing controller design and use TFT-LCD panel to drive that frame rate control algorithm is available. Finally in section 5 we will illustrate this thesis conclusion and the future work of TFT-LCD panel timing controller.

Chap 2 Related Works

2.1 Flat Panel Display Classifications

In flat panel display application, we can divide the luminance to non-emission and emission group. See Figure 2. In this research, we will focus on active matrix driving methods in TFT-LCD non-emission device. There are two types of material used in TFT-LCD manufacture. One is a-Si and the other is Poly-Si. In a-Si, there are some advantages like cheap and reliable technology for very large IC area but the has very slow electron mobility and sensitive to head and light, it also reduce brightness. The Advantages of Poly-Si material are higher speed, inherent stability, brighter and higher resolution. On the other hand, it's expensive due to the higher processing temperature and larger OFF state current leakage.

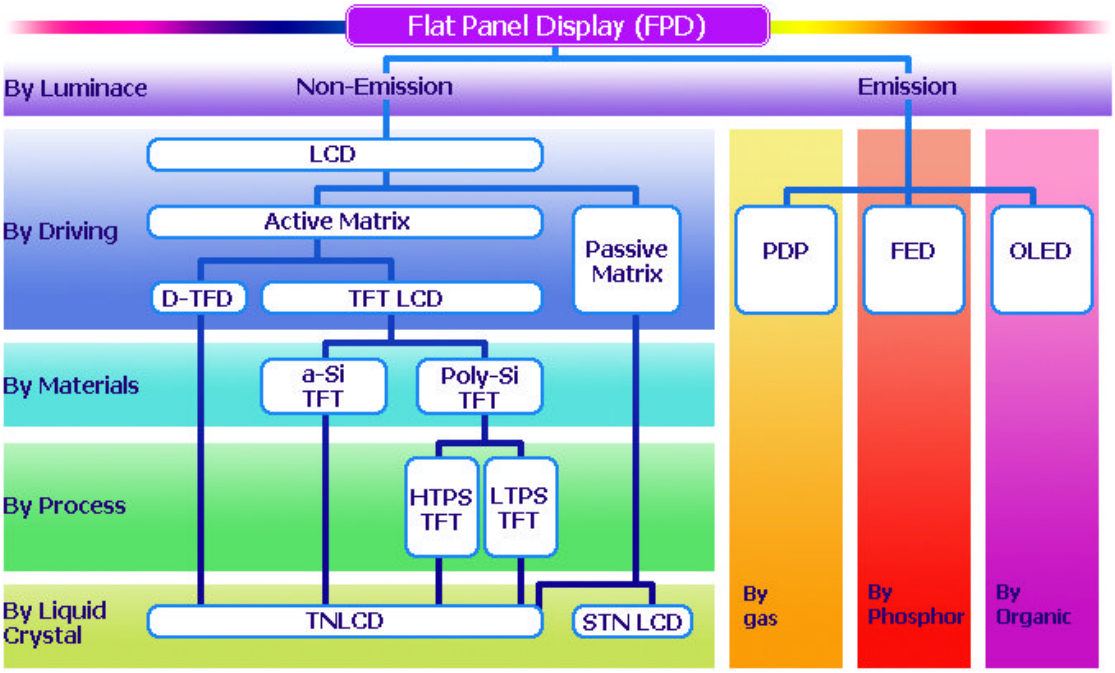


Figure 2. Classification of FPD.

2.2 LC Operation theory

In this section, we will stand on electro-optical convert principle to describe LC operation, TFT-LCD module architecture, VESA standard timing specification, and column and row driver.

2.2.1 Twisted-Nematic Cell

The electro-optical effect in twisted nematic (TN) liquid-crystal cell is now widely used in active-matrix liquid-crystal displays. As shown in Figure 3, a thin layer of nematic liquid-crystal is placed between two glass plates which provided a transparent and conductive coating.

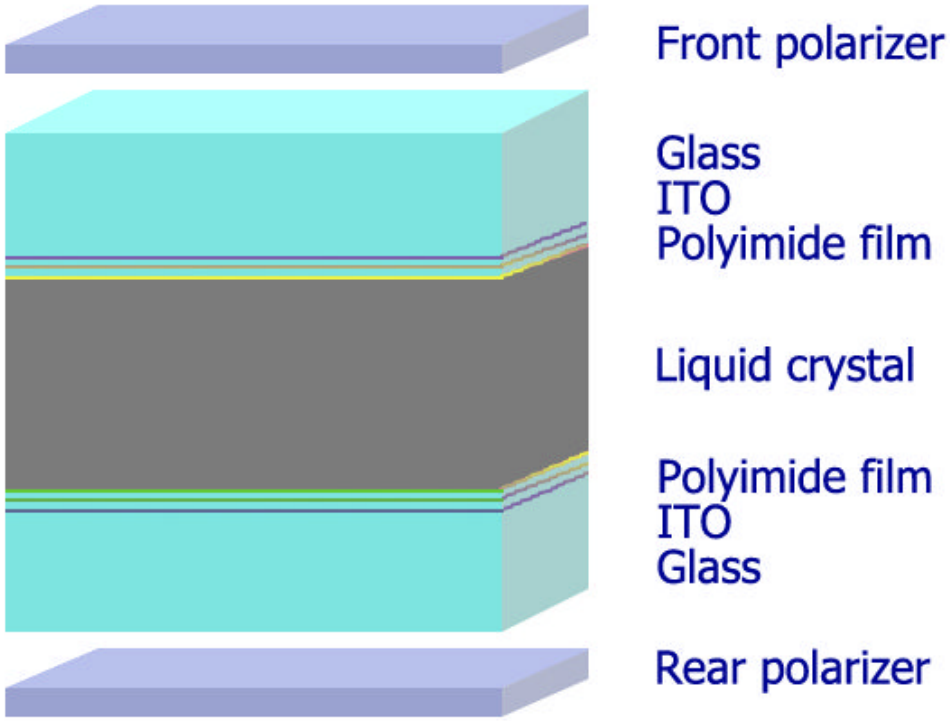


Figure 3. Functional of the TN cell [7]

The orientation of liquid-crystal molecules or director on both plates is aligned to be nearly parallel to the surface of the glass plate (planer or homogeneous alignment), and as shown schematically in Figure 4, this orientation on each plate twisted 90^0 with respect to that of the other plate, so that the orientation is continuously twisted from the bottom to the top by 90^0. The homogeneous alignment of liquid-crystal molecules on each plate is produced by rubbing the surface of a polyimide thin file in the proper direction with a fabric.

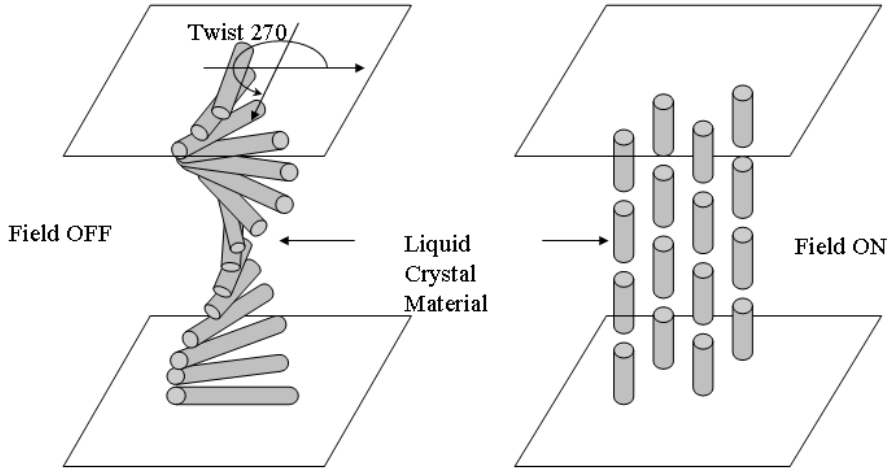


Figure 4. Molecular alignment in TN cell.

With a twist angle by 90^0 and a cell thickness by 5um, the resulting pitch of cholesteric equivalence is 20um. Since this is much greater than the wavelength of light, the polarization plane of linearly polarized light traveling normal to the glass plates rotates with the liquid-crystal axis; the 90^0 twist of the director should lead to a 90^0 rotation of the linearly polarized light. Therefore, in this normally white (NW) mode of operation where the two polarizers are set perpendicular to each other, the light is transmitted through the cell when there is no applied voltage.

2.2.2 Light Valve Characteristics

When voltage applied to the TN cell, it modified the director orientation. When applied to the cell modifies the director orientation. When the applied voltage is below a threshold level, there is no charge of the orientation, but at the threshold the molecular orientation begins to be aligned to the electric field and tends to be perpendicular to the glass plate. At voltage well above the threshold the alignment of the molecules is completely parallel to the field except the regions adjacent to the surface of glass. There are two kinds of models in TN cell. One is normal black (NB) and the other is normal white (NW). These two models respectively correspond to the parallel and the perpendicular polarizer schemes. See Figure 5.

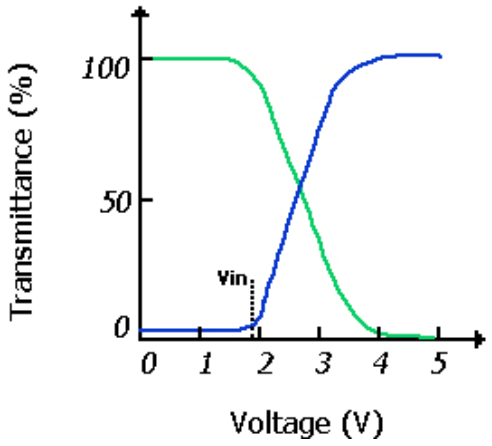


Figure 5. Normal black (NB) and normal white (NW) models of operation.

The TN cell becomes optically inactive and linearly polarized high travels through the cell without any rotation of the polarization then the light polarization becomes perpendicular to the output polarizer resulting in no transmission of light.

The originally proposed TN cell used a parallel scheme: the two polarizer where parallel to each other. In the NB (normal black) configuration, the light is not transmitted in a field-free state and is transmitted when the applied voltage is above the threshold. When there is no bias voltage. However, transmission is suppressed to zero only for monochromatic light of wavelength λ. Therefore in a practical display in which a broad-band illumination is used. In the NB mode this leakage reduce a contrast ration which is the ratio between the “on” and “off” transmission.

In the normally white mode, if operation has little reduction in the contrast ratio since this ration is governed by an “off” transmission corresponding to a high bias voltage. When a sufficiently high voltage is applied, the liquid-crystal molecules are aligned parallel to the electric field or perpendicular to the glass substrate and there is no rotation of electric vector of the polarized light. Transmission is suppressed completely regardless of the wavelength of the light. The transmission in the “on” state is wavelength dependent. But this transmission does not have a critical effect on the contrast ratio. A contrast ratio exceeding 100 can be readily in the normally white mode of operation. This is why normally white mode is preferred in the practical TFT-LCD display.

2.2.3 Threshold Voltage of TN Cell

Liquid-crystal modules are easily affected by an external field. The TN cell is sandwiched between the two glass plates and the director orientation at the surfaces of these plates differs from each other by an angle.

In Equations (1) and (2) the time constant is proportional to the square of cell gap. Reducing the cell gap is therefore an effective way to shorten the cell response time. Where threshold voltage on TN cell is V_{th}, τ_r is rise time constant, τ_d is delay time when threshold voltage turn off on TN cell [12].

$$\tau_r = \frac{\gamma_1 d^2}{\left[\Delta\varepsilon\left(V^2 - V_{th}{}^2\right)\right]} \tag{1}$$

$$\tau_d = \frac{\gamma_1 d^2}{\Delta\varepsilon V_{th}{}^2} \tag{2}$$

For a display like an LCD as well as CRT, the rise and fall times are defined for convenience as the times when the brightness reaches, after the turn on and turn off the drive voltage, 90% and 10% respectively of full brightness, see Figure 6. These turn on and turn off times (t_{on} and t_{off}) are given by

$$t_{on} \approx 2.3\tau_r \tag{3}$$

and

$$t_{off} \approx 2.3\tau_d \tag{4}$$

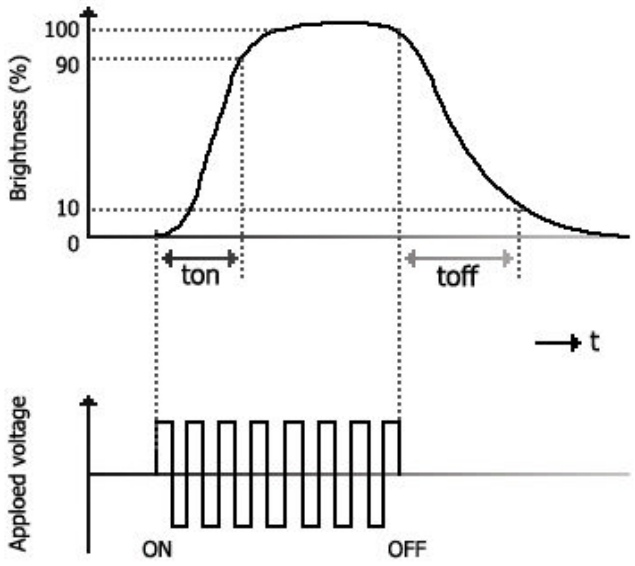


Figure 6. Response time of a twisted-nematic liquid-crystal cell.

An example of the temperature dependence of t_{on} and t_{off} is shown in Figure 7. The turn on time is usually shorter than turn off time, and room temperature these times are about 10ms [12]. The response time is reasonable for such application TV and computer terminals.

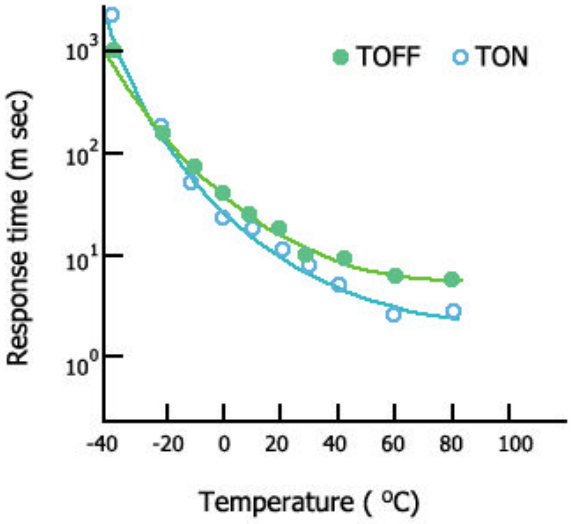


Figure 7. Temperature dependence of the response time of the TN cell.

2.3 Color TFT-LCD Module Structure

The basic configuration of a TFT-LCD is shown in Figure 8. Liquid-crystal is encapsulated between two glass substrates one is a TFT substrate and the other is a color-filter substrate. The color-filter substrate is also called the common electrode substrate. There are two parallel sheets of glass with liquid crystal injected between them. A crossed-polarizer system is shown here, corresponding to a normally-white display [21].

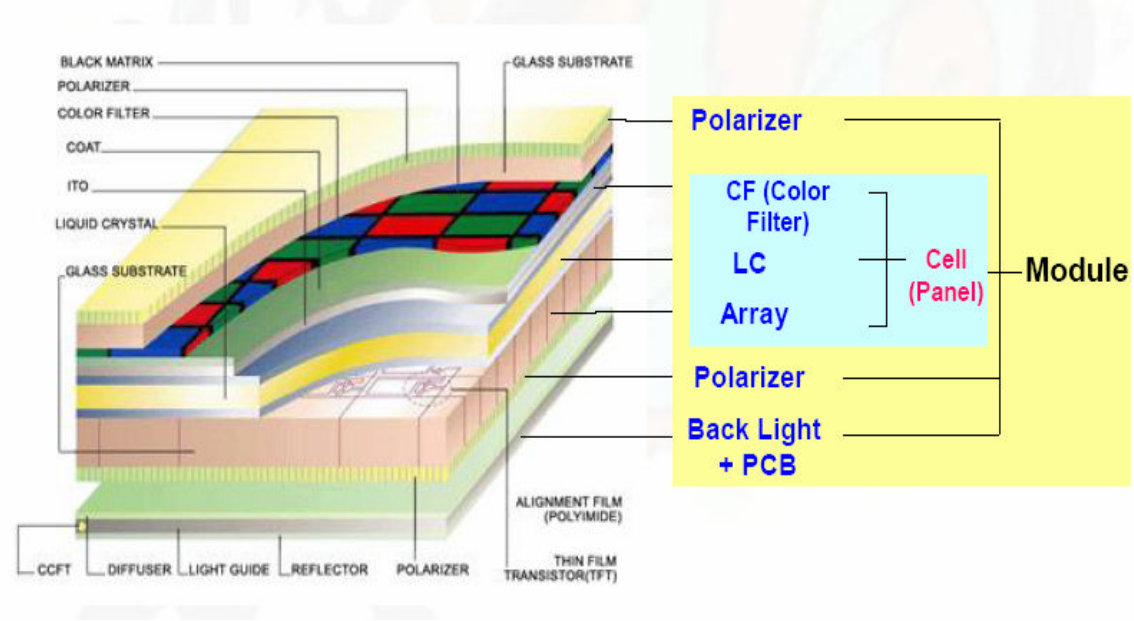


Figure 8. Top view of color TFT-LCD Module structure [21].

The transparent common electrode on this substrate is made of ITO (Indium Tin oxide), and is deposited on top of the color filter. In order to obtain good display quality, the cell gap of the liquid-crystal (i.e., the spacing between the two glass substrates) has to be precisely controlled to a specific value. This gap has to be uniform over the whole display area and reproducible from run to run. Therefore, transparent spacers such as plastic beads are placed on the surface of the glass substrate. The liquid-crystal cells are twisted-nematic type in which the director of the liquid-crystal molecules is twisted 90° between the TFT substrate and the common electrode substrate [11].

In Figure 9 it is a cross view of color TFT-LCD module. The crossed-polarizer system is shown in which the first polarizer works as a backlight polarizer and the other acts as an analyzer. In this system, light passes through the analyzer when there is no applied voltage on

the cell, and is blocked when the applied voltage is high enough to align the liquid-crystal molecules vertically. The liquid-crystal is anchored on the surface of the glass substrates so that its molecules are oriented to a proper direction. In order to set the anchoring direction, the glass substrate is coated with an organic film such as a polyi ride film and the surface of the film is rubbed with a fabric in a specific direction. The liquid-crystal molecules are tilted several degrees with respect to the glass surface. This tilt angle is called the pre tilt angle and plays an important role in determining the electrical and optical characteristics of the TFT-LCD, which will be described in the following sections.

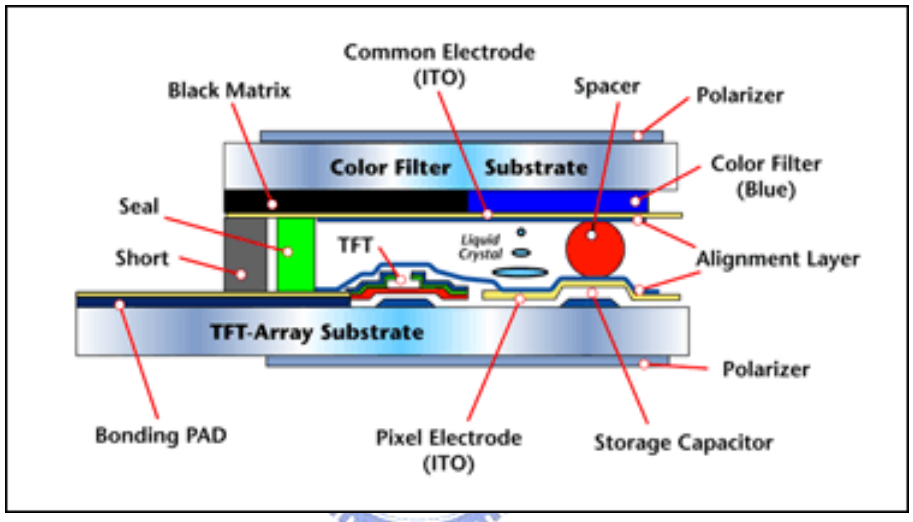


Figure 9. Cross section of Color TFT-LCD configuration [30].

2.4 TFT-LCD Panel System and Active Matrix Driving Method

The TFT substrate consists of a TFT array and a gray of external terminals on which column driver and row driver that are bonded to drive the TFT-LCD panel. The column and row driver are essentially scan generators for the horizontal and vertical bus-lines. These drivers are directly bonded to the glass with TCP (Tape Carrier Package) connectors, and they provide each pixel of the panel with video signals that are transferred to the panel via a video signal processor and timing controller. A schematic diagram of TFT-LCD module and controllers is shown in Figure 10.

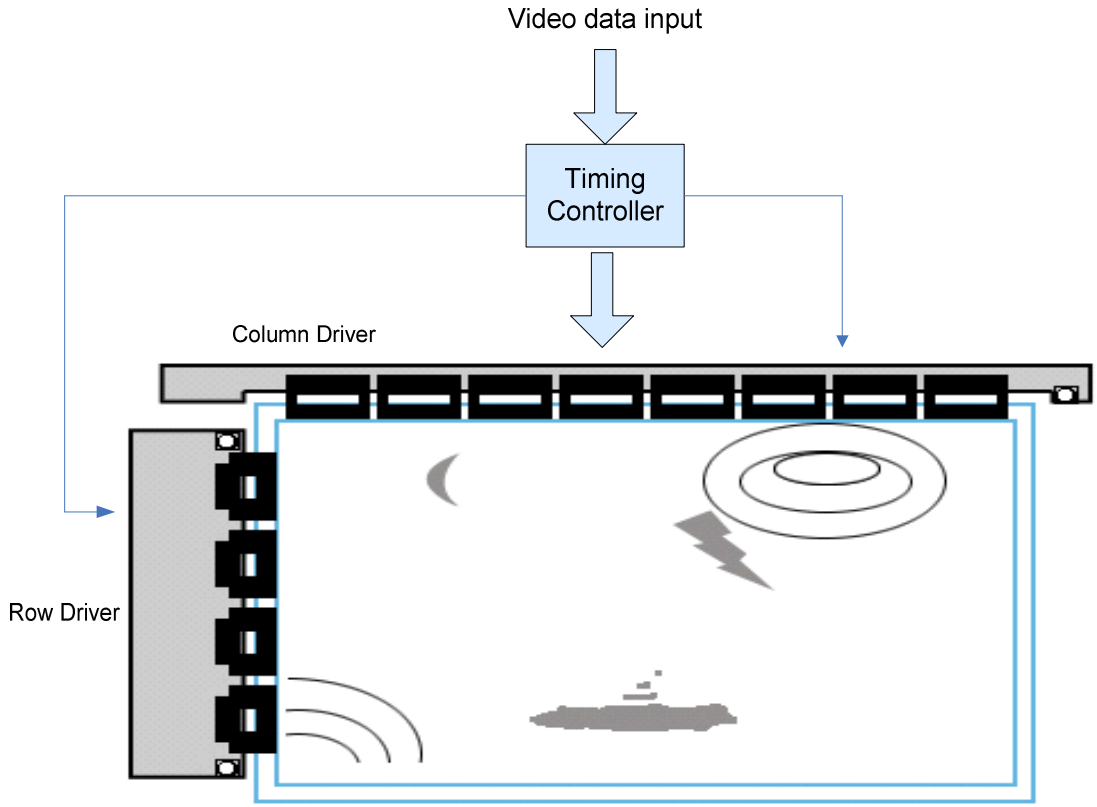


Figure 10. System block of TFT-LCD panel. [12]

In Figure 11 it shows that the brightness of the display module is much lower than that of the backlight illumination. Only 5% of the original brightness is being output from the front polarizer.

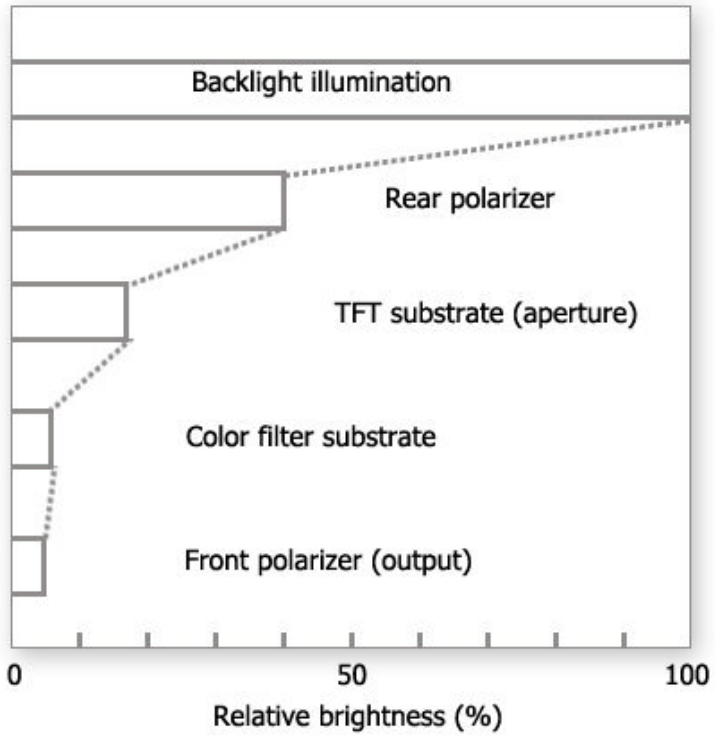


Figure 11. The brightness of the TFT-LCD module.

The backlight system can be either direct or indirect. With direct lighting, one or more fluorescent lamps are positioned directly beneath the rear polarizer. With indirect lighting, a light-guide is used to guide the light from lamp(s) situated beside it. The backlight illumination is attenuated as it passes through the display module. The maximum transmittances of the polarizer and color filter are one-half and one-third, respectively, resulting in a utility factor of one-sixth. The aperture ratio of the pixels further- reduces this factor. if an aperture ratio of 50% is assumed, the utility factor will be 8%. However, this is only the upper limit of the transmittance of the total system. In a practical system, the total utility factor is 3%-6% [10].

A TFT is formed at each intersection of these bus lines to turn on and off the voltage applied to the liquid-crystal cell. This cell is represented by an equivalent capacitance (C_{LC}) and in parallel this capacitor formed a storage capacitor (C_S) in which they improve the retention characteristics of the signal charge. See Figure 13.

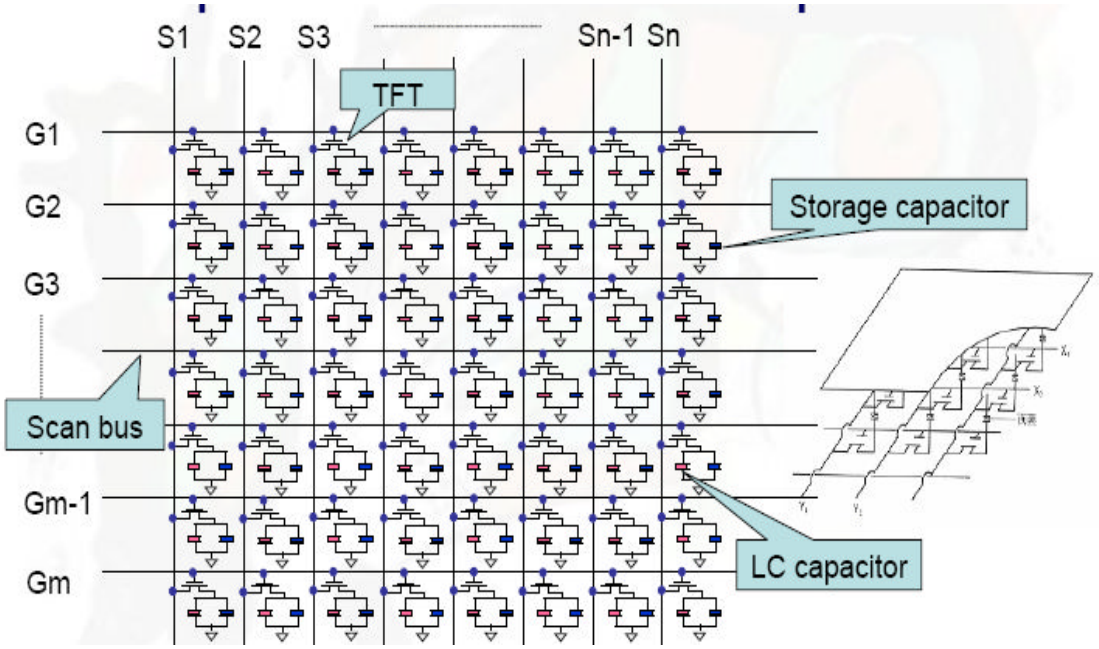


Figure 12. Schematic diagram of a TFT-LCD [21].

The color filter is formed in a striped R, G and B configuration. One pixel is formed by three dots. The display operates one line at a time then video signals are fed to the data bus lines simultaneously through a data buffer during the gate turn on time. The scan gate voltage pulse applied to a certain gate bus line opens the gates of the TFT connected to this bus line. The signal voltage is then applied to the pixel electrode of each dot on this gate bus line. The timing chart for scanning the TFT-LCD is shown in Figure 14 [7].

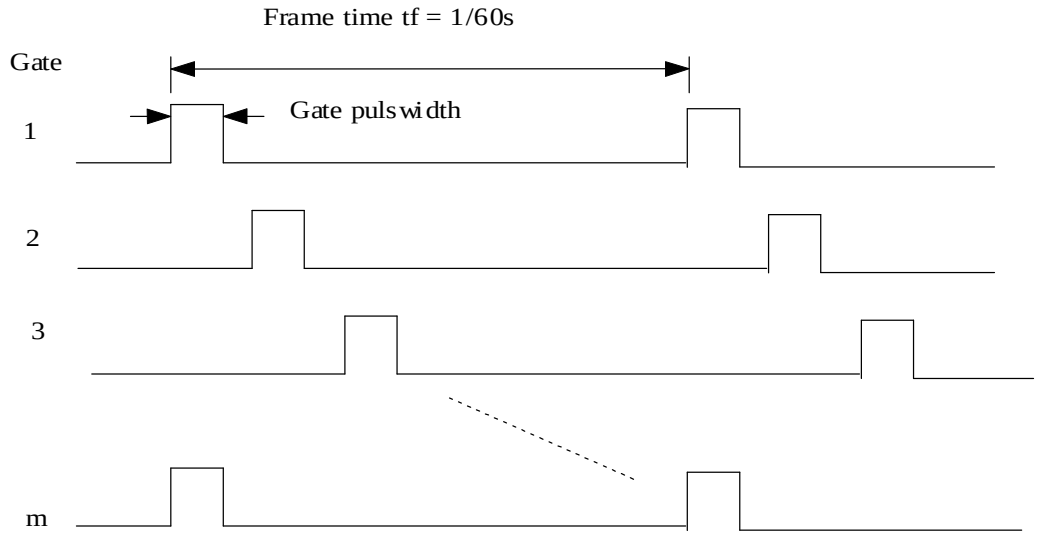


Figure 13. Timing chart of the 1024x768 resolution TFT-LCD panel.

The period *t* to turn on the TFT on the i-th gate line, given by Equation (5).

$$t_{CPV-on} = \frac{1}{mf_F}, \tag{5}$$

where m is the number of gate lines and f_F is the frame frequency, that means the panel is refreshed at a rate of f_F frames per second. Assume panel resolution is XGA (1024x768) display with 768 gate bus lines and 60 frames per second. If the frame frequency is 60 Hz and there are 768 gate bus lines, in formula (5) the t_{CPV-on} will be 2.16. During this time period, the charging of the capacitance (the liquid-crystal cell and the storage capacitor) has to be completed. After this charging period, the liquid-crystal cells on the *i*-th gate line are cut off from the data lines and the cells connected to the $(i+1)$th gate line are charged. The cell cutoff has to be perfect, i.e., the cut off cell has to keep its charged voltage until the next charging step takes place. If, for some reason, there is an increase of the off-current of the TFT, the signal voltage will discharge causing crosstalk and degraded display quality. In fact, the most frequent cause of crosstalk is an increase in leakage current due to the photocurrent induced by intense illumination from the backlight.

2.4.1 Gate Bus-line Delay

TFT-LCD panel likes the one that is shown in Figure 14 operated on a line-at-a-time basis. Each gate bus line is selected sequentially, and a voltage pulse is applied to the selected gate bus line. This pulse propagates down the bus line in which we assume is represented by the RC.

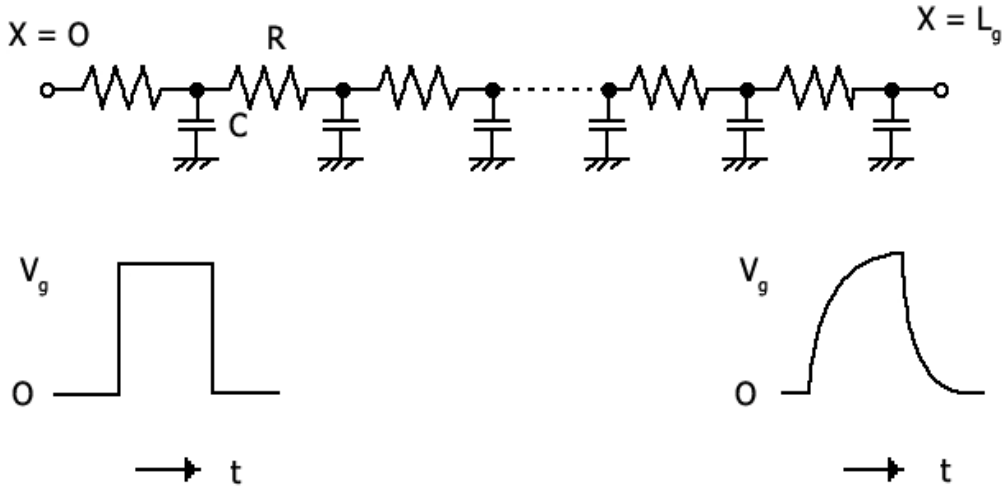


Figure 14. Distributed-constant representation of the fate bus-line.

Distributed-constant circuit is shown in Figure 15, where C and R are the capacitance and resistance per unit length. The rectangular gate pulse at the input is delayed and distorted as it travels along the gate bus line. The gate delay is defined as the time between the onset of the pulse at the starting point of the bus-line and the time when the pulse height at the end of the bus line reaches 90% of the pulse amplitude V_g [7].

$$t_d = 1.03RCL^2{}_g \tag{6}$$

where t_d is defined as the time at which the voltage reaches 90% of the pulse voltage. Therefore, t_d can be closely approximated by a simple expression of $RCL^2{}_g$. Another good approximation for t_d is $2RCL^2{}_g$, which corresponds to the time for 99% charging. A more practical expression for t_d (90%) is $R_pC_pn^2{}_p$ where R_p and C_p, are the resistance and capacitance per pixel (dot), respectively, and n_p is the number of pixels (dots).

In Equation (6), R is the resistance per unit length of the gate metallization. In high-resolution panels with over a thousand gate lines, the gate address time is 16.7 ms or less. In this case the gate metallization must be made with lower resistively metal. Since the

charging time of a unit cell of liquid crystal is approximately 13 μs, t_d of 1~2 us is more than reasonable.

2.4.2 LC Driving Voltage

Figure 15 is signal pixel electrical mode on TFT-LCD. $Vgate(i_{row})$ is scan voltage of row driver output on *j*-th gate bus line. $Vsource(j_{column})$ is video signal voltage of column driver output and $Vpixel(i_{row,}\, j_{colume})$ is voltage of pixel electrode. When $Vgate(i_{row})$ is high voltage (V_{GH}), the $TFT(i_{row},\, j_{column})$ turn on, and it will turn off when low voltage (V_{GL}).

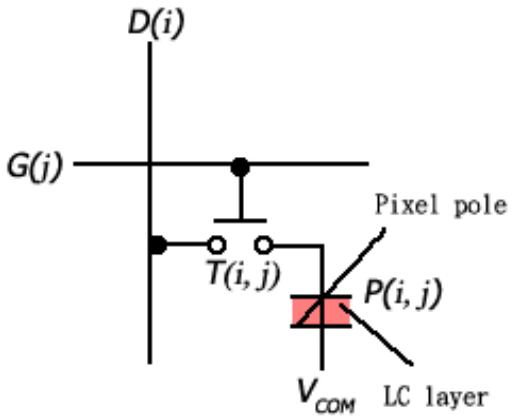


Figure 15. TFT-LCD single pixel electrical model.

In Figure 17, it's single pixel driving waveform shows us when gate bus-line turn on ($Vgate(i_{row})=V_{GH}$) the column driver output positively voltage and charging the storage capacitance (C_{st}) and liquid crystal (C_{LC}) between the T_1 period, the $V_{LC}(j_{column})$ voltage level is reference on common voltage (V_{com}) and charging to $V^{+}{}_{0}$, therefore across of the liquid crystal voltage is Equation (7)

$$V_{LC}(i_{row,}\, j_{colume}) \;=\; V_{source}(i_{row},\, j_{column}) - V_{com} \qquad (7)$$

After T_1 period the gate bus-line turn off ($Vgate(i_{row}) = V_{GL}$) the $V_{LC}(i_{row}, j_{column})$ must retain V^+_0 voltage level between T_2 period till the next time gate bus-line turn on (T_3). In T_3 period column driver output negative voltage and charge the C_{st} and C_{LC}. Let across liquid crystal voltage is $V_{LC}(i_{row}, j_{column}) = V^-_0$ and then gate bus-line turn off and $V_{LC}(i_{row}, j_{column})$ retains V^-_0 voltage level during T_4 period. Repeat sequence of T_1 to T_4 driving method is call pixel inversion. It is one of the driving methods on TFT-LCD. This driving method has some advantage like no flicker due to spatial averaging and highest quality image due to reduction in both horizontal and vertical cross-talk. Although this driving method has some disadvantages on TFT-LCD but for image quality issue, this driving method is widespread using on current TFT-LCD panel. In Table 1 to 4 we listed some of driving methods on TFT-LCD.

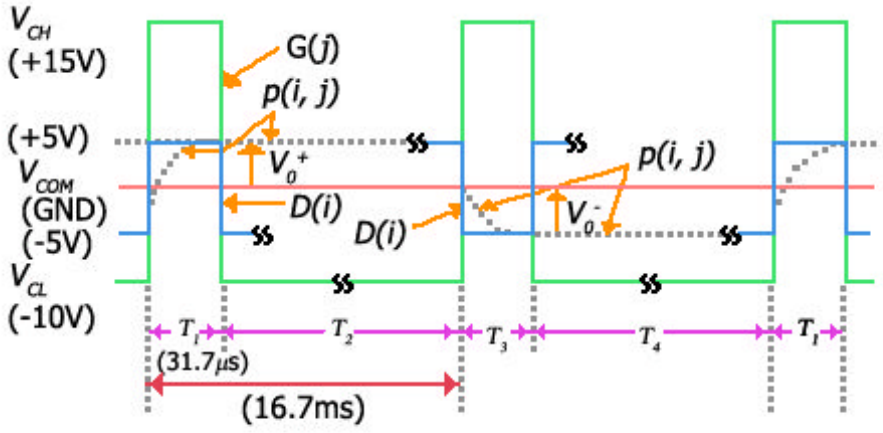


Figure 16. Signal pixel driving waveform.

2.4.3 Common Modulation

In Figure 17, we know that each pixel is connection to V_{com}, so it is a large electrode on TFT-LCD panel. V_{com} plays the role of reference voltage for all liquid crystal in the pixel and compensation for the coupled pixel voltage. In Equation (7) shows that if we want to change $V_{LC}(i_{row}, j_{column})$, we can change V_{com} voltage. Therefore if we want to reduce column driver driving voltage, we can modulation V_{com} voltage. See Figure 17. There are some

disadvantages on V_{com} modulation. For example it's only available by using frame and line inversion and poor image quality like flicker or crosstalk, poor power dissipation and low voltage output range. For these reasons, it is seldom used on TFT-LCD panel driving methods [2].

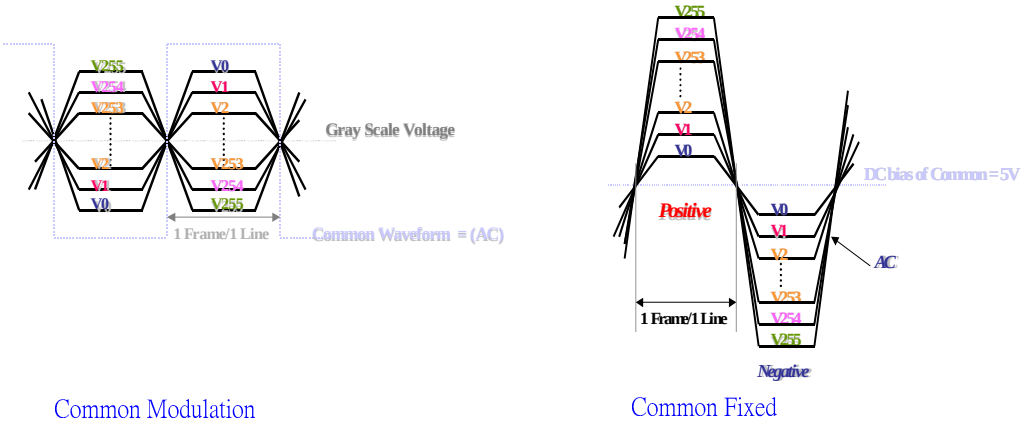


Figure 17. Common modulation and common fixed waveform.

Table 1. Frame inversion on TFT-LCD panel.

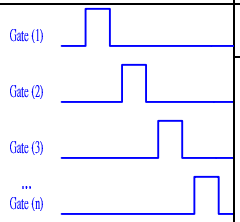
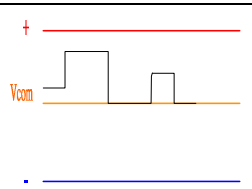
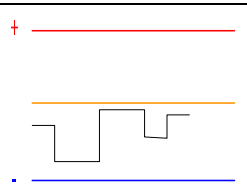
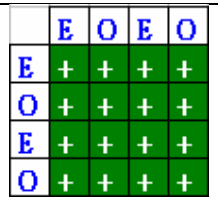
<table>
<tr><th rowspan="2">Polarity inversion</th><th colspan="3">Driving signal</th><th colspan="2">Pixel polarity</th></tr>
<tr><th>Gate bus-line</th><th colspan="2">Source bus-line</th><th>Frame M</th><th>Frame M+1</th></tr>
<tr><td>Frame inversion</td><td> 
</td><td>Frame M
 
</td><td>Frame M+1
 
</td><td> 
</td><td> 
</td></tr>
<tr><td colspan="6">Advantage:
➢ Low power operation.
Disadvantage:
➢ Due to lack of spatial averaging and slight transmissivity mismatches for + and – polarities so this method sensitive to Flicker.
➢ Reduce horizontal and vertical cross-talk.</td></tr>
</table>

Table 2. Line inversion on TFT-LCD panel.

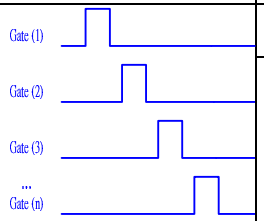
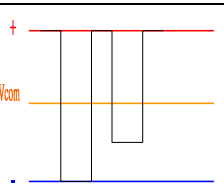
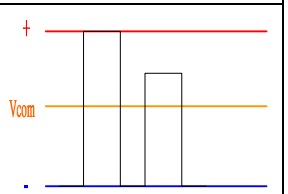
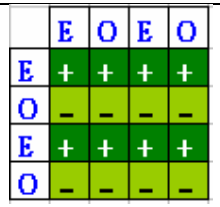
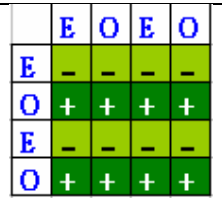
<table>
<tr><th rowspan="2">Polarity inversion</th><th colspan="3">Driving signal</th><th colspan="2">Pixel polarity</th></tr>
<tr><th>Gate bus-line</th><th colspan="2">Source bus-line</th><th>Frame M</th><th>Frame M+1</th></tr>
<tr><td>Line inversion</td><td> 
</td><td>Frame M
 
</td><td>Frame M+1
 
</td><td> 
</td><td> 
</td></tr>
<tr><td colspan="6">Advantage:
➢ Due to spatial averaging so this method can reduced flicker
➢ Reduce vertical cross-talk and
➢ Compatible with V_{com} Modulation Scheme.
Disadvantage:
➢ High Power Operation than frame or column Inversion and sensitive to horizontal cross-talk.</td></tr>
</table>

Table 3. Column inversion on TFT-LCD panel.

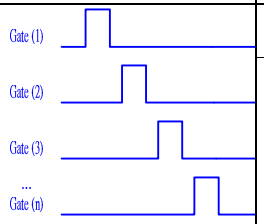
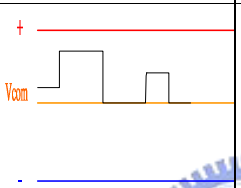
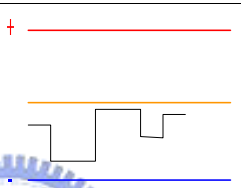
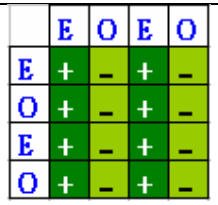
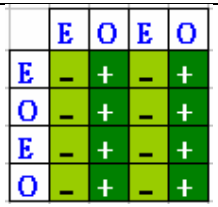
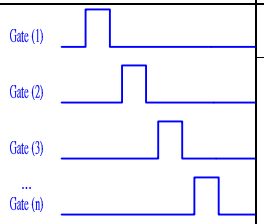
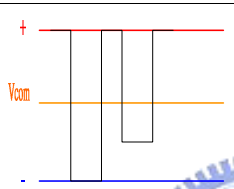
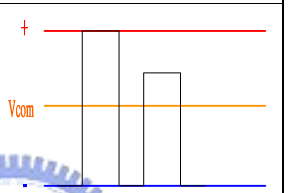
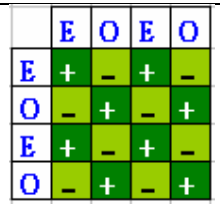
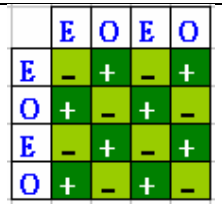
<table>
<tr><th rowspan="2">Polarity inversion</th><th colspan="3">Driving signal</th><th colspan="2">Pixel polarity</th></tr>
<tr><th>Gate bus-line</th><th colspan="2">Source bus-line</th><th>Frame M</th><th>Frame M+1</th></tr>
<tr><td>Column inversion</td><td> 
</td><td>Frame M
 
</td><td>Frame M+1
 
</td><td> 
</td><td> 
</td></tr>
<tr><td colspan="6">Advantage:
➢ Low power operation.
➢ Due to Spatial Averaging so further flicker reduction and greatly reduced horizontal cross-talk.
➢ Reduces component count and complexity.
Disadvantage:
➢ Requires high voltage column driver
➢ Incompatible with V_{com} modulation.</td></tr>
</table>

Table 4. Pixel inversion on TFT-LCD panel.

<table>
<tr><th rowspan="2">Polarity inversion</th><th colspan="3">Driving signal</th><th colspan="2">Pixel polarity</th></tr>
<tr><th>Gate bus-line</th><th colspan="2">Source bus-line</th><th>Frame M</th><th>Frame M+1</th></tr>
<tr><td>Pixel inversion</td><td> 
</td><td>Frame M
 
</td><td>Frame M+1
 
</td><td> 
</td><td> 
</td></tr>
<tr><td colspan="6">Advantage:
➢ Due to reduction in both horizontal and vertical cross-talk highest quality image.
➢ Due to spatial averaging so this method reduces flicker.
Disadvantage:
➢ Requires High voltage column driver.
➢ Incompatible with V_{com} modulation.
➢ Due to line inversion component higher power driving voltage.</td></tr>
</table>

2.5 TFT-LCD Panel Timing and Image Signal

In Table 5 it shows display timing. These resolutions and their timing are defined for computer monitors by the Video Electronics Standards Association (VESA) [14]. Displays based on one of these native resolutions are usually capable of accepting many input resolutions, scaling the source to match the display resolution. In TFT-LCD display usually using DE (data enable) signal represent the available image data in this period, and using pixel clock to be base timing unit to sample image data. For instance TFT-LCD panel resolution is design for SXGA application so it has 1280 pixels for column direction and 1024 scan line for row direction.

STV and STH signal are synchronous signal for row driver and row driver. Therefore after STV synchronization it will count to 1024 scan line by DE signal and each DE signal is contain 1024 x RGB pixels data. See Figure 18.

Table 5. VESA Timing Standard.

Format Nemonic	Aspect Ratio	Total area		Active area									
		Hor Total Area	Ver Total Area	Hor Addr Area	Ver Addr Area	Hor Blank Start	Hor Blank Time	Hor Sync Start	Ver Blank Start	Ver Blank Time	Ver Sync Start	Refresh Rate	Pixel Clock Rate
		(Pixels)	(Lines)	(Pixels)	(Lines)	(Pixels)	(Pixels)	(Pixels)	(Lines)	(Lines)	(Lines)	(Hz)	(MHz)
VGA		800	525	640	480	800	640	648	525	480	488	60	25.175
		832	520	640	480	648	176	664	488	24	489	72	31.5
	4:3	840	500	640	480	640	200	656	480	20	481	75	31.5
		832	640	640	480	640	192	696	480	29	481	85	36
SVGA		1056	628	800	600	800	256	840	600	28	601	60	40
	4:3	1040	666	800	600	800	240	856	600	66	637	72	50
		1056	625	800	600	800	256	816	600	25	601	75	49.5
		1048	631	800	600	800	248	832	600	31	601	85	56.25
XGA	4:3	1344	806	1024	768	1024	320	1048	768	38	771	60	65
		1312	800	1024	768	1024	288	1040	768	32	769	75	102.25
WXGA		1664	798	1280	768	1280	384	1344	768	30	771	60	65
	16:10	1696	805	1280	768	1280	416	1360	768	37	771	70	75
		1712	809	1280	768	1280	432	1360	768	41	771	85	94.5
SXGA		1688	1066	1280	1024	1280	408	1328	1024	42	1025	60	108
	5:4	1688	1066	1280	1024	1280	408	1296	1024	42	1025	75	135
		1728	1072	1280	1024	1280	448	1344	1024	48	1025	85	157.5
UXGA		2160	1250	1600	1200	1600	560	1664	1200	50	1201	60	162
	4:3	2160	1250	1600	1200	1600	560	1664	1200	50	1201	65	175.5
		2160	1250	1600	1200	1600	560	1664	1200	50	1201	70	189
HDTV	16:9	2080	1235	1920	1080	1920	160	1968	1200	35	1203	60	195
WUXGA	16:10	2080	1235	1920	1200	1920	160	1968	1200	35	1208	60	195

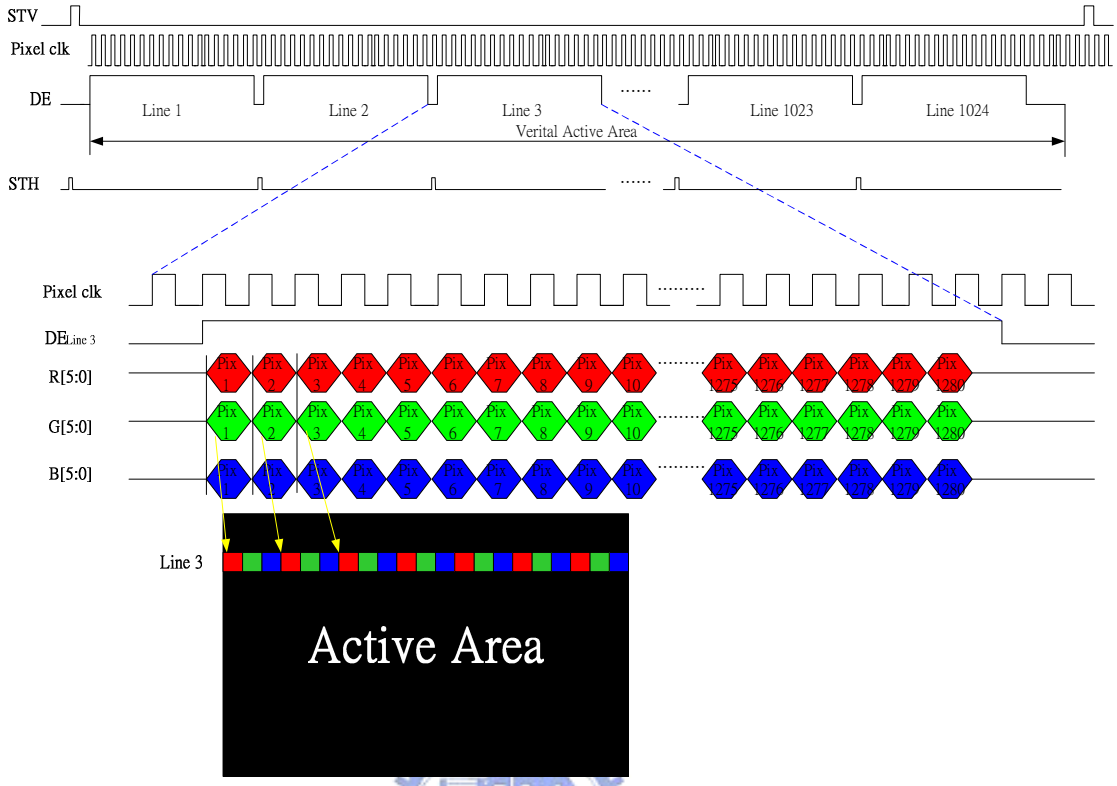


Figure 18. Digital Image Timing Diagram.

2.5.1 Color Space - CIERGB

The “color-matching experiment” was devised during the 1920s to characterize the relationship between physical spectra and perceived color. The experiment measures mixtures of different spectral distributions that are required for human observers to match colors. The statistics obtained by the observers who participate in these experiments. In 1931 the CIE standardized a set of spectral weighting functions that models the perception of color. See Figure 19. These curves are called the X(λ), Y(λ), and Z(λ) color matching functions (CMFs) for the CIE Standard Observer. The functions of the CIE Standard Observer were standardized based upon experiments with visual color matching. Research since then revealed the spectral absorbance of the three types of cone cells – the cone fundamentals [16]. We would expect the CIE CMFs to be intimately related to the properties of the retinal

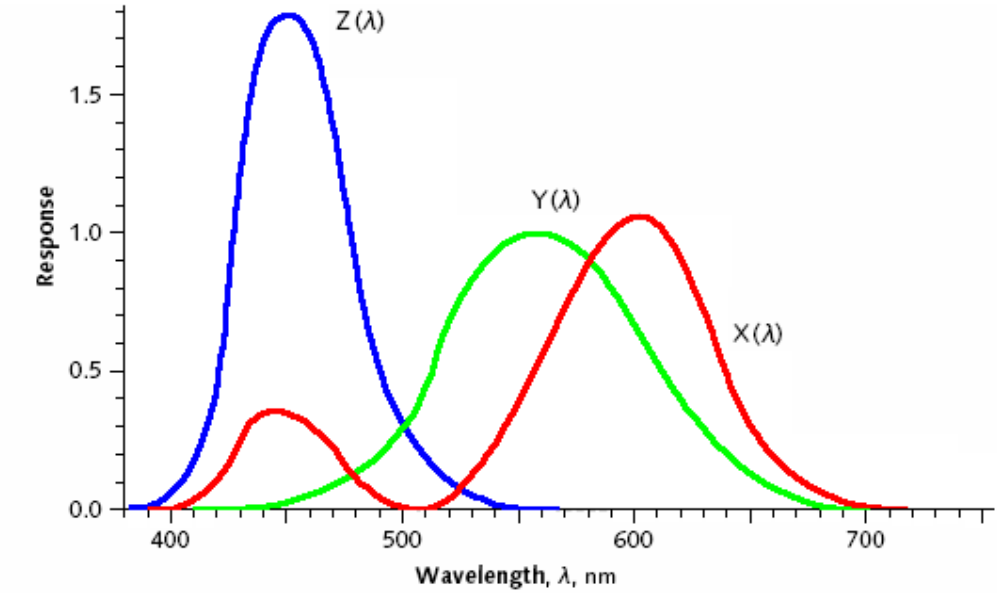


Figure 19. CIE 1931,color-matching functions.

photoreceptors many experimenters have related the cone fundamentals to CIE tristimulus values through 3×3 linear matrix transforms. None of the proposed mappings is very accurate, apparently owing to the intervention of high-level visual processing. For engineering purposes, the CIE functions suffice. The Y(λ) and Z(λ) CMFs have their own peak – they are "unimodal." However, the X(λ) CMF has a secondary peak, between 400 nm and 500 nm. This does not directly reflect any property of the retinal response; instead, it is a consequence of the mathematical process by which the X(λ), Y(λ), and Z(λ) curves are constructed.

Weighting a spectral power distribution under the Y(λ) color-matching function yields luminance (symbol Y). It is defined as radiance weighted by the spectral sensitivity function, the sensitivity to power at different wavelengths that is characteristic of vision. The luminous efficiency of the CIE Standard Observer, denoted Y(λ), is graphed as the black line of Figure 21 above. It is defined numerically, positive in everywhere, and peaks at about 555 nm.

The tristimulus values computed from the sum of a set of spectral power distribution is identical to the sum of the tristimulus values of each spectral power distribution. Due to this linearity of additive color mixture, any set of three components that is a nontrivial linear combination of X,Y, and Z – such as R, G, and B – is also a set of tristimulus values.

It is convenient for both conceptual understanding and computation to have a representation of "pure" color in the absence of lightness. The CIE standardized a procedure for normalizing XYZ tristimulus values to obtain two chromaticity values x and y.

Chromaticity values are computed by this projective transformation:

$$x = \frac{X}{X+Y+Z} = \frac{\left[x_r\left(\frac{Y_r}{y_r}\right) + x_g\left(\frac{Y_g}{y_g}\right) + x_b\left(\frac{Y_b}{y_b}\right)\right]}{\frac{Y_r}{y_r} + \frac{Y_g}{y_g} + \frac{Y_b}{y_b}} \tag{8}$$

$$y = \frac{Y}{X+Y+Z} = \frac{Y_r + Y_g + Y_b}{\frac{Y_r}{y_r} + \frac{Y_g}{y_g} + \frac{Y_b}{y_b}} \tag{9}$$

A third chromaticity coordinate, z, is defined, but is redundant since x + y + z = 1. The x and y chromaticity coordinates abstract values that have no direct physical interpretation.

A color can be specified by its chromaticity and luminance, in the form of an x, y, Y triple. To recover X and Z tristimulus values from [x, y] chromaticities and luminance, use the inverse of Equation (9)

$$X = x_r\left(\frac{Y_r}{y_r}\right) + x_g\left(\frac{Y_g}{y_g}\right) + x_b\left(\frac{Y_b}{y_b}\right) \tag{10}$$

$$Y = Y_r + Y_g + Y_b \tag{11}$$

$$Z = \frac{1-x-y}{y}Y \tag{12}$$

$$X + Y + Z = \frac{Y_r}{y_r} + \frac{Y_g}{y_g} + \frac{Y_b}{y_b} \tag{13}$$

A color plots as a point in a [x, y] chromaticity diagram, plotted in Figure 21. The spectral locus is a shark-fin-shaped path swept by a monochromatic source as it is tuned from 400 nm to 700 nm. The set of all colors is closed by the line of purples which traces spectral power distribution which combined long-wave and short-wave power but have no medium-wave power. All colors lie within the shark-fin-shaped region and points outside in this region are not colors.

This diagram is not a slice through [X, Y, Z] space! Instead, points in [X, Y, Z] project onto the plane of the diagram in a manner comparable to the perspective projection. White has [X, Y, Z] values near [1, 1, 1]. Attempting to project black, at [0, 0, 0], it would require dividing by zero: Black has no place in this diagram.

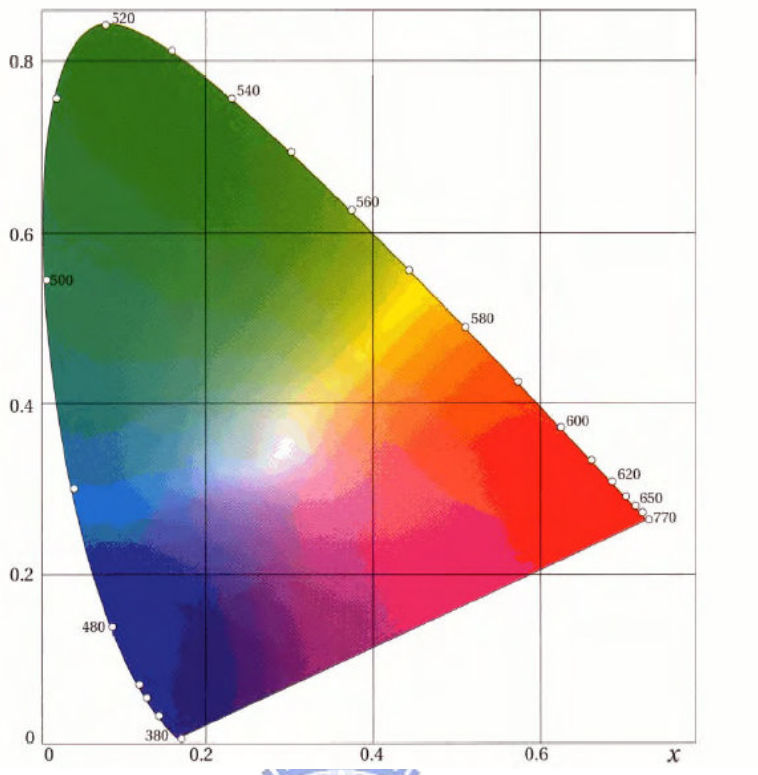


Figure 20. CIE 1931 2° [x, y] chromaticity diagram.

2.5.2 Color Image on TFT-LCD Panel

Three primary colors red, green and blue on [x, y] chromaticity diagram is fixed by color filter. And in Equation (11) we change luminance Y_r, Y_g and Y_b and quantification in each level from 0 to 255 gray level. See Figure 21, we can obtain 16.7($2^8 \times 2^8 \times 2^8$) million color on each pixel.

Therefore, in special area we can divide each pixel to red, green and blue sub-pixel. When pixel size is small enough and frame rate is more than human perception, we use luminance to control colors. See Figure 22.

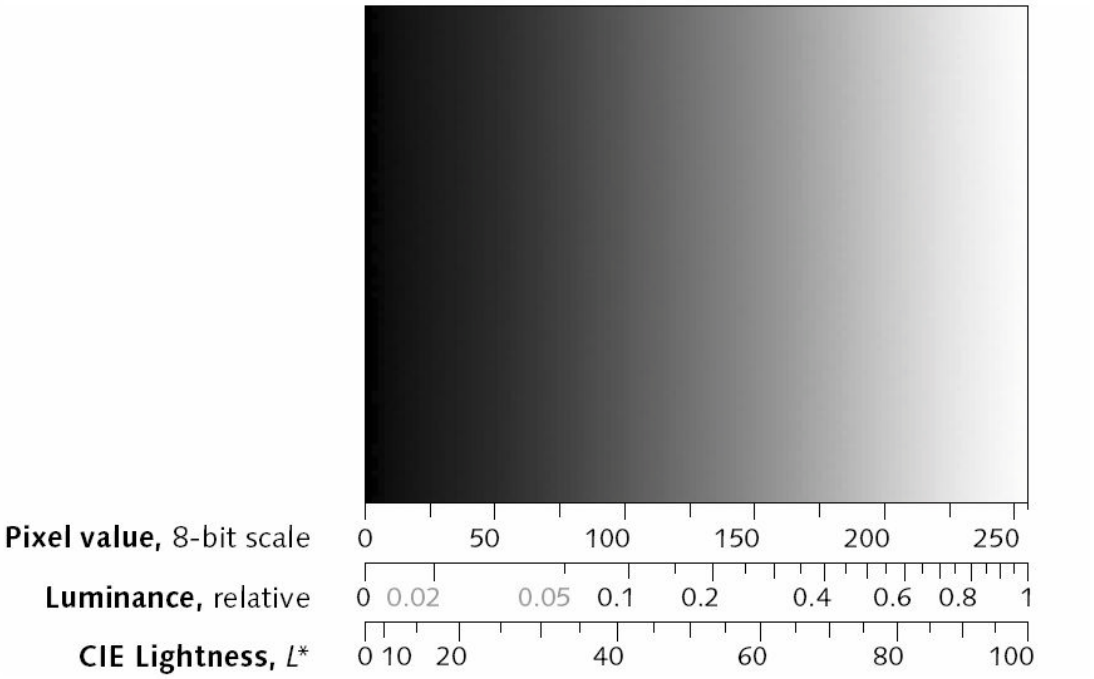


Figure 21. Grayscale ramp augmented with CIE lightness

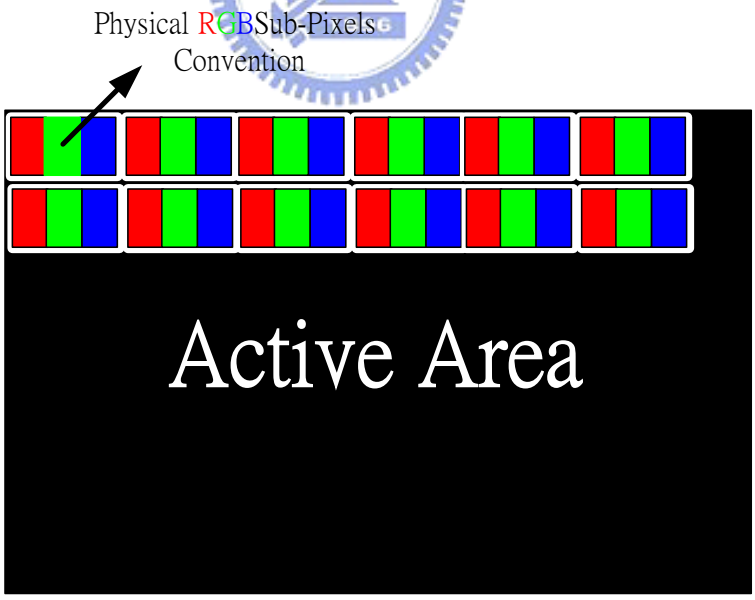


Figure 22. Pixel construct on color filter

2.6 TFT-LCD Panel Receiver and Transmitter Interface

TFT-LCD panel is use analog interface to be transmitter and receiver. The transmitter is using RSDS technology and receiver is LVDS technology. These technologies have some characteristics for low noise, low power and low amplitude for high-speed transmission application.

2.6.1 LVDS Interface

LVDS is a new data interface standard that is defined in the TIA/EIA-644 and the IEEE 1596.3 standards [32] [33]. It is essentially a signaling method used for high-speed transmission of binary data over copper. It uses a lower voltage swing than other transmission standards. This low voltage differential is what delivers higher data transmission speeds and inherently greater bandwidth at lower power consumption [13].

In LVDS driver, it converts a TTL/CMOS signal into a low-voltage differential signal. This differential signal can travel at rates up to 655 Mbps over media such as copper cables or printed circuit board traces to the LVDS receiver [15]. The receiver then translates the differential signal back into a TTL/CMOS signal. In addition, to delivering high speed, we use differential signal reduces the susceptibility to noise of the system and reduces EMI emissions. This results in a very cost-effective solution to some of the greatest bandwidth bottlenecks in many transmission applications. LVDS offers designers flexibility around their power supply solution, working equally well at 5V, 3.3V and lower. As a result, designers can reuse their LVDS solution even as systems move to lower voltages. Finally, LVDS has simple termination requirements usually one resistor at the inputs of the receiver compared to multiple resistor solutions for other standards.

2.6.2 LVDS Data Format

Two companies defined LVDS data format. One is National Semiconductor (NS). For notebooks and monitors, it uses 6 or 8 bits color bits for data representation. In TV applications, it uses 10 bits or larger bits. See Figures 23 and 24.

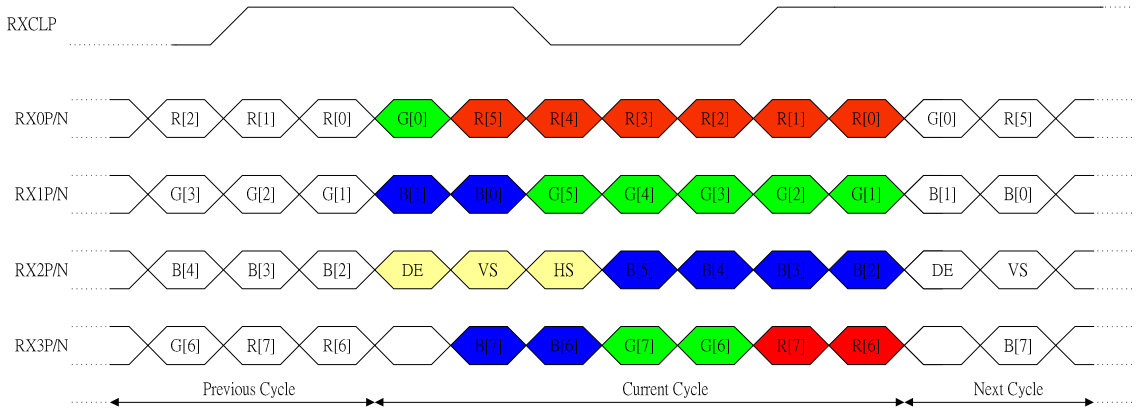


Figure 22. NS input format for 8 bits. [12]

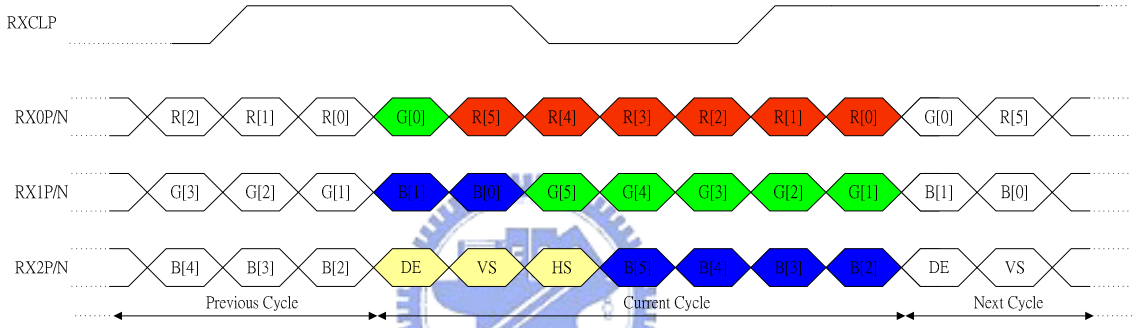


Figure 23. NS input format for 6 bits. [12]

2.6.3 RSDS Interface

Reduced Swing Differential Signaling (RSDS) is a signaling standard that defines the output characteristics of a transmitter and inputs of a receiver along with the protocol for a chip-to-chip interface between Flat Panel timing Controllers and Column Drivers [29]. The RSDS bus provides many benefits to the applications which include reduced bus width, it's enables smaller and thinner column driver boards, low power dissipation, eliminates EMI suppression components and shielding, high noise rejection, high throughput for high resolution displays. RSDS interfaces tend to be used in display applications with resolutions between VGA and UXGA.

2.6.4 RSDS Data Format

RSDS support 10 bits per R, G, B color mapping. 6 bits for primarily notebook PC and value line monitor application. 8 bit for premium line LCD monitors applications and 10 bit for LCD TV applications. See Figures 25 to 27

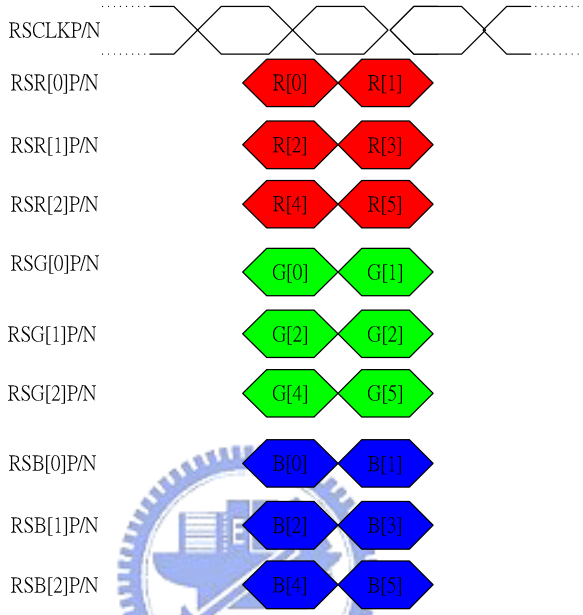


Figure 24. RSDS 6 bits data mapping.

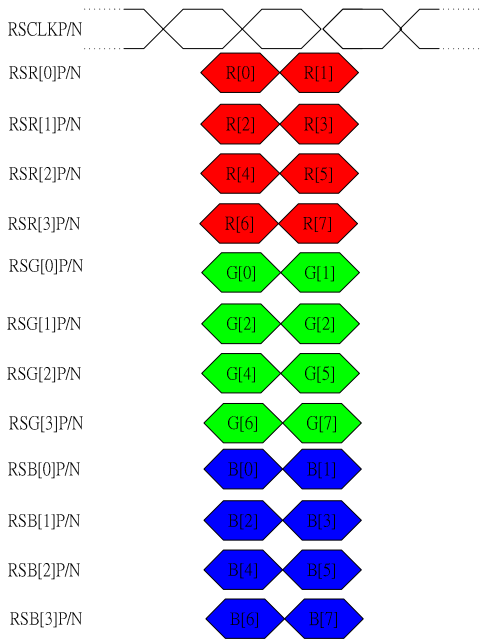


Figure 25. RSDS 8 bits data mapping.

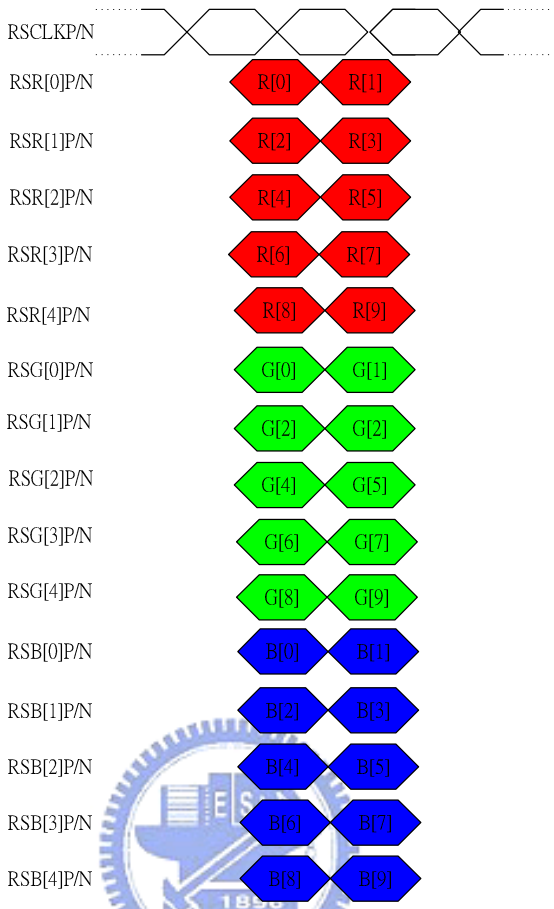


Figure 26. RSDS 10 bits data mapping.

Chap 3 TFT-LCD Control Timing Design

TCONs (Timing Controllers) are a key element in the “make-up” of LCD modules. They are essentially the “brains”, and control center to the heart of a TFT LCD module [22]. In the past and in the current generation, TCONs have been implemented through the use of fully custom ASIC devices. These custom ASICs can rarely be re-used in other LCD panel designs. Along with TCON, discrete LVDS devices are also required for interface and control of the LCD module. A new family of highly functional (programmable) and highly integrated TCON have now been developed which can be used on multiple LCD panel designs.

They can support non-standard resolutions and different LCD panel configurations from various LCD manufacturers. These TCON offer higher levels of integration resulting in smaller PCBs outlines and lower power consumption. This higher level of integration has been achieved by integrating an on chip LVDS Receiver. In addition to the higher levels of integration, a new high-speed low-voltage differential interface between the TCONs and column driver has also been developed. This new development, RSDS (Reduced Swing Differential Signaling), offers higher data transfer rates and enables higher display resolutions at lower EMI.

By providing a flexible and integrated TCON platform, LCD manufacturers can use the same device on multiple LCD Panel designs, result in shorter develop cycles and shorter time to market cycles.

In this thesis, we do not implementation LVDS and RSDS analog interface in our timing controller. We focus on digital section. In digital circuit, we divided it into 5 modules in our implementation. See Figure 28.

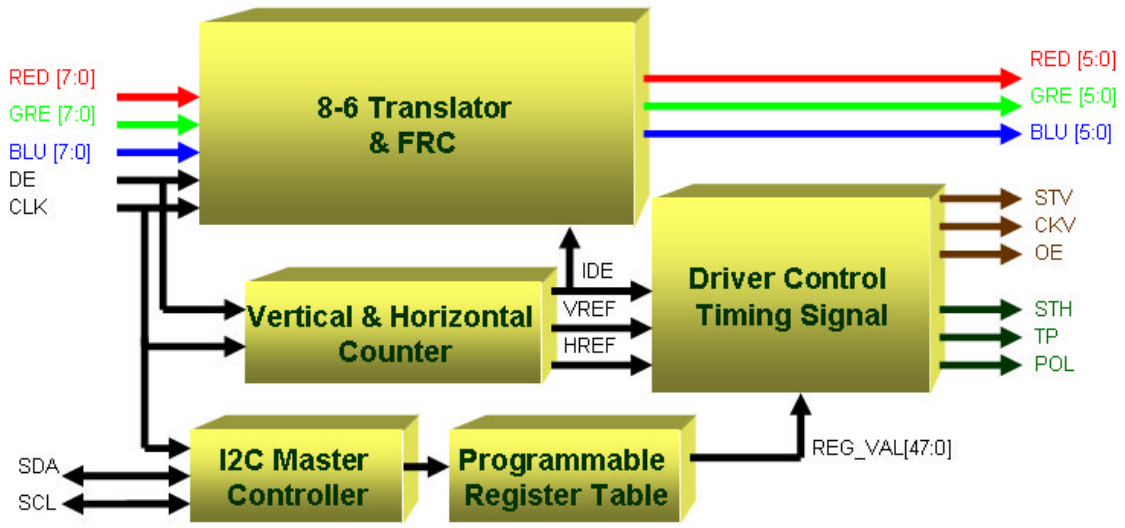


Figure 27. FPGA base timing controller architecture.

3.1 Design Flow

In this thesis, we are using Verilog hardware description language to accomplish controller circuit [17]. The verilog has become an industry standard as a result of extensive used in the design of integrated circuit chips and digital systems. Verilog comes into as a proprietary language supported by a simulation environment that was the first to support mixed-level design representations comprising switches, gates, RTL, and higher levels of abstractions of digital circuits. The simulation environment provided a powerful and uniform method to express digital designs as well as tests that were meant to verify such designs. After implementation circuit and simulation, we are using FPGA (Field Programmable Gate Array) to emulation our hardware circuit. See Figure 29.

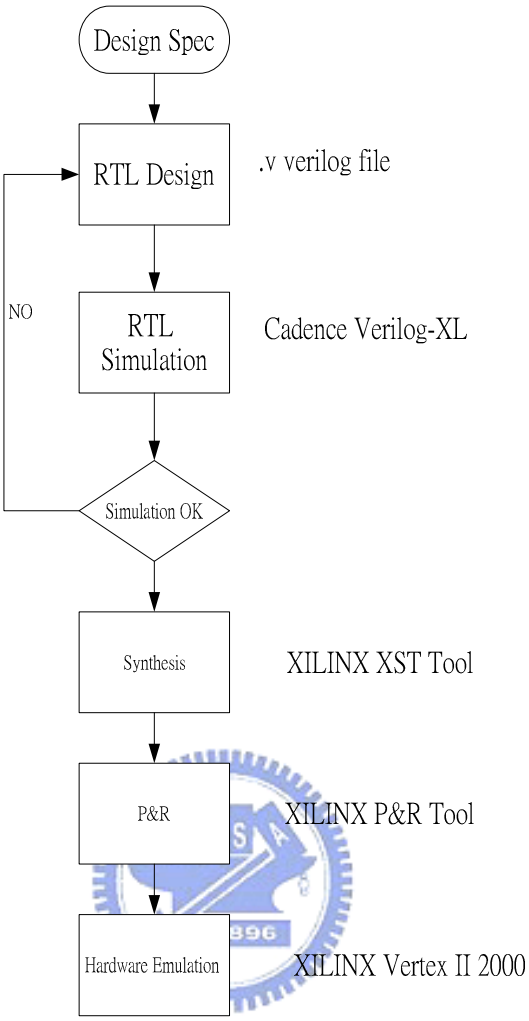


Figure 28. FPGA base design flow.

3.2 I^2C Protocol and Master Control Module

The I^2C bus is a very easy bus to understand and use. It uses a serial data line (SDA) and a serial clock line (SCL) for data transfers. All devices connected to these two signals must have open drain or open collector outputs. The logic AND function is exercised on both lines with external pull-up resistors [18].

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line and a byte-by-byte basis. Each data byte is 8 bits long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be

changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL high is interpreted as a command (sees START and STOP signals).

3.2.1 I²C Protocol

Within the procedure of the I²C bus, unique situations arise which are defined as START (S) and STOP (P) conditions. In START condition a high to low transition on the SDA line while SCL is high. In STOP condition a low to high transition on the SDA line while SCL is high. See Figure 30.

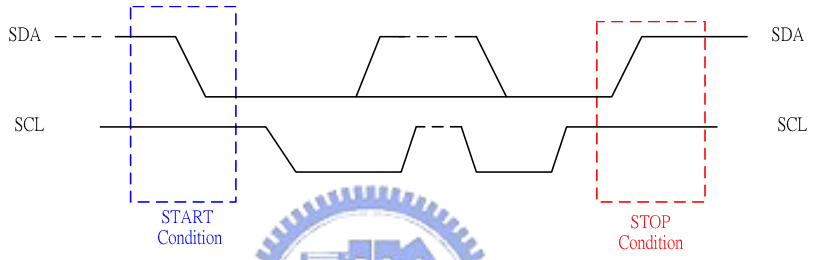


Figure 29. I²C START and STOP conditions.

SDA bus communication is established and 8-bit bytes are exchanged, each one being acknowledged by using a 9th data bit generated by the receiving party until the data transfer is complete. The bus is made free for use by other ICs when the 'master' releases the SDA line during a time when SCL is high. Apart from the two special exceptions of start and stop, no device is allowed to change the state of the SDA bus line unless the SCL line is low. If two masters try to start a communication at the same time, arbitration is performed to determine a "winner" (the master that keeps control of the bus and continue the transmission) and a "loser" (the master that must abort its transmission). The two masters can even generate a few cycles of the clock and data that 'match', but eventually one will output a 'low' when the other tries for a 'high'. The 'low' wins, so the 'loser' device withdraws and waits until the bus is freed again. There is no minimum clock speed; in fact any device that has problems to 'keep up the pace' is allowed to 'complain' by holding the clock line low. Because the device generating the clock is also monitoring the voltage on the SCL bus, it immediately 'knows' there is a problem and has to wait until the device releases the SCL line.

I²C address scheme is shown Figure 31. Any I²C device can be attached to the common I²C bus, they talk with each other, and passing information back and forth. Each device has a unique 7-bit or 10-bit I²C address. For 7-bit devices, typically the first four bits are fixed and the next three bits are set by hardware address pins (A0, A1, and A2) that allow the user to modify the I²C address allowing up to eight of the same devices to operate on the I²C bus. These pins are held highly to VCC, sometimes through a resistor or held low to GND. The last bit of the initial byte indicates that if the master is going to send (write) or receive (read) data from the slave, each transmission sequence must begin with the start condition and end with the stop condition. On the 8th clock pulse, SDA is set 'high' if data is going to be read from the other device, or 'low' if data is going to be sent (write). During its 9th clock, the master releases SDA line to accomplish the Acknowledge phase. If the other device is connected to the bus and has decoded and recognized its 'address', it will acknowledge by pulling the SDA line low. The responding chip is called the bus 'slave'. See Figure 32

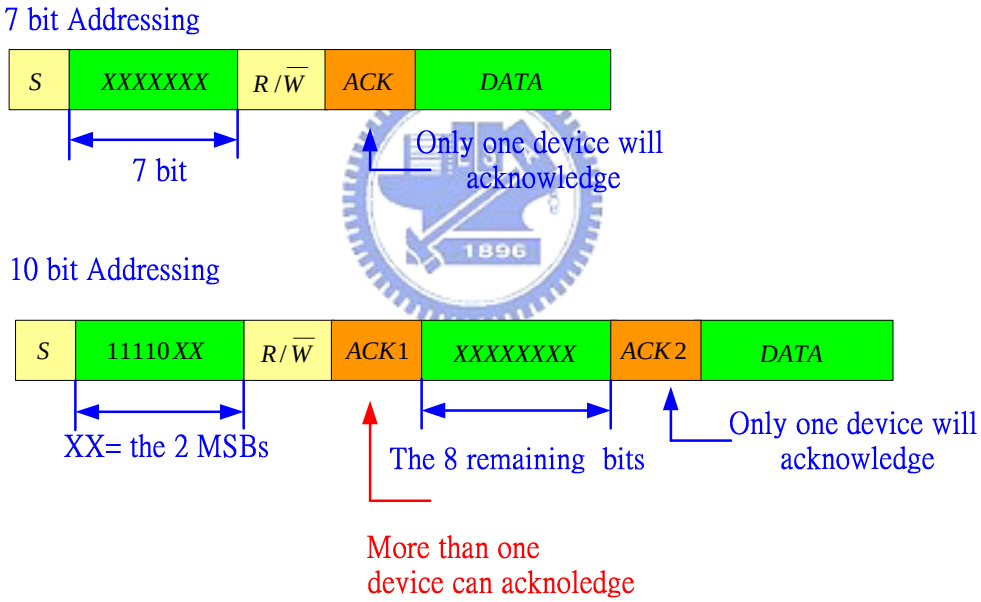


Figure 30. I²C **address scheme.**

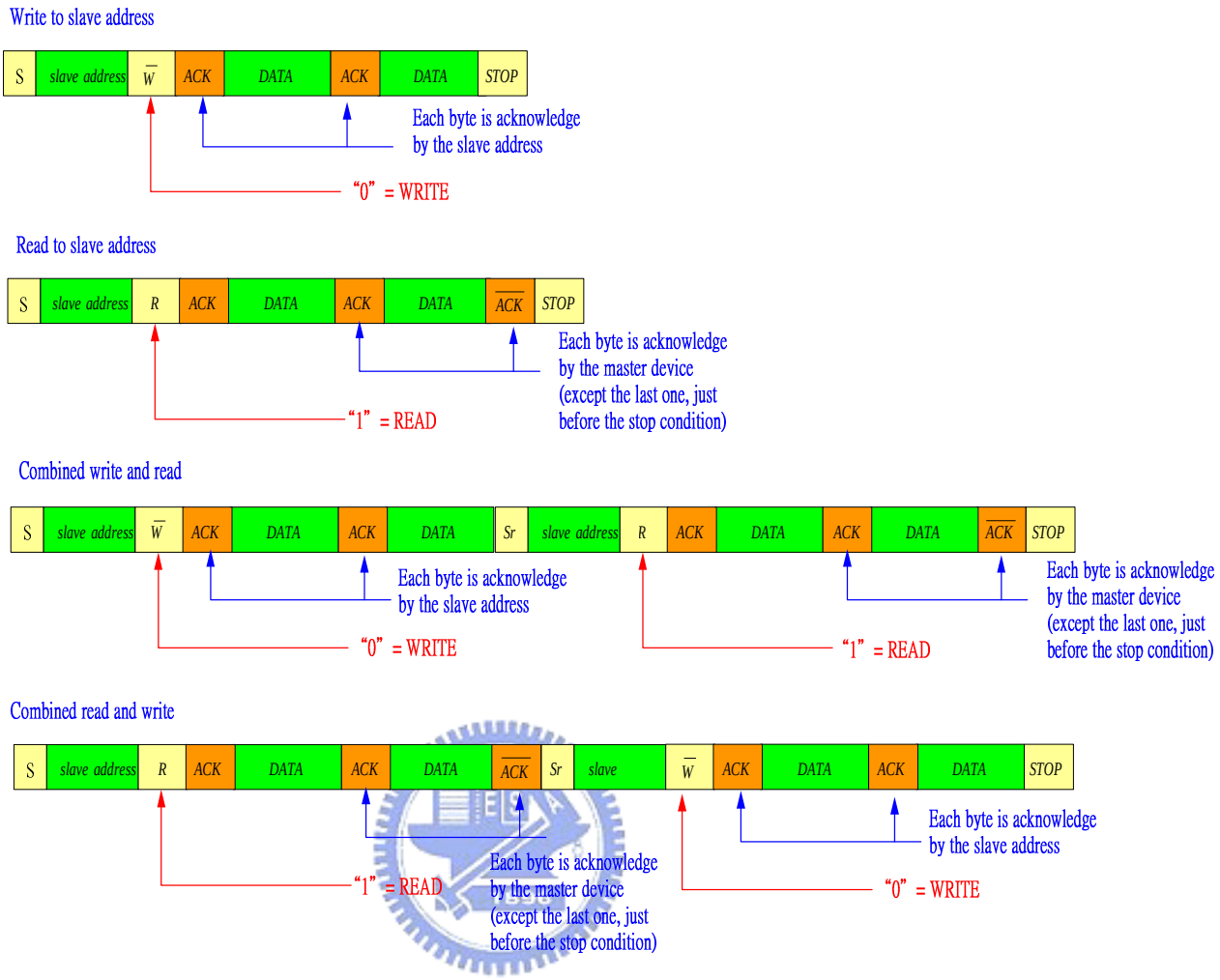


Figure 31. I^2C **read and write operation.**

3.3 Column and Row Driver Timing Control Signal

In driver timing control, we using 10 bits binary counter to counting vertical and horizontal value for line and pixel reference, for example, if resolution is SXGA (1280x1024) it means 1280 pixels per one line period and 1024 lines per one frame. Therefore, we can follow this rule to build internal DE and associate driver control timing. There are six control signals for column driver and row driver. There are STH, TP and POL control signals in column driver. STH is start plus for synchronization first column driver, and TP is transfer signal and it inform column driver latches the data register contents with leading edge, also it transfers the data to D/A converter and outputs the gradation voltage with the trailing edge. Due to bus-line delay in different panel process, so TP will have different timing, therefore we use 16 bits binary counter to control TP signal. POL is polarity reversal signal for pixel inversion control

in column driver. When POL is low, the odd number of higher gamma voltage in column driver is output and even the numbers of lower gamma voltage outputs are reference power supplies. On the other hand, when POL is high, the odd-number of lower gamma voltages in column driver are output and even-number of higher gamma voltage outputs are reference power supplies.

There are three control signals in row driver. That is STV, CPV and OE. STV is start plus for synchronization first row driver and output at the falling of CKV. CKV is vertical shift clock plus for row driver and OE signal cascade start plus and read at rising edge of CKV. In section 2.4.1 we know that gate bus-line delay problem, so OE signal is used to control gate line turn off to prevent two-gate bus-line turn on simultaneously. Therefore, CKV and OE will have different control timing for different process, so we use 16 bits binary counter to control. See Figure 33

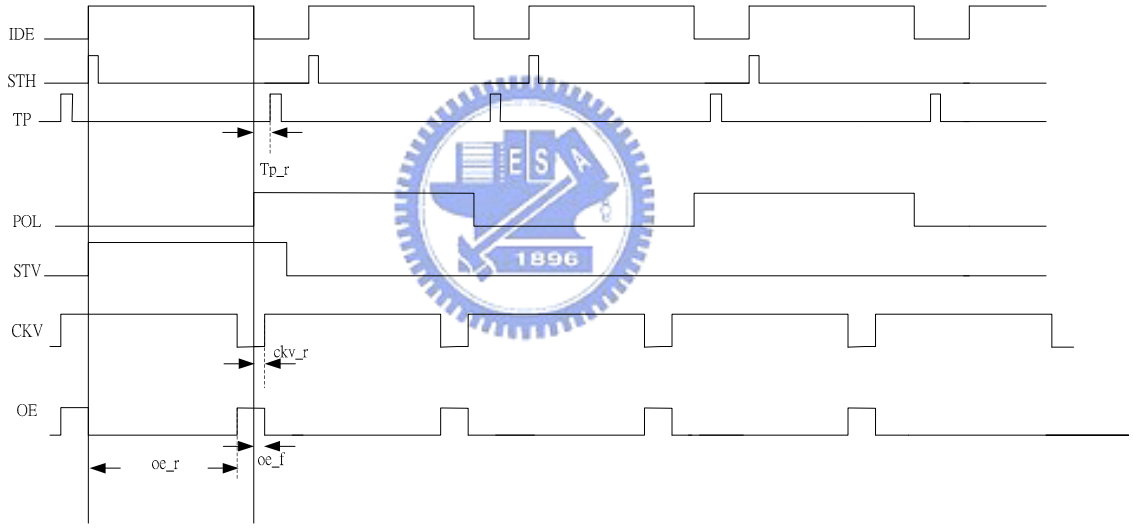


Figure 32. Driver control timing waveform.

3.4 Image Enhancing using Frame Rate Control Algorithm

In Electronic displays, are consumer electronics devices and because of that they are very price-sensitive, so they make available the minimum number of levels to represent maximum levels by using digital processing algorithms. TFT-LCD panels usually for monitor or notebook application are using 6-bit driver IC to generate 64 analog levels, so range is from 0 to 63. Again, image data input to TFT-LCD is 8-bit data stream but driver IC is 6-bit data output, so if we using frame rate control algorithm we can get 0 to 252 in 8-bit expression [19] [24].

Frame rate control algorithm also call dithering algorithm. This algorithm usually used in printing and electronic displays but they have two major differences as bellow:

1. The spatial resolution in the case of electronic displays is very close to the eye's resolution (to make the display as cheap as possible).
2. Unlike printing, electronic display is a time component that is available to the algorithm designer to play with.

Each of these factors is exploited to enhance the number of levels created for each pixel. Because the spatial resolution is just at the limit of visibility, and something similar to the spatial modulation encountered in the printing case is adapted for TFT-LCD displays, in technique that is called error diffusion. Again, the eye's behavior was exploited and knowing that because of its limited spatial resolution it will low pass filter the high frequency components, a noise signal was submitted. By controlling its parameters, the same goal was achieved. The error diffusion method does exactly the same thing, and it adds a noise that when integrated will have an error of zero. The area of integration is just a 2x2 window because this is the maximum that the eye can still do low pass filtering on. Pixels are further away than next to each other will not be perceived as being together and the eye will not perform any integration across them. Base on these characteristics we create 2 units 2x2 windows for 4 conditions spatial field. It chooses lower 2-bit from 8-bit image data input. In temporal field we extend 4 frames to average 6-bit image data for 8-bit expression. See Figure 34.

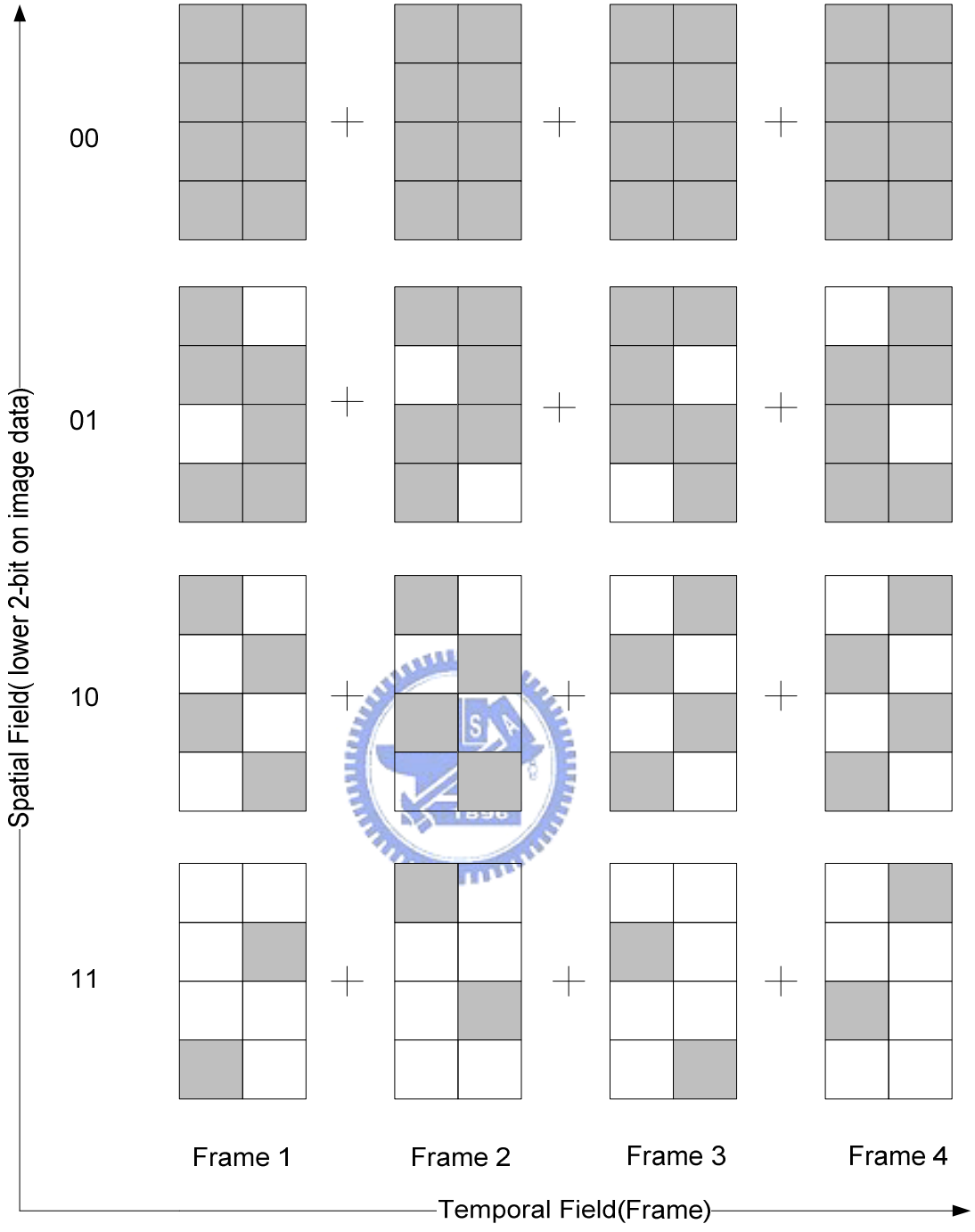


Figure 33. Spatial dithering and temporal averaging pattern on frame rate control

For instance if input image data is 130_d (10000010_b) gray level, the lower 2-bit is 10_b, in Figure 35 shows the sequence of the upper left pixel data is 128_d gray level form pixel 1 in frame 1 to frame 4, in pixel 1 the temporal average value is $\frac{128+128+132+132}{4}=130_d$. The other pixel has different data sequences, but it has some temporal average value of 130_d.

In Figure 36 it shows 2 units of 2x2 windows have some average value for 130d. The total spatial average is also 130d. Through all frames, the spatial averaging of 2 units of 2x2 windows is maintained as 130d.

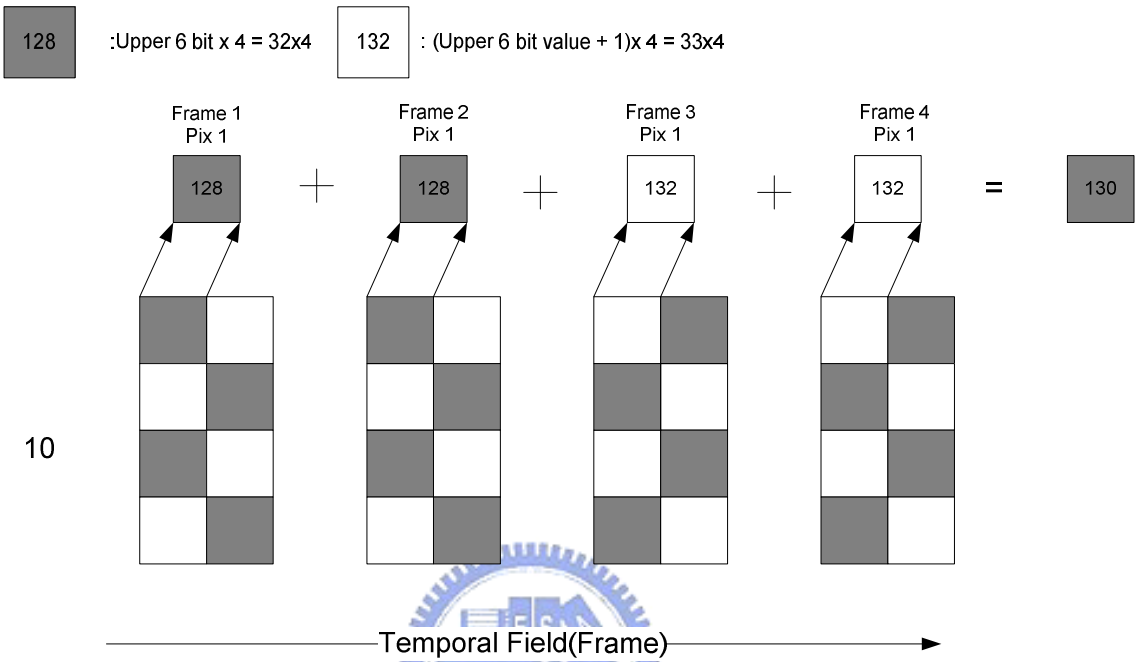


Figure 34. Temporal average of FRC to display luminance of gray level 130d

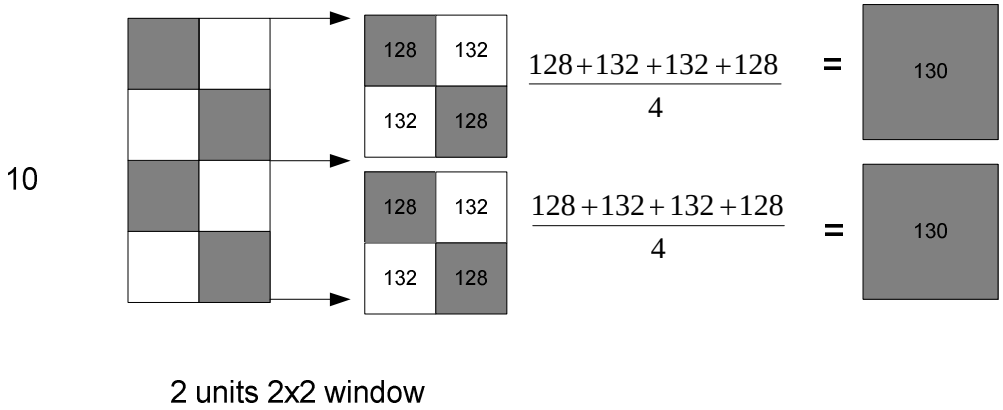


Figure 35. Spatial average of FRC to display luminance of gray level 130d

Chap 4 Simulation and Verification Results

In this chapter, we separate two sections to illustrate TFT-LCD control timing and frame rate control algorithm. First in RTL simulation we follow section 3.2 to design column and row driver control timing signal. In section 4.2 we create FPGA-based verification flow to verify frame rate control algorithm in TFT-LCD panel.

4.1 Simulation Results

In Figures 37 and 38, they show that I^2C master module access external EEPROM data from timing controller. After download external control timing value finish then generate STV, CKV and OE signal for control row driver and STH, TP and POL to control column driver, see Figure 39. It is described in details in sections 3.1.1 and 3.2.

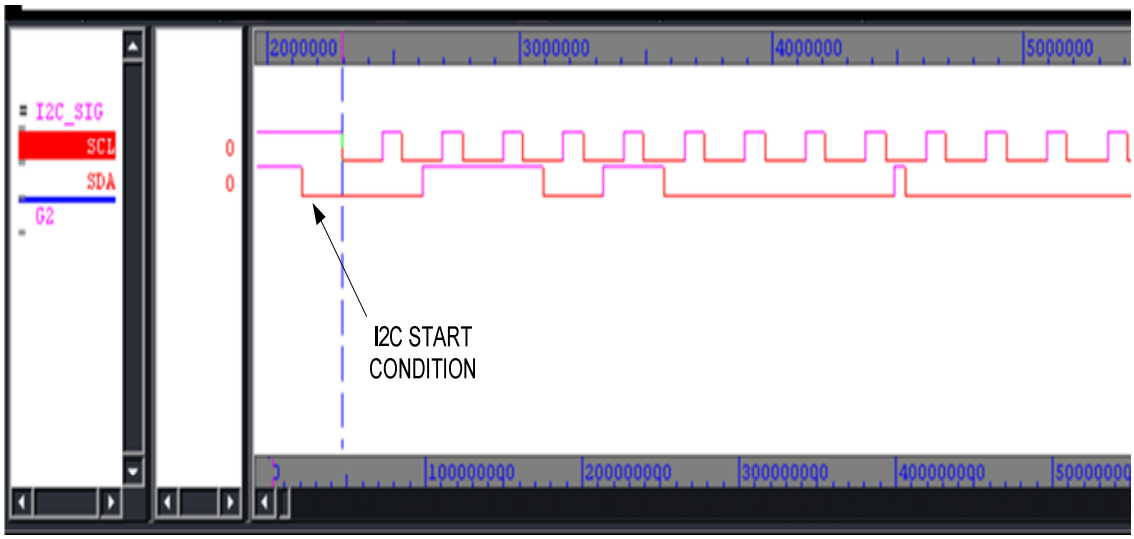


Figure 36. I^2C **master start condition simulation result.**

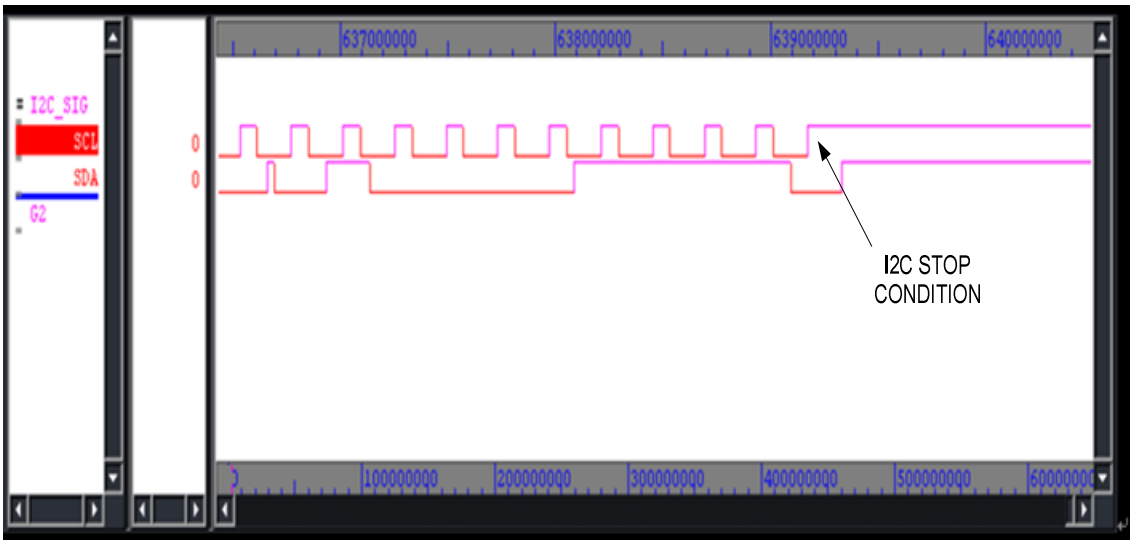


Figure 37. I^2C **master stop condition simulation result.**

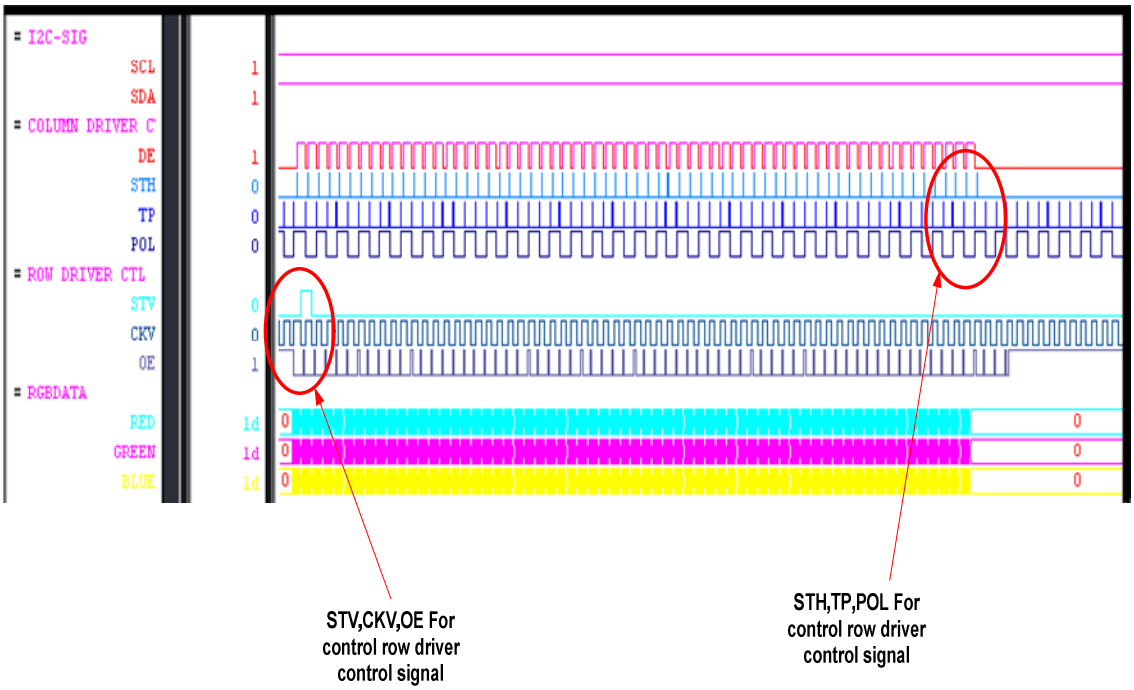


Figure 38. Row and column driver control signal simulation results.

4.2 Verification Flow and Results

In this section we illustrate the verification flow, see Figure 40. To control timing and frame rate control algorithm, first in timing control signal we use digital oscillator scope to probe STV, CKV and OE for verification row driver control timing and then probe STH, TP and POL for column driver control timing. See Figure 41.

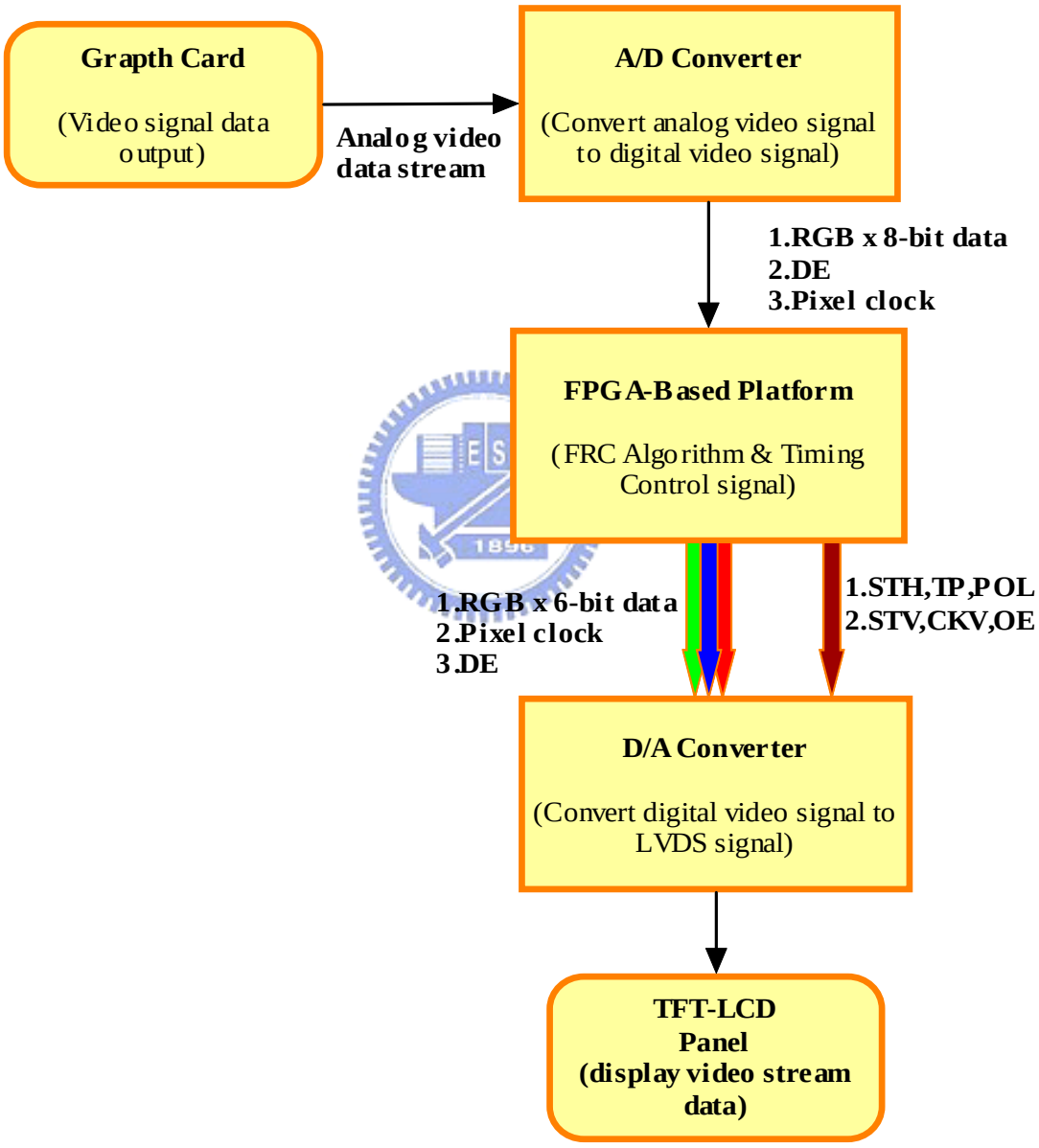


Figure 39. FPGA-Based verification flow.

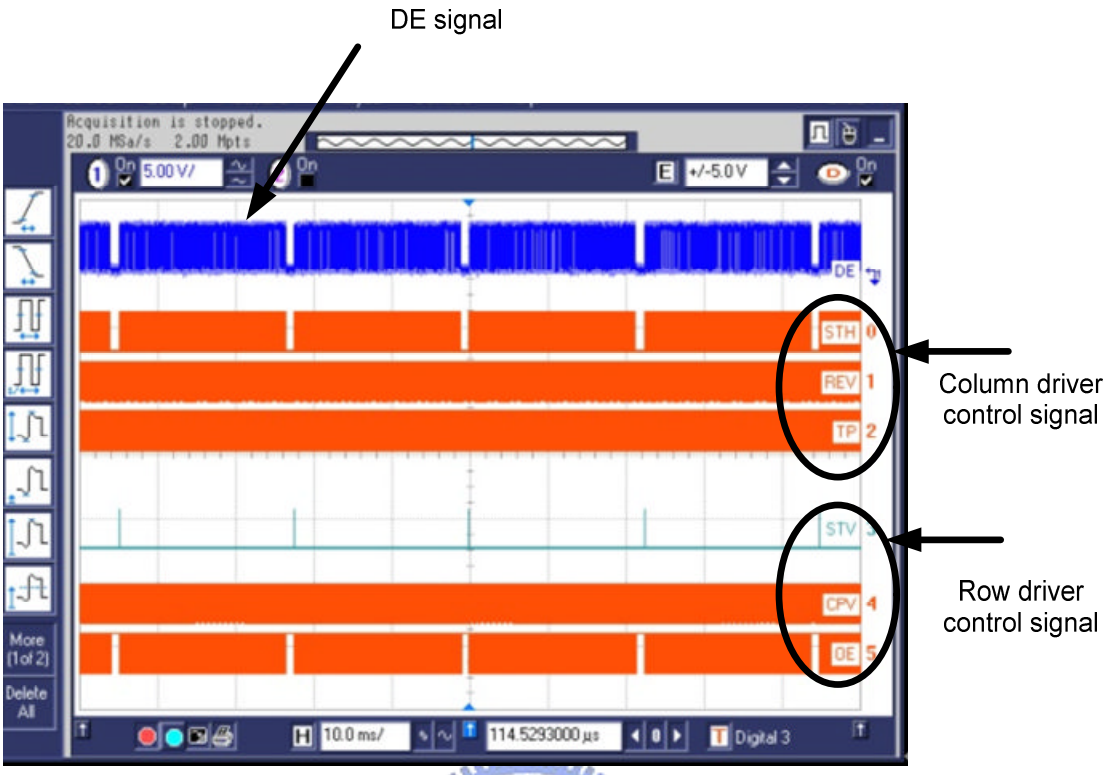


Figure 40. Row and column driver control signal for FPGA verification.

4.2.1 On-Panel verification

In this section we separate two experiments to verify FRC algorithm performance and display image. First we use color analyzer to measure luminance of FRC enable and disable. In Figure 42 we can see when FRC enable we can get smoothly luminance on TFT-LCD display.

The other experiment we generate vertical 256 gray levels pattern from graph card to verify frame rate control algorithm on panel. According to RGB data is from 0 to 256, so if we disable frame rate control algorithm the RGB data only can display from 0 to 63 gray levels, on the other hand we enable frame rate control algorithm we can obtain 8-bit expression image quality.

In this experiment we use two sets of TFT-LCD panels to compare with the enable and disable of the frame rate control algorithm. In Figure 43 we can compare the panel from the left is FRC algorithm disable and on the right is panel direct 8 bit vertical 256 grays from video card. The image quality is rather different. Again we redo experiment and enable FRC algorithm to see the panel image on the left in Figure 43 is almost the same as the panel on the right.

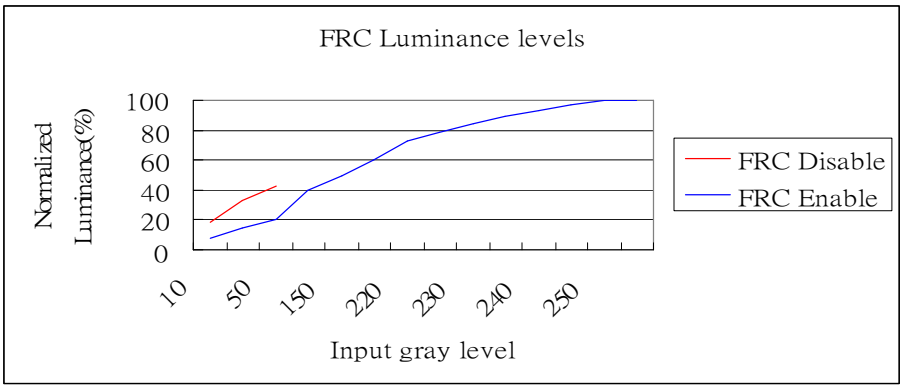


Figure 41. Compare FRC Luminance levels

Figure 42. Disable frame rate control algorithm on TFT-LCD panel.

Figure 43. Enable frame rate control algorithm on TFT-LCD panel.

Chap 5 Conclusions And Future Works

5.1 Conclusions

In this thesis, we improve that tradition timing controller problem and implementing new timing controller needs to be flexible and reusing for different panel process. Besides, in image quality, we use frame rate control algorithm to improve 262K colors to 16.2M colors.

5.2 Future Works

In this thesis, the frame rate control algorithm only can display 252 gray levels distinguishable, so it can not show full-color display. More research is needed to solve this problem and get perfect scheme for image quality. Furthermore, in modern TFT-LCD controller includes improvement of response time called “overdrive”. For instance DVD movies are filmed at 24 frames per second (fps), which are about 42 milliseconds. Because the shutter is open too much at that time, it is easy to understand that much of the faster moving imagery is recorded as smeared or blurred from the start, so to improve slow response time for TV application is what we need to do for future work.

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