國立交通大學

電機學院與資訊學院 資訊學程

碩 士 論 文

基於邏輯導向的生產排程知識庫系統

A Logic-Oriented Wafer Fab Lot Scheduling Knowledge-Based System

研 究 生：黃亮中

指導教授：曾憲雄 教授

中 華 民 國 九 十 五 年 六 月

基於邏輯導向的生產排程知識庫系統

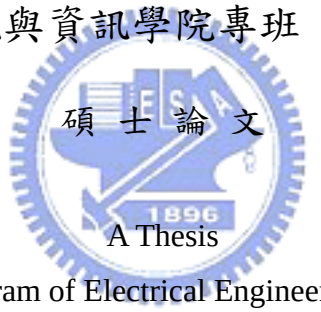
A Logic-Oriented Wafer Fab Lot Scheduling Knowledge-Based System

研 究 生：黃亮中　　Student：Liang-Chung Huang

指導教授：曾憲雄教授　　Advisor：Dr. Shian-Shyong Tseng

國 立 交 通 大 學

電機學院與資訊學院專班 資訊學程



碩 士 論 文

A Thesis

Submitted to Degree Program of Electrical Engineering and Computer Science

College of Computer Science

National Chiao Tung University

in Partial Fulfillment of the Requirements

for the Degree of

Master of Science

in

Computer Science

June 2006

Hsinchu, Taiwan, Republic of China

中華民國九十五年六月

基於邏輯導向的生產排程知識庫系統

研究生：黃亮中　　指導教授：曾憲雄 博士

國立交通大學電機學院與資訊學院專班資訊組

摘要

生產排程在半導體前段工廠中扮演相當重要的角色。好的排程機制可以依據真實現況，合理地調配整體資源，為企業帶來更佳的效益。由於多樣化的生產製程，生產環境的變化，以及不同的生產需求，在大部份的工廠中，由生產排程專家依據其知識及經驗法則來進行生產排程，藉以達成較優異的生產績效。但是，往往必須有足夠的產業經驗，並且歷經數年的實務上的磨練後，才能培養出一位稱職的排程專家; 除此之外，每個工廠的生產環境不同，所需的排程知識亦不盡相同，如何將排程知識保留下來，並且能輕易地傳承，也是這個領域非常重要的問題。

欲解決上述問題，我們提出一套完整的生產排程知識庫系統。在這篇論文中，為了讓生產排程的知識能妥善地保存、輕易地複製沿用以及簡單地表達，進而定義了以邏輯為導向，且易於機器讀取的圖形化 XML-based 知識表達法(以下簡稱為 XLogic)，知識擷取方法(以下稱為 KA)跳脫過去訪談式的 KA，提出圖形化的知識擷取工具(以下簡稱 Logic Map Builder)，直接由專家以圖形拖拉的方式維護排程知識元件(以下稱為 Logic Component)，產生排程邏輯圖(以下稱為 Logic Map)，不僅便於操作，並且更容易了解整個排程的過程。架構上可分為三階段：Meta Knowledge Acquisition(以下稱為 MKA)階段，專家可依據知識的重要度及順序性去建構 Meta Knowledge(以下稱為 MK)；KA 階段，由專家透過圖形化的 Logic

Builder 產生排程 Logic Map 進而轉換至 NORM-based 的規則庫中；排程推論階段，專家經由程式介面，輸入 Lot 相關排程資料後，再利用 DRAMA 推論引擎，推論產生排程結果。

針對排程精確度與準確度於系統與專家的比較上，我們發現大部分的情況皆能彼此符合。透過專家的回饋，證實本系統確實有保存延續排程知識之能力，並可作為新進排程人員之教學系統。

關鍵字：批量排程、知識擷取、知識庫系統

A Logic-Oriented Wafer Fab Lot Scheduling Knowledge-Based System

Student: Liang-Chung Huang Advisor: Dr. Shian-Shyong Tseng

Degree Program of Electrical Engineering and Computer Science
National Chiao Tung University

Abstract

Lot scheduling plays a very important role in semiconductor wafer Fab. According to the up-to-date market situation, a good Lot scheduling mechanism can help wafer Fab to meet constraints and allocate reasonable resources to gain higher profit. The complexity of wafer Fab Lot scheduling comes from various process flows, dynamic manufacturing environment and variant market requirement. In order to increase average performance, in the most wafer Fabs, the Lot scheduling expert (Production Controller) utilizes her/his knowledge and experience to do the Lot scheduling. However, it's difficult to train a comprehensive Lot scheduling human expert who must have enough industry experience and real Fab practice through a couple of years. In addition, different Lot scheduling know-how is required in different wafer Fab. How to share and re-use the existing knowledge is also the main issue in this domain.

For those reasons, we propose a suite of Lot scheduling knowledge-based system. In this thesis, we define a logic-oriented XML-based knowledge representation for the usage of knowledge repository, knowledge re-use and graphic expression. Besides, we design a graphic knowledge acquisition tool (Logic Map Builder) to elicit the Lot scheduling logic construction (Logic Map). Therefore, human expert can directly construct the Logic Map by the drag-drop function. There are three phases in this

system. Firstly, *Meta-Knowledge Acquisition Phase* is designed to acquire the importance and sequence of knowledge components, says meta-knowledge. Secondly, *Knowledge Acquisition Phase* is designed to acquire Lot scheduling Logic Map. Finally, *Lot Scheduling Phase* is designed for knowledge inference by DRAMA to receive relevant facts and generate Lot scheduling result.

The comparison of precision and accuracy between the results of our system and human expert is processed. The results of most cases are totally matched. From the feedback of human expert, we assure that the system not only has the capability to reposit and re-use Lot scheduling knowledge, but also can be used as a Lot scheduling tutoring system.

Keywords: Lot scheduling, knowledge acquisition, knowledge-based system

誌　　謝

重返學校進修，內心的想法與目標更為明確；兩年來豐碩而忙碌的學習過程，不僅完成學術上的研究，更進一步得到許多思考上的啟發，對於實務領域上的運用有著莫大的助益。

這篇論文的完成，首先必須感謝指導教授　曾憲雄博士的指導與勉勵，嚴謹而充實的學習過程，讓我得以順利完成此篇論文。同時必須感謝我的論文口試委員，李允中教授，林妙聰教授，以及廖岳祥主任，對此篇論文提出了許多寶貴的意見與精闢的建議，讓此篇論文更加充實。

此外，必須感謝實驗室中各位學長、同學平日的諸多協助，特別是威州、慶堯及衍旭學長對於此篇論文的方向與架構，提供許多珍貴的意見，在此深表感激。而實驗室中一起學習的夥伴 – 碧如、宗平、秀怡以及嘉妮學妹等人互相鼓勵與扶持，使得忙碌的碩士班生涯能夠愉快而紮實的度過。

最後，我要感謝我的母親　黃桂子、妻子惠珍及愛女榆庭對我的支持與鼓勵，這是引領我努力向前的最大動力。

黃亮中　　謹誌

交通大學　電機學院與資訊學院專班資訊組

中華民國九十五年六月

Contents

Lists of Figures

Lists of Tables

Chapter 1 Introduction

Generally speaking, scheduling means the temporal assignment of activities to resources where several constraints have to be fulfilled [13]. A lot of scheduling problems occurred in production environment and several approaches have been proposed. However, the scheduling problem of today's semiconductor wafer fabrication is more difficult than other production systems because of more complex and dynamic manufacturing environment. Since the traditional scheduling solution is difficult to incorporate with human expertise, it can not be easily utilized. Therefore, we propose a knowledge-base system solution.

In a mass production front-end semiconductor fabrication factory (referred to as wafer Fab hereafter), Lot scheduling plays a very important role in wafer Fab, where the product is processed by a batch size, says 'Lot'. According to the up-to-date customer-oriented market situation, a good Lot scheduling mechanism should help the wafer Fab to meet numbers of constraints and allocate reasonable resources to gain higher profit.

The manufacturing process flows are controlled by an existing information system, manufacturing execution system (referred to as MES hereafter), in most wafer Fabs. As we know, there are more than 300 process steps for a product and over 20 products in a wafer Fab at the same time. This brings a big challenge for Lot scheduling. As shown in Figure 1.1, every step is served by a machine group. Maybe more than one machine is setup in one machine group. For instance, one machine is

shutdown for preventive maintenance. It is possible that Lots are piling up for waiting process. Furthermore, numbers of re-enter flows are in a product flow and different products are using the same machine group in some steps and the recipes are maybe different. Many concerns, like product delivery date, machine utilization, Fab throughput, line balance, shared resource, manpower arrangement, process causal restrictions, etc., make the wafer Fab Lot scheduling problem be more and more complicated.

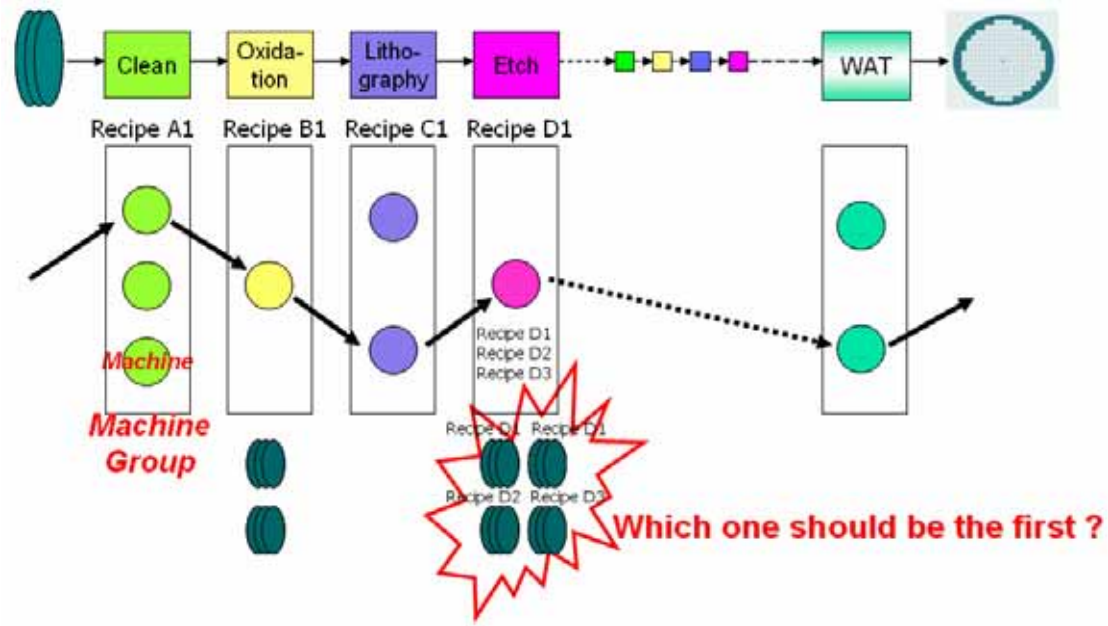


Figure 1-1 Flow Control and Lot Scheduling Problem

The overall complexity of wafer Fab Lot scheduling comes from the various process flows, dynamic and uncertain manufacturing environment and changeful market requirements.

There are a lot of performance criterions in wafer Fab manufacturing, including:

- On-time delivery
- High machine utilization
- High throughput
- Low product cycle time
- Low material and gas usage
- Well manpower arrangement

It is difficult to consider all the criterions in the same time. Especially, criterions are conflicted in some situations. For example, the criteria of product on-time delivery maybe decrease the utilization of machines which is one of the criterions. Thus, different situations adopt different criterions normally.

In order to increase average performance, in most wafer Fabs, there would be a specific human expert, called Production Controller who is responsible for the Lot scheduling job in the manufacturing management department, utilizes on her/his knowledge, including sales order requirement, inventory management, manufacturing status, flow control and process machine usage, and experience to make an adaptive Lot scheduling and generates a suite Lot scheduling logics to prioritize Lots. Of course, it is hard to train a comprehensive production controller, who must have enough industry experience and real Fab practice through a couple of years.

In order to avoid any product tardiness, resource waste and machine utilization lost, Lot scheduling is a daily operational planning in semiconductor wafer Fab. According to the short-term production requirement, production controller aggregates overall relative factors to do the Lot scheduling. The factors are:

1) Delivery due date of processing products: It is a commitment for customers.

2) Bottleneck machines: A machine will be identified as a bottleneck machine, if the queuing Lots of the machine are over its 2 days throughput.

3) Current manufacturing policy: It is a particular manufacturing policy for current business strategy. For example, a cost down policy is to reduce the times of recipe change. The policy will increase machine/manpower utilization and decrease material usage.

4) Engineering Lot control: It is an interrupt to process engineering Lot for some experiments. For a new process development, sometimes engineering department will borrow some machines for experiments and may affect the normal production.

5) Machine preventive maintenance arrangement: A periodic maintenance of machine is needed in order to guarantee the process quality of the machine

6) Process restriction: For example, the reticles which are used in photo-lithograph stage have a high cost and are unique at each layer. The process step must use its corresponding reticle.

7) Inventory handling: The outsourcing manufacture exists in some products process flows.

8) Uncertainty events: For example, unexpected machine down occurs. It means some process steps are stopped. Lot scheduling must respond this kind of special event.

Production controller makes good use of his/her expertise to decide which constraints or heuristics she/he should take. As shown in Figure 1-2, there are 5 Lots are waiting processes by bottleneck machine X. Production controller just concerns

the commitment of due date and product cycle time constraints. She/He adopts two sorting procedures - the most recent due date first and the shortest queuing time first. After series calculations, the prioritized result comes out.

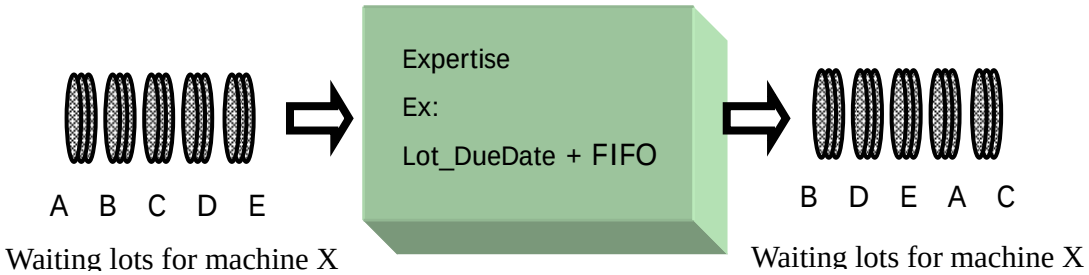


Figure 1-2 The Progress of Lot Prioritizing

For the purpose of solving complex Lot scheduling issue, we propose a LS-KBS (**L**ot **S**cheduling **K**nowledge-**B**ased **S**ystem) approach to utilize human expertise appropriately. First of all, we define a machine-readable XML-based knowledge representation to represent Lot scheduling logic for sharing knowledge. Secondly, depending on our knowledge representation, we provide a visual knowledge acquisition mechanism to elicit human expertise. More detailed reasons of adopting above approach will be shown in coming chapters.

The scope of this thesis is outlined here. In Chapter 2, some related solutions are classified and introduced. Besides, the motivation of this thesis is also described. In Chapter 3, the system architecture is explained. Chapter 4 introduces the knowledge representation and knowledge acquisition mechanism of our Lot scheduling knowledge-based system. Two cases are demonstrated for problem solving in Chapter

5. Evaluation is done in Chapter 6 and conclusion is given in Chapter 7.

Chapter 2 Related Works and Motivation

Scheduling of a semiconductor manufacturing factories is one of the most complex tasks encountered. Some related solutions are classified and introduced in this chapter. Besides, theoretical approaches to scheduling strive to search for an optimal solution; however, these approaches suffer from combinatorial complexity that can be proved to be computationally challenging [12][10]. Therefore, the motivation of adopting knowledge-based system is also described in this chapter.

2.1 Researches of Scheduling Problem in Generic Factories

In generic factory, there are few constraints in scheduling problems. Depending on factory types, researches focus on algorithm development, heuristics modeling and knowledge base implementation. Maybe the complexity is lower than the situation in the semiconductor wafer Fab, but some academic researches are still worthy of reference.

Factory Type

According to the dimensions of product quantity, process steps and the numbers of machine within a process step, factories could be classified into following types: (as shown in Table 2-1)

- Single-machine: Every job is finished by one machine.

- Parallel-machine: There are at least two identical machines with the same capability in the factory. Each job can be processed in parallel.
- Flow shop: Each job has the same process flow which has multiple steps. If every step is served by multiple machines, the factory type is a flexible flow shop.
- Job shop: It is different from flow shop because of multiple process flows in the factory.
- Open shop: It is a special case of job shop in which each job has its own process flow.

		Single machine within a process step	Multiple machine within a process step
Single Product	One-step process flow	**Single-machine Scheduling**	**Parallel-machine scheduling**
	Multi-steps process flow	**Flow shop scheduling**	**Flexible flow shop scheduling**
Multiple Products	One-step process flow		
	Multi-steps process flow	**Job shop scheduling**	**Job shop with duplicate machine scheduling**
	Without a specific flow	**Open shop scheduling**	

Table 2-1 Classification of Scheduling Problem

Algorithmic Approach

Some mathematical programming and algorithmic approaches have been

developed for finding optimal solutions. The earliest papers could be due to Dantzig, Fulkerson, and Johnson (1954). The cutting-plane method was introduced. The famous Johnson algorithm is used to solve the problem with 2 sequential machine tasks.

Heuristics Approach

For improving specific performance criteria, some dispatching rules were brought out. The strategy of dispatching rules is designed to simplify the scheduling problem by sorting relevant attributes of the index. For example, in flow shop factory, the shortest processing time first (SPT) was proven as one of the best ways of decreasing product cycle time. As shown in Table 2-2, the characteristics of these dispatching rules are not only easy to understand, but also efficient in calculation.

Rule	Stand For	Description
SIRO	Service in random order	Random job selection
FCFS	Fist Come First Served	Shortest queuing time job is processed first
SPT	Shortest Processing Time	Shortest processing time job is processed first
LPT	Longest Processing Time	Longest processing time job is processed first
EDD	Earliest Due Date	Earliest due date job is processed first

Table 2-2 Well-Known Dispatching Rules in Generic Factory

Some researches, in this approach, designed individual heuristic rules in a single critical stage – photo stepper machines [7]. For the purpose of real-time scheduling, the methodology considers the line balance and equipment efficiency indices to provide a Queue Selection Rule (QSR) for Lot selection of a stepper processing and a

Server Selection Rule (SSR) for Lot dispatching of steppers.

2.2 Researches of Scheduling Problem in Wafer Fabs

Heuristics Approach

Some researches also inherit the concept of heuristics in generic factories. The Lot scheduling in wafer Fab also use simple logical rules to decrease the complexity of computation and space. Furthermore, the rules are designed more close to wafer Fab process operations and special environment features. Although it is not necessarily an optimal solution and does not work in other environment, it is still frequently applied due to efficiency calculation and easy understanding.

As shown in Tabe2-3, the dispatching rules were summarized by [9]

Rule	Stand For	Description
SIRO	Service in random order	Random job selection
FCFS	Fist Come First Served	Shortest queuing time job is processed first
SPT	Shortest Processing Time	Shortest processing time job is processed first
LPT	Longest Processing Time	Longest processing time job is processed first
EDD	Earliest Due Date	Earliest due date job is processed first
CR1	Critical Ratio 1	Critical ratio means the ratio of due date related objective date to the residue time ＞ 1, can be finished before due date. ＝ 1, can be finished on time ＜ 1, it's critical job and maybe will delay
CR2	Critical Ratio 2	Like CR1, but just for current step
MS	Minimum Slack Time First	Smallest due date related objective date job is processed first
MWKR	Most Work Remaining Time First	Largest working remaining time job is

		processed first
LWKR	Least Work Remaining Time First	Opposite to MWKR
MOPNR	Most Operations Remaining	Most operational steps job is processed first
WINQ	Work In Next Queue	The job with fewer jobs in next queue is processed first.
HV	Highest Value First	Highest value job is processed first
LPF	Lowest Punishment First	Lowest punishment job is processed first
RR	Rule by Raghu and Rajendran	Specific rule

Table 2-3 Well-Known Dispatching Rules in Wafer Fabs

Simulation-based approach

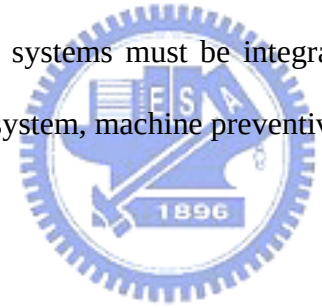
Some simulation methodologies are developed for wafer Fab Lot scheduling. This approach has the advantages of high fidelity and flexibility, but often comes at an expense of computational requirements and data maintenance. In order to simulate a complex wafer Fab environment, a large amount data of current wafer Fab current state must be well-prepared by production controller for the simulation model. Besides, the execution complexity of the model is very high for simulation process. As mentioned above, since wafer Fab is a dynamic and uncertain environment, it is very unlikely for production controllers to spend so much time and effort. They would prefer to use heuristic rules and time-saving methodologies.

Some algorithms and hybrid rules are used with this kind of simulation model. For example, using the Genetic algorithm (GA) characteristics of reproduction, mutation and crossover gets the fitness function as a static optimal formula. This formula helps to identify Lot processing order.

Multiple dispatching criteria are combined into a single rule which used a linear combination with relative weights [4]. The weights identify the contribution of the different criteria. The assignments of weights to the different criteria are optimized using a mixture design of experiments (DOE) and multiple response optimizations.

Machine-Learning Approach

A machine-learning engine is designed to extract Lot dispatching policies from manufacturing execution system (MES) [1]. However, the scheduling attributes of MES are finite and the policies must be reviewed by human expert. In this approach, more relevant manufacturing systems must be integrated, like supply-chain system, enterprise resource planning system, machine preventive maintenance system, etc.



Agent-based Approach

Agent-based approach decomposes wafer Fab Lot scheduling job into several intelligent agents and solve the problems in a distributed way. [15] proposed an Adaptive Negotiation Framework which models the dynamic nature of agent based manufacturing scheduling at negotiation level explicitly. Autonomous agents coordinate with each other by utilizing negotiation mechanisms.

2.3 Motivation

Every domain has its core technology or know-how to represent the value or

competitiveness. Our major purpose is to extract and utilize human expertise adaptively. Thus, we propose a suite of Lot scheduling knowledge-based system (referred to as KBS hereafter) to describe, acquire, reposit, extend and replicate the expertise of Lot scheduling thinking procedures (referred to as Scheduling Logic hereafter).

Many academic researches focus on manufacturing scheduling but lack a complete KBS. The most difficulty is to extract the Lot scheduling knowledge from the human expert (knowledge acquisition referred to as KA hereafter) in this domain. In order to acquire the Lot scheduling knowledge, a formal knowledge representation (referred to as KR hereafter) is essential and the relationships of knowledge components must be identified. Therefore, we try to come out a complete Lot scheduling KBS to store and re-use knowledge and implement a prototype for Lot scheduling.

For the purpose of implementing a KBS, we will propose a KR to represent the Lot scheduling logic. Besides, the KR should have following capabilities:

- Visualized: For knowledge acquisition, we would like to propose a visualized KA tool to elicit the knowledge by a user-friendly interface.
- Machine-readable: Due to the data exchange requirement between KA tool and knowledge-base, this representation must have machine-readable capability.
- Graph-describable: In order to show the relative graphic components in the interface, this representation must include graphic information.

Therefore, an XML-based graphic Lot scheduling logic-oriented KR was adopted.

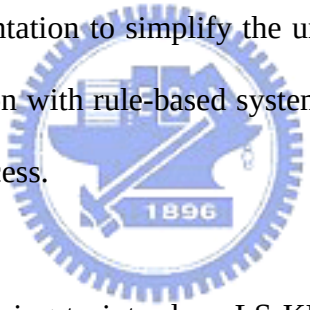
Basically, KA is the core stage in a KBS. We discard the traditional interview procedures to do KA. More advanced approach is taken. As mentioned above, a graphic KA tool will be designed in this thesis, which provides a graphic user-friendly interface to carry out knowledge elicitation.

Including a specific KR and KA mechanism, a logic-oriented Lot scheduling knowledge-based system architecture will be discussed.

Through the visualized KA tool, Lot scheduling knowledge could be saved, modified and represented easily. It is helpful to transfer and explain this kind of knowledge to new production controller as well as a Lot scheduling tutoring system.

Chapter 3 Architecture of Logic-Oriented Wafer Fab Lot Scheduling Knowledge-Based System

In order to solve complex Lot scheduling problem, we propose a **L**ot **S**cheduling **K**nowledge-**B**ased **S**ystem (referred as LS-KBS hereafter) approach. In traditional approaches, it is difficult to utilize human expertise to solve Lot scheduling problem. Besides, the specific knowledge is also hard to reserve and re-use. For these reasons, our approach helps to elicit human expertise appropriately. In addition, we adopt visualized knowledge representation to simplify the understanding of Lot scheduling process. Finally, the integration with rule-based system and inference engine is made to achieve Lot scheduling process.



In this chapter, we are going to introduce LS-KBS. The system architecture of LS-KBS as shown in Figure 3-1 compromises 3 key phases which include Meta-Knowledge Acquisition Phase, Knowledge Acquisition Phase and a Lot Scheduling Phase.

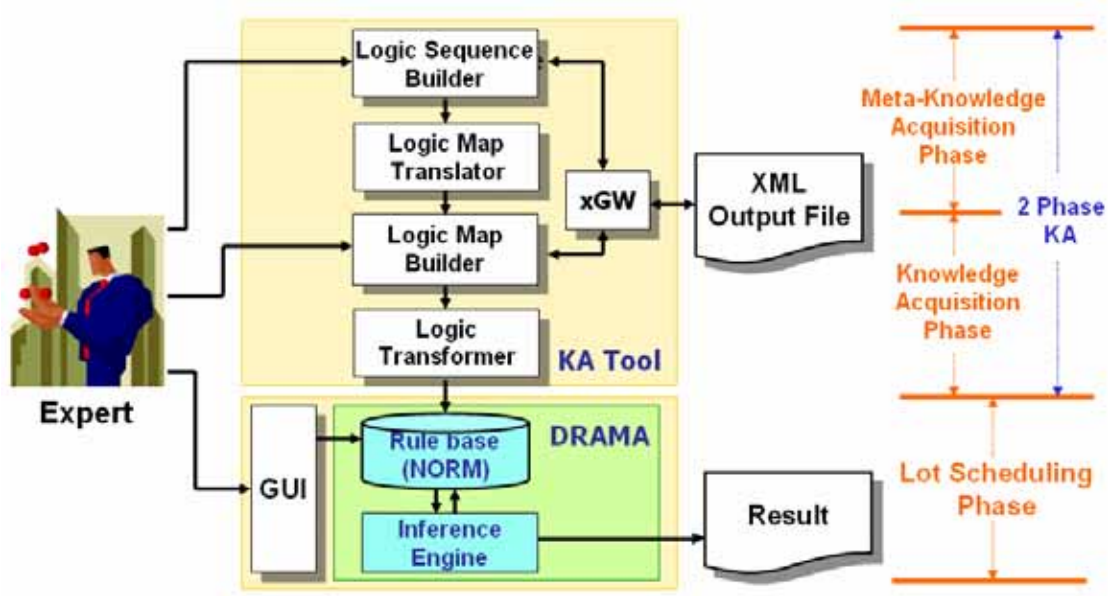


Figure 3-1 System Architecture of LS-KBS

3.1 Meta-Knowledge Acquisition Phase

There is a lot of Lot scheduling knowledge in LS-KBS and partial knowledge could be applied to similar situations. It means the same logic of attributes can be re-used again and again. For example, in the same due-date oriented strategy, the Lot scheduling logics are the same in ion implanter and lithograph coater. As long as the Lot scheduling logic of ion implanter was constructed in LS-KBS, the same Lot scheduling logic of lithograph coater also can be constructed by referring to the same logic of attributes.

Based on this reason, we design a meta-knowledge acquisition phase to acquire the ordering of attributes from the production controller. This process helps to generate Lot scheduling logic automatically by referring to existing attributes and is able to simplify the knowledge acquisition operation. Therefore, we design a user interface (referred as Logic Sequence Builder hereafter) for the production controller

to assign the importance ordering for Lot scheduling attributes. Actually production controller can select the target attributes and the sequence of importance. More details will be described in Section 4.3.

In order to translate meta-knowledge to knowledge, meta-knowledge translator (referred as Logic Map Translator hereafter) is brought up. Logic Map Translator translates the meta-knowledge into a Lot scheduling logic graph (referred as Logic Map hereafter). Depending on the requirement of production controller, she/he can adjust Logic Map again once she/he needs.

In addition, we adopt XML-based knowledge representation to reposit the knowledge and meta-knowledge easily. An XML parsing and interpreting process is designed as an XML gateway (referred as xGW hereafter). xGW achieves to interpret knowledge and meta-knowledge into XML repository file. Oppositely, xGW also helps to parse XML file into knowledge and meta-knowledge.

3.2 Knowledge Acquisition Phase

Knowledge Acquisition (KA) Phase is the most important process in constructing knowledge-based system. Instead of interviewing production controller, our idea is to elicit Lot scheduling knowledge through a visual KA tool and the Lot scheduling logic graph (Logic Map) will be generated by production controller. Before KA process, how to represent Lot scheduling knowledge is a key problem. The knowledge representation will be introduced in Section 4.2.

Logic Map can express the Lot scheduling thinking procedures more clearly. The detailed expression and operation of Logic Map will be described in Section 4.3. Therefore, we design a graphic knowledge acquisition tool, named Logic Map Builder, to generate Logic Map. The characteristics of Logic Map are easy to maintain and understand by human expert. This is also our major goal in knowledge acquisition.

3.3 Lot Scheduling Inference Phase

According to the Lot scheduling thinking procedures, it looks like a series logics and matches the knowledge representation of rule-base. Thus, we adopt rule-base (NORM-base model) as our knowledge-base and make use of the corresponding inference shell, DRAMA [14], as our inference engine.

Lot Scheduling Phase is designed for inference by DRAMA to receive relevant attributes/facts from production controller and generate Lot scheduling result. The process of rule transformation will be discussed in Section 4.3.

Chapter 4 Knowledge Representation and Knowledge Acquisition Tool of Wafer Fab Lot Scheduling

As we know, knowledge acquisition (KA) is the most difficult process in constructing knowledge-based system [2] especially in semiconductor wafer Fab because of many complicated factors, like various process flows, dynamic manufacturing environment and variant market requirement. It is hard to collect relative knowledge through manual interview. In addition, the Lot scheduling human expert, called Production Controller, owns her/his particular Lot scheduling thinking procedures adaptively for various situations. For these reasons, our idea is to acquire knowledge from production controller via a user-friendly visualized KA tool.

For the purpose of constructing a specific visual KA tool for semiconductor wafer Fab Lot scheduling. The essential requirement is a design of knowledge representation which represents the Lot scheduling knowledge. On the other hand, the knowledge should be shareable and reusable. Therefore, we adopt Extensible Markup Language (XML) data description which is a simple and flexible text format description for data exchange.

This chapter introduces the knowledge representation and knowledge acquisition mechanism of our Lot scheduling knowledge-based system. First of all, the key logic

components should be classified. The XML and DTD (a file that describes the structure of XML and defines the tag of XML) are reviewed and XML-based representations are provided at the same time. For the purpose of knowledge acquisition, the systematical knowledge acquisition mechanism is designed in this chapter.

4.1 Lot Scheduling Logic Components

For the expected features of describing, acquiring, repositing, extending and replicating the knowledge of Lot scheduling, after discussing with the production controllers who work in real wafer Fab, we found the expertise, a series of thinking procedures as shown in Figure 4-1, could be decomposed into a combination of logics as shown in Figure 4-2. In other words, the Lot scheduling logics are componentized.

The benefits of componentized logics are including:

1) We are able to represent the Lot scheduling knowledge as a graph. This kind of expression is easier to understand. Besides, componentized logics also contribute to process knowledge acquisition.

2) Traditionally the Lot scheduling procedures are described in sequence and programmed by hard code in application. The programming effort can be reduced by components reusing and componentized logics are more flexible once the logics are modified.

3) Componentized logics are corresponding to our rule-base design. Especially we are adopting knowledge-based approach.

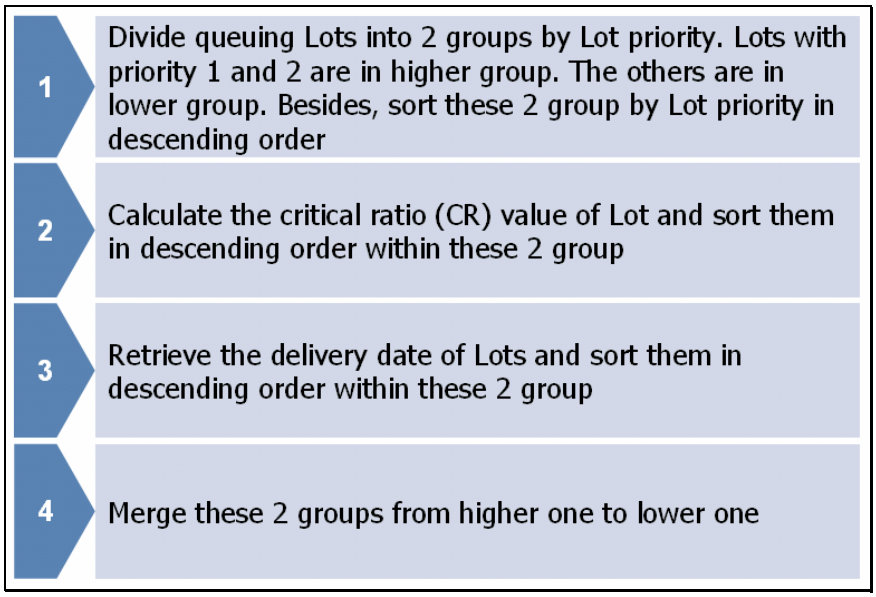


Figure 4-1 Example of Human Expert Thinking Procedure

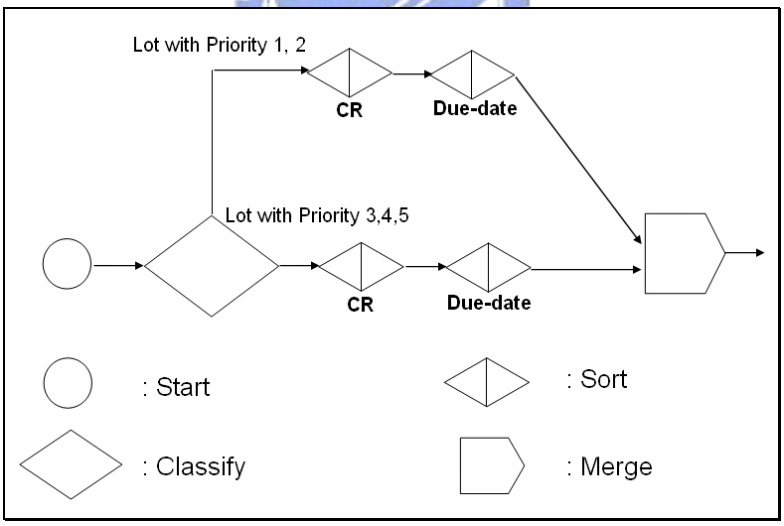


Figure 4-2 Graphic Expression of Lot Scheduling

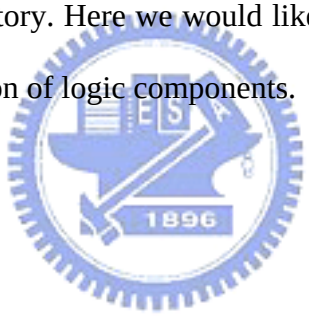
Here we classify the logic components as following:

- Start : express the starting node of Lot scheduling
- IF-ELSE : express conditional control and generate 2 conditional results

- Sort : generate sorting result
- Next : express the processing sequence
- Merge : merge the multiple inputs into a single result
- Logic module : express a combination of logic components. It is a special design for flexibility.

4.2 XML-Based Representation

In the thesis, we use the advantages of simple, flexible and machine-readable of Extensible Markup Language (XML) [16] for knowledge representation, knowledge sharing and knowledge repository. Here we would like to have an overview on XML and introduce the representation of logic components.



Preliminary

The XML (eXtensible Markup Language), a meta markup language, is suitable to describe the documents and to define the structure of the documents by its DTD (Document Type Definition). It has the property of reuse, especially in structure, and there are many examples of document reuse [6]. XML is intended as a machine-readable rather than human-readable language; therefore, it is mainly generated and read by machines not the people [8].

In order to represent a logic-oriented knowledge graph of Lot scheduling, we define a series of logic components which are based upon XML, named xLogic. [3]

XLogic

The XML-based representation of logic components (referred as XLogic hereafter) are shown as follows:

	DTD	<!ELEMENT basic_comp (#PCDATA)> <!ATTLIST basic_comp shape CDATA #REQUIRED>
	XML	<basic_comp shape=”begin_node”>Start</basic_comp>

Table 4-1 Format of START Component

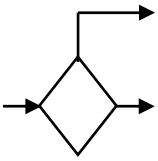
	DTD	<!ELEMENT if_else_comp (#PCDATA)> <!ATTLIST if_else_comp shape CDATA #REQUIRED>
	XML	<if_else_comp> <decision_symbol exit_no=”2”> A=1?</decision_symbol> <BLOCK0>…….. </BLOCK0> </ if_else_comp >

Table 4-2 Format of IF-ELSE Component

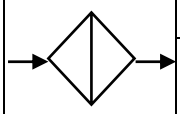
	DTD	<!ELEMENT sort_comp (#PCDATA)> <!ATTLIST sort_comp shape CDATA #REQUIRED>
	XML	<sort_comp shape=”sort_node”>Due Date</sort_comp>

Table 4-3 Format of SORT Component

	DTD	<!ELEMENT next_comp (#PCDATA)> <!ATTLIST next_comp shape CDATA #REQUIRED>
	XML	<next_comp shape=”next”>Next</next_comp>

Table 4-4 Format of NEXT Component

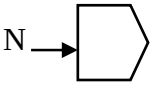
	DTD	<!ELEMENT end_comp (#PCDATA)> <!ATTLIST end_comp shape CDATA #REQUIRED>
	XML	<end_comp shape=”end_node”>End merge</end_comp>

Table 4-5 Format of START Component

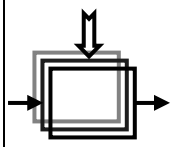
	DTD	<!ELEMENT logic_mod (#PCDATA)> <!ATTLIST logic_mod shape CDATA #REQUIRED>
	XML	<logic_mod shape=”logic_mod”>Logic module</logic_mod>

Table 4-6 Format of LOGIC MODULE Component

4.3 Design of Knowledge Acquisition Tool

In this thesis, we design a two-phase KA process to acquire meta-knowledge and

knowledge of human expert for Lot scheduling logic construction. In first phase, the main task is to elicit the guiding knowledge of Lot scheduling knowledge. In second phase, we design a user-friendly KA tool to construct Lot scheduling logic by graph. The system architecture is described in Chapter 3 detailedly. The relative KA tools and mechanisms will be introduced in this section.

Meta-Logic Builder

Meta-knowledge, a kind of knowledge about knowledge, is a control strategy that tells how rules can be applied for knowledge verification and validation [5]. The rule model type of meta-knowledge determines if the new rule is in the appropriate form to be entered in the knowledge base. In a rule-based expert system, determining if the new rule is in the correct form is called verification of the rule. Determining that a chain of correct inferences leads to the correct answer is called validation. Basically, verification has to do with internal correctness while validation has to do with external correctness.

In this thesis, we design a user interface for the production controller to assign the importance ordering for Lot scheduling attribute. The goal is to help the human expert to construct Lot scheduling logic easier. The user interface is shown in Figure 4-3. Production controller can select the target attribute and importance sequence. By the assignments, we provide a Logic Translation mechanism to translate the meta-knowledge into a graphical Lot scheduling thinking procedure, is called Logic Map.

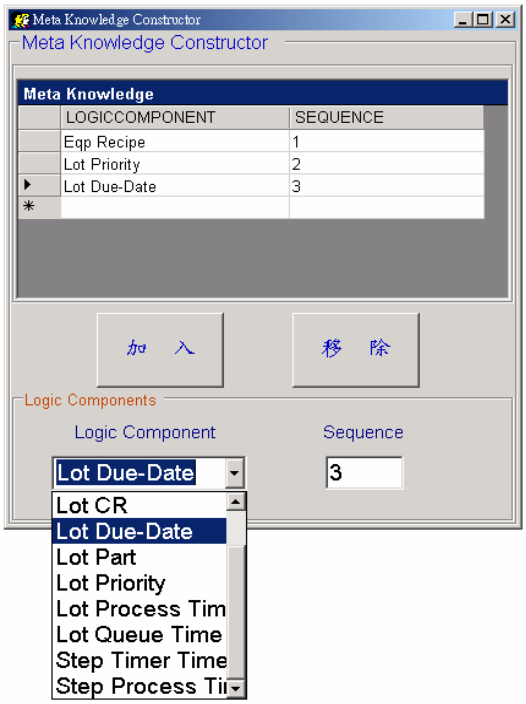


Figure 4-3 Logic Sequence Builder

Logic Map Translator

Besides, we design a logic translation mechanism to transform meta-knowledge to Lot scheduling Logic in XML format as shown in Figure 4-4.

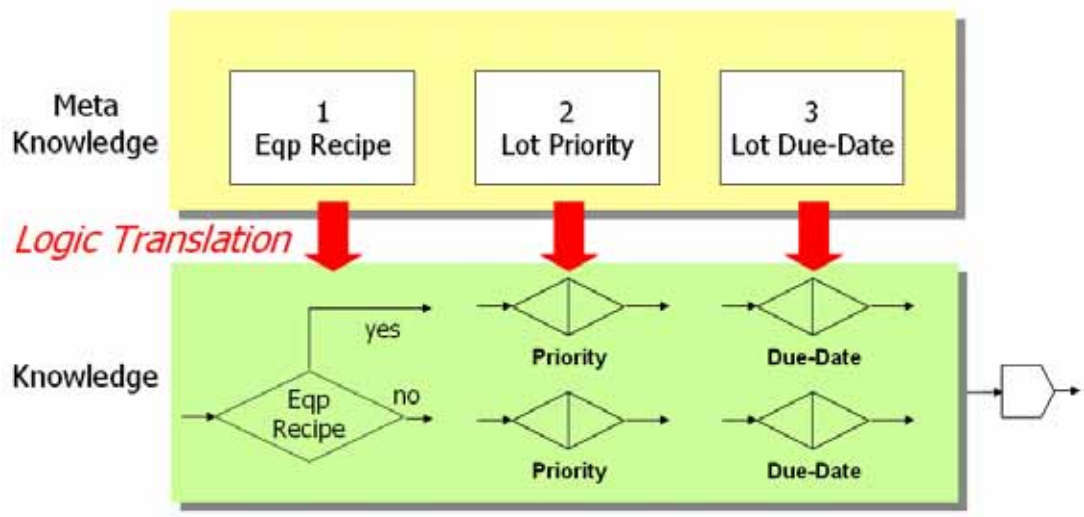


Figure 4-4 Meta-Knowledge Translation

Therefore, we propose a process of Logic Map Translation as shown in Figure 4-5.

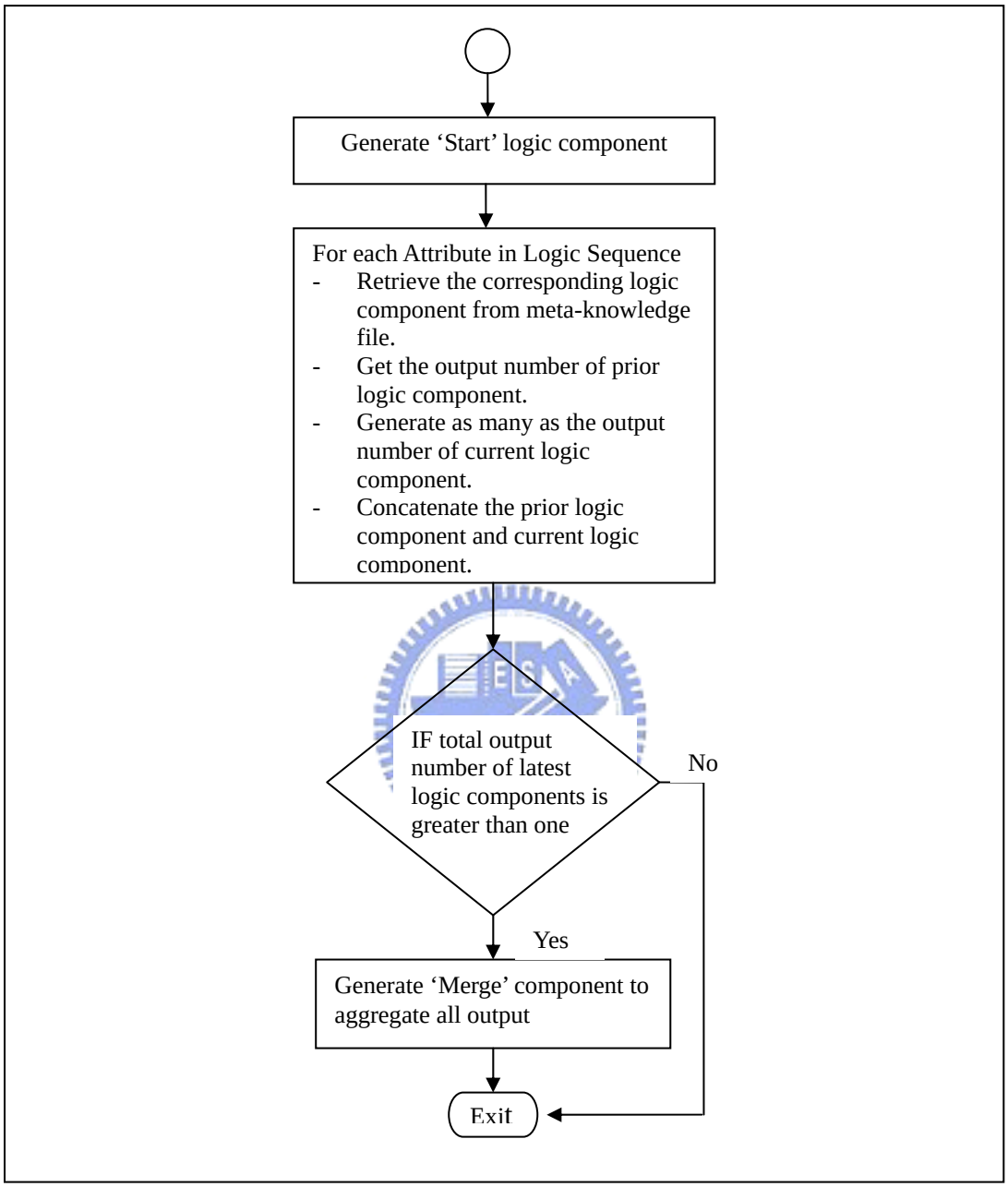


Figure 4-5 Process of Logic Map Translation

Logic Map Builder

A graphic knowledge acquisition tool, named Logic Map Builder as shown in Figure 4-6, is designed to elicit the Lot scheduling logic construction, named Logic

Map. Logic Map is easy to maintain and understand by expert.

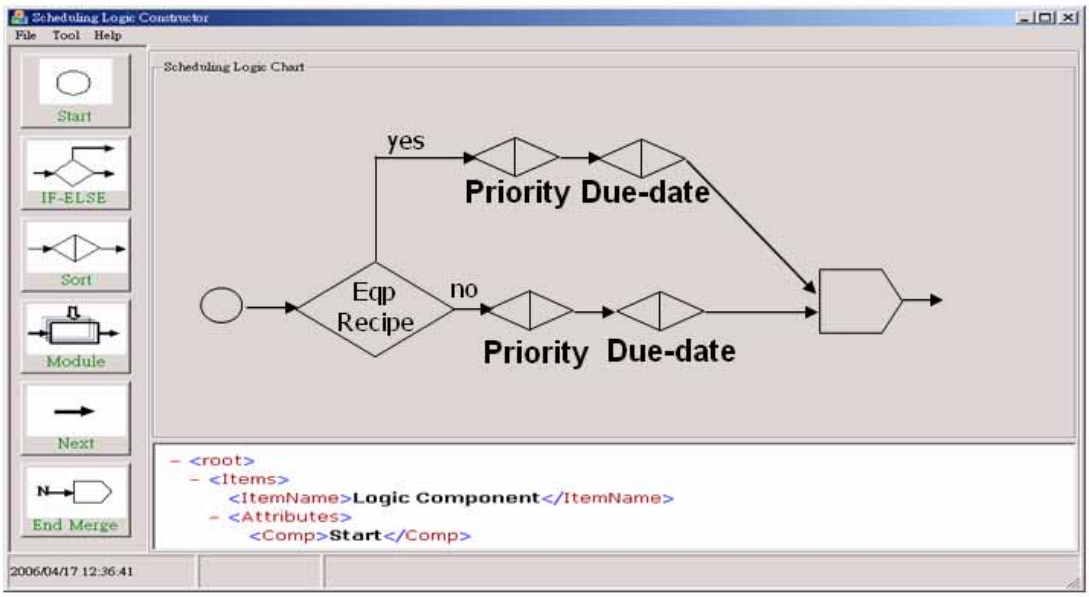


Figure 4-6 Logic Map Builder

Logic Transformer

In this thesis, for the purpose of flexible inference and knowledge maintenance, we adopt the rule-based mechanism for logic selection as shown in Figure 4-7. Therefore, we have to translate Logic Map into NORM-base rule base.

NORM is designed by object-oriented concept. Thus, two level rule classes are designed in this thesis. The top rule class, named logic component rule class, is responsible for logic selection. The bottom rule class, named logic attribute rule class, is a set of attribute classes for the acquirement of logic component rule classes.

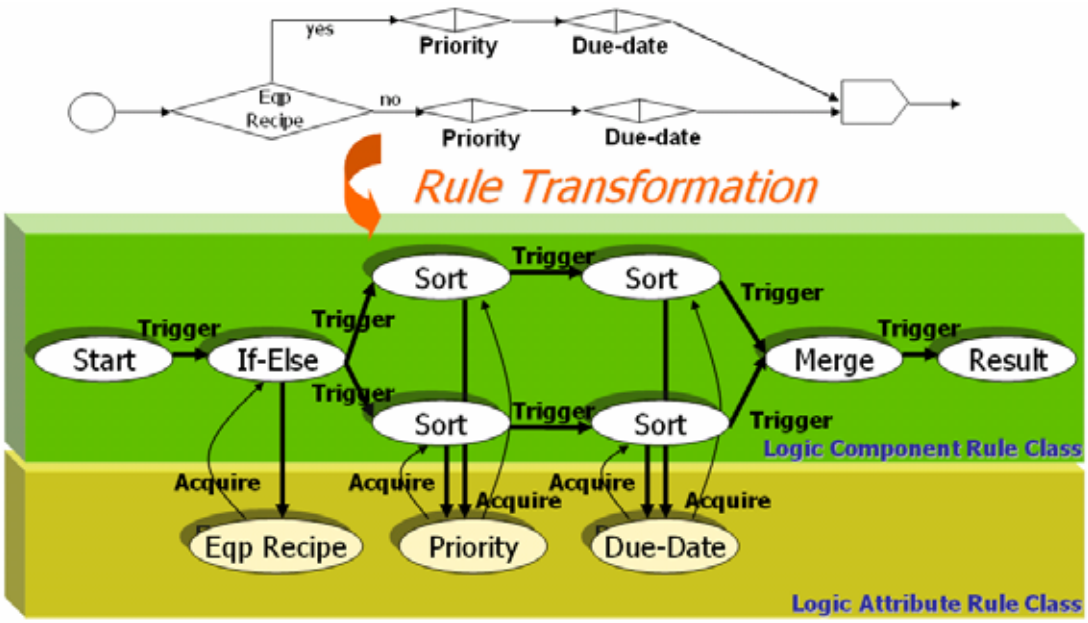


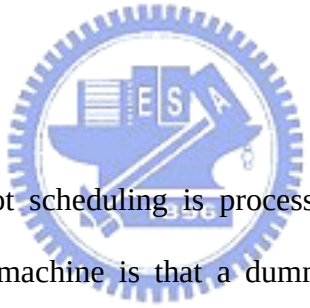
Figure 4-7 Logic Map – Rule Class Transformation

Chapter 5 Cases Analysis

In order to demonstrate the contribution of LS-KBS, two cases are described for problem solving in this chapter. This analysis helps to realize the manipulation of LS-KBS and shows the power of our approach.

5.1 Heuristics Combination

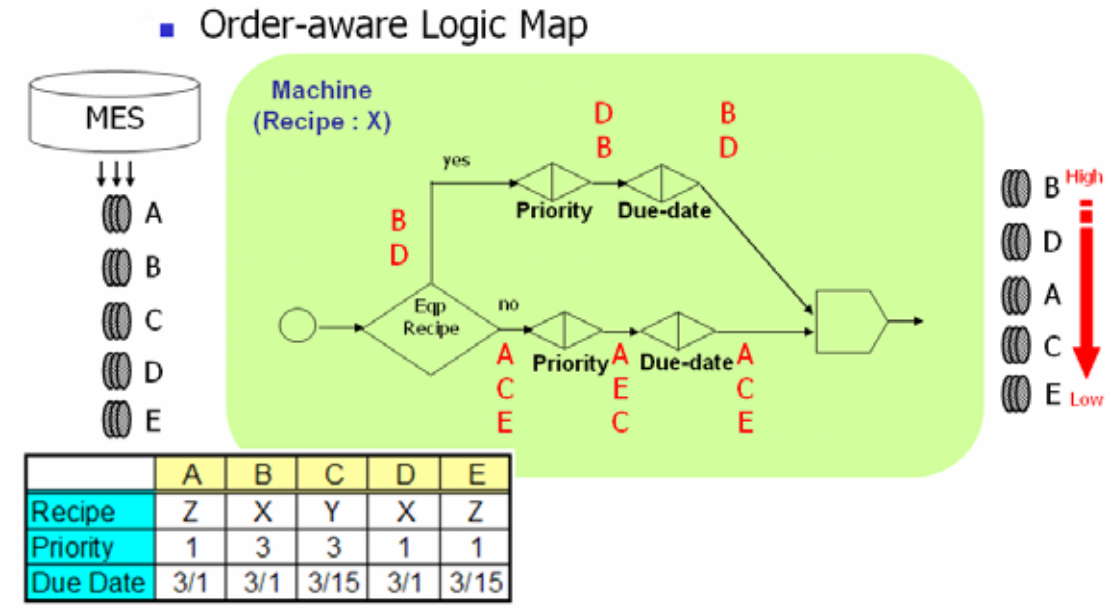
For different purposes, production controller comes out different strategies for gaining higher profit.



The first example of Lot scheduling is processed in ion implant machine, a special characteristic of this machine is that a dummy testing run is needed once recipe changes. It results in the resources of materials and manpower are wasted and the machines utilization is decreased if the recipe changed unreasonably. Thus, production controller must make a lot of effort to keep monitoring the recipe change and to prevent any meaningless dummy run.

In most situations, production controller takes care of the on-time delivery of Lots in wafer Fab production. Besides, they must satisfy the trial process requirement from the engineering department via Lot priority assignment. Therefore, in their thinking procedures, they consider the recipe of queuing Lots to realize whether the recipe of Lots is corresponding to current recipe of machine firstly. This process classifies the queuing Lots into two groups. Secondly, they sort the two groups

individually by the due date and priority of Lots. Two Lot ordering sequences are obtained. As shown in Figure 5-1 the queuing Lots are A, B, C, D and E. After the processing, the order of Lot scheduling becomes B, D, A, C and E.



	A	B	C	D	E
Recipe	Z	X	Y	X	Z
Priority	1	3	3	1	1
Due Date	3/1	3/1	3/15	3/1	3/15

Figure 5-1 Order-Aware Logic Map

In some special situations, for instance of cost down policy, recipe change makes too much resource wasting. Production takes the recipe change as the most important issue. Then, Cost-oriented Logic Map is maintained as shown in Figure 5-2.

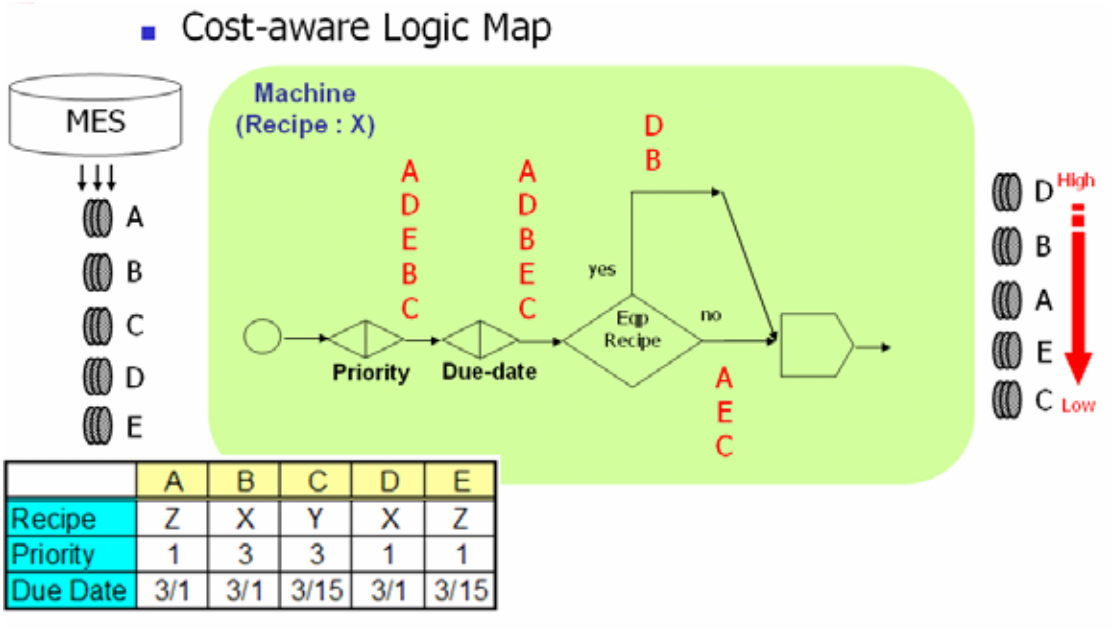


Figure 5-2 Cost-Aware Logic Map

The same queuing Lots are processed in this kind of cost-saving way. The order of Lot scheduling results in D, B, A, E and C. Different result comes from different Lot scheduling logics as well as Logic Map. Logic Map is flexible and powerful for production controller to adjust their strategy.

5.2 Process Causal Restriction

For the Quality of Photo-Resister, metal oxidation issue before diffusion and wafer cleanliness issue, there is a special process causal restriction. A validation time exists between two causal steps, called Queue-time. If a Lot runs out of the Queue-time, the Lot must be re-processed by a number of process steps. It's a big punishment once the issue occurred. Therefore, production controller must take care of this restriction.

For the purpose of controlling process flow, manufacturing execution system (MES) start a timer once a Lot leaves the prior step. The timer counts down and the residue time can be queried from MES.

For Lot scheduling, production controller must extra consider the residue timer time as shown in Figure 5-3. Basically most of Logic Maps are similar. In this case, the extra residue time attribute has to be considered. Within our design, the Module Logic component is able to replace the similar Logic Map. This way erases the effort of Logic Map maintenance and assures the capability of solving complicated process problem.

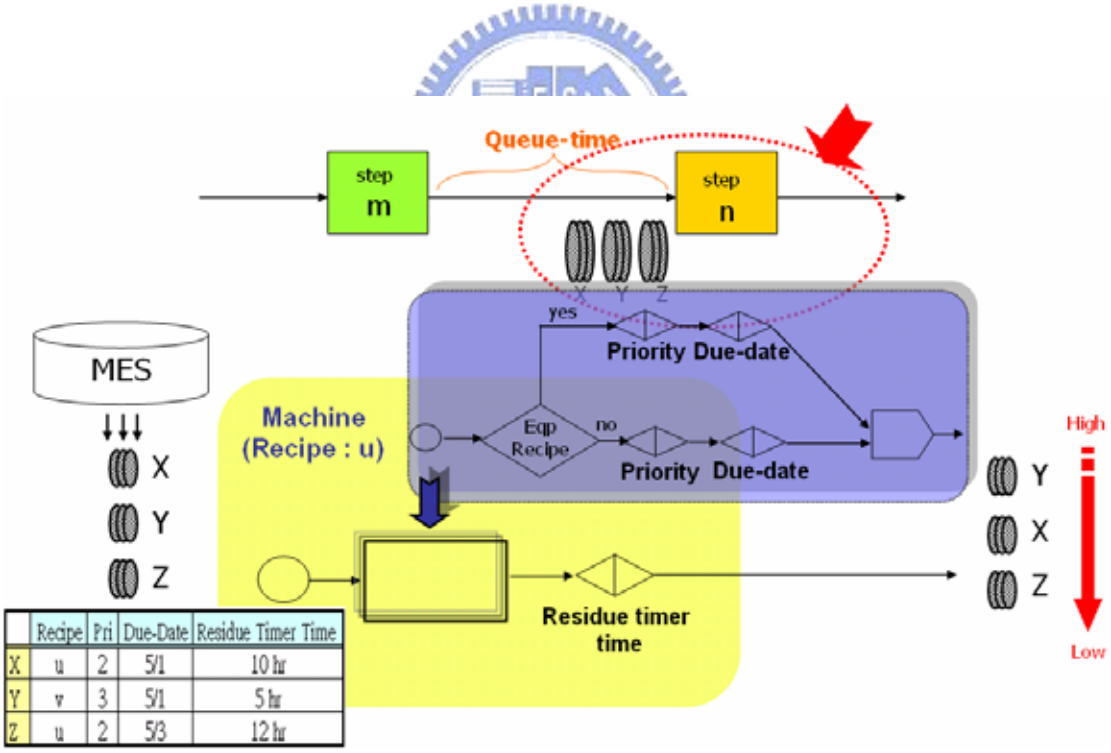


Figure 5-3 Causal Restrictions Logic Map

Chapter 6 Experiment

The experiment was done in a real wafer Fab. We designed a parallel test with two production controllers and LS-KBS. Our goal is to evaluate the comparison results between LS-KBS and human experts on precision and accuracy. We want to show that LS-KBS could schedule Lots like human experts and to know in case of missing consideration.

6.1 Experiment Design

Experiment Procedure

The experiment was designed to proceed for 10 days, i.e. 10 different situations, on the same machine. Two human experts, production controllers, joined this experiment and scheduled the Lots as well as their daily operation. One is senior production controller and the other is a junior one. Besides, the senior production controller maintained the Logic Map in LS-KBS and faced the same raw data, as shown in Appendix A.

The testing machine is a metal sputter, which is known as physical vapor deposition and widely used for depositing thin metal layers on semiconductor wafers. The characteristics are: 1) It needs a dummy testing run if recipe changes. The resources of materials and manpower are wasted and the machines utilization is decreased once recipe change again and again. 2) Relative recipe change is no need to

have any extra dummy testing run. It means human expert had better to arrange the Lots of relative recipe into a continuous sequence.

The Logic Map is generated by senior production controller as shown in Figure 6-1.

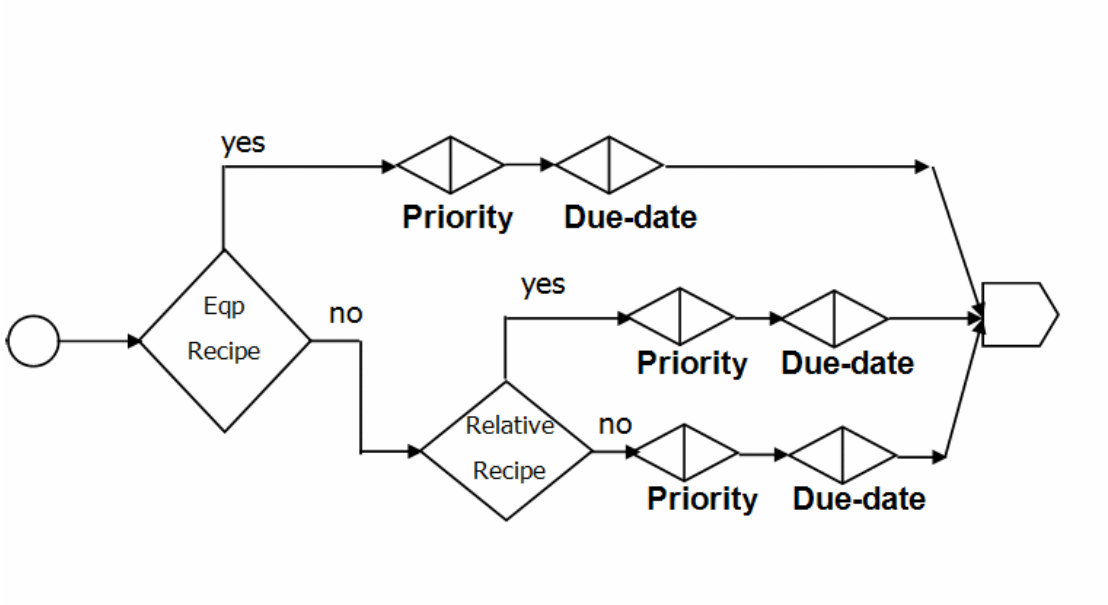


Figure 6-1 Logic Map of Experiment

The throughput of this machine is around 5 Lots. We just consider the sequence of top 5 Lot sequence for evaluation.

Experiment Indices

We define two evaluation indices to verify LS-KBS.

- Precision Testing Index (PTI) : compared top 5 Lots shooting rate between human experts and LS-KBS over 10 situations.

  (1) 100 : Top 5 Lots of LS-KBS all are included in top 5 of human experts;

  (2) 80 : Only 4 of top 5 are included in top 5 of human experts;

(3) 60 : Only 3 of top 5 are included in top 5 of human experts;

(4) 40 : Only 2 of top 5 are included in top 5 of human experts;

(5) 20 : Only 1 of top 5 is included in top 5 of human experts;

(6) 0 : No one is included in top 5 of human experts.

- Accuracy Testing Index (ATI) : compared top 5 Lots process sequence similarity rate between human experts and LS-KBS over 10 situations. We define a distance-weighting function for score calculation. The principle is the higher Lot it matches and a higher score it gets.

ATI Score Function: $\sqrt{\sum_{i=1}^{5} W_i (M_i)^2}$

where i means i - th order Lot

M_i means whether matching at i - th Lot

if match, $M_i = 1$; if not match, $M_i = 0$

W_i means the weight value of i - th order Lot

$W_1 = 45, W_2 = 25, W_3 = 15, W_4 = 10, W_5 = 5$

6.2 Experiment Results

After parallel testing, the comparison score result comes out. The detailed Lot scheduling results are listed in Appendix B. The resulting table is shown in Table 6-1.

Day	PTI		ATI	
	Expert 1	Expert 2	Expert 1	Expert 2
1	100	100	100	100
2	100	100	100	100
3	100	100	100	100
4	80	100	75	100

5	100	100	100	100
6	80	80	85	85
7	100	100	100	100
8	100	100	100	100
9	100	100	100	100
10	100	100	100	100
Sub-mean	96	98	96	98.5
Mean		97		97.25

Table 6-1 Scoring Table of Experiment Result

6.3 Verification and Feedback from Human Experts

According to the result scores, most of the situations are totally matched and only fewer cases are not corresponded. We discussed these cases with our production controllers.

In Day 4 as shown in Figure 6-2, the senior production controller arranged the special Lot on 2nd place, but LS-KBS puts that Lot on 7th place. The senior production controller explained that the Lot used a special recipe and was an only processing Lot of the product in the Fab. If she/he put the Lot after recipe S_ALCU2S, the Lot must be waiting until 5 Lots were processed. However, it had a higher priority 2.

LS-KBS

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
APR0002.AF	1P6C158.1	EP	24	3	1TCU0000	MTM1DP01.0	2006/4/15	eS_Cu06
APR0002.AF	1N6A264.3	EC	1	2	1TAU0000	MSSD3DP0.01	2006/5/12	eS_Au08
AP92501.AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/4/20	EALCU11K
AP92501.AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/4/20	EALCU11K
AP92501.AF	1N5K066.1	PC	24	3	1TALCU01	M215DP00.01	2006/4/30	EALCU11K
AP92501.AF	1N5K140.1	PC	23	3	1TALCU01	M215DP00.01	2006/4/30	EALCU11K
AP91201.AI	1N6A048.1	PC	22	4	1TALCU01	M109DP00.01	2006/4/30	EALCU5K

Expert 1

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
APR0002.AF	1P6C158.1	EP	24	3	1TCU0000	MTM1DP01.0	2006/4/15	eS_Cu06
APR0002.AF	1N6A264.3	EC	1	2	1TAU0000	MSSD3DP0.01	2006/5/12	eS_Au08
AP91201.AI	1N6A048.1	PC	22	4	1TALCU01	M109DP00.01	2006/4/30	EALCU5K
AP92501.AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/4/20	EALCU11K
AP92501.AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/4/20	EALCU11K

Expert 2

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
APR0002.AF	1P6C158.1	EP	24	3	1TCU0000	MTM1DP01.0	2006/4/15	eS_Cu06
APR0002.AF	1N6A264.3	EC	1	2	1TAU0000	MSSD3DP0.01	2006/5/12	eS_Au08
AP91201.AI	1N6A048.1	PC	22	4	1TALCU01	M109DP00.01	2006/4/30	EALCU5K
AP92501.AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/4/20	EALCU11K
AP92501.AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/4/20	EALCU11K

Figure 6-2 Comparison of Day 4 Results

In Day 6, both senior and junior production controllers arranged a Lot on 3rd place, but LS-KBS puts the Lot on 7th place. Because the production controllers received a special request from the engineering Dept. in the morning meeting, they promoted the Lot to 2nd place.

LS-KBS

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
APR0002.AF	1P6C158.1	EP	24	3	1TCU0000	MTM1DP01.0	2006/4/15	eS_Cu06
APR0002.AF	1N6A264.3	EC	1	2	1TAU0000	MSSD3DP0.01	2006/5/12	eS_Au08
AP92501.AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/4/20	EALCU11K
AP92501.AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/4/20	EALCU11K
AP92501.AF	1N5K066.1	PC	24	3	1TALCU01	M215DP00.01	2006/4/30	EALCU11K
AP92501.AF	1N5K140.1	PC	23	3	1TALCU01	M215DP00.01	2006/4/30	EALCU11K
AP91201.AI	1N6A048.1	PC	22	4	1TALCU01	M109DP00.01	2006/4/30	EALCU5K

Expert 1

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
APR0002.AF	1P6C158.1	EP	24	3	1TCU0000	MTM1DP01.0	2006/4/15	eS_Cu06
APR0002.AF	1N6A264.3	EC	1	2	1TAU0000	MSSD3DP0.01	2006/5/12	eS_Au08
AP91201.AI	1N6A048.1	PC	22	4	1TALCU01	M109DP00.01	2006/4/30	EALCU5K
AP92501.AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/4/20	EALCU11K
AP92501.AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/4/20	EALCU11K

Expert 2

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
APR0002.AF	1P6C158.1	EP	24	3	1TCU0000	MTM1DP01.0	2006/4/15	eS_Cu06
APR0002.AF	1N6A264.3	EC	1	2	1TAU0000	MSSD3DP0.01	2006/5/12	eS_Au08
AP91201.AI	1N6A048.1	PC	22	4	1TALCU01	M109DP00.01	2006/4/30	EALCU5K
AP92501.AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/4/20	EALCU11K
AP92501.AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/4/20	EALCU11K

Figure 6-3 Comparison of Day 6 Results

In the first case, we suggest the more Logic Components should be appended into the Logic Map to synchronize the Lot scheduling logic. Even the junior production planer didn't know the tricky point.

In the second case, an unexpected event occurred. If the Lot had been maintained the correct priority, we believed the result would be matched.

From the feedback of human experts, it assures the system not only has the capability to reposit and re-use Lot scheduling knowledge, but also can be a Lot scheduling tutoring system for new production controller.

Chapter 7 Conclusion

For the purposes of eliciting the hidden knowledge, repositing the expertise and scheduling production Lots, we proposed a suite of Lot scheduling knowledge-based system.

In this thesis, we defined a logic-oriented knowledge representation, based upon XML, named XLogic. This achieves the usage of knowledge repository, knowledge re-use and graphic expression.

In order to acquire the knowledge of Lot scheduling easier, we designed a two-phase KA tool including meta-knowledge and knowledge acquisition. The tool provides a user-friendly and graphic interface for knowledge construction. In meta-knowledge acquisition phase, the importance and sequence of the Lot scheduling attributes are collected to verify and construct Lot scheduling logic by Meta-Logic Builder. Besides, we designed a logic translation mechanism to transform meta-knowledge to Lot scheduling Logic in XML format. In knowledge acquisition phase, we designed a graphic knowledge acquisition tool, named Logic Map Builder, to elicit the Lot scheduling logic construction, named Logic Map. Logic Map is easy to maintain and understand by expert. This is also our major goal in knowledge acquisition. Through the rule translation mechanism, we translate Logic Map into rule base. Finally, after inputting relevant facts, the Lot scheduling is done by inference via DRAMA .

The comparison of precision and accuracy between the results of our system and human experts was processed for evaluation. The results of most cases were totally matched. From the analyzed cases, we realized that a complete Logic Map can help to generate a correct Lot scheduling result which matches the logics of senior production controller. In addition, the junior production controller can benefit greatly from the Logic Map for extra Lot scheduling knowledge she/he never know.

From the feedback of human experts, it proved that the system not only has the capability to reposit and re-use Lot scheduling knowledge, but also can be a Lot scheduling tutoring system.

In the future, after accumulating more and more Logic Maps as well as enriching Lot scheduling knowledge with relative production situations, we plan to design a diagnostic mechanism of Lot scheduling knowledge construction. We hope the mechanism can help to validate and verify the Logic Map once new production controller need to construct a new Logic Map.

In addition, we hope to decrease the loading of relevant facts input by production controller in Lot scheduling inference phase. We will integrate LS-KBS with Manufacturing Execution System for automatic data exchange requirement.

Reference

[1] Yi-Ju Chang: A Learning Agent for Supervisors of Semiconductor Tool Dispatching, Master Thesis, Nation Taiwan University, Taiwan.(2001)

[2] Chang-Sheng Chen: Design and Implementation of a Unifying Intelligent DNS Management System, Doctor Dissertation, National Chiao-Tung University, Taiwan. (2003)

[3] Jin-Huei Chen : A New XML-based Knowledge Representation for Flowchart. Master Thesis, National Chiao-Tung University, Taiwan. (2000)

[4] R.M. Dabbas, J.W. Fowler: A New Scheduling Approach Using Combined Dispatching Criteria in Wafer Fabs, IEEE Transactions on Semiconductor Manufacturing (2003)

[5] J. C. Giarratano, G. D. Riley: Expert Systems principles and programming. 4th Edition. Page(s): 182-183

[6] E. Guerrieri: Software Document Reuse with XML, Fifth International Conference on Software Reuse, Proceedings(1998)pp. 246 –254

[7] M. Ham, F. Dillard: Dynamic photo stepper dispatching/scheduling in wafer fabrication. Semiconductor Manufacturing, 2005. ISSM 2005, IEEE International Symposium on 13-15 Sept. (2005)

[8] P. Martin and P. Eklund: “Embedding knowledge in Web documents”, Computer Networks 31 (1999) pp.1403-1409

[9] Jan-Ren May: The Design of Dispatching Rules for the Primary Machines of Wafer Fabrication Factories, Master Thesis, National Chiao-Tung University, Taiwan (1996)

[10] Garey, Michael. R., Johnson, D. S., Computers and Intractability: A Guide to the Theory of NP-Completeness. Freeman, New York. (1979)

[11] MIT's OpenCourseWare: Semiconductor Manufacturing – Chapter19 scheduling (2003)

[12] D. Rajpathak, et al.:A Generic Library of Problem Solving Methods for Scheduling Applications, K-CAP’03, October 23–25, 2003, Sanibel Island, Florida, USA.

[13] J. Sauer: Knowledge-based systems in scheduling. Knowledge-based systems techniques and applications. Vol4. Academic press (2000)

[14] S.S. Tseng, G.J. Hwang: Artificial Intelligence and Expert System : Theory, Practice and Application, Flag Publishing Co., Taiwan (2005)

[15] C.Wang, W. Shen, H. Ghenniwa: An Adaptive Negotiation Framework for Agent

Based Dynamic Manufacturing Scheduling. Systems, Man and Cybernetics. IEEE International Conference on Volume 2. Page(s):1211 - 1216 vol.2 (2003)

[16] W3C XML, World Wide Web Consortium Extensible Markup Language, http://www.w3.org/XML/

Appendix A Evaluation Raw Data

2006/4/1

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP91201AI	1N5K026.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/30	EALCU8K
AP92501AF	1N5K066.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP91201AI	1N5K136.1	PC	24	3	1TALCU01	M215DP00.01	2006/05/30	EALCU8K
AP92501AF	1N5K140.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5K145.1	PC	13	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5K145.3	PC	11	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L009.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L010.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/12	EALCU11K
AP92501AF	1N5L019.1	PC	22	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L019.2	PC	2	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L027.1	PC	22	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L028.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L029.2	PC	11	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP91201AI	1N5L073.1	PC	18	3	1TALCU01	M215DP00.01	2006/04/30	EALCU8K
AP92501AF	1N5L078.1	PC	22	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L079.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L082.1	PC	24	3	1TALCU01	M215DP00.01	2006/05/30	EALCU11K
AP92501AF	1N5L083.2	PC	11	3	1TALCU01	M215DP00.01	2006/05/30	EALCU11K
AP92501AF	1N5L085.1	PC	23	3	1TALCU01	M215DP00.01	2006/06/30	EALCU11K
AP91201AJ	1N5L104.1	EC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU8K
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L108.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L110.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L111.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K

2006/4/2

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP91201AI	1N5K026.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/30	EALCU8K
AP92501AF	1N5K066.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP91201AI	1N5K136.1	PC	24	3	1TALCU01	M215DP00.01	2006/05/30	EALCU8K
AP92501AF	1N5K140.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5K145.1	PC	13	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5K145.3	PC	11	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L009.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L010.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/12	EALCU11K
AP92501AF	1N5L019.1	PC	22	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L019.2	PC	2	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L027.1	PC	22	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L028.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L029.2	PC	11	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP91201AI	1N5L073.1	PC	18	3	1TALCU01	M215DP00.01	2006/04/30	EALCU8K
AP92501AF	1N5L078.1	PC	22	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L079.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L082.1	PC	24	3	1TALCU01	M215DP00.01	2006/05/30	EALCU11K
AP92501AF	1N5L083.2	PC	11	3	1TALCU01	M215DP00.01	2006/05/30	EALCU11K
AP92501AF	1N5L085.1	PC	23	3	1TALCU01	M215DP00.01	2006/06/30	EALCU11K
AP91201AJ	1N5L104.1	EC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU8K
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L108.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L110.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L111.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
APR0002AF	1N6A264.3	EC	1	2	1TAU0000	MSSD3DP0.01	2006/05/12	eS_Au08
APR0001AB	1N6C063.3	EC	1	3	1TCU0000	MTM1DP01.01	2006/06/16	eS_Cu06
APR0001AE	1N6C137.1	EC	24	3	1TCU0000	MTM1DP01.01	2006/06/16	eS_Cu06
APR0001AE	1N6C138.1	EC	24	3	1TCU0000	MTM1DP01.01	2006/06/16	eS_Cu06
APR0002AF	1N6C180.1	EC	24	3	1TTI0000	ZERODP00.01	2006/06/16	Ti300

2006/4/3

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP91201AI	1N5K026.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/30	EALCU8K

AP94601AD	1N5K035.1	EC	24	2	1TTAAL00	M200DP00.03	2006/04/30	S_ALCU1S
AP92501AF	1N5K066.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP91201AI	1N5K136.1	PC	24	3	1TALCU01	M215DP00.01	2006/05/30	EALCU8K
AP92501AF	1N5K140.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5K145.1	PC	13	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5K145.3	PC	11	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L009.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L010.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/12	EALCU11K
AP92501AF	1N5L019.1	PC	22	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L019.2	PC	2	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L027.1	PC	22	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L028.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L029.2	PC	11	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP91201AI	1N5L073.1	PC	18	3	1TALCU01	M215DP00.01	2006/04/30	EALCU8K
AP92501AF	1N5L078.1	PC	22	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L079.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L082.1	PC	24	3	1TALCU01	M215DP00.01	2006/05/30	EALCU11K
AP92501AF	1N5L083.2	PC	11	3	1TALCU01	M215DP00.01	2006/05/30	EALCU11K
AP92501AF	1N5L085.1	PC	23	3	1TALCU01	M215DP00.01	2006/06/30	EALCU11K
AP91201AJ	1N5L104.1	EC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU8K
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L108.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L110.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L111.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
APR0002AF	1N6A264.3	EC	1	2	1TAU0000	MSSD3DP0.01	2006/05/12	eS_Au08
APR0002AF	1N6A266.3	EC	2	3	1TCU0000	MTM1DP01.01	2006/05/05	NULL
AP94901AF	1N6C011.1	EC	24	3	1TTAAL00	M200DP00.03	2006/04/24	S_ALCU12
APR0001AB	1N6C015.2	EC	1	3	1TCU0000	MTM1DP01.01	2006/05/19	eS_Cu06
APR0002AF	1N6C137.1	EC	24	3	1TCU0000	MTM1DP01.01	2006/06/16	eS_Cu06
APR0002AF	1N6C138.1	EC	24	3	1TCU0000	MTM1DP01.01	2006/06/16	eS_Cu06
APR0002AF	1N6C181.1	EC	24	3	1TTI0000	ZERODP00.01	2006/06/16	Ti300

2006/4/4

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID

AP92501AF	1N5K066.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5K140.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5K145.1	PC	13	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5K145.3	PC	11	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L009.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L010.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/12	EALCU11K
AP92501AF	1N5L019.1	PC	22	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L019.2	PC	2	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L027.1	PC	22	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L028.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L029.2	PC	11	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L078.1	PC	22	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L079.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L082.1	PC	24	3	1TALCU01	M215DP00.01	2006/05/30	EALCU11K
AP92501AF	1N5L083.2	PC	11	3	1TALCU01	M215DP00.01	2006/05/30	EALCU11K
AP92501AF	1N5L085.1	PC	23	3	1TALCU01	M215DP00.01	2006/06/30	EALCU11K
AP91201AJ	1N5L104.1	EC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU8K
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L108.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L110.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L111.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
APR0002AF	1N6A264.3	EC	1	2	1TAU0000	MSSD3DP0.01	2006/05/12	eS_Au08
APR0001AE	1N6B038.9	EC	1	1	1TCU0000	MSSD4DP0.01	2006/04/21	S_Cu06
APR0001AE	1N6B038.9	EC	1	1	1TCU0000	MSSD4DP0.01	2006/04/21	S_Cu06
AP93301AB	1N6C005.1	EC	24	2	1TTAAL00	M211DP00.01	2006/04/30	S_ALCU35
AP94901AF	1N6C008.1	EC	24	3	1TTAAL00	M200DP00.03	2006/04/30	S_ALCU12
AP94901AF	1N6C009.1	EC	24	3	1TTAAL00	M200DP00.03	2006/04/30	S_ALCU12
AP93101AB	1N6C012.1	EC	24	2	1TTAAL00	M200DP00.03	2006/04/16	S_ALCU2S
APR0002AF	1N6C015.2	EC	1	3	1TCU0000	MTM1DP01.01	2006/05/19	eS_Cu06
AP95201AB	1N6C020.1	EC	24	3	1TTAAL00	M200DP00.03	2006/04/25	S_ALCU2S
AP94701AA	1N6C022.1	EC	24	2	1TTAAL00	M200DP00.03	2006/04/20	S_ALCU1S
AP95201AB	1N6C051.1	EC	24	2	1TTAAL00	M200DP00.03	2006/04/19	S_ALCU2S
AP95201AB	1N6C052.1	EC	24	2	1TTAAL00	M200DP00.03	2006/04/14	S_ALCU2S
APR0002AF	1N6C063.3	EC	1	3	1TCU0000	MTM1DP01.01	2006/06/16	eS_Cu06
APR0002AF	1N6C137.1	EC	24	3	1TCU0000	MTM1DP01.01	2006/06/16	eS_Cu06
APR0002AF	1N6C138.1	EC	24	3	1TCU0000	MTM1DP01.01	2006/06/16	eS_Cu06

APR0002AF	1N6C138.1	EC	24	3	1TCU0000	MTM1DP01.01	2006/06/16	eS_Cu06
TK21501AA	1P5L021.1	EP	8	2	1TALCU00	M2CLDP00.01	2006/03/31	S_ALCUM

2006/4/5

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP92501AF	1N5K066.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5K140.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5K145.1	PC	13	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5K145.3	PC	11	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L009.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L010.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/12	EALCU11K
AP92501AF	1N5L019.1	PC	22	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L019.2	PC	2	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L027.1	PC	22	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L028.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L029.2	PC	11	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L078.1	PC	22	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L079.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L082.1	PC	24	3	1TALCU01	M215DP00.01	2006/05/30	EALCU11K
AP92501AF	1N5L083.2	PC	11	3	1TALCU01	M215DP00.01	2006/05/30	EALCU11K
AP92501AF	1N5L085.1	PC	23	3	1TALCU01	M215DP00.01	2006/06/30	EALCU11K
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L108.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L110.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L111.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
APR0002AF	1N6A264.3	EC	1	2	1TAU0000	MSSD3DP0.01	2006/05/12	eS_Au08
AP95201AB	1N6B082.1	EC	12	3	1TTAAL00	M200DP00.03	2006/04/14	S_ALCU2S

2006/4/6

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP92501AF	1N5K066.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5K140.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K

AP92501AF	1N5K145.1	PC	13	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5K145.3	PC	11	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L019.1	PC	22	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L019.2	PC	2	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L027.1	PC	22	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L028.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L029.2	PC	11	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L078.1	PC	22	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L079.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L083.2	PC	11	3	1TALCU01	M215DP00.01	2006/05/30	EALCU11K
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L110.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP91201AI	1N6A048.1	PC	22	4	1TALCU01	M109DP00.01	2006/04/30	EALCU5K
APR0002AF	1N6A264.3	EC	1	2	1TAU0000	MSSD3DP0.01	2006/05/12	eS_Au08
APR0002AF	1P6C158.1	EP	24	3	1TCU0000	MTM1DP01.01	2006/04/15	eS_Cu06

2006/4/7

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP92501AF	1N5K066.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5K140.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5K145.1	PC	13	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5K145.3	PC	11	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L019.1	PC	22	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L019.2	PC	2	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L027.1	PC	22	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L028.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L029.2	PC	11	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L078.1	PC	22	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L079.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L083.2	PC	11	3	1TALCU01	M215DP00.01	2006/05/30	EALCU11K
AP92501AF	1N5L084.1	PC	24	3	1TALCU01	M109DP00.01	2006/04/30	EALCU7K1
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L110.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K

AP92501AF	1N6A065.1	PC	24	3	1TALCU01	M215DP00.01	2006/06/30	EALCU11K
APR0002AF	1N6A264.3	EC	1	2	1TAU0000	MSSD3DP0.01	2006/05/12	eS_Au08
AP95201AB	1N6C021.1	EC	24	3	1TTAAL00	M200DP00.03	2006/04/25	S_ALCU2S
AP94701AA	1N6C023.1	EC	24	3	1TTAAL00	M200DP00.03	2006/04/24	S_ALCU1S
AP10604BD	1N6C139.1	PC	24	2	1TALSICU	ALSCDP00.01	2006/04/28	ALCU8K

2006/4/8

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP92501AF	1N5K066.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5K140.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5K145.1	PC	13	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L019.1	PC	22	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L019.2	PC	2	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L027.1	PC	22	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L028.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L029.2	PC	11	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L078.1	PC	22	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L079.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L083.2	PC	11	3	1TALCU01	M215DP00.01	2006/05/30	EALCU11K
AP91201AI	1N5L097.1	PC	24	3	1TALCU01	M109DP00.01	2006/04/30	EALCU5K
AP91201AI	1N5L100.1	EP	24	3	1TALCU01	M215DP00.01	2006/03/30	EALCU8K
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L110.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP91201AI	1N6A049.1	PC	23	4	1TALCU01	M109DP00.01	2006/04/30	EALCU5K
AP92501AF	1N6A065.1	PC	24	3	1TALCU01	M215DP00.01	2006/06/30	EALCU11K
APR0002AF	1N6A264.3	EC	1	2	1TAU0000	MSSD3DP0.01	2006/05/12	eS_Au08

2006/4/9

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP92501AF	1N5K066.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5K140.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5K145.1	PC	13	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K

AP92501AF	1N5L019.2	PC	2	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L027.1	PC	22	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L028.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L083.2	PC	11	3	1TALCU01	M215DP00.01	2006/05/30	EALCU11K
AP91201AI	1N5L100.1	EP	24	3	1TALCU01	M215DP00.01	2006/03/30	EALCU8K
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N6A065.1	PC	24	3	1TALCU01	M215DP00.01	2006/06/30	EALCU11K
APR0002AF	1N6A264.3	EC	1	2	1TAU0000	MSSD3DP0.01	2006/05/12	eS_Au08
AP94701AA	1N6C024.1	EC	22	3	1TTAAL00	M200DP00.03	2006/04/24	S_ALCU1S

2006/4/10

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP92501AF	1N5K066.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5L083.2	PC	11	3	1TALCU01	M215DP00.01	2006/05/30	EALCU11K
AP91201AI	1N5L100.1	EP	24	3	1TALCU01	M215DP00.01	2006/03/30	EALCU8K
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N6A065.1	PC	24	3	1TALCU01	M215DP00.01	2006/06/30	EALCU11K
APR0002AF	1N6A264.3	EC	1	2	1TAU0000	MSSD3DP0.01	2006/05/12	eS_Au08
APR0001AE	1N6B038.9	EC	1	1	1TCU0000	MSSD4DP0.01	2006/04/21	S_Cu06
AP95201AB	1N6B082.1	PC	12	2	1TTAAU01	TAU3DP00.01	2006/04/14	ETAAU4
APR0002AF	1N6C014.1	EC	12	2	1TCU0000	MTM1DP01.01	2006/06/16	eS_Cu06
APR0002AF	1N6C014.2	EC	12	2	1TCU0000	MTM1DP01.01	2006/06/16	eS_Cu06
AP95201AB	1N6C052.1	PC	24	2	1TTAAU01	TAU3DP00.01	2006/04/14	ETAAU4

Appendix B Lot Scheduling Results

Result of Human Expert 1

2006/04/01

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP92501AF	1N5L010.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/12	EALCU11K
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L111.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5K066.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K

2006/04/02

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP92501AF	1N5L010.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/12	EALCU11K
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L111.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5K066.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K

2006/04/03

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP94601AD	1N5K035.1	EC	24	2	1TTAAL00	M200DP00.03	2006/04/30	S_ALCU1S
AP94901AF	1N6C011.1	EC	24	3	1TTAAL00	M200DP00.03	2006/04/24	S_ALCU12
APR0001AB	1N6C015.2	EC	1	3	1TCU0000	MTM1DP01.01	2006/05/19	eS_Cu06
APR0002AF	1N6C137.1	EC	24	3	1TCU0000	MTM1DP01.01	2006/06/16	eS_Cu06
APR0002AF	1N6C138.1	EC	24	3	1TCU0000	MTM1DP01.01	2006/06/16	eS_Cu06

2006/04/04

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
APR0001AE	1N6B038.9	EC	1	1	1TCU0000	MSSD4DP0.01	2006/04/21	S_Cu06
AP93301AB	1N6C005.1	EC	24	2	1TTAAL00	M211DP00.01	2006/04/30	S_ALCU35
AP95201AB	1N6C052.1	EC	24	2	1TTAAL00	M200DP00.03	2006/04/14	S_ALCU2S
AP93101AB	1N6C012.1	EC	24	2	1TTAAL00	M200DP00.03	2006/04/16	S_ALCU2S
AP95201AB	1N6C051.1	EC	24	2	1TTAAL00	M200DP00.03	2006/04/19	S_ALCU2S

2006/04/05

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP95201AB	1N6B082.1	EC	12	3	1TTAAL00	M200DP00.03	2006/04/14	S_ALCU2S
AP92501AF	1N5L010.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/12	EALCU11K
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L111.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K

2006/04/06

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
APR0002AF	1P6C158.1	EP	24	3	1TCU0000	MTM1DP01.01	2006/04/15	eS_Cu06
APR0002AF	1N6A264.3	EC	1	2	1TAU0000	MSSD3DP0.01	2006/05/12	eS_Au08
AP91201AI	1N6A048.1	PC	22	4	1TALCU01	M109DP00.01	2006/04/30	EALCU5K
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K

2006/04/07

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP95201AB	1N6C021.1	EC	24	3	1TTAAL00	M200DP00.03	2006/04/25	S_ALCU2S
AP94701AA	1N6C023.1	EC	24	3	1TTAAL00	M200DP00.03	2006/04/24	S_ALCU1S
AP92501AF	1N5L084.1	PC	24	3	1TALCU01	M109DP00.01	2006/04/30	EALCU7K1

AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K

2006/04/08

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP91201AI	1N5L100.1	EP	24	3	1TALCU01	M215DP00.01	2006/03/30	EALCU8K
AP91201AI	1N5L097.1	PC	24	3	1TALCU01	M109DP00.01	2006/04/30	EALCU5K
AP91201AI	1N6A049.1	PC	23	4	1TALCU01	M109DP00.01	2006/04/30	EALCU5K
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K

2006/04/09

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP94701AA	1N6C024.1	EC	22	3	1TTAAL00	M200DP00.03	2006/04/24	S_ALCU1S
AP91201AI	1N5L100.1	EP	24	3	1TALCU01	M215DP00.01	2006/03/30	EALCU8K
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5K066.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K

2006/04/10

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
APR0001AE	1N6B038.9	EC	1	1	1TCU0000	MSSD4DP0.01	2006/04/21	S_Cu06
APR0002AF	1N6C014.1	EC	12	2	1TCU0000	MTM1DP01.01	2006/06/16	eS_Cu06
APR0002AF	1N6C014.2	EC	12	2	1TCU0000	MTM1DP01.01	2006/06/16	eS_Cu06
AP95201AB	1N6B082.1	PC	12	2	1TTAAU01	TAU3DP00.01	2006/04/14	ETAAU4
AP95201AB	1N6C052.1	PC	24	2	1TTAAU01	TAU3DP00.01	2006/04/14	ETAAU4

Result of Human Expert 2

2006/04/01

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP92501AF	1N5L010.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/12	EALCU11K
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L111.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5K066.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K

2006/04/02

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP92501AF	1N5L010.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/12	EALCU11K
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L111.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5K066.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K

2006/04/03

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP94601AD	1N5K035.1	EC	24	2	1TTAAL00	M200DP00.03	2006/04/30	S_ALCU1S
AP94901AF	1N6C011.1	EC	24	3	1TTAAL00	M200DP00.03	2006/04/24	S_ALCU12
APR0001AB	1N6C015.2	EC	1	3	1TCU0000	MTM1DP01.01	2006/05/19	eS_Cu06
APR0002AF	1N6C137.1	EC	24	3	1TCU0000	MTM1DP01.01	2006/06/16	eS_Cu06
APR0002AF	1N6C138.1	EC	24	3	1TCU0000	MTM1DP01.01	2006/06/16	eS_Cu06

2006/04/04

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID

APR0001AE	1N6B038.9	EC	1	1	1TCU0000	MSSD4DP0.01	2006/04/21	S_Cu06
AP95201AB	1N6C052.1	EC	24	2	1TTAAL00	M200DP00.03	2006/04/14	S_ALCU2S
AP93101AB	1N6C012.1	EC	24	2	1TTAAL00	M200DP00.03	2006/04/16	S_ALCU2S
AP95201AB	1N6C051.1	EC	24	2	1TTAAL00	M200DP00.03	2006/04/19	S_ALCU2S
AP95201AB	1N6C020.1	EC	24	3	1TTAAL00	M200DP00.03	2006/04/25	S_ALCU2S

2006/04/05

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP95201AB	1N6B082.1	EC	12	3	1TTAAL00	M200DP00.03	2006/04/14	S_ALCU2S
AP92501AF	1N5L010.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/12	EALCU11K
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L111.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K

2006/04/06

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
APR0002AF	1P6C158.1	EP	24	3	1TCU0000	MTM1DP01.01	2006/04/15	eS_Cu06
APR0002AF	1N6A264.3	EC	1	2	1TAU0000	MSSD3DP0.01	2006/05/12	eS_Au08
AP91201AI	1N6A048.1	PC	22	4	1TALCU01	M109DP00.01	2006/04/30	EALCU5K
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K

2006/04/07

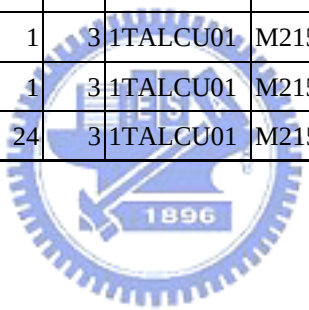
Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP95201AB	1N6C021.1	EC	24	3	1TTAAL00	M200DP00.03	2006/04/25	S_ALCU2S
AP94701AA	1N6C023.1	EC	24	3	1TTAAL00	M200DP00.03	2006/04/24	S_ALCU1S
AP92501AF	1N5L084.1	PC	24	3	1TALCU01	M109DP00.01	2006/04/30	EALCU7K1
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K

2006/04/08

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP91201AI	1N5L100.1	EP	24	3	1TALCU01	M215DP00.01	2006/03/30	EALCU8K
AP91201AI	1N5L097.1	PC	24	3	1TALCU01	M109DP00.01	2006/04/30	EALCU5K
AP91201AI	1N6A049.1	PC	23	4	1TALCU01	M109DP00.01	2006/04/30	EALCU5K
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K

2006/04/09

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP94701AA	1N6C024.1	EC	22	3	1TTAAL00	M200DP00.03	2006/04/24	S_ALCU1S
AP91201AI	1N5L100.1	EP	24	3	1TALCU01	M215DP00.01	2006/03/30	EALCU8K
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5K066.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K



2006/04/10

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
APR0001AE	1N6B038.9	EC	1	1	1TCU0000	MSSD4DP0.01	2006/04/21	S_Cu06
APR0002AF	1N6C014.1	EC	12	2	1TCU0000	MTM1DP01.01	2006/06/16	eS_Cu06
APR0002AF	1N6C014.2	EC	12	2	1TCU0000	MTM1DP01.01	2006/06/16	eS_Cu06
AP95201AB	1N6B082.1	PC	12	2	1TTAAU01	TAU3DP00.01	2006/04/14	ETAAU4
AP95201AB	1N6C052.1	PC	24	2	1TTAAU01	TAU3DP00.01	2006/04/14	ETAAU4

Result of LS-KBS

2006/04/01

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID

AP92501AF	1N5L010.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/12	EALCU11K
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L111.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5K066.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K

2006/04/02

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP92501AF	1N5L010.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/12	EALCU11K
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L111.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5K066.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K

2006/04/03

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP94601AD	1N5K035.1	EC	24	2	1TTAAL00	M200DP00.03	2006/04/30	S_ALCU1S
AP94901AF	1N6C011.1	EC	24	3	1TTAAL00	M200DP00.03	2006/04/24	S_ALCU12
APR0001AB	1N6C015.2	EC	1	3	1TCU0000	MTM1DP01.01	2006/05/19	eS_Cu06
APR0002AF	1N6C137.1	EC	24	3	1TCU0000	MTM1DP01.01	2006/06/16	eS_Cu06
APR0002AF	1N6C138.1	EC	24	3	1TCU0000	MTM1DP01.01	2006/06/16	eS_Cu06

2006/04/04

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
APR0001AE	1N6B038.9	EC	1	1	1TCU0000	MSSD4DP0.01	2006/04/21	S_Cu06
AP95201AB	1N6C052.1	EC	24	2	1TTAAL00	M200DP00.03	2006/04/14	S_ALCU2S
AP93101AB	1N6C012.1	EC	24	2	1TTAAL00	M200DP00.03	2006/04/16	S_ALCU2S
AP95201AB	1N6C051.1	EC	24	2	1TTAAL00	M200DP00.03	2006/04/19	S_ALCU2S
AP95201AB	1N6C020.1	EC	24	3	1TTAAL00	M200DP00.03	2006/04/25	S_ALCU2S
AP94701AA	1N6C022.1	EC	24	2	1TTAAL00	M200DP00.03	2006/04/20	S_ALCU1S
AP93301AB	1N6C005.1	EC	24	2	1TTAAL00	M211DP00.01	2006/04/30	S_ALCU35

AP94901AF	1N6C008.1	EC	24	3	1TTAAL00	M200DP00.03	2006/04/30	S_ALCU12
AP94901AF	1N6C009.1	EC	24	3	1TTAAL00	M200DP00.03	2006/04/30	S_ALCU12

2006/04/05

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP95201AB	1N6B082.1	EC	12	3	1TTAAL00	M200DP00.03	2006/04/14	S_ALCU2S
AP92501AF	1N5L010.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/12	EALCU11K
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L111.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K

2006/04/06

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
APR0002AF	1P6C158.1	EP	24	3	1TCU0000	MTM1DP01.01	2006/04/15	eS_Cu06
APR0002AF	1N6A264.3	EC	1	2	1TAU0000	MSSD3DP0.01	2006/05/12	eS_Au08
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5K066.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP92501AF	1N5K140.1	PC	23	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K
AP91201AI	1N6A048.1	PC	22	4	1TALCU01	M109DP00.01	2006/04/30	EALCU5K

2006/04/07

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP95201AB	1N6C021.1	EC	24	3	1TTAAL00	M200DP00.03	2006/04/25	S_ALCU2S
AP94701AA	1N6C023.1	EC	24	3	1TTAAL00	M200DP00.03	2006/04/24	S_ALCU1S
AP92501AF	1N5L084.1	PC	24	3	1TALCU01	M109DP00.01	2006/04/30	EALCU7K1
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K

2006/04/08

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP91201AI	1N5L100.1	EP	24	3	1TALCU01	M215DP00.01	2006/03/30	EALCU8K
AP91201AI	1N5L097.1	PC	24	3	1TALCU01	M109DP00.01	2006/04/30	EALCU5K
AP91201AI	1N6A049.1	PC	23	4	1TALCU01	M109DP00.01	2006/04/30	EALCU5K
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K

2006/04/09

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
AP94701AA	1N6C024.1	EC	22	3	1TTAAL00	M200DP00.03	2006/04/24	S_ALCU1S
AP91201AI	1N5L100.1	EP	24	3	1TALCU01	M215DP00.01	2006/03/30	EALCU8K
AP92501AF	1N5L107.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5L110.2	PC	1	3	1TALCU01	M215DP00.01	2006/04/20	EALCU11K
AP92501AF	1N5K066.1	PC	24	3	1TALCU01	M215DP00.01	2006/04/30	EALCU11K

2006/04/10

Product	Lot	Type	Qty	Pri	Capability	Recipe	Due Date	PPID
APR0001AE	1N6B038.9	EC	1	1	1TCU0000	MSSD4DP0.01	2006/04/21	S_Cu06
APR0002AF	1N6C014.1	EC	12	2	1TCU0000	MTM1DP01.01	2006/06/16	eS_Cu06
APR0002AF	1N6C014.2	EC	12	2	1TCU0000	MTM1DP01.01	2006/06/16	eS_Cu06
AP95201AB	1N6B082.1	PC	12	2	1TTAAU01	TAU3DP00.01	2006/04/14	ETAAU4
AP95201AB	1N6C052.1	PC	24	2	1TTAAU01	TAU3DP00.01	2006/04/14	ETAAU4

簡　　歷

黃 亮 中 (Liang-Chung, Huang) Mar-29, 1972

< 工作經歷 >

2002.06 – 迄今 亞太優勢微系統

目前擔任本公司系統運作部副理，工作內容涵括前段後段晶圓製造生產管理系統運作，工程資料分析系統運作，及各項系統客製化需求開發。公司成立初期，負責生產管理系統之導入工作；目前公司已進入量產階段，藉由對生產流程及資訊系統之熟悉，附加過去在其他廠的經驗，冀望能提昇公司生產營運效率，並強化公司的競爭力。

2001.11 – 2002.05 上海中芯國際

擔任機台連線自動化專案 Leader，帶領一個 14 人的團隊進行機台連線自動化專案，除了導入自行研發的機台連線系統及建立架構外，並訓練這 14 位大陸剛畢業的大學生成為半導體自動化的人員。

1999.11 – 2001.10 華邦電子

負責機台連線。進入半導體製造產業，參與與生產線、工程部門息息相關的機台自動化部門，負責開發依製程特性或機台型別不同的自動化連線程式；由於對 communication protocol SECS/GEM 的熟悉，附加對製程的了解，擔任 survey 先進製程控管 solution 的 coordinator，與三家廠商進行長達 8 個月之線上測試與驗證之工作。

1997.07 – 1999.11 長榮海運

由系統開發人員(程式設計師)做起，爾後曾擔任系統分析人員、全球化系統開發及推展人員，在此 Global 的企業中，深切感受到，做任何事皆須有全球化的眼光。