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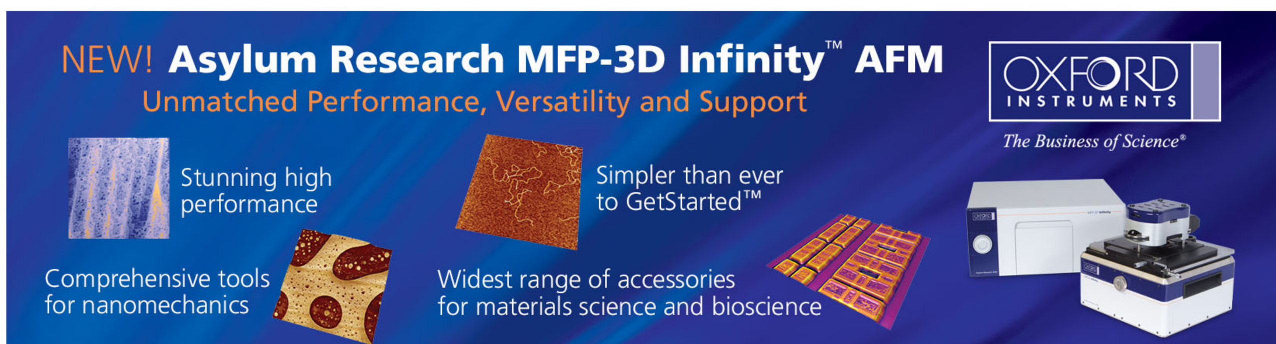

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Crucial integration of high work-function metal gate and high-*k* blocking oxide on charge-trapping type flash memory device

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Charge-trapping type flash memory devices with various integrations of metal gates having different work functions and blocking oxides were investigated in this work. Improved erasing speed together with acceptable reliability characteristics can be achieved by the integration of high work-function metal gate and high-*k* blocking oxide due to an efficient suppression of electron back tunneling through the blocking oxide during erasing operation for the MoN sample. Specifically, the high work-function value of MoN metal gate can be kept only by integrating with the Al_2O_3 blocking oxide because it can suppress the formation of molybdenum-silicide. Moreover, high-speed erasing can also be demonstrated by combining the MoN metal gate with an HfAlO charge trapping layer when band-to-band hot hole erasing method is adopted. © *2008 American Institute of Physics*. [DOI: 10.1063/1.3043976]

Polysilicon-oxide-nitride-oxide-silicon (SONOS) nonvolatile memory (NVM) device is one of the most attractive candidates in realizing the continuity of vertical scaling on flash memory.[1–3] However, the phenomenon of electron back tunneling (EBT) is known as a serious concern due to the limitation caused by the low erase states threshold voltage V_{th} during higher erasing voltage.[4,5] Besides, characteristics such as erasing speed and the phenomenon of overerase are still main bottlenecks for SONOS devices to replace the floating-gate ones. In order to overcome these limitations, some approaches about adopting high work-function (WF) metal gate and high-*k* charge trapping layer for the NVM device have been proposed.[6,7] However, the integration of high-WF metal gate, high-*k* blocking oxide, and high-*k* trapping layer has rarely been reported. In this work, effects of various metal gates and different blocking oxides on the erasing characteristics for traditional SONOS devices are investigated first. Afterward, the integration of MoN metal gate, HfAlO charge trapping layer, and Al_2O_3 blocking oxide was further studied in detail based on the above result.[8]

Metal-oxide-semiconductor (MOS) capacitors with MONOS [the flash device with metal/$SiO_2/Si_3N_4/SiO_2$/SI (MONOS) structure] (ONO, the flash device with gate/$SiO_2/Si_3N_4/SiO_2$/SI structure) and MANOS [the flash device with metal/$Al_2O_3/Si_3N_4/SiO_2$/SI (MANOS) structure] (ANO, the flash device with gate/$Al_2O_3/Si_3N_4/SiO_2$/SI structure) and flash cells with MAHOS [the flash device with metal/Al_2O_3/high-k/SiO_2/SI (MONOS) structure] (AHO) structures were respectively fabricated. A tunneling SiO_2 was formed by an advanced clustered vertical furnace on the cleaned *p*-type wafers; its thickness is ~4.0–5.0 nm for capacitor devices and ~3.0 nm for flash cell devices.

For capacitor devices, the ~6 nm Si_3N_4 trapping layer was deposited after the formation of tunneling oxide. Next, a blocking oxide with 7.5–8 nm SiO_2 (samples S1 and S2)[9] and with 15 nm Al_2O_3 (S3)[9] was formed by low-pressure chemical vapor deposition (CVD) and metal-organic CVD systems, individually. Afterward, TaN (S1)[9] and MoN (S2 and S3)[9] metal gates on ONO stack were deposited by a sputter system. Finally, high temperature annealing was performed to all samples, which were intended to simulate the influences of source/drain activation in general NVM cell processes.

For AHO flash cell devices, ~6 nm HfAlO films as charge-trapping layer and ~15 nm Al_2O_3 films as blocking oxide were subsequently deposited by atomic layer deposition system after the formation of tunneling oxide, followed by a deposition of TaN (S4)[9] or MoN (S5)[9] metal gate using a sputter system. After gate patterning, source/drain regions were formed by implantation with arsenic, activated at 900 °C for 30 s. Finally, sintering was conducted in a N_2/H_2 ambient at 420 °C for 30 min.

The erasing characteristics for SONOS devices with various blocking oxides and metal gates are illustrated in Fig. 1(a). The erasing speed of S2 (MoN) sample is obviously enhanced as compared with that of S1 (TaN) one. This illustrates that the erasing properties can be improved by adopting high-WF metal gate. Figure 1(b) shows a schematic energy band diagram of SONOS devices with the two different metal gates during erasing operations. For a TaN gate with WF value of ~4.5 eV, a relatively low electron barrier height is observed; it results in an additional electron current ($J_{e,TaN}$) injecting from the metal gate. Therefore, the sum of J_e and hole current J_h causes a small erasing window and a low erasing speed. However, with an increased WF value (~5.15 eV) by adopting MoN gate, erasing characteristics are obviously improved due to the rise in electron barrier height and the suppression of the additional electron current ($J_{e,MoN}$) injecting under erasing mode.

Next, the erasing performances of devices with MoN gate combined with different blocking oxides were investigated. The erasing speed for a device with Al_2O_3 blocking

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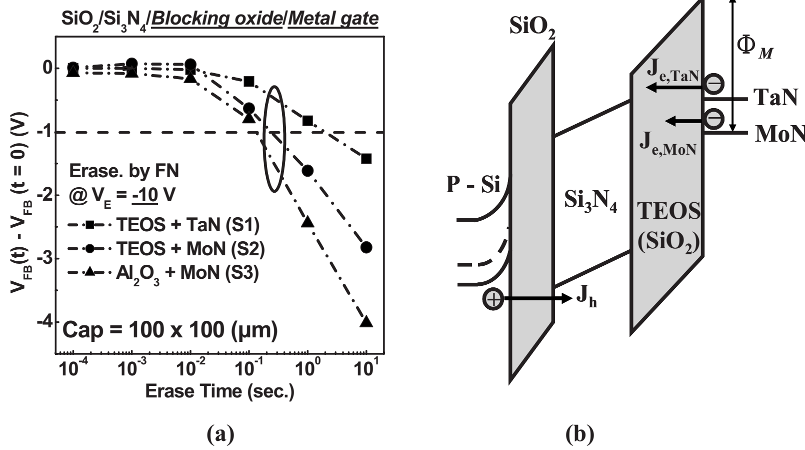

FIG. 1. (a) The erasing characteristics with erasing voltage $[V_{\mathrm{Erase}}(V_{\mathrm{E}})=(V_{\mathrm{Gate}}(V_{\mathrm{G}})-V_{\mathrm{Flatband}}(V_{\mathrm{FB}})]=-10$ V for charge-trapping type capacitors with various blocking oxides and metal gates. (b) Energy band diagram of charge-trapping type devices with various metal gates during erasing operations.

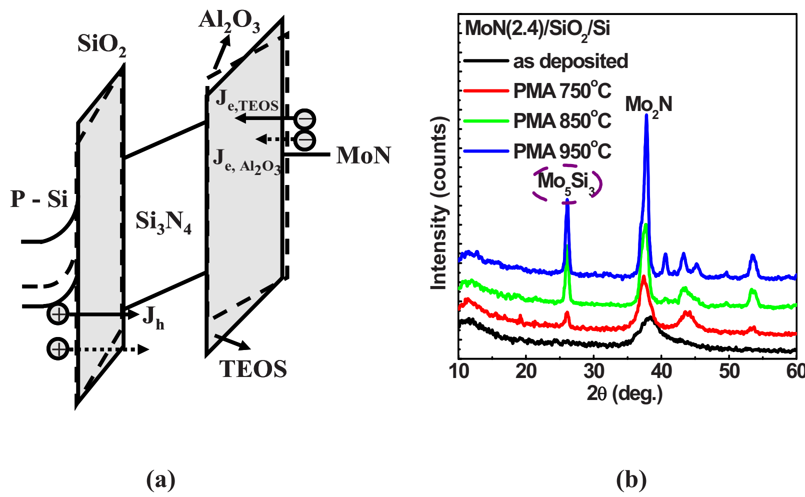

FIG. 2. (Color online) (a) Energy band diagram of charge-trapping type devices with MoN gate and various blocking oxides during erasing operations. (b) XRD spectra of MoN metal gate deposited on SiO_2 blocking oxide with different temperature annealings.

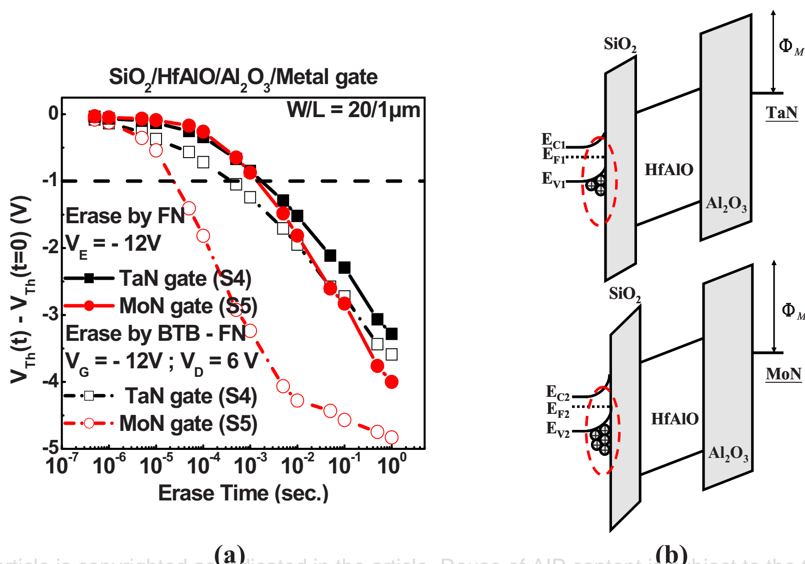

FIG. 3. (Color online) (a) Erasing characteristics for S4 and S5 (Ref. 9) samples with $[V_{\mathrm{Erase}}(V_{\mathrm{E}})=V_{\mathrm{Gate}}(V_{\mathrm{G}})-V_{\mathrm{Threshold}}(V_{\mathrm{Th}})]=-12$ V (channel FN) and $V_g/V_d=-12/6$ V (BTB hot hole), respectively. (b) Energy band diagram of the MAHOS NVM device with TaN and MoN gates during BTB hot hole erasing operations.

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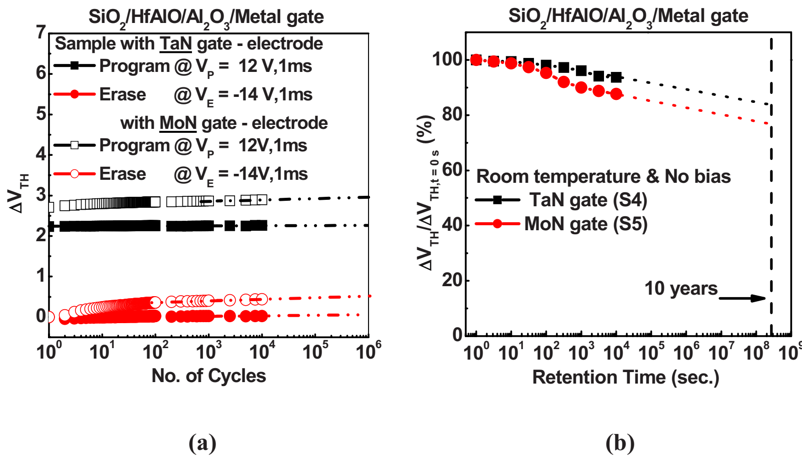

FIG. 4. (Color online) (a) P/E endurance characteristics of MAHOS NVM device with TaN (S4) and MoN (S5) (Ref. 9) metal gates. (b) Data retention of the normalized V_t window for MAHOS devices with TaN (S4) and MoN (S5) (Ref. 9) metal gates after the data retention test.

oxide (S3)[9] is clearly higher than that with the traditional SiO_2 (S2).[9] The enhancement in erasing properties can be explained by examining the band diagram illustrated in Fig. 2(a). The additional electron current ($J_{e,\mathrm{Al2O3}}$) during operation is suppressed by the Al_2O_3 blocking oxide, which possesses larger physical thickness as compared with the SiO_2 one having identical effective thickness.[8]

The influence caused by the formation of molybdenum-silicide is another issue that needs to be studied. Figure 2(b) displays the x-ray diffraction (XRD) spectra for samples with MoN deposited on SiO_2 oxide under different annealing temperatures. The crystalline peak of Mo_5Si_3 is clearly observed after high temperature annealing, which indicates the formation of molybdenum silicide. The presence of molybdenum silicide in MoN film may lower down the WF value.[10] Therefore, the integration of MoN gate with Al_2O_3 blocking oxide can suppress the formation of metal silicide, thus enhance the erasing characteristics of the flash device.

To further improve the operating speed, the metal gates of TaN (S4)[9] and MoN (S5)[9] were adopted for NVM devices with MAHOS structures.[7] Once more, the enhancement in erasing speed by the Fowler–Nordheim (FN) operation for NVM device with MoN metal gate is achieved as shown in Fig. 3(a), which can also be attributed to the suppression of EBT through the blocking oxide during erasing operation. In addition, adopting MoN gate leads to a higher magnitude in hole current, which exceeds the electron current under erasing mode. As a result, the erasing V_{th} can be lower than that of the TaN one.

Regarding NOR device applications, erasing with band-to-band (BTB) hot hole was adopted and the relative erasing characteristics are also shown in Fig. 3(a). Results indicate that the improvement in erasing speed is obvious for the MoN sample. Since adopting BTB hot hole erasing leads to a higher electric field across the gate and the drain sides, the additional electron tunneling current from metal gate can be suppressed more efficiently with the MoN gate. Besides, due to the higher WF value of MoN gate, its substrate and tunneling oxide bands bend downward much larger than those of the TaN one at thermal equilibrium. Therefore, when the fixed erasing voltage of BTB-FN operation is applied, a more band bending for the substrate of MoN device can be expected [Fig. 3(b)], which leads to more hot-hole accumulation during BTB-FN operation and then causes more hot holes to be injected into the trapping layer.

Finally, some reliability characteristics for MAHOS flash devices with different metal gates were investigated. The program/erase (P/E) endurance characteristics of the S4 and S5[9] samples are plotted in Fig. 4(a). The results show that both memory windows remain large enough (~2.2 and 2.5 V) and only a negligible V_t-shift is seen. The remained threshold voltage (V_{th}) windows after data retention test for MAHOS flash devices with different metal gates are illustrated in Fig. 4(b). Anticipated memory window loss after 10 years is about ~17.3% for the S4[9] sample and ~23.5% for the S5,[9] indicating that the retention performance for all samples is acceptable.

Electrical characteristics of charge-trapping type flash memory devices with various metal gates and blocking oxides are studied in this work. Results indicate that the erasing performance of flash devices can be improved by adopting high-WF metal gate. Notably, the MoN metal gate should be integrated with high-k blocking oxide to keep its high work function. Besides, by integrating the MoN gate, Al_2O_3 blocking oxide, and HfAlO charge trapping layer of MAHOS flash devices and adopting BTB hot hole erasing method, high erasing speed and satisfactory reliability characteristics are also demonstrated.

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