國 立 交 通 大 學

工學院專班半導體材料與製程設備學程

碩 士 論 文

使用 I-line stepper 開發 Low cost 及可大量生產之

0.25 μm gate pHEMT

Development of Cost Effective and Manufacturable 0.25 μm gate-length Power pHEMT using I-line Stepper

研 究 生：賴宗志

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in Partial Fulfillment of the Requirements

for the Degree of

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in

Program of Semiconductor Material and Processing Equipment

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摘要

當無線通訊的應用越來越廣泛，頻寬的需求增加，元件所需的線寬，則趨向更小的尺寸，以增加元件射頻的特性，本論文之 gate 線寬尺寸目標為 0.25 μm，操作頻寬約為 10Ghz-40Ghz，並以傳統 I-line stepper 來達成，目前 sub-micro 線寬之元件以 E-beam writer 為主流，故以 I-line stepper 來開發元件可以使 cost 下降，以達到大

量生產的需求為本篇論文探討的重點。

在本篇論文中將以正負光阻及光阻之 re-flow 製程來形成 T 型閘極並達到閘極線寬有效縮小，形成所需要之閘極線寬 0.25 μm 製程，本實驗並將導入 6 寸之砷化鎵晶片的量產開發，過程中對於光阻的 hard-bake 及 re-flow 與線寬的關係作了許多研究，以達成晶片之均一性及製程穩定性，最後對於光阻的去除上，在考量晶片的潔淨與 gate 的 damage 成為實驗的主要挑戰，晶片表面的潔淨是一個重要的課題，元件的崩潰電壓及元件的可靠度及晶片上的良率皆有其相對重要的關係。

閘級的製程主要是在 AlGaAs/InGaAs 雙層摻雜(其中 Al 含量為 0.24，銦含量為 0.15)之通道層的砷化鎵晶圓上加工，此元件主要作為 Ka/Ku band 之 MMICs 功率放大器之應用上，此實驗中轉導值(Gm)亦提高為 452 mS/mm，此元件也展現了在 VDS=1.5V, VGS=-0.45V,條件下高達 58.9 GHz 的高截止頻率(fT)與 146.82 GHz 的最高震盪頻率(fmax) ，此實驗所產生的崩潰電壓約為 19.7 伏特。

在 RF 特性上亦展現出優異之特性，在 Ka band 29 GHz 下有 P1db =390-430 mW/mm 及最大之 33.3% 之 PAE ，定義在 VD=6V, ID=133mA/mm, VG=-0.55V，在 Ku band 10 GHz 下有 P1db =550 mW/mm 及最大之 47.2% 之 PAE ，定義在 VD=7V, ID=133mA/mm, VG=-0.8V，本製程之元件亦通過 MTTF 可靠度測試，其 MTTF 超過 106 小時。

Development of cost Effective and manufacturable 0.25μm gate-length Power pHEMT using I-line stepper

Student: William Lai Advisor: Dr. Edward Yi Chang

College Engineering

National Chiao Tung University

Abstract

A robust, manufacturable and coat effective high-performance 0.25 μm gate length AlGaAs/InGaAs pseudomorphic High-Electron Mobility Transistor (pHEMT) MMICs process on 150 mm substrates is revealed. The process that base on 0.25 μm gate lengths are achieved using cost effective I-line photolithography process technology. The gate process is by triple photo resister layers and re-flows to 0.25 μm by photo resister bake process. The process features a depletion-mode transistor with a nominal Pinch-off voltage

@ Ig=1 mA/mm of -1.2V, on-resistance of 0.8 ohm-mm, Extrinsinic Transconductance (GM_PEAK) is 450 mS/mm, gate to- drain breakdown voltage of 19.5 V, unity current gain cut-off frequency of 146.82 GHz (peak), Cut-off frequency (ft) @ Vds=1.5 volt of 60 GHz, IDmax @VDS=1.5 V, VGS=0.5 V of 500 mA/mm, and Drain current @VGS=0 V;VDS=1.5 V of 300 mA/mm. Passive components include 400 pF/mm2 MIM capacitors, 150 ohm/square epitaxial resistors, precision 50 ohm/square TaN resistors, and low-loss inductors using air-bridge. A wide variety of applications can be realized over a broad frequency range including low-noise amplifiers for consumer Direct Broadcast Satellite dish systems (Ku-band) and medium power amplifiers for automotive radar (W-band), for example.

致謝

求學的過程中，首先感謝美麗又嫻慧的老婆大人 金玉梅小姐，全力的支持，才有可能完成學業，有她堅強的後援，在精神與金錢上打點一切之下，完成學業。

特別感謝黃振華 博士，個人在任職全球聯和通訊時，給我很多的提攜與觀懷，之後在穩懋半導體開始進行本論文之實驗開發，在產品的開發與論文的撰寫過程當中，更要感謝屠德威 博士、苑成剛 博士及張維德 博士，給我許多經驗的教導，並感謝我的同事葉世偉、余家誠及黃介甫，給予實驗上的協助，在團隊合作下，一起解決許多工程上的問題，如光阻 profile 的形成，如何達成目標的線寬尺寸，並在晶片的清洗製程上進行許多研究與改善，才有可能共同完成本次的產品開發。

再以感恩的心謝謝以上諸位，及其他幫助過我的所有人，皆能以喜悅及幸福的心境，完成自己想做的事。

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Chapter 1

Introduction

1.1. The most important microwave and millimeter-wave power device application is pHEMT device. The pHEMT is also provides high speed and very low noise performance. Significant opportunities arise for GaAs MMICs in commercial applications such as digital radios for cellular backhaul (6-40 GHz), VSAT ground terminals (27-31 GHz), automotive radar (76-77GHz). And a wide variety of applications can be realized over a broad frequency range including low-noise amplifiers. Such as for consumer Direct Broadcast Satellite dish systems (Ku-band) and medium power amplifiers for automotive radar (W-band).

GaAs processing technology, designed specifically for cellular applications has benefited from significant investment in processing equipment new FABs take effort to increase wafer diameter leading to very high yielding, extremely low cost products. However, high performance millimeter wave MMICs have been based on 4” and 6” wafer diameter processes and e-beam lithography can achieve to high unit selling price, low yield and variable performance. Ideally, millimeter wave MMIC technology should leverage advances in handset area. A coat effective and manufacturable submicron gate process is developed on 6” GaAs wafer using I-line stepper for wide band commercial pHEMT MMICs.

Chapter 2

Concept and method of Gate Process Development

2.1 Current 0.25μm gate formation technology review

From 1991 [1] D. K. Atwood, developed the T-gates. TriQuint presented an optical T-gate for high power GaAs pHEMT based on dielectric film in 2002. The gate process with 0.33μm CD was defined by Canon I-line 5X stepper with a single layer of photo-resister on Dielectric film. The sub-micron gate process for high performance GaAs pHEMT devices has been widely investigated.

This study considers advantages and limitations of the Photo-resister in developing a 0.25μm gate using I-line stepper for a GaAs pHEMT power transistor. A 0.35μm resolution positive photo-resister fabricated by TOK Company was selected as the bottom layer. The top layer is negative PR of AZ NLOF-5500 type forming T-sharp gate. The inter-missing layer divides both PR layers from AZ Company of R-200 serious. The gate was shirked by an inter-missing layer (R-200) and Photo-resister Re-flow bake process. The optical gate process was found to be more cost effective and manufacturable than the E-Beam process.

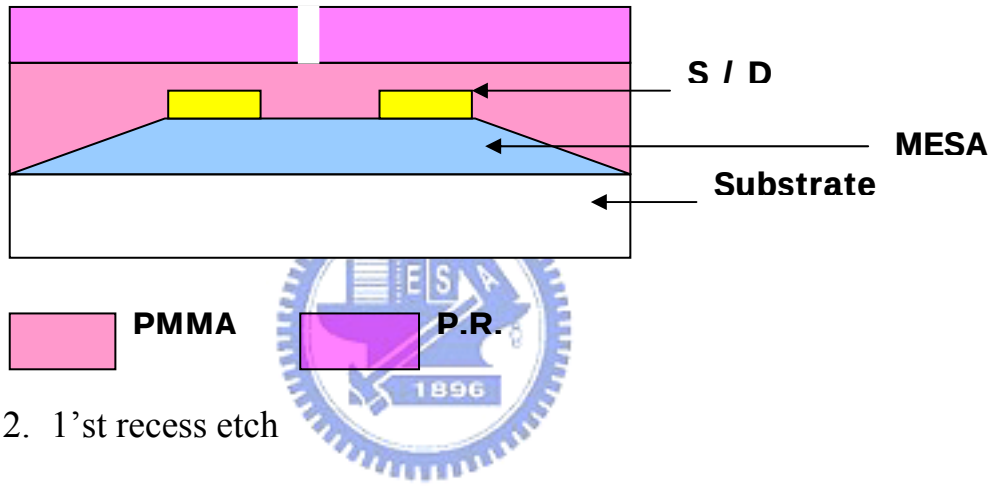
2.2 Gate lithography process technology

Several PR processes have been presented for sub-micro process as following section.

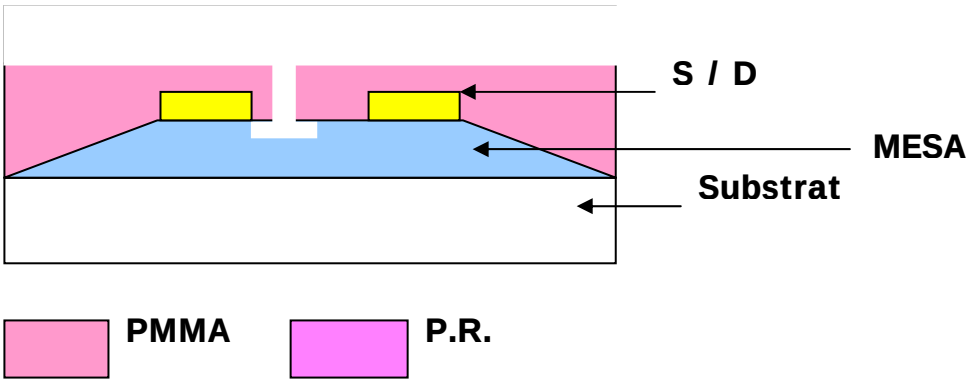
2.2.1 The PMMA with negative PR using bake and re-flow process to form the sub-micro T gate process. The process flow as Figure 2-1.

The PMMA with PR re-flow process scheme as follows:

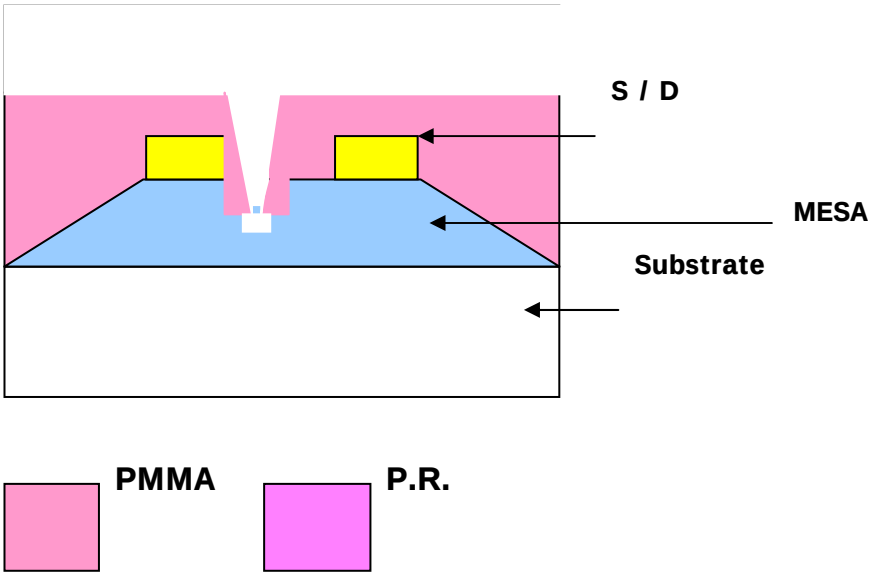
1. Coat PMMA & PR



2. 1'st recess etch



3. PMMA re-flow



4. PR coat for T-gate formatting

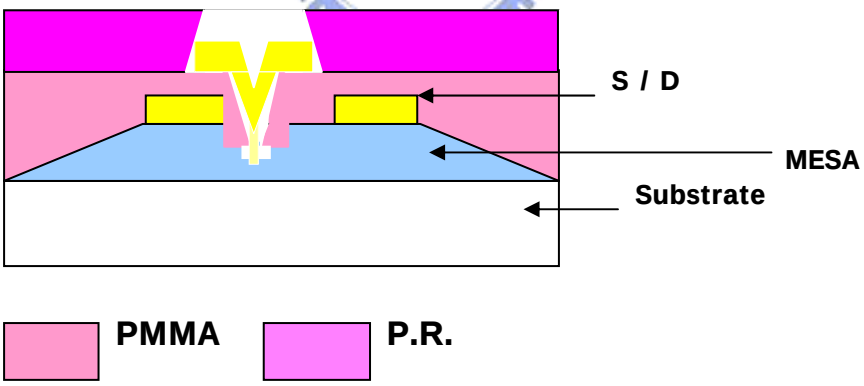


Figure 2-1 The PMMA with PR re-flow process

From: WIN Semiconductors Corp.

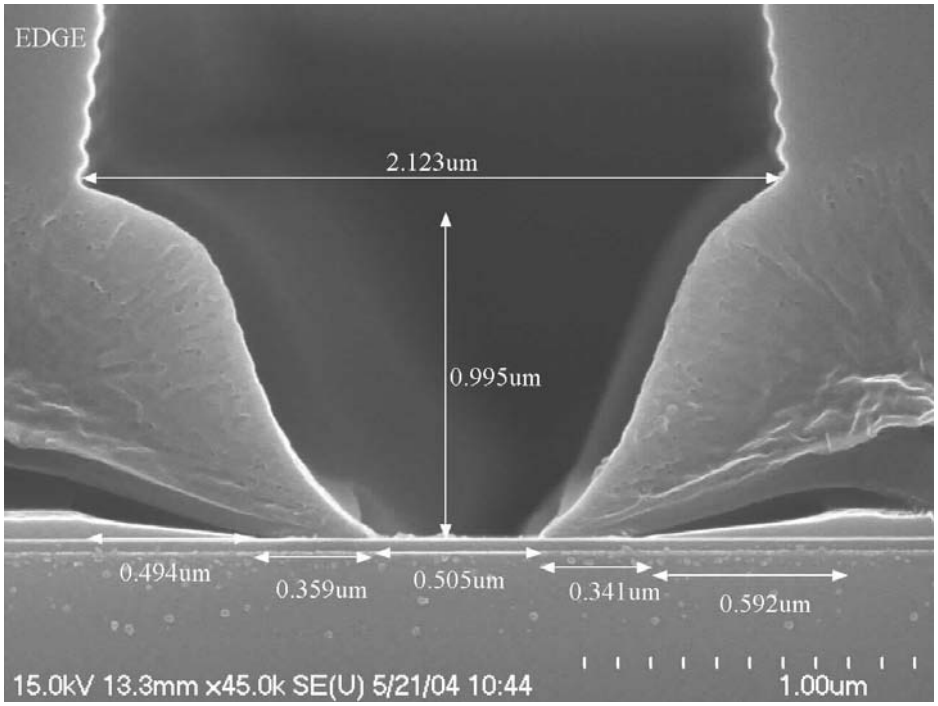


Figure 2-2 The cross-section SEM structure of lithographic photo-resister after re-flow

From: WIN Semiconductors Corp.

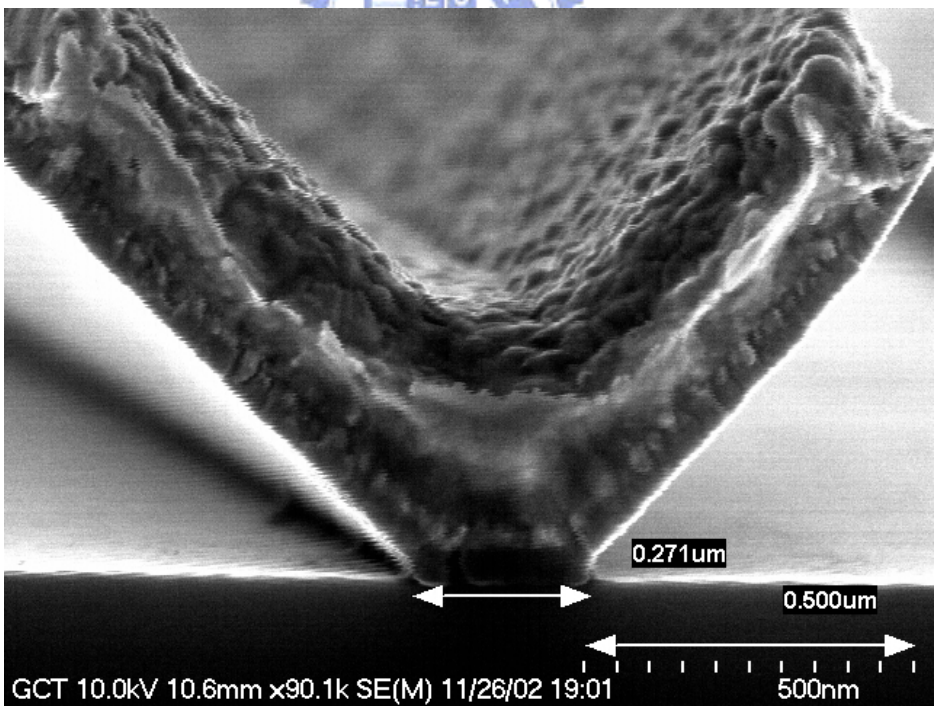


Figure 2-3 The gate cross-section SEM structure after gate lift-off.

From: WIN Semiconductors Corp.

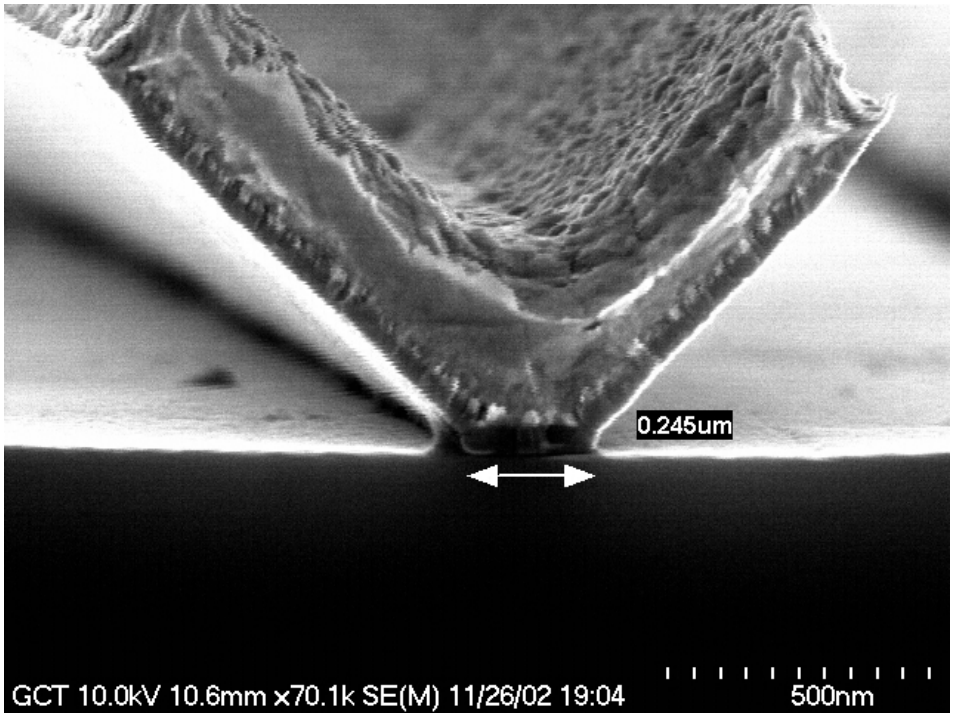


Figure 2-4 The gate cross-section SEM structure after gate lift-off.

From: WIN Semiconductors Corp.

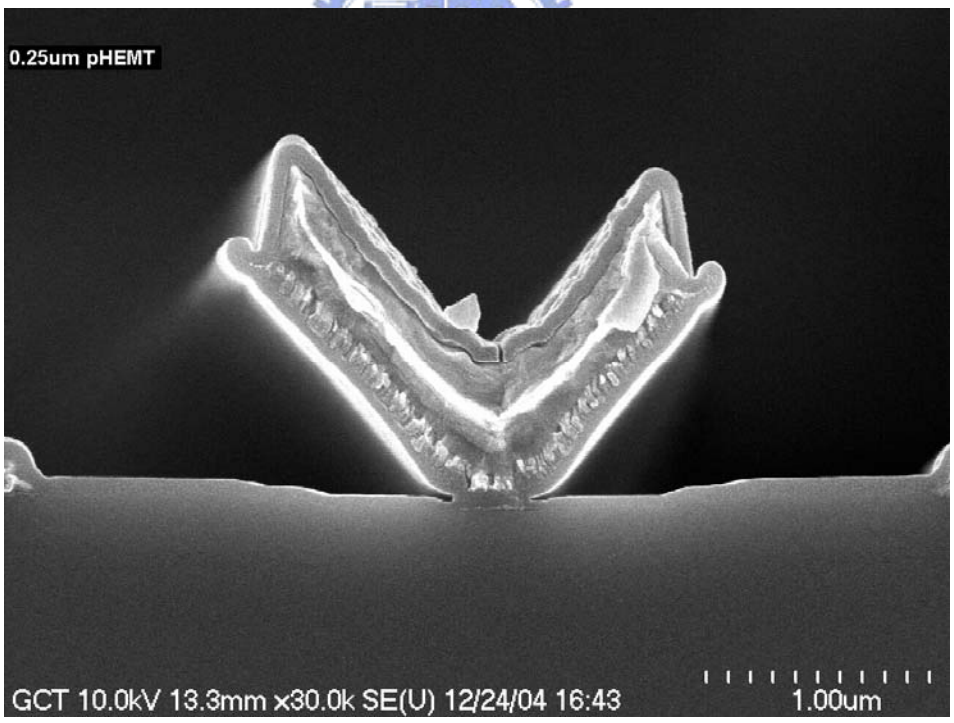


Figure 2-5 The gate cross-section SEM structure after gate lift-off.

From: WIN Semiconductors Corp.

2.2.2 The E-beam writer process

An undercut profile based on the PMMA (poly methyl methacrylate)/PMAA (poly methyl methacrylate-methacrylic acid)/PMMA (poly methyl methacrylate) mult-layer system process was obtained using E-beam lithography. However, the very low throughput and expensive equipment cost are the major disadvantages for the E-beam lithography process. The E-beam writer for submicron gate photo process in shown below as Figure 2-6:

The PMMMA/PMMB coat and E-Beam writer gate area.

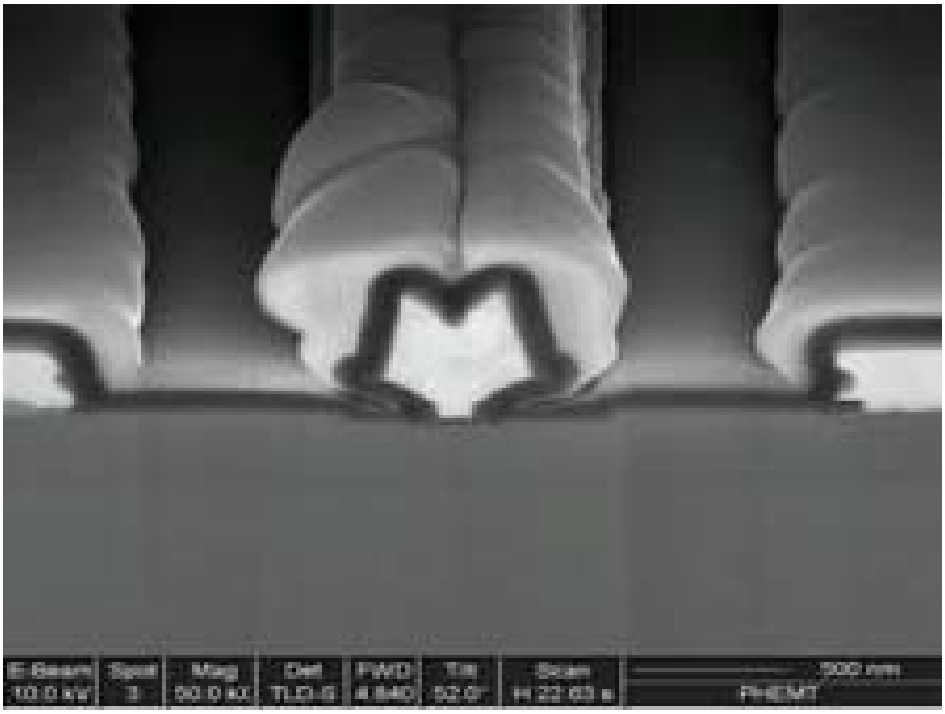


Figure 2-6 The top view of gate cross-section SEM structure after gate lift-off and SiN passivation.

From: WIN Semiconductors Corp.

2.2.3 The triple Photo-resister layers process

This study applied the triple Photo-resister layer to develop this sub-micron gate process technology. The process adopts uses sub-micro resolution positive type Photo-resister as the bottom layer. The top layer is negative PR type forming a T-sharp gate. The inter-missing layer separating the positive PR and negative PR by AZ series named r-200.

The AZ-200 is coated after positive PR develops. The R-200 involves chemical reaction and inter-mixing with positive layer by simple PR bake process. Therefore the negative PR coat and develop process can be divided by R-200 layer. The gate CD shirking efficiency is determined by inter-missing layer R-200 and Photo-resister Re-flow bake process. The detail is as the scheme of Figure 2-7.

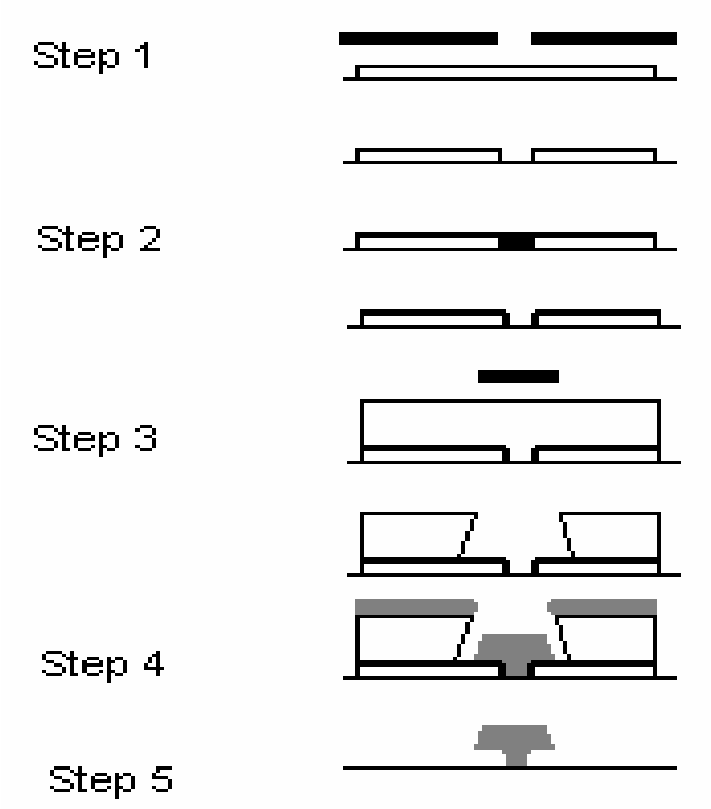


Figure 2-7 The R-200 inter-miss layer process introductions

From: WIN Semiconductors Corp.

The AZ R-200 inter-miss process reaction mechanism

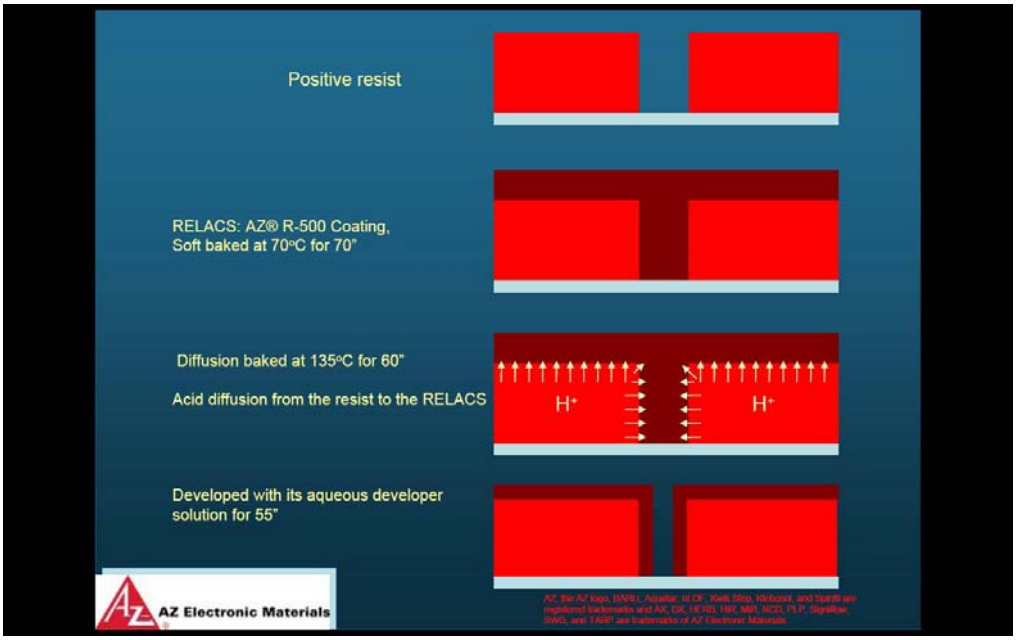


Figure 2-8 R-200 inter-miss layer reaction mechanism from AZ Company.

From: AZ Corp.

2.3 The concept of gate lift-off process

The metal lift-off processes are popular for Ohmic metal, gate metal and inter-connect metal layer formed in compound semiconductor industry. The process forms multiple layers material in with one mask and one process. Dry etch processing is not adopted so that the critical dimension different with Si semi-conductor field. The disadvantage is difficult to control the particle contamination. The yield loss will be suffered depend on gate CD size.

The lift-off process scheme as follows:

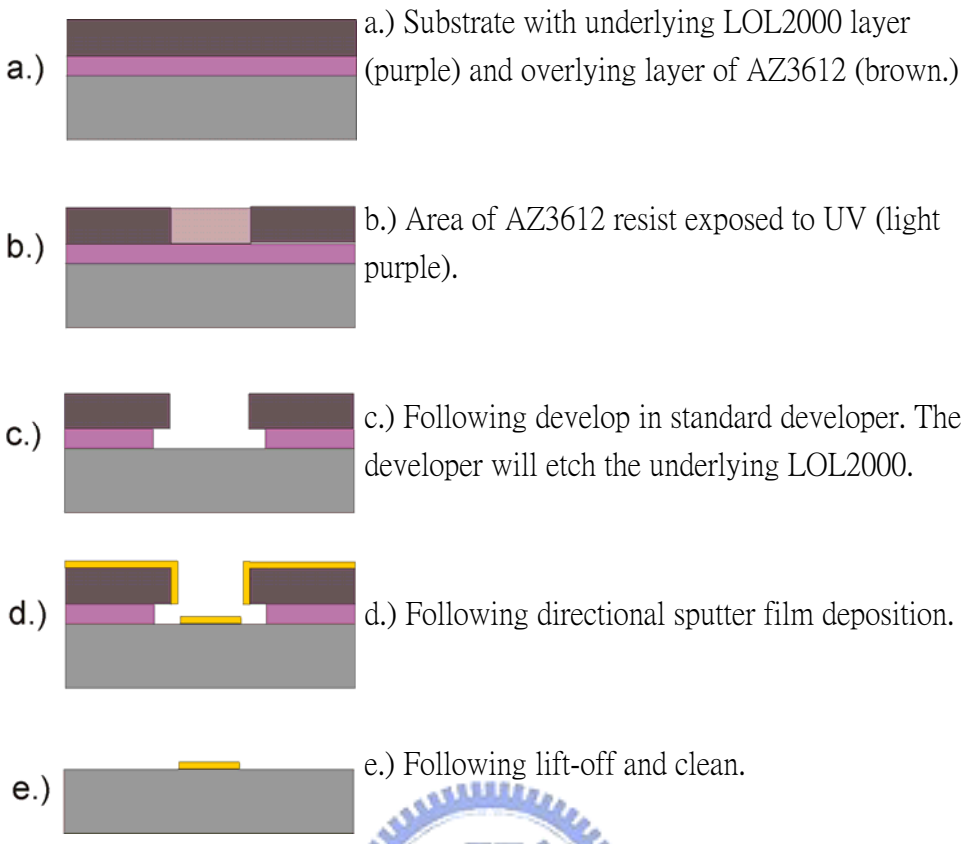


Figure 2-9 The typical lift-off process introduction

From: AZ Corp.

2.4 The Cost comparison of E-beam writer and stepper

The E-beam will get 3 times capital expansion than stepper.

Table 2-1 The coat comparison of E-beam writer and Stepper (This estimation is based on both EBL & STP are at full loading)

	Stepper		E-beam	
Schedule	Q3/'06	Q4/'06	Q3/'06	Q4/'06
WPM	2,000/M	3,000/M	2,000/M	3,000/M
Yield	77%	77%	77%	77%
Var.	2,629	2,344	3,121	2,717
Allocate	1,753	1,667	6,159	5,078
Idle	11,367	9,489	35,714	28,506
Var.+ Fix. (Allocate)	4,382	4,011	9,280	7,795
Total Cost	15,749	13,500	44,994	36,301

From: WIN Semiconductors Corp.

2.5 The Epi structure of pHEMT

Since the device is for power amplifier transistor application. The higher ΔEC is require. The epitaxial structure is used AlAs as stop layer. The active portion of the device consists of an undoped InGaAs channel sandwiched between two silicon planar doping layers, separated from the channel by un-intentionally doped AlGaAs spacer layers. The 2 deg bend diagram as the figure 2-10.

The Al concentration is about 0.24. From the bend diagram the ΔEC is about 0.8eV shown as the compound material band diagram Figyre 2-11. The epitaxial as following table:

Table 2-2 The Epi structure

Layer	Al or In content
n - GaAs	
i - AlAs	1
n - GaAs	
i - AlAs	1
n - GaAs	
n - AlGaAs	0.24
Delta Doping	
i - AlGaAs	0.24
i - InGaAs	0.15
i - AlGaAs	0.24
Delta Doping	
i - AlGaAs	0.24
12x(AlGaAs /GaAs)	0.24
i- GaAs	

From: WIN Semiconductors Corp.

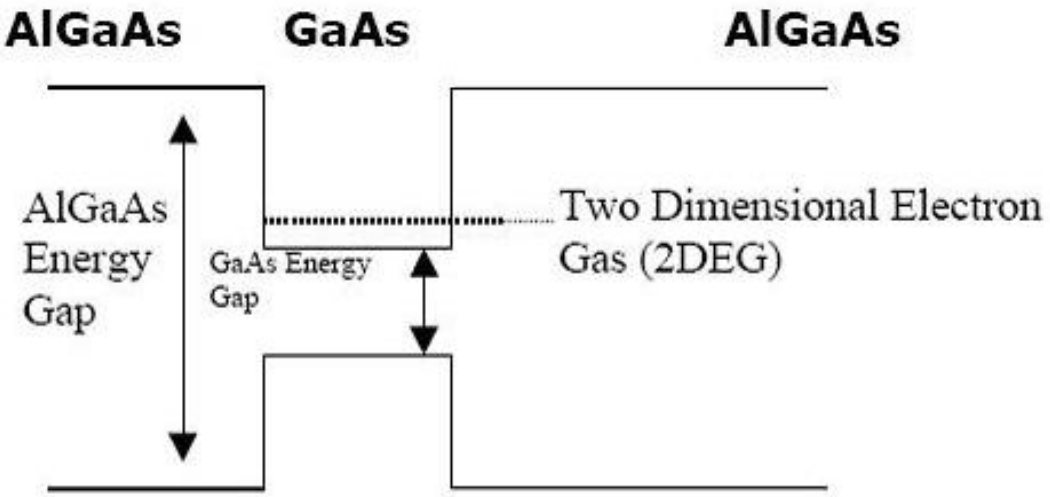


Figure 2-10 The 2DEG Quantum wall structure

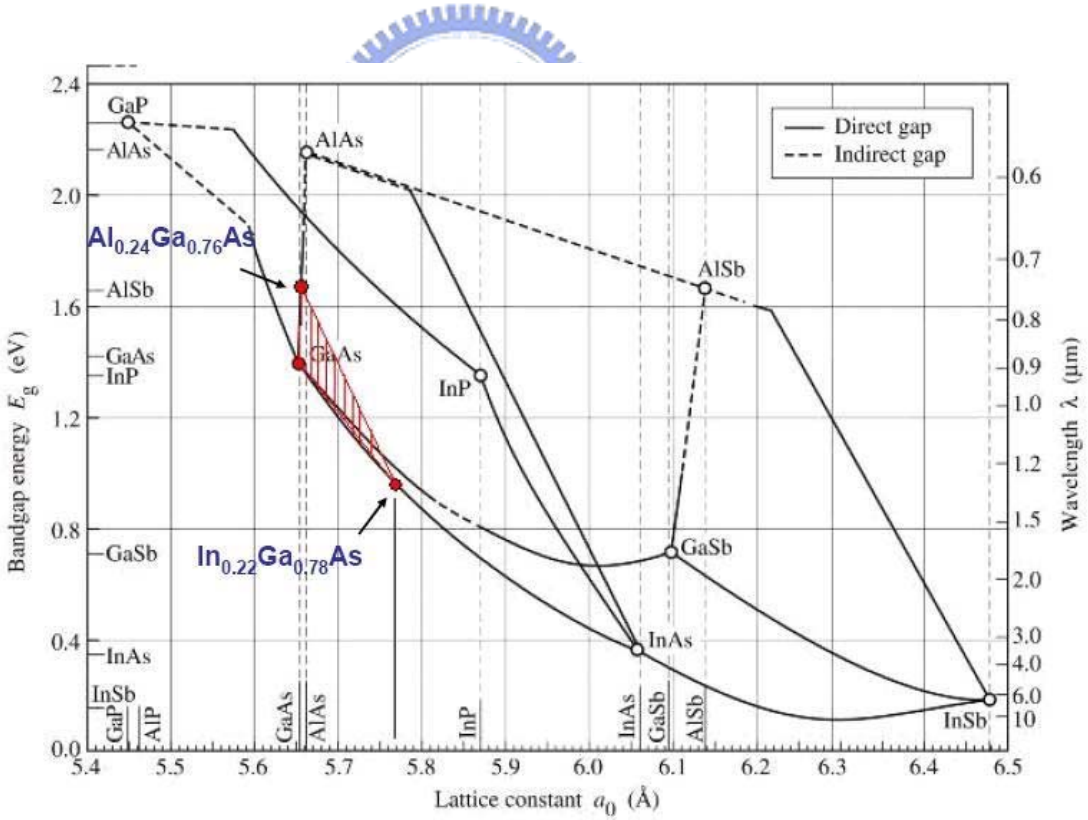


Figure 2-11 Bandgap versus lattice constant plot

2.6 Study the DC and RF characteristics

The device commercial purpose is for Ka or KU bend power amplifier. The device specification is as next table.

Table 2-3 device DC specification

Parameter Description	Unit	Value
Extrinsinic Transconductance (GM_PEAK)	mS/mm	350
IDmax @VDS=1.5 V;VGS=0.5 V	mA/mm	500
Drain current @VGS=0 V;VDS=1.5 V	mA/mm	300
Gate-Drain Breakdown Voltage @ IGD=1mA/mm	V	18
Gate Voltage @GM_PEAK	V	-0.45
Pinch-off voltage @ Ig=1 mA/mm	V	-1.2
Epi sheet resistance	ohm/sq	150
TFR @ 1 mA/mm	ohm/sq	50
Capacitor	pf/mm2	400 (MIM)
Cut-off frequency (ft) @ Vds=1.5 volt	GHz	60

From: WIN Semiconductors Corp.

Table 2-4 device circuit specification

Item	Unit	Value
Gate Length	μm	0.25
# of Frontside Mask Layer		13
# of Backside Mask Layer		2
Wafer Final Thickness	μm	100
Gate Metal Thickness	A	4800
Metal 1 Thickness	μm	1
Metal 2 Thickness	μm	4
TFR	ohm/sq	50
Capacitor (MIM)	pf/mm2	400
Interconnect Crossover		Air-Bridge
Protection Layer		SiN
Backvia	μm^2	30 x 60 (min)

From: WIN Semiconductors Corp.

Chapter 3

Theoretical Basic of pHEMT device

3.1 The DC characteristics

3.1.1 The I-V characteristics

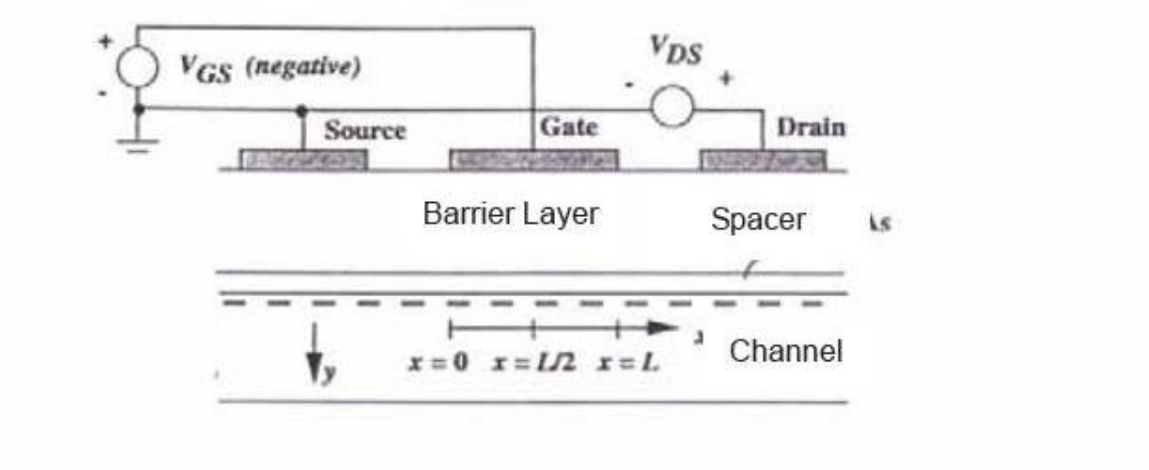


figure 3-1 The HEMT structure

From figure 3-1 the HEMT is a negative quantity in direction parallel to the channel, since electrons accumulated in the channel are negative charges. In fact, if we choose $x = L$ at the drain, this constant channel current is equal to the negative of the drain current. Hence, we have $I_D = -I_{CH}$, we find:

$$\int_0^L I_{DS}\,dx = -C'O\int_{V_{CS(o)}}^{V_{CS(L)}} C_{OX}\,\mu_n[V_{(GS)} - V_{(T)} - V_{(CS)}(\chi)]dV_{CS}(\chi) \tag{3-1}$$

To carry out the integration in Eq. (3-1), we assume temporarily that we are working in the linear region such that current saturation due to channel pinch off at the drain does not occur. The *I-V* characteristics after pinch off will be dealt with shortly. In the linear operating region, the boundary conditions are $V_{CS}(L) = V_{DS}$ and $V_{CS}(0) = 0$. Hence, Eq. (3-1) leads to:

$$I_D = \frac{W_g C'_{OX} \mu_n}{L_g}[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}]$$

(3-2)

Eq. (3-3) is plotted schematically in Fig. 3.2, with I_D shown as a function of V_{DS}. The value of V_{DS} corresponding to the attainment of $I_{D,sat}$ is denoted as $V_{DS,sat}$, the saturation voltage. The saturation voltage can be obtained by taking the derivative of I_D will respect to V_{DS} and setting the result to zero. We find that:

$$V_{DS,SAT} = V_{GS} - V_T$$

(3-3)

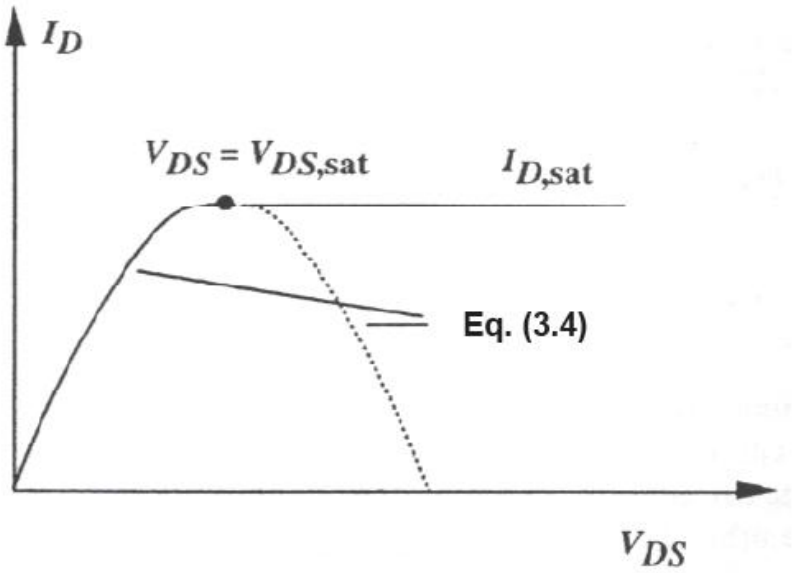


Figure 3-2 The I-V curve

When a positive potential V_{DS} is applied to the drain electrode, electron flow from source to drain, giving a current I_{DS} from drain to source. The gate is at a negative potential relative to the semiconductor beneath it, and a part of this semiconductor is depleted of carriers, restricting the current path to the "channel" between the depletion region and the high-resistivity buffer layer. The result is that the Drain-Source current I_{DS} is a function not only of the Drain-Source voltage V_{DS} but also of the gate-source voltage $V_{GS.}$ At the zero drain-source bias, the depletion layer beneath the gate is symmetric, and of a depth dependent on the gate-source potential V_{GS} (Figure 3-3). At zero gate bias, the depletion depth is that of the build-in potential of the Schottky barrier. As V_{DS} is increased from zero, the depletion layer becomes asymmetric since the potential difference between the gate and the active semiconductor beneath the gate is greater at the drain end of the gate than at the source end. The channel is more constricted at the drain end of-the gate (Figure 3-4) and so the field is higher in that region. As the drain-source voltage is increased still further. The field at the drain end of the gate approaches the value at which the electron velocity saturates. Beyond this value, which corresponds to the "Knee voltage" on the D.C. characteristics, further increases in drain-source voltage do not substantially increase the drain-source current. The length of the region of the channel over which the electrons are in velocity saturation increases (Figure 3-4c) and, as shown in Section 10.3, there is some carrier accumulation within the channel. The depletion layer edge at the drain end of the gate moves closer to the drain as the drain-source voltage increases. At a sufficient negative gate potential, the depletion layer punches through to the high-resistivity buffer layer, and the source and drain electrodes are connected only by

leakage paths within the buffer layer and substrate. These paths are located not only directly beneath the channel but also between any contacts pads formed on the buffer layer.

Figure 3-5 shows typical D.C. characteristics for a device with a total gate width of 400 μm. At low drain-source voltage V_{DS}, the channel acts as a resistor with a resistance dependent on the gate-source voltage. Above the knee voltage, the drain-source current I_{DS} is essentially independent of V_{DS}: The value of this current at zero gate-source bias is referred to as the saturated drain-source current I_{DSS}, Since the Schottky barrier has a built-in negative potential of between 0.6 and 0.8 V, the gate-source potential may be taken somewhat positive before the gate electrode takes significant forward current. The drain-source current corresponding to this condition is denoted Imax. The gate-source voltage V_{GS} necessary to reduce the drain-source current to a very small value (typically less than 1 % I_{DSS}) is the "pinch-off" voltage V_P. The mutual conductance g_m is the rate of change of drain-source current with gate-source voltage.

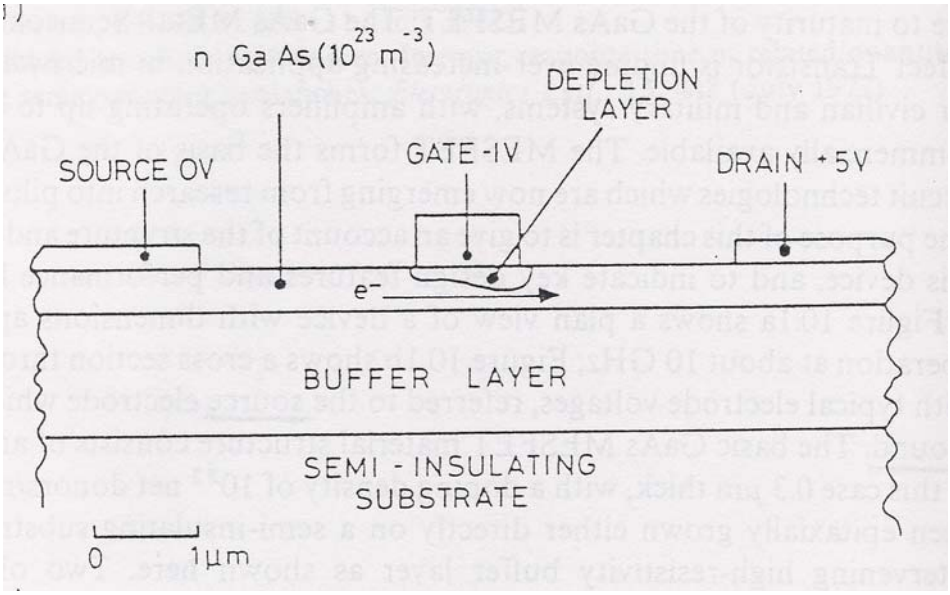


Figure 3-3 GaAs FET cross section

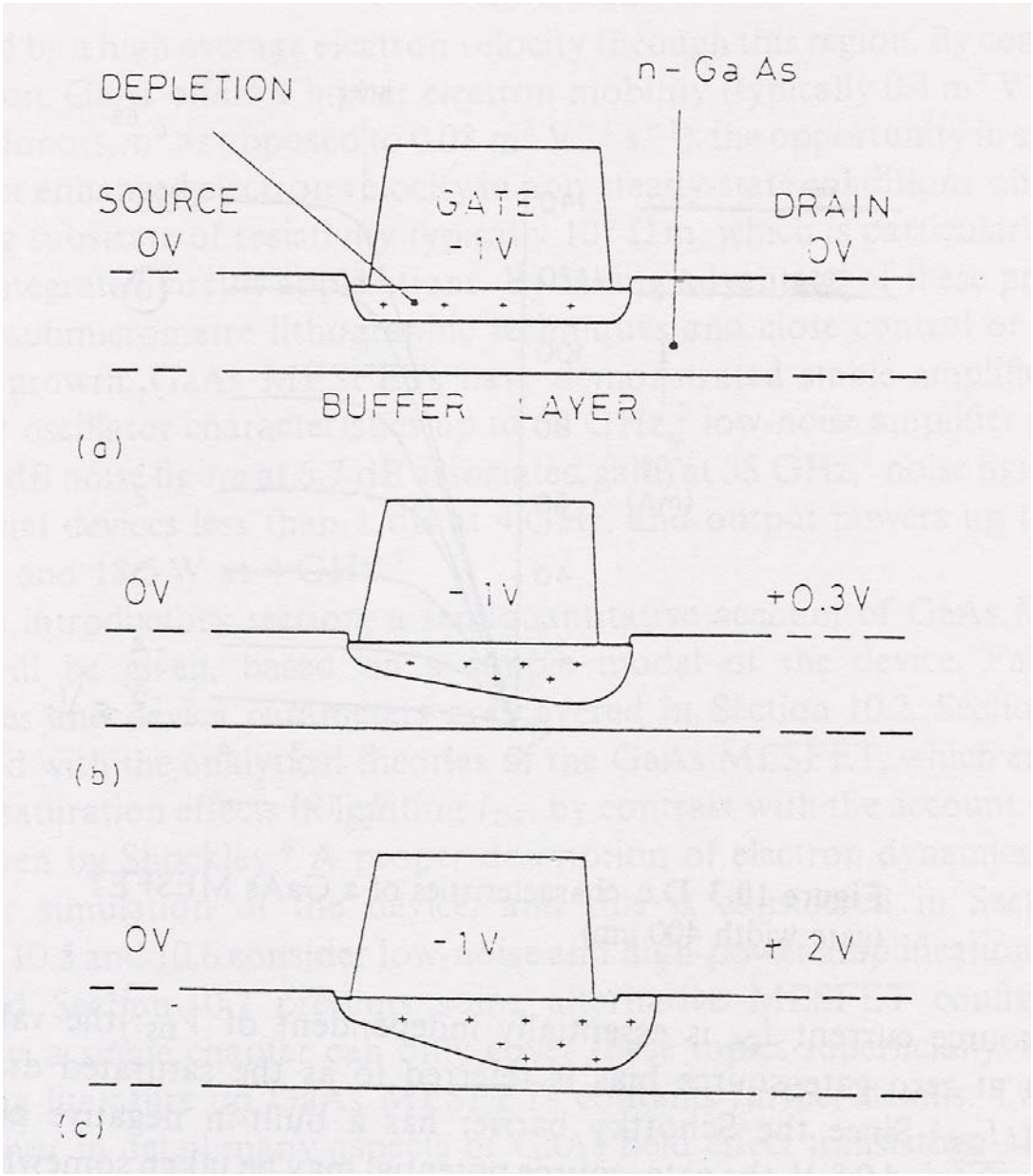


Figure 3-4 Depletion layer profiles(schematic) : (a) V_{DS}=0

(b) V_{DS}=0.3V(Below velocity saturation): (c) V_{DS}=2V(above velocity saturation).

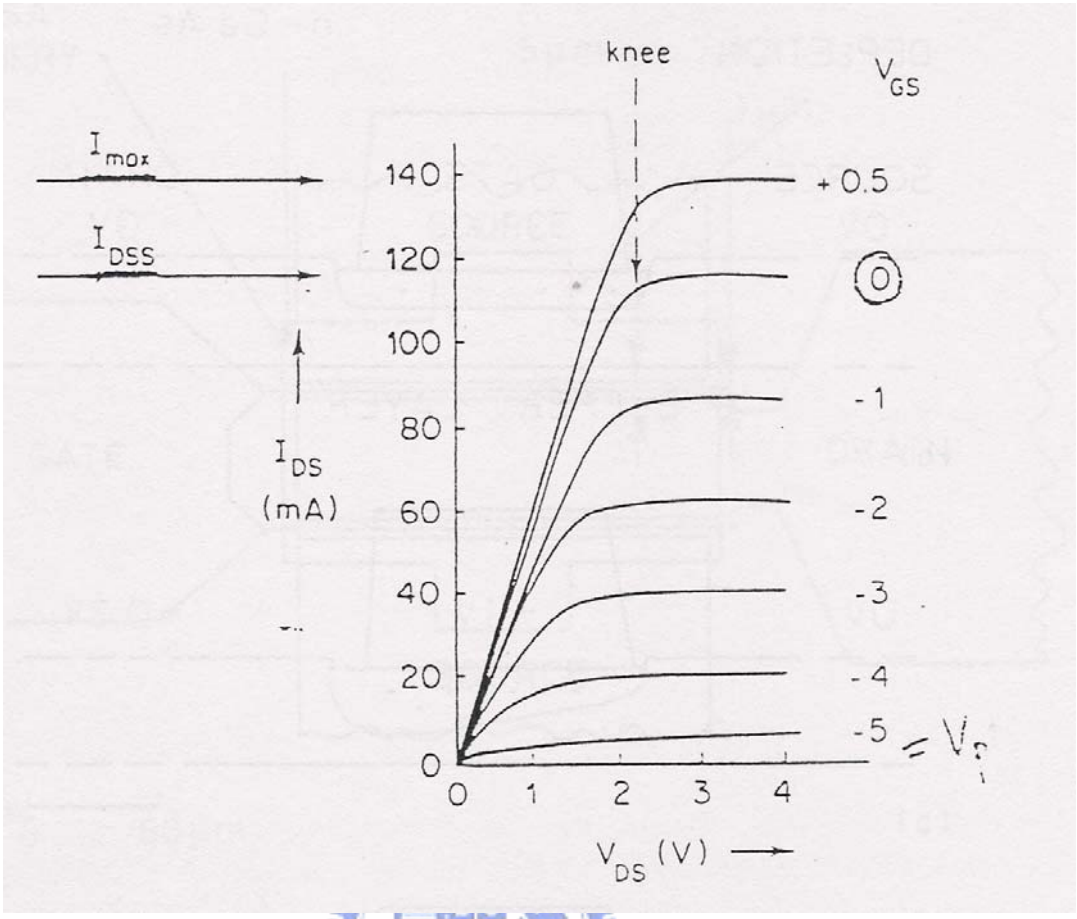


Figure 3-5 D.C. characteristics of a GaAs SFET (gate width 400 JLm)

3.1.2 Transconductance, g_m

The transconductance, g_m, is a very significant factor of determining the quality of a device. g_m is a measure of the efficiency of the channel current control, which means the amount of channel current change for a given gate voltage change. It is the ability of gate voltage on controlling drain current. To improve the efficiency (g_m), often, a well controlled recess geometry is necessary.

The transconductance of a device is defined as the slope of the IDs-Vg characteristics with the drain-source voltage held' constant. The mathematical representation of it is(3-4)

$$g_m = \frac{dI_{DS}}{dV_{GS}} = \frac{\varepsilon_2}{d_2} Z_G v_{sat} \Big|_{V_{DS}=constant} \quad (3\text{-}4)$$

Where V_{sat} sat is the electron velocity of the two dimensional electron gas (2DEG).

The transonductance of a device is easily obtained by measurement. It is one of the most important indicators of device quality for microwave and millimeter wave applications. When all other characteristics are equal, a device with higher transconductance will provide greater gains and superior high-frequency performance.

To measure gm, initial gate voltage, gate voltage step, and drain voltage at which the measurement is done must be specified first. The source-drain current is a function of gate voltage and is nonlinear; therefore, gm generally becomes less as pinch-off bias is approached. That is to say, smaller voltage step will give higher transconductance. In addition, gm is closely related to the gate length and the channel material used.

3.2 Unit Current Gain Cutoff Frequency, f_T

When defining the high frequency performance of the MHEMT, de-embedding all the conductors on the top surface of the wafer (pad, interconnect, and metal) and defining the reference plane horizontally are necessary. This helps to understand what is going on of the active region of the device and is helpful in device model development where RF quantities can be miniscule. Yet the device cannot be run without metal, so de-embedding using this method is not useful for designing circuits. Rather, de-embed up to the edge of the device, cutting the reference plane vertically through the wafer. The Device-Under-Test (DUT) then includes some device metal but not the

probe pads and interconnecting lines. Because the interconnecting lines are different with layout, they should be excluded from the DUT model.

In addition, pad parasitic can have a demonsratable effect on the device cut-off frequency f_T. In field effect transistors (FETs), f_T is defined as (3-5) :

$$f_T = \frac{g_m}{2\pi (C_{gs} + C_{gd})} \quad (3\text{-}5)$$

where g_m is the transconductance, C_{gs} the gate-source capacitance, C_{gd} the gate-drain capacitance,

, and the (Cgs + Cgd) is the total capacitance related to the Schottky gate contact.

From this relation, we could see that in order to achieve high fT, large gm and small total gate capacitance must be achieved. Small total gate capacitance is accomplished by short gate length; for millimeter-wave applications the gate length is usually smaller than 0.15μm. In this equation: (3-6)

$$f_T = \frac{g_m}{2\pi C_G} = \frac{Z_G v_{sat} \varepsilon}{w} \bullet \frac{w}{\varepsilon Z_G L_G} \bullet \frac{1}{2\pi} = \frac{v_{sat}}{2\pi L_G} \quad (3\text{-}6)$$

the L_G is the is the gate length; therefore, the shorter the gate length the higher the fT and higher the g_m.

3.3 Maximum Frequency of Oscillation, f_{max}

Another important parameter is f_{max}, which is the frequency where the power gain falls to unity. f_{max} is expressed as : (3-7)

$$f_{\max} = \frac{f_T}{2\left(\frac{R_g + R_i + R_s}{R_{ds}} + (2\pi f_T R_g C_{gd})\right)^{\frac{1}{2}}} \qquad (3\text{-}7)$$

This expression shows that to obtain useful power gain at high frequency, the f_T of a device must be large; in addition, the resistances of gate, source and drain must be small.

A typical HEMT device structure is consisted of a doped AlGaAs layer next to an undoped GaAs layer. One of the major elements that determine the mobility of electrons in GaAs is impurity. Impurity scattering will lower the mobility of electrons; therefore It is preferred that electrons flow through the undoped GaAs layer. With a doped AlGaAs layer, the electrons are supplied from this AlGaAs layer, but actual flow happens in the adjacent undoped GaAs layer. This phenomenon is possible because the band-gap discontinuity between the two layers allows the electrons to stay in GaAs layer, see Figure 2-2. Since the electrons are electro-statically constrained to stay close to the donor atoms, electrons tend to stay close to the boundary between GaAs and AlGaAs. This phenomenon is known as the two-dimensional electron gas channel.

Chapter 4

Device fabrication

4.1 Gate lithography process

4.1.1 We choose the 0.35μm resolution positive of TOK AR-80 type as the bottom layer. The second layer is negative PR of AZ NLOF-5500 type that forming T sharp gate. The inter-mixing layer separates both positive PR and negative PR by AZ R-200 serious. The process of AZ-200 is coated after positive PR develops. The R-200 will inter-mix with positive layer by simple PR bake process. So the negative PR coat process can be divided by R-200 layer. The gate CD shirking efficiency is by inter-mixing layer R-200 and Photoresist Re-flow bake process. The detail is as the scheme.

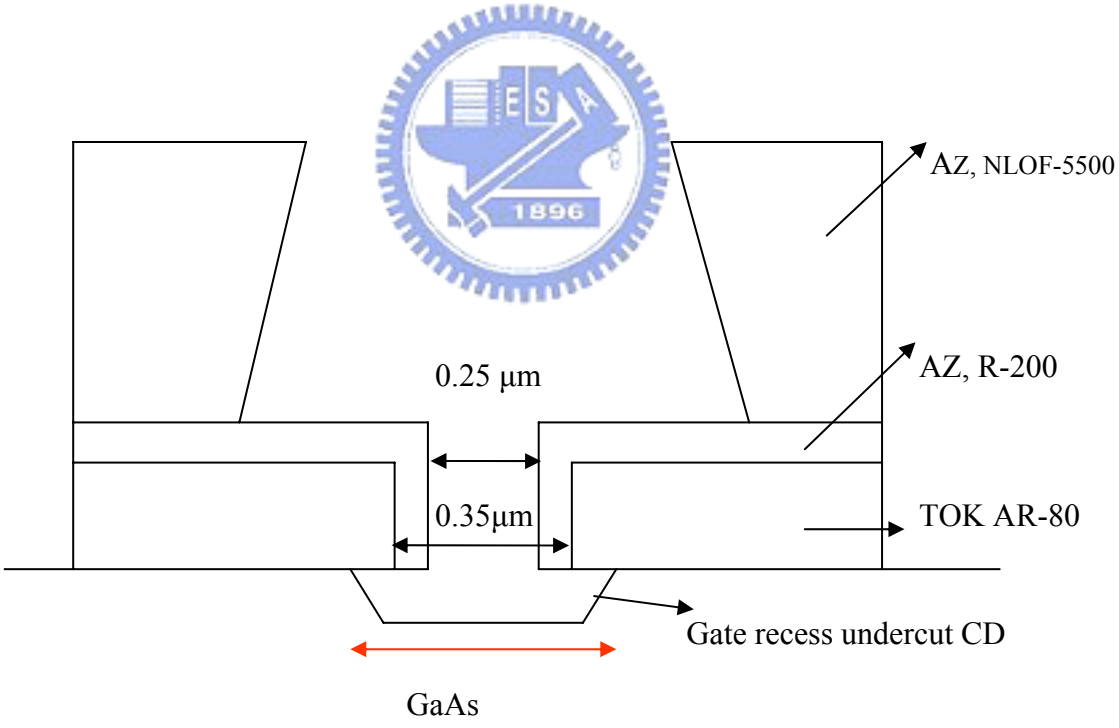


Figure 4-1 The Triple PR layer process scheme

From: WIN Semiconductors Corp.

4.1.2 The positive PR process window tuning by photolithography

Table 4-1 The positive PR thickness window check

rpm	min	max	Range	mean
1000	5581	5753	172	5605.47
1250	5063	5183	120	5083.29
1500	4693	4784	91	4714
1750	4394	4420	26	4403.18
2000	4109	4145	36	4115.76
2250	3894	3924	30	3902.65
2500	3713	3726	13	3720.12
2750	3560	3577	17	3568.71
3000	3394	3436	42	3419.76
3250	3273	3299	26	3289.71
3500	3168	3190	22	3182.35
3750	3062	3086	24	3080.59
4000	2974	2983	9	2978
4250	2883	2891	8	2886.47
4500	2811	2890	9	2816.35
4750	2754	2759	5	2757.12
5000	2677	2690	13	2685.35

From WIN Semiconductors Corp.

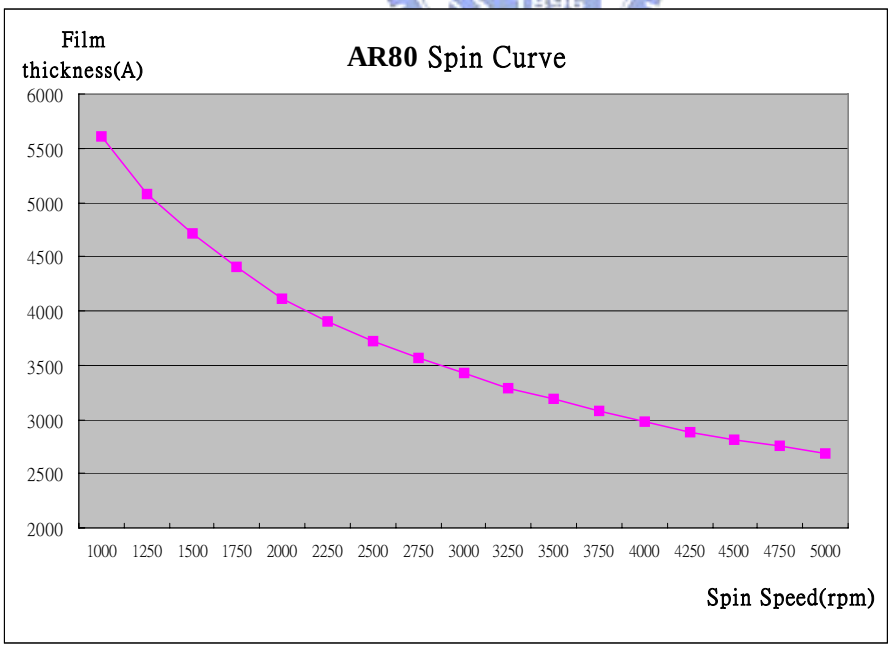


Figure 4-2 1’st positive PR coating spin curve

From: WIN Semiconductors Corp.

Table 4-2 The PR thickness V.S spin speed

Spin Speed(RPM)	Film thickness(A)	Eth (J/M^2)
1000	5605.47	1025
1250	5083.29	640
1500	4714	880
1750	4403.18	1275
2000	4115.76	780
2250	3902.65	660
2500	3720.12	720
2750	3568.71	950
3000	3419.76	1175
3250	3289.71	1150
3500	3182.35	1125
3750	3080.59	1000
4000	2978	875
4250	2886.47	780
4500	2816.35	720
4750	2757.12	720
5000	2685.35	740

From WIN Semiconductors Corp.

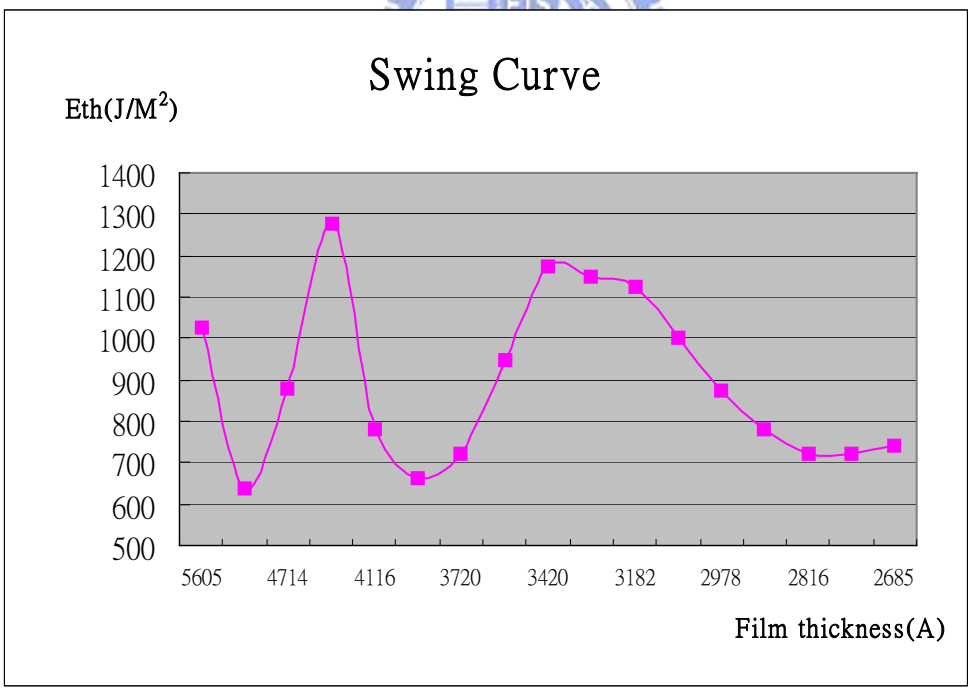


Figure 4-3 1'st positive PR coating swing curve

From: WIN Semiconductors Corp.

Table 4-3 1'st positive PR focus and dose V.S CD table

Stepper Dose

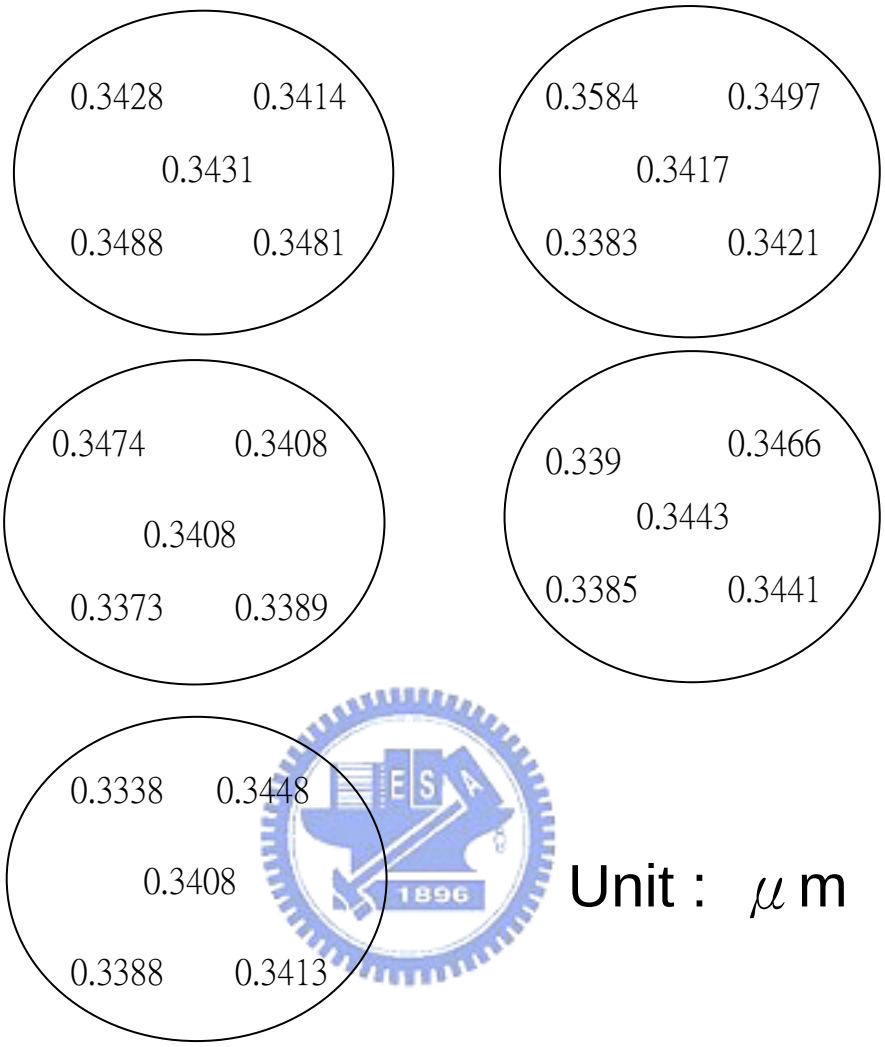
Focus	1750	1800	1850	1900	1950	2000	2050	2100	2150	2200	2250	2300	2350	2400	2450	2500	2550	2600	2650	2700
-0.5		x		x		x		x		x		x		x		x		x		x
-0.45	x		x		x		x		x		x		x		x		x		0.4444	
-0.4		0.2975		x		x		x		x		x		0.3652		x		x		0.442
-0.35	x		x		x		x		x		x		x		x		x		0.4299	
-0.3		0.3153		x		x		x		x		x		0.3426		0.4025		x		0.393
-0.25	x		x		x		x		x		x		x		0.4151		x		0.412	
-0.2		0.3084		x		x		x		0.3224		x		0.3644		0.3751		0.3851		0.3978
-0.15	x		x		x		x		x		x		0.3841		0.3937		0.4155		0.4391	
-0.1		0.2938		x		x		x		0.3512		0.3756		0.3656		0.3862		0.4154		0.4205
-0.05	x		x		x		x		0.3681		0.3409		0.378		0.3966		0.4244		0.4273	
0		0.3056		x		0.3315		0.327		0.363		0.3715		0.382		0.4071		0.4208		0.4234
0.05	x		x		0.3424		0.3487		0.373		0.3541		0.3864		0.3996		0.4236		0.4417	
0.1		0.3114		0.3173		0.3241		0.349		0.3658		0.3616		0.3921		0.4093		0.4099		0.4142
0.15	0.3323		0.3139		0.3449		0.3664		0.3713		0.3642		0.3937		0.4053		0.4134		0.4328	
0.2		0.3232		0.3277		0.3412		0.3598		0.3718		0.3525		0.399		0.4157		0.4166		0.4208
0.25	0.3301		0.3386		0.3429		0.3705		0.3747		0.3817		0.3941		0.417		0.4164		0.4193	
0.3		0.325		0.3297		0.3504		0.3545		0.3751		0.3733		0.3934		0.405		0.4098		0.4128
0.35	0.3308		0.3503		0.3543		0.3504		0.382		0.3904		0.3979		0.4166		0.4102		0.4154	
0.4		0.3294		0.3243		0.358		0.3724		0.3755		0.3641		0.3889		0.4003		0.4126		0.4162
0.45	0.3379		0.3428		0.35		0.3716		0.381		0.3894		0.4116		0.4164		0.4148		0.4192	
0.5		0.3376		0.3478		0.3677		0.3795		0.3873		0.3951		0.4061		0.4142		0.4272		0.433
0.55	0.342		0.3616		0.3753		0.3877		0.3907		0.3981		0.4087		0.425		0.4356		0.4427	
0.6		0.3262		0.3464		0.3743		0.3712		0.3849		0.3981		0.4114		0.4225		0.4371		0.4375
0.65	0.333		0.3654		0.3669		0.3902		0.3947		0.4015		0.4116		0.4278		0.4337		0.4426	
0.7		0.2587		0.3541		0.3627		0.3808		0.3823		0.3917		0.4089		0.419		0.4354		0.4366
0.75	0.3457		0.3699		0.3783		0.378		0.4043		0.4045		0.4049		0.414		x		0.4399	
0.8		0.3426		0.368		0.363		0.3728		0.389		0.4016		0.4053		0.4257		0.4293		0.4347
0.85	0.3447		0.365		0.3747		0.3839		0.396		0.4067		0.406		0.4182		x		0.4478	
0.9		0.3253		0.3538		0.3718		0.3881		0.3892		0.4079		0.4141		0.4253		0.4406		0.4332
0.95	0.3392		0.3654		0.3728		0.3773		0.4032		0.4086		0.4096		0.4286		x		0.4568	
1		0.331		0.3493		0.3673		0.3741		0.4012		0.4081		0.4177		0.4315		0.4384		0.4372
1.05	0.3343		0.3448		x		0.3791		0.3971		0.4089		0.4207		0.4374		x		0.4678	
1.1		0.2835		0.3328		0.3651		0.3753		0.3979		0.4064		0.4187		0.4006		0.4445		0.4358
1.15	0.3231		0.3336		x		0.3701		0.3878		0.4041		0.4227		0.4379		x		0.4688	
1.2		0.296		0.3383		0.3459		0.3615		0.3782		0.3967		0.4296		0.4365		0.4389		0.4587
1.25	0.3272		0.3153		x		x		0.3831		0.401		x		0.4418		x		0.4826	
1.3		0.2643		0.3132		0.3103		0.3633		0.3652		0.4027		0.4325		0.4438		0.4467		0.4615
1.35	0.2994		0.3194		x		x		0.3817		0.3969		x		0.4423		x		0.469	
1.4		0.2682		0.287		0.3169		0.365		0.3587		0.3815		0.4216		0.4222		0.433		0.4481

CD table list

From WIN Semiconductors Corp.

Table 4-4 The experience result of positive CD uniformity

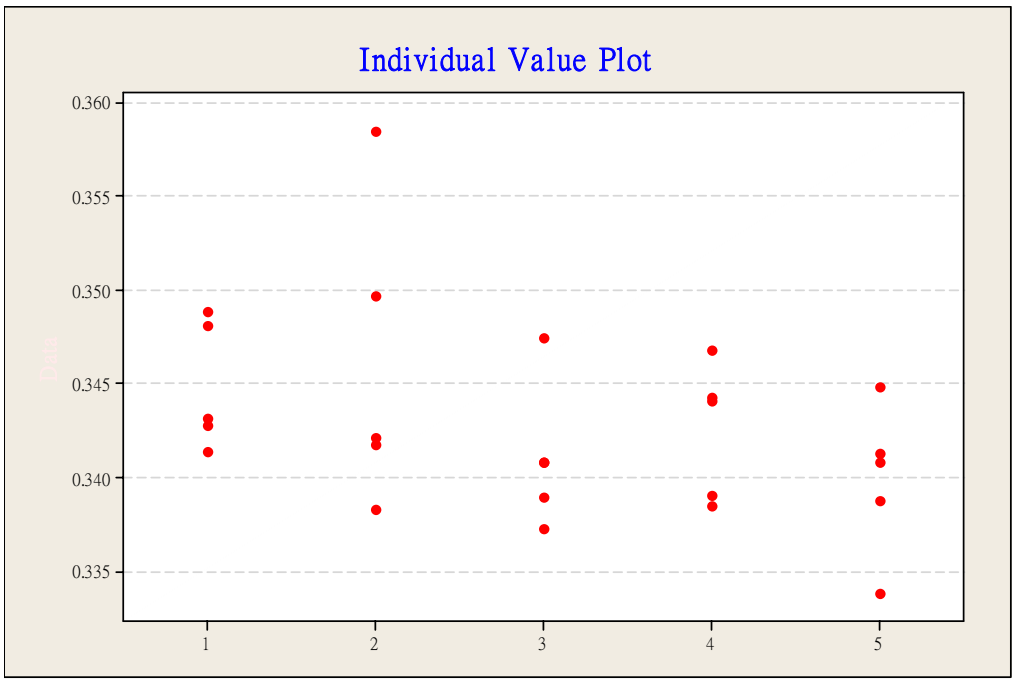
EP131 OGATE-C-F			DOSE=2300		
			FOCUS=0.35		



- Within wafer U%: 1.0-2.9% , STDEV : 0.003-0.008
- Wafer to wafer uniformity :1.6 %
- **All wafers P-value is 0.284.**

From: WIN Semiconductors Corp.

Table 4-5 The ANOVA analysis of positive CD.



One-way ANOVA

Source	DF	SS	MS	F	P
Factor	4	0.0001310	0.0000328	1.36	0.284
Error	20	0.0004826	0.0000241		
Total	24	0.0006137			

S = 0.004912 R-Sq = 21.35% R-Sq(adj) = 5.62%

Level	N	Mean	StDev	Individual 95% CIs For Mean Based on Pooled StDev
1	5	0.34484	0.00337	(----------*----------)
2	5	0.34604	0.00807	(----------*----------)
3	5	0.34104	0.00384	(----------*----------)
4	5	0.34254	0.00362	(----------*----------)
5	5	0.33990	0.00404	(----------*----------)

From: WIN Semiconductors Corp.

4.1.3 The repeatable optical gate CD and STDEV.

Table 4-6 The repeat test result of final CD uniformity

	Ogate photo CD (before descum)	
Date	Mean (um)	StDev (um)
10/3/2006	0.218	0.010
10/5/2006	0.210	0.004
	0.207	0.005
	0.211	0.003
	0.207	0.003
	0.203	0.002
	0.202	0.002
10/12/2006	0.213	0.007
11/6/2006	0.215	0.006
	0.211	0.007
11/18/2006	0.219	0.004
	0.207	0.004
11/10/2006	0.217	0.007
	0.213	0.006
	0.206	0.004
	0.205	0.007
12/1/2006	0.208	0.003
	0.201	0.004
12/4/2006	0.194	0.006
12/8/2006	0.212	0.004
	0.207	0.008
12/13/2006	0.216	0.007
	0.205	0.005
	0.204	0.012
	0.217	0.006
	0.213	0.004
12/26/2006	0.216	0.006
	0.211	0.006
	0.211	0.007
12/26/2006	0.215	0.005

- The Average gate CD is 0.21 μm and CD are between 0.194 μm to 0.217 μm .
- The process CPK is 1.13 within +_10% CD spec.

From: WIN Semiconductors Corp.

4.1.4 Gate photo Process condition fixed.

The total resist stack structure, shown in Figure 4-1, is suitable to construct the final metal gate structure. The metal deposition is directed to the center of the trenches, by the shadowing effect of the inverted top resist profiles. Thus, the bottom trenches can be completely filled with deposited metal and form the T gates, without touching the upper resist sidewalls. The inverted negative resist side wall profiles prevent the metal from filling the upper trenches and allow the lift-off process to completely strip the resist stack

4.2 Gate metal lift-off

After we fixed PH process condition the gate lift-off is the next challenge. The surface cleanliness is signification factor of RF performance and device reliability. The gate metal lift-off is base on NMP solvent first. But the NMP solvent is different to dissolve inter-missing layer with Negative PR. We tried the tape process to remove the top metal layer first then remove the all PR layers by EKC-922, ACE and IPA solvent. To control the PR bake temperature and bake time is key issue for following lift-off process. The better bake temperature and bake time are at 130C within 30 min.

4.3 The structure analysis by SEM of gate

4.3.1 The 0.25μm gate Photo-resistor SEM

4.3.1.1 The Top view of Photo-resister

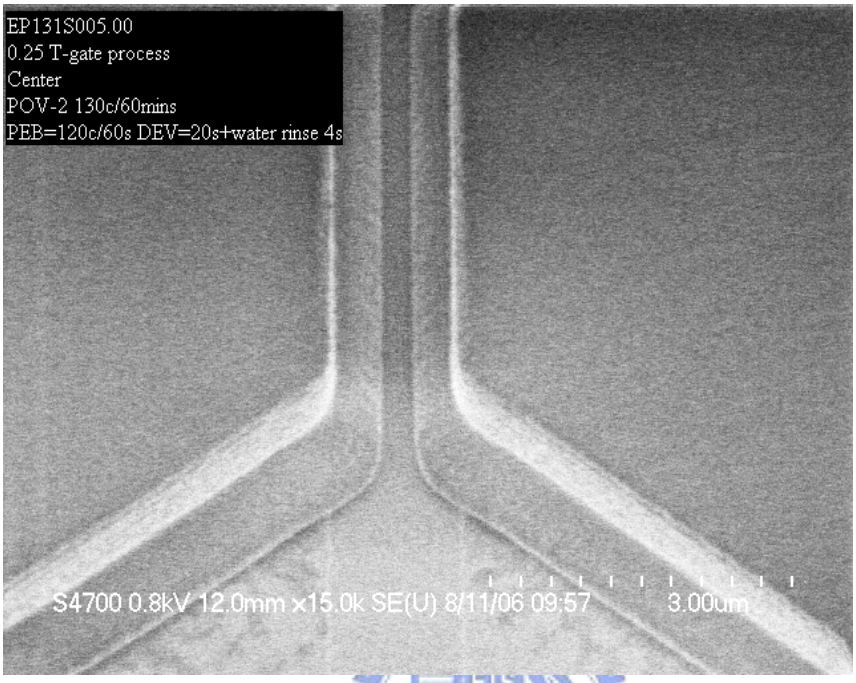


Figure 4-4 The SEM picture after PR developed

From: WIN Semiconductors Corp.

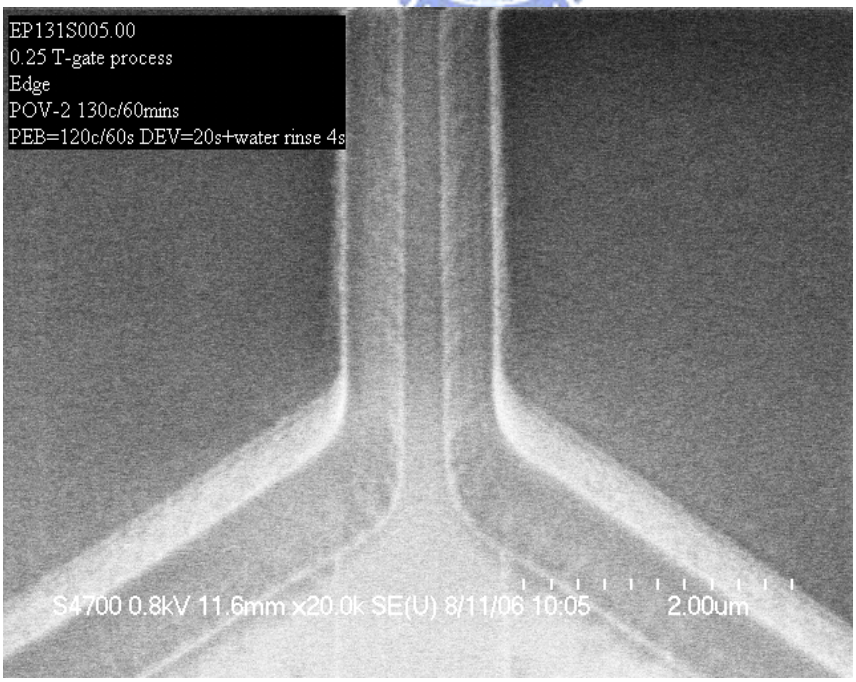


Figure 4-5 The SEM picture after PR developed

From: WIN Semiconductors Corp.

4.3.1.2 The cross-section of photo-resister

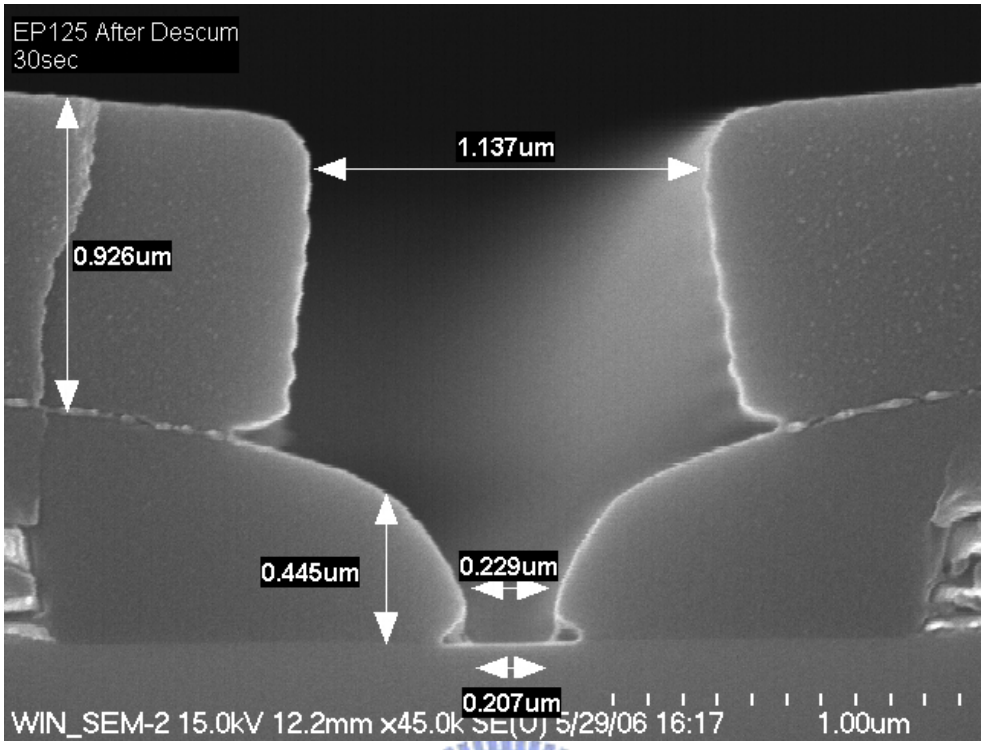


Figure 4-6 The cross-section of SEM picture after PR developed

From: WIN Semiconductors Corp.

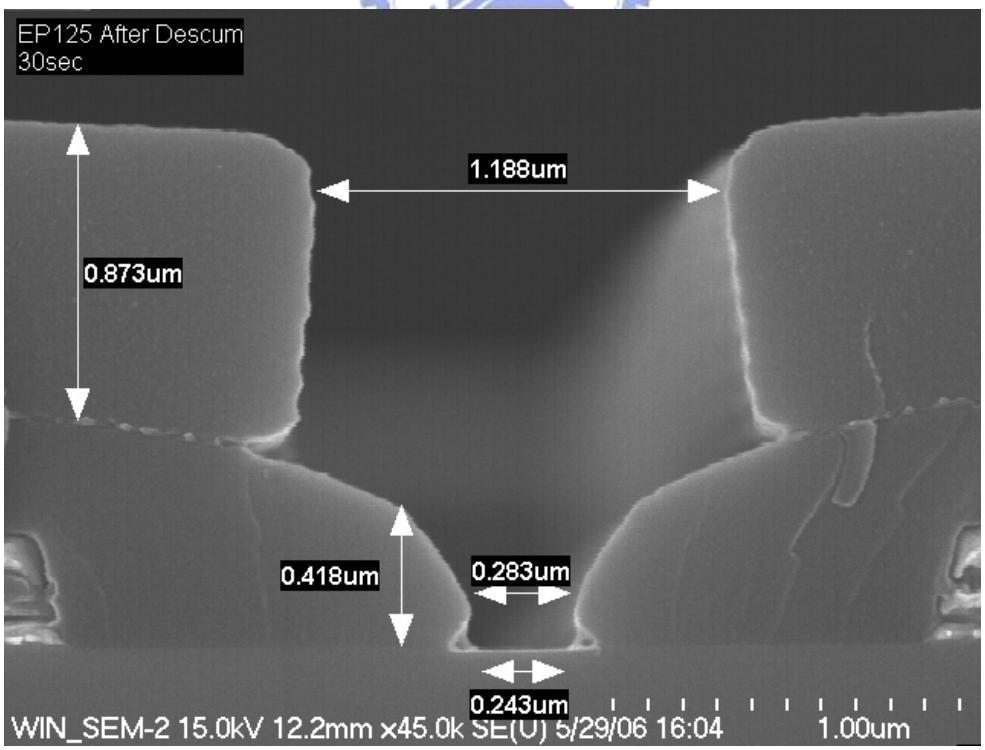


Figure 4-7 The cross-section of SEM picture after PR developed

From: WIN Semiconductors Corp.

4.3.1.3 The top cross-section of gate metal

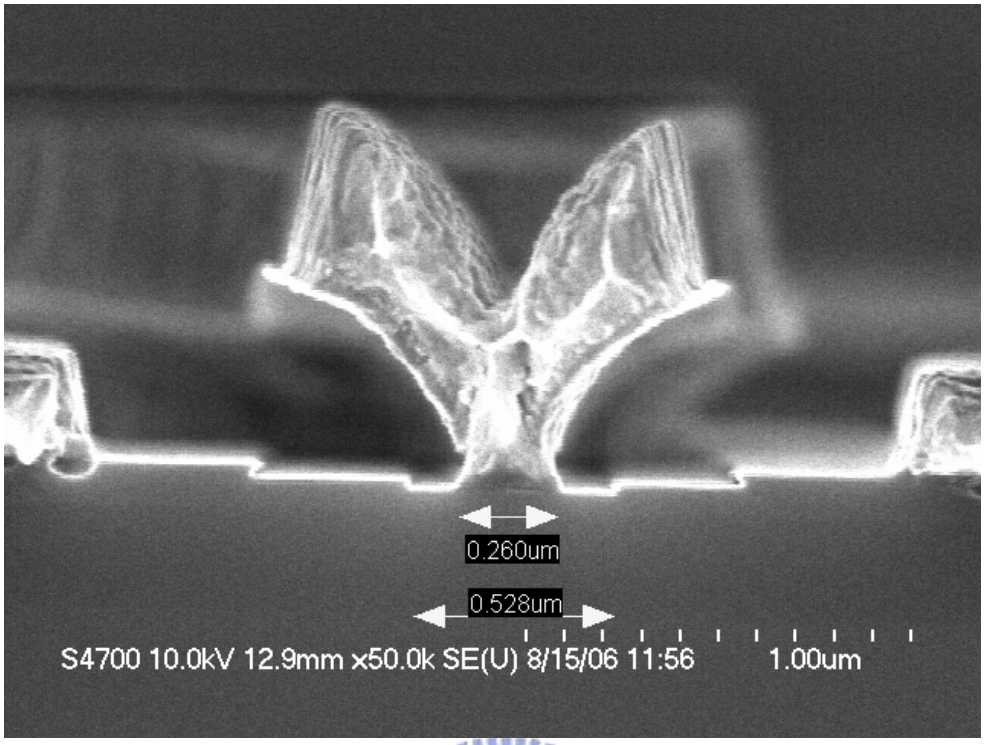


Figure 4-8 The cross-section of SEM picture after gate lift-off

From: WIN Semiconductors Corp.

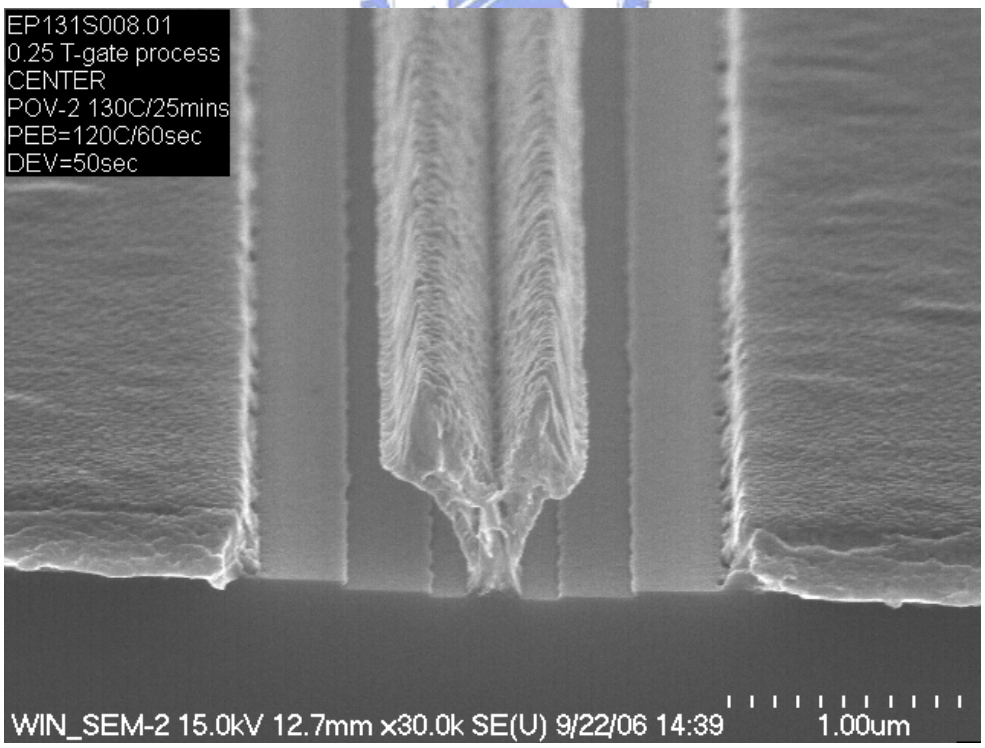


Figure 4-9 The cross-section of SEM picture after gate lift-off

From: WIN Semiconductors Corp.

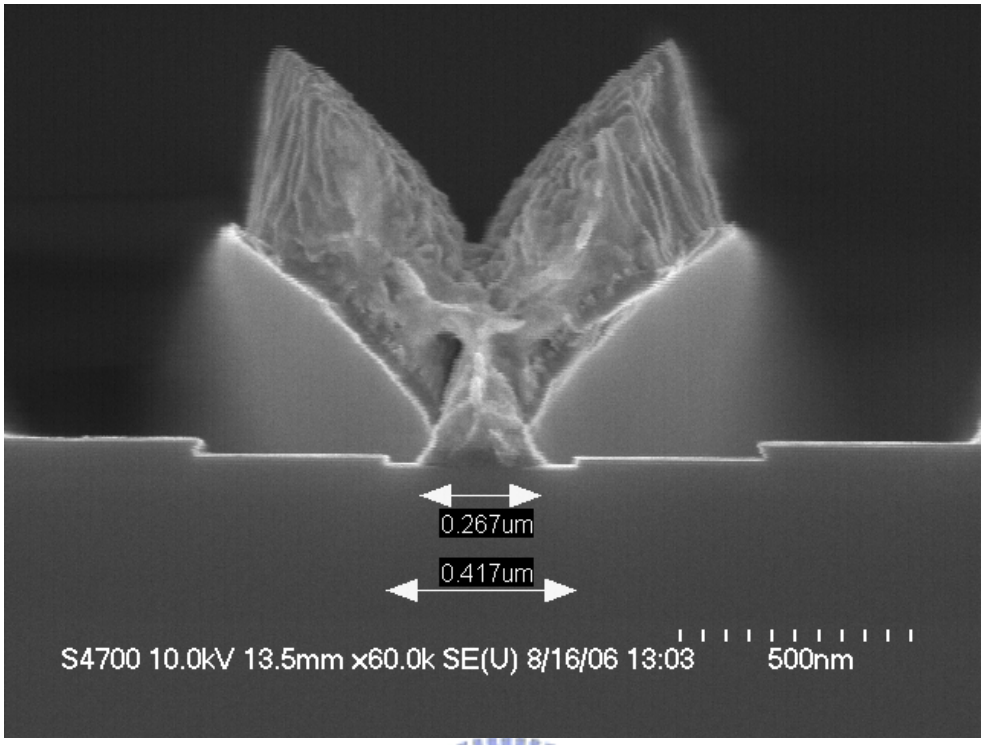


Figure 4-10 The cross-section of SEM picture after gate lift-off

From: WIN Semiconductors Corp.

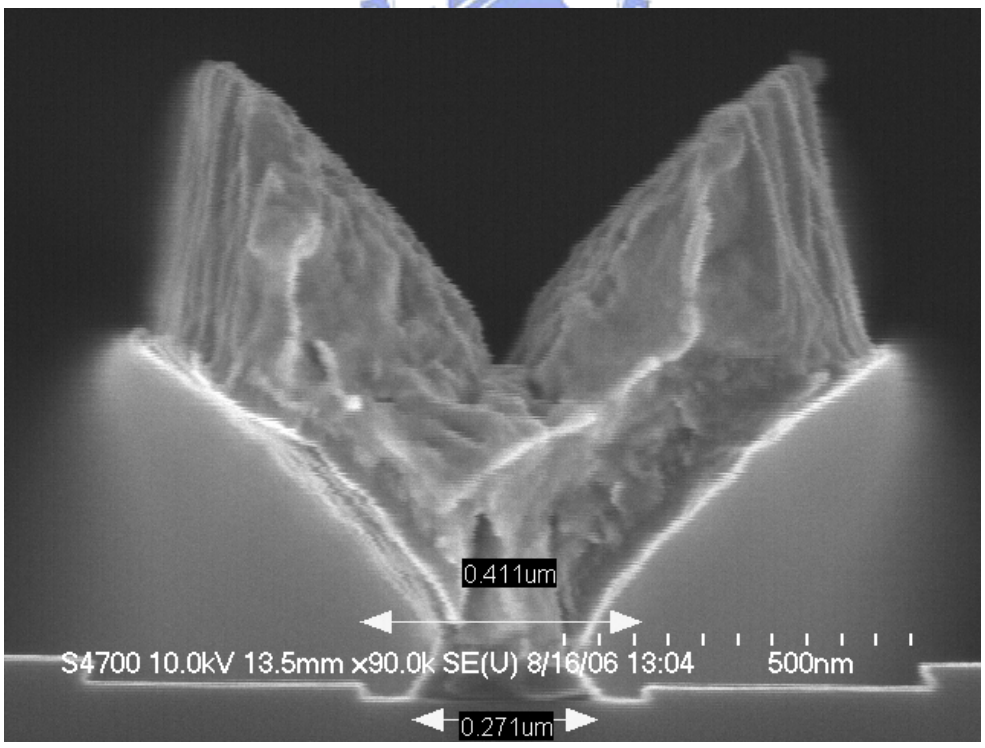


Figure 4-11 The cross-section of SEM picture after gate lift-off

From: WIN Semiconductors Corp.

4.3.1.4 The top view of wafer after whole gate process by Optical microscope

There are very clean after gate metal lift-off.

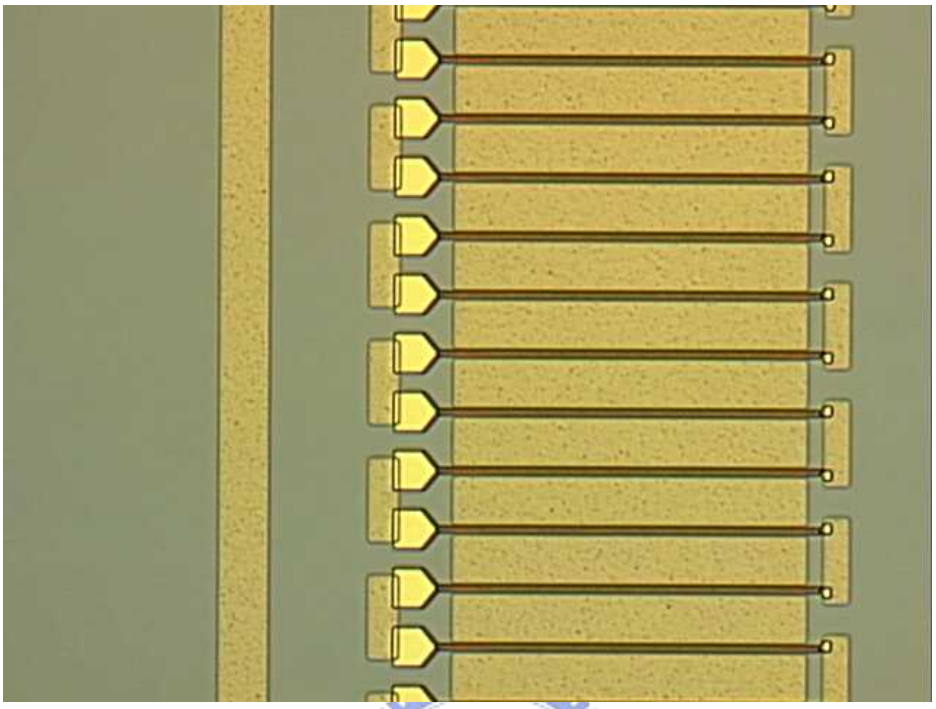


Figure 4-12 The Optical microscope picture after gate lift-off

From: WIN Semiconductors Corp.

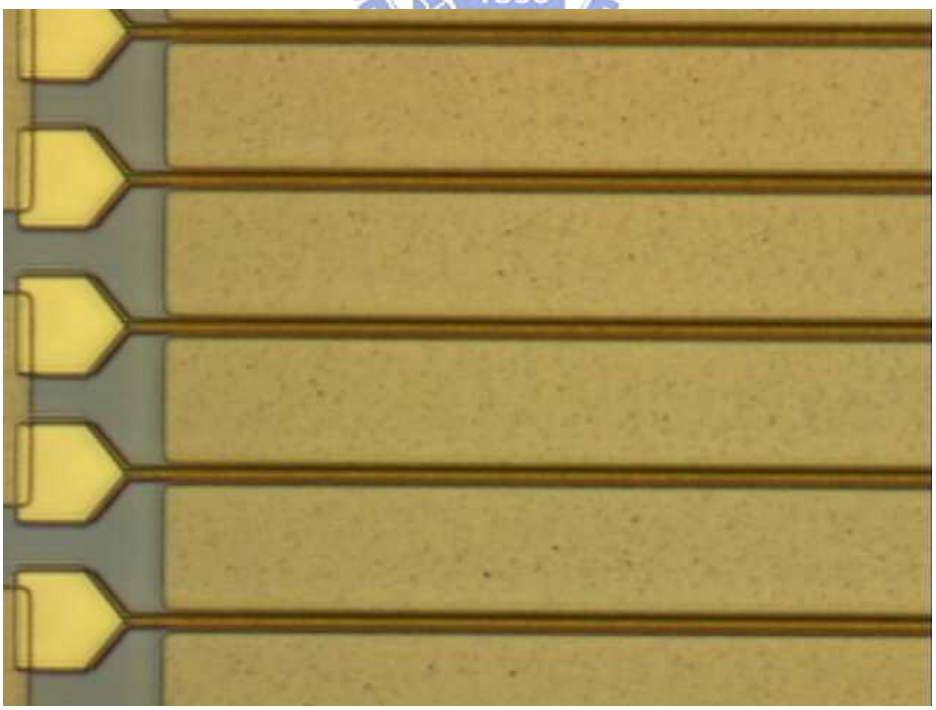


Figure 4-13 The Optical microscope picture after gate lift-off

From: WIN Semiconductors Corp.

4.3.1.5 The top view of wafer after whole gate process by SEM

There are very clean on wafer by SEM 0.8 KV energy checking.

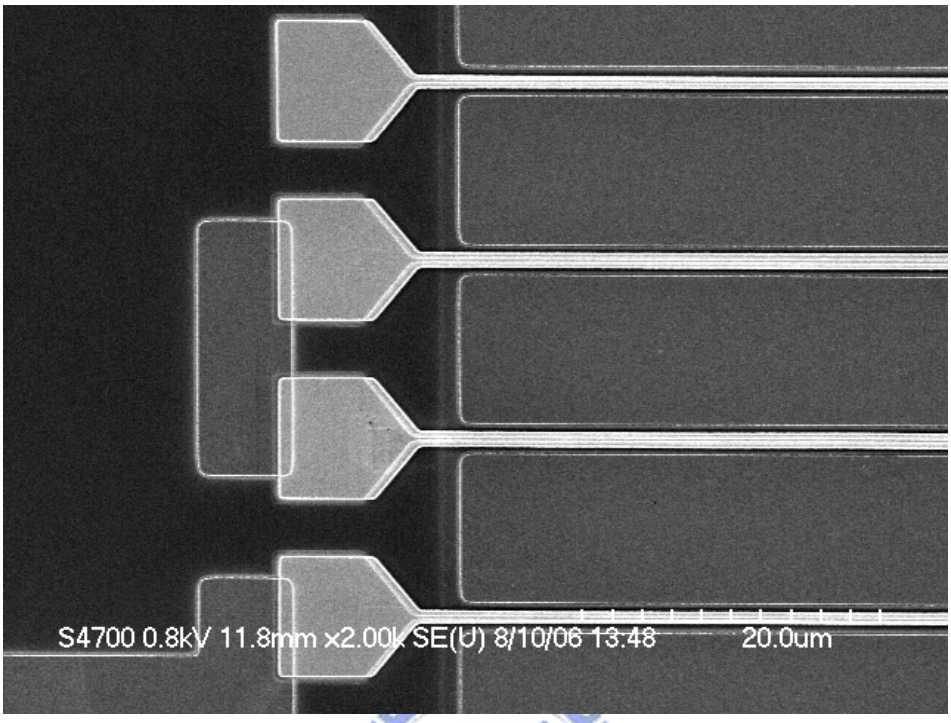


Figure 4-14 The low SEM energy surface check picture

From: WIN Semiconductors Corp.

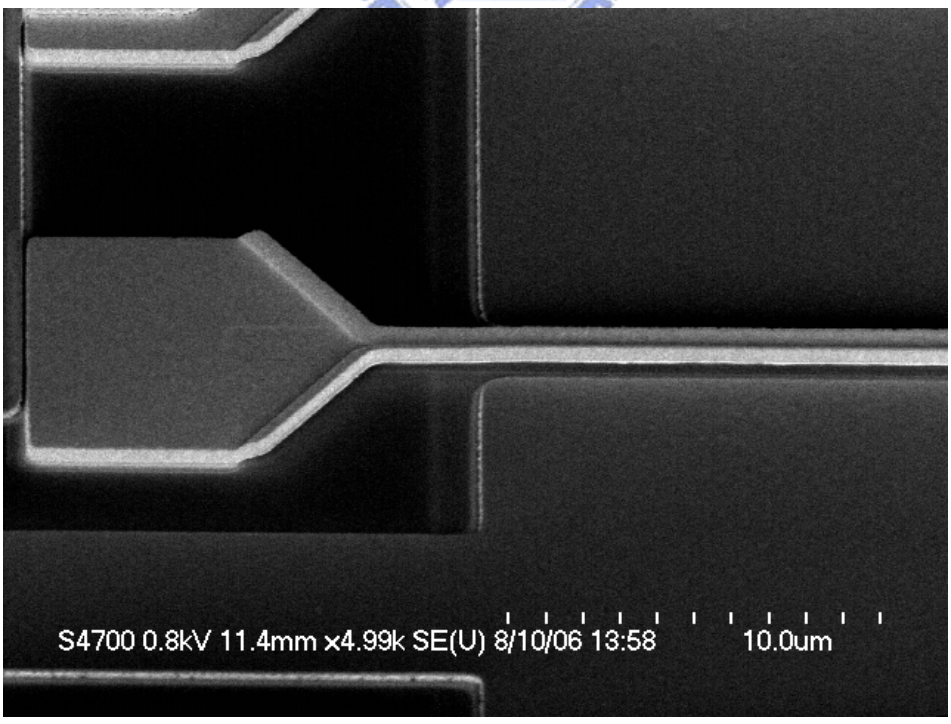


Figure 4-15 The low SEM energy surface check picture

From: WIN Semiconductors Corp.

4.4 The device process flow

The key of gate process have been overcome the next device process flow are the Mesa, Ohmic, Gate, TFR, M1, passivation SiN deposition, SiN via etch, M2 air-bridge, Protect SiN deposition. Back grading, BS through hole etch, BS planting etc.

The process flow shown as next table:

Table 4-7 The pHEMT device process layer flow.

Process Step	Cadence Name	Full Name
1	Ohmic	Ohmic Metal and Alignment Key
2	Mesa	Mesa layer
3	Wrecess	Wide Recess
4	Ogate	Optical Gate
5	DRES	T-sharp gate
6	Via1	First Nitride Deposition, Via Etch
7	TFR	Thin Film Resistor
8	Met1	First Interconnect Metal
9	Via2	Second Nitride Deposition, Via Etch
10	Air-bridge	Air-bridge
11	Met2	Second Interconnect Metal
12	Protect	Protection Nitride, Pad Opening
13	Backvia	Backside Via
14	Street	Backside Street

From: WIN Semiconductors Corp.

4.5 The result of DC and RF characteristics

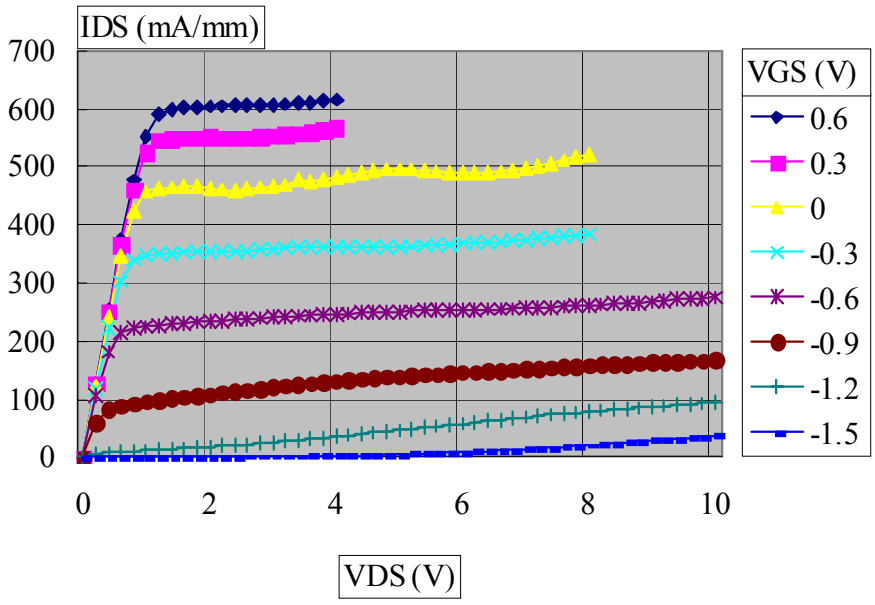
4.5.1 Ka band DC characteristics

Table 4-8 The Ka band DC characteristics.

		0.25 um CD
GM_PEAK	mS/mm	452
Idmax	mA/mm	592
IDSS	mA/mm	486
RC_TL_EP	Ohm-mm	0.12
RON	Ohms*mm	1.5
RS_TL_EP	Ohm/sq	137
VDG	V	15.4
Vto	V	-1.43
gate leakage	mA/mm	2.96E-03
ft	GHz	75.5

From: WIN Semiconductors Corp.

4.5.1.1 Ka band I-V and break down characteristics



From: WIN Semiconductors Corp.

Figure 4-16 The Ka band I-V characteristics.

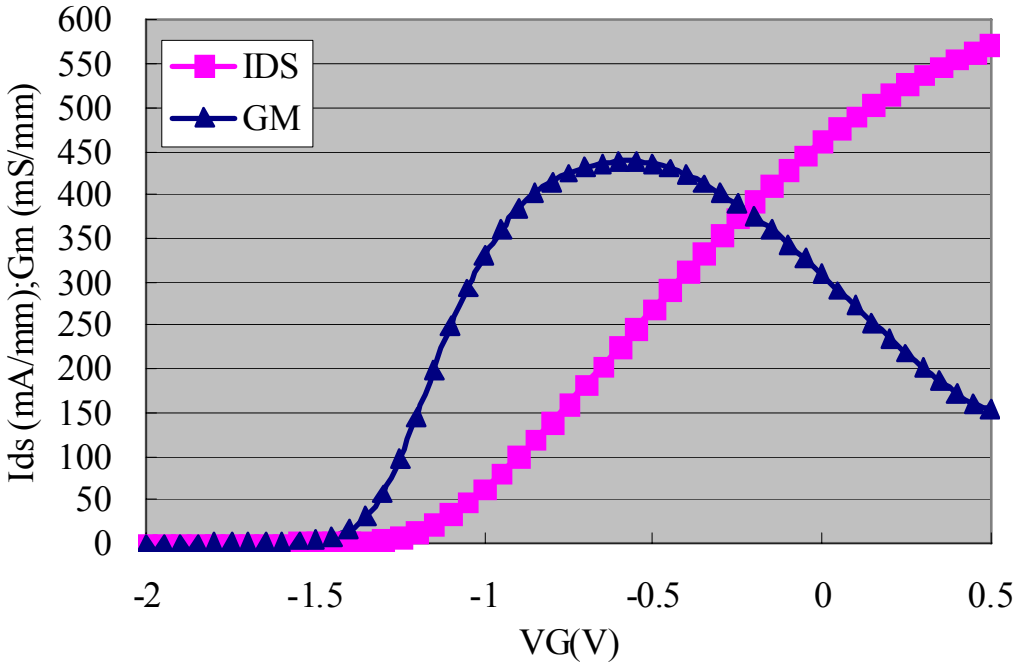


Figure 4-17 The Ka band g_m characteristics.

From: WIN Semiconductors Corp.

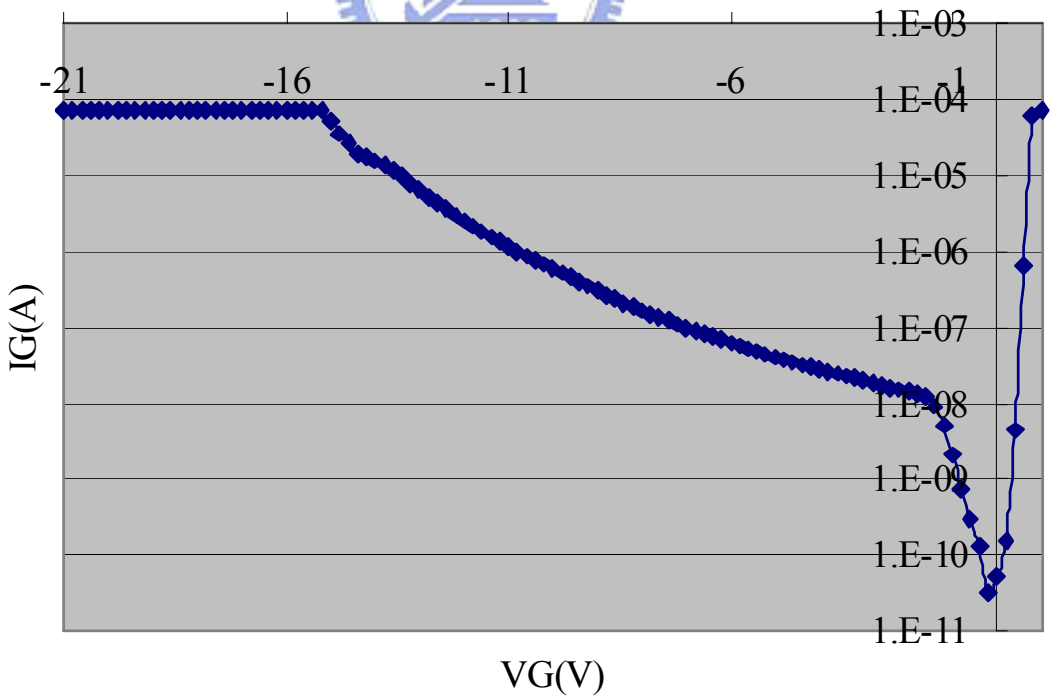


Figure 4-18 The Ka band breakdown characteristics.

From: WIN Semiconductors Corp.

4.5.2 Ku band DC characteristics

Table 4-9 The Ku band DC characteristics

		Ku band
		0.25 um CD
GM_PEAK	mS/mm	350
Idmax	mA/mm	513
IDSS	mA/mm	411
RC_TL_EP	Ohm-mm	0.09
RON	Ohms*mm	1.3
RS_TL_EP	Ohm/sq	164
VDG	V	22.8
Vto	V	-1.48
Gate leagage	mA/mm	1.2E-04
ft	GHz	52.7

From: WIN Semiconductors Corp.

4.5.2.1 Ku band I-V and break down characteristics

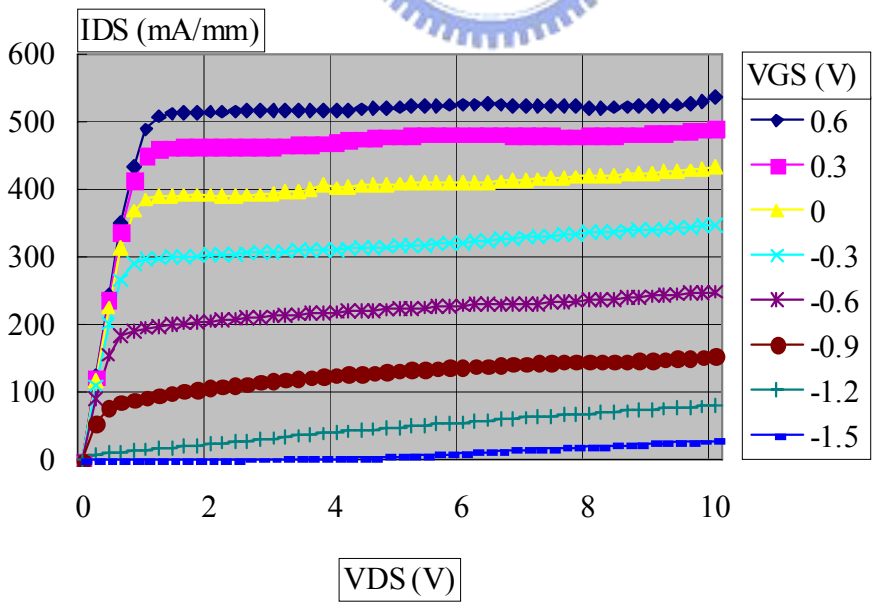


Figure 4-19 The Ku band I-V characteristics.

From: WIN Semiconductors Corp.

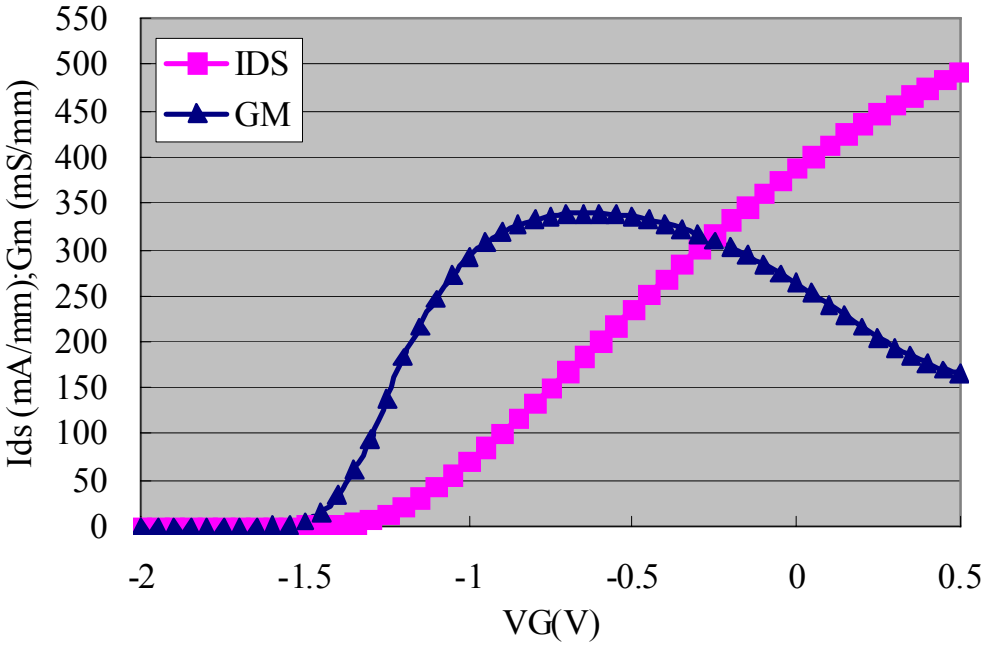


Figure 4-20 The Ku band g_m characteristics.

From: WIN Semiconductors Corp.

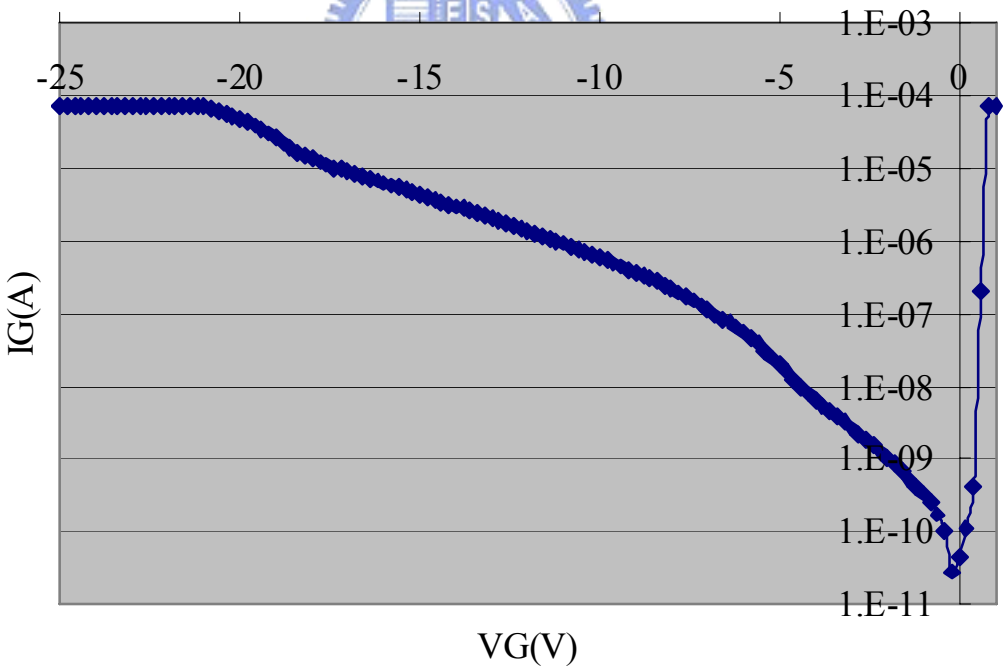


Figure 4-21 The Ku band breakdown characteristics

From: WIN Semiconductors Corp.

4.5.2.2 Compare DC parameter with 0.15μm gate CD pHEMT

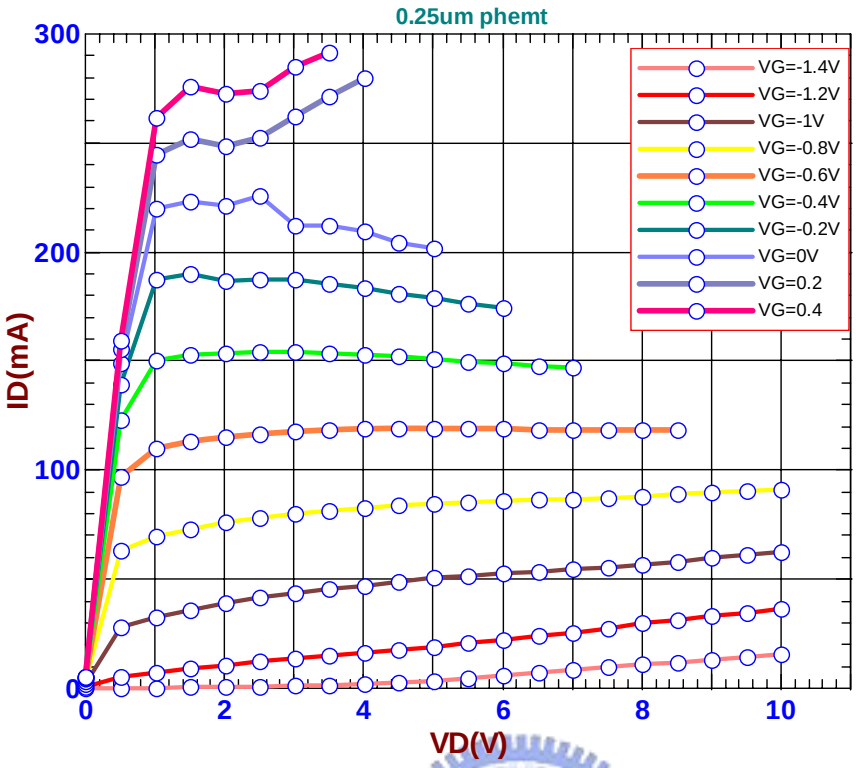


Figure 4-22 The 0.25μm pHEMT characteristics

From: WIN Semiconductors Corp.

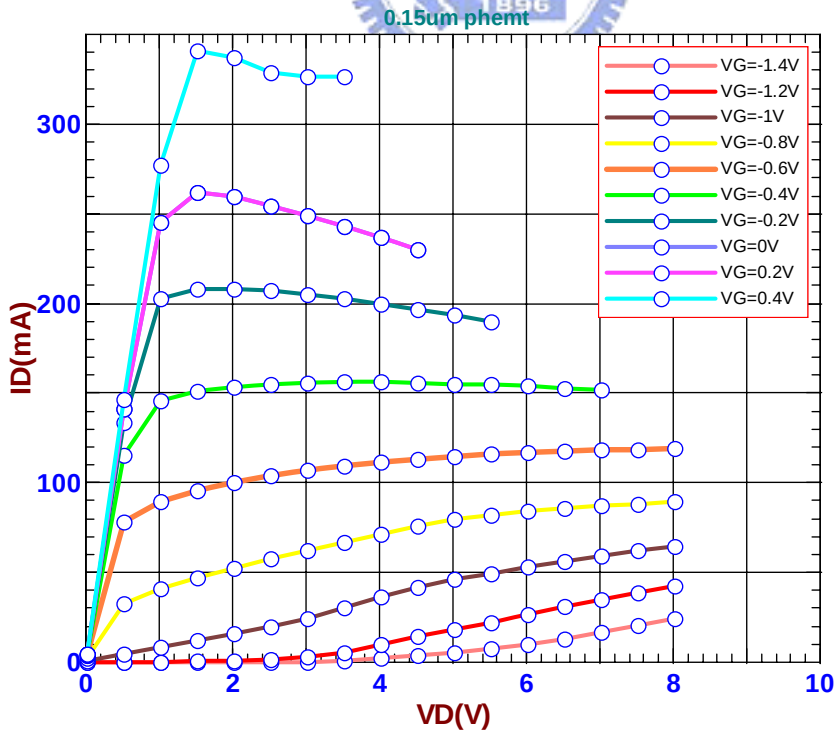


Figure 4-23 The 0.15μm pHEMT characteristics

From: WIN Semiconductors Corp.

4.5.3 The device PCM analysis

4.5.3.1 The PCM check item are as follows:

Table 4-10 The PCM yield list

Slot No	PARAM_ID	TEST_ PTS	Valid_ PTS	Inspec _PTS	Mean	STDEV	MIN	MAX	Yield %
1	GM_PEAK	25	25	25	430.37	18.93	372.03	457.03	100
2	GM_PEAK	25	25	25	484.41	26.51	423.83	521.53	100
1	IDSS	25	25	25	474.47	15.76	420.49	491.82	100
2	IDSS	25	25	25	500	13.56	471.67	526.47	100
1	Idmax	25	25	25	583.58	12.03	557.45	597.66	100
2	Idmax	25	25	25	610.76	12.47	580.21	630.45	100
1	akage current	25	25	25	0.2554	0.9583	8.82E-05	4.49	92
2	akage current	25	25	25	5.82E-04	1.24E-04	4.09E-04	7.81E-04	100
1	RON	25	25	25	1.47	0.1505	1.3	1.89	100
2	RON	25	25	25	1.16	0.1382	0.9546	1.45	100
1	breakdown	25	25	25	14.56	0.9341	11.25	15.55	100
2	breakdown	25	25	25	14.32	0.2512	13.7	14.7	100
1	rn on Voltage	25	25	25	4.00E+10	1.38E+11	-1.50	5.00E+11	92
2	rn on Voltage	25	25	25	-1.35	0.0408	-1.40	-1.28	100

There is gate leakage and turn on voltage yield loss caused by gate damage during gate metal lift-off process.

From: WIN Semiconductors Corp.

4.5.4 RF characteristics

4.5.4.1 Cutoff frequency and maximum frequency

Table 4-11 The F_T characteristics

	0.25 μm gate pHEMT	
	Ft (GHz)	Fmax (GHz)
VDS=1.5V, VGS=GM_peak	58.97 VGS=-0.45V	146.82 VGS=-0.45V
VDS=3V, VGS=GM_peak	48.34 VGS=-0.45V	133.09 VGS=-0.45V
VDS=5V, VGS=GM_peak	42.96 VGS=-0.45V	120.39 VGS=-0.45V
VDS=7V, VGS=GM_peak	38.93 VGS=-0.45V	113.17 VGS=-0.45V

From: WIN Semiconductors Corp.

4.5.4.2 Power characteristics Current gain and efficiency

4.5.4.2.1 The Ku band power performance at 10 GHz

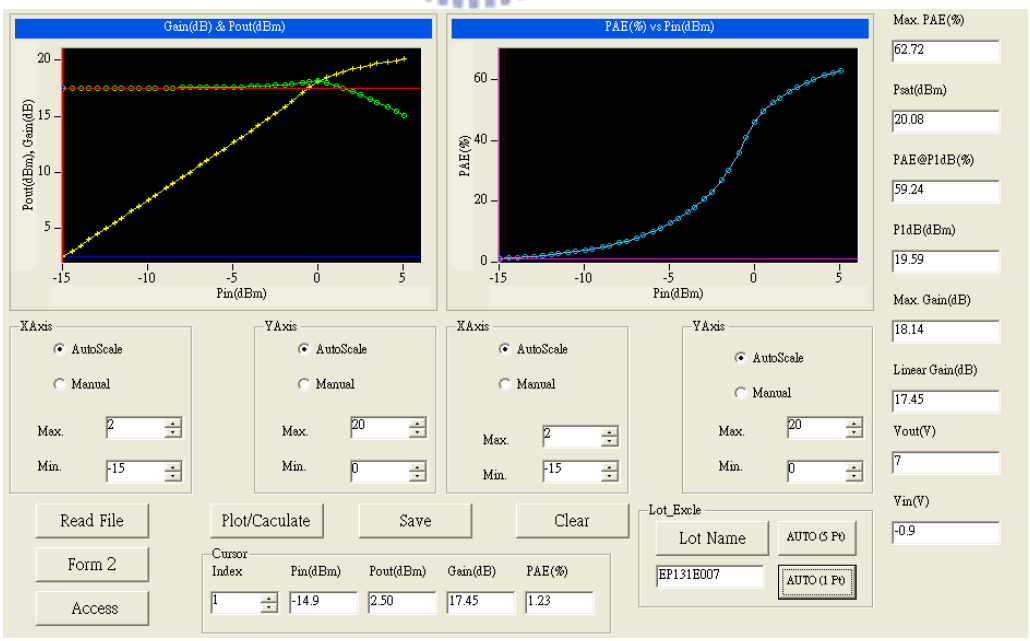


Figure 4-24 Ku band power performance at 10 GHz

From: WIN Semiconductors Corp.

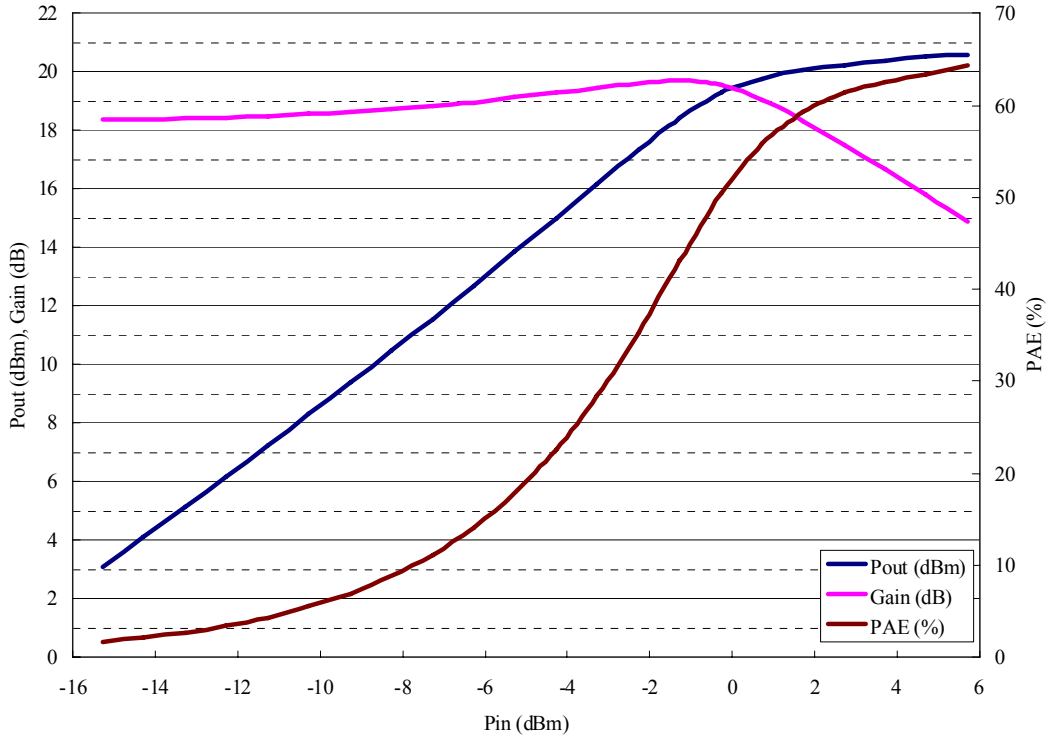
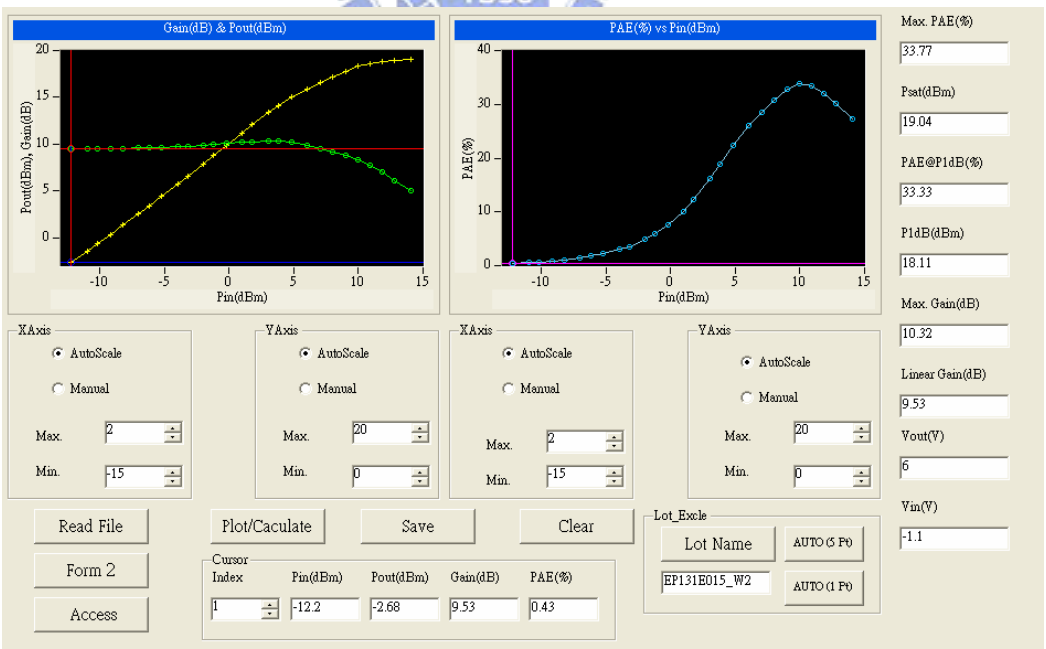


Figure 4-25 The Ku power gain and PAE of 10 GHz

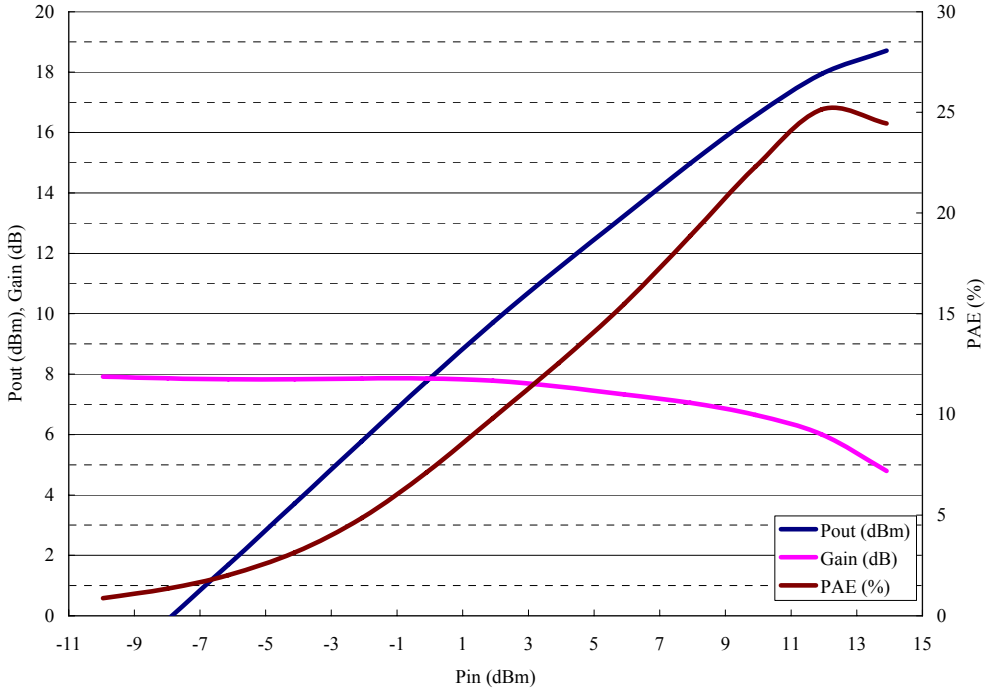
From: WIN Semiconductors Corp.

4.5.4.2.2 The Ka band power performance at 29GHz



(P1dB Power density=390~430 mW/mm @ 6V, 29GHz, 133mA/mm)
Figure 4-26 The Ka band power performance at 29 GHz

From: WIN Semiconductors Corp.



The power performance at 29 GHz (VD=6V, ID=10mA, VG=-0.55V)

Figure 4-27 The Ka band power and PAE of 29 GHz

From: WIN Semiconductors Corp.

4.5.4.2.3 The Power gain summary

Table 4-12 The Ka and Ku band power performance summary

Ka Band

			Bias Conditions				Power Performance					
VDG	Vto	DUT (μm)	Freq. (GHz)	VD (V)	ID (mA/mm)	VG (V)	Gain (dB)	P1dB (dBm)	P1dB (mW/mm)	Psat (dBm)	Psat (mW/mm)	PAE Max (%)
15.4	**-1.43**	**150**	**29**	**6**	**133**	**-1.10**	**9.8**	**17.6**	**385**	**19.1**	**538**	**33.8**
							9.5	**18.1**	**431**	**19.0**	**534**	**33.8**
							9.5	**18.1**	**431**	**19.1**	**541**	**34.1**

Ku band

			Bias Conditions				Power Performance					
VDG	Vto	DUT (μm)	Freq. (GHz)	VD (V)	ID (mA/mm)	VG (V)	Gain (dB)	P1dB (dBm)	P1dB (mW/mm)	Psat (dBm)	Psat (mW/mm)	PAE Max (%)
22.8	**-1.48**	**150**	**10**	**7**	**133**	**-0.90**	**17.5**	**19.6**	**607**	**20.1**	**679**	**62.7**
							18.4	**20.3**	**710**	**20.6**	**772**	**65.4**
							16.8	**19.2**	**551**	**19.5**	**597**	**47.2**

From: WIN Semiconductors Corp.

4.5.4.3 Noise characteristic

4.5.4.4 Table 4-13 The Noise characteristic

Freq:12GHz

DUT:2x75μm

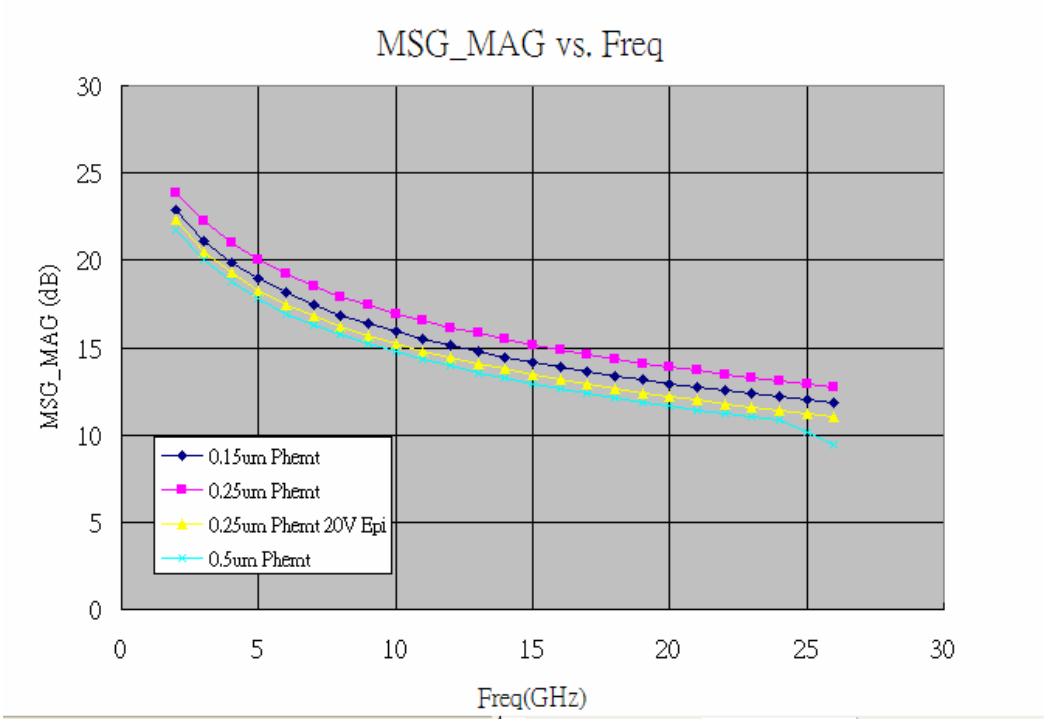
VDS=3V

IDS=10mA

VDS (V)	IDS (mA)	VG (V)	K factor	Fmin (dB)	Gassoc (dB)	MAG_MSG (dB)
3	10	-0.78	0.28	0.76	12.93	16.12
3	10	-1.05	0.30	0.85	11.42	14.43

From: WIN Semiconductors Corp.

4.5.4.4.1 The Noise comparison with 0.15μm gate pHEMT



(VD=3V, ID=10mA)

Figure 4-28 The Noise comparison with 0.15μm pHEMT.

From: WIN Semiconductors Corp.

4.6 The device performance comparison

We compared the DC and RF power performance with TRW Company by next table:

Table 4-14 The device performance comparison

29GHz	Gain (dB)	P1dB (mW/mm)	Pae(%)	vgd
0.15um pHEMT Ka@5V	11	600	52	10
0.15um pHEMT Ka@5V	10.5	750	43	10
TRQ 0.15 um Ka@6V	?	780	52	14
WIN 0.25 um Ka@6V	10.9	600	43	14
TRQ 0.25 um Ka@6V	7	550	34	14
0.25um pHEMT Ka@7V	10.7	760	40	14
0.25um pHEMT Ku@9V	20	1100	56	18
TRQ 0.25 um Ku@ 9 V	10	800	50	18

From: WIN Semiconductors Corp.

4.7 Device MTTF life test result

4.7.1 Test criteria

Bias conditions: 6V, 30mA (33% Idmax) Temperature:

150C (Tj=280C)

165C (Tj=299C)

180C (Tj=318C)

4.7.2 Test result. The MTTF>106 hrs

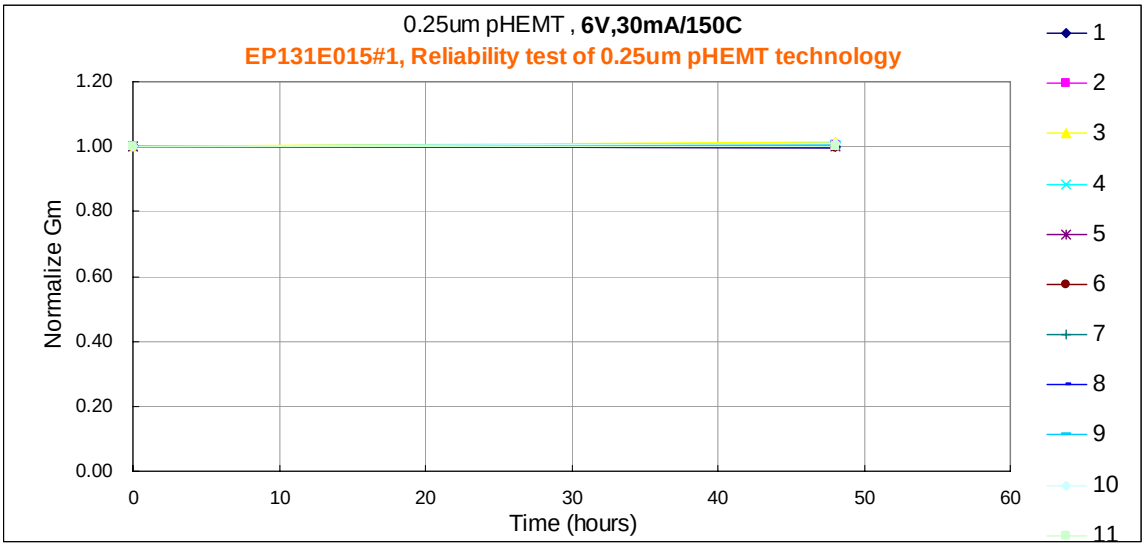


Figure 4-29 150C (Tj=280C)

From: WIN Semiconductors Corp.

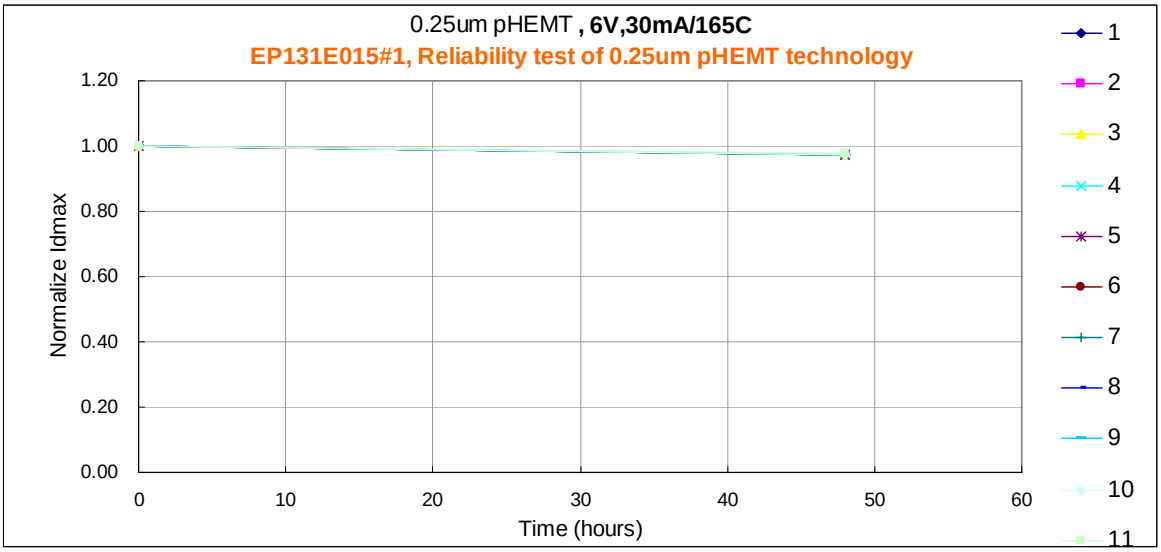


Figure 4-30 165C (Tj=299C)

From: WIN Semiconductors Corp.

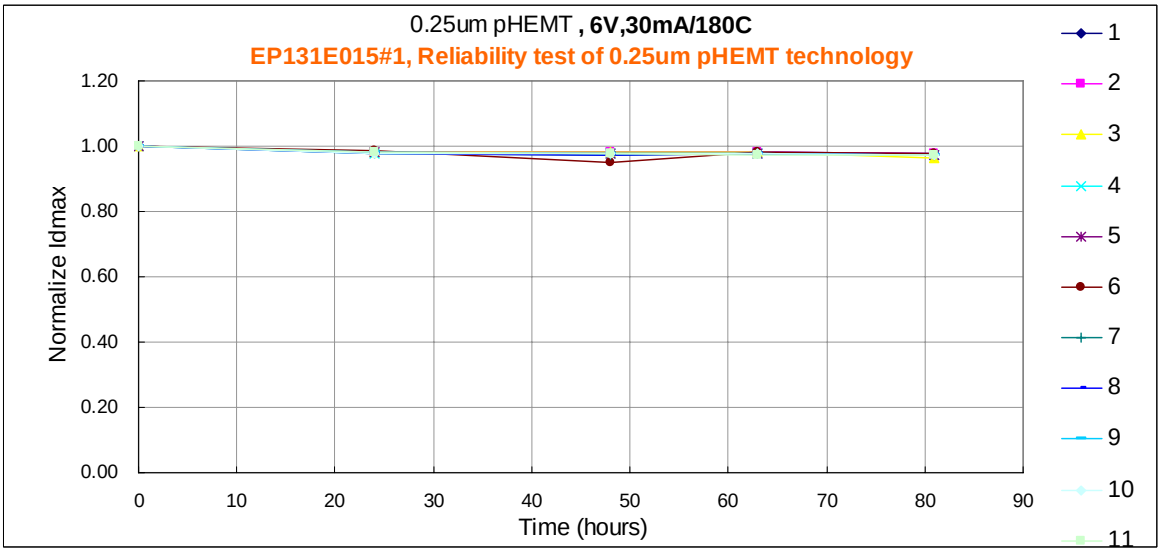


Figure 4-31 180C (Tj=318C)

From: WIN Semiconductors Corp.

Chapter5

Conclusion

We have demonstrated the triple lithographic Photoresist layers of 0.25μm gate process by I-line stepper for pHEMT ka/ku-band MMICs applications. We get good performances both of power and noise characteristics.

The technology of gate photo process is confirmed by ANOVA and process CPK analysis. The gate CD is on target 0.25 μm and uniform both within wafer and wafer to wafer. This is robust sub-micron gate process by I-line stepper for mass-production.

This triple lithographic Photoresist gate process has good coat effective than E-beam process. It's also good for mass-production and easy for manufacturable. The overall Ka and Ku band characteristics have developed. There is very clean surface on device after gate lift-off process. We checked by optical microscope and SEM inspection also. There are no any scum remain and no gate broken or other damage. We can check the gate leakage PCM data. The gate leakage is around 1E-3 to 1E-4 mA/mm. It means the gate is wall stand up on substrate. And there are also no scums remain caused leakage through the source-drain surface. The reliability of MTTF test has shown the good performance over 100 hrs. This process proved the cost effective, mass-production and good performance for Ka/Ku band MMICs application.

This process device has more Gain and similar P1dB to TRQ PP25@6V with 10% better PAE. When device @9V has better P1dB compare to TRQ This PHEMT device has higher Gain then TRQ for Ku and Ka band. This technology T-Gate has lower Cgd then TRQ T-Gate.

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