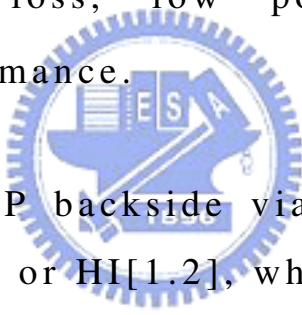# Chapter 1

Introduction

1.1 Overview

Indium Phosphide (InP) is a great semiconductor for high speed Monolithic Millimeter-wave Integrated Circuits (MMICs) and high speed digital and mixed-signal IC operating at frequencies from DC to 100 GHz. Superior high-frequency InP HBT performance with characteristics including a transit frequency, f_T of over 300 GHz and an oscillation frequency, f_{max} of greater than 300 GHz had been achieved. There are two attributes of InP HBT technology for high speed digital and mixed-signal IC with low to medium level of integration:

1) High Speed: InP HBT has the highest cut-off frequency as compare to technology at the similar or smaller critical dimension.

2) High reproducibility: The reproducibility of InP turn on voltage is typically a few millivolts while GaAs PHEMT is hundreds of millivolts.

To full fill the potential of InP HBT a robust IC process is required. One of the key process of InP HBT is backside via etch,

Backside via provides the following to an IC:

1. Dissipating heat: RF devices generate heat during operating, especially, the power amplify devices. The substrate ground pad is the only path that can dissipate most heat through this path. The primary heat path is through chip substrate, and the secondary heat path is backside via.

2. Lowers ground inductance: Not only improving high frequency performance but also simplifying assembly.

3. Low insertion loss, low power consumption and broadband performance.

Currently the InP backside via dry etch uses Halogen gases such as HBr[1.1] or HI[1.2], which are highly corrosive, dangerous and hazardous. HBr reacts with most metals in the presence of moisture, liberating hydrogen, an extremely flammable gas. When HBr is mixed with water, it canvases rapid corrosion of some metals. For environment concerns, the HBr requires anti-corrosive valves, pipes and exhausting system. An environment friendly, safe InP dry etch process is needed. Etch gas such as Cl_2 could be a good candidate to be studied. Also needed to make the backside via process highly manufactureble are proper wafer mounting and wafer thinning, masking techniques.

1.2 Advantage of InP- based semiconductors

InP-based process technology is a disruptive technology platform because it can be used to build both ultra-fast electronics as well as photonics integrated circuits; thereby truly integrate the manipulation of both electrical and optical signals in a single chip. In particular, InP-based heterojunction bipolar transistors (HBT) is suited for all high speed and low power digital-analog military and commercial applications [1.3]. It offers carrier velocities and mobilities which are significantly higher compared to silicon. High carrier velocities and mobilities can drastically increase the device figures of merit f_T and f_{max}. A comparison of material properties for SiGe, InP and GaAs is given in table 1.1. The electron mobility of both Si and Ge has significant lower than GaAs and InP group (InGaAs, InAs and InP). The velocity is given by product of mobility and applied electron field, which is associated with the energy gap of materials. Overall, the InP group is an excellent material for high-speed application. The equations as below explain the relationship between each others.

The drift velocity (ν_d) is given by

$$\mu \equiv q\tau_c / m_n \qquad (1)$$

$$\nu_d = -\mu\, E \qquad\qquad (2)$$

where

τ_c is mean free time.

m_n is effective mass.

μ is the mobility.

E is the applied electric field.

.

InP-based HBTs and high electron mobility transistors (InP HEMTs) are promising to realize high-frequency and high-performance MMICs. Figure 1.1 shows the comparison of f_T for Si- GaAs- and InP- based semiconductors. The important for high cutoff frequency, f_T, and maximum frequency of oscillation, f_{max}, is fast carriers (i.e. μ, Vpeak , Vsat) and for high output power is high breakdown field and voltage, i.e. wide bandgap.

$$1/2\pi f_T = \tau_{CE}(I_C) = \tau_B + \tau_C + kT(C_{je} + C_{cb})/q\, I_C + (R_e + R_c)\, C_{cb} \quad (3)$$

$$f_{max} \equiv (f_T / 8\pi R'_b C'_{cb})^{1/2} \qquad\qquad (4)$$

A commercial semiconductor foundry, GCS had demonstrated InP/InGaAs SHBT with the cutoff frequency reaches 200 GHz and the maximum frequency reaches 180 GHz, respectively. Figure 1.2 shows the InP SHBT cutoff frequency, f_T and f_{max} which were manufactured at GCS Inc.

InP HEMT devices with 0.1 µm gate length and 80 µm periphery have the average Gmp = 800 mS/mm, average Imax = 545 mA/mm, and average Vgp is 0.1 V. The typical sigma for Gmp, Imax, and Vgp is 66 mS/mm, 41 mA/mm, and 0.06 V, respectively. Device f_T is in excess of 190 GHz.[1.4] The applications include high performance power amplifier for cellular phones, ultra-efficient ultra-linear power amplifiers for digital communication systems and satellite networks ICs, highly integrated mixed signal and high-speed fiber-optic circuits. The rapidly expanding demand for broadband telecommunications provides a strong market due to the superior performance provided by InP microelectronics.

1.3 Challenges of InP Backside Via Process

The backside via is essential for MMIC technology, because it provides low parasitic inductance and low access resistance to the grounding plane, and a heat dissipation path. For higher frequency applications, accurate control of via properties becomes very important [1.5]. Since the final wafer thickness is in the order of 100 um, a back side via hole need to be etched about 100 um deep. To form deep vias into InP, high etch rate etching with vertical sidewall is required. Cl_2-based dry etching technologies are usually used for InP front side circuits etching [1.6] but not in Back side via etch. Because of the low volatility of etch by-products of $InCl_x$, high wafer temperatures are needed to obtain acceptable etch rate and good vertical sidewall profile for high aspect ratio via.

Using Chlorine chemistry to etch InP requires elevated temperatures approaching 160 ℃ or higher and/or significant ion bombardment to obtain acceptable surface morphology [1.7]. Tadocoro et, al. adopted $Cl_2/Ar/N_2$ process at a platen temperature of 180 ℃ to achieve the InP etch rate ~1.6 μm/min and the optimum profile of ~85° for waveguide application. However, when use same conditions for backside via process there will have two challenges. First, at backside via process the wafer needs to be thinned down, a proper

wafer mounting is need for the thinning and subsequent etch process. The mounting material must be able to sustain the high etch temperature and also can be easily removed when the process is completed. The second challenge is a proper mask which can endure the long etching time .But chlorine base gases are never be chosen at backside via etching, which requires high selectivity of InP to mask and also stable bonding material because the long etching time and high etching temperature.

Meanwhile, a metal mask that can endure high temperature is used. There are a few approaches for InP backside via etching using other gases. One approach used HBr gas and photoresist as mask, high etch rate of 1.5 μm/min was reported [1.8-1.9]. The other approach using HI-based ICP reported an average InP etch rate of 1.6 um/min with smooth etching surface at a low wafer temperature of 140 ℃ . The selectivity of InP to the silicon oxide mask is ~16:1[1.10]. Reactive ion beam etching (RIBE) system for InP backside via was also studied. The employed etching gas was ionized by electron cyclotron resonance (ECR) at a gas pressure of about 0.6 mTorr and the applied microwave power was 300 W. The maximum etch rate for InP was 2.0 μm/mim at 200 ℃ [1.11-1.12].

The profiles and surface have to be compatible with

device fabrication. Etch rates were determined using step heights measurement from patterned material of interest. In this study, we chose STS ICP as the dry etching tool. The ICP chamber was operating at 2 MHz and an additional RF bias was at 13.56 MHz for the sample chuck. Backside flowing He was used with a mechanical clamping configuration. The profiles were measured with a scanning electron microscope (SEM). SEM is a versatile instrument for characterization of etching features, and it provides high resolution, allowing submicron structures to be investigated. An electron gun is used to emit electrons with relatively high energy (5-30 keV), which are focused on a target. These electrons are incident on the target surface, and cause the electrons to be emitted. The secondary electron i.e. loosely bound electrons have the highest yield and are the ones usually measured. Since the electron wavelength is much smaller than the photon wavelength of visible light a much large magnification is possible than for an optical microscope.

The other dry etching method at InP HBTs is Emitter Mesa etching. Typical the epi structure is n^+ InGaAs and undoped InP is the barrier. The current recombination problem can be solved if the surface was protected by nitride or some studies present surface pretreatment and also have precision well controlled by using dry etch to remain about hundred angstrom of InP as a passivation layer. The precision etching

control is difficult in recent technologies. [1.13-1.14]

1.4 Objective of this study

- Establish a dry etch gases: Chlorinde (Cl_2) as InP backside via etching gas will be studied. The effect of gas compositions, pressure, temperature and power to the etch rate selectivity will be studied.

- Evaluate and select proper wafer bonding material for etching process: In order to accelerate evaporation of etching products so the substrate needs to heat up to certain temperature. Higher melting temperature bonding material is required to meet this requirement.

- Establish a proper etching mask: The top priority of establish a proper etching mask is higher selectivity of InP v.s. mask and also the productivity.

- Select proper carrier: Supporting carrier requires the same thermal expansion coefficiency as InP substrate in order to prevent the stress induced delaminating problem during thermal process. High anti-acid and anti-solvent soluble are also important.

Chapter 2
Theoretical of Dry Etching Process

There are two main types of etching process have been used in semiconductor fabrication: wet etching and dry etching. Wet etching tends to be highly selective but isotropic. Isotropic etching implies undercutting. Selectivity is usually excellent in wet etching. Mask erosion can be an issue for both isotropic and anisotropic etching profiles. Dry etching is preferred when precise control of etched feature is required.

2.1 Dry Etching Mechanism

There are three principal mechanisms in dry etching process: chemical etching, physical etching and ion-enhanced etching.

Chemical etching: the chemical reactions are done by reactive neutral species, such as free radicals. Additives can help to react with etchants to form more free radicals that enhance the etching rate. The free radical etching mechanism is similar with the wet etching and therefore tends to isotropic and selective. The sticking coefficient number is almost 0, that means, the free radicals do not adsorb upon the surface.

Physical etching: ions travel toward to wafer surface when apply the electron field cross the plasma sheath. Ion etching is much more directional and its sticking coefficient is almost 1 so the ions do adsorb upon surface, i.e. ions don't bounce around if they do not lose their energy. Etching species remove material by sputtering. The result is not very selective since all materials sputter at about the same rate. Physical sputtering can cause damage to surface, with extent and amount of damage a direct function of ion energy.

Ion enhanced etching: chemical and physical components of dry etching do not always act independently. These two components in terms of net etch rate and in resulting etch profile. Etch profiles can be very anisotropic, and selectivity can be good. Many different mechanisms proposed for this synergistic etching between physical and chemical components. Ion bombardment can enhance etch process in the following ways: damage the surface to increase reaction, remove etch byproducts, or remove inhibitor that is an indirect byproduct of etch process such as polymer formation from carbon in gas or from photoresist. Multiple mechanisms may occur at same time.

Figure 2.2 shows a diagram of etching formation mechanism. There are molecules dissociation, ionization, absorption, product formation, recombination and product adsorption.

- Dissociation, ionization and recombination: In general, the plasma species can be broken into two broad categories: electrically charged (ions and electrons) and charge-neutral (radicals). An ion is an atom or molecule which has lost or gained one or more electrons, making it positively or negatively charged. A negatively charged ion, which has more electrons in its electron shells than it has protons in its nuclei, is known as an anion due to its attraction to anodes. Conversely, a positively-charged ion, which has fewer electrons than protons, is known as a caution due to its attraction to cathodes. Ions are denoted in the same way as electrically neutral atoms and molecules except for the presence of a superscript indicating the sign of the net electric charge and the number of electrons lost or gained, if more than one. Radicals (often referred to as free radicals) are atomic or molecular species with unpaired electrons on an otherwise open shell

configuration. These unpaired electrons are usually highly reactive, so radicals are likely to take part in chemical reactions. For example, Cl_2 into $2Cl\cdot$ has a $\Delta H°$ of +243 kJ/mol. The symptom of recombination is, the reaction can be opposite when the broken molecules join together to form the original state. An example of BCl_3 and Cl_2 plasma is as below.

$$e* + 2Cl_2 + 2BCl_3 <=> Cl_x^+ + BCl_x^+$$

$$+ Cl_x + BCl_x + e$$
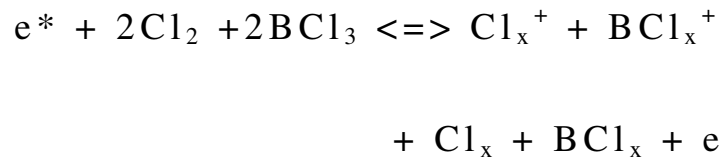
- Absorption and product formation: The Boron trichloride and Chlorine (BCl_3/Cl_2) gases will form ions after plasma striking. Those ions can react with InP to form volatile products. After the etchants formation, those etchants will adsorb onto the wafer surface due to the plasma potential difference. The discharge creates uncharged etchant radicals which react with a surface material through conventional chemical reactions. Ions induce general surface heating, or sputter cleaning from the surface. There are dozen of products are formed once the etching process occurred.

$$4Cl_x^+ + 4BCl_x^+ + 4InP \rightarrow 2InBCl_x + 2InCl_x + PBCl_x +$$

$$PCl_x + BCl_x + PB + Cl + P_x$$
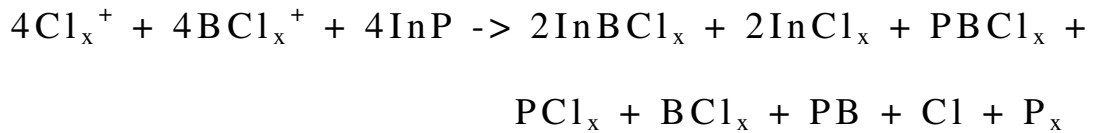
2.2 Choosing etcher and gases for InP backside via etching

ICP was chosen as the etch system in the study because it has the following advantages:

1. It has over two orders of magnitude higher plasma density than conventional RIE systems to enhance the chemical reactions.[2.1]

2. A ICP etcher is relatively free of contamination because the plasma generating electrodes are completely outside the reaction chamber. Also, the ICP offers effective decoupling between the ion density and the ion energy to improve the dry etch control capabilities.

In a ICP etcher, the gas molecular is starting dissociated and ionized once the ICP RF power is delivered. Part of ions will recombine in the plasma. Boride and chlorine ion flux is perpendicular to substrate and adsorb on surface once the platen RF power is delivered. Chemical etching and sputtering etching will occur. Chloride products are formed when the ions or neutral radicals are reacting with substrate. Inhibitor films can be formed and deposits on feature sidewalls. Etch rate is limited by the ion flux, how volatile of products and sputter yields. ICP discharges are of relatively

high electron density, of the order of 10^{15} cm^{-3}. As a result, ICP discharges have wide applications when a high density plasma is necessary. Another benefit of ICP discharges is that.

Cl$_2$ and BCl$_3$ are chose as the etching gas for the following reasons: Chlorine is the main gas which ionized in the plasma and react with InP to perform etching.

Boron trichloride is a particularly attractive discharge, because it getters water vapor and so is quite forgiving of its residual amounts in the vacuum chamber. It also readily attacks the native oxide, and provides smooth, controlled etching. Pure chlorine tends to have extremely fast etching rates and non uniform etching due to the inhibiting native oxide on the semiconductor surface.

2.3 The principal of ICP etcher

Figure 2.1 shows the schematic of ICP chamber with cylinder geometry. In cylindrical geometry, it is like a helical spring. Inductively coupled source does not have an electrode in the plasma. This type of coupling is a much more efficient method of transferring power to the electrons and, consequently of increasing the plasma density. When an electric current is passed through the inductor of copper coil, it creates a time varying magnetic field within the chamber. The electromagnetic field is typically set to a frequency of 13.56 megahertz, applied at a few hundred watts. The electrons oscillate with this electric field and collide with neutral atoms to form the excited species and ions. Electron field is formed; the density is $\sim 10^{15} cm^{-3}$. Electron temperature is $\sim$ 11,600 K and its velocity is 9.5×10^{7} cm/sec. Ion temperature is $\sim$500 K and its velocity is 5.2×10^{4} cm/sec. Neutral temperature is $\sim$293 K and its velocity is 4.0×10^{4} cm/sec.

ICP discharges have wide applications when a high density plasma is necessary. Another benefit of ICP discharges is that they are relatively free of contamination because the electrodes are completely outside the reaction chamber. The ICP offers effective decoupling between the ion

density and the ion energy to improve the dry etch control capabilities.

A RF (radio frequency) power through a coupling capacitor is applied the substrate chuck. In each cycle of the field, the electrons are electrically accelerated up and down in the chamber. At the same time, the much more massive ions move relatively little in response to the RF electric field. When electrons are absorbed into the chamber walls they are simply fed out to ground and do not alter the electronic state of the system. However, electrons absorbed into the wafer platter cause the platter to build up charge due to its DC isolation. This charge build up develops a large negative voltage on the platter, typically around a few hundred volts. The plasma itself develops a slightly positive charge due to the higher concentration of positive ions compared to free electrons.

Because of the large voltage difference, positive ions tend to drift toward the wafer platen, where they collide with the samples to be etched. The ions react chemically with the materials on the surface of the samples, but can also knock off (sputter) some material by transferring some of their kinetic energy. Due to the mostly vertical delivery of reactive ions, reactive ion etching can produce very anisotropic etch profiles, which contrast with the typically isotropic profiles

of wet chemical etching. [2.3]. The sample placed on this powered electrode is subject to intense ion bombardment. ICP has an advantage of synergism between physical and chemical etching mechanisms and is able to provide fast anisotropic etching.

2.4 Side effects in etching process

If the reactions between etchant and pure substrate are the main event in etching, then other phenomena that are not a direct part of these reactions might be termed "side effects." The complexity of feed gases and etching systems may be understood in terms of these secondary phenomena. Of course some "side effects" are nearly unavoidable in all etching processes and they can either be beneficial or harmful. Such effects arise from the chemistry of feed additives, others stem from variability in substrate composition, and still other things are attributable to reactor chamber design. A few effects are listed in Table 2.3, along with an example of each and their influence on etch rates, sidewall passivation (in inhibitor anisotropic etching), and profiles.

Etch rate definition: The etch rate is given by the Arrhenius expression

$$\text{Etch Rate} = A n_F T^{1/2} e^{-E_A/RT} \quad (5)$$

Where A is Preexponential factors and n_F is the number of fermions and E_A is activation energies and R is the gas constant and T is temperature in kelvins.[2.4]

Dissociation species and mass numbers: Table 2.2 is shown the dissociation species and mass numbers at BCl_3/Cl_2 plasma when etching InP materials. The by-products and etchants for plasma etching of InP were determined using a mass spectrometer.[2.5]

Chapter 3

InP Wafer backside fabrication

3.1 InP Wafer Backside Process Flow

The final steps in fabricating InP HBTs and HEMTs are wafer backside process, which includes thinning, via hole formation, metallization, demounting and separating. The purpose of wafer thinning from the backside is to improve thermal impedance and easy to do chip singulation. A 100 µm final substrate thickness is typically used. A 50 µm substrate has been adopted for power application devices. Uniform substrate thickness is required to produce an uniform via hole etching process. The backside via hole provides electrical conductivity, thermal dispensation and low inductance for high performance high frequency power devices and low noise devices.

Via hole can be formed by wet chemical etching or dry etching. The dry etching process is less sensitive to the uniformity of wafer thickness and also provides small vias with controlled etching profiles. The next step after via hole etching is metallization, metal plating technology is typically used. Seed-layer is required before metal plating. E-beam evaporator and sputter are typically used to provide every good contact of metal to substrate. The wafer has to be

mounted on tapes before separating. Sawing or scribe and break technique is typically used.

Figure 3.1 shows the backside process flow. The challenge step of InP backside process is via hole etching. InP materials have an intrinsic property of hard to corrosive even by halogen gases. The etch normally take place at high temperature and high plasma density. Proper mounting and mask are required to make the process successful. Table 3.1 has a list of the importance of process materials; bonding materials, backside via mask and wafer carrier. The bonding materials require high melting temperature and high resistance to acid chemicals. The candidate for the bonding material has high melting temperature resin, high melting temperature was and high temperature thermal release double side tape. Figure 3.2 shows the process temperature limitation of current commercial bonding materials in semiconductor industry. The C, H, O are the key elements to form the resin which will be easier to dissolve in solvent and/or strip by oxygen plasma. The backside via mask has to be easier to produce and higher selectivity to InP during dry etch and the bi-product nust to be easier to remove. The candidate for the mask has photoresist, dry film resister, low temperature nitride and Ni metal masks. Figure 3.3(a) shows photoreisist mask thickness is 17 µm, which was done by using single coating and photolithography processes. Figure 3.3(b) shows

Ni mask, the pattern was defined by wet etching process on thinned InP substrate. The wafer carrier must to have the same thermal coefficiency as InP, higher mechanical stress and can resist solvent, acid and ion bombards. The candidate has sapphire, glasses and SiC. Table 3.2 lists the thermal properties of InP, SiC, glasses and Sapphire materials. Sapphire has an advantage that it has almost the same linear thermal expansion with InP. But Sapphire has a disadvantage of poor thermal conductivity, substrate thickness is limited to avoid thermal effect during processing.

In this study samples were fabricated according to the process flow shown in Fig.3.1 to back side via mask. The wafers were then cut into 10 mm x 10 mm for etching experiment. Next step is to re-bond each sample on sapphire for dry etching experiment. The purpose is to conserve the InP wafers. Figure 3.4 shows the specimen process flow.

3.1.1 Wafer Bonding

Before the wafer is mounted for wafer thinning, the wafer front side must be protected first. A frontside processed 4-inch diameter InP wafer was coated with non-photosensitive Polymethyl methacrylate (PMMA), which can protect the frontside circuits without any contamination during entire backside process. The next was coated with Pentalyn X resin, which has higher softening point of 158 ℃ and has reflective

index of 1.54. Then the wafer was bonded at 190 ℃ hotplate by using dynatex wafer bonder. The diameter 4.25 inches sapphire wafer was as a carrier to support 4 inches InP wafer. The sapphire carrier was designed with holes that can demount the wafer sufficiently. Although thicker sapphire can resist mechanical strain but it will effect the thermal conduction. 1mm or less is more popular spec using in current compound semiconductor Fabs.

3.1.2 Wafer Thinning

Wafer grinding process: After InP wafer was bonded on the sapphire carrier, the next step is to thin down to 120 μm by use grinder. The grind grit size and feeding rate both are very important to reduce the surface damage, respectively. At the last 30 μm, the feeding rate should lower than 2 μm/min.

Chemical polishing process: Wet chemical polishing is necessary for relieving stress. It not only removes the damage layer but also smooth the surface. The polishing bath is one part of HCl and 1 part of H_3PO_4, which polishing rate is ~ 2.5 μm/min at room temperature.

3.1.3 BV Mask

After the wafer was thinned down to 100 µm, the next step is to deposit Ti/Ni on the backside surface. Before wafer loading into the evaporator, pre-clean is necessary to remove the oxidation layer [3.1]. The wafer was immersed into diluted HCl. Wafer needs to be loaded into the evaporator within 20 min after pre-cleaning. The chamber has to be pumped down to 8×10^{-7} torr before metal deposition in order to evacuate moisture and gas residues. The evaporated Ni metal has very high film stress so the Ni thickness and deposition rate are important to prevent this issue. In my study, the Ni thin film will peel-off if the Ni thickness exceeded 5,000 Å and if the deposition rate is higher than 5 Å /sec.

The positive photoresist and i-line proximity contact aligner were used to define via patterns. Ni was etched by nitric acid at the etching rate of 2,000 Å/min at room temperature. And the underneath Ti was etched by diluted BOE.

3.1.4 Backside Via dry etching

Gas: Halogen gases, BCl_3/Cl_2 composition, are the main etching gases. They have been used in GaAs wafer dry etching process for at least twenty years. They do not damage the gas

delivery systems, chambers and pumping systems if operating properly. The dry etching tool can be used for both GaAs and InP wafer substrates in the same chamber. The tool can not only be improved the capability but also be improved the flexibility as well.

Tool: STS ICP etcher, which has 13.56 MHz ICP power, the max power is 1.2 kW and has the same frequency platen power, the max power is 0.3 kW. The chuck chiller temperature can be lower down to -40 $^{\circ}$℃ and be higher to 160 $^{\circ}$℃. The BCl_3 and Cl_2 gas flows were varied from 50 sccm to 200 sccm, that can be optimized both the etching rate and etching profile. The etching profile obtains to isotropic if the total gas flow has Cl_2 reached. The ICP power was varied from 300 W to 900 W that higher ICP power induces that more gas molecules have been ionized and also the plasma temperature will rise to obtain higher etching rate. The platen power was varied from 50 W to 250 W that higher platen power enhances bombardon force and results physical sputtering effect. The working pressure was varied from 10mtorr to 30 mtorr that lower chamber pressure will increase the mean free path of energized molecules and natural species so the selectivity and etching rate also increased. The chuck temperature was varied from room temperature to 140 ℃ that the higher chuck temperature helps the etching products

volatile and then increases the etching rate. Before each run, chamber was cleaned by oxygen plasma and was conditioned by dummy run. The specimens were sitting on the chuck for 10 min before delivering RF powers. Etching times were fixed at 10 min. Via pattern was 50 µm. All specimens were measured by α-step height measurement tool and were inspected under optical microscope and scanning electron microscope as well.

3.1.5 BV Clean and Seed-layer Sputtering

The clean process after BV etching is important to remove all etching products. Wafers were immersed in diluted hydrochloride acid for 5 min to remove residue products. And following immerse into diluted nitric acid and BOE to remove the hard mask metals. Before seed layer TiW/Au sputtering, a proper cleaning process is necessary to obtain clean of backside surface. Diluted hydrochloride acid can remove oxidation layer on the substrate and follow by QDR to wash residue acid away. Appropriate wafer drying process is necessary to avoid the water bead trapping inside via holes. Hot N_2 spin dryer was used for this approach.

3.1.6 Gold Plating

- The next step is gold plating. To improve the

uniformity of plated Au thickness in the vias, we optimized the plating current and plating liquid flow condition. Figure 4.3b shows a cross-section of the InP backside via after Au plating. The diameter at the opening of the via was 50 µm. Via etching was stopped at the frontside Au stack and the thickness of plated Au was 5 µm. The current density is controlled at 0.1ASD and the plating liquid is circulating with the flow of 20GPM. Pulse current plating also can be used to increase the Au thickness. The duty cycle is typically 10:90.

3.1.7 BS Photo Lithography, Gold Etching and PR striping

The 17 µm thick photoresist was used to protect the un-etched metal. Gold metal around the via will expose without photoresist covered if the resist thickness is less than 12 µm. I-line proximity contact aligner was used to define backside street patterns. Gold etching was done by using GE 8148 gold etchant, the etching rate of the gold is about 0.5 µm per min. Agitation is required for better etching uniformity. The underneath TiW was removed by using pure H_2O_2 at room temperature. ACE can thoroughly remove the photoresist. O_2 plasma clean was used to clean all organic

residues.

3.1.8 Wafer Demounting

The traditional wafer demount process has low visual yield problem because of breakage, scratches and contamination issues. Thin wafer handling process is an essential step for InP wafer. Proper fixture support is necessary to prevent low yield problem during cleaning and handling steps. The idle for the fixture design is to reduce the contact area at both fixture and wafer, adequate contact is also required. The demount fixture (Patent application number 208854 of ROC was public in Taiwan since Aug. 2003 and application number 582406 in China since Oct. 2002) was implemented at 4 inches and 6 inches wafers successfully. Figure 4.11 shows the schematic fixture design.

3.2 Study of backside via inductance measurement:

The Z parameters are derived from the S parameters normally measured on 2 port network RF test system[2.6]. This measurement from 0.1 to 19.9 GHz, and do typically see a slight decrease in L for higher frequencies, due to a structure stray inductance.

$$Z_{11} = (1+S_{11})/(1-S_{11}) \quad (6)$$

$$L = ImZ_{11}/j\omega \qquad (7)$$

In the equations, L is via inductance, $\omega = 2\pi f$, and f =measurement frequency.

Chapter4

Results and Discussion

The best etching condition for 100 µm InP backside via hole etching; the gas flow is 160 sccm BCl_3 / 160 sccm Cl_2 with 20 mtorr working pressure and the wafer was sit on the 140 ºC chuck and with delivering 900 watts ICP power / 150 watts platen power. The result of each process step of the InP wafer backside process and the effect of dry etching conditions are shown in this chapter. The backside via RF inductance result is also and measured and discussed.

4.1 Wafer Bonding

3 µm thick non-photosensitive PMMA was coated primary on the InP wafer surface. 15 µm thick resin was coated onto the PMMA. The wafer and perforated sapphire were bonded together on the 190 ºC hot plate. The total thickness variation is less than 3 µm.

4.2 Wafer Thinning

After InP wafer was bonded on the sapphire carrier, the next step is to thin down to 120 µm by use grinder. The grind grit size is #600 and feeding rates are 12 µm per min for rough grinding and 2 µm per min for fine grinding,

respectively. The post grinded wafer was etched in one part of HCl and one part of H_3PO_4, polishing solution, which polishing rate is ~2.5 µm/min at room temperature. Figure 4.1 shows the result of wafer substrate thickness after thinning can be controlled within +-5µm and its Cpk is 1.33. The average wafer thickness is 100 µm and the range of wafer thickness is less than 3 µm. The surface roughness after chemical polishing is 0.25 µm, which was measured at alpha step height measurement.

4.3 Ni Hard Mask

Before wafer loading into the evaporator, the wafer was immersed into diluted HCl for surface cleaning. When the chamber pressure is reached to $8x10^{-7}$ torr, 500 Å thick Ti was first to be evaporated in order to increase the adhesion between InP surface and Ni. 4000 Å thick Ni was evaporated at very low deposition rate is about 2 Å/sec. $9x10^9$ dynes/cm^2 tensile film stress was measured at film stress measurement gauge. The Ni etching rate is about 2000 Å/min by using 50% diluted HNO_3 acid. The Ti etching rate is 750 Å/min by using 2% diluted HF acid. Figure 4.2 shows the Ni undercut is 0.24 µm and Ti is 0.72 µm, respectively.

4.4 Backside Via etching

The best etching condition for 100 μm InP backside via hole etching; the gas flow is 160sccm BCl_3 / 160sccm Cl_2 with 20mtorr working pressure and the wafer was sit on the 140 °C chuck and with delivering 900 watts ICP power / 150 watts platen power. After the wafer was etched for 100 min, the 100 μm deep via was obtained. The bottom via diameter is about 50 μm and the top diameter is about 90 μm, respectively. And its profile was perfected round cylinder with vertical shape, which is the best result for the backside metal plating. Figure 4.3(a) shows the top view of the etched via, which was etched 50 μm depth. The undercut is about 10 μm. As illustrated in Figure 4.3(b), the vertical and tapered via holes were readily produced. The result also revealed the possibility of increasing InP backside via etch rate 1.2 μm/min.

4.4.1 Effect of the chlorine percentage

Figure 4.4 shows the etching rate of InP v.s. percentage volume of chlorine in BCl_3/Cl_2 plasma. The etching rate increases when chlorine flow rate increases. The lower Cl_2 gas flow represents 0.1 μm/min lower etching rate because of the inhibitors start to from on the substrate surface, which limits the etchant absorb onto the surface. The other hand, the higher Cl_2 gas flow represents 1.3 μm/min higher etching rate but the profile is more isotropic.

4.4.2 Effect of ICP power variation

Figure 4.5 (a) shows the etching rate of InP v.s. ICP power. Higher ICP power increases ion plasma density so the etch rate increasing. The contribution of the higher etching rate is due to the more ion plasma density and more plasma temperature introduced at higher ICP power. We can achieve 1.2 µm/min etching rate when the ICP power setting is 900 W. Figure 4.5 (b) shows the wafer temperature as a function of ICP power, temperature was recorded by using TL-E-250 and TL-E-330 temperature dot indicators that were taped on the wafer surface.

4.4.3 Effect of chuck temperature and working pressure

Figure 4.6 (a) shows the etching rate of InP varies chuck temperature. Temperature is the most important variable for improving etch rate and selectivity. In order to remove the InClx products, the surface temperature has to increase to above 140 ℃, which increases the activation energy. At 140 °C it is possible to obtain an etch rate up to 1.2 µm/min. At room temperature, the InP can't be etched even at low working pressure. The reason is the etching products still absorb on the surface since the temperature can't reach volatile point. When the chuck temperature was set at 140 °C we can achieve 1.2 µm/min etching rate at 20

mtorr working pressure and 2.0 µm/min etching rate at 10 mtorr working pressure, respectively. Figure 4.6 (b) shows the etching rate as a function of the working pressure. Because of the mean free path of molecule and nature species increase the lift time of the etchant. Figure 4.7 shows the SEM micrograph of via profiles when were etched under different working pressures, 10 mtorr, 20 mtorr and 30 mtorr. The undercut was significant when increasing the working pressure. Maintaining the plasma density and uniformity at high pressure is very important for achieving a high etch rate. A high pressure means that there is an abundance of the reactive species available. Energetic free electrons within the plasma impact with the heavier Cl-containing molecules, breaking the chemical bonds and thereby releasing charged Cl radicals for etching.

4.4.4 Effect of platen power variation

Using a platen power means that the etchant radicals are accelerated vertically down onto the substrate, so features with high aspect ratios such as via holes can be etched. Figure 4.8 shows the etching rate of InP varies platen power. The etching rate increases when platen power increases. The ion flux induces the sputtering yield, which results much more bombardment etching. The etching rate is slightly increase at the higher working pressure because of the products can't diffuse away from the surface and slow the etchants absorb onto the surface to form product. The maximum etching rate at 250 W higher platen power is only 1µm/min. The etching

rate significant increase to 7 µm/min at 10mtorr working pressure and 250 W platen power was applied but the selectivity became very low. Figure 4.9 shows the hard mask Ni was completely etched away during etching process and the InP substrate was over etched about 30 µm. This is a tradeoff situation that we can't keep higher etching without the good electivity.

4.4.5 Selectivity of hard masks

Figure 4.10 shows the selectivity of Ni, photoresist and low temperature nitride. The photoresist and nitride have poor selectivity compare to InP substrate which is less than 5 even though the specimen was etched at high working pressure. Another word, the photoresist and low temperature nitride are not suitable at this application. By using Ni metarial as a hard mask, we can achieve the selectivity is over 200 when the working pressure is set at 20 mtorr or 30 mtorr. Even though the lower pressure operation, the selectivity still can reach 50.

4.5 Backside via clean

When the InP wafer has been dry etched, the wafer immersed in 20% diluted HCl for 1min. The wafer surface color changed obviously from brown to silver, the phenomenon is that the surface $NiCl_x$ dissolved in the acid chemical. And then the wafer was put into the quick dump

rinse tank for 5 min to wash aide chemical away. The adhesive Ti layer was exposed when the Ni hard mask was removed. To remove the Ti layer, the wafer was immersed in the 2% diluted HF for 45 sec. The wafer surface started to generate bubbles when it was immersed in the diluted HF for approximate 35 sec. The bubble creation phenomenon was that the Ti reacted with HF and was stopped after 3~5 sec. Followed by quick dump rinse for 5 min to wash acid away and then spin dry the wafer.

4.6 Backside metal plating

In order connect the circuits from frontside to backside through the vias, gold plating is necessary at this application. 500 Å thick TiW and 2000 Å thick Au were sputtered on the wafer backside in DC sputtering machine. Before these two layers were sputtered, the wafer was dry cleaned by using Ar ions for 5min inside the sputtering machine under the 5×10^{-7} torr pressure. The purpose of this step is to remove the impurities and oxidation layer on the wafer backside surface in order to make a good contact to TiW and Au. In order to reduce via resistance, the 5 μm thick gold was plated on the backside surface. Usually, the gold thickness inside the via is very difficult to reach the good step coverage because of the high aspect ratio of the via. In my studies, there were three improvement actions were taken to increase the step coverage to 80%. First, was to improve the gold surface wettability by treating at O_2 plasma, which can eliminate the air bubbles inside the via. Second, was to maintain the gold concentration as highest as supplier recommended, which can improve the

gold ions diffuse into the via, it will help if the bath has a good circulation. Third, was to use the pulse plating instead of DC, which can improve the uniformity of the current density on the wafer backside surface.

Backside street photolithography was done to define the individual die. Diluted KI solution was used to etch the plating gold and sputtering gold. And the TiW was removed by pure H_2O_2 solution at room temperature. When the gold and Tiw were etched, the photoresist was stripped by ACE and IPC.

4.7 Backside metal adhesion

Poor backside metal adhesion will affect the device reliability and cause failure. So the adhesion check is important to make sure the backside metal has no problem before the wafer has been singulated. Tape taping test was performed. The procedure of this test is, first, to tape the blue tape with 30 g / 25 mm viscosity on the wafer backside. Second, this tape was peeled at 45 degree departure angle. The result was shown that there was no any metal piece lifting.

4.8 Wafer demount

Accommodated adequate demount fixture at wafer demount step in which we can establish high yield rate demount process. 4 inch InP thin wafer was demounted intact

and was perfectly clean after inspected by using high magnification optical microscope.

4.9 RF inductance

In order to measure the accurate inductance and resistance of via holes, an appropriate pattern design is essential. Figure 4.12 shows the PCM test pattern. There are two set of the opposite rectangle metal patterns. Via hole is underneath every single pattern and is connected by backside plating metal. Figure 4.13 shows the measurement result. From S-parameter measurements that the frequency was applied to 19.9 GHz, the average inductance of 46 pH was extracted and expressed for the vias with 50 μm diameters at the range of 10~15 GHz frequency , which is the same as the existing GaAs result.

Chapter5

Conclusion

A high yield InP back side via process with environment safe dry etching gas was developed in this study. A high softening temperature (150 ℃ ~ 160 ℃) resin was used for wafer bond. Carbon, hydrogen and oxygen are the main elements in the resin which can be removed easily by using either solvent or oxygen plasma. The Sapphire disc was used as the backing substrate for the back side vis process because Sapphire not only has almost the same thermal expansion coefficient as InP (4.5 and 4.6 for sapphire and InP, respectively) but also has high mechanical strength and can endure the solvent, acid and ion bombards encountered in the backside via process.

Wafer grinding and chemical-mechanical polishing were used for wafer thinning. The wafer thickness uniformity is controlled within +-5 µm and its Cpk is 1.33. The average wafer thickness is 100µm and the range of wafer thickness is less than 3 µm across a 4" wafer. An alpha step measurement result indicated that the suface roughness after polishing is less than 0.25 µm.

Ni was selected as the etching mask due to it has very high etching selectivity over InP. The product of Ni in the ICP etch, $NiCl_x$, has very high volatile point (about 1000 ℃ at 1 atm) that give Ni a very high selectivity to InP during ICP plasma etching. However, Ni has poor adhesion to InP

substrate. It is necessary to have a interlayer Ti evaporate deposit onto InP before Ni is deposited. To stand the etching of a 100 um via hole, a 4000 Å thick Ni is needed. In this study it was determined that Ni must be deposited at a very low deposition rate to avoid peeling. A 4000Å Ni deposited at rate 2 Å/sec on 500 Å/InP had been successfully used in this study without any peeling problem. The metal film has a $9x10^9$ dynes/cm^2 tensile film stress as measured with a film stress measurement gauge. The Ni/Ti can be chemically removed easily after via etching process. The Ni etching rate is about 2000 Å/min by using 50% diluted HNO_3 acid. The Ti etching rate is 750 Å/min by using 2% diluted HF acid. The Ni undercut is 0.24 μm and Ti is 0.78 μm, respectively.

The etching rate and selectivity v.s. ICP parameters were studied. Best via etching process condition is 20 mtorr working pressure, 160 sccm BCl_3 and 160 sccm Cl_2 gas flows, 900 W ICP power, 150 W platen power, 140 ℃ chuck temperature. At this etching conditions a via hole on100 μm thick wafer have diameters of about 50 μm and 90 μm at the bottom and top of the via, respectively. And the via hole profile was similar to a bowl shape. The etching rate is 1.2 μm/min and the hard mask selectivity is over 200.

The gold step coverage inside the via is about 80% with excellent adhesion. There is no backside metal adhesion

problem as verified by tape test on the entire wafer.

Wafer has no breakage or scratch after demounting by using a patented wafer handing fixture, number 208854 of ROC.

From *S*-parameter measurements that the frequency was applied to 19.9 GHz, the average inductance of 46 pH was extracted for the vias with 50 µm diameters at the range of 10~15 GHz frequency, which is the same as the existing GaAs results.

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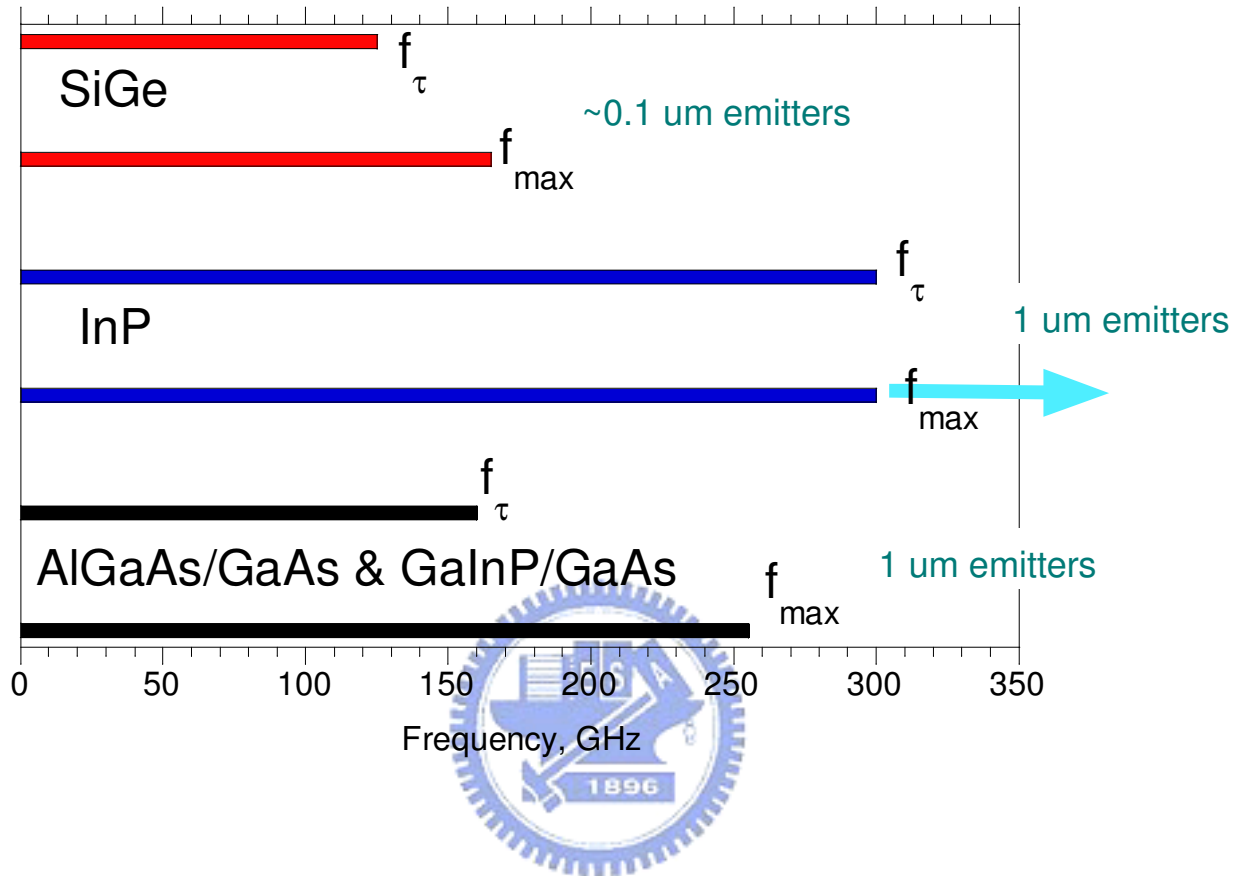
Figure 1.1 Cutoff frequency comparison of Si- GaAs- and InP- based semiconductors. Source from Rodwell et al, UCSB: Keynote talk, 2000 IEEE Bipolar/BICMOS Circuits and Technology Meeting, Minneapolis, September.
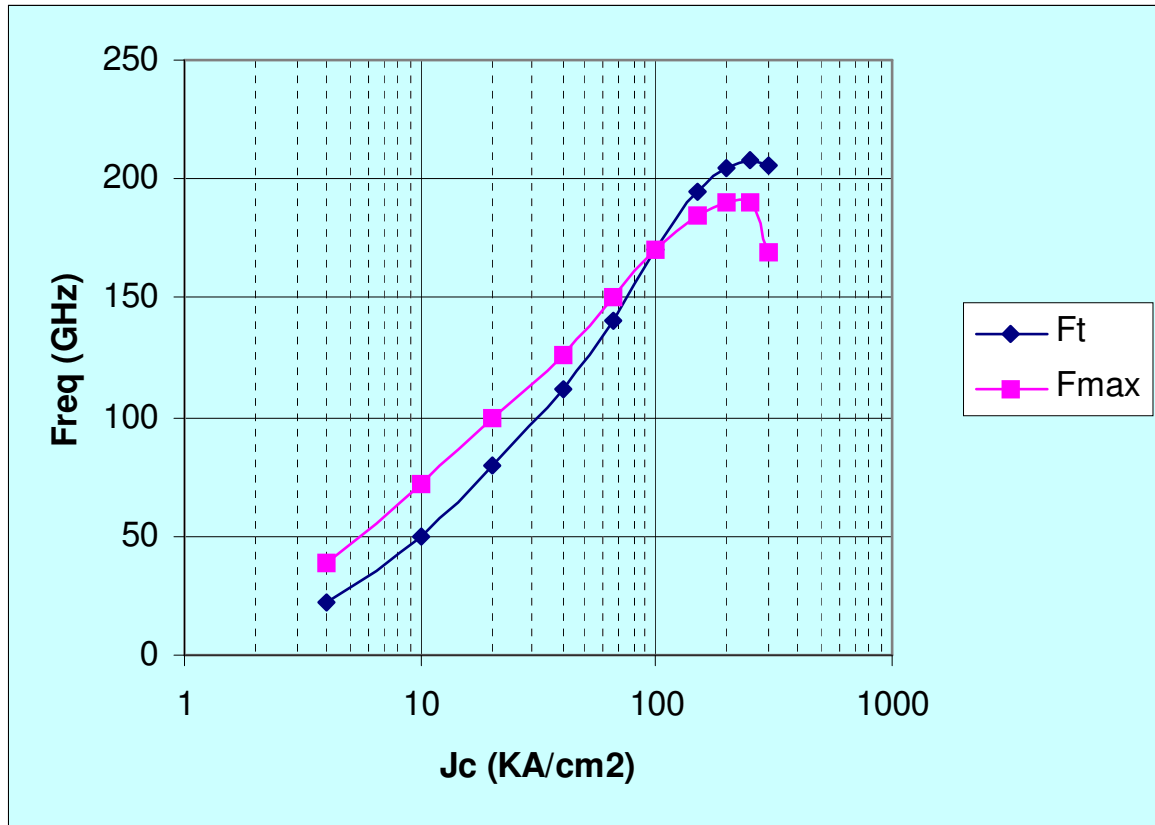
Figure 1.2 InP single HBT Ft and Fmax vary junction current, which were measured at 1x3 μm^2 device and Vce=1V. Devices were manufactured at GCS Inc.
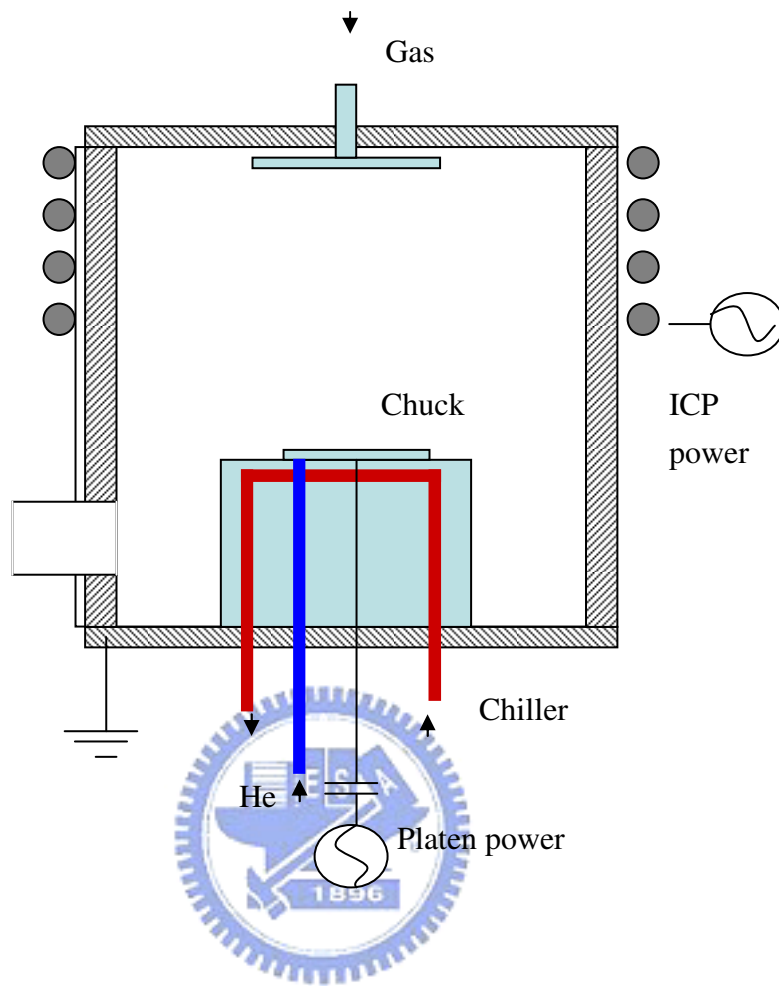
Figure 2.1 A diagram of ICP chamber.
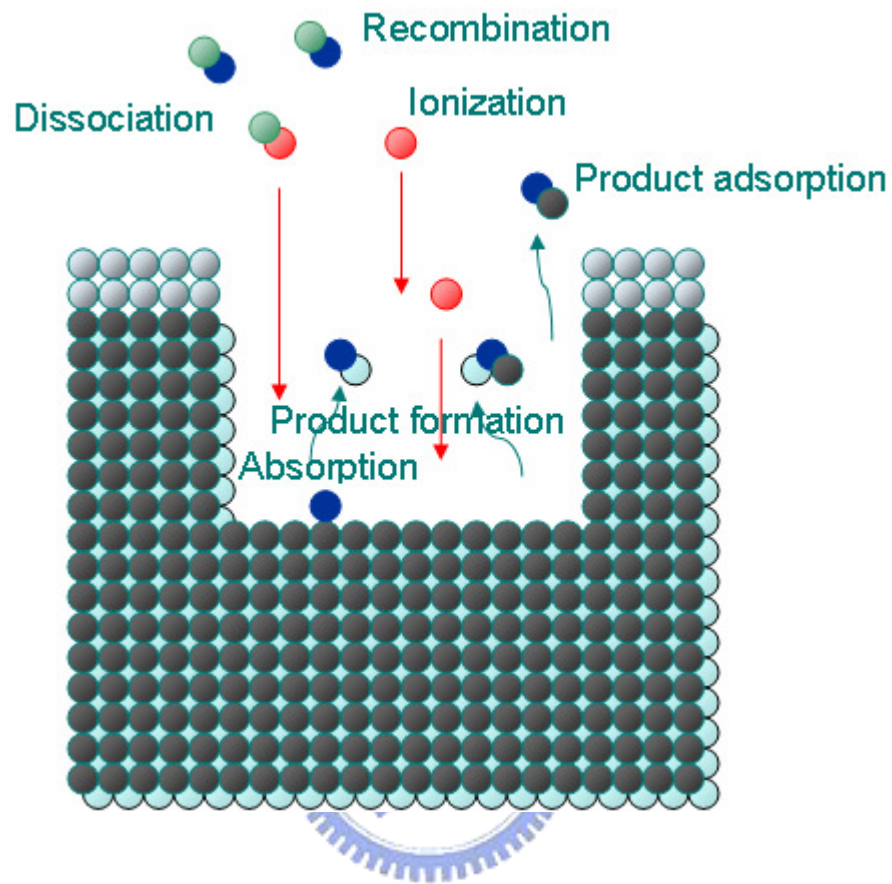
Figure 2.2 A diagram of etching formation mechanism.
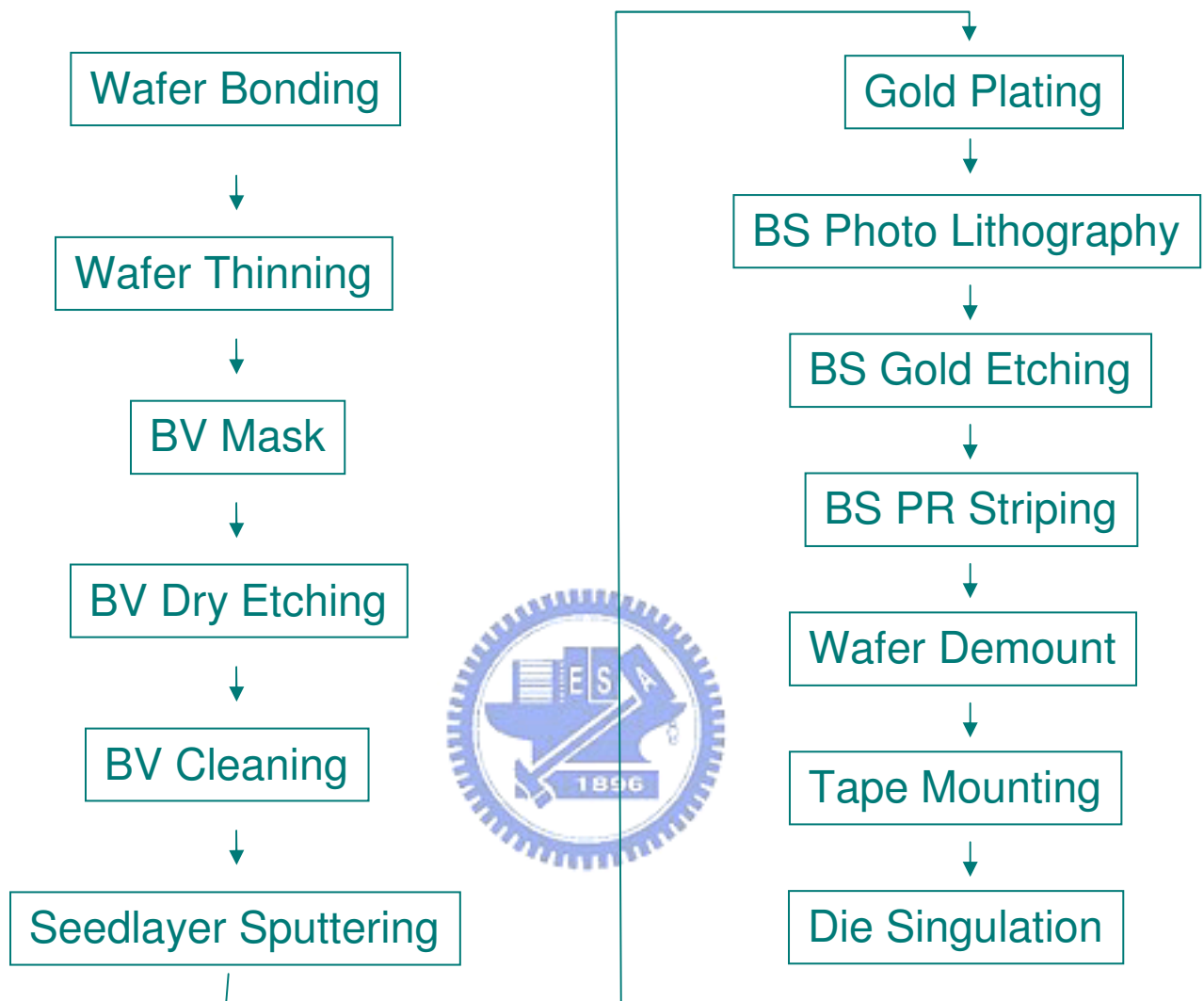
Figure 3.1 Flow chart of the InP wafer backside process.
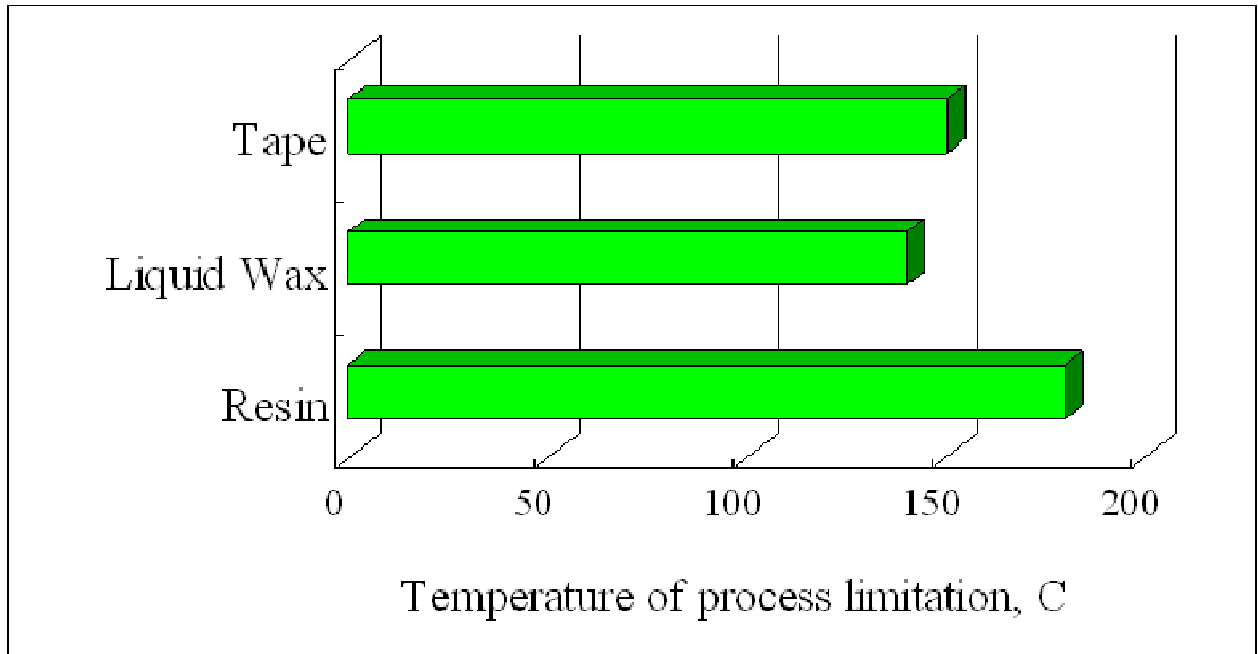
Figure 3.2 Process temperature limitation of current commercial bonding materials in semiconductor industry.
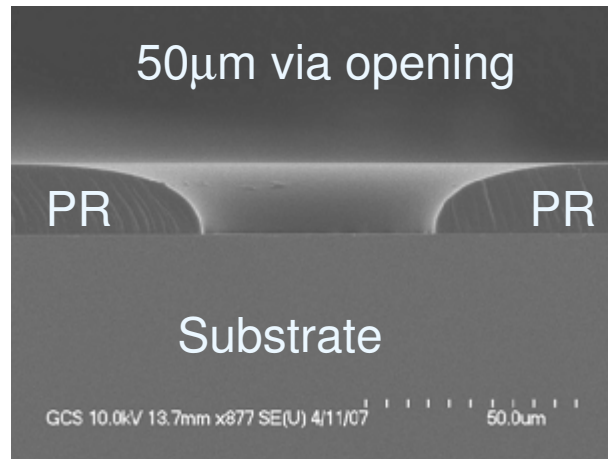
(a)
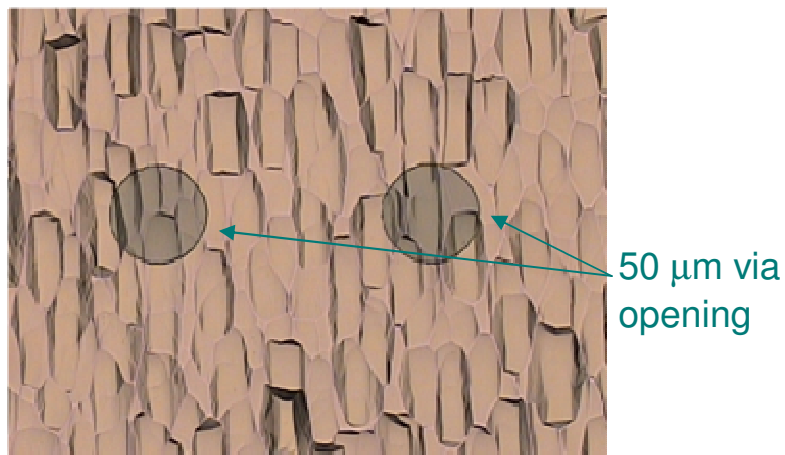
(b)

Figure 3.3 (a) Photoreisist mask thickness is 17 µm, which was done by using single coating and photolithography processes. (b) Ni mask, the pattern was defined by wet etching process on thinned InP substrate.
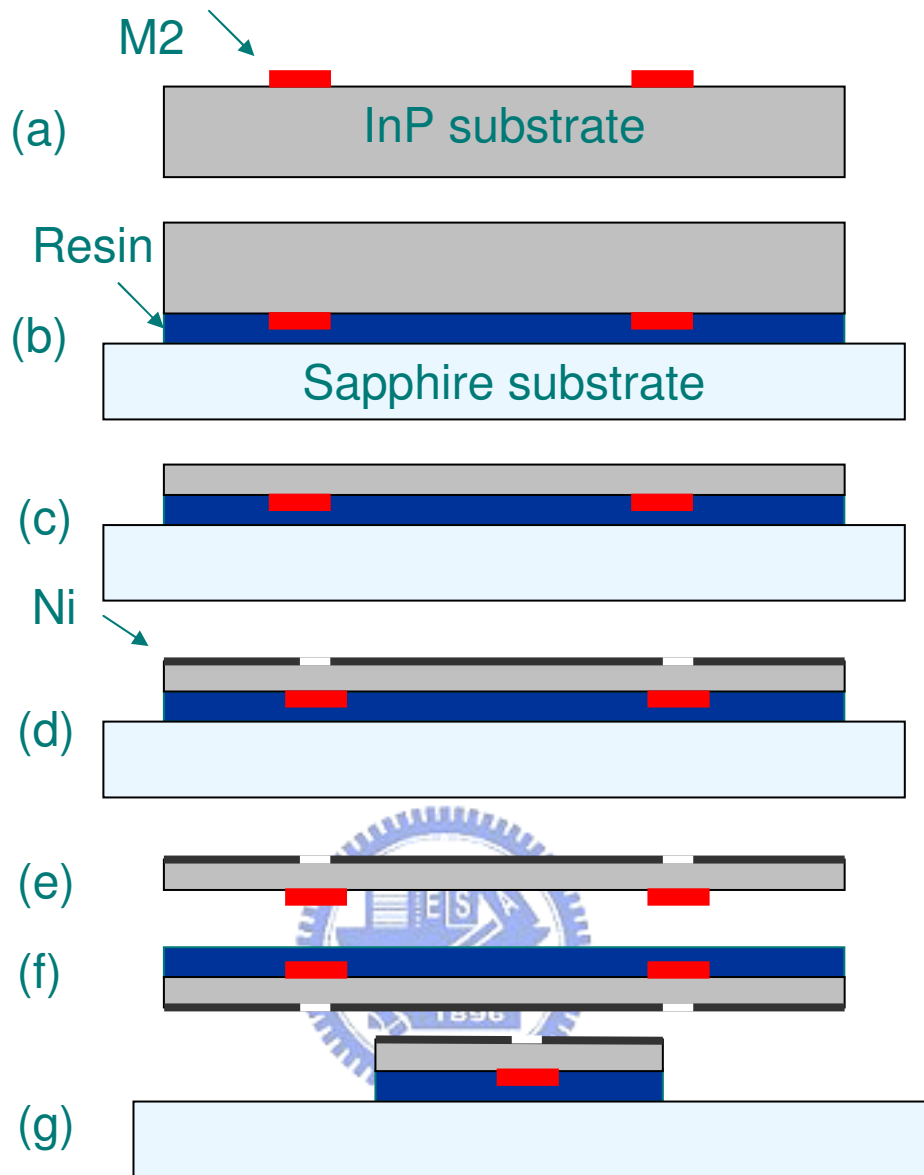
Figure 3.4 Specimen preparation flow.
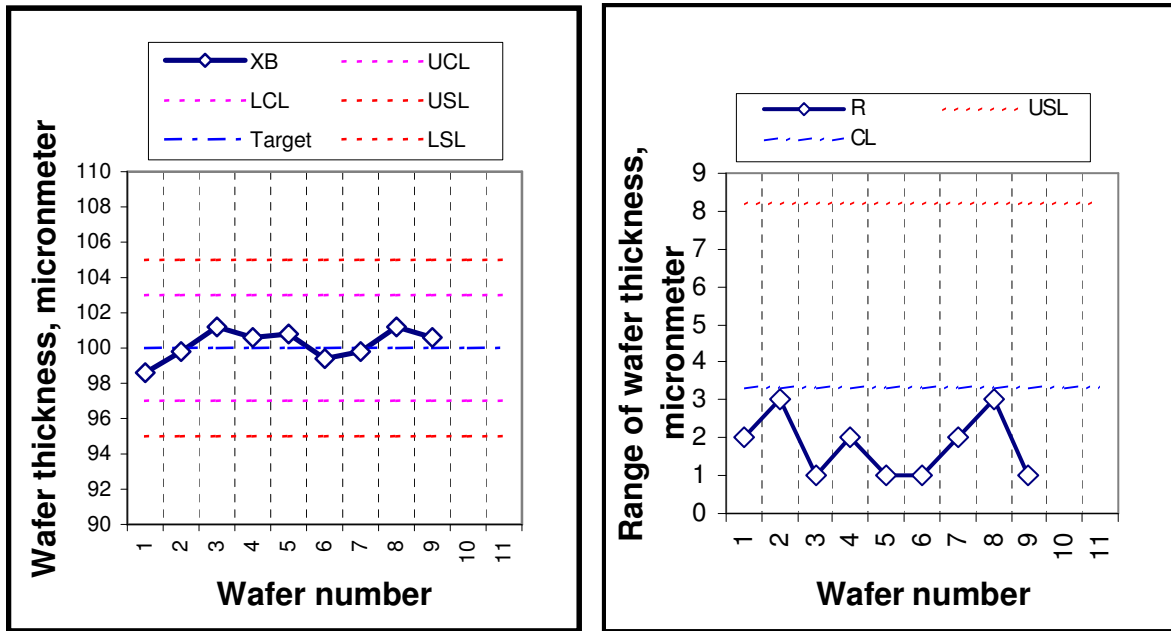
Figure 4.1 The result of wafer substrate thickness after thinning that can be controlled within +-5µm and its Cpk is 1.33.
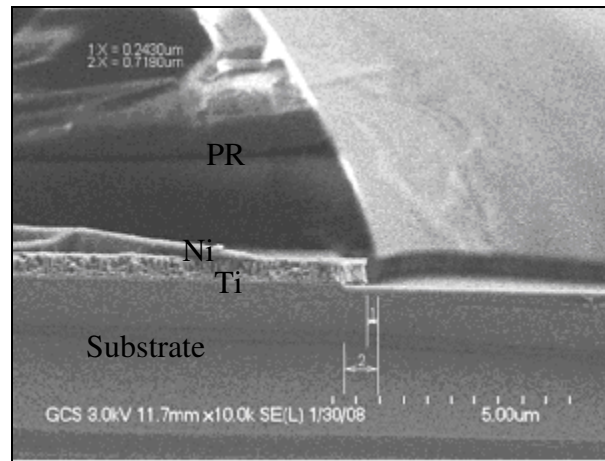
Figure 4.2 SEM micrograph of the Ni undercut is 0.24 μm and
Ti is 0.72 μm, respectively.
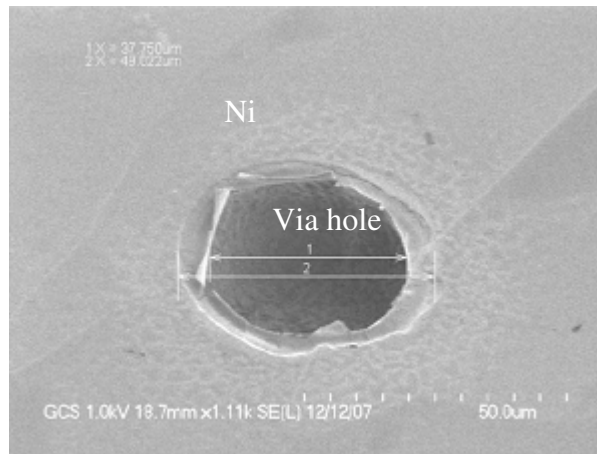
(a)
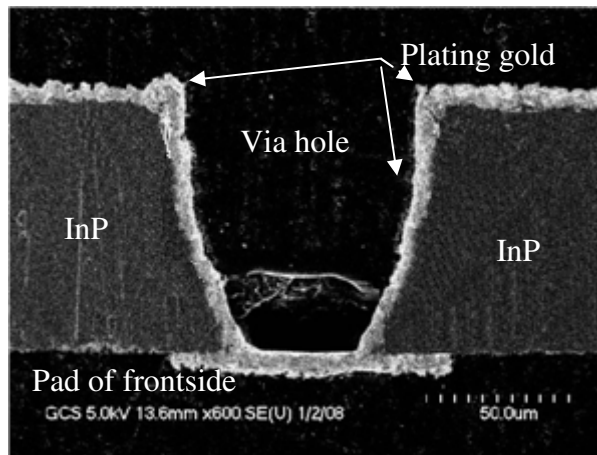
(b)

Figure 4.3 (a) Top view of 40 µm via was etched and 10µm undercut was obtained when the etching depth is 50 µm. Ni mask was wrinkled. (b) Cross section result at 50 µm via which substrate thickness is 100µm.
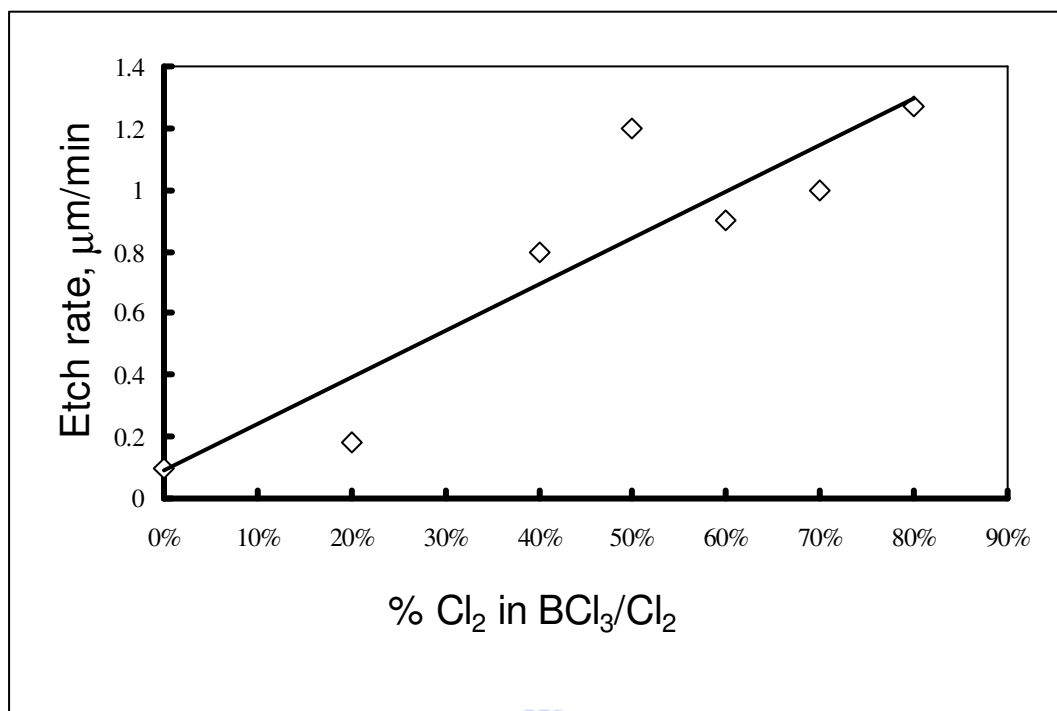
Figure 4.4 Etching rate as a function of platen power at the condition of ICP power was 900 W, platen power was 150 W and the chuck temperature was 140 ℃

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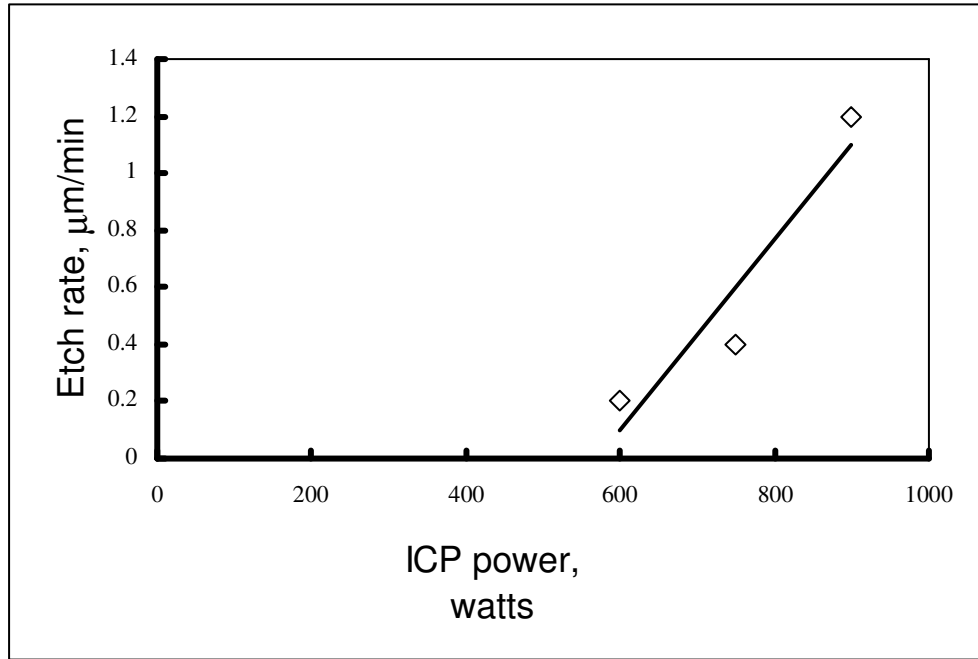
Figure 4.5 (a) Etching rate of InP v.s. ICP power. Specimens were etched at BCl_3/Cl_2 plasma ($BCl_3:Cl_2$ =160 sccm/160 sccm), platen power was 150 W and the chuck temperature was 140 ℃ .
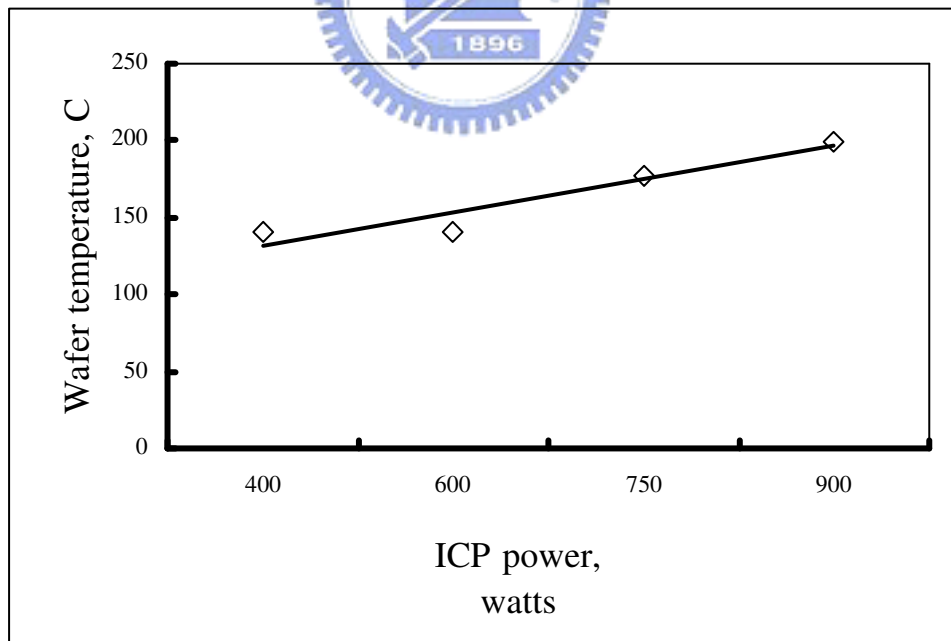
Figure 4.5 (b) Wafer temperature as a function of ICP power.
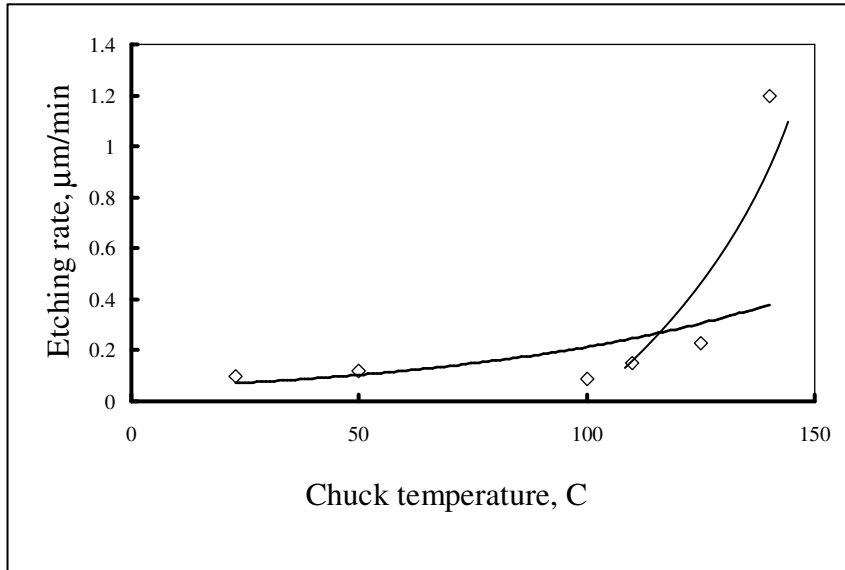
Figure 4.6 (a) Etching rate as a function of chuck temperature at the condition of BCl3:Cl2 =160 sccm/160 sccm, ICP power was fixed at 900 W, platen power was 150 W.
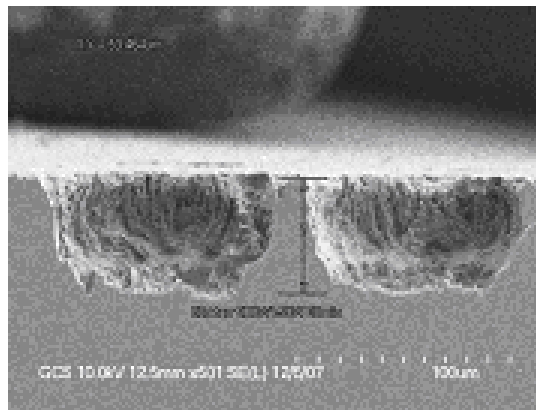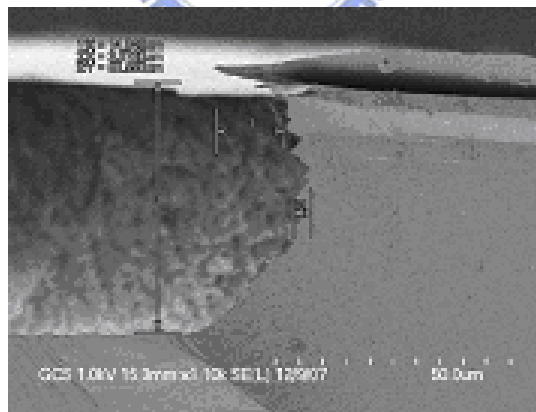
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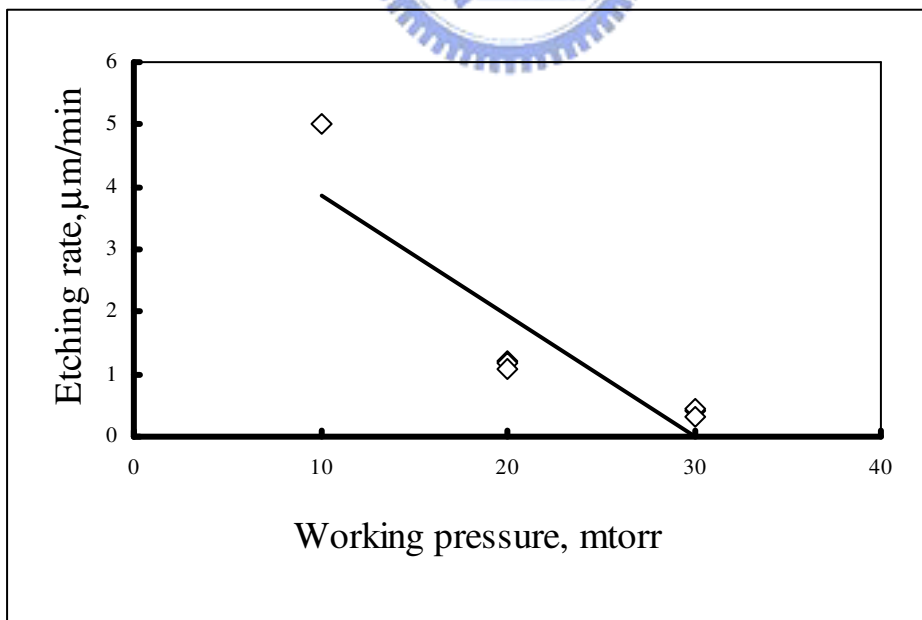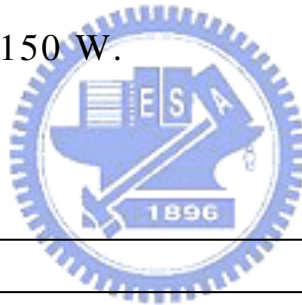
Figure 4.6 (b) Etching rate as a function of working pressure.
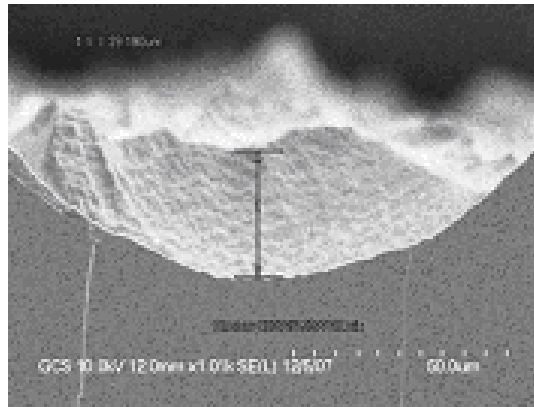
(a) 10 mtorr. Ni and the substrate with Ni protected were etched. The via profile tends to V shape.
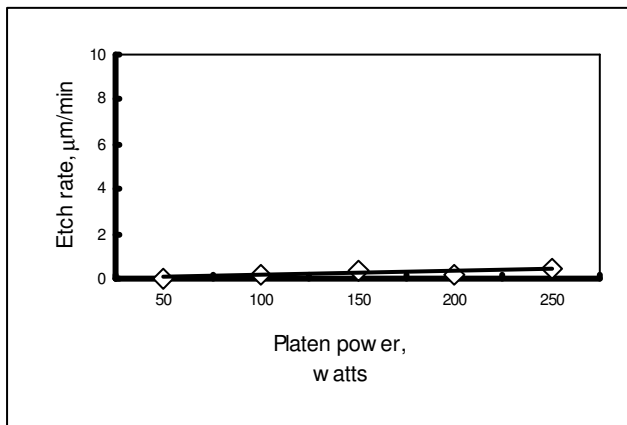

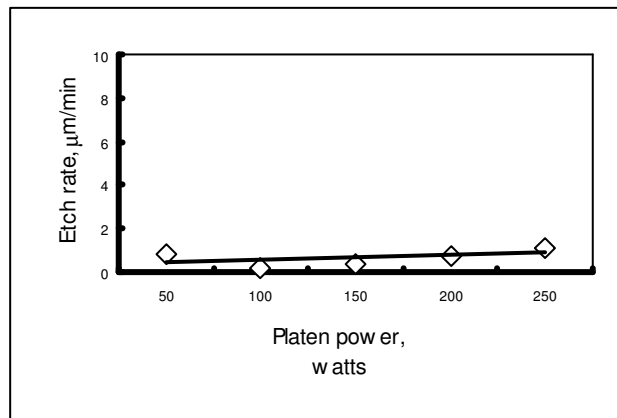(b) 20 mtorr. The via profile tends to vertical.

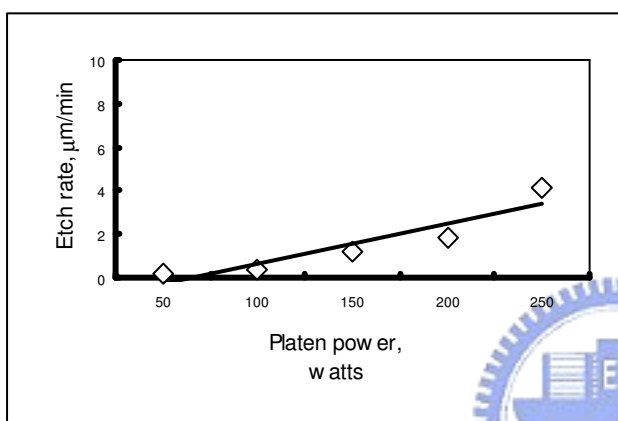(c) 30 mtorr. The via profile tends to bow shape.

Figure 4.7 SEM micrograph of via profiles when were etched under different working pressures, 10 mtorr, 20 mtorr and 30 mtorr.
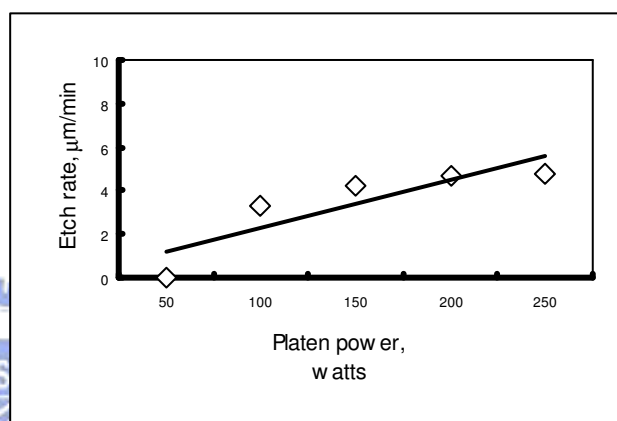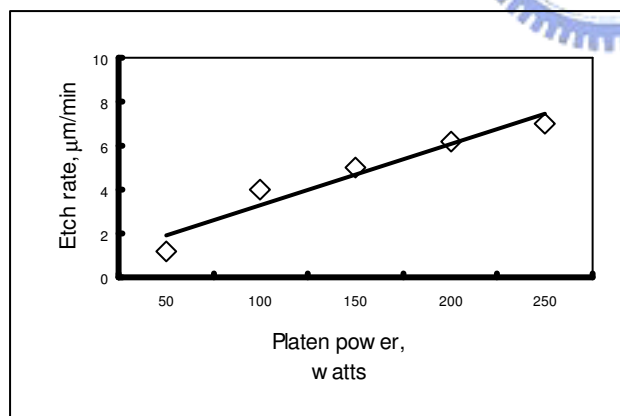
(a) 30 mtorr

(b) 25 mtorr

(c) 20 mtorr

(d) 15 mtorr

(e) 10 mtorr

Figure 4.8 Etching rate as a function of the platen power st the condition of $BCl_3:Cl_2=160$ sccm/160 sccm, ICP power was 900 W, chuck temperature was 140 ℃
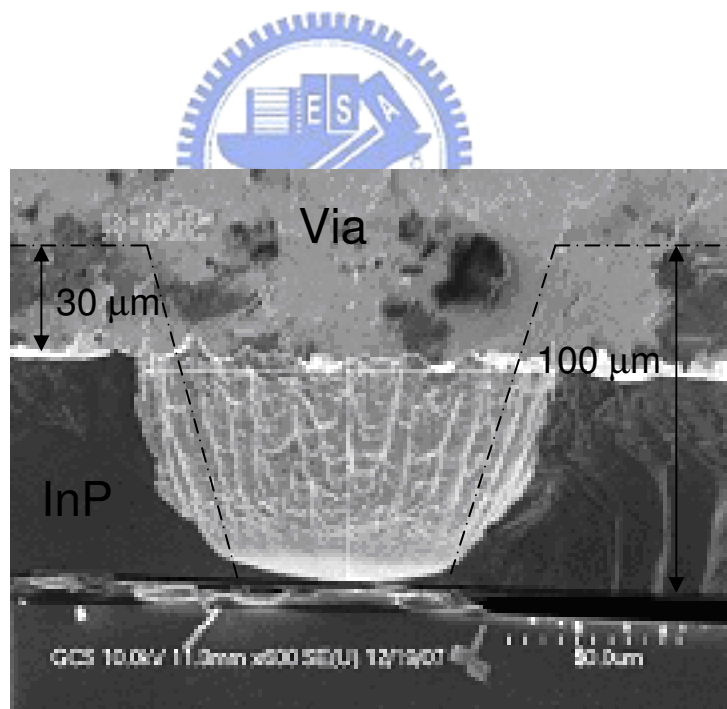
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Figure 4.9 Shows the hard mask Ni was completely etched
away during etching process and the InP substrate was over
etched about 30 µm. This is a tradeoff situation that we can't
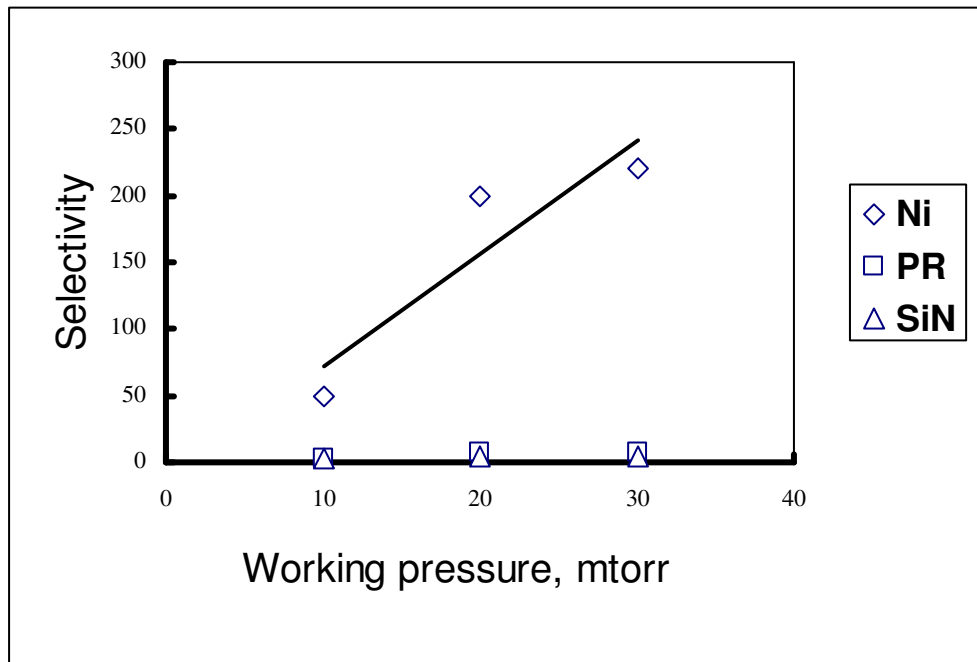keep higher etching without the good electivity.

Figure 4.10 Selectivity of Ni, photoresist and low temperature nitride.
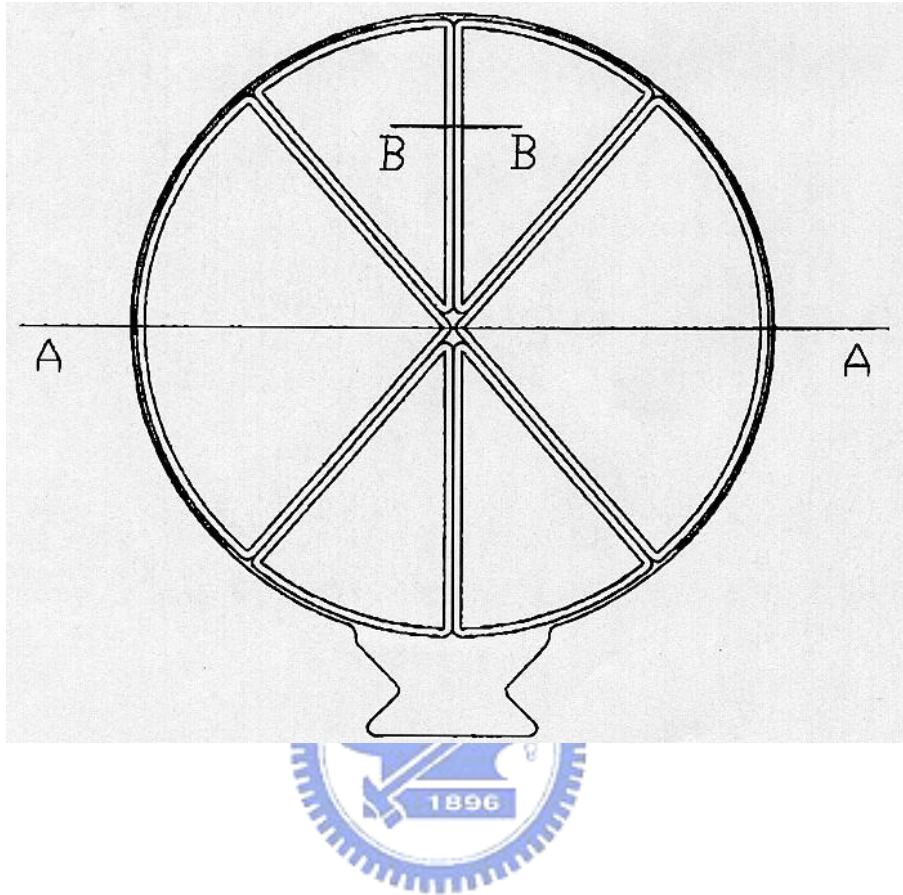
Figure 4.11 Photograph of the thinned wafer demount fixture, the ROC patent application number is 208854.
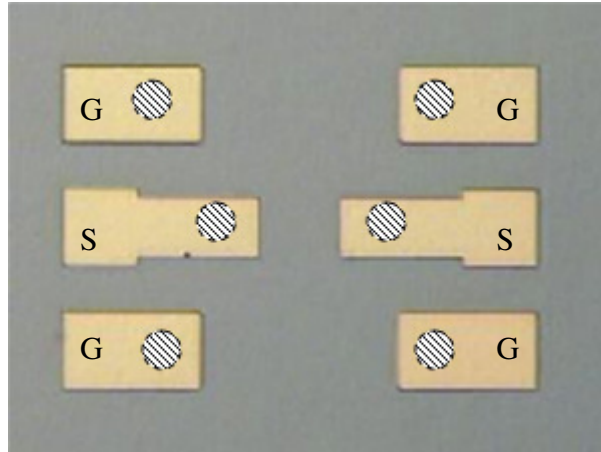
Figure 4.12 Backside via inductance test pattern.
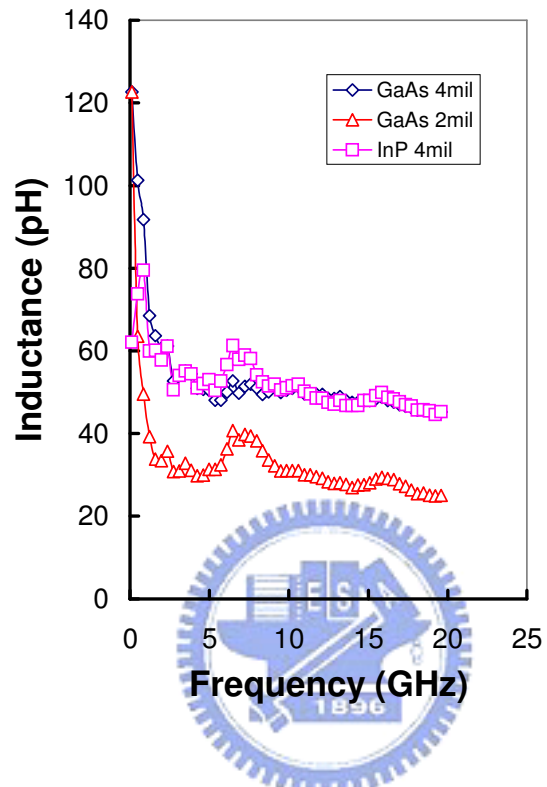
Figure 4.13 GaAs 2 mil, GaAs 4 mil and InP 4 mil backside via inductance measurement result.

Material	Mobility, u kcm2/Vs	Electronic Velocity, Vd E7 cm/s	Energy gap, Eg
Silicon	1	~1	1.12
Ge	2	~1	0.66
GaAs	5	1~2	1.42
In0.53Ga0.47As	10	~3.5	0.7
InAs	25	5.0	0.36
InP	3	3.5	1.35

Table 1.1 Electrical properties of Si- GaAs- and InP- Based semiconductors.

	Melting Point, ℃	Boiling Point, ℃
GaCl$_3$	78	201
AsCl$_3$	-16	130
InCl	225	608
InCl$_2$	235	550~570
InCl$_3$		583
PCl$_3$	-111	76
NiCl$_2$	1001	993
InBr	285	656
InBr$_3$	435	371
NiBr$_2$	965	

Table 2.1 List of the melting point, Mp and boiling point, Bp at Ni, GaAs and InP halides.

Mass numbers	Species	Mass numbers	Species
31	P^+	112,114	$PBCl_2^+$
35	Cl^+	118,120,122	BCl_3^+
41,43	PB^+	124	P_4^+
46,48	BCl^+	136,138,140,142	PCl_3^+
62	P_2^+	149	$PBCl_3^+$
66,68	PCl^+	161,163	$InBCl^+$
77,79	$PBCl^+$	187,189	$InCl_2^+$
81,83,85	BCl_2^+	198,200	$InBCl_2^+$
93	P_3^+	220,222,224,226	$InCl_3^+$
101,105	PCl_2^+	231,233,235,237	$InBCl_3^+$

Table 2.2 Dissociation species and mass numbers at BCl_3/Cl_2 plasma when etching InP materials. The by-products and etchants for plasma etching of InP were determined using a mass spectrometer.

Factor	Example	Effect on
Heating	Ions, chuck	Acceleration of etch rate, isotropy
Contamination	Ni	Form inhibitors, anisotropy
Sputter Redeposition		Grass formation

Table 2.3 Some side effects that are nearly unavoidable in all etching processes and they can either be beneficial or harmful.

Items	Description of requirement	Materials
Bonding Material	Higher melting temperature. Higher chemical resistance.	Resin Wax Tape
BV Mask	Easy to produce. Higher selectivity to InP. Easy to remove bi-products.	Photoresist DFR, dry film resist Metal Nitride
Carrier	Similar thermal expansion. Higher chemical resistance. Good thermal conductivity.	Sapphire SiC

Table 3.1 Challenge of ICP etching process.

Material	Linear Thermal Expansion, 10-6 /°C	Thermal conductivity, W/ cm°C	Chemical Resistance
InP	4.6	0.68	Good
SiC	4.0	1.2	Good
Glass	9.0	1.05	Good
Pyrex	4.0	1.00	Good
Quartz	0.6	3.00	Good
Sapphire	4.5	0.42	Good

Table 3.2 Thermal Properties of InP, SiC, glasses and Sapphire materials.