國立交通大學

電機學院微電子奈米科技產業研發碩士班

碩 士 論 文

新穎元件結構之衰退機制分析

A Study of HC-TFTs Degradation under HC Stress

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摘　要

過去這些年來，多晶矽薄膜電晶體(poly-Si TFTs)在主動式液晶顯示器(AMLCD)和主動式有機電激發光二極體(AMOLED)的週邊電路整合應用上皆備受矚目。相較傳統的非晶矽薄膜電晶體，低溫多晶矽擁有較優的電子遷移率。由於整體製程溫度低於 600^0 C，低溫多晶矽可以廣泛應用在便宜的玻璃基板上。綜合上述的優點，使得低溫多晶矽被用於整合畫素電路及週邊驅動電路上。如果可以進一步提昇低溫多晶矽的電流驅動能力，這個技術將會是實現系統化面板(System On Panel)的關鍵。然而，應用在驅動電路上的電晶體是操作在高頻率交流電壓的環境下。因此，除了直流電壓操作的衰退機制外，在交流電壓操作下所產生的衰退機制也是值得去關注跟探討的。

在本篇論文中，我們提出了一個新穎的元件結構，用來觀測元件的衰退機制。這個新穎的元件結構主要是在傳統結構通道的垂直方向額外做了三副的源極/汲極。藉由對此新穎元件結構施加不同的交流/直流應力，我們便可進一步去分析在通道上不同區域的衰退機制。

A Study of HC-TFTs Degradation Under HC Stress

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Abstract

Polycrystalline silicon (poly-Si) thin film transistors (TFTs) have received lots of attention in past years for their capability in integrating pixel elements and driver circuits together on the same substrate for active matrix liquid crystal displays (AMLCDs) and active matrix organic light emitting diode (AMOLED) displays. The electron mobility of low-temperature poly-Si thin-film-transistors (TFTs) is much larger than that of the conventional amorphous silicon TFTs. By limiting the maximum processing temperature to lower than 600^0 C, poly-Si TFTs can be fabricated on a wide variety of cheap glasses. Taking advantage of these features, poly-Si TFTs are used both as pixel TFTs and driver circuits. If the mobility of poly-Si TFTs could be further increased, this technology will become attractive for

the realization of system on panel (SOP) that will integrate memory, CPU, and display altogether. However, unlike pixel TFTs, TFTs in driver circuits are subjected to high-frequency voltage pulses. Therefore, the degradation mechanism under dynamic operation should be understood in detail as well as the degradation mechanism under static operation.

In this study, a novel thin-film transistor test structure, called HC-TFT, is proposed for monitoring the device hot-carrier (HC) degradations. This new test structure consists of three source/drain electrode pairs arranged in the direction perpendicular to the normal (i.e., lateral) channel of the test transistor. By applying such tester to hot-carrier stressing, the relationship between different stages of the input signal and resultant damage location can be established.

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Chapter 1
Introduction

1.1 An Overview of Low-Temperature Polycrystalline Silicon Thin Film Transistors (LTPS TFTs)

In recent years, polycrystalline silicon thin-film transistors (poly-Si TFTs) have drawn much attention because of their wide applications to active matrix liquid crystal displays (AMLCDs) [1], and organic light-emitting displays (OLEDs) [2]. In addition to large area displays, poly-Si TFTs also have been applied to memory devices such as dynamic random access memories (DRAMs) [3], static random access memories (SRAMs) [4], electrical programmable read only memories (EPROM) [5], electrical erasable programmable read only memories (EEPROMs) [6], linear image sensors [7], thermal printer heads [8], photo-detector amplifier [9], scanner [10], neutral networks [10]. Lately, superior performance of poly-Si TFTs also has been reported by scaling down device dimension or utilizing novel crystallization technologies to enhance poly-Si film quality [11], [12]. This provides the opportunity of applying poly-Si TFTs to three-dimension (3-D) integrated circuit fabrication. Of course, the

application to AMLCDs is the primary trend, leading to the rapid development of poly-Si TFT technologies.

Traditionally, AMLCDs were fabricated using hydrogenated amorphous silicon (a-Si:H) TFTs as the pixel switching devices [13]. The a-Si:H TFTs have many advantages, particularly its compatibility with low temperature process on large glass substrate and high off-state resistivity which results in a low leakage current. However, the low electron field effect mobility in a-Si:H TFTs has limited the technology development for AMLCDs application. To integrate the switching elements with the driving circuits on the same substrate is very desirable not only to reduce the cost but also to improve the system performance. In line of this, poly-Si TFTs, which provide higher electron field effect mobility, have been developed as a substitute for a-Si:H TFTs. Besides, poly-Si TFTs have other advantages such as CMOS capability and better reliability [14], thus enabling the integration of peripheral circuits as well as the active-matrix switching elements on the same substrate.

Actually, the effective carrier mobilities in poly-Si are significantly higher than those in amorphous-Si, so that both n-channel and p-channel devices with reasonably high drive currents can be achieved in poly-Si [15]. The higher drive current allows smaller TFTs to be used as the pixel-switching elements, resulting in higher aperture ratio and lower parasitic gate-line capacitance for improved display performance [16].

In addition, the capability of fabricating complementary metal- oxide-semiconductor (CMOS) circuits allows low-power driver circuitry to be integrated with the active matrix in order to reduce display-module cost and improve reliability [17].

Previously, poly-Si TFT technology was primarily applied to small, high-definition LCD panels for projection display systems, because the high processing temperature typically required made it incompatible with commercially available large-area glass substrates and necessitated the use of quartz substrates. In recent years, however, rapid progress has been made in the development of fabrication processes which are compatible with glass substrates and also in the improvement of process-module throughput, so that the cost-effective manufacture of LTPS TFT AMLCDs and AMOLEDs on large-area substrates now becomes feasible.

Recently, more and more researches have been made to develop various technologies for improving the performance and reliability of LTPS TFTs. Crystallization of a-Si thin films has been considered the most important process for fabricating high-performance LTPS TFTs. Among various crystallization technologies, excimer laser crystallization (ELC) has become the mainstream technology for mass production of flat panel displays (FPDs) because of high throughput, low temperature process compatible with glass substrates, and the formation of high-quality poly-Si [18]. However, other low-temperature process technologies in the procedure of

fabricating LTPS TFTs, such as gate dielectric formation, ion doping/dopant activation, defect passivation, thin film deposition, lithography, and etching, are also indispensable for producing high-performance LTPS TFTs [19].

The modification of process procedure for reducing fabrication cost and enhancing TFT performance is another issue in the fabrication of LTPS TFTs on large-area glass substrates. Self-aligned processes are very attractive for advanced circuit systems on large-area glass substrates, while reducing masks and process steps can effectively promote production yield and reduce fabrication cost. In addition, various device architectures, which are different from the conventional self-aligned source/drain structure, have also been adopted to enhance TFT performance and reliability, such as offset gate [20], [21], lightly doped drain (LDD) [22], [23], multi-gate structure [24], gate-overlapped LDD [25]-[27], and so on. Most of these structures effectively reduce the electric field near the drain junction. Consequently, the anomalous leakage current and kink effect in poly-Si TFTs can be effectively reduced, accompanying with a promotion of reliability in poly-Si TFTs.

1.2 Electrical Characteristics of Poly-Si TFTs

In comparison with single-crystalline silicon, poly-Si is rich in grain boundary defects as well as intra-grain defects, and the electrical activity of these

charge-trapping centers profoundly affects the electrical characteristics of poly-Si TFTs. The turn-on characteristics, such as threshold voltage, substhreshold swing, and field-effect mobility, of poly-Si TFTs are much inferior to those of single-crystalline silicon counterparts due to the abundance of defect states in the device active region. Devices whose channels have more defects simply require larger gate voltage in order to fill the greater number of traps before the device can turn on. Carrier mobility is degraded by scattering with charge-trapping centers and surmounting the potential barrier height which is built by charged traps [28].

An anomalous high leakage current has also been found in poly-Si TFTs, and the dominant leakage current mechanism is identified as the field emission via the traps by high electric field near the drain junction [29]-[31]. In addition to reducing the defect density, another approach to reduce the anomalous high leakage current is to adopt drain- field-relief structures, such as LDD and offset gate structure.

The floating-body architecture and charge trapping by defect states result in serious avalanche induced effects in poly-Si TFTs [32]. Due to impact ionization occurring in the high electric field region at the drain end of the channel, holes are injected into the floating body forcing further electron injection from the source, which are then collected by the drain. This added drain current augments impact ionization which, in turn, forward-biases the floating body harder, thereby causing a

regenerative action which leads to a premature breakdown. As a result, the output characteristics exhibit an anomalous current increase in the saturation regime, and such a phenomenon is often called “kink” effect [33].

The avalanche induced effects become more severe as the TFT size is reduced due to the enhancement of impact ionization caused by the increased electric field. Therefore, more severe short channel effects are shown in poly-Si TFTs compared with the single-crystalline silicon counterparts, including significant threshold voltage shifts and degradation in drain breakdown voltage as the gate length decreases [34], [35].

Since the defect traps place a profound influence on electrical characteristics of poly-Si TFTs, the most effective approach to improve the performance of poly-Si TFTs is to reduce the defect traps by promoting the quality of poly-Si thin films. The other important work is to reduce the undesirable effects, which result from the high drain electric field and floating body of poly-Si TFTs, by modifying the architecture of poly-Si TFTs.

1.3 Reliability Issues in LTPS TFTs

The stability of device characteristics under long-term operation is important for

circuit applications. So the reliability of LTPS TFTs must be taken into consideration before they can be applied to advanced circuitry such as data-driver in AMLCDs or driving elements in AMOLEDs. The special processes used in the fabrication of LTPS TFTs and the intrinsic properties of crystallized poly-Si make the reliability issues in LTPS TFTs different from those in the conventional MOSFETs.

The gate oxide used in LTPS TFTs is generally deposited at low temperature by CVD methods. Consequently, it always exhibits poorer physical and electrical quality, such as lower density, higher gate leakage current, and lower breakdown field, compared with high-temperature thermally-grown oxide used in single-crystal MOSFETs. In addition, the mobile ions, Si-H and/or Si-OH bonds, as well as fixed charges existing in low-temperature deposited gate oxide are also the potential causes of instability of LTPS TFTs [36]-[40].

In general, crystallized poly-Si is full of weak strain Si-Si bonds and dangling bonds. Besides, the hydrogenation process also creates a large amount of weak Si-H bonds in poly-Si. These weak bonds can easily be broken during device operation, and result in the shift of device characteristics [41], [42].

As the glass substrate is a poor thermal-conducting media, heat generated during device operation is hard to dissipate. Consequently, the device temperature can rise to a degree which causes bonds breaking, or even burns out the device. Such a

phenomenon is called “self- heating”. The degradation rate caused by self-heating depends on the operation power and the capability of heat dissipation of the device. In general, wide-channel TFTs and/or small-size TFTs suffer from serious self-heating [43]-[46].

The surface roughness of poly-Si resulting from laser crystallization will enhance the local electric field near the interface between gate oxide and poly-Si channel, which will also degrade the reliability of TFT under high gate bias operation.

The hot carrier effects which originate from high electric field near the drain junction have been widely investigated in MOSFETs. Meanwhile, it also represents another important reliability issue in LTPS TFTs. Conduction carriers can obtain energy from the high electric field and become “hot”. And then these high-energy carriers can easily break weak bonds existing in poly-Si, creating lots of defect states and oxide charges. Serious degradation can be generated in the hot carrier operation mode, and the degree of degradation depends on the strength of electric field, that is, the energy of the hot carriers. Generally, introducing electric-field-relief TFT structures, such as LDD, offset drain, and gate-overlapped LDD, can reduce the hot carrier degradation.

1.4 Motivation

With the improved channel mobility, the hot-carrier (HC) degradation represents one of the most critical reliability concerns in poly-Si TFTs. Therefore, reliability testing and understanding of reliability mechanisms become more and more important.

Hot carriers are generated during normal device operation by the high-electric field existing near the drain site. Charge trapping in the oxide and the creation of interface states would occur and lead to device degradation. As compared with the bulk CMOS counterparts, the situation becomes even more complicated for poly-Si TFTs owing to the lack of substrate contact in typical device configuration, as well as the large amount of potential defect sites existing at the grain boundaries.

In the past, a lot of research efforts (i.e., Maeda, Khamesra, Uraoka, Hastas, Moon et al.) have been made to study the degradation mechanism of static operation. In recent years, there were researches (i.e., Toyota, Uraoka et al.) made to investigate the degradation mechanism of dynamic operation in recent years. Even so, it is still hard to resolve and understand the detailed mechanisms responsible at different portions of the stressed channel.

In this study, a novel test structure for spatially resolving the non-uniform damage

of HC stress was employed to investigate the HC degradation caused by DC/AC stress. The characteristics of such structure under various stress conditions, including gate/drain/source voltage, stressing time, frequencies, swing range, and falling/rising times, were discussed to verify the degradation mechanism under DC/AC stress.

1.5 Thesis Organization

This thesis is divided into four chapters. After a brief introduction given in Chapter 1, we describe the fabrication of the novel HC-TFTs device structure In Chapter 2. In addition, we also give a brief description about the DC stress definition and the degradation mechanism of DC stress in the same chapter. We conclude Chapter 2 by presenting and analyzing the results of the characteristics of HC-TFTs under various DC stress conditions.

In Chapter 3, we first give a brief description about the AC stress definition and the degradation mechanism of AC stress. Then we show and analyze the electrical characteristics of HC-TFTs under various AC stress conditions.

Finally, we summarize our conclusion and future work in Chapter 4.

Chapter 2
Device Fabrication and HC-TFTs Under DC Stress

2.1 Experiment

· 2.1.1 Device Fabrication of HC-TFTs

In this study, the channel was prepared by solid-phase crystallization (SPC) method in which an amorphous Si deposited on oxidized Si wafers was annealed at 600 °C in N_2 for 24 hours. A 35 nm-thick TEOS-oxide layer and a 200 nm-thick n^+ poly-Si layer were then deposited and patterned as gate dielectric and gate electrode, respectively. S/D doping was formed by implanting phosphorous ions with a dosage of 5×10^{15} cm^{-3} at 45 keV. After standard processing steps, passivation, and metallization, the test structure further received a plasma treatment in NH_3 ambient at 300 °C for 1 hour.

The top view of the test structure is shown in Fig. 1(a). The test structure is configured with four pairs of n^+ electrodes at the edge of the channel. In Fig. 1(b), one pair of n^+ electrodes is placed along the x (horizontal) direction to form the source and drain (S/D) of the normal (lateral) test transistor that will be subjected to HC stressing.

In Fig. 1(c), the other three pairs are arranged along the y (vertical) direction to form three separate monitor transistors (MTs) to allow spatial characterization of the HC degradations along the channel of the test transistor after stressing. A common gate electrode shared by the test transistor as well as all three MTs is lying over the entire channel. Since each pair of n^+ electrodes could be configured as the S/D of the respective MT, the current–voltage (I–V) characteristics of the corresponding MT could be characterized. The pair of S/D placed along the x-direction that serves to form the test transistor is subjected to HC stressing by applying a high voltage to its drain for inducing the HC degradations in the test transistor. According to their respective location relative to the channel of the test transistor, the three MTs are denoted as the source-side MT (S-MT), central MT (C-MT), and drain-side MT (D-MT), respectively. This unique configuration allows us to resolve the damage and identify the associated mechanisms at different locations along the channel of the test transistor after stressing. Important planar structural dimensions for the test structure characterized in this thesis are detailed in Fig. 1(a).

・2.1.2 DC Stress Conditions

Fig. 2 shows the arrangement of the DC stress condition. The basic parameters of

DC signal consist of gate voltage (V_G), drain voltage (V_D), source voltage (V_S), and stress time.

In this chapter, the static stress is used to degrade the HC-TFTs. The total stress time is 1000 sec.

2.2 Degradation Mechanism in Poly-Si TFTs under Static Stress

Fig. 3 depicts the hot-carrier degradation scheme of Poly-Si TFTs under DC stress. As the impact ionization occurs near the drain site at high drain bias conditions, hot holes and electrons are generated. The injection efficiency into the gate oxide for hot holes and electrons depends on the vertical electric field near the drain and source. The generated hot electrons release their energy inside the channel and at the oxide/channel interface, and could generate defect states and interface states, respectively. In the mean time, since no substrate contact is present in the TFT structure, hot holes generated by the impact ionization during hot-carrier stressing will drift toward the grounded source. Some of them with sufficient energy may surmount the barrier and be injected into the oxide.

2.3 Results and Discussion

Subthreshold characteristics of the lateral test transistor, as shown in Fig. 1(b), were measured before and after DC stress, and the results are shown and compared in Fig. 4. In Fig. 4(a), the test transistor was stressed under high bias of V_G = 9 V and V_D = 18 V for 1000 sec to induce hot-carrier degradations. The degradations in device characteristics in terms of increased subthreshold swing and reduced on-current are indeed observed after DC stress, as can be seen in this figure. The post-stress I_D–V_G shift is more significant when the lateral test transistor was measured at a low drain bias of V_D = 0.1 V after DC stress. Furthermore, an increase in off-current could be detected at V_D = 3 V and V_G = −2 ~ −4 V. The above-mentioned observations are consistent with the well-known consensus that most of the damage events occur in the channel near the drain side of the test transistor. As a larger drain bias was applied during the measurements of subthreshold I_D–V_G characteristics, the depletion region near the drain side would extend. This phenomenon might in turn screen out more defects induced in the channel near the drain side, thus relieving the post-stress I_D–V_G shift. Besides, it is well known that when the DC stress voltages are reduced, the degradation will also reduce. This is shown in Fig. 4(b) where the test transistor was stressed under lower biases of V_G = 6.5 V and V_D = 13 V for 1000 sec. The post-stress

I_D–V_G curve shows only a negligible shift relative to the fresh device under the milder stress condition.

The above-mentioned results of the conventional test transistor provide us the information about the major damage location in the stressed channel and the effect of stress voltages, as is well known in the literature. However, the detailed degradation mechanisms at different sections of the stressed channel could not be resolved by the conventional test structure. Moreover, the conventional test structure is also insensitive in detecting the induced damages while the applied stress voltages are low. To resolve these shortcomings, the subthreshold characteristics of three separate monitor transistors (MTs) in the test structure were measured and the results are shown in Figs. 5 and 6. It is worth noting that the characteristics of the three MTs, as shown in Fig. 5, were measured using the same test structure with its test transistor DC-stressed and measured in Fig. 4(a). It can be seen that among the three MTs, the D-MT shows the worst degradation. Fig. 5(c) shows that the post-stress I_D–V_G shift is very significant even measured at a high V_D bias of V_D = 3 V. This phenomenon indicates that the induced traps are uniformly distributed along the entire channel of the D-MT. And this observation simultaneously confirms the inference drawn above in analyzing the results of Fig. 4(a). However, the remaining S-MT and C-MT exhibit some interesting results that are not explicitly revealed in Fig. 4(a). First, even though

not clearly distinguishable in Fig. 4(b), the C-MT indeed has a slightly degraded subthreshold swing when the measurement data are normalized. This implies that the generation of interface states at the oxide/channel interface is mainly responsible for the degradation. Second, the S-MT shows negative parallel shift in subthreshold characteristics, and this phenomenon indicates that positive hole trapping is preponderant in the oxide near the source side of the test transistor after DC stress. These holes are generated by the impact ionization during the DC stress of the test transistor. Since no substrate contact is present in the TFT structure, these holes would tend to drift toward the grounded source, and some of them with sufficient energy might overcome the barrier and be injected into the oxide, causing positive hole trapping. Based on the results shown in Fig. 5, major degradation mechanisms occurred at different channel sections could be clearly distinguished and identified by the proposed novel test structure.

Fig. 6 shows the subthreshold characteristics of the MTs for the same test structure measured in Fig. 4(b) after stressing the test transistor under lower biases of V_G = 6.5 V and V_D = 13 V for 1000 sec. It can be seen that both S-MT and C-MT exhibit negligible shift in I–V curves after the stress, similar to the result of the test transistor, as shown in Fig. 4(b). By contrast, the D-MT shows obvious performance degradation after the stress. This phenomenon demonstrates the high sensitivity of the test

structure in detecting the hot carrier effects.

Chapter 3
HC-TFTs Under AC Stress

3.1 AC Stress Conditions

Fig. 7(b) shows the waveform of the AC signal. The basic parameters of AC signal consist of frequency (Freq.), signal high level (V_{G_high}), signal low level (V_{G_low}), high-level time (T_{high}), low-level time (T_{low}), rising time (T_r), falling time (T_f), and duty ratio.

Under AC stress, a pulse voltage is applied to the gate electrode by 8110A pulse generator, source is grounded and a high bias is applied to the drain, as shown in Fig. 7(a). T_r (rising time) is the time that voltage signal rises from 10% to 90% of the amplitude (V_{G_high} – V_{G_low}), while T_f (falling time) is the time that voltage signal falls from 90% to 10% of the amplitude (V_{G_high} – V_{G_low}). The total stress time is the summation of T_{high} under the stress condition. The standard AC stress condition in the experiment is the gate voltage swing of 6.5 V to 0 V or 13 V to 0 V, the drain voltage of 13 V, frequency of 500 kHz, T_r and T_f of both 100 ns, duty ratio of 50%, and the total stressing time of 1000 sec. By changing these parameters, we can perform various stress conditions to test the reliability of HC-TFTs, and further

analyze the detailed degradation at different portions of the stressed channel by the new structure.

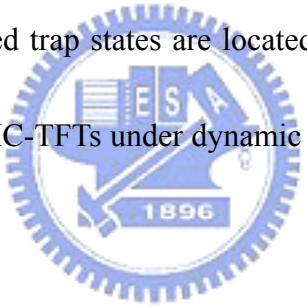
In this study, we first change the frequency from 100 kHz to 1000 kHz. Then, we change T_r from 100 ns to 10 ns. Finally, we change T_f from 100 ns to 10 ns.

3.2 Degradation Mechanism in Poly-Si TFTs under Dynamic Stress

Fig. 8 shows a schematic diagram for degradation model of the poly-Si TFTs under dynamic operation. When a high voltage is applied to the gate, the device turns on and is operating in ON state. The electrons gather to form a channel and the damage can be attributed to impact ionization stress, as shown in Fig. 8(a). In addition to the on-state hot-carrier degradation, the testers receive transient hot-carrier stressing when elections move rapidly from the inversion layer to the drain, as shown in Fig. 8(b). When the gate voltage falls, the electrons in the channel move rapidly to the drain, according to the Fermi energy level at the SiO_2/poly-Si interface. In the case of a slow falling time, most electrons have enough time to be swept to the drain while the gate voltage falls from high to V_{th}. Thus, less electrons would be affected by the electric field at the channel/drain interface and less electrons are turned into hot

electrons to damage the drain side while the gate voltage falls from V_{th} to 0 V. In the case of a short falling time, more electrons do not have enough time to be swept to the drain while the gate voltage falls from high to V_{th}. They remain in the channel, taking into account the electron mobility in the channel, and are swept out while the gate voltage falls from V_{th} to 0 V. As mentioned above, the electric field at the channel poly-Si layer/drain interface becomes high, and the electrons gain energy from the electric field to become hot carriers. Therefore, more hot electrons are generated and cause traps in the grain boundaries near the drain regions in poly-Si in the latter case.

Since most of the generated trap states are located near the drain side of the test transistor, the degradation in HC-TFTs under dynamic stress can be easily detected by D-MT, as shown in Fig. 8(d).



3.3 Results and Disccusion

・3.3.1 Frequency

The tester was first stressed under the stress conditions of V_{G_high} = 6.5 V, V_D = 13V, Freq. = 100 kHz, $T_r = T_f$ = 100 ns, and duty ratio = 50%. Fig. 9 shows I_D-V_G curves of TT, S-MT, C-MT and D-MT before and after 1000-sec AC stress, respectively. For Conventional TFTs, as shown in the I_D-V_G curve in Fig. 9(c), the

hot-carrier degradation is so minor and difficult to detect. In this study, we divide the channel into three parts, and measure the different portions of the channel as Figs. 9(a), (b), and (d) in order to resolve the degradation mechanisms occurred at these three different channel sections. In Figs. 9(a) and (b), S-MT and C-MT exhibit negligible degradation in the I_D-V_G curves after AC stress. However, in Fig. 9(d), D-MT shows a clear and obvious degradation in both subthreshold swing and ON current. As described previously in Chap 3.2 about the degradation mechanism under AC stress, most of the generated trap states are located near the drain side of the lateral TT, and can be easily detected by D-MT, as shown in Fig. 8(d).

Under the stress conditions of V_{G_high} = 6.5 V, V_D = 13V, T_r = T_f = 100 ns, and duty ratio = 50%, Figs. 9(c), 9(d) and 10(a), 10(b) show the I_D-V_G curves of TT and D-MT before and after 1000-sec AC stress under different frequency of 100 kHz and 1000 kHz, respectively. By comparing Figs. 9(c) and 10(a), though the case of 1000 kHz seems to be slightly worse, the difference in degradation between these two cases is very minor and the damaged location cannot be resolved without further examination. In contrast, the subthreshold characteristics of the D-MTs shown in Figs. 9(d) and 10(b) clearly indicate that an increase in stress frequency would lead to a higher degradation. In these figures, the on-state current and the subthreshold swing degradation are both observed under the AC stress. Since in these two cases, the total

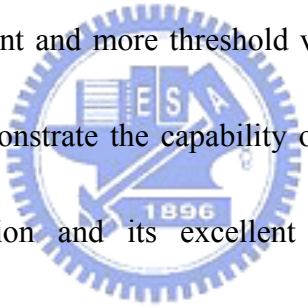
time under V_{G_high} is the same, the repetitions of the transient stages (T_r and T_f) are the reasonable cause of damage. According to the degradation mechanism under AC stress described in Chap 3.2, the single and major stressing parameter under AC stress is the transient hot-carrier stress. Thus, with higher frequency, more repetitions of the transient stress occur and lead to worse degradation.

Furthermore, the tester was stressed under another stress conditions of V_{G_high} = 13 V and V_D = 13V. Under the stress conditions of V_{G_high} = 13 V, V_D = 13V, $T_r = T_f$ = 100 ns, and duty ratio = 50%, Figs. 11(a), 11(b) and 12(a), 12(b) show I_D-V_G curves of TT and D-MT before and after 1000-sec AC stress under different frequency of 100 kHz and 1000 kHz, respectively. The subthreshold characteristics of D-MTs shown in Figs. 11(b) and 12(b) clearly indicate that an increase in stress frequency would lead to a higher degradation, similar to the trend for D-MTs under the stress conditions of V_{G_high} = 6.5 V, V_D = 13V, as shown previously in shown in Figs. 9(d) and 10(b).

To further examine the effect of transient stage during stressing, the stress condition of V_{G_high} = 13 V, V_D = 13 V was performed. The characteristics of D-MTs under static and dynamic (Freq. = 100 kHz) stress conditions are shown in Figs. 13(a) and (b), respectively. It is seen that negligible degradation is observed for the former case, as can be seen in Fig. 13(a). This is reasonable since the voltage difference between the gate and drain electrodes is zero. Nevertheless, the degradation becomes

obvious as AC stress mode is applied. This provides a unambiguous evidence that the damage is incurred during the transient stages, with the aid of the novel test structure.

Figs. 14 and 15 show the on-current degradation and threshold voltage shift, respectively, of the TTs and all kinds of MTs under the stress conditions of V_{G_high} = 6.5 V, V_D = 13V, T_r = T_f = 100 ns, and duty ratio = 50%. By comparing the characteristics of C-MTs and S-MTs, the major damage location along the channel of the TT is unambiguously identified to be near the drain side. And, while the higher frequency is applied during stressing, the characteristics of D-MTs clearly exhibit worse degradation in on-current and more threshold voltage shift, as shown in Figs. 14 and 15. These results demonstrate the capability of the test structure in spatially resolving the damage location and its excellent sensitivity for detecting the frequency-dependent degradation.



・3.3.2 Rising Time and Falling Time

The testers were stressed under the stress conditions of V_{G_high} = 6.5 V, V_D = 13V, Freq. = 500 kHz, and duty ratio = 50%. Figs. 16(a), 17(a) and 18(a) show the on-state current degradation, threshold voltage shift and subthreshold swing under 1000-sec AC stress with stable T_r = 100ns albeit different T_f, respectively. Figs. 16(a), 17(a) and

18(a) clearly show that the degradation of TT is mainly related to D-MT. This is because the testers receive transient hot-carrier stressing when electrons move rapidly from the inversion layer to the drain as the device is turned off quickly. While T_f decreases, the testers receive much severe transient hot-carrier stressing with worse degradation, similar to the degradation mechanism under AC stress described previously in Chap 3.2. Thus, the major damage location along the channel of the TT is unambiguously identified to be near the drain side. And with the aid of the novel test structure, the results of the D-MTs in terms of on-state current degradation, threshold voltage shift and subthreshold swing under 1000-sec AC stress with stable T_r = 100ns, albeit different T_f, provide a clear and definite evidence.

Figs. 16(b), 17(b) and 18(b) show the on-state current degradation, threshold voltage shift and subthreshold swing under 1000-sec AC stress with stable T_f = 100ns but different T_r, respectively. As the test transistor with T_r = 20ns shows a strange trend in the on-state current degradation, threshold voltage shift and subthreshold swing, a solid line was used to fit the trend in this study, and will be re-visited in the future work. With the aid of the novel test structure, we note some interesting phenomena. First, TTs, S-MTs, C-MTs and D-MTs exhibit negligible shift in the on-state current with decreasing T_r, as shown in Fig. 16(b). Second, in Figs. 17(b) and 18(b), TTs, S-MTs and C-MTs also exhibit negligible threshold voltage shift and

subthreshold swing with decreasing T_r. In contrast, D-MTs show an obvious trend that larger threshold voltage shift and worse subthreshold swing degradation occur with shorter T_r. The reason for the above-mentioned phenomenon is still not clear at present, and will be studied in detail in the future.

Chapter 4
Conclusions

In this study, we have proposed and successfully demonstrated a new test structure suitable for monitoring the spatial hot-carrier degradation in poly-Si TFTs not previously possible. Our results indicate that this unique configuration is capable of resolving the spatial damage induced at different locations along the channel of the test transistor and, based on the observations, major mechanisms responsible for the resultant degradation could be identified. The new test structure is also shown to be highly sensitive for detecting degradations in even slightly damaged devices.

With the aid of this novel test structure, we can perform electrical characterization not possible with the conventional TFTs. Thus, new phenomena are waiting for us to unveil. In the future, we will further analyze the hot-carrier degradation of HC-TFTs under various stress conditions in detail. The new HC-TFTs thus allow us to gain a clear understanding of the model of the hot-carrier degradation mechanism under both static and dynamic stressing.

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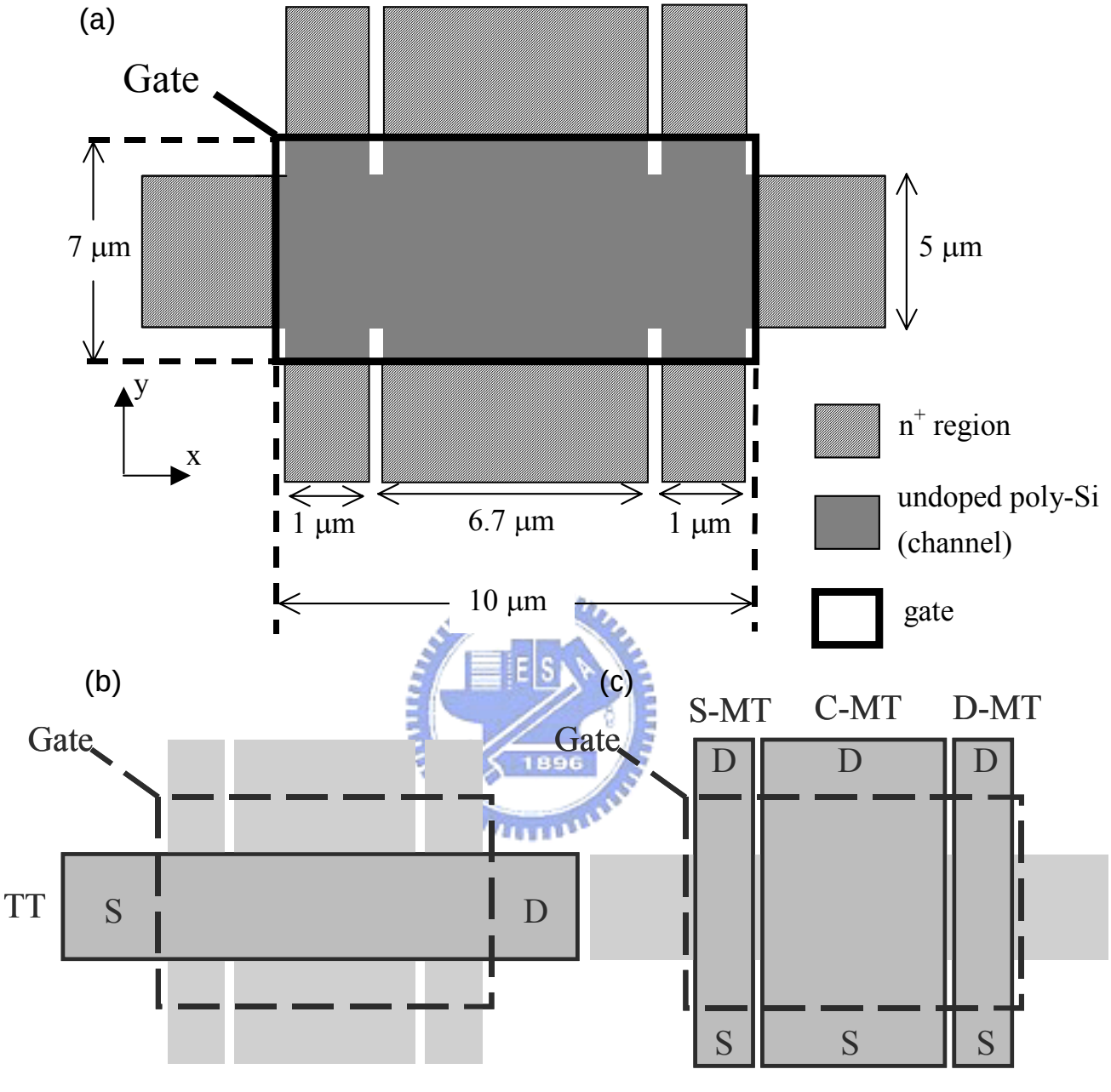

Fig. 1 Top view of the test structure.

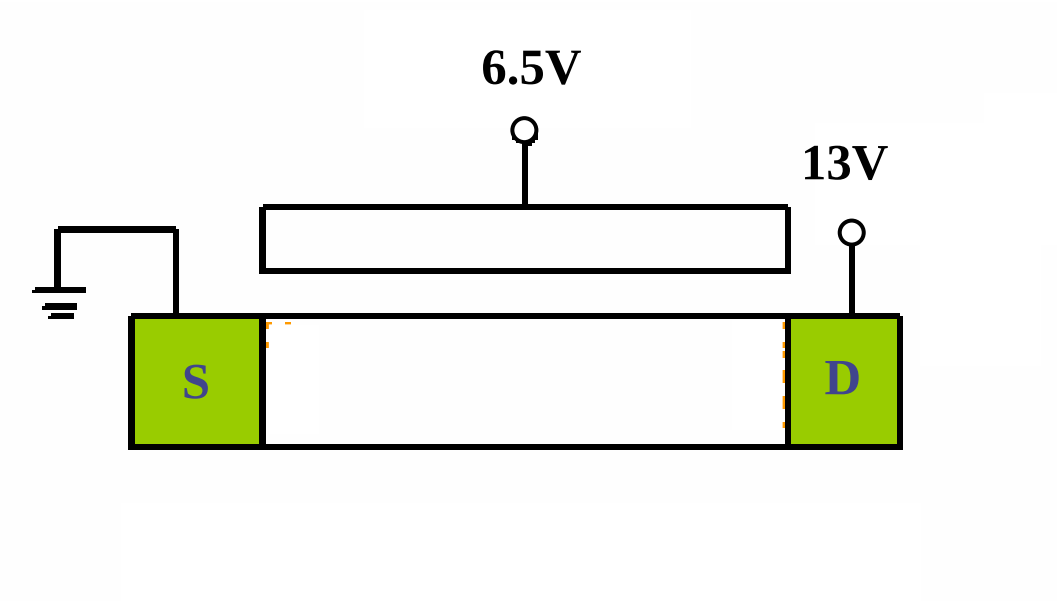

Fig. 2 DC Stress Condition.

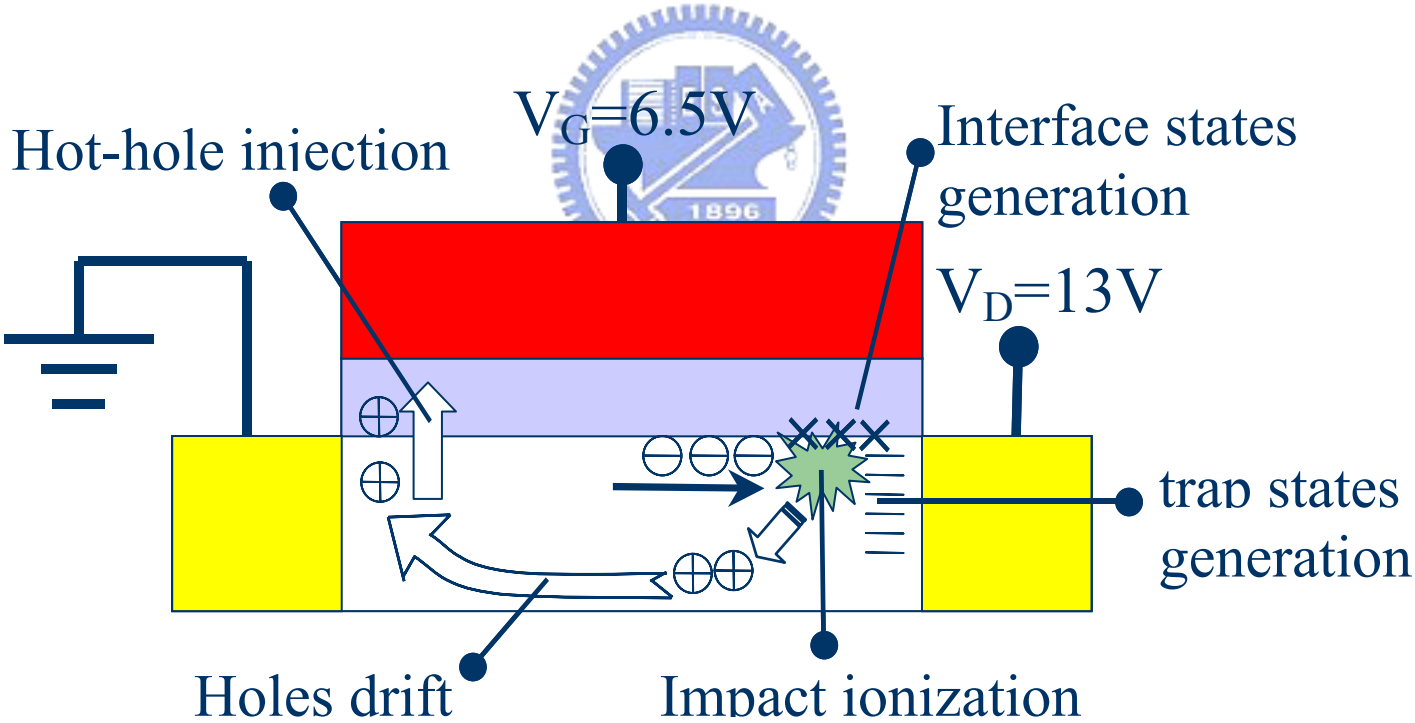

Fig. 3 Schematic illustration of hot-carrier-degradation mechanisms under V_G/V_D=6.5V/13V.

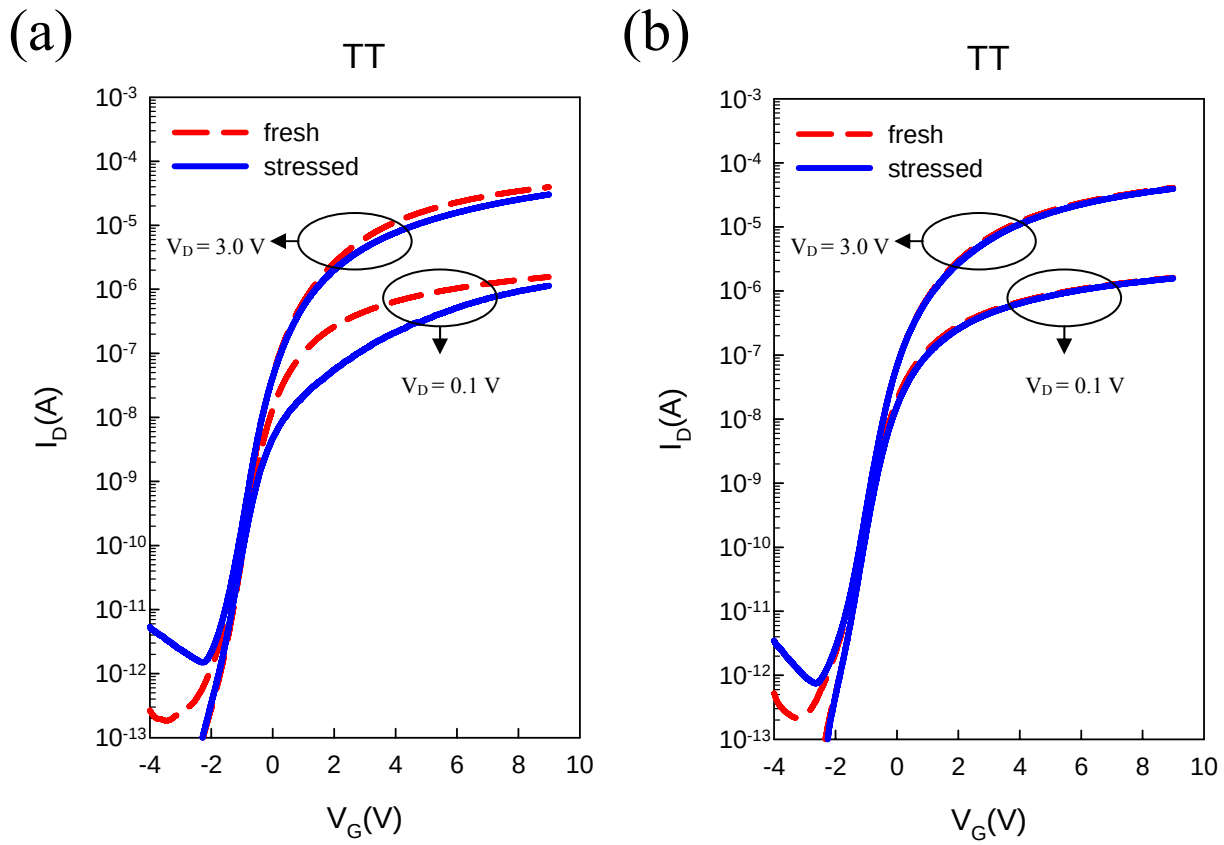

Fig. 4 Subthreshold characteristics of the test transistor before and after DC stressing at V_G/V_D of (a) 9V/18V and (b) 6.5V/13V for 1000 sec.

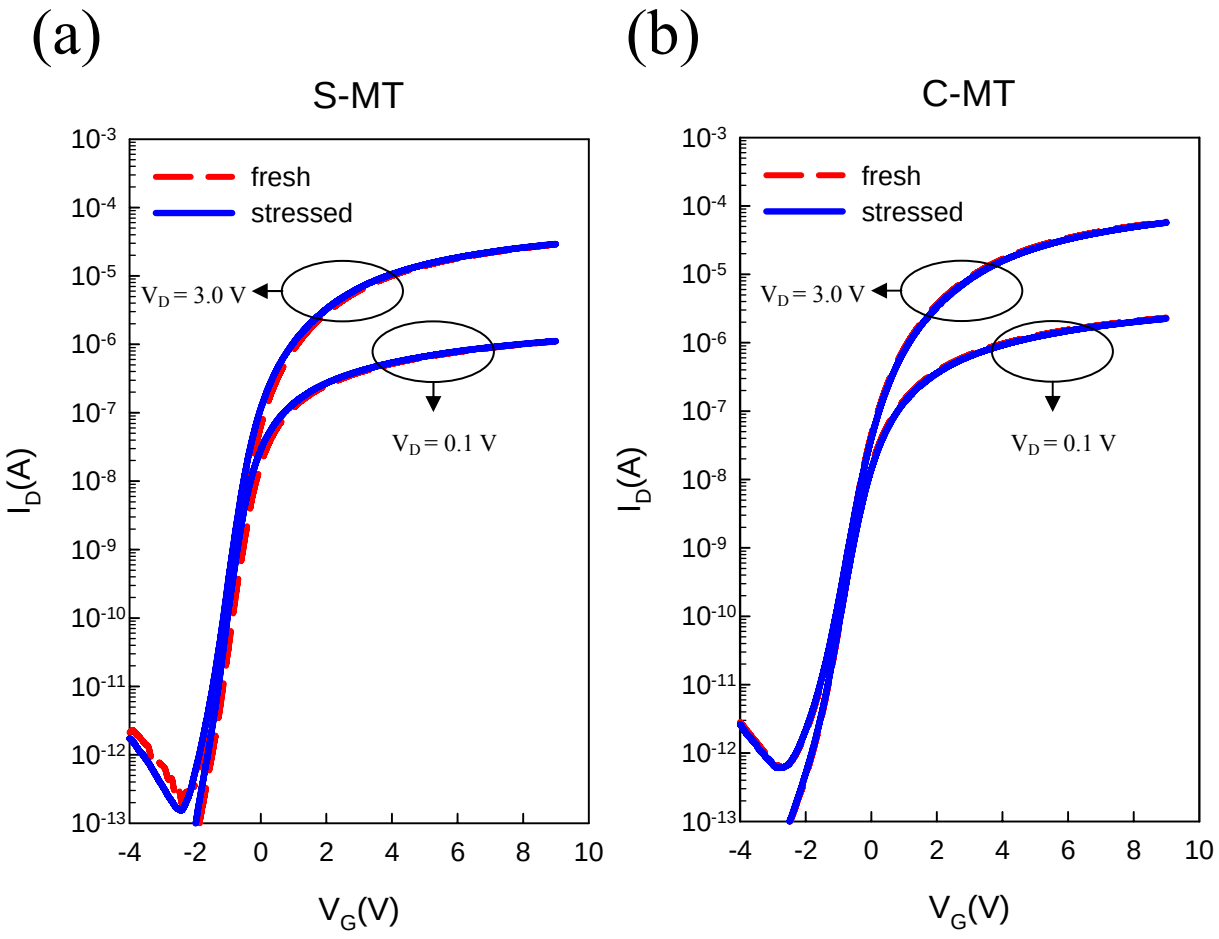

Fig. 5(a), (b) Subthreshold characteristics of (a) S-MT, (b) C-MT, and (c) D-MT transistors in the same test structure characterized in Fig. 1(a) before and after DC stressing at V_G/V_D of 9V/18V for 1000 sec.

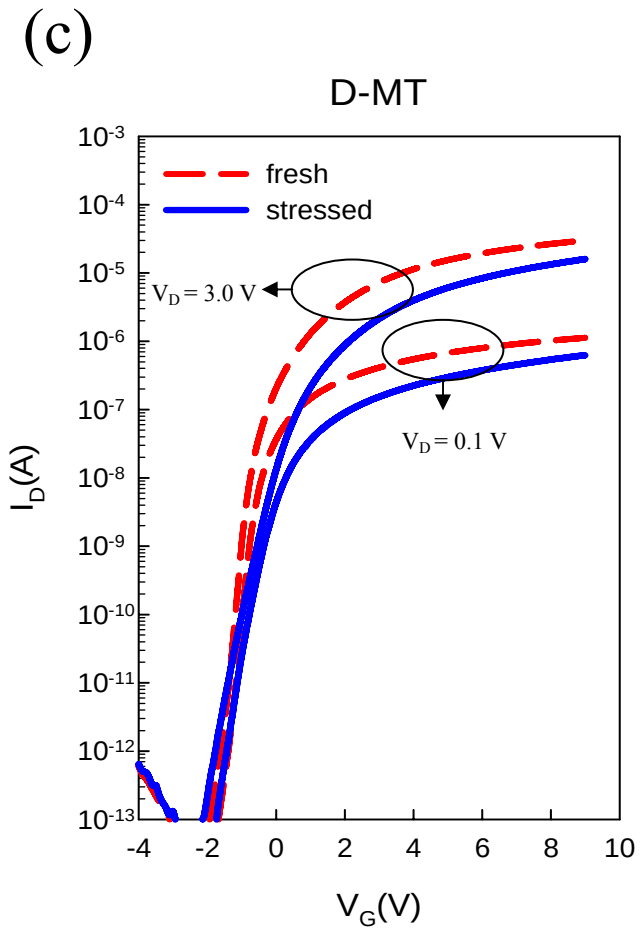

Fig. 5(c) Subthreshold characteristics of (a) S-MT, (b) C-MT, and (c) D-MT transistors in the same test structure characterized in Fig. 1(a) before and after DC stressing at V_G/V_D of 9V/18V for 1000 sec.

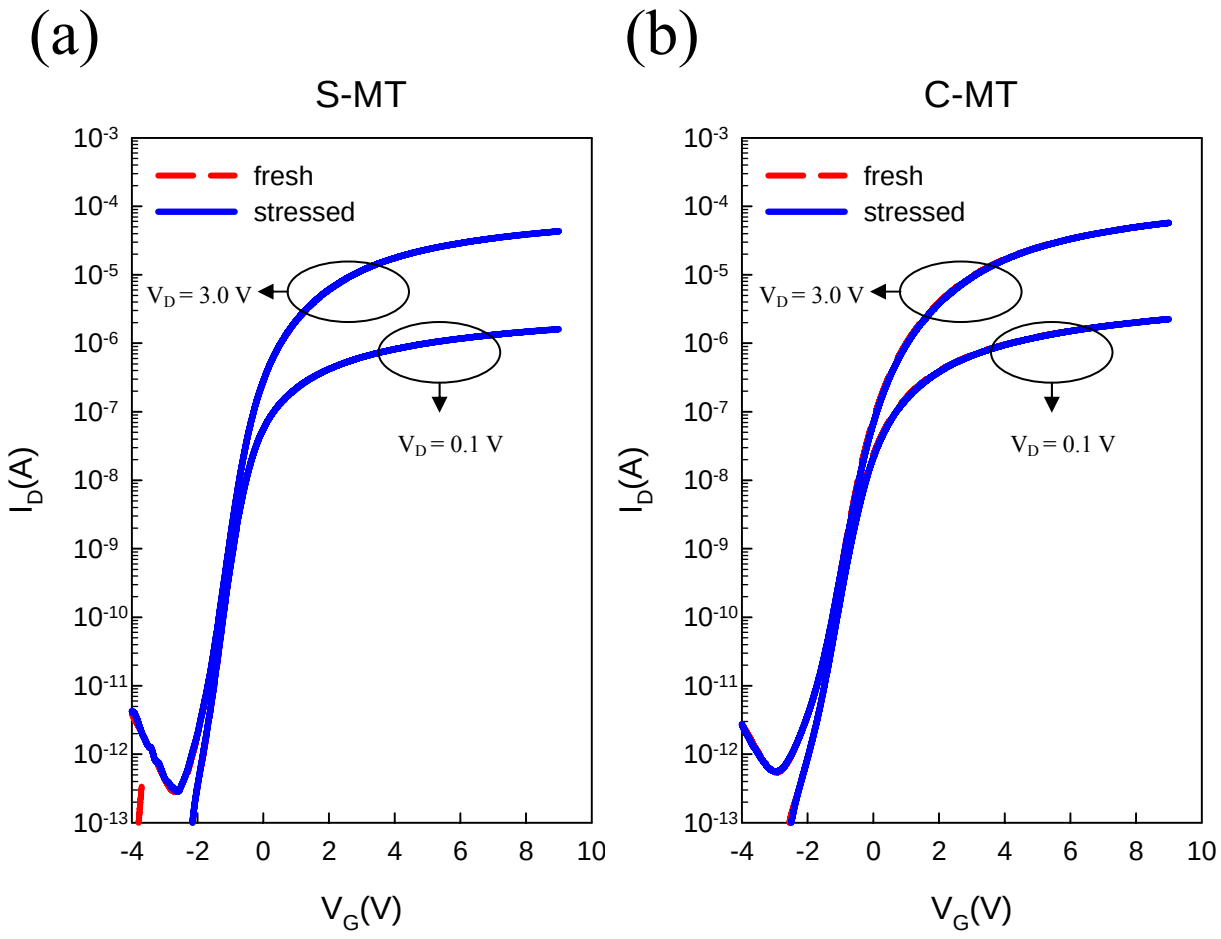

Fig. 6(a), (b) Subthreshold characteristics of (a) S-MT, (b) C-MT, and (c) D-MT transistors in the same test structure characterized in Fig. 1(a) before and after DC stressing at V_G/V_D of 6.5V/13V for 1000 sec.

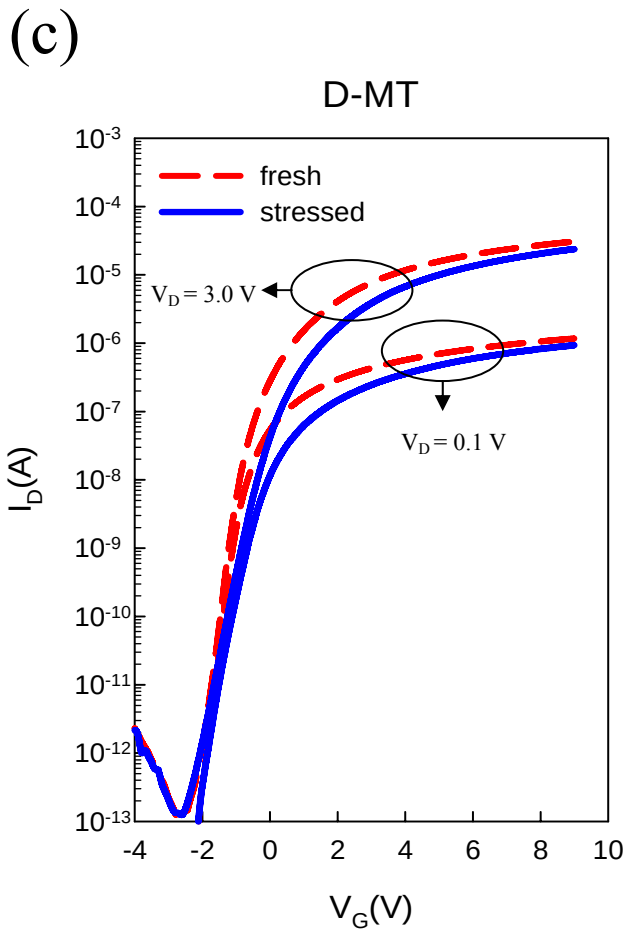

Fig. 6(c) Subthreshold characteristics of (a) S-MT, (b) C-MT, and (c) D-MT transistors in the same test structure characterized in Fig. 1(a) before and after DC stressing at V_G/V_D of 6.5V/13V for 1000 sec.

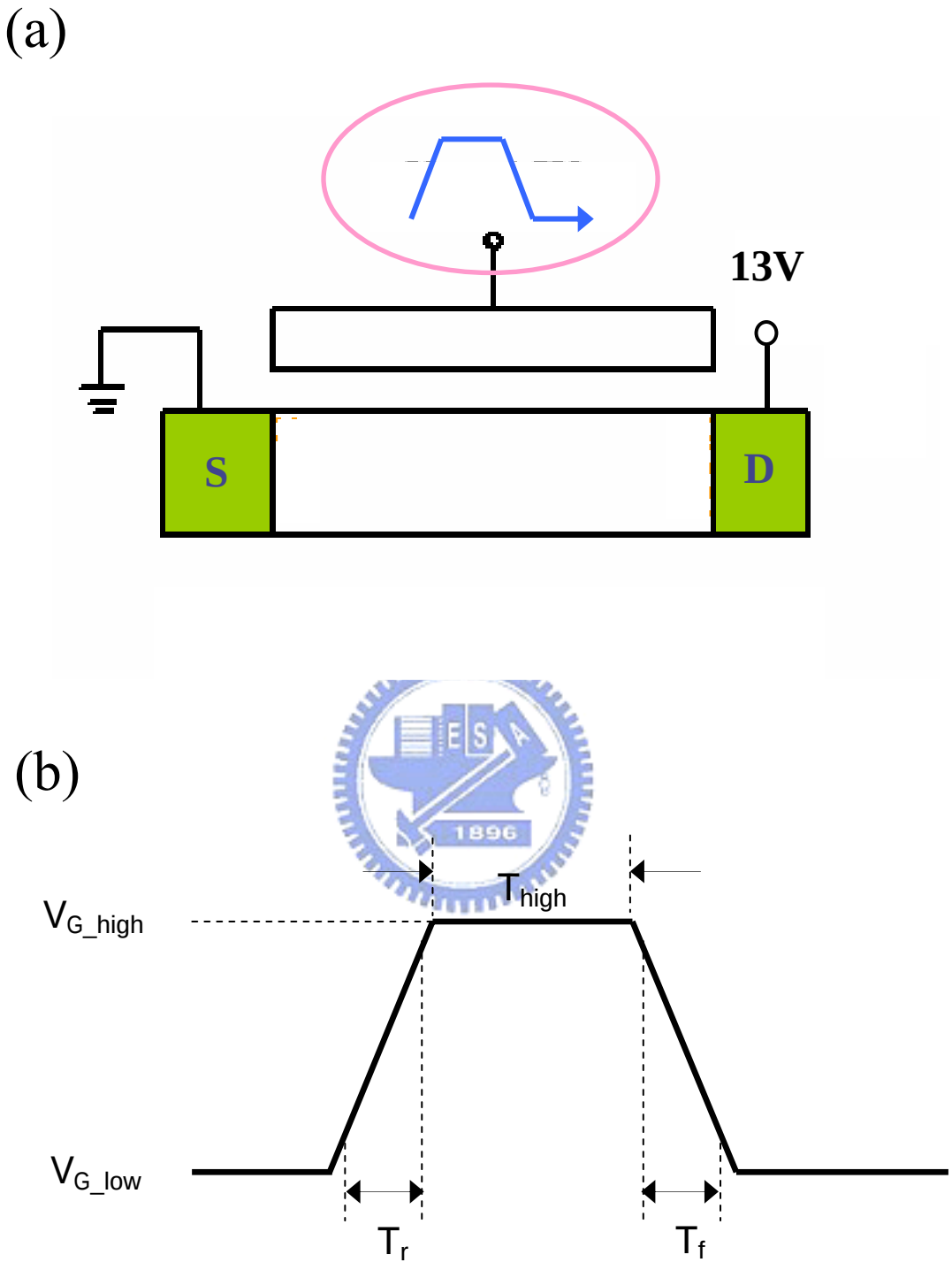

Fig. 7 Definition of AC Stress.

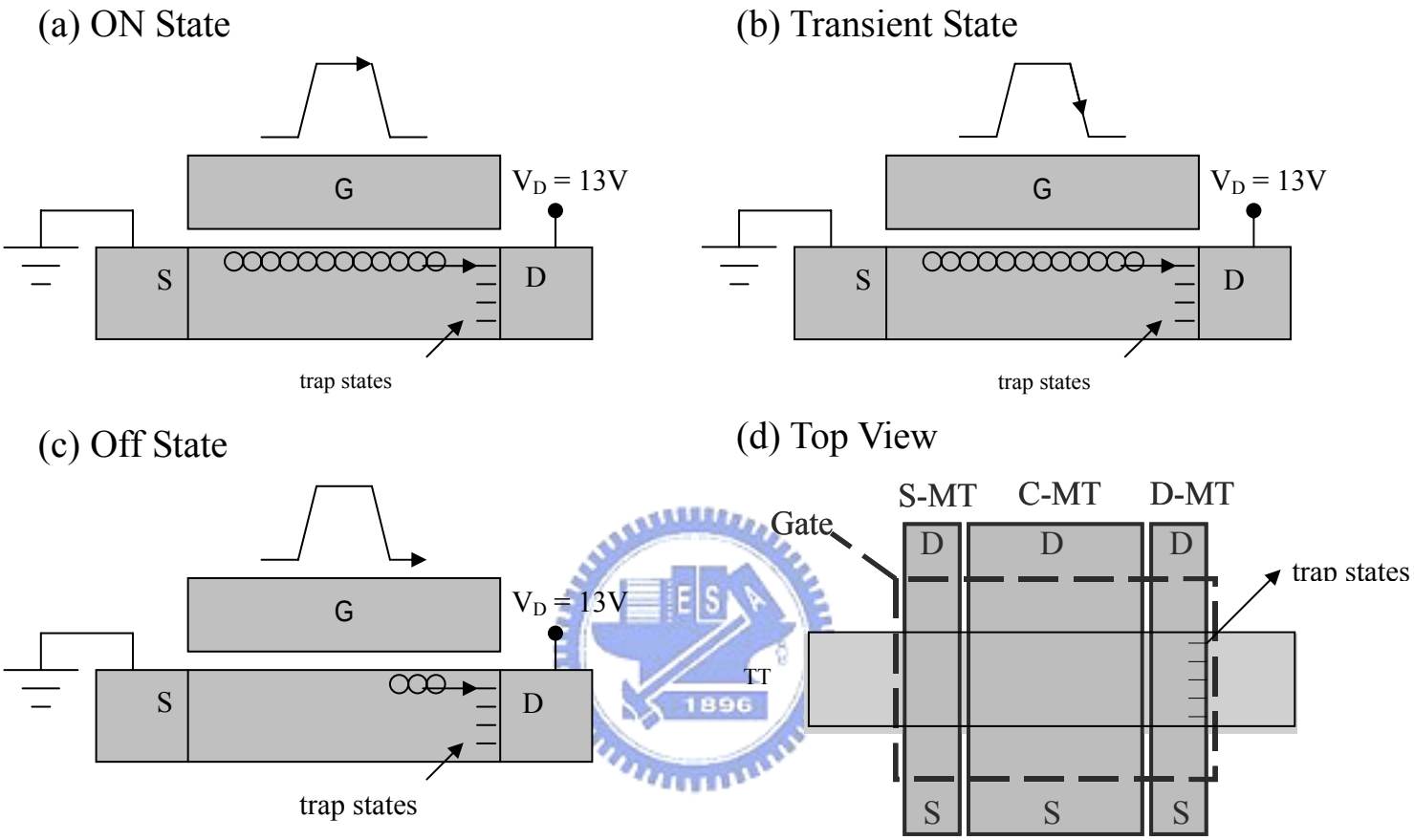

Fig. 8 Mechanisms of AC stress induced degradation.

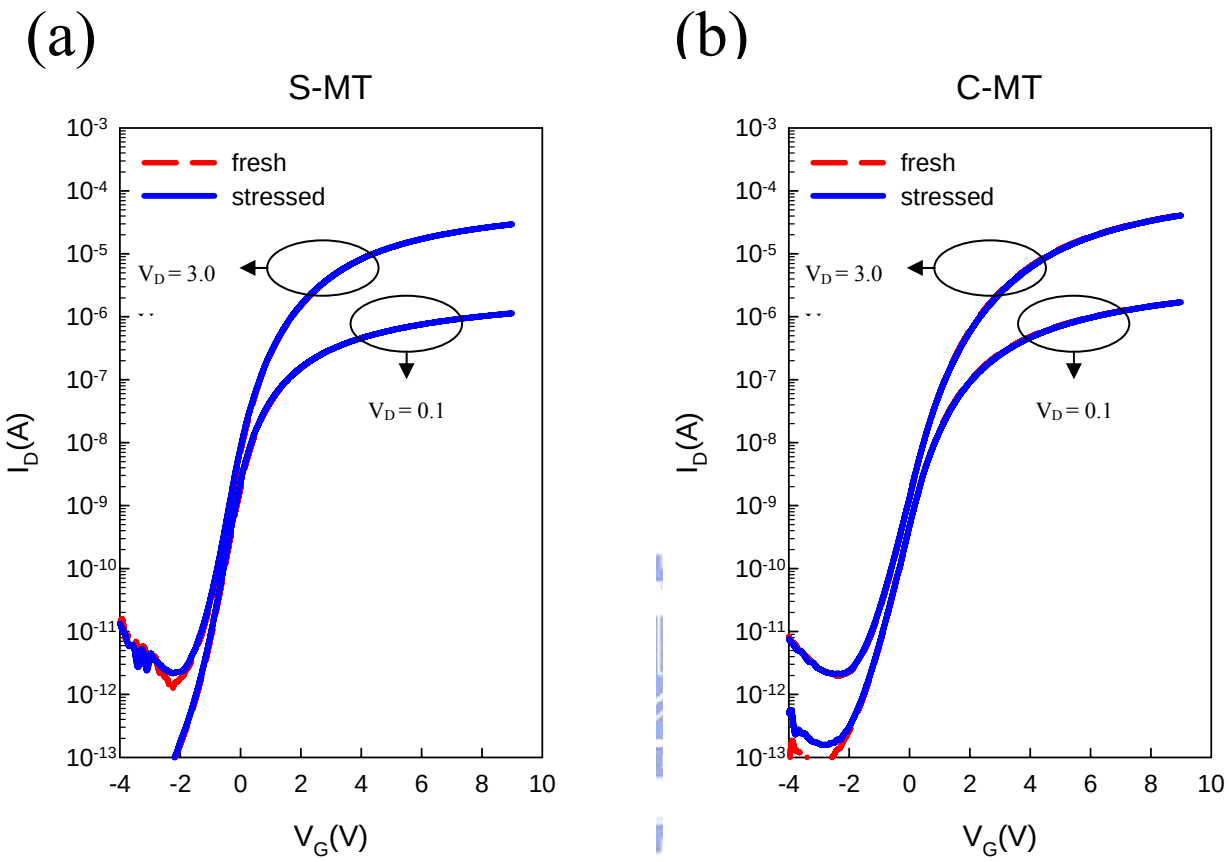

Fig. 9(a), (b) I_D-V_G curves of HC-TFTs before and after AC stress under V_G/V_D = 6.5V/13V for 1000sec with the frequency of 100 kHz for (a) S-MT, and (b) C-MT, (c) TT, and (d) D-MT.

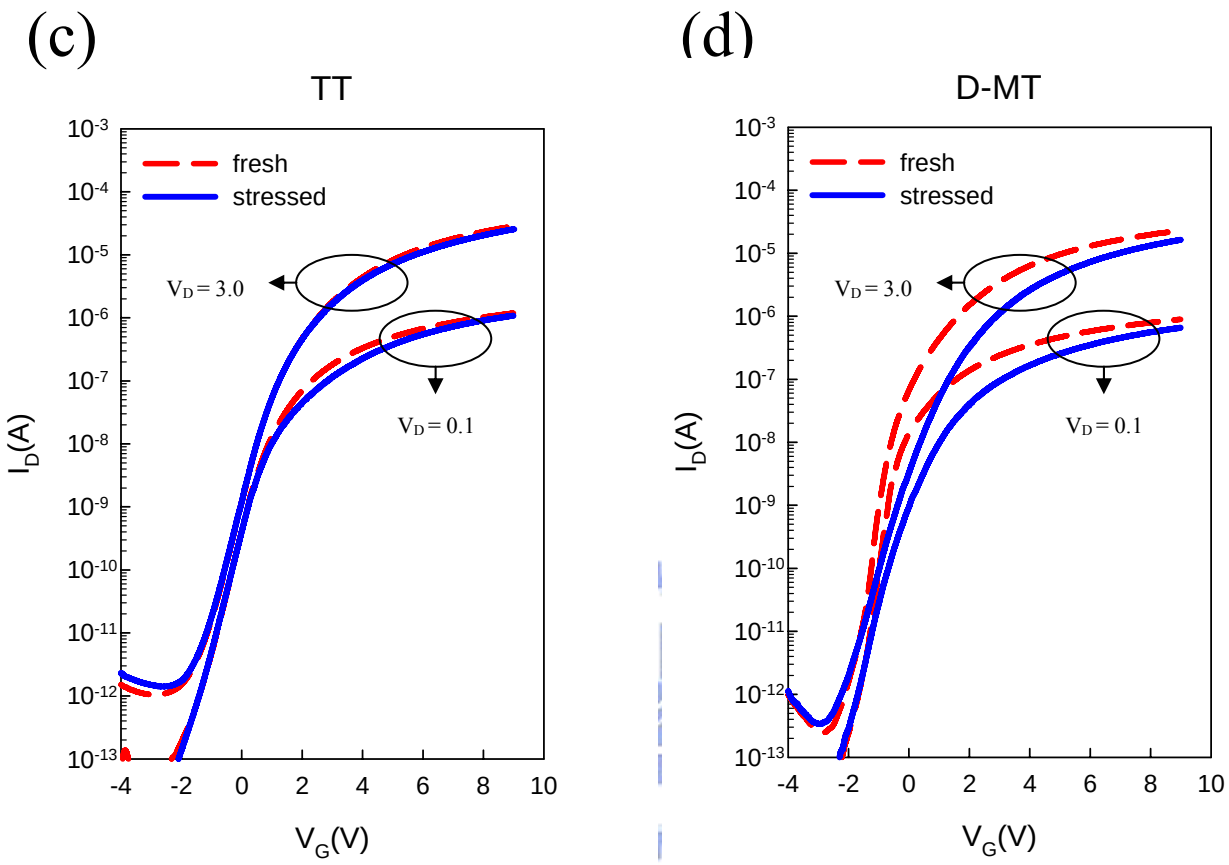

Fig. 9(c), (d) I_D-V_G curves of HC-TFTs before and after AC stress under V_G/V_D = 6.5V/13V for 1000sec with the frequency of 100 kHz for (a) S-MT, and (b) C-MT, (c) TT, and (d) D-MT.

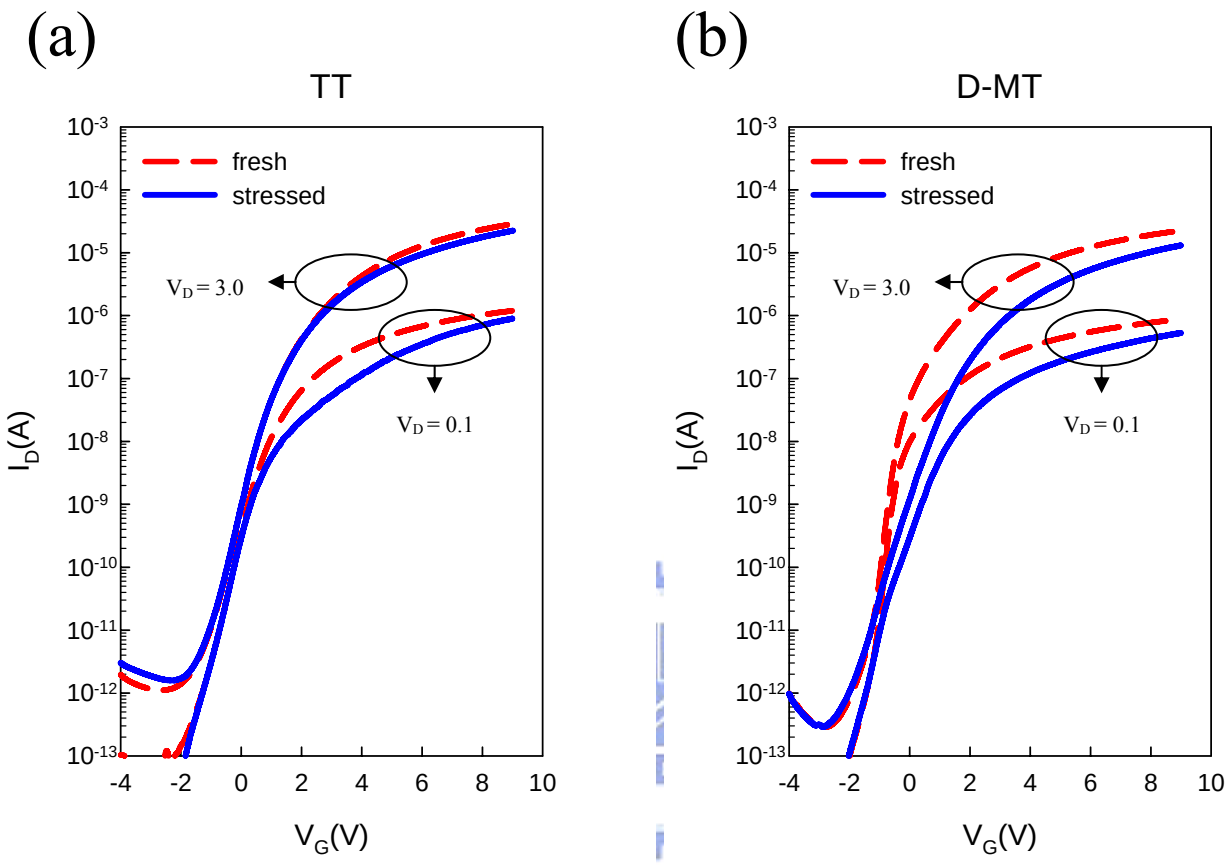

Fig. 10 I_D-V_G curves of HC-TFTs before and after AC stress under V_G/V_D = 6.5V/13V for 1000sec with frequency of 1000 kHz for (a) TT, and (b) D-MT.

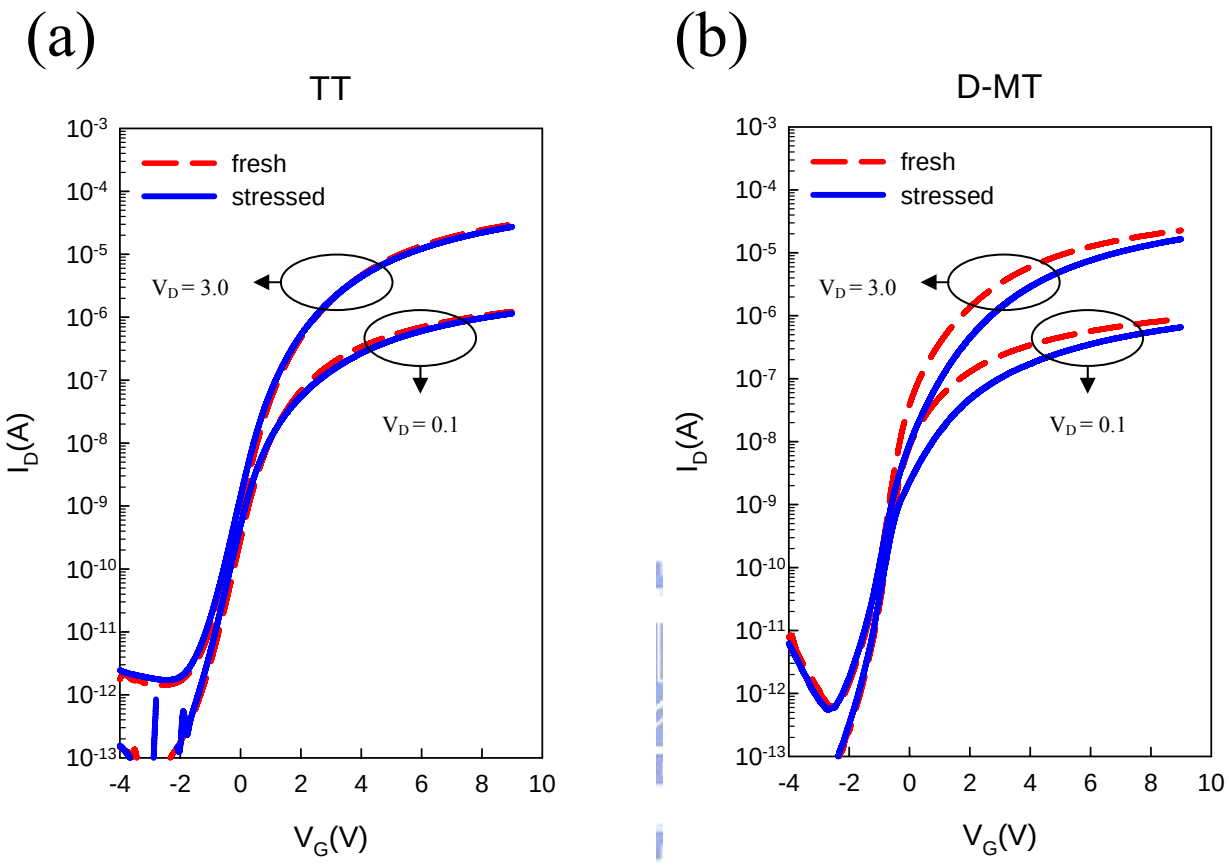

Fig. 11 I_D-V_G curves of HC-TFTs before and after AC stress under V_G/V_D = 13V/13V for 1000sec with frequency of 100 kHz for (a) TT, and (b) D-MT.

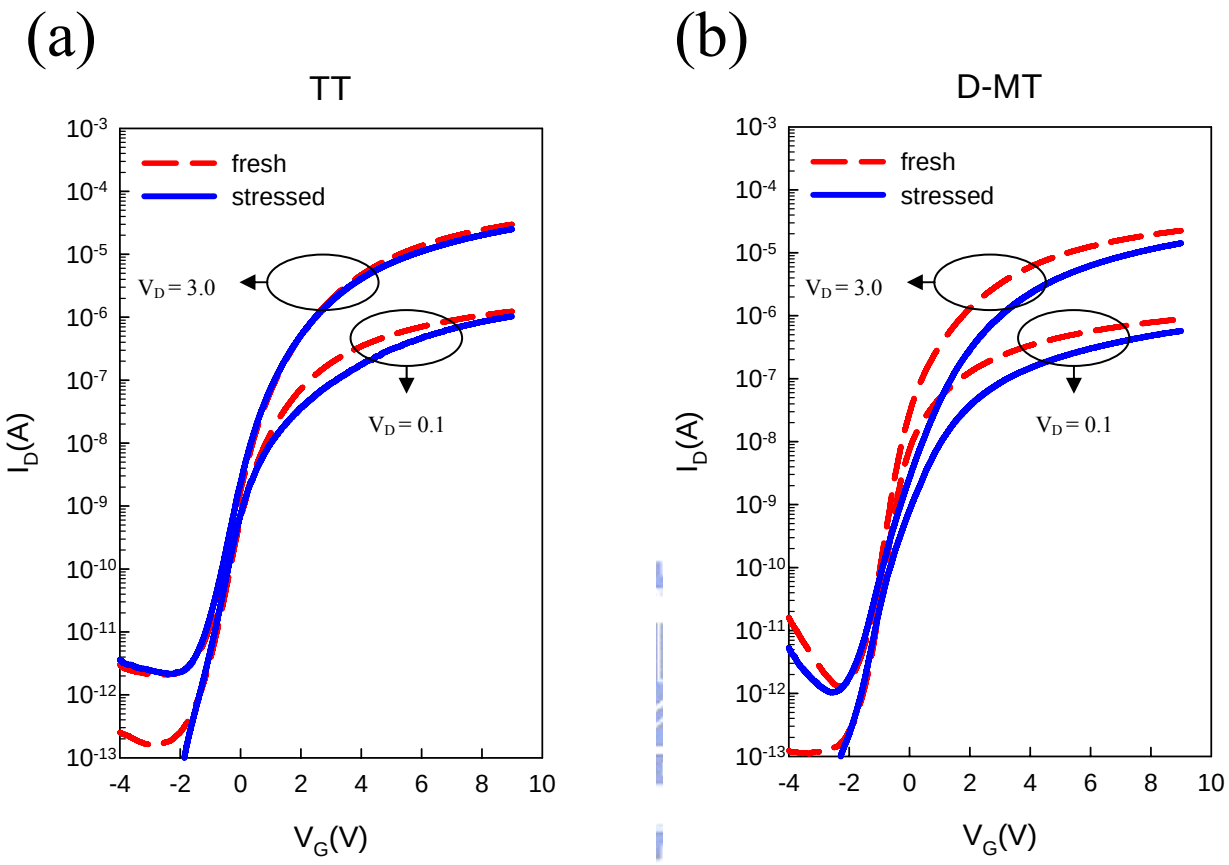

Fig. 12 I_D-V_G curves of HC-TFTs before and after AC stress under V_G/V_D = 13V/13V for 1000sec with frequency of 1000 kHz for (a) TT, and (b) D-MT.

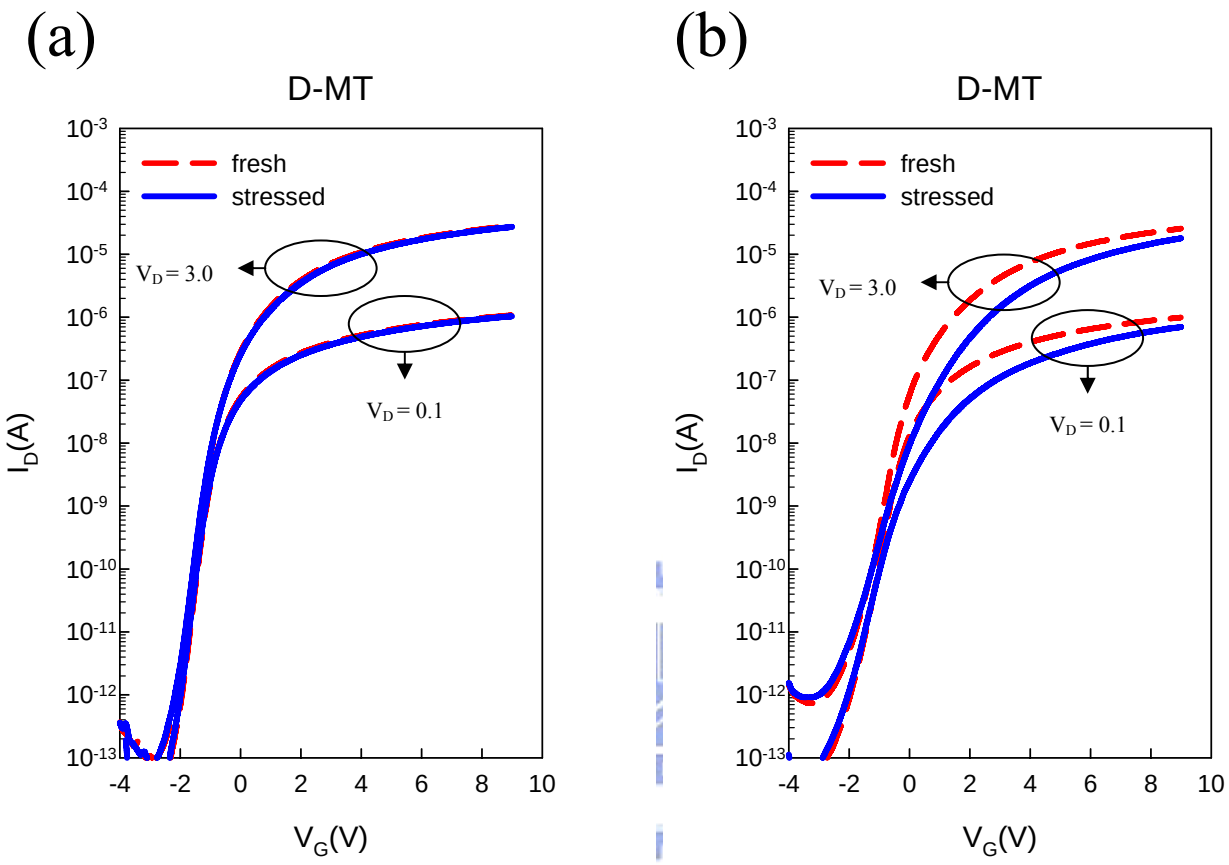

Fig. 13 I_D-V_G curves of D-MT before and after (a) DC (b) AC stress

under V_G/V_D = 13V/13V for 1000sec.

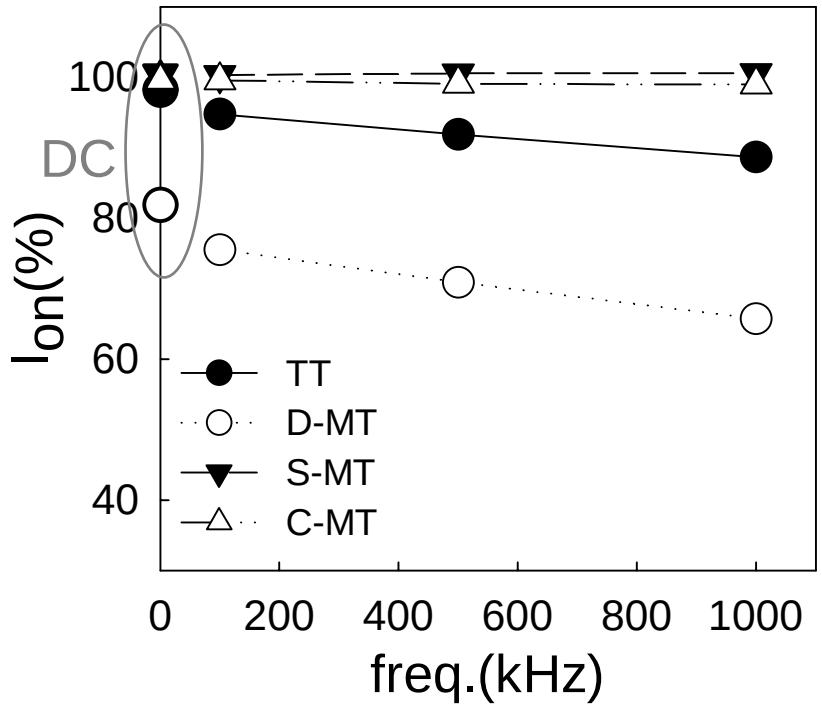

Fig. 14 On-current degradation as a function of frequency under AC stress.

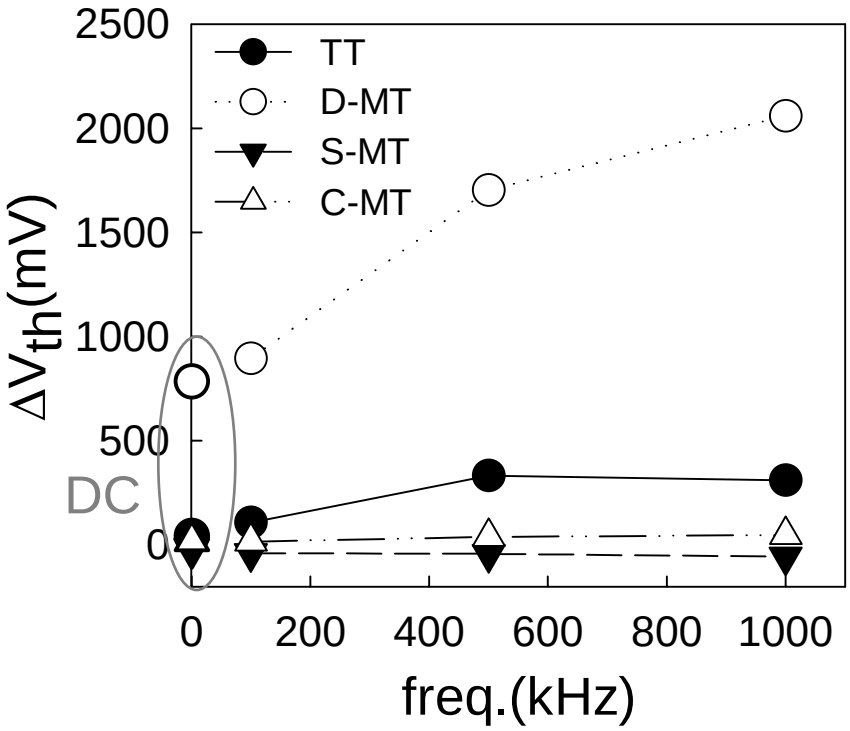

Fig. 15 Threshold voltage shift as a function of frequency under AC stress.

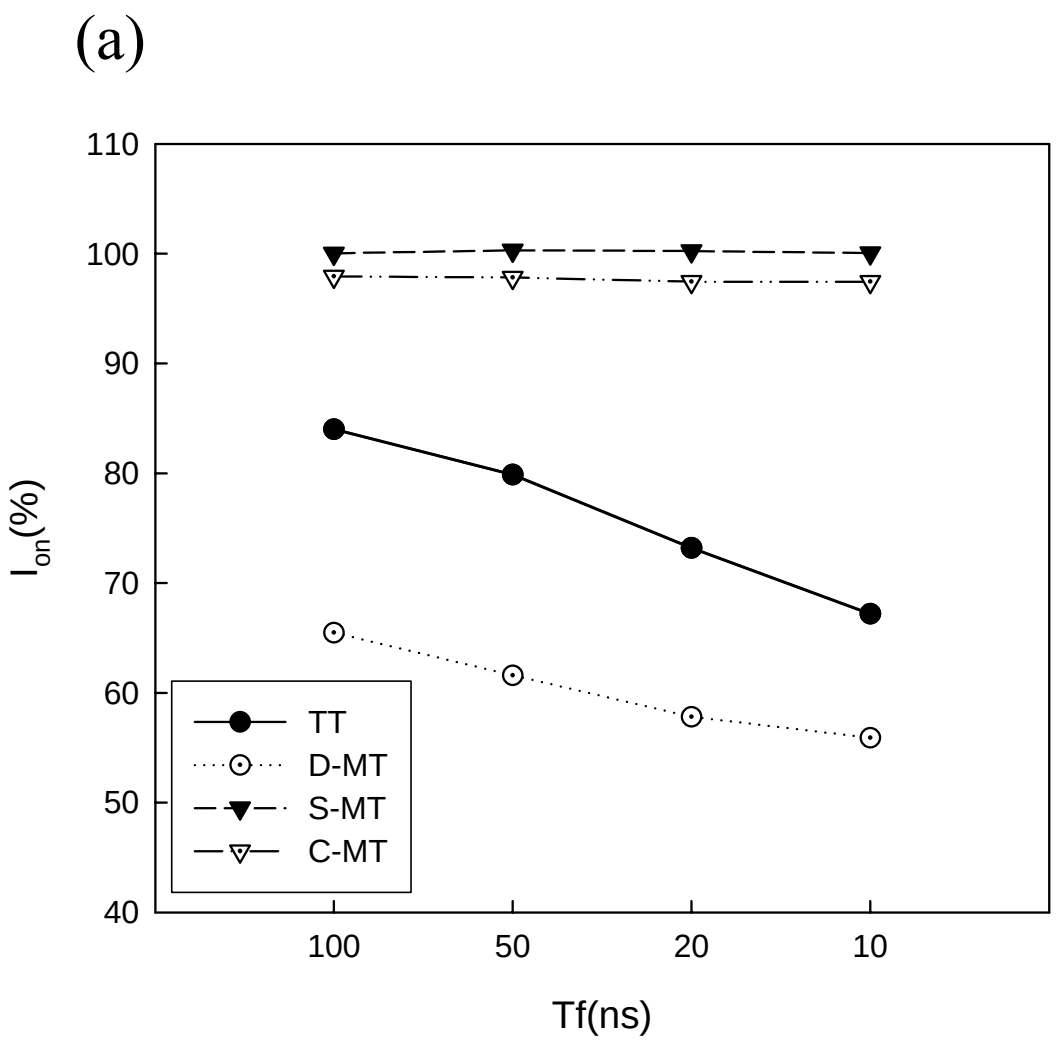

Fig. 16(a) On-current degradation under AC stress as a function of

(a) Tf and (b) Tr.

(b)

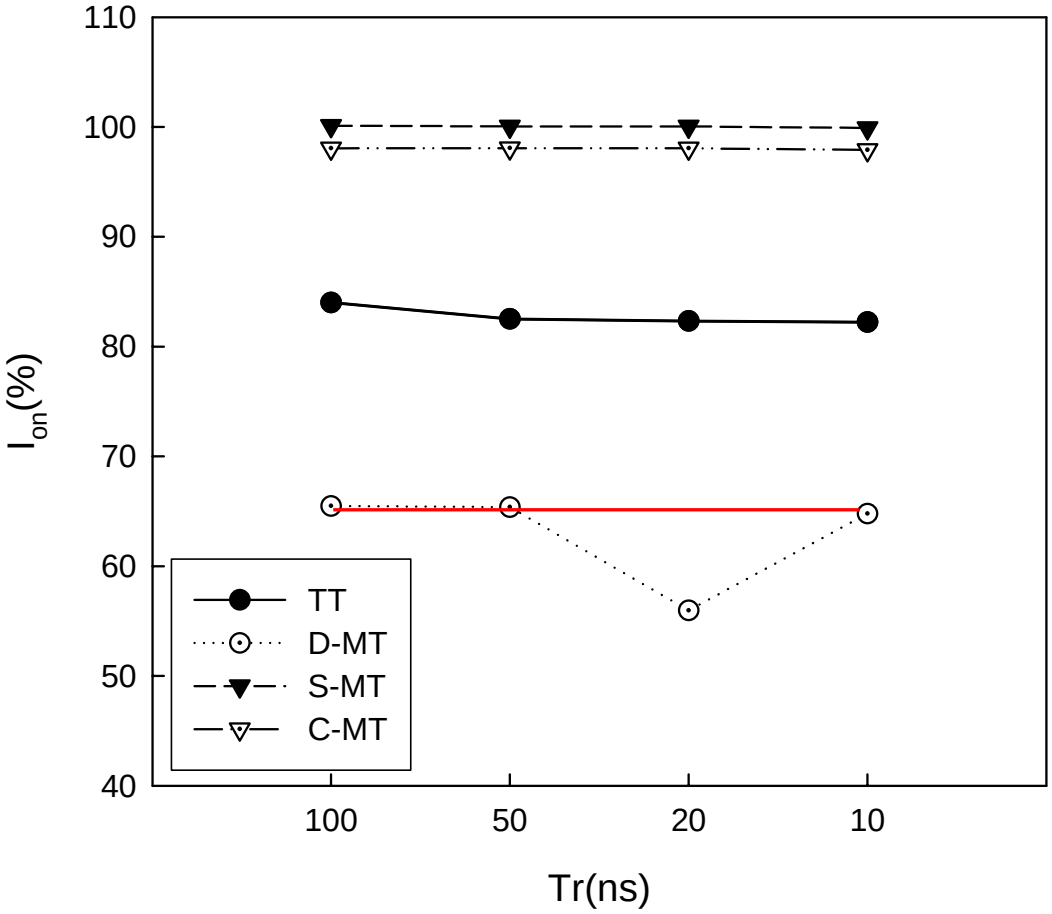

Fig. 16(b) On-current degradation under AC stress as a function of

(a) Tf and (b) Tr.

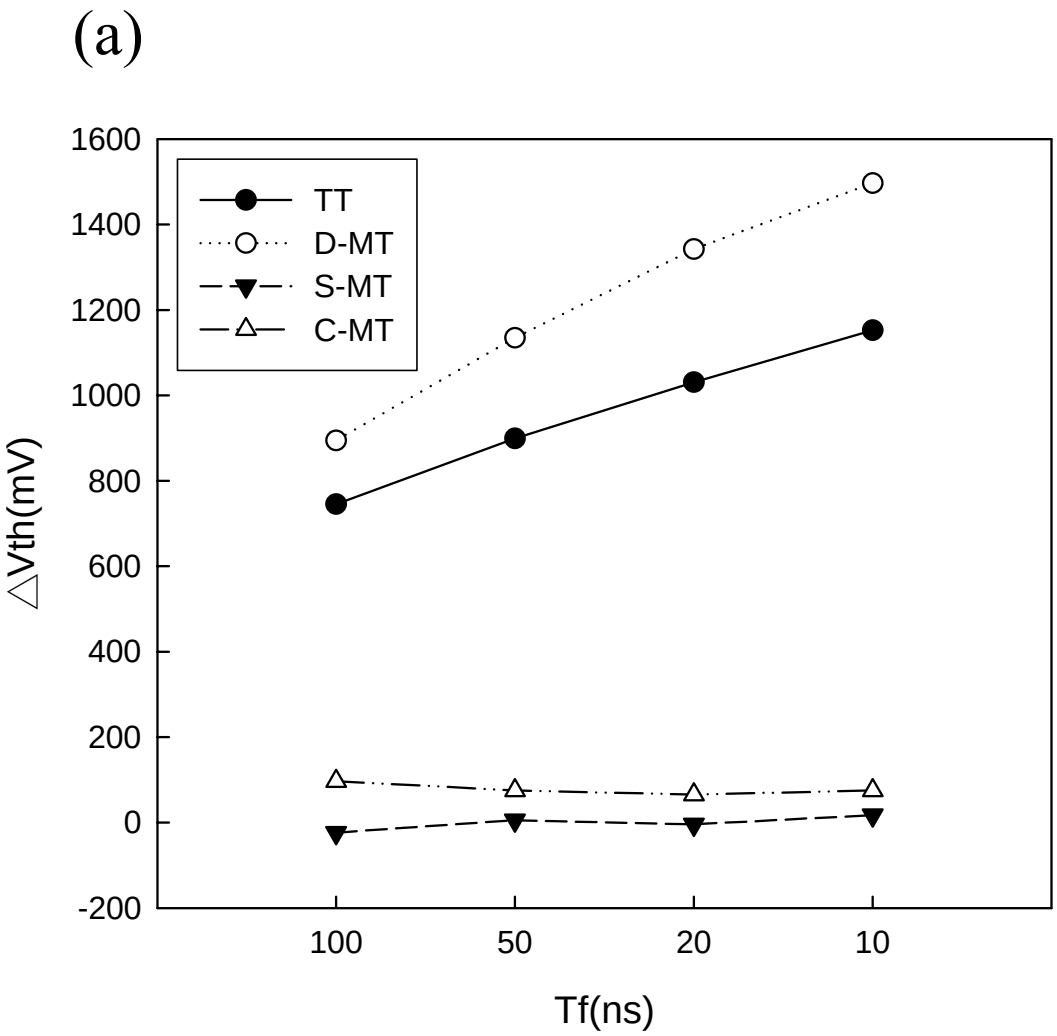

Fig. 17(a) Threshold voltage shift under AC stress as a function of

(a) Tf and (b) Tr.

(b)

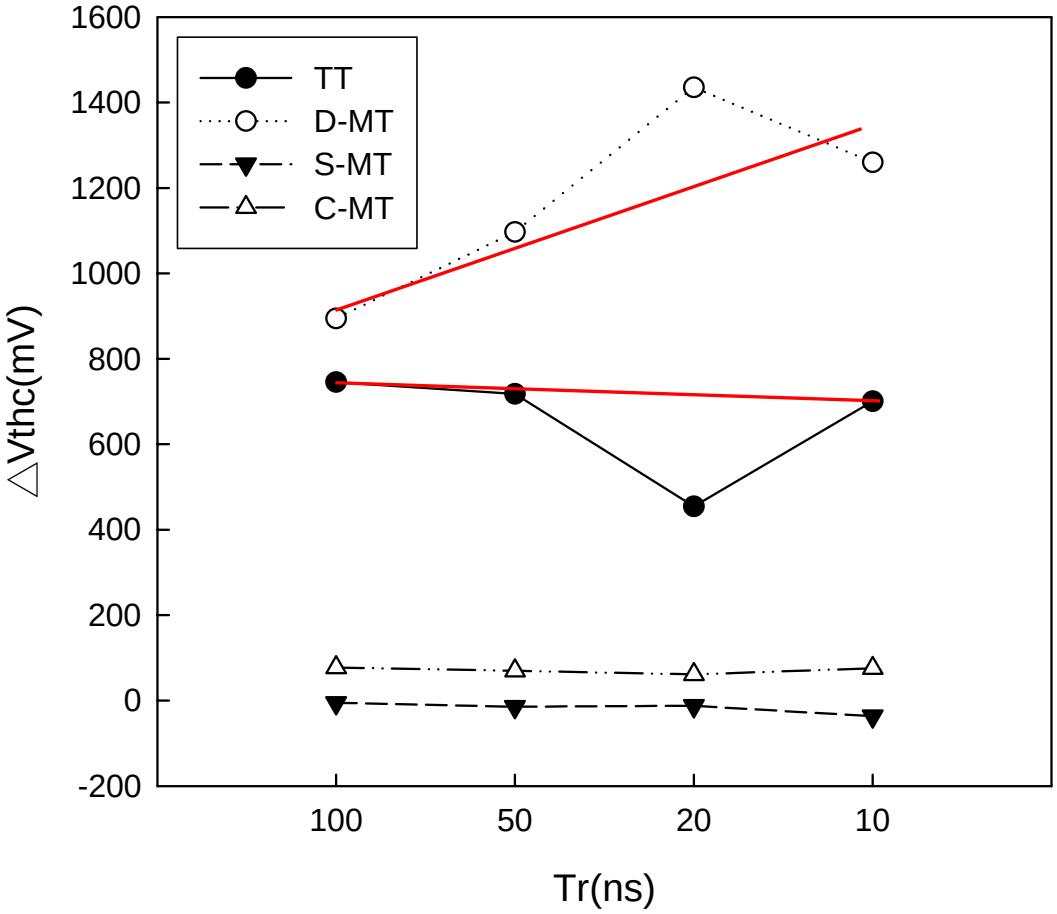

Fig. 17(b) Threshold voltage shift under AC stress as a function of

(a) Tf and (b) Tr.

(a)

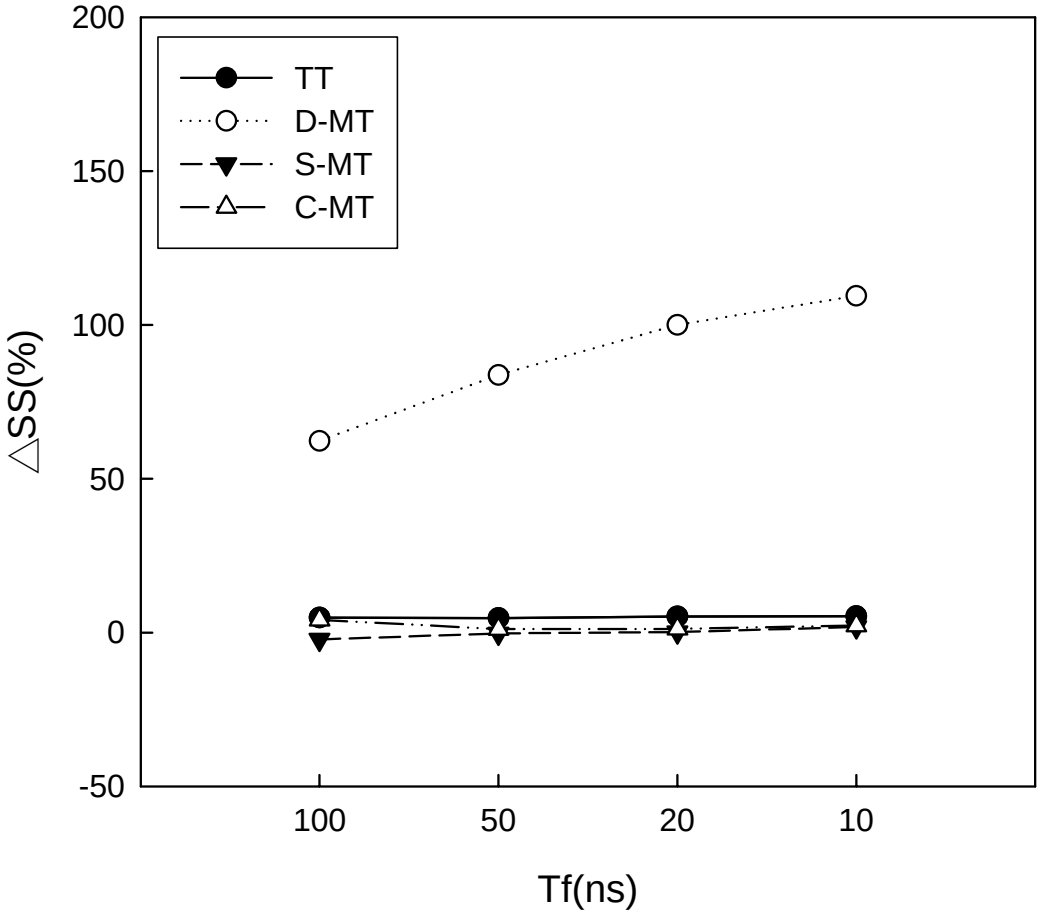

Fig. 18(a) Subthreshold swing shift under AC stress as a function of

(a) Tf and (b) Tr.

(b)

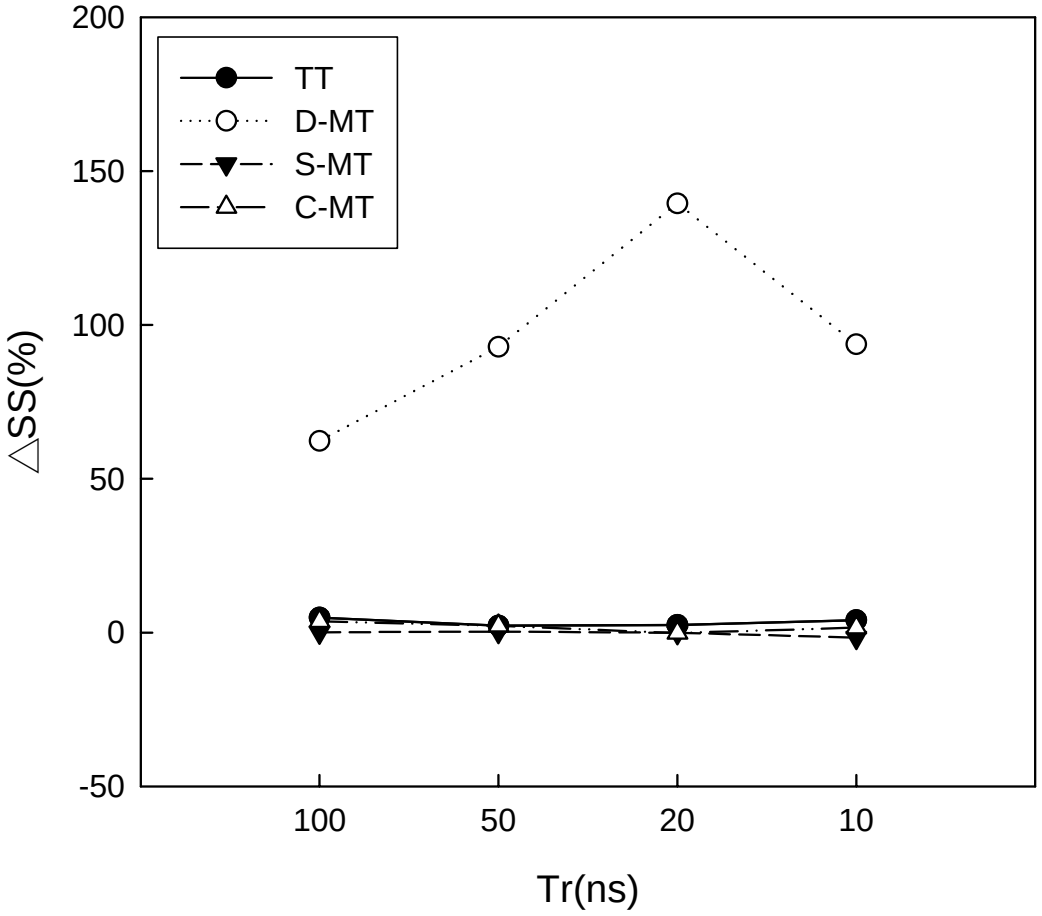

Fig. 18(b) Subthreshold swing shift under AC stress as a function of

(a) Tf and (b) Tr.

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