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碩士論文

新穎的SONOS儲存單元製程之研究

A Study of Novel SONOS Cell Storage Process

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中華民國九十六年五月

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摘要

在非揮發性記憶體的發展與研究過程中，矽-氧化矽-氮化矽-氧化矽-矽(Silicon-Oxide-Nitride-Oxide-Silicon，SONOS)記憶體元件具有許多優點備受矚目。然而隨著尺寸的微縮以及為了維持良好的儲存能力，各種材料及結構也被使用在SONOS 結構裡用以改善可靠度的相關問題。

本篇論文提出一種新穎的 SONOS 儲存單元製造之方法。首先，我們在試片上成長一層薄的化學氧化層（chemical oxide)；接著使用 LPCVD 通入 NH_3 氮化化學氧化層，然後沈積氮化矽層；之後使用爐管通入 O_2 對氮化矽層進行再氧化。優點在於 LPCVD 可同時氮化化學氧化層以及沈積氮化矽；而再氧化過程中，可趕走氮化穿遂氧化層所產生的氫，使得穿遂氧化層表面形成具高氮濃度的氮氧化層，同時使得氮化矽層形成具漸變式梯形能帶的結構。另外探討不同再氧化時間對於可靠度特性的影響。研究結果發現，經過再氧化處理之後，在適當的條件下，確實能有效增大記憶體操作窗口，並且減緩寫入、抹除等操作所造成性能退化的速率。

A Study of Novel SONOS Cell Storage Process

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Abstract

Nowadays, SONOS (Silicon-Oxide-Nitride-Oxide-Silicon) memory device becomes popular because of its simplicity and scalable in structure by comparing with conventional floating gate flash memory.

In this thesis, we proposed a novel process to fabricate a SONOS capacitor. This process mainly included four process stages – chemical oxide growth, nitridation, forming the Si_3N_4 and subsequent furnace O_2 reoxidation. By this process, the oxynitride as tunnel dielectric and a tapered bandgap nitride are obtained.

It is found that the structure formed by this novel process exhibits improved cycling endurance and charge-trapping efficiency. The result of the experiment can provide a very promising solution for future flash memory design.

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謹以此文獻給所有在求學過程中幫助過我的人，謝謝你們。

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Chapter 1

Introduction

1.1 General Background

Floating gate flash memory have been widely used in commercial products, such as IC cards, digital camera, compact card, cell phone, and mp3 player etc. Recently, the demand for the flash memory device grows with each passing day, the density and operation speed of flash memory and its reliability issues become the popular research theme. The operation principal of floating gate flash memory is using the polycrystalline silicon as floating gate to be the charge stored units. When electrons are injected from the channel and stored in floating gate, the threshold voltage of devices will be changed. Therefore, the logical "0" and "1" definition of nonvolatile memory devices are used for the difference between threshold voltages.

In 1960's, magnetic-core memory was not a good memory device due to the high cost, large volume, and high power consumption, it was necessary to find a new kind of memory device to replace the magnetic-core memory. In 1967, D. Kahng and S. M. Sze invented the floating-gate (FG) nonvolatile semiconductor memory at Bell Labs [1.1]. As shown in Figure 1-1, a conventional flash memory device is similar to the Intel ETOX (EPROM Tunnel Oxide) structure. The basic device is a MOSFET with a modified gate stack structure that has a control gate (CG) and a floating gate (FG) embedded in a dielectric material such as silicon dioxide (SiO_2). The first SiO_2 energy barrier between the floating gate and the channel prevents electrons from leaking into the channel. A second barrier between the floating gate and the control gate prevents electrons from escaping to the

control gate. The invention of FG memory impacts more than the replacement of magnetic-core memory, and creates a huge industry of portable electronic systems. Nowadays, the stacked-gate FG device structure has played an important role in the nonvolatile-memory, and is widely used in both standalone and embedded memories.

In a FG memory device, the thickness of the tunnel oxide must be reduced in order to improve the program/erase speed. However, the thickness of the tunnel oxide has its limits. If the tunnel oxide is made thicker to get better retention characteristics, the program/erase speed will be slower. On the other hand, the tunnel oxide must be less than 2.5 nm in order to achieve 100 ns write/erase time for a reasonable programming voltage (<10V). When the tunnel oxide is thinner in order to get high program/erase efficiency, the retention characteristics may be degraded. Therefore, we need to balance the speed and reliability and the thickness of the tunnel oxide is compromised to about 8-11 nm, which is barely reduced over more than five successive generations of the industry [1.2]. Furthermore, if the tunneling oxide can not be thinned any more, both the speed and operation voltage of memory can not be improved.

In order to solve the scaling problems, the SONOS structure [1.3-1.5] has become an appealing alternative for next-generation Flash memory application. As for SONOS structure in Figure 1-2, the nitride layer is used as the charge-trapping element. The intrinsic distributed storage takes an advantage of the SONOS device over the FG device, and it can improve endurance due to a single defect will not cause the discharge of the memory [1.3]. In addition, it keeps charges from loss by SILC (stress induced leakage current). Furthermore, the programming voltages can be reduced, good retention (over than 10 years), and high endurance (greater than 10^5 cycles) are possible in SONOS structure as the intermediate Si_3N_4 layer is scaled to thicknesses of 50 Å [1.7-1.8].

Figure 1-3 illustrates energy-band diagram of the write/erase operation for SONOS

memory device. The electrons injected from the channel are trapped in the forbidden gap of the silicon nitride layer. The electrons, which are not trapped in the nitride layer, tunnel through the blocking oxide into the gate electrode. It is noted that for SONOS device operation, both electrons and holes are involved in the transport process. It depends on what kind of material poly-Si gate doped.

The simplified ONO gate stack in SONOS memory transistors is economical in scaled CMOS circuits. The compatibility of SONOS technology with advanced CMOS logic technology permits economical integration of NVSM as embedded EEPROMs in ASIC chips. Finally, radiation hardness provides a unique and important feature for advanced military and space systems.

1.2 Motivation

For SONOS cells, there is a mechanism to degrade the ability of charge retention is by trap to trap tunneling (TTT), which means that electron stored in nitride trap directly tunnel through the tunnel oxide to silicon substrate via the interface state.

The cycling degradation to be a manifestation of interface trap generation at the tunnel oxide/silicon interface. In order to reduce the interface trap generation, oxynitride has been used as tunnel dielectric in the fabrication of NVSM devices due to its lower-trap density compared to silicon-rich nitride layers [1.10]. Also, low-barrier tunnel dielectric is necessary to improve the programming speed with the possibility of increasing the retention time if the tunnel dielectric can offer lower gate leakage current compared to the SiO_2 tunnel dielectric.

In addition, a tapered bandgap nitride has been investigated as a storage medium [1.11]. The charge-trapping efficiency of the tapered bandgap nitride increases due to lateral hopping mechanism. Since trapped charges can move to deeper trapping levels from the

shallow trapping levels. On the other hand, charges trapped in deeper trapping levels can be erased clearly by lateral hopping mechanism.

It is desired to have a simple way to obtain high quality oxynitride film and a tapered bandgap nitride, and its process must be suitable for the compatibility with current manufacturing technology of semiconductor industry.

1.3 Organization of the dissertation

This dissertation is divided into four chapters. The contents in each chapter are described as follows.

In chapter 1, the potential memory devices about conventional Flash memory and SONOS memory devices are introduced.

In chapter 2, the studied focus on the introduction of the basic principles of flash memory device.

In chapter 3, the studied describes a SONOS structure has tapered bandgap nitride layer and oxynitride as tunnel dielectric. In addition, a novel process for fabricating this structure is proposed.

In chapter 4, this chapter is included the conclusions and the future work.

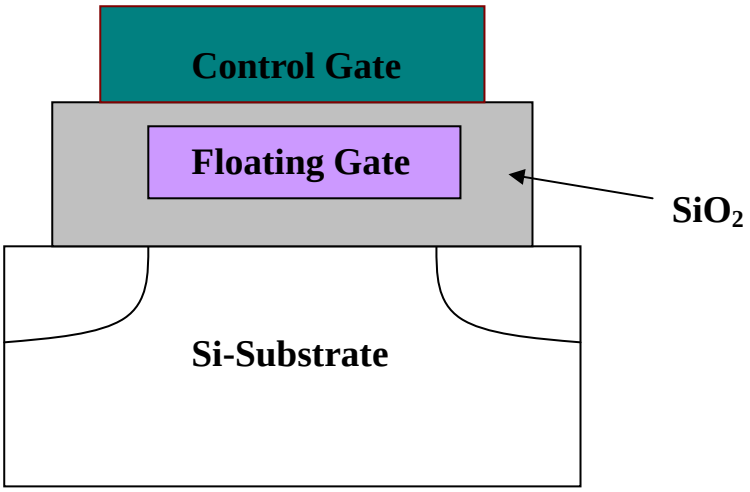


Figure 1-1 Schematic cross section of the conventional floating gate nonvolatile memory device. Continuous poly-Si floating gate is used as the charge storage element.

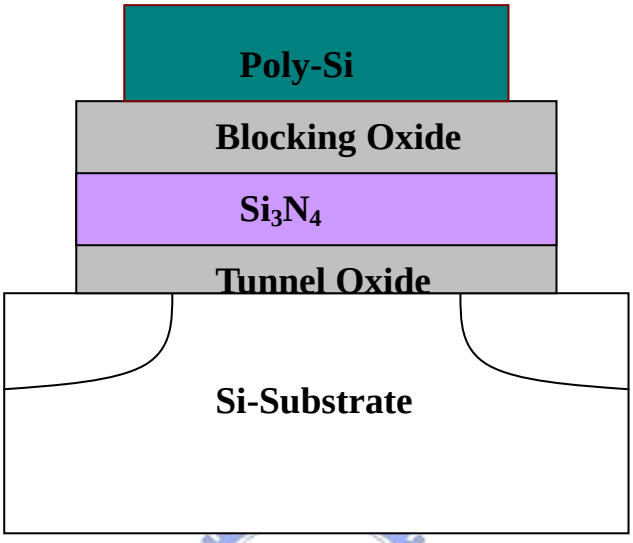


Figure 1-2 Schematic cross section of the SONOS memory device. The nitride layer is used as the charge-trapping element.

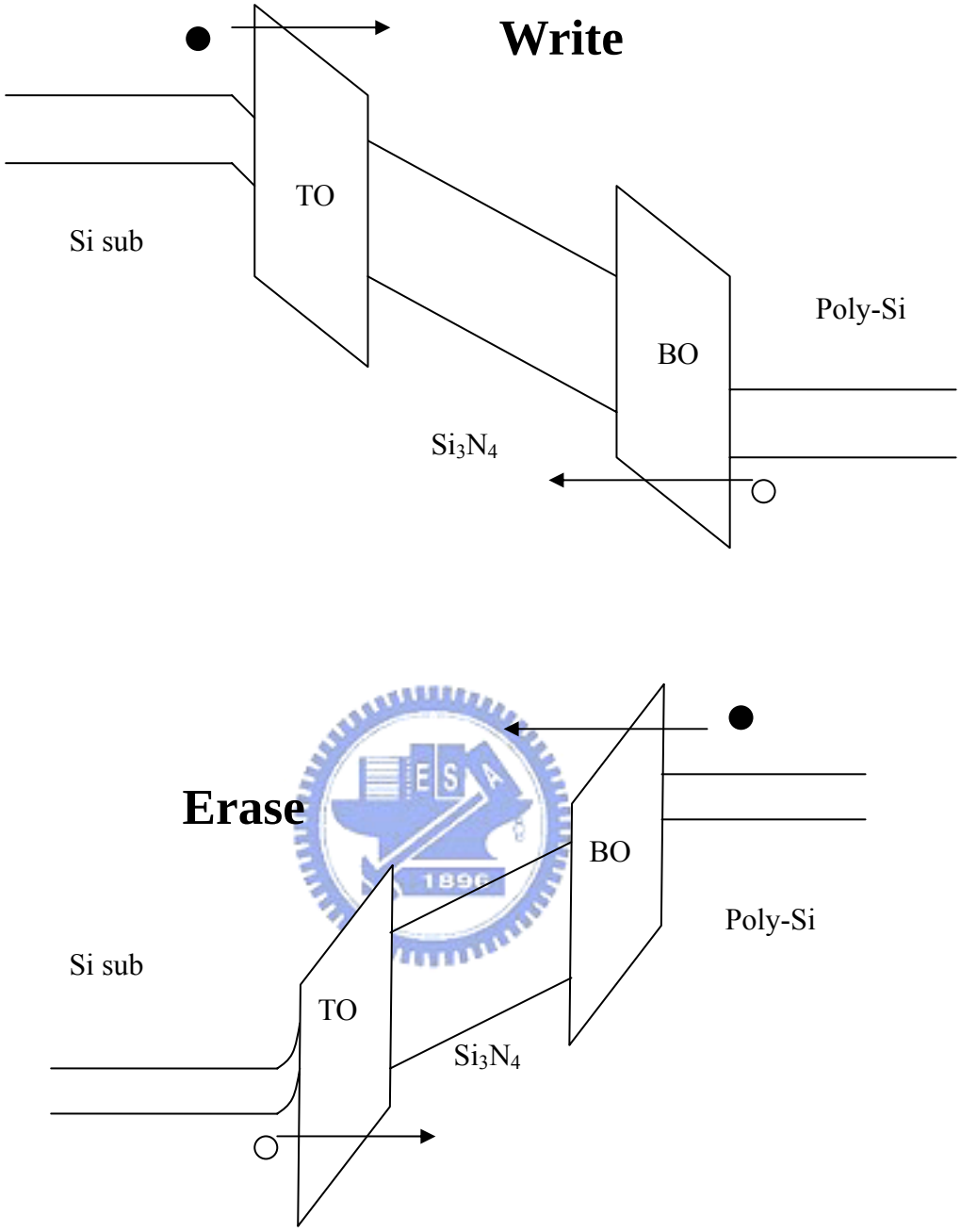


Figure 1-3 Energy band diagram of the write/erase operation for the SONOS memory device.

Chapter 2

Basic principles of SONOS memory

2.1 Introduction

In this chapter, we will introduce the program and erase mechanisms of SONOS memory device. Programming operations involve Fowler-Nordheim tunneling and hot electron injection. In erasing mechanism, Fowler-Nordheim tunneling is mainly used in SONOS memory. Moreover, the reliability characteristic of data retention and endurance will be discussed.

2.2 Operation Mode

In the floating gate memories, four main physical mechanisms are introduced as follows: Fowler-Nordheim tunneling (F-N), modified Fowler-Nordheim tunneling, trap-assisted tunneling, and channel hot-electron injection (CHE). The first three mechanisms are quantum-mechanical tunnel induced by an electric field. The CHE mechanism is that electrons gain enough energy to pass the oxide–silicon energy barrier, due to the electric field in the transistor channel between source and drain.

In the SONOS memory devices, Fowler-Nordheim tunneling (FN), direct band to band tunneling (DT), trap-assisted tunneling (TAT), and modified Fowler-Nordheim tunneling mechanisms (MFN) are the main programming mechanism [2.1].

Generally, channel hot-electron injection and FN tunneling are most utilized to program and erase the flash memories. In this section, these operation mechanisms

will be described briefly.

2.2.1 Fowler-Nordheim Tunneling

Fowler-Nordheim tunneling is a field-assisted carrier tunneling mechanism [2.1]. As shown in Figure 2-1, due to high electrical field, electrons in the p-type substrate conduction band transfer from trapezoidal to triangular energy barrier. At sufficient high fields, an electron current directly tunnel through the oxide from the substrate conduction band into the silicon nitride.

A significant tunnel current can be observed when the tunnel oxide thickness is less than 4nm. However, for thicker tunneling oxide, the electric field is necessary larger or equal to 10MV/cm, the FN tunneling will occurs. The FN tunneling current related formula is shown in Eq. 2-1.

$$J=A*E_{ox}^{2}exp(-B/E_{ox}) \quad \text{.....(2-1)}$$

2.2.2 Channel Hot Electron Injection

Fig. 2-2 shows the cross section view of channel hot electron injection in SONOS memory device. During programming, the positive voltages applied to the gate and drain while the source is grounded. These voltages generate a lateral and vertical electric field along the channel. The electrons will move from the source to the drain and be accelerated by high lateral field near the drain junction in the channel. Once the electrons gain enough energy, they can surpass the energy barrier of the oxide layers and inject into the silicon nitride and be trapped [2.2].

2.2.3 Poole-Frenkel Emission

The Poole-Frenkel is usually used to describe trap-assisted tunneling for a highly defective dielectric [2.3]. For example, silicon nitride is a material which contains a high density of structure defects. As shown in Fig. 2-3, the Poole-Frenkel emission is due to field-enhanced thermal excitation of trapped electrons in the insulator into the conduction band. The current density (J) can be expressed by:

$$J_{PF}=qn_0\mu E_N exp\left[-\frac{q}{kT}\left(\phi_n-\sqrt{\frac{qE_N}{\pi\varepsilon_N}}\right)\right]$$

Due to large density of shallow traps in CVD silicon nitride makes Poole-Frenkel emission a frequently observed and well-characterized mechanism.

2.3 Reliability

Nonvolatility implies at least ten years of charge retention, and the data must be stored in a cell after many read/program/erase cycles. In this section, the reliability issues such as endurance, and retention will be introduced.

2.3.1 Endurance

Flash products are specified for 10^5 program/erase cycles. Cycling is used to investigate the reliability of the flash memory. As the cycling numbers increases, the cell performance will wear out gradually mainly due to the tunnel oxide degradation, which eventually limits the endurance characteristic. Fig. 2-4 shows the typical result

of an endurance test [2.4].

The endurance characteristics give the memory threshold voltage window, which is the difference between the threshold voltages in the programmed state and the erased states. It is the parameters to describe how good the reliable is a nonvolatile memory cell. The P/E cycle usually use the FN tunneling or channel hot electron injection mechanism under room temperature environment.

2.3.2 Retention

Charge detrapping mechanism in SONOS devices and MNOS devices have been studied for more than 30 years. For SONOS memory devices, data are represented as electrons stored in the silicon nitride layer, the stored charges leak away from the trapping layer through the tunnel oxide or through the interpoly dielectrics, and the lateral migration of charges trapped in the silicon nitride layer. [2.5][2.6]. The leakage current, caused by mobile ions, oxide defects, or other mechanisms, results in a shift of the threshold voltage of the memory cell. The threshold voltage shift can also be caused by the detrapping of electrons or holes from oxide traps.

Floating gate flash memories are limited to a rather low number (e.g., 10^5) write/erase cycles due to a low oxide charge-to-breakdown. In contrast, an ultra-thin tunnel oxide can conduct a high current for a dramatic increase in the Q_{ED}, with a concomitant improvement in NVSM reliability for scaled SONOS device.

During retention, trapped electrons can back-tunnel to the conduction band of the silicon substrate, or to the $Si–SiO_2$ interface traps (trap-to-trap tunneling). Meanwhile, holes from the substrate may tunnel through the thin tunneling oxide and become trapped in the nitride.

2.4 Summary

Short data retention and poor endurance are important issues of the SONOS memory device. These issues affect the scalability of thin dielectric such as tunnel oxide. In the following chapter, we propose a novel process to fabricate a SONOS structure to improve the problems of these reliabilities.

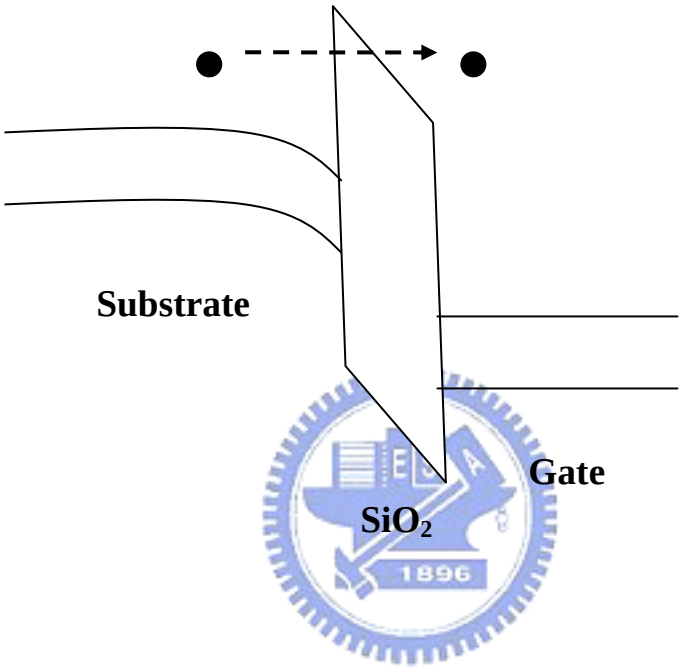


Figure 2-1 Energy-band representation for explaining FN tunneling.

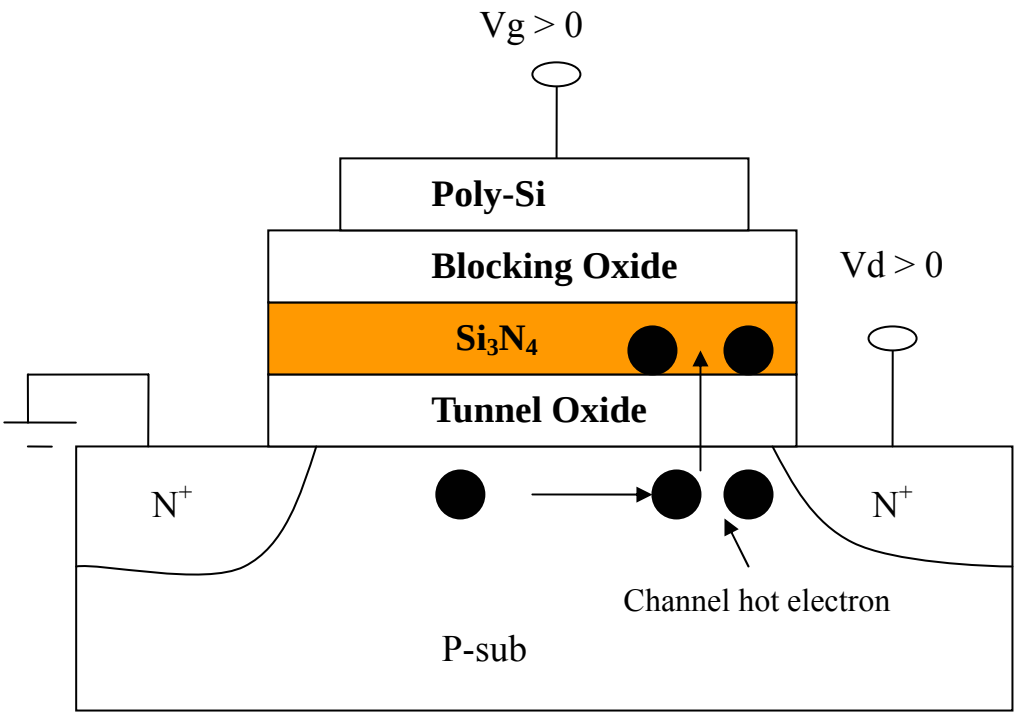


Figure 2-2 Channel hot electron injection in the SONOS memory device.

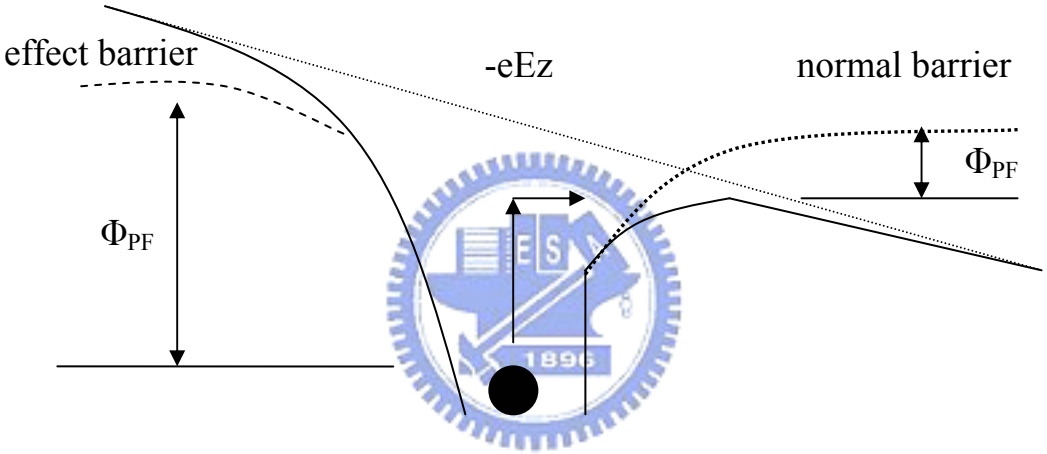


Figure 2-3 Band-diagram of Poole-Frenkel emission.

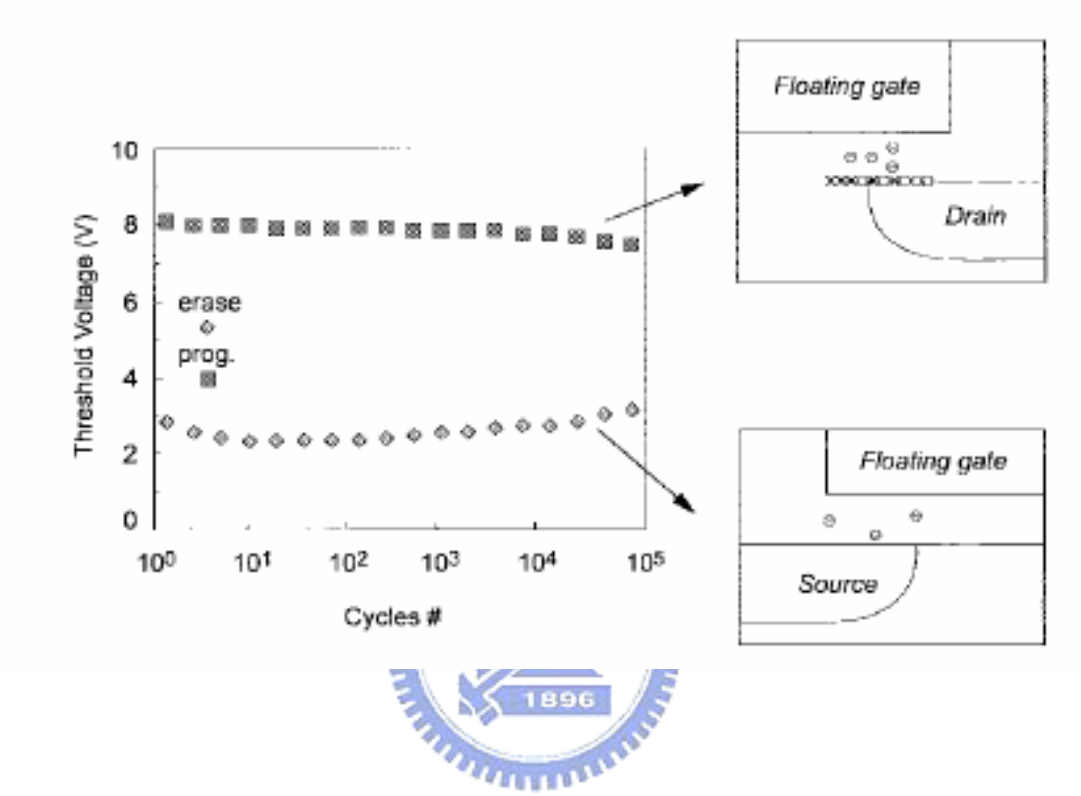


Figure 2-4 A typical endurance characteristic. [2.4]

Chapter 3

Experimental Process and discussion of results

3.1 Introduction

To scale down the thickness of the tunnel oxide in a flash memory is essential to reduce the cell size and the operating voltage. However, a thinner tunnel oxide results in the reliability degradation such as data retention and high-field breakdown characteristics [3.1] [3.2].

Recently, oxynitrides have drawn much attention as a candidate tunnel dielectric for flash memory due to the small charge trapping amount and the low stress-induced leakage current [3.3] [3.4]. In general, benefit of a silicon oxynitride film is the nitrogen in the film accumulates at the silicon interface to reduce the concentration of strained Si-O bond, potentially reducing the creation of hot electrons by as much as three orders of magnitude. Therefore, various approaches have been employed to produce oxynitride tunnel dielectric, such as jet vapor (JVD), remote plasma nitridation (RPN), decoupled plasma nitridation (DPN), and reoxidation of NH_3 nitridation. Unfortunately, they usually require specific equipment or gas. It is desired to have a simple way to obtain the oxynitride film and retain its quality. Meanwhile, chemical oxide as a starting oxide can provide a better controllability in film thickness [3.5]. Nowadays, lower process temperatures and thinner oxynitride films are preferred in ULSI technology.

Furthermore, the charge-trapping efficiency, poor endurance, and short retention are needed to be overcome in next-generation SONOS memory applications. A

tapered bandgap nitride in a SONOS memory device is proposed [3.6]. A tapered bandgap shape causes the charges injected from the substrate fall into shallow trapping levels and are transferred to adjacent deeper levels by lateral hopping. On the contrary, the trapped charges can be erased by transferred from deeper levels to adjacent shallow trapping levels. By this mechanism, more trapping levels are available for storing charges. Therefore, the tapered bandgap nitride can improve the P/E efficiency in SONOS memory.

In this chapter, we proposed a novel process for forming an oxynitride tunnel dielectric with high nitrogen content on the surface, and a tapered bandgap silicon niride layer. The process was mainly divided into four steps. First, a chemical oxide was growth. Then, the chemical oxide was nitridation by NH_3 in a low-pressure chemical vapor deposition (LPCVD) reactor. Subsequently, the silicon nitride was formed in a mixture of NH_3 + SiH_2Cl_2 ambient. Fourth, the silicon nitride was re-oxidized with O_2 in furnace. It is noted that we used the CVD nitride as the trapping layer without using thermal nitride because the oxygen atoms can penetrate into the CVD nitride within 5nm. By this technique, the oxynitride as the tunnel dielectric and a tapered bandgap nitride layer are obtained. Oxynitride with Dit could improve the charge retention of SONOS. In the tapered bandgap silicon nitride, we can obtain Oxygen-rich at the top and N-rich at the bottom of the nitride layer. The desirable structure can be obtained to meet the requirement of the SONOS device performance as shown in figure 3-1. It is noted that the process proposed here is simple and fully compatible with current IC industry fabrication technology.

3.2 Experimental procedures

Figure 3-2 schematically describes a process flow of a SONOS nonvolatile memory.

Experiments were carried out on 4-inch p-type (100)-oriented silicon wafers with a resistivity of 15-25 Ω cm. Wafers were cleaned using standard RCA cleaning. Before growing the chemical oxide film, the wafers were dipped in diluted HF solution to remove native oxides.

Subsequently, the wafers were immediately immersed into H_2O_2 solution at room temperature for 20 min to grow 12Å chemical oxide [3.5]. The chemical oxide was nitrided by LPCVD in low-pressure (180 mTorr) NH_3 ambient at 750℃ for 15 min, and then 30Å Si_3N_4 was deposited by SiH_2Cl_2+ NH_3. Following that, the Si_3N_4 was placed in furance O_2 ambient at 900℃ with various durations (5min and 45min) for reoxidation treatment. Furthermore, 80Å blocking oxide was then deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) followed by a N_2 densification process at 850℃ for 5 min.

Then, 3000Å poly-Si film doped with $POCl_3$ was deposited by low-pressure chemical vapor deposition (LPCVD) at 900℃ for 30 min. Finally, a 5000 Å Al metal film was deposited by sputtering. A 5000Å Al film was also deposited on the backside of wafers after stripping the oxide on the backside. In addition, a conventional SONOS capacitor was fabricated with standard process for comparing with the capacitor fabricated by this novel process. All tunnel dielectric of SONOS capacitors with an area of 10^{-4} was measured. The SONOS capacitors were defined by lithography, and then Al and poly-Si films were etched by wet etching. The process steps of SONOS are shown in figure 3-2.

The film thickness in this thesis was characterized with an ellipsometer. High-frequency (100 kHz) and capacitance-voltage (C-V) characteristics of all SONOS capacitors were measured by HP4284. The Current-Voltage characteristics were measured by HP4156C Precision Semiconductor Parameter Analyzer. The construction of measurement system is shown in figure 3-3.

3.3 Results and discussions

Figure 3-4(a) shows the capacitance-voltage (C-V) hysteresis of the SONOS capacitor after furnace reoxidation 5 minutes at 900℃ in O_2 process. When this capacitor is operated in positive polarity, the electrons directly tunnel from the Si substrate through the tunnel oxide, and are trapped in the forbidden gap of the Si_3N_4 layer. When the capacitor is negatively operated, the holes may tunnel through the tunnel oxide to recombine with electrons trapped in Si_3N_4. The blocking oxide is utilized to prevent the carriers of gate electrode from injecting into the charge-trapping layer by FN tunneling. Figure 3-4(a) and Figure 3-5(a) shows a larger threshold voltage shift than that of the standard SONOS capacitor as shown in figure 3-6(a). As shown in figure 3-4(a) and figure 3-5(a), they are both a counterclockwise direction of the hysteresis, which implies the electrons injected from the deep inversion layer and holes injected from the deep accumulation layer of silicon substrate. In figure 3-4(b), when the voltage applied over the -6V, the leakage current becomes large. However, in figure 3-5(b) and figure 3-6(b), the leakage currents of the capacitor with reoxidation 45min and standard SONOS capacitor are all smaller than that with reoxidation 5min.

In Figure 3-7, when the voltage applied over 6V, the leakage current of the capacitor with reoxidation 45min is smaller than the capacitor with reoxidation 5min about two orders of magnitude. It implies that longer reoxidation time may cause enough oxygen extend into the silicon nitride, and the tunnel oxide. It can reduce the dangling bonds and the positively charged silicon ions in the nitrided-chemical oxide, since hydrogen gas produced by the dissociation of ammonia gas deteriorates the quality of chemical oxide during nitridation. Active hydrogen gas dissolves Si-O bonds in SiO_2 and may result in positively charged silicon ions, proton ions and

dangling bonds. When the gate voltage was close to 8V, the leakage current of the capacitor with reoxidation 45min is almost the same with standard SONOS capacitor. However, the capacitor with reoxidation 45min has a large memory window, it means we can have better charge trapping efficiency than the standard SONOS capacitor, and the leakage current doesn't become large.

Secondary ion mass spectrometry (SIMS) analysis was conducted to characterize the composition of the ONO stack. Figure 3-8 exhibits the SIMS depth profile of the capacitor with reoxidation 45min. Although the SIMS spectra may not show the real distribution of bonds and atoms in this sample, it still provides useful information for study.

As shown in figure 3-8(a), the oxygen concentration at the 52nm is 33%. It is noted that the peak concentration is reduced as depth increases, and also proved that the certain amount oxygen atoms extend into the silicon nitride and nitrided-chemical oxide. When the certain oxygen atoms extend into the nitrided-chemical oxide, the more hydrogen-containing bonds were substituted with oxygen-containing bonds. These hydrogen-containing bonds are necessary to be removed in order to obtain better memory properties. It is noted that oxygen-rich is at the top and the nitrogen-rich is at the bottom in the silicon nitride layer. Figure 3-8(b) shows the tapered bandgap diagram of the SONOS capacitor after reoxidation. The tapered bandgap shape causes a lateral hopping mechanism [3.6], and it helps electrons to be easily erased and programmed. In addition, there is a high nitrogen concentration on the surface of the nitrided tunnel oxide, and it can reduce the Dit.

Figure 3-9 shows the normalized CV curves of SONOS capacitor with reoxidation 5min after different voltage writing 1ms at 25℃. The FN tunneling occurs when the applied voltage is over 18V, however, its leakage current is very large. Figure 3-10 shows the normalized CV curves of SONOS capacitor with reoxidation 5min after

different voltage W/E 1ms at 85℃. The memory window is less than 1V, and it means the W/E time may be too short to obtain an enough memory window to be defined as "1" or "0". Figure 3-11 shows the normalized CV curves of SONOS capacitor with reoxidation 5min after different voltage W/E 10ms at 85℃. The memory window is over 1V. Therefore, an optimal asymmetric W/E operating voltage of 12V/-8V at 10ms was determined. Figure 3.12 shows the normalized CV curves of SONOS capacitor with reoxidation 5min after different voltage W/E 100ms at 85℃. When the writing time reaches 100ms, we found almost all the leakage currents become very large. It could be that there are too many hydrogen atoms in the nitrided-chemical oxide after nitridation without being replaced by oxygen atoms.

Endurance is the capability of maintaining the stored information after W/E cycling. It is the parameters to describe how good the reliable is a nonvolatile memory cell. Figure 3-13 shows the endurance characteristics of the SONOS capacitor with reoxidation 5min. This measurement is performed under accelerated conditions at 85℃. An initial memory window is 1.22V at 85℃. After 10^4 W/E cycles, the memory window is 0.58V. The memory window decreases due to interface-trap generation and lots of dangling bonds. It cause the leakage current becomes large, and deteriorates the quality of the ntrided-chemical oxide due to the presence of hydrogen.

Figure 3-14 ~ figure 3-15 shows the normalized CV curves of SONOS capacitor with reoxidation 45min after different voltage W/E from 1ms to 10ms at 85℃. As shown in Figure 3-14, though we can apply the gate voltage over 18V for writing, the slop of the 18V is getting smoother than the other voltages. It means D_{it} of the 18V is larger than the other voltages. In addition, it is noted that over-erasing may occur after -8V 1ms erasing operation due to the fewer writing time. As shown figure 3-15, we can obtain 1.18V the memory window by 12V/-8V and it is enough to be defined as "1" or "0".

Figure 3-16 shows the endurance characteristics of the SONOS capacitor with reoxidation 45min at 85℃. The initial memory window is 1.18V at 85℃. After 12V/(-8V) W/E 10^4 cycles, it maintains a memory window about 0.84V, which is close to be defined as "1" or "0" for the circuit design.

Figure 3-17 shows the normalized CV curves of the standard SONOS capacitor after different voltage W/E 10ms at 85℃. Due to Pool-Frenkel and FN tunneling effect, the ONO stack can't be applied the voltage over 14V. It makes the tunnel oxide breaks down. Figure 3-18 shows the endurance of the standard SONOS capacitor. The initial memory window is 1.08V at 85℃. After 10^4 cycles, the memory window is just 0.6V. The decaying rate is faster than the capacitor with 45min reoxidation.

Figure 3-19~ figure 3-22 shows the surface roughness comparison. The different AFM samples were presented in table 3-1. We compare A1 with A2, surface roughness increase from 0.219 to 0.279. It means the chemical oxide with nitridation treatment have a good uniform surface than the one which directly deposits Si_3N_4 layer without nitridation treatment. We compare A3 with A4, surface roughness increase from 0.215 to 0.257. The furnace oxide with nitridation still has a better uniform surface. Nitridation treatment provides better uniform surface due to the enough incubation time, similar material characteristics and the coefficient of thermal expansion between the nitride and oxide film. A good memory device will have a less leakage current due to a uniform surface.

3.4 Summary

We have proposed a novel process for forming an oxynitride as the tunnel oxide and a tapered bandgap nitride as the trapping layer. The capacitor with reoxidation 45min obtains an enough memory window to define "1" or "0" for logic circuit and

the better endurance performance. Most importantly, the process we proposed is not complicated and could be successfully integrated into current ULSI technology.

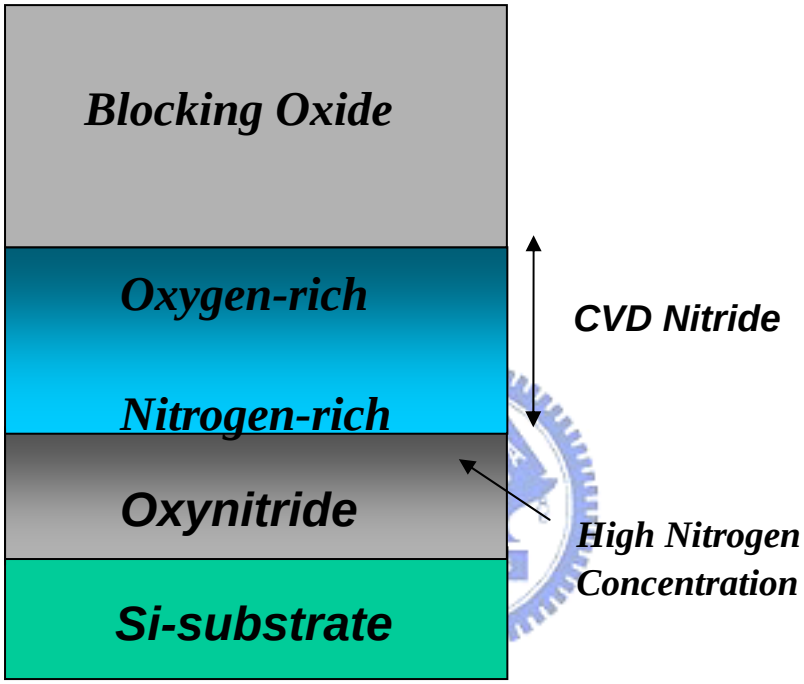


Figure 3-1 Schematic cross section of the ONO structure after reoxidation.

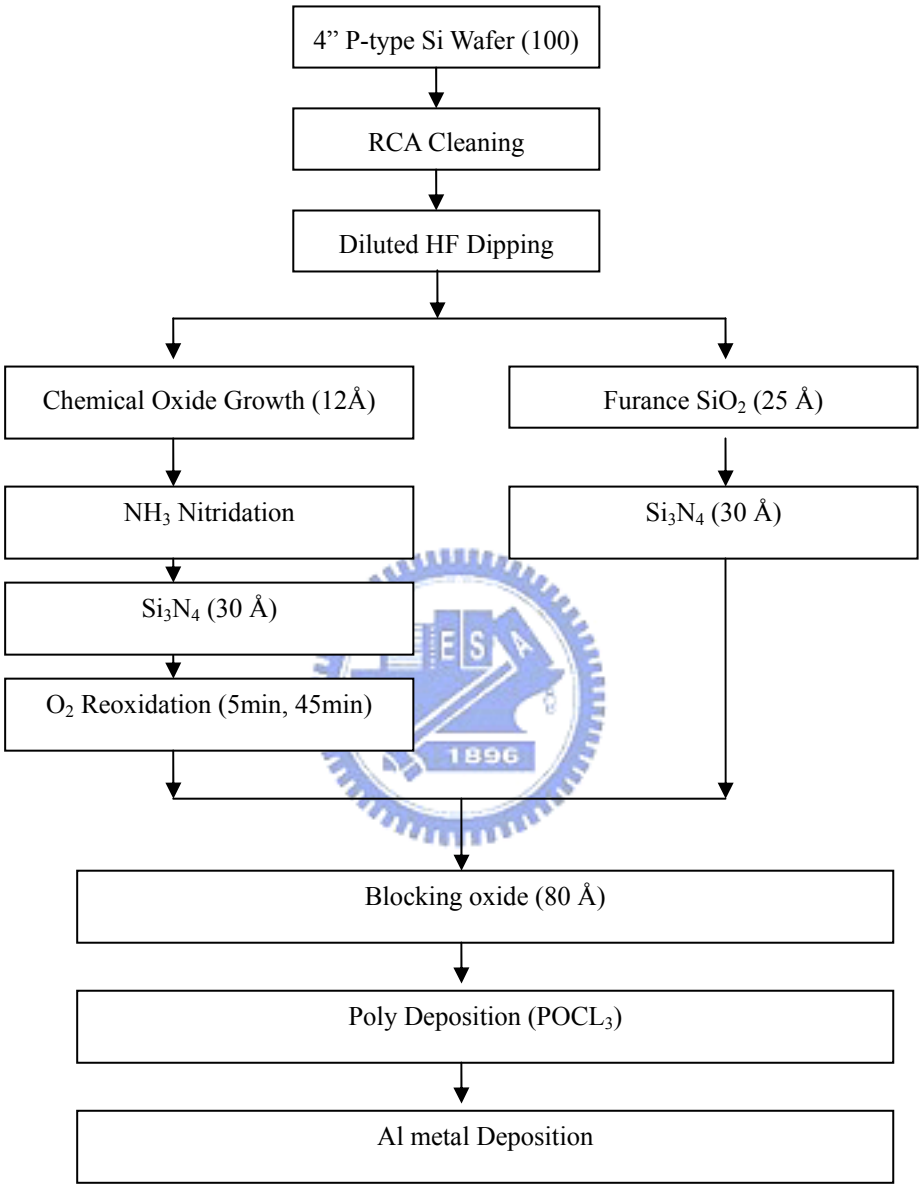


Figure 3-2 Process flows for fabricating various SONOS capacitors.

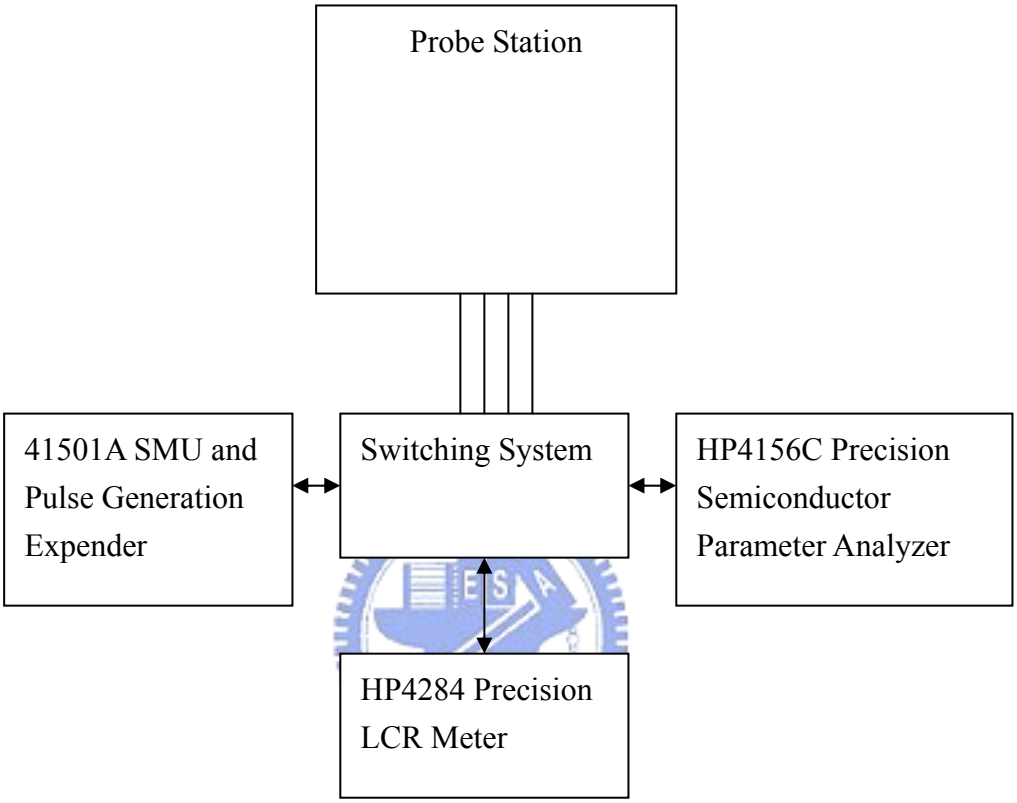


Figure 3-3 The construction of measurement system

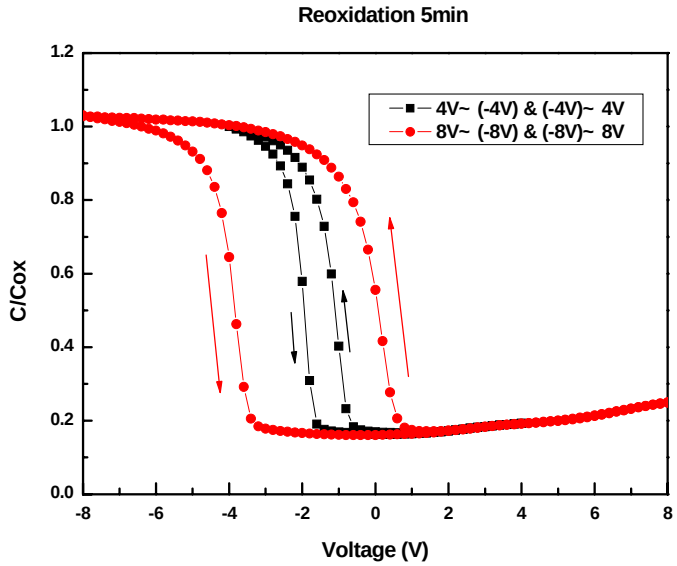


Figure 3-4(a) The C-V hysteresis of the capacitor with reoxidation 5min in O_2 process after bidirectional sweeps.

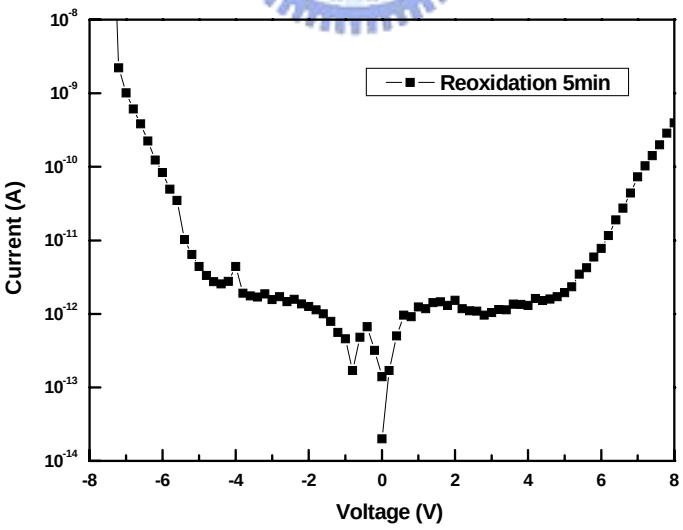


Figure 3-4(b) The leakage current of the capacitor with reoxidation 5min in O_2 process.

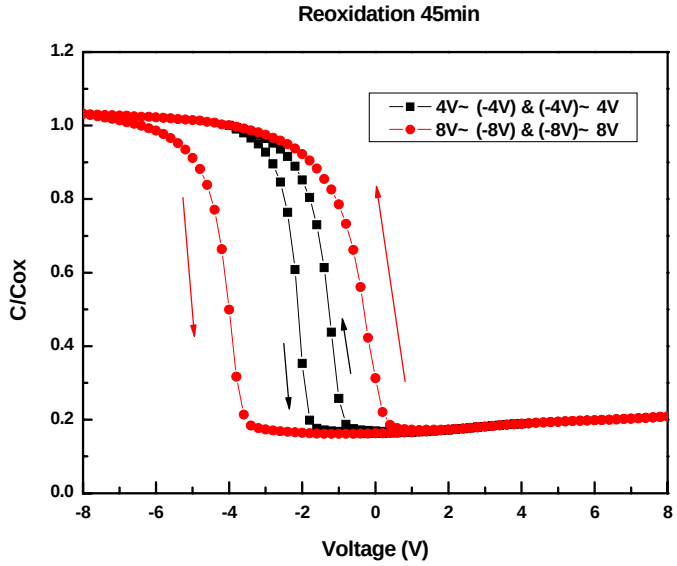


Figure 3-5(a) The C-V hysteresis of the capacitor with reoxidation 45min in O_2 process after bidirectional sweeps.

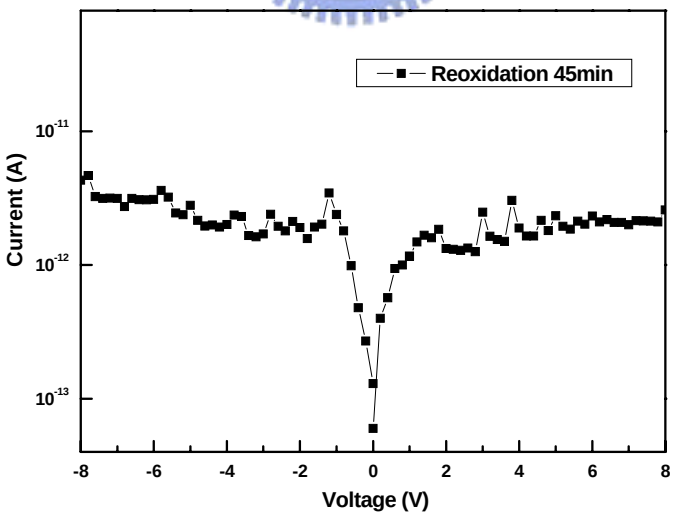


Figure 3-5(b) The leakage current of the capacitor with reoxidation 45min in O_2 process.

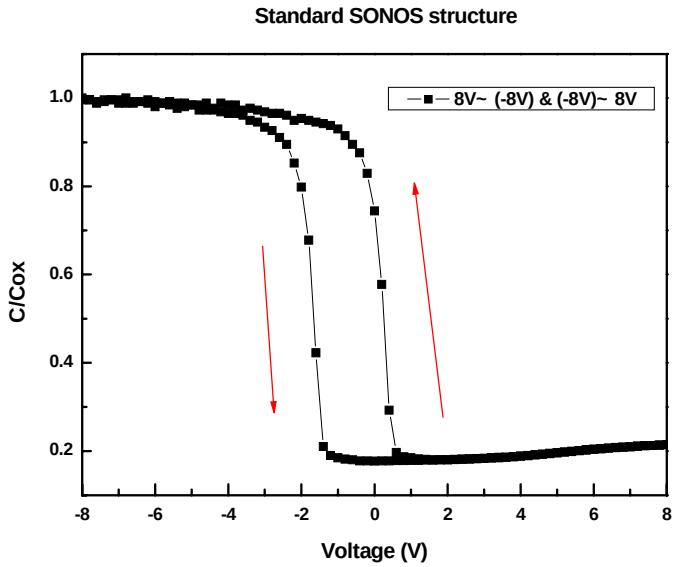


Figure 3-6(a) The C-V hysteresis of the standard SONOS capacitor without reoxidation after bidirectional sweeps.

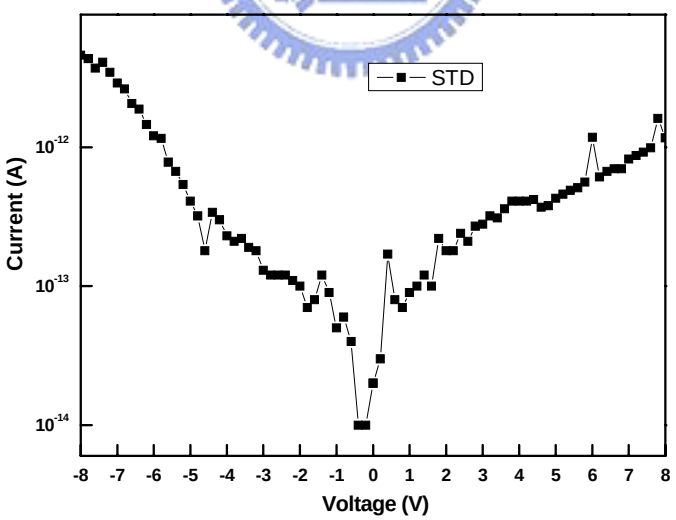


Figure 3-6(b) The leakage current of the capacitor with standard SONOS capacitor.

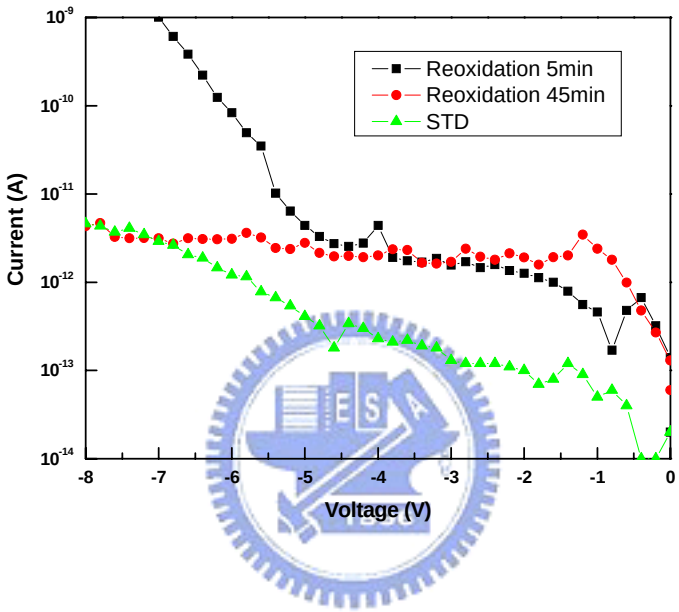


Figure 3-7 Comparison of I-V characteristics of the capacitor with reoxidation 5 min, reoxidation 45min, and standard SONOS capacitor.

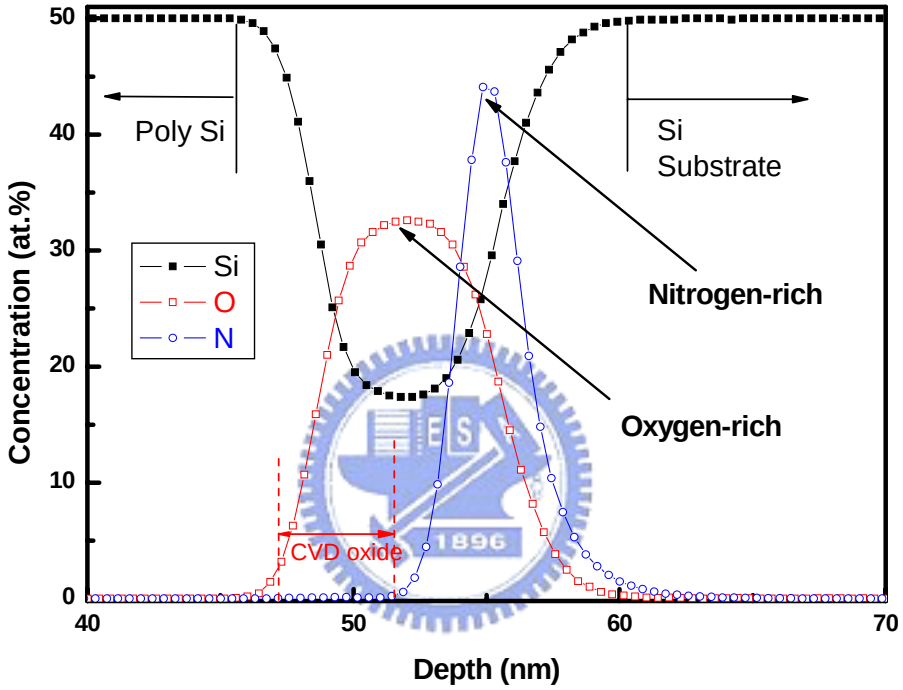


Figure 3-8(a) The SIMS depth profile of the capacitor with reoxidation 45min.

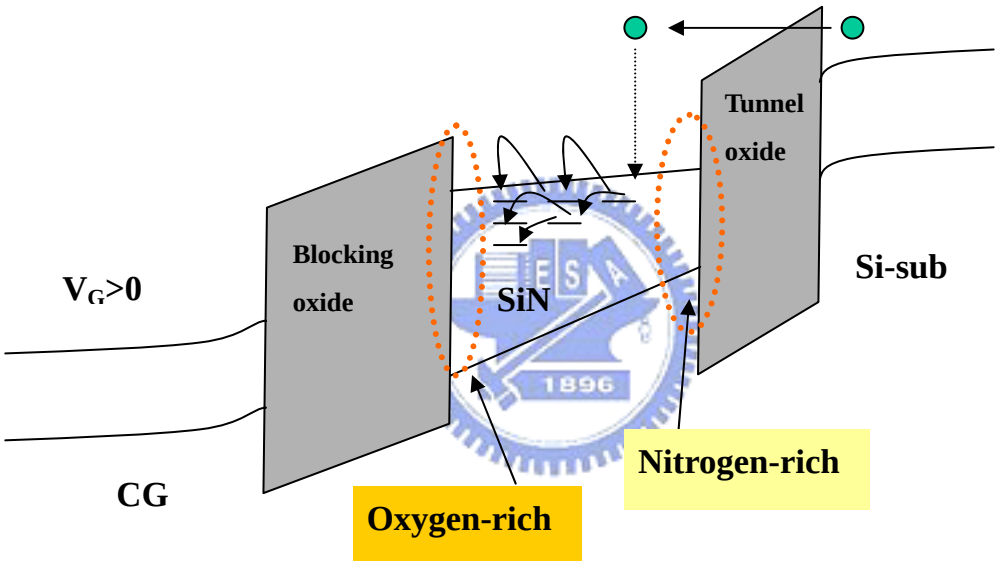


Figure 3-8 (b) The band diagram of the SONOS capacitor after reoxidation.

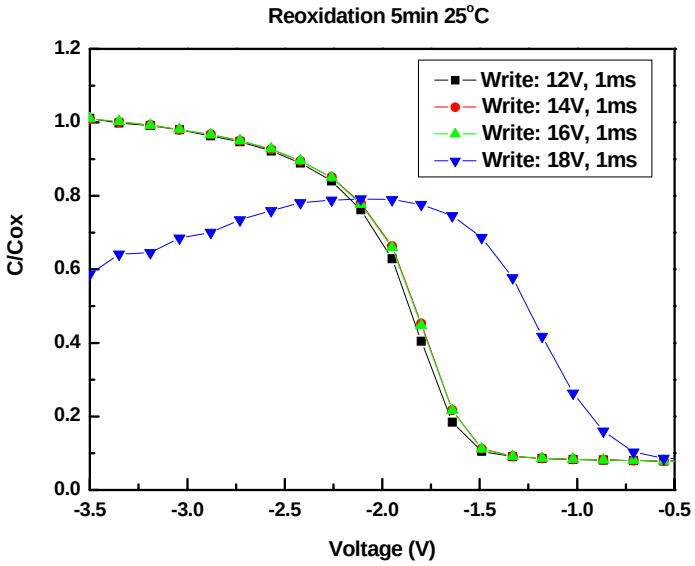


Figure 3-9 Normalized C-V curves of SONOS capacitor with reoxidation 5min after different voltage writing 1ms at 25℃.

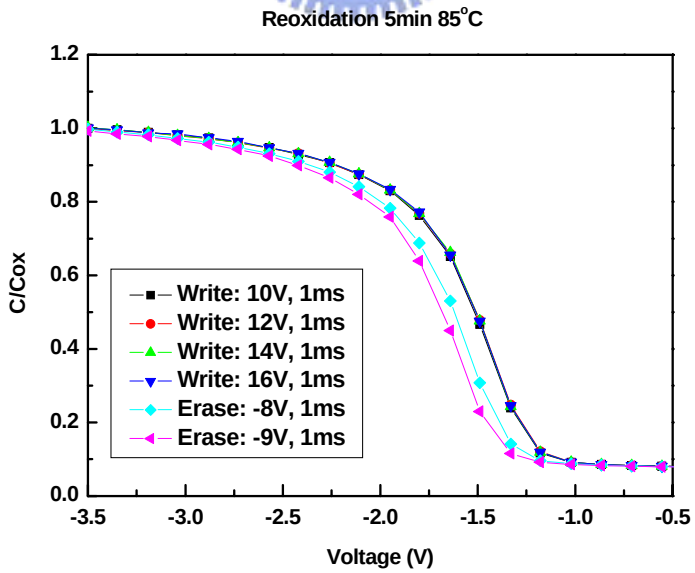


Figure 3-10 Normalized C-V curves of SONOS capacitor with reoxidation 5min after different voltage W/E 1ms at 85℃.

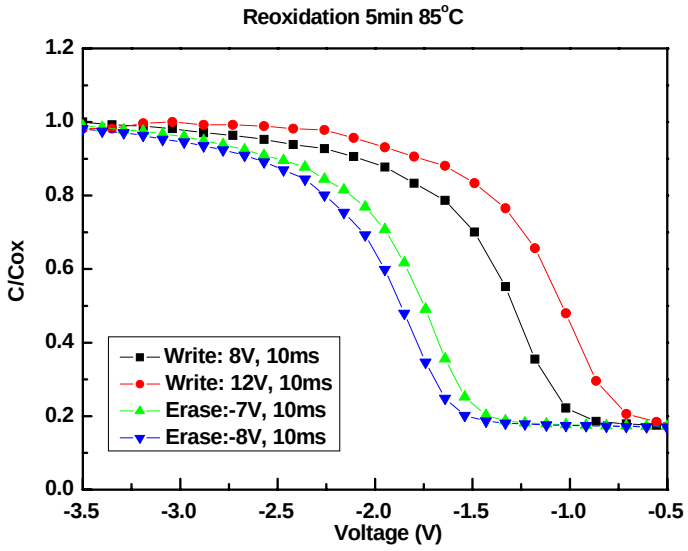


Figure 3-11 Normalized C-V curves of SONOS capacitor with reoxidation 5min after different voltage W/E 10ms at 85℃.

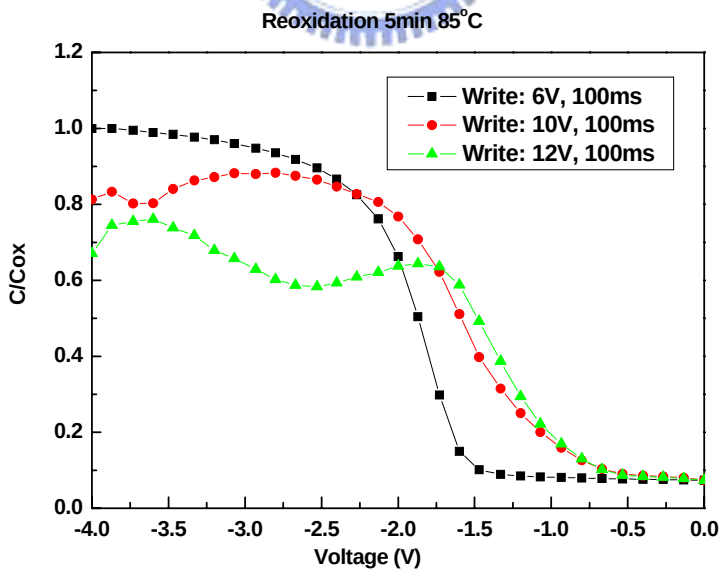


Figure 3-12 Normalized C-V curves of SONOS capacitor with reoxidation 5min after different voltage W/E 100ms at 85℃.

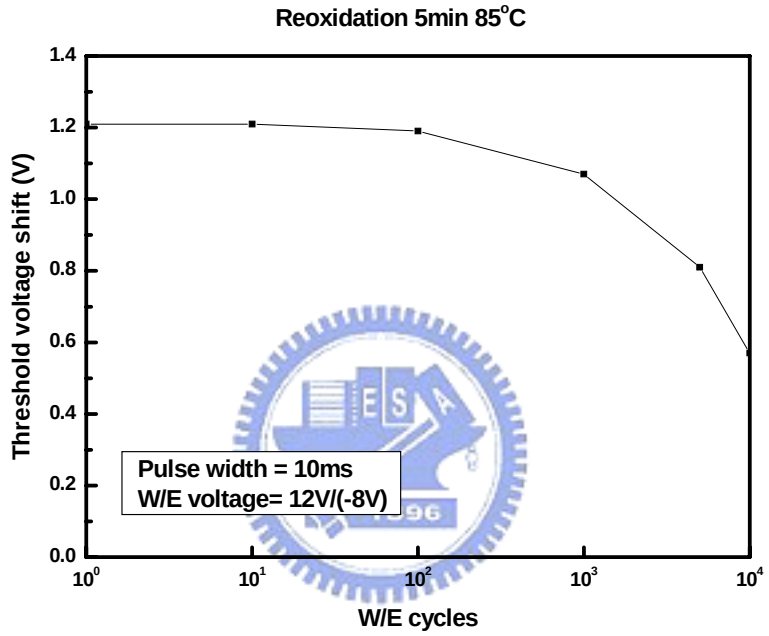


Figure 3-13 Endurance characteristics of the SONOS capacitor with reoxidation 5min at 85℃.

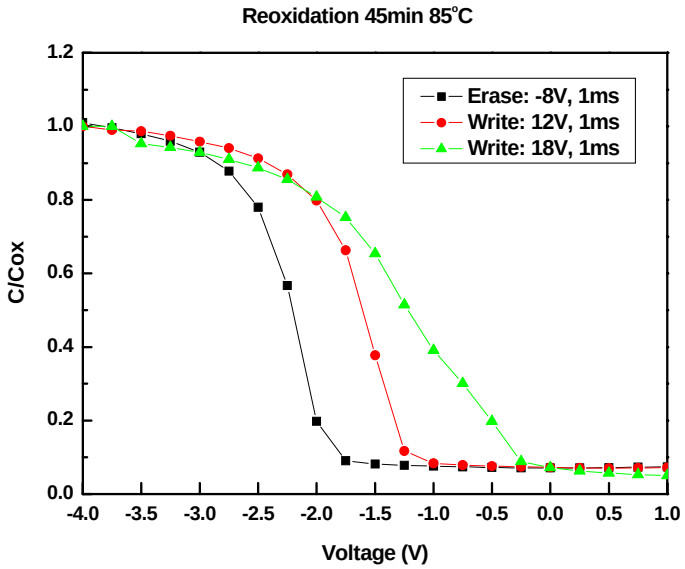


Figure 3.14 Normalized C-V curves of SONOS capacitor with reoxidation 45min after different voltage W/E 1ms at 85℃.

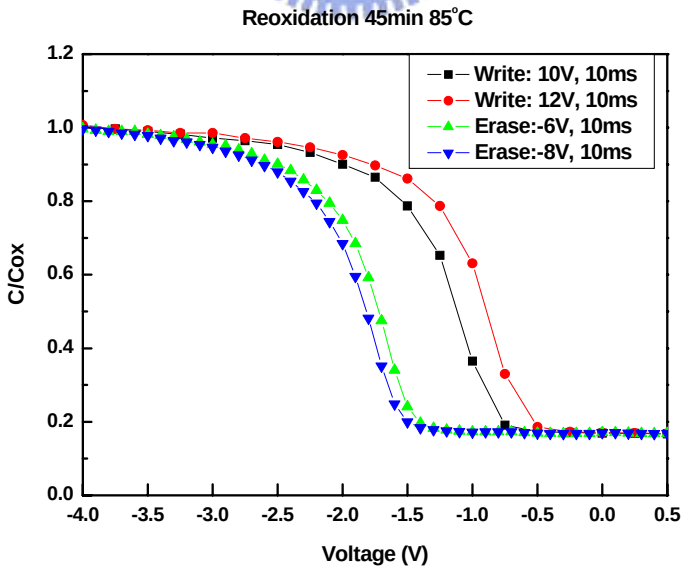


Figure 3-15 Normalized C-V curves of SONOS capacitor with reoxidation 45min after different voltage W/E 10ms at 85℃.

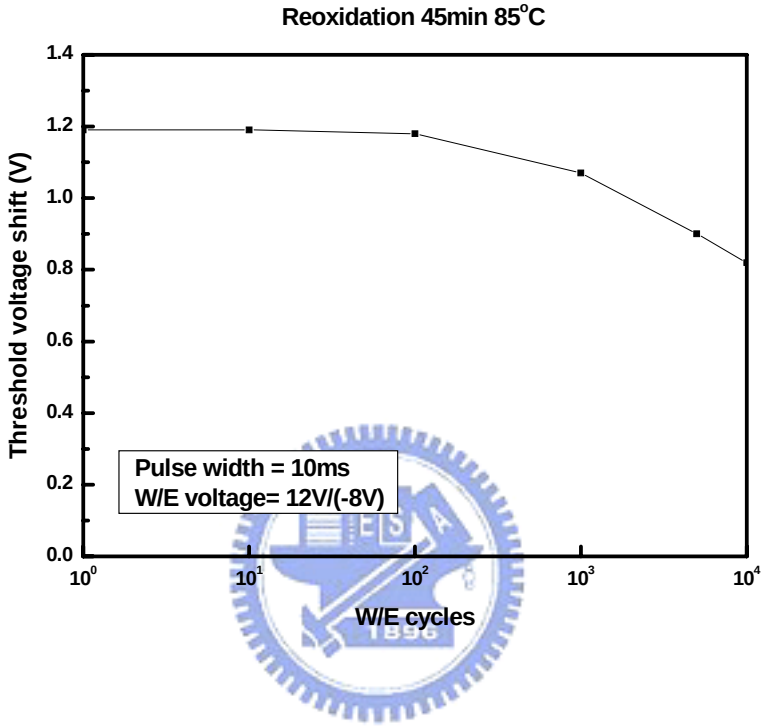


Figure 3-16 Endurance characteristics of the SONOS capacitor with reoxidation 45min at 85℃.

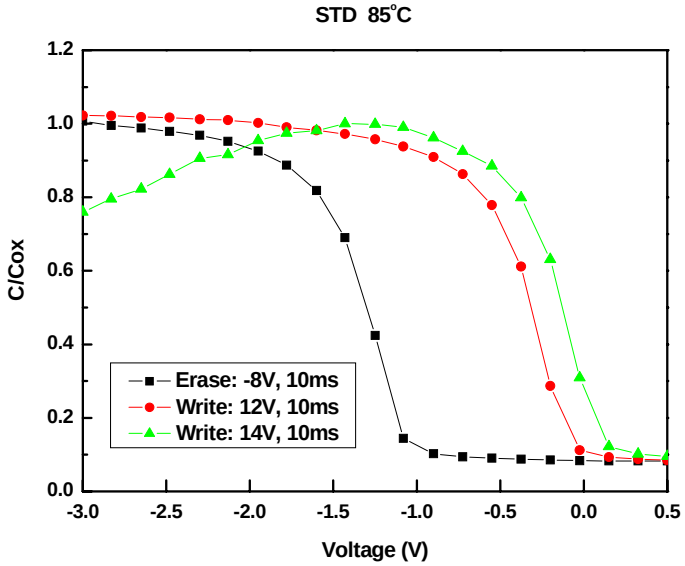


Figure 3-17 Normalized C-V curves of standard SONOS capacitor after different voltage W/E 10ms at 85℃.

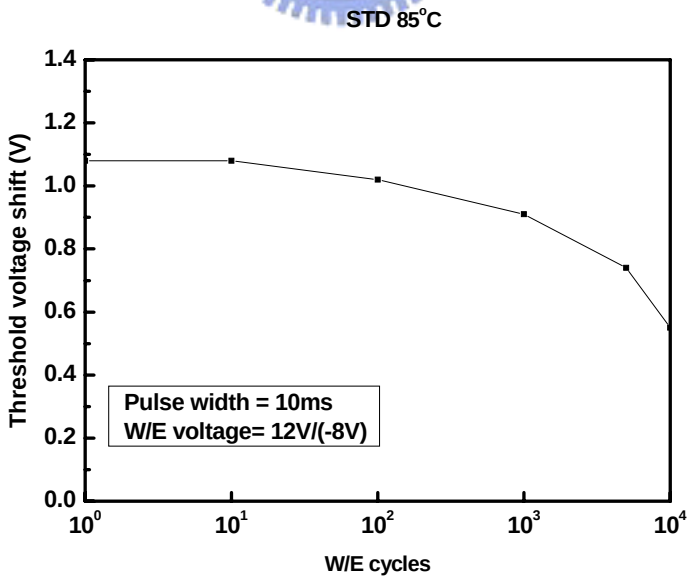
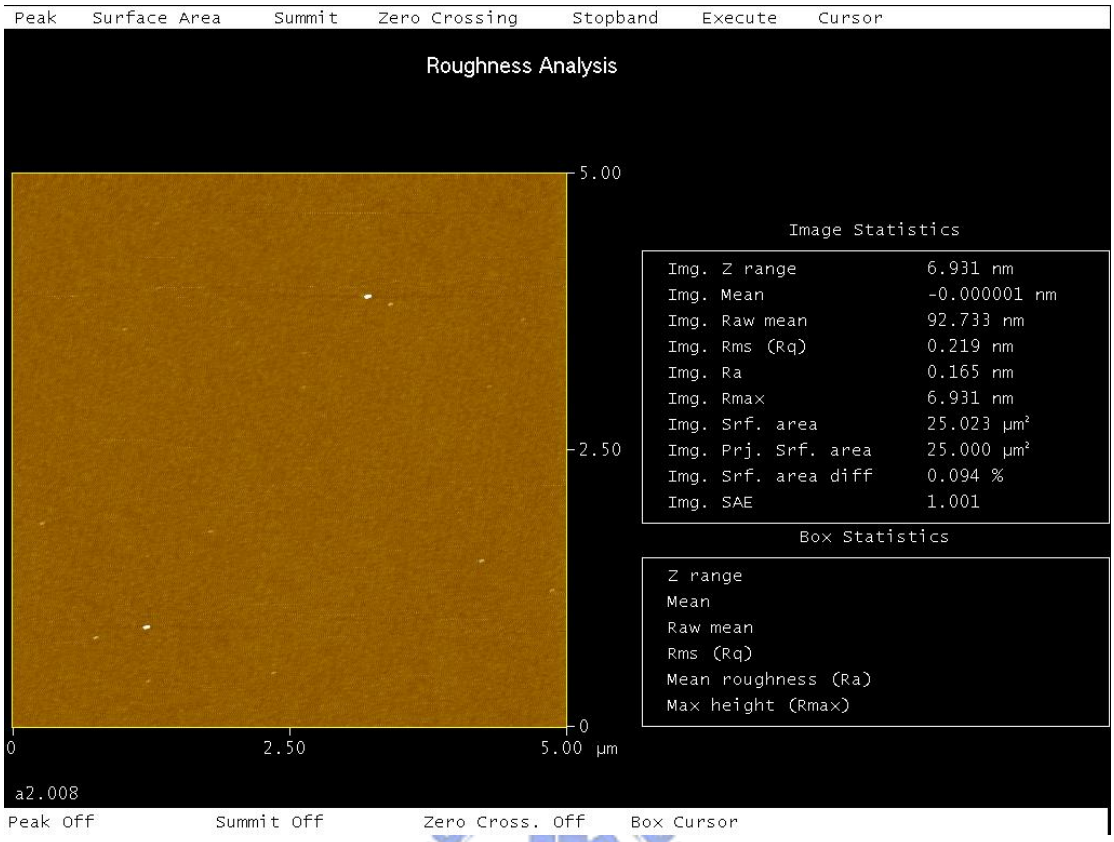


Figure 3-18 Endurance characteristics of standard SONOS capacitor at 85℃.



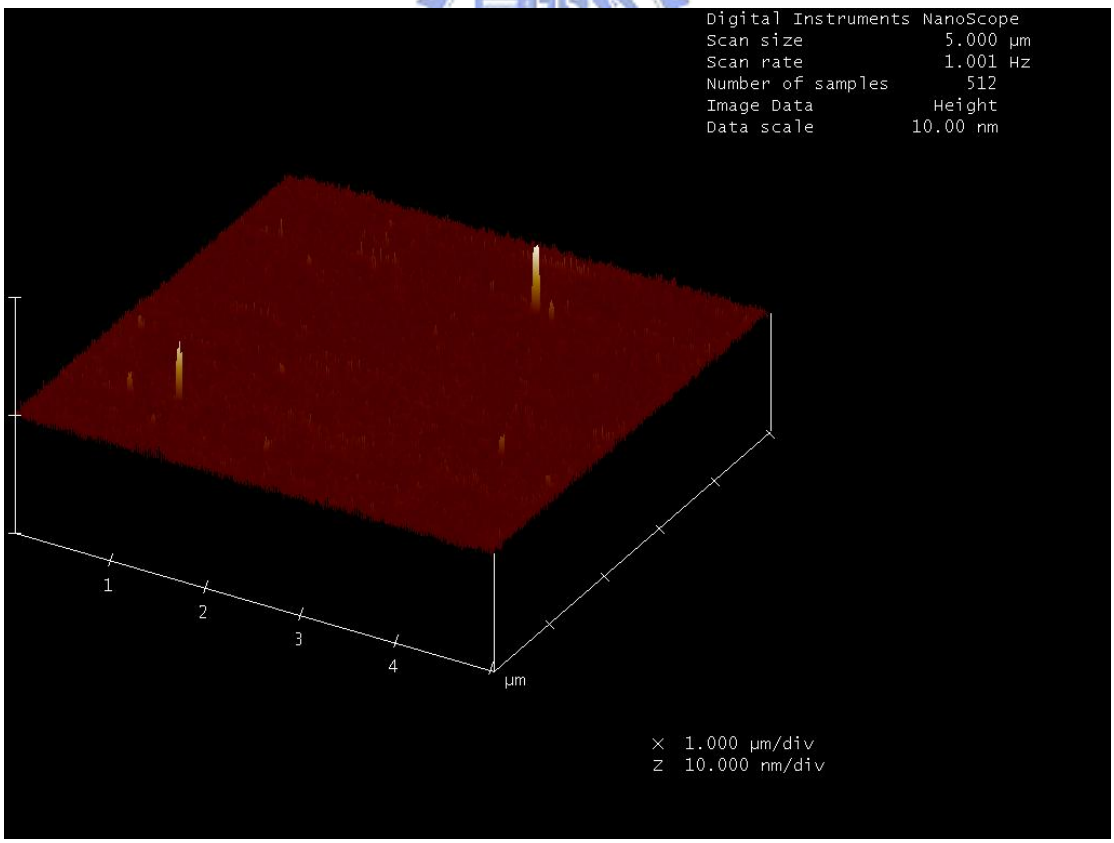
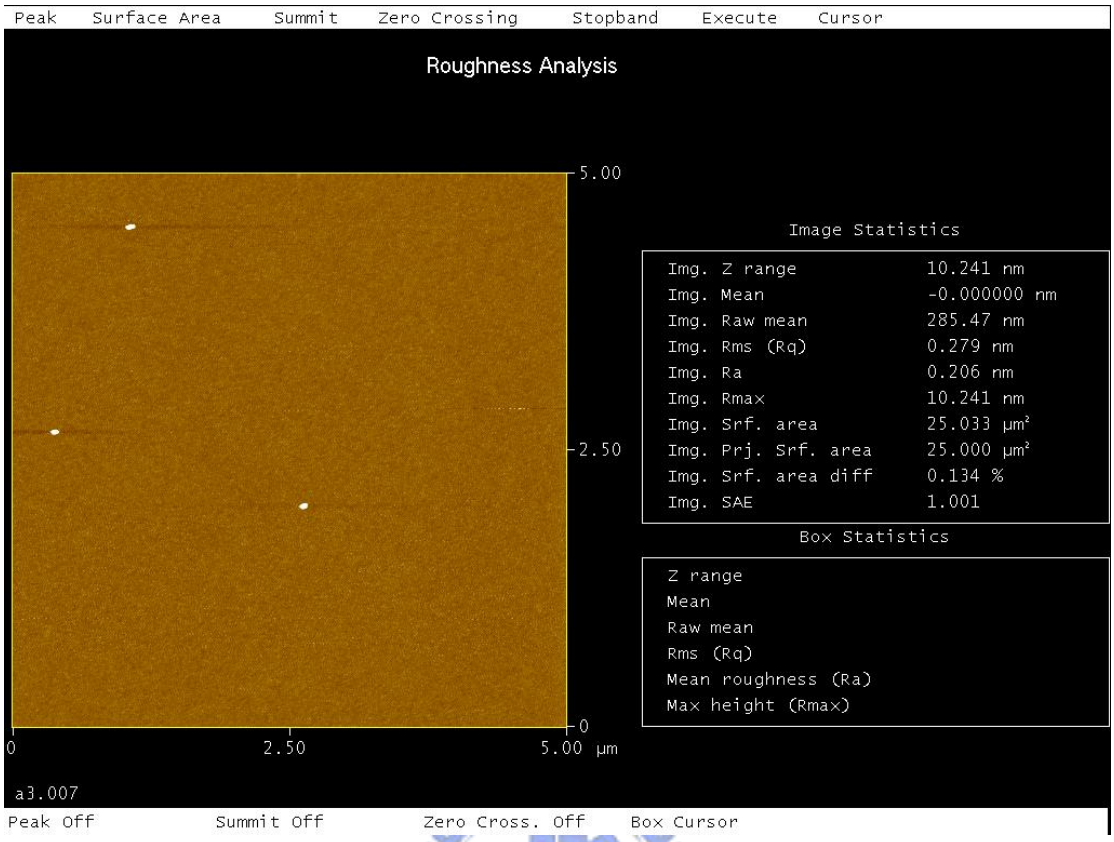


Figure 3-19 (a) and (b) AFM topography of chemical oxide/Si_3N_4 structure with nitridation.



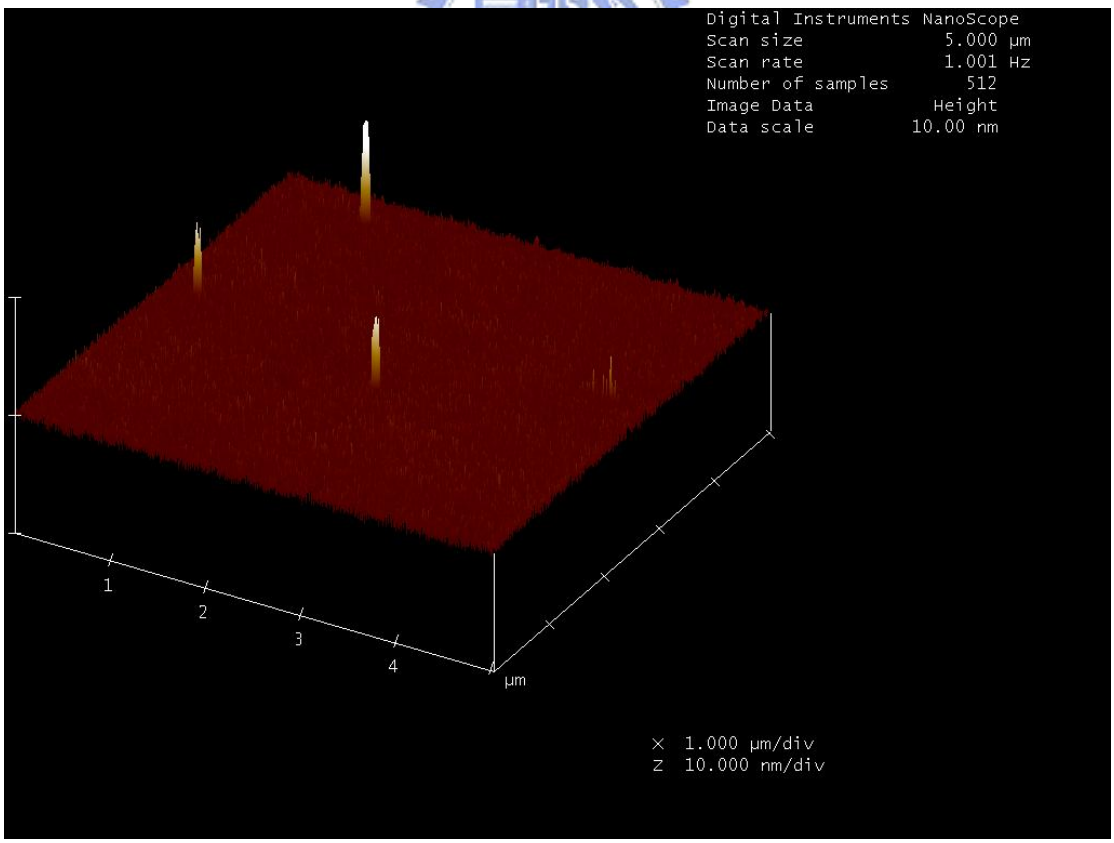
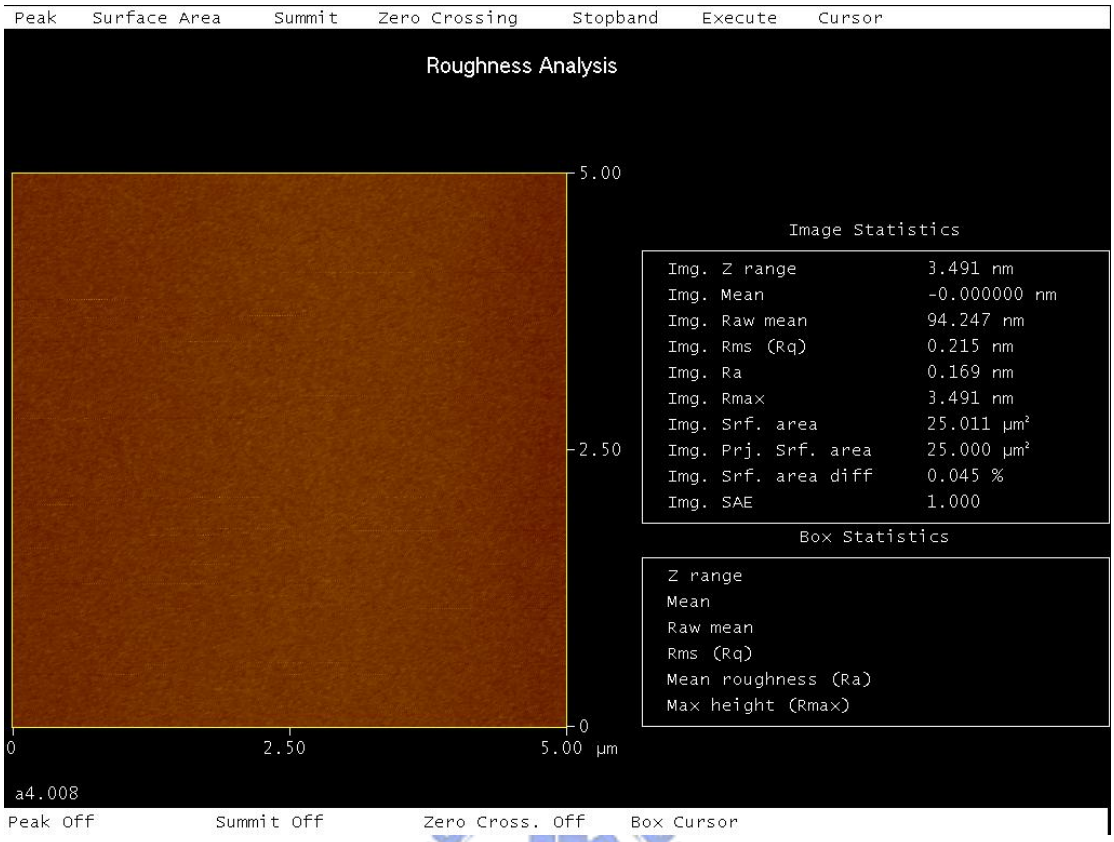


Figure 3-20 (a) and (b) AFM topography of chemical oxide/Si_3N_4 without nitridation.



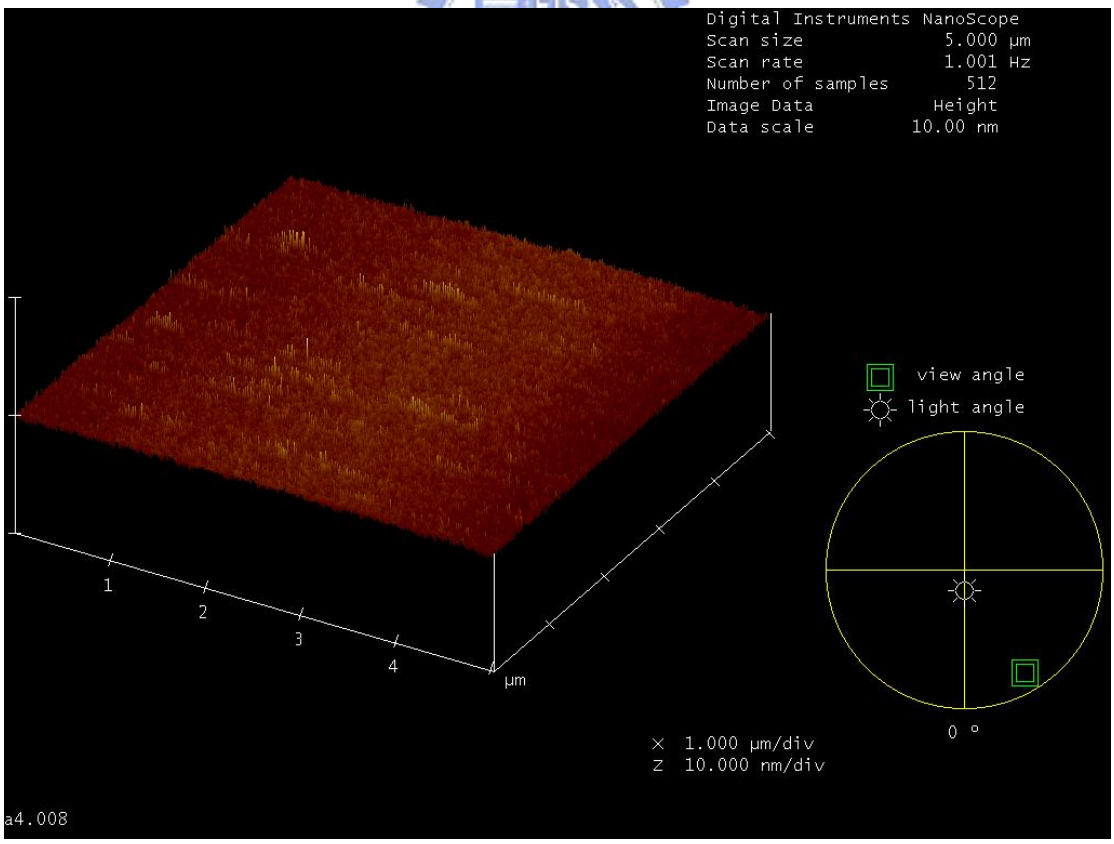


Figure 3-21 (a) and (b) AFM topography of furnace SiO_2/Si_3N_4 structure with nitridation.

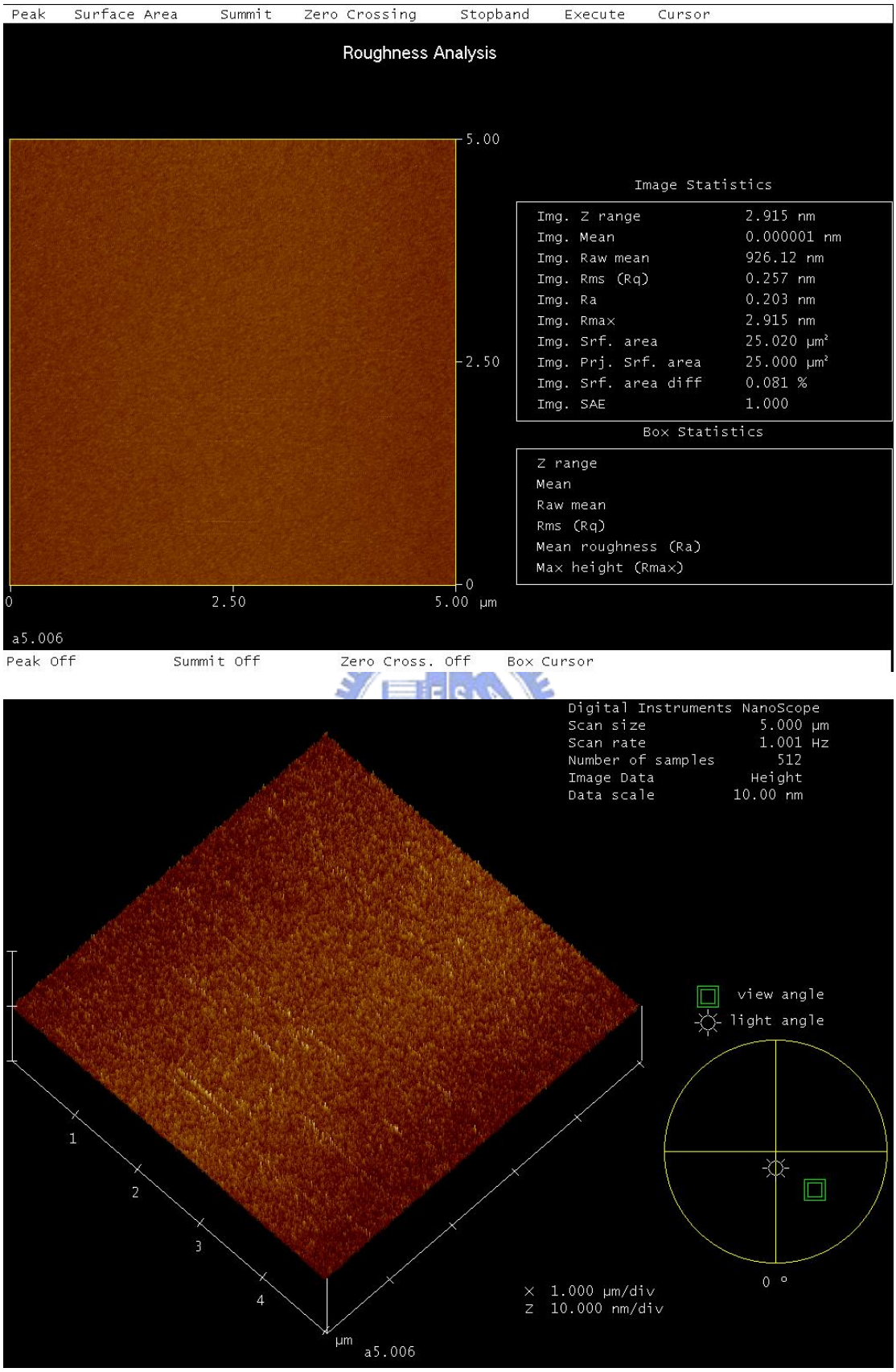


Figure 3-22 (a) and (b) AFM topography of furnace SiO_2/Si_3N_4 structure without nitridation.

Spilt number	Structure	RMS(nm)
A1	Chemical oxide + nitridation + Si_3N_4	0.219
A2	Chemical oxide + Si_3N_4	0.279
A3	Furnace SiO_2 + nitridation+ Si_3N_4	0.215
A4	Furnace SiO_2 + Si_3N_4	0.257

Table 3-1 Process conditions of different AFM samples.

Chapter 4

Conclusions and Suggestions for Future Work

4.1 Conclusions

We propose a novel process to fabricate a SONOS cell storage. This process mainly included four process stages – chemical oxide growth, nitridation, forming the Si_3N_4 and subsequent dry O_2 reoxidation. We obtain the oxynitride as the tunnel oxide, and a tapered bandgap nitride for trapping electrons in a SONOS structure. Meanwhile, chemical oxide as a starting oxide can provide a better controllability in film thickness. In addition, chemical oxide with nitridation treatment can provide a uniform surface. The process we proposed is simple and fully compatible with current manufacturing technology of semiconductor industry.

Finally, by this technique, the SONOS capacitor with 45min reoxidation demonstrates the better electrical characteristics than the capacitor with reoxidation 5min and the standard SONOS capacitor.

4.2 Suggestions of Future Work

1. More HRTEM images to evidence the thickness variation of tunneling oxide and silicon nitride.
2. More SIMS measurements to evidence the distribution of the atoms and bonds in the ONO stack
3. Fully Fabricated stacked-gate flash memory device to study the device

characteristics, including program/erase speed, retention time, endurance, read-disturb and charge loss mechanism.

References

Chapter 1:

[1.1] D. Kahng, and S. M. Sze, “A floating gate and its application to memory devices,” *Bell Syst. Tech, J.*, 46, 1288 (1967).

[1.2] J. D. Blauwe, “Nanocrystal nonvolatile memory devices”, *IEEE Transaction on Nanotechnology*, 1, 72 (2002).

[1.3] H. E. Maes, J. Witters, and G. Groeseneken, *Proc. 17 European Solid State Devices Res. Conf. Bologna 1987*, 157 (1988).

[1.4] M. H. White, Y. Yang, A. Purwar, and M. L. French, ”A low voltage SONOS nonvolatile semiconductor memory technology,” *IEEE Int’l Nonvolatile Memory Technology Conference*, 52 (1996).

[1.5] M. H. White, D. A. Adams, and J. Bu, “On the go with SONOS,” *IEEE circuits & devices*, 16, 22 (2000).

[1.6] W. D. Brown and J. E. Brewer, “Nonvolatile Semiconductor Memory Technology,” *IEEE press New York*, p. 309, 1998.

[1.7] T. Noraki, T. Tanaka, Y. Kijiya, E. Kinoshita, and T. Tsuchiya. “A 1 Mbit EEPROM with MONOS Memory Cell for Semiconductor Disk Application,” *IEEE Journal of Solid-State Circuits*, 26(4):497-501, April 1991.

[1.8] F.R.Libsch, A. Roy, and M.H. White. “A True 5V EEPROM Cell for High Density NVSM,” *IEEE Pansactions on Electron Devices*, 34(11):2372, 1987. 45th Annual Device Research Conference (IEEE) Santa Barbara, CA, June 1987.

[1.9] Xu D, Kapoor VJ. “Effects of oxygen content and oxide layer thickness on interface state densities for metal – oxynitride – oxide – silicon devices,” *J Appl Phys 1991*;70(3).

[1.10] Kamagaki Y, Minami S, Kato H. “A new portrayal of electron and hole traps in amorphous silicon nitride,” *J Appl Phys 1990*;68:2211.

[1.11] Kuo-Hong Wu, Hua-Ching Chien, Chih-Chiang Chan, Tung-Sheng Chen, and Chin-Hsing Kao, “SONOS Device With Tapered Bandgap Nitride Layer,” *IEEE Trans. Electron Devices*, vol. 52, 2005.

Chapter 2:

[2.1] J. Bu and M. H. White. Aerospace Conference Proceedings, 2002. IEEE , Vol. 5 , pp. 2383, 2002.

[2.2] Bez, R., Camerlenghi, E., Modelli, A., and Visconti, A., "Introduction to flash memory," *Proc. IEEE*, 2003, 91, pp. 489 – 5028.

[2.3] J. R. Yeargan, and H. L. Taylor, "The Poole-Frenkel Effect with Compensation Present," *Journal of Applied Physics,* vol.39, 1968, pp.5600.

[2.4]P. Cappelletti, R. Bez, D. Cantarelli, and L. Fratin, "Failure mechanisms of Flash cell in program/erase cycling," *IEDM Tech. Dig.*, 1994, pp. 291–294.

[2.5] Yakov Roizin, Micha Gutman, Efraim Aloni, Victor Kairys, Pavel Zisman, "Retention Characteristic of micro FLASH Memory (Activation Energy of Traps in the ONO stack)".

[2.6] W. J. Tsai, S. H. Gu, N. K. Zous, C. C. Yeh, C. C. Liu, C. H. Chen, Tahui Wang, Sam Pan and Chih-Yuan Lu, "Cause of Data Retention Loss in a Nitride-Based Localized Trapping Storage Flash Memory Cell," *IEEE 40th Annual International Reliability Physics Symposium*, 2002, pp. 34~38.

Chapter 3:

[3.1] S. Aritome, R. Shirota, G. Hemink, T. Endoh and F. Masuoka, “Reliability Issues of Flash Memory Cells,” *Proceedings of IEEE*, Vol. 81, 1993, pp. 776-787.

[3.2] K. Naruke, S. Taguchi and M. Wada, “Stress Induced Leakage Current Limiting to Scale Down EEPROM Tunnel Oxide Thickness,” *IEEE IEDM Tech. Dig.*, 1988, pp. 389-392.

[3.3] U. Sharma, R. Moazzami, P. Tobin, Y. Okada, S. K. Cheng and J. Yeargain, “Vertically Scaled, High Reliability EEPROM Devices with Ultra-thin Oxynitride Films Prepared by RTP in N20/02 Ambient,” *IEEE IEDM, Tech. Dig.*, 1992, pp. 461-464.

[3.4] H. Fukuda, M. Yasuda, T. Iwabuchi and S. Ohno, “Novel N_2O-Oxynitridation Technology for Forming Highly Reliable EEPROM Tunnel Oxide Films,” *IEEE Electron Device Lett.*, Vol. 12, 1991, pp. 587-589.

[3.5] B. C. Lin, K. M. Chang, C. H. Lai, K.Y. Hsieh and J. M. Yao, “Reoxidation Behavior of High-Nitrogen Oxynitride Films after O2 and N2O Treatment,” *Jpn. J. Appl. Phys.*, vol. 44, pp.2993-2994, 2005.

[3.6] Kuo-Hong Wu, Hua-Ching Chien, Chih-Chiang Chan, Tung-Sheng Chen, and Chin-Hsing Kao, “SONOS Device With Tapered Bandgap Nitride Layer,” *IEEE Trans. Electron Devices*, vol. 52, 2005.

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碩士論文題目：

新穎的 SONOS 儲存單元製程之研究

A Study of Novel SONOS Cell Storage Process