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碩士論文

複晶矽薄膜電晶體製程效應與偏壓溫度不穩定性之研究

Study on Process Effects and Bias Temperature Instability of Poly-Si Thin-Film Transistors

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摘　要

在本論文中，首先，我們在閘極氧化層沉積後利用高溫通氧的條件來提升閘極氧化層的可靠度。另外我們在成長薄膜電晶體通道之前，運用低溫低壓的條件預沉積一氧含量較高的薄膜矽襯墊層，因為較高的氧含量會抑制固相再結晶(Solid-Phase Crystallization) 時的成核。藉由這個方式，可以在通道中形成更大的晶粒尺寸(Grain size) ，藉而得到更高的載子場效遷移率。我們發現，特別是在小尺寸的元件中，預沉積矽襯墊層有效的提高複晶矽薄膜電晶體 (poly-Si TFTs) 的場效遷移率、驅動電流，並有效降低閘極引發汲極漏電流 (GIDL current) 以及次臨限擺幅 (Subthreshold Swing)。再者藉由使用預沉積矽襯墊層，也改善了元件的可靠度以及均勻性。

接著，我們分別對 p-通道複晶矽薄膜電晶體進行負偏壓溫度不穩定性 (Bias Temperature Instability) 之研究，以及對 n-通道複晶矽薄膜電晶體進行正偏壓溫度不穩定性對於元件可靠度的影響之研究。我們分別探討不同的溫度以及所施加的偏壓，對於上述兩種偏壓溫度不穩定性在元件退化所造成的影響。實驗結果顯示，正、負偏壓溫度不穩定性在低溫複晶矽薄膜電晶體中會有著不同的退化機制，但對於元件可靠度都有很大程度的影響。

最後，我們探討動態負偏壓溫度不穩定性對於 p-通道複晶矽薄膜電晶體可靠度的影響。藉由不同的偏壓方式，我們可以發現元件在進行負偏壓溫度不穩定性之測試時所產生的缺陷狀態，會在正閘極偏壓下被修補。在 CMOS 反向器使用中，這樣的修補會使得元件使用期限大幅提升，藉由使用動態負偏壓溫度不穩定性測試，可以得到更貼近現實使用下的元件使用期限。

Study on Process Effects and Bias Temperature Instability of Poly-Si Thin-Film Transistors

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ABSTRACT

In this thesis, first, we used a post-anneal procedure with oxygen ambient after the deposition of gate oxide. Poly-Si TFTs with such a post-anneal procedure have enhanced electrical characteristics and much improved reliability. In addition, we deposited a buffer amorphous Si (a-Si) layer under both low temperature and pressure before the deposition of the channel. Si layers grown under this condition would have higher oxygen concentration, and this would suppress the nucleation mechanism under solid-phase crystallization (SPC). With the buffer Si layer, the bi-layer Si, with a-Si layer beneath the poly-Si channel after the SPC process, would have larger grain size and lead to enhanced performance. Measurements revealed that the devices' electrical characteristics are improved not only in field effect mobility and gate-induced-drain leakage (GIDL) current, but also in driving current and

subthreshold swing. Moreover, the ability of immunity against hot-carrier injection and device uniformity are improved.

Then, we studied the degradation mechanisms of negative bias temperature instablity (NBTI) and positive bias temperature instability (PBTI) in p- and n-channel low-temperature polycrystalline silicon thin-film transistors (LTPS TFTs), respectively. As the stress gate voltage increases, the absolute values of threshold voltages shift ($|\Delta V_{th}|$) increase under NBTI and PBTI stress. When the stress temperature is raised, the $|\Delta V_{th}|$ increases under NBTI stress but almost unchanged under PBTI stress, indicating that the degradation mechanisms of NBTI and PBTI are different. Furthermore, the field-effect mobility is rarely changed under NBTI stress; however, it increases under PBTI stress. From the experimental results, we demonstrated that the NBTI degradation can be explained by the diffusion-controlled electrochemical reactions, while the PBTI degradation is caused by charge trapping in the gate dielectric.

Finally, we investigated the impact of dynamic NBTI in p-channel LTPS TFTs. In conventional NBTI studies, static gate bias is used to determine the lifetime of p-channel LTPS TFTs. However, DNBTI in p-MOSFETs showed that the lifetime was much longer than that derived from static NBTI stress because of the passivation effect. We found that LTPS p-TFTs have passivation effect under positive gate bias during a stress-passivation-stress process. As a result, we would underdetermine the true lifetime of LTPS p-TFTs when we use static NBTS to derive it. Therefore, it is necessary to use DNBTS to simulate the bias condition of their really applications.

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Contents

TABLE CAPTIONS

Chapter 2

Chapter 3

FIGURE CAPTIONS

Chapter 2

Chapter 3

Chapter 4

Chapter 1

Introduction

1.1 Overview of Poly-Si Thin-Film Transistors

In recent years, thin-film transistors (TFTs) have been widely investigated in industrial applications, such as active-matrix liquid-crystal displays (AMLCDs) [1-3], high density static random access memories (SRAMs) [4], electrical erasable programming read only memories (EEPROM) [5][6], linear image sensors [7], photodetector amplifiers [8], and also candidates for 3-D ICs' applications [9], etc. Within those applications, the application of active-matrix liquid-crystal displays (AMLCDs) is the major driving force to promote the developments of poly-Si TFT technology.

It is known that hydrogenated amorphous silicon (a-Si:H) TFTs were used for the pixel switching device at the first generation of AMLCDs. The advantages of a-Si:H TFTs are their compatibility with low processing temperature on large-area glass substrates and high off-stated impedance which result in a low leakage current. However, the low electron mobility ($\leqq 1$ $cm^2/V \cdot s$) make it hard to realize the integration of the switching pixels with the peripheral driver circuits in one signal substrate to further reduce the production cost of AMLCDs. It was until 1966, the first polycrystalline silicon thin film transistors (poly-Si TFTs) were fabricated by C. H. Fa *et al.* [10]. In comparison with a-Si TFTs, poly-Si TFTs have superior carrier mobility, higher CMOS capability, and better reliability. The high driving current of poly-Si TFTs makes the integration of switching pixels and driver circuits possible [11].

Moreover, the aperture ratio (A.R.) and the panel brightness can also be greatly promoted for the sake of the scaling device size, needed using poly-Si [12]. Therefore, the performance of display can be significantly improved. As a result, poly-Si TFTs have a great potential to realize both high-performance and large-area AMLCDs, and further to accomplish System-on-Panel (SOP).

The study of poly-Si TFTs fabrication with the maximum process temperature below 620°C was not commenced until 1980s. These TFTs fabricated with such low maximum process temperature are so-called Low-Temperature Poly-Si (LTPS) TFTs. With such low process temperature, poly-Si TFTs could be fabricated on inexpensive, low-melting point, and large-area glass substrates. So far, many crystallization techniques have been proposed to achieve LTPS TFTs, such as solid-phase crystallization (SPC) [13-16], metal-induced crystallization (MIC) [17-19], metal-induced lateral crystallization (MILC) [20-22], and laser annealing crystallization [23-27], and etc. Among these techniques, excimer lacer annealing (ELA) crystallization is believed to become the mainstream technology for mass production because high-quality poly-Si films can be obtained.

Compared to the single crystal silicon, the performance of poly-Si TFTs are strongly related to grain boundaries and intra-grain defects. For example, defects in the grain boundary would trap carriers and generate a potential barrier which degrades the on-stated current of poly-Si TFTs. Moreover, the grain boundaries also provide the path of leakage current. In order to obtain desirable electrical characteristics of poly-Si TFTs, it is necessary to improve the device performance by enlarging the grain size of poly-Si films [28] and reducing the trap states in grain boundaries to raise the field effect mobility. Additionally, there were other methods such as plasma treatments to passivate the defects in the channel or narrowing the channel width to reduce the trap state density [29-32].

Moreover, novel structures are also used to fabricate high-performance poly-Si TFTs. These techniques are focus on the reduction of the electric field near the drain junction, thus suppress the OFF-state leakage current of the device. Many structures such as multi-channel ones [33], offset drain/source ones [34], lightly doped drain (LDD) ones [35], field induced drain ones [36], and etc. have been proposed and investigated intensively.

1.2 Overview of Bias Temperature Instability

With the continuous scaling of the dimensions of transistors, negative bias temperature instability (NBTI) stress in p-MOS transistors has become one of the most critical reliability issues which determine the lifetime of CMOS devices [37]-[40]. In the contrary, positive temperature instability (PBTI) stress ultimately determine the lifetime of n-MOS transistors, especially of high-*k* n-MOS transistors [41]-[47]. Hot carrier stressing and Fowler–Nordheim tunneling can cause degradation both near the SiO_2 /Si interface [48] [49] and in the bulk of gate oxide [50]-[52], while BTS only induces degradation within a few nm of the interface [53] [54]. In conventional NBTI studies, the degradation refers to the generation of positive oxide charge and interface traps under negative gate bias at elevated temperature, especially in p-channel MOSFETs. While NBTI includes both interface state generation and positive oxide charge formation [55]-[58], PBTI only exists the formation of donor-like interface states [59].

NBTI was first reported by Miura and Matukura [37], named as Instability Number VI by Deal [60], and further researched by Goetzberger et al., which was one of the first groups at Bell Labs trying to show the detailed characterization of NBTI [61]. Despite numerous efforts in researching the NBTI degradation mechanism, it

has not been fully understood till now. Hot carrier injection (HCI) would no longer play the dominator in device when the gate oxide thickness of device is shrunk to nm scale due to the reducing applied operation voltage. However, NBTI is more and more severe for ultra-thin oxides because of the increasing interface trap density induced by it. Recently, NBTI has been identified as one of the major reliability concerns for deep sub-micron pMOSFETs [62]. During negative-bias-temperature stressing (NBTS), typical stress temperature lies in the 100-250°C range, a large number of interface states and positive fixed charges are generating. Either negative gate voltage or elevated temperatures can produce NBTI, but a stronger and faster effect is produced by their combined action. Additionally, the higher the origin interface trap density ($D_{it)}$ is, the higher the final stress-induced D_{it}. The D_{it} increased with gate voltage and time with a time dependence of $t^{0.25}$, D_{it} (T=250°C) > D_{it} (T=150°C), and devices with p-type substrates give higher D_{it} than devices with n-type substrate do. The shift in threshold voltage and degradation in transconductance have been suggested to be due to the interfacial electro-chemical reactions related to the holes from the channel inversion layer. During the NBTS, both fixed oxide charges and interface trap density (D_{it}) increase. However, the generation of fixed oxide charges is independent of oxide thickness, while the interface trap generation is inversely proportional to oxide thickness.[63] This suggests that NBTI is worse for thinner oxide.

In the other hand, it is found that the importance of PBTI in nMOSFETs could be as critical as that of NBTI in pMOSFETs. Various models have been proposed to explain PBTI with Vt shift or on-current degradation. There are roughly two kinds of models which explain the mechanisms responsible for the degradation in PBTI stress. One of these models indicates that the degradation due to PBTI stress is owing to the charge de-trapping from the high-k gate insulator, which possesses numerous defects.

This kind of models has ignored the influence of the generation of trap states under the PBTI stress. Another kind of models shows that there is still another mechanism which causes degradation except the charge de-trapping mechanism, i.e., the trap creation mechanism. As a result, it is necessary to take the trap creation during a positive-bias-temperature stressing (PBTS) into consideration.

Both NBTI and PBTI do play important parts in the device reliability issues. Because of the shrinking dimensions of devices and the integrating scale of circuits, devices would work under high temperature. As a result, it is necessary to investigate BTI not only under conventional DC stress bias but also under AC stress condition.

1.3 Motivation

In this thesis, we focus not only on the enhancement of mobility, but also on the reliability of poly-Si TFTs. It is necessary for TFTs to have both high performance and good reliability to meet the criteria of commercial applications such as AMLCDs, 3-D IC's application, SRAMs, and EEPROMs. Compared to the single crystal silicon, the performance of poly-Si TFTs are strongly related to grain boundaries and intra-grain defects. Defects in the grain boundary would trap carriers and degrades the on-stated current of poly-Si TFTs. Moreover, the grain boundaries also provide the path of leakage current. In order to obtain desirable electrical characteristics of poly-Si TFTs, it is necessary to improve the device performance by enlarging the grain size of poly-Si films and reducing the trap states in grain boundaries to raise the field effect mobility.

There are several ways to improve the electrical characterization of TFTs, such as SPC and ELA, mentioned above. One coincidence of them is to enlarge the grain size in the poly-Si channel of TFTs. By means of growing larger grains, we can derive

not only higher carrier mobility but also suppressed path of leakage current due to the decrease of GBs in channel. In order to achieve high performance poly-Si TFTs, we fabricated poly-Si TFTs with a novel method using a buffer a-Si layer to enhance their performance.

Besides, NBTI in p-MOSFETs, while PBTI in n-MOSFETs have been found to be important reliability issues and have been widely investigated yet. It has been reported the degradation of NBTI in MOSFETs is mainly due to the generation of interface states and fixed oxide charges, and NBTI can be thermally and electrically activated[19]-[22]. Owing to the poor thermal conductivity of the glass substrates and high voltage operations in poly-Si TFTs, BTI must be the important issue in the reliability of poly-Si TFTs. However, BTI is still not thoroughly studied in poly-Si TFTs and the mechanism is not fully understood. In addition, the degradation mechanism of BTI stress in poly-Si TFTs, due to the grain boundaries in the channel region, might be different from MOSFETs. So, we studied the instabilities and mechanisms of LTPS TFTs upon BTI stress.

Finally, we investigated both the degradation and the passivation mechanisms under dynamic NBTI (DNBTI) stress. With DC NBTI stress, we would ignore the passivation mechanism for actually applications in IC circuits. As a result, we would underestimate the device lifetime. So we studied the degradation mechanisms of LTPS TFTs upon DNBTI stress.

1.4 Organization of the Thesis

In the following sections, we will show our research efforts.

In Chapter 2, the fabrication process and electrical characteristics of poly-Si TFTs using a buffer a-Si layer beneath the channel and devices with anneal procedure after gate oxide deposition will be proposed. Experimental results reveal that the

performance and reliability of our devices have remarkable improvement in comparison with conventional TFTs. Additionally, we made a detail discussion to explain the results of our experiment.

In Chapter 3, we discuss the reliability issues of p-channel TFTs and n-channel TFTs under NBTI and PBTI, respectively. Experimental results reveal that the mechanisms of NBTI and PBTI are quite different from each other. NBTI and PBTI also caused different degradation on p-TFTs and n-TFTs, respectively. We will make a detail discussion between the NBTI and PBTI.

In Chapter 4, the passivation phenomenon under dynamic negative-bias temperature stress (DNBTS) will be investigated by applying different stress gate biases, different stress frequencies, and different passivation voltages under different temperatures. Then, we will analyze the degradation and passivation mechanisms under DNBTI from our experimental results.

In the end of this thesis, we will make conclusions in Chapter 5.

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Chapter 2

Characteristics of Low Temperature Poly-Si TFTs Using a Bi-layer Poly-Si channel

2.1 Introduction

In recent years, polycrystalline silicon thin-film transistors (poly-Si TFTs) have been used to realize the integration of driving circuits and pixel switching elements on a single glass substrate in active matrix liquid crystal displays (AMLCDs) [1]-[3], and also attracted much attention for the potential to accomplish the System-on-Panel (SOP) [4]. Both high-performance and high-reliability poly-Si TFTs are required to accomplish this goal. However, it is known that trap states in poly-Si channel lead to lower carrier mobility and higher off-state leakage current. As a result, it is need for the number of trap states to be as low as possible. For example, Solid-Phase-Crystallization (SPC) [5]-[9] and Excimer Laser Annealing (ELA) [10]-[13] has been utilized in enlarging the grain size of the poly-Si to reduce trap states, leading to an excellent device performance.

It was found that with the increasing concentration of oxygen in the amorphous Si (a-Si) layer, the re-crystallization mechanism in it would be suppressed [14]. With the use of an optimized condition to form an oxygen-rich a-Si film before the deposition of the a-Si layer, we could derive larger grain size and less grain boundaries in poly-Si channel after SPC.

In this chapter, we used the method mentioned above to form the poly-Si channel to enlarge the grains, combing with the use of anneal with oxygen ambient

after the deposition of gate oxide to mend the defects in it. It was found that our devices have better electrical characteristics and stress immunization from Hot-Carrier Stress (HCS) than conventional poly-Si TFTs. We enhanced the transform characteristics in higher driving current and field effect mobility, and less leakage current, leading to a higher ON/OFF ratio, and also better reliability. We will make a detail discussion in the following sections.

2.2 Device Fabrication

Fig 2-1 schematically depicts the process flow and the cross-sectional view of the proposed n-channel poly-Si TFTs. First, a 550nm-thick thermal oxide layer was grown on the 6-in Si wafer with a furnace system. All the experimental devices in this study were fabricated on thermally oxidized Si wafers. Then, 100-nm amorphous Si layer was deposited on the thermally oxidized wafers as the control one and two, denoted as C1 and C2 later, with a low-pressure chemical vapor deposition (LPCVD) system at 550 ^{o}C and 100 mTorr in pressure, while the other one, denoted as Bi-layer later, deposited a 10-nm amorphous Si layer as the buffer layer under 500 ^{o}C and 15 mTorr before a 90-nm amorphous Si deposited under the environment as the controls without venting the system. Then, we checked the thicknesses of them respectively with n&k system to make sure they had almost the same thickness. Then, we used solid-phase-crystallization (SPC) method to recrystallize the amorphous Si films into poly-Si ones at 600 ^{o}C for 24 hours in N_2 ambient. The poly-Si films were patterned into active regions by transformer couple plasma (TCP) etching system using mixture gases of Cl_2 and HBr.

After RCA cleaning procedure, we deposited 50-nm TEOS oxide on them by TEOS and O_2 gases at 695 ^{o}C with LPCVD system to form the gate insulators. After

the deposition, we annealed C2 and Bi-layer by furnace with O_2 ambient at 700 ^oC for 1hr, while no treatment was done with C1. Then 200-nm amorphous Si was deposited with LPCVD system followed by SPC at 600 ^oC for 24 hours to serve as the poly-Si gate electrodes. Then, the poly-Si films were patterned by TCP etching system to form the gate electrodes and the gate oxides on source/drain were removed with dilute HF solution. The regions of sources, drains, and gates were doped by a self-aligned phosphorous ion implantation at the dosage and energy of 5E15 ions/cm^2 and 20 KeV, respectively. The dopants were activated at 600 ^oC for 12 hours by furnace system, and 400-nm passivation oxide layers were deposited with plasma-enhanced CVD (PECVD) system at 300 ^oC. After the definition of contact holes with BOE solution, 500-nm Al layers were deposited by sputter and patterned as metal pads. Finally, we passivated them by NH_3 plasma treatment for 1 hour at 300 ^oC.

2.3 Methods of Device Parameter Extraction

In this thesis, all of the electrical characteristics of proposed poly-Si TFTs were measured by HP 4156B-Precision Semiconductor Parameter Analyzer.

Many methods have been proposed to extract the characteristic parameters of poly-Si TFTs. In this section, those methods are described.

2.3.1 Determination of Threshold Voltage

Threshold voltage (V_{th}) is an important parameter required for the channel length-width and series resistance measurements. However, V_{th} is not defined uniquely. Various definitions have been proposed and reasons can be found in I_D-V_{GS} curves. One of the most common techniques is the linear extrapolation method with the drain current measured as a function of gate voltage at a low drain voltage of

50~100mV to ensure operation in the linear region [15]. The drain current is not zero when V_{GS} below threshold voltage and approaches zero asymptotically. Hence the I_{DS} versus V_{GS} curve can be extrapolated to I_D=0, and the V_{th} is determined from the extrapolated intercept of gate voltage (V_{GSi}) by

$$V_{th} = V_{GSi} - \frac{V_{DS}}{2} \quad \text{---------- (Eq. 1.1)}$$

Equation (1.1) is strictly only valid for negligible series resistance. Fortunately series resistance is usually negligible at the low drain current when threshold voltage measurements are made. The I_{DS}-V_{GS} curve deviates from a straight line at gate voltage below V_{th} due to subthreshold current and above V_{th} due to series resistance and mobility degradation effects. It is common practice to find the point of maximum slope of the I_{DS}-V_{GS} curve and fit a straight line to extrapolate to I_D=0 by means of finding the point of maximum of transconductance (Gm).

In this thesis, we use a simpler method to determinate the V_{th} called constant drain current method. The voltage at a specified threshold drain current is taken as the V_{th}. This method is adopted in the most studied papers of poly-Si TFTs. It can be given a threshold voltage close to that obtained by the complex linear extrapolation method. Typically, the threshold current is specified at (W/L)×10nA for V_{DS}=0.1V and (W/L)×100nA for V_{DS}=5V, where W and L are channel width and channel length, respectively.

2.3.2 Determination of Subthreshold Swing

Subthreshold swing (S.S.) is a typical parameter to describe the control ability of gate toward channel, which reflects the turn on/off speed of a device. It is defined as the amount of gate voltage required to increase/decrease drain current by one order of magnitude.

The S.S. should be independent of drain voltage and gate voltage. However, in reality, the S.S. increases with drain voltage due to channel shortening effect such as charge sharing, avalanche multiplication and punchthrough effect. The subthreshold swing is also related to gate voltage due to undesirable and inevitable factors such as the serial resistance and interface states.

In this thesis, the S.S. is defined as one-third of the gate voltage required to decrease the threshold current by three orders of magnitude. The threshold current is specified to be the drain current when the gate voltage is equal to threshold voltage.

2.3.3 Determination of Field Effect Mobility

Usually, field effect mobility (μ_{eff}) is determined from the maximum value of transconductance (Gm) at low drain bias. The transfer characteristics of poly-Si TFTs are similar to those of conventional MOSFETs, so that the first order of I-V relation in the bulk Si MOSFETs can be applied to poly-Si TFTs. The drain current in linear region ($V_{DS} < V_{GS} - V_{th}$) can be approximated as the following equation:

$$I_{DS} = \mu_{eff} C_{ox} \left(\frac{W}{L}\right)\left[(V_{GS} - V_{th})V_{DS} - \frac{1}{2}V_{DS}^{\ 2}\right] \quad \text{---------- (Eq. 1.2)}$$

where W and L are channel width and channel length, respectively. C_{ox} is the gate oxide capacitance per unit area and V_{th} is the threshold voltage. Thus, the transconductance is given by

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu_{eff} C_{ox} \left(\frac{W}{L}\right) V_{DS} \quad \text{---------- (Eq. 1.3)}$$

Therefore, the field-effect mobility is

$$\mu_{eff} = \frac{L}{C_{ox} W V_{DS}} g_{m(\max)}\Big|_{V_{DS} \to 0} \quad \text{---------- (Eq.1.4)}$$

2.3.4 Determination of ON/OFF Current Ratio

On/off current ratio is one of the most important parameters of poly-Si TFTs since a high-performance device exhibits not only a large on-current but also a small off-current (leakage current). The leakage current mechanism in poly-Si TFTs is not like that in MOSFET. In MOSFET, the channel is composed of single crystalline Si and the leakage current is due to the tunneling of minority carrier from drain region to accumulation layer located in channel region. However, in poly-Si TFTs, the channel is composed of poly-Si. A large amount of trap state densities in grain structure attribute a lot of defect states in energy band gap to enhance the tunneling effect. Therefore, the leakage current is much larger in poly-Si TFTs than in MOSFET. When the voltage drops between gate voltage and drain voltage increases, the band gap width decreases and the tunneling effect becomes much more severe. Normally we can find this effect in typical poly-Si TFTs' I_{DS}-V_{GS} characteristics where the magnitude of leakage current will reach a minimum and then increase as the gate voltage decreases/increases for n/p-channel TFTs.

There are a lot of ways to specify the on and off-current. In this chapter, take n-channel poly-Si TFTs for examples, the on-current is defined as the drain current when gate voltage at the maximum value and drain voltage is 5V. The off-current is specified as the minimum current when drain voltage equals to 5V.

$$\frac{I_{ON}}{I_{OFF}} = \frac{Maximum\ \ Current\ \ of\ \ I_{DS}-V_{GS}\ \ Plot\ \ at\ \ V_{DS}=5V}{Minimum\ \ Current\ \ of\ \ I_{DS}-V_{GS}\ \ Plot\ \ at\ \ V_{DS}=5V} \quad \text{-------- (Eq. 1.5)}$$

2.3.5 Extraction of Grain Boundary Trap State Density

The Trap State Density (N_t), which can be determined by the theory established by Levinson *et al.* [16], which is based on Seto's theory [17].

For poly-Si TFTs, the drain current I_{DS} can be given as following:

$$I_{DS} = \mu_{FE} C_{ox} \left(\frac{W}{L} \right) V_{DS} V_{GS} \exp\left(\frac{-q^3 N_t^{\,2} L_c}{8\varepsilon_{Si} kTC_{ox} V_{GS}} \right)$$ ---------- (Eq. 1.6)

Where,

μ_{eff}	field-effect mobility of carriers
q	electron charge
k	Boltzmann's constant
ε_{Si}	dielectric constant of silicon
T	temperature
N_t	trap-state density per unit area
L_c	channel thickness

This expression, first developed by Levinson *et al.*, is a standard MOSFET's equation with an activated mobility, which depends on the grain-boundary barrier height. Levinson *et al.* assumed that the channel thickness was constant and equal to the thickness of the poly-Si film (t). This simplifying assumption is permissible only for very thin film (t<10nm). The trap-state density can be obtained by extracting a straight line on the plot of $ln(I_{DS}/V_{GS})$ versus $1/V_{GS}$ at low drain voltage and high gate voltage.

Proano *et al.* [18] thought that a barrier approximation is to calculate the gate induced carrier channel thickness by solving Poisson's equation for an undoped material and to define the channel thickness (L_c) as a thickness in which 80% of the total charges were induced by the gate. Doing so, one obtains

$$L_c = \frac{8kTt_{ox}\sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{SiO_2}}}}{q\left(V_{GS} - V_{fb}\right)}$$ ---------- (Eq. 1.7)

which varies inversely with $(V_{GS}-V_{fb})$. This predicts, by substituting Eq.2.7 into Eq.1.6, that $ln[I_{DS}/(V_{GS}-V_{fb})]$ versus $1/(V_{GS}-V_{fb})^2$. We use the gate voltage at which

minimum leakage current occurs as flat-band voltage (V_{fb}). Effective trap-state density (N_t) can be determined from the square root of the slope.

2.4 Results and Discussion

2.4.1 Characteristics of poly-Si TFTs with post anneal after gate oxide deposition

Figure 2-2 shows the transfer characteristics (I_{DS}-V_{GS}) of the conventional poly-Si TFT and the poly-Si TFT which was annealed after gate oxide deposition. The measurements was performed at drain voltage of V_{DS}=5V. The measured and extracted parameters from the devices are listed in Table 2-1. The on-current (at V_{GS}=15V), and off-current (at V_{GS}=-10V) were measured at V_{DS}=5V, while the threshold voltage and the subthreshold swing were derived from the transfer characteristics at V_{DS}=0.1V.

In Fig. 2-2, we can see that the poly-Si TFTs with an anneal procedure exhibit better on-state and off-state characteristics than those of the conventional sample. Notably, the annealed poly-Si TFT has higher ON-state current and lower OFF-state leakage current, leading to larger ON/OFF current ratio. Moreover, the annealed poly-Si TFT also has smaller threshold voltage, smaller subthreshold swing, and larger field effect mobility than the conventional poly-Si TFT. From Fig. 2-3, we found that the poly-Si TFT with annealed gate oxide has much better reliability than the conventional poly-Si TFT under high stressed gate voltages at high temperature. From these significant improvements mentioned above, we found that the quality of the gate oxide has been mended after anneal. In order to exclude the influence of the oxide quality in our study, we used the same anneal procedure in our fabrication process of control sample and our proposed sample, Bi-layer.

2.4.2 Characteristics of Poly-Si TFTs with Bi-layer Poly-Si Channels

Fig. 2-4(a) shows the transfer characteristics (I_{DS}-V_{GS}) of the annealed conventional poly-Si TFT, Control, and the proposed bi-layer poly-Si TFTs, Bi-layer. The measurements was performed at drain voltage of V_{DS}=5V. The on-current (at V_{GS}=15V), and off-current (at V_{GS}=-10V) were measured at V_{DS}=5V, while the threshold voltage and the subthreshold swing were derived from the transfer characteristics at V_{DS}=0.1V.

From Fig. 2-4(a), we can see that Bi-layer exhibit better ON-state characteristics than the control sample. In OFF-state, under a large negative gate bias, the leakage current of Bi-layer (3.84×10^{-9} A) is significant lower than that of the control sample (1.05×10^{-8} A). It was obvious that the gate induced grain leakage (GIDL) was suppressed in Bi-layer. Moreover, the threshold voltage and subthreshold swing of Bi-layer (0.26V & 0.71V/dec.) was found to be superior to the control sample (0.48V & 1.05V/dec.). In Fig. 2-4(b), we compared the field effect mobility between these two samples, the proposed poly-Si TFTs Bi-layer shows obvious enhancement in mobility compared with the conventional TFT from 38 ($cm^2/V \cdot s$) to 45 ($cm^2/V \cdot s$). The mobility of Bi-layer has been enhanced by 18.4%. Fig. 2-5 shows the plot of $ln[I_{DS}/(V_{GS}-V_{fb})]$ versus $1/(V_{GS}-V_{fb})^2$ at low drain voltage and high gate voltage for Control and Bi-layer. The effective trap state density calculated from the slopes for Control and Bi-layer were 3.22×10^{12} and 2.68×10^{12} cm^{-2}, respectively. Bi-layer has less trap state density than that of Control, and we deduced that Bi-layer has less grain boundary trap states than Control. Fig. 2-6 shows the output characteristics of the control and the proposed poly-Si TFTs. We can see that the driving current of the proposed poly-Si TFTs has been significantly enhanced. The measured and extracted parameters from the devices are listed in Table 2-2.

2.4.3 Reliability of Poly-Si TFTs with Bi-layer Poly-Si Channels

Furthermore, we discussed the reliability of the proposed TFTs and conventional TFTs. In Fig. 2-7, we applied DC stress to the devices with channel length and width equal to 5 μm and 10 μm, respectively. The hot-carrier stress (HCS) test was performed at $V_G = V_D = 25V$ while $V_S = 0V$ under 25°C for 1000 seconds to investigate the device reliability. Fig. 2-7 (a) shows the shift of their threshold voltages while Fig. 2-8 (b) shows the variation of their subthreshold swings under the HCS test. The shift of threshold voltage was defined as $V_{th,stressed} - V_{th,initial}$ and the variation of subthreshold swing was defined as $100\% * (S_{stressed} - S_{initial})/ S_{initial}$, where $V_{th,stressed}$ and $V_{th,initial}$ represent the threshold voltage after and before stress, respectively while $S_{stressed}$ and $S_{initial}$ represent the subthreshold swing shift after and before stress, respectively.

Moreover, we applied DC stress to the devices with channel length and width equal to 10 μm and 10 μm, respectively. The Hot-Carrier Stress test was performed at $V_G = V_D = 20V$ while $V_S = 0V$ under 100°C for 1000 seconds to investigate the device reliability under high temperature use. The variation of their threshold voltages and subthreshold swings of them are shown in Fig. 2-8, the same definition as in Fig. 2-7 was used.

From Fig. 2-7 and Fig. 2-8, we found that the proposed TFT shows suppression in device degradation owing to HCS not only at room temperature but also at high temperature, indicating that it has much better reliability than conventional TFTs.

2.5 Summary

We used an anneal procedure after gate oxide deposition to improve the transfer characteristics and reliability of poly-Si TFTs. With the deposition of a buffer a-Si layer under low-temperature and low-pressure condition, we fabricated high-performance poly-Si TFTs with enhanced reliability. The characteristics of the

proposed TFTs have great improvement, such as higher On-state current, higher field effect mobility, lower subthreshold swing, suppressed GIDL current, and better reliability. With an optimized deposition condition of the buffer a-Si layer, the proposed TFTs would be candidates in high performance TFTs application.

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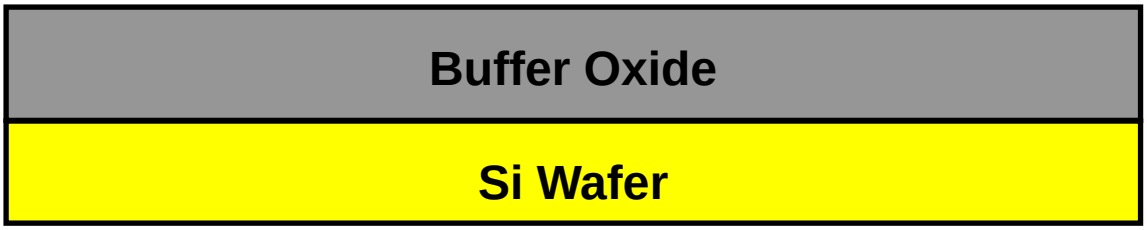
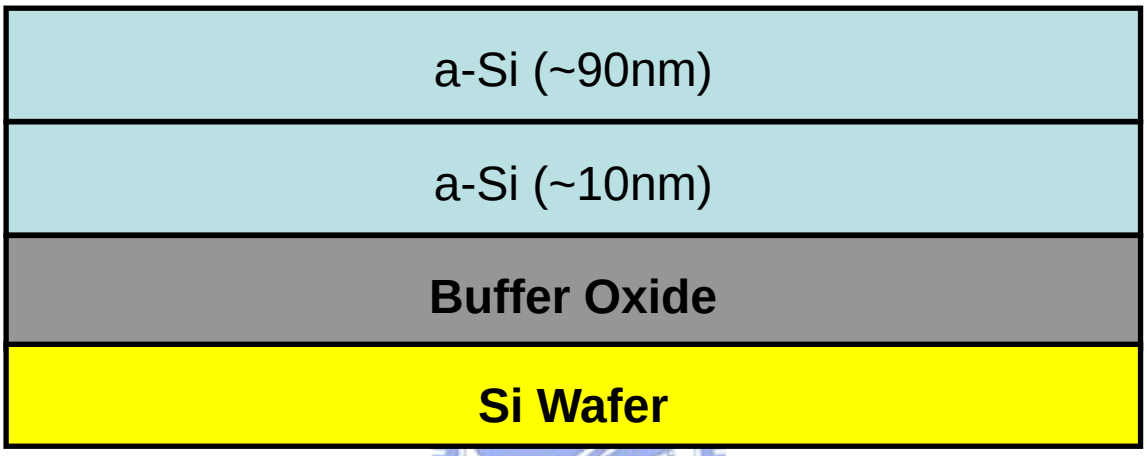
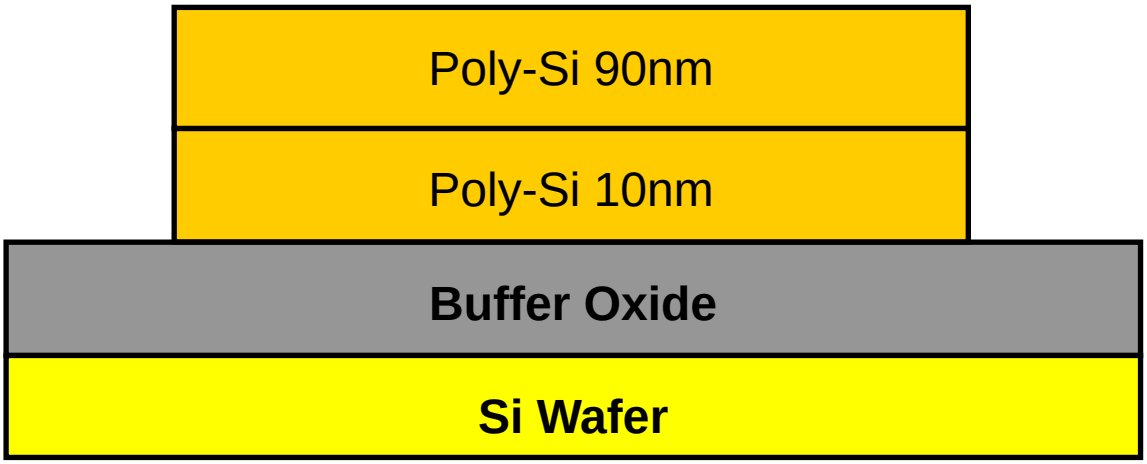


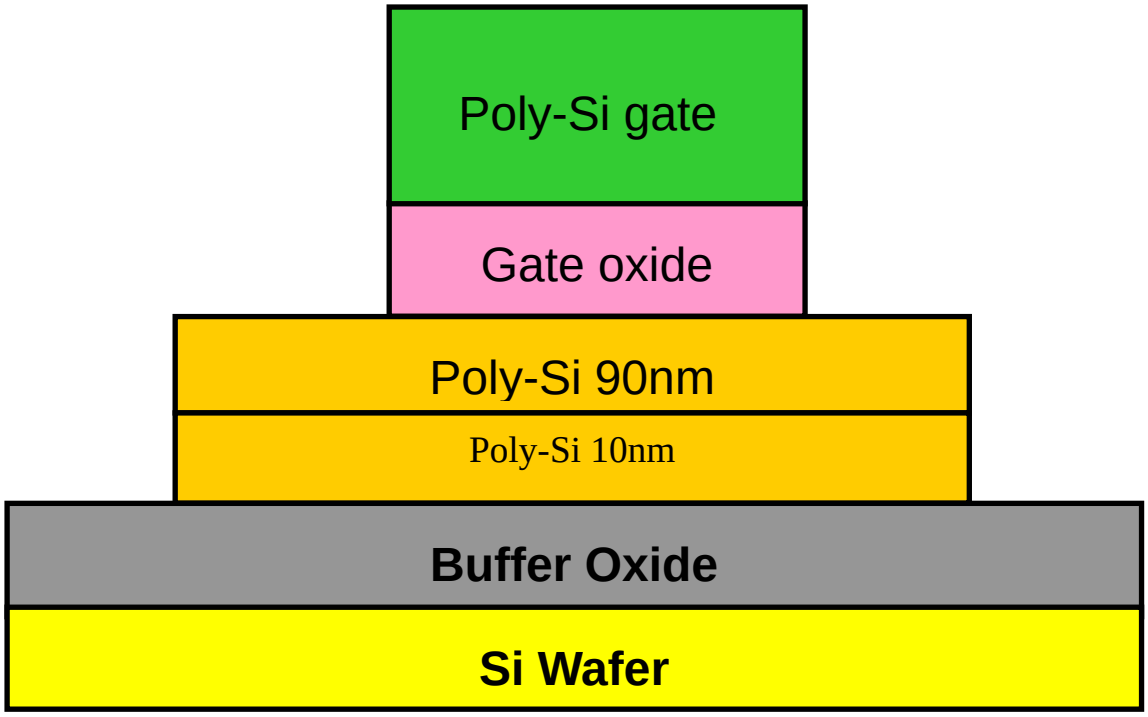
(a) Thermal oxidation grown by furnace.



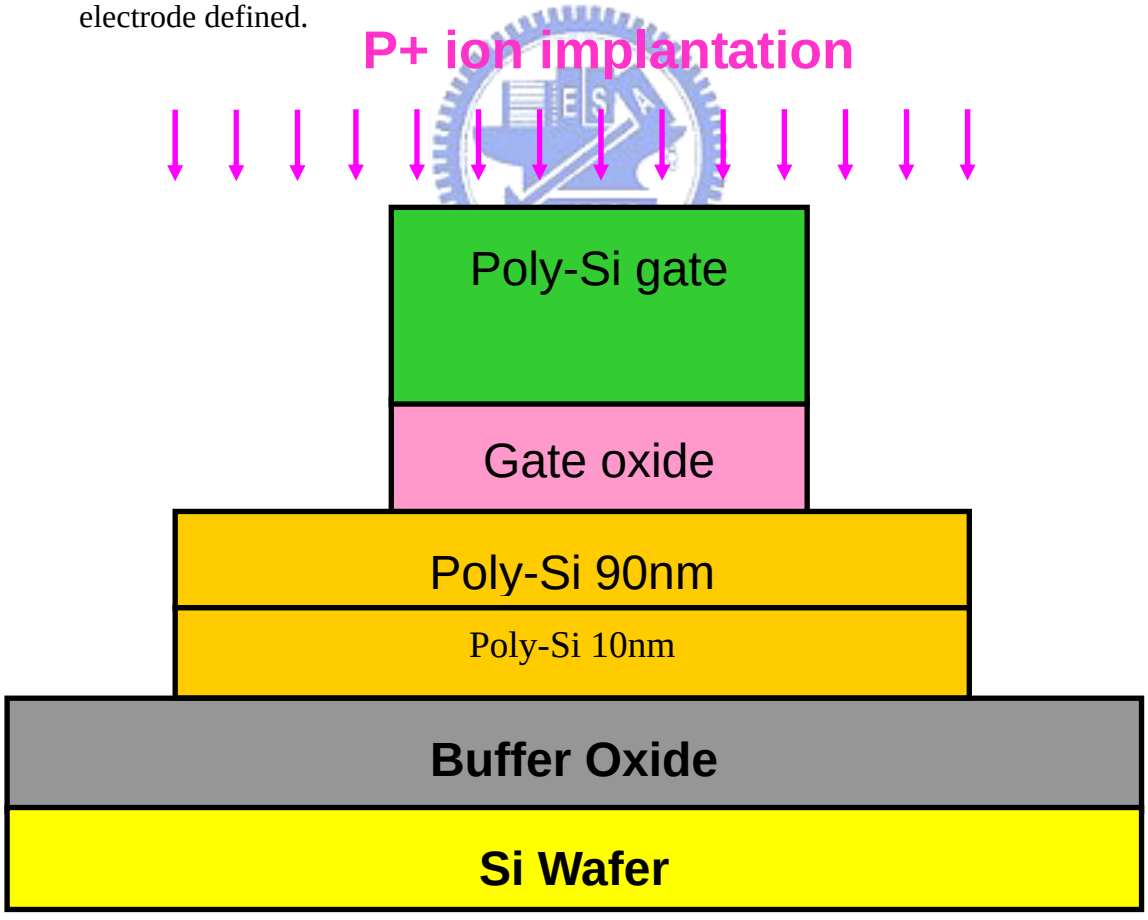
(b) Bi-layer amorphous Si (a-Si) deposited by LPCVD.



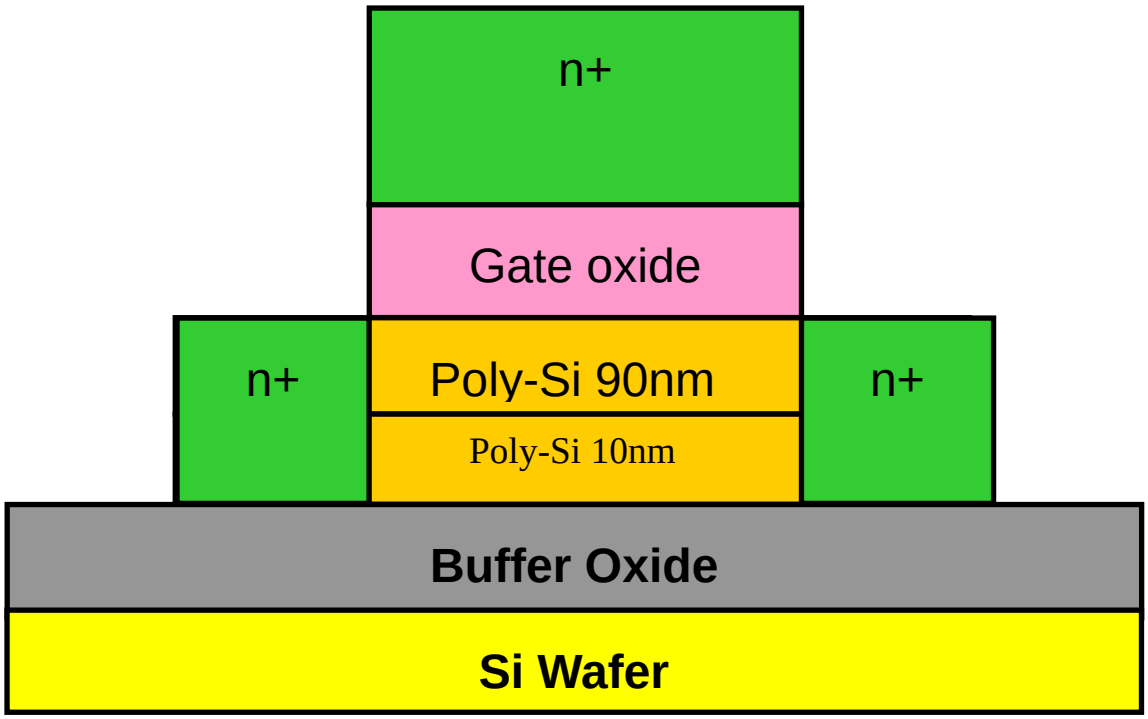
(c) Recrystallization of a-Si film into poly-Si channel by SPC, followed by active region definition.



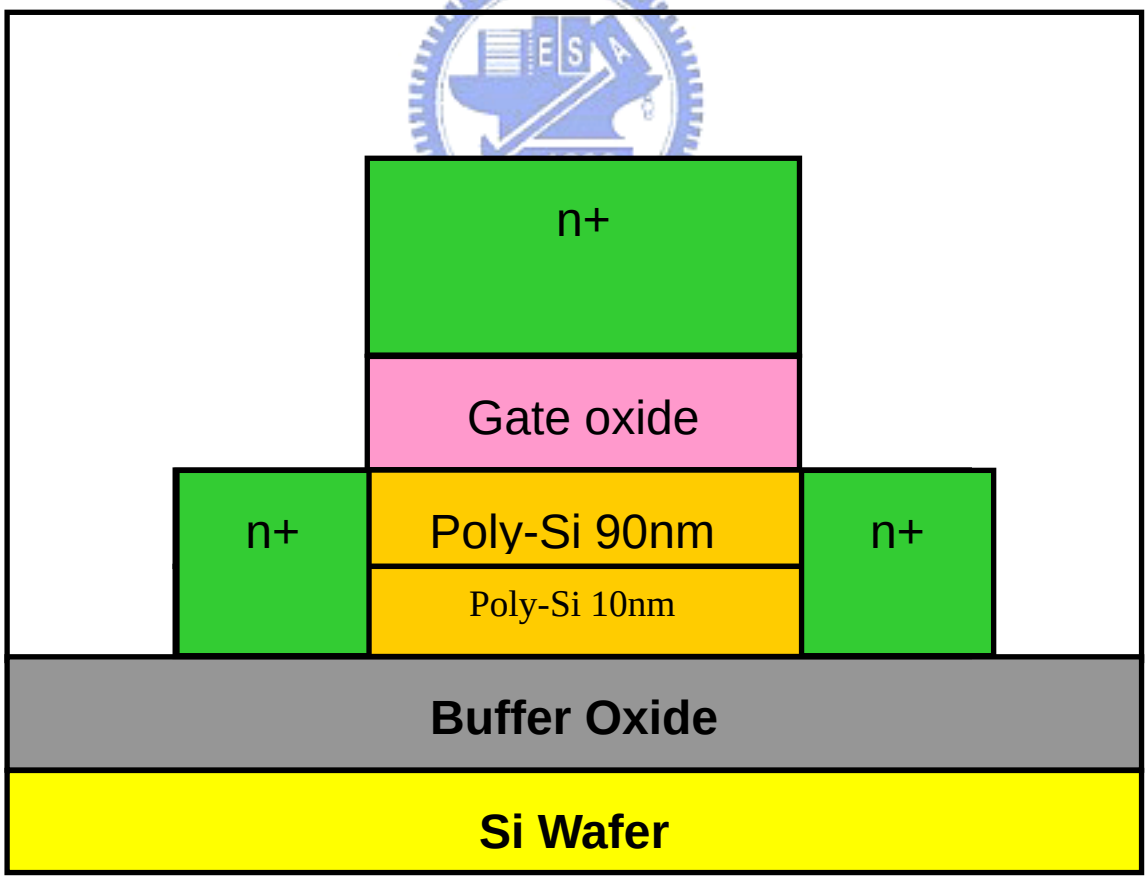
(d) Deposition of TEOS gate oxide by LPCVD and poly-Si gate by LPCVD, gate electrode defined.



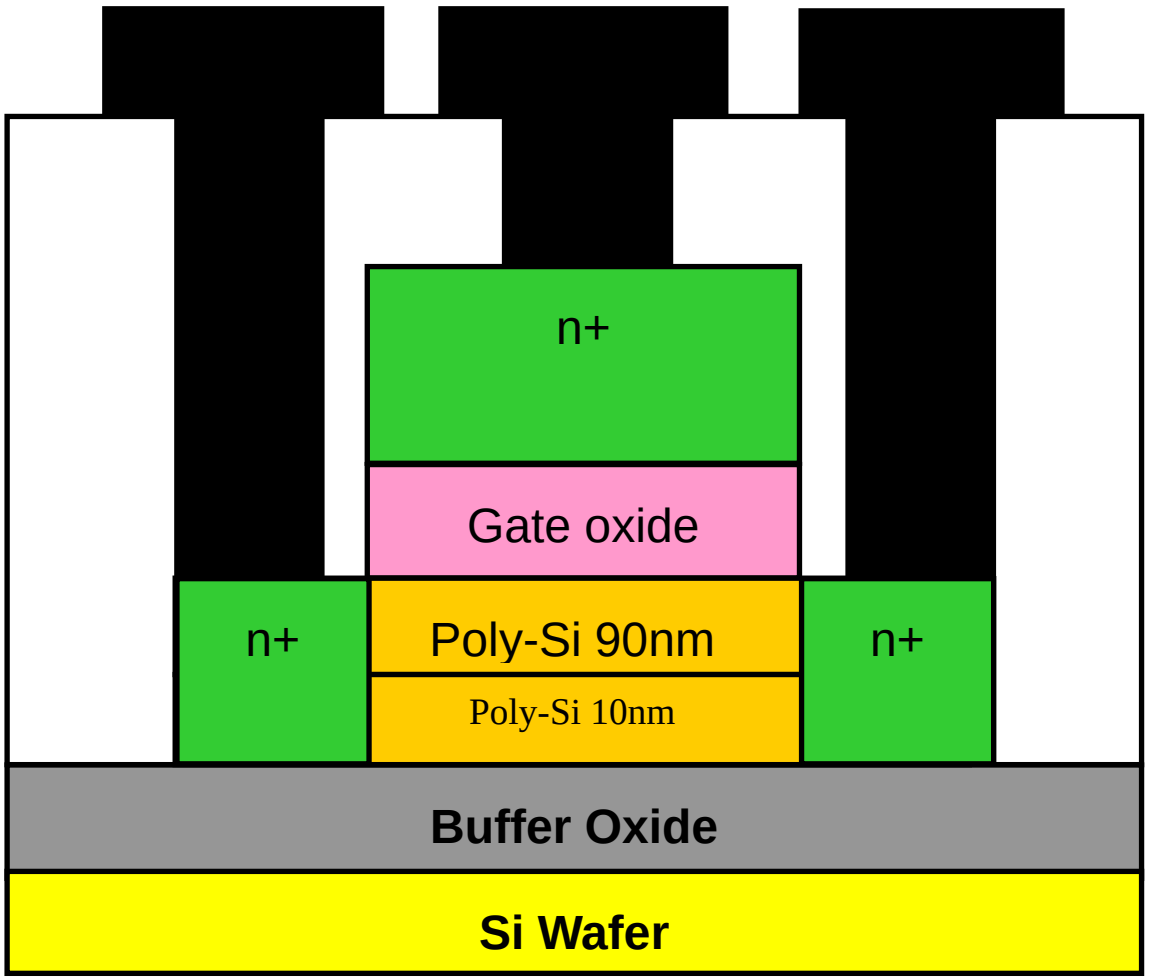
(e) Self-aligned phosphorous ion implantation.



(f) Dopants activated by furnace.



(g) Deposition of passivation oxide by PECVD.



(h) Contact holes opened and metal pads formation.

Fig. 2-1 Schematic diagram of fabrication process for bi-layer poly-Si TFTs.

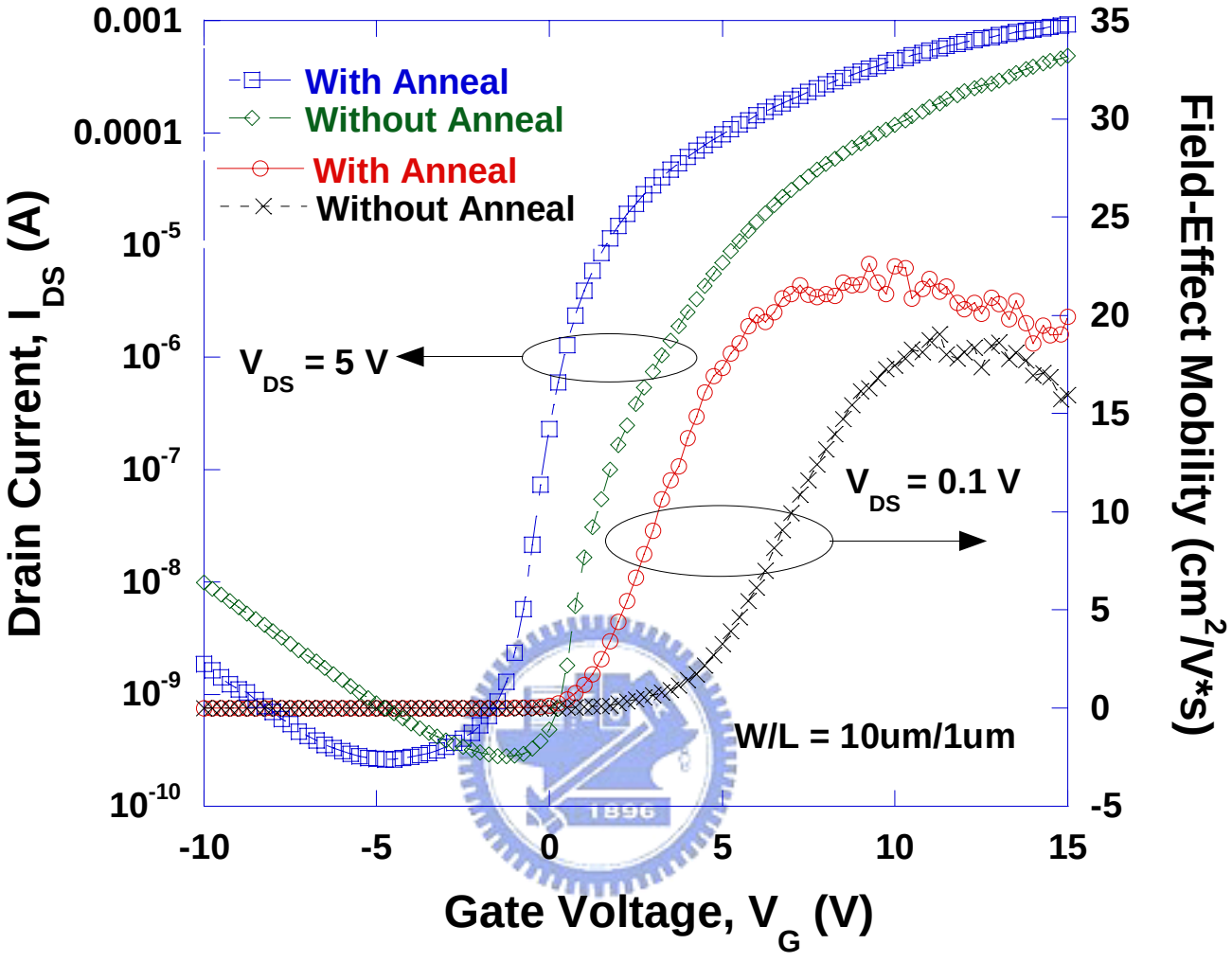


Fig. 2-2 Transfer characteristics of the poly-Si TFTs with and without an anneal procedure after the deposition of gate oxide.

Table 2-1 Comparison of device characteristics of the poly-Si TFTs with and without an anneal procedure after the gate oxide deposition (W/L=10um/1um).

	Without Anneal	With Anneal
V_{th} (V)	4.02	1.76
S. (V/dec.)	1.07	0.90
μ_{FE} ($cm^2/V*s$)	19.8	22.5
I_{on} @ V_G=10 V, V_D= 5 V (A)	7.72×10^{-4}	8.71×10^{-4}
I_{off} @ V_G=-10V, V_D = 5V (A)	6.92×10^{-9}	2.58×10^{-9}
I_{on}/I_{off}	1.12×10^{5}	3.38×10^{5}
N_t (cm^{-2})	7.31×10^{12}	3.47×10^{12}

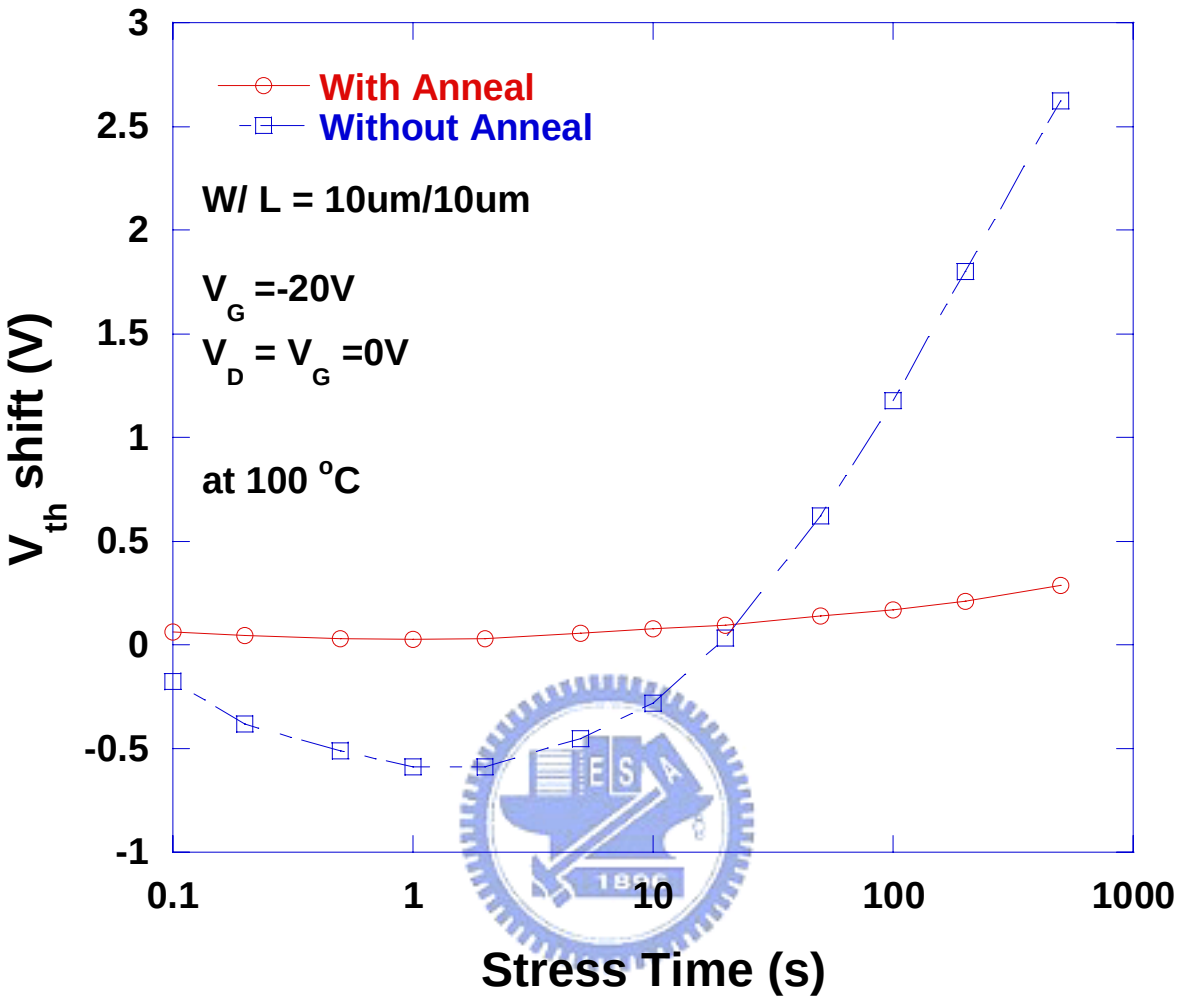


Fig. 2-3(a) Threshold voltage (V_{th}) shift versus stress time of n-TFTs with and without gate oxide anneal under static gate bias V_G=-20V while S/D were grounded at 100°C.

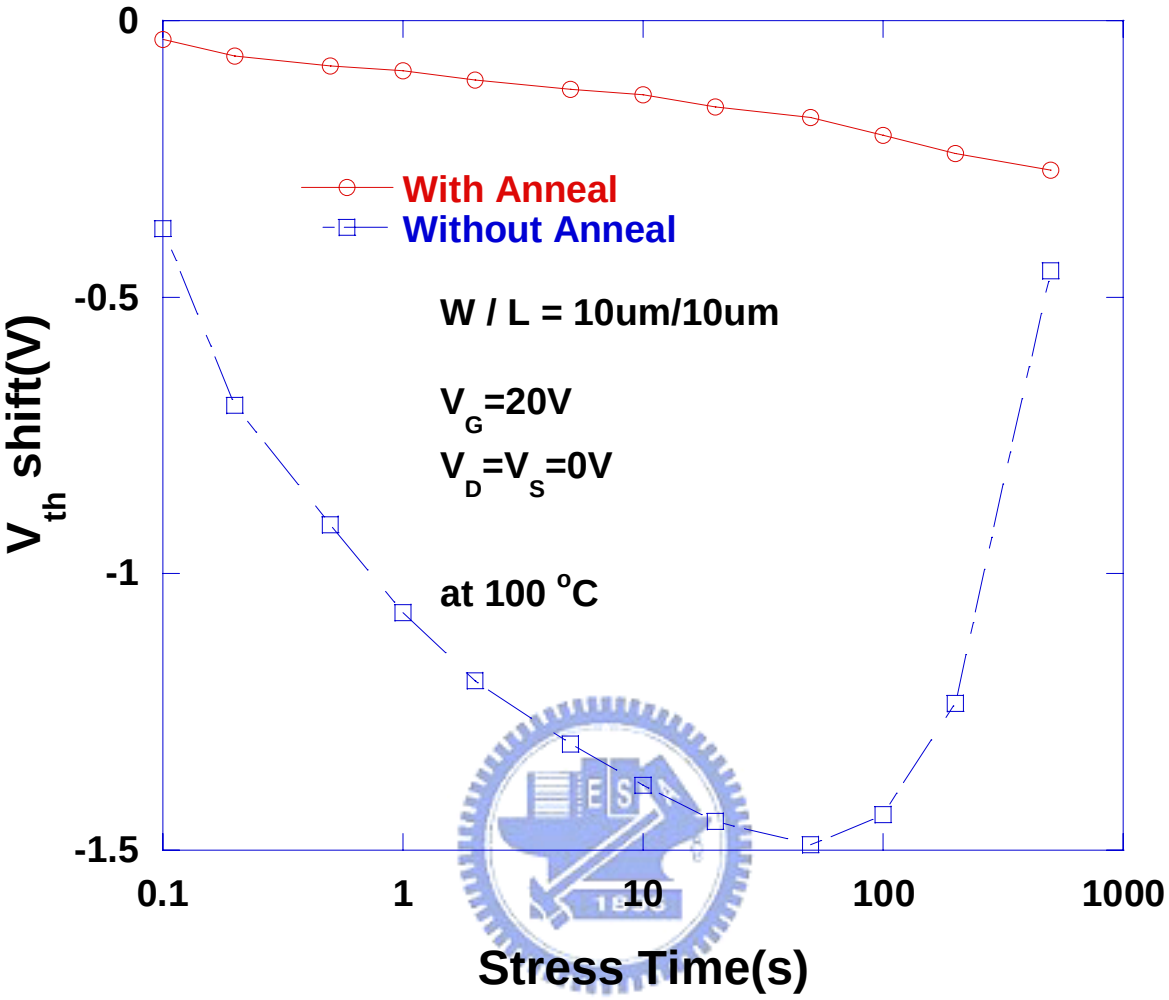


Fig. 2-3(b) Threshold voltage (V_{th}) shift versus stress time of n-TFTs with and without gate oxide anneal under static gate bias V_G=20V while S/D were grounded at 100°C.

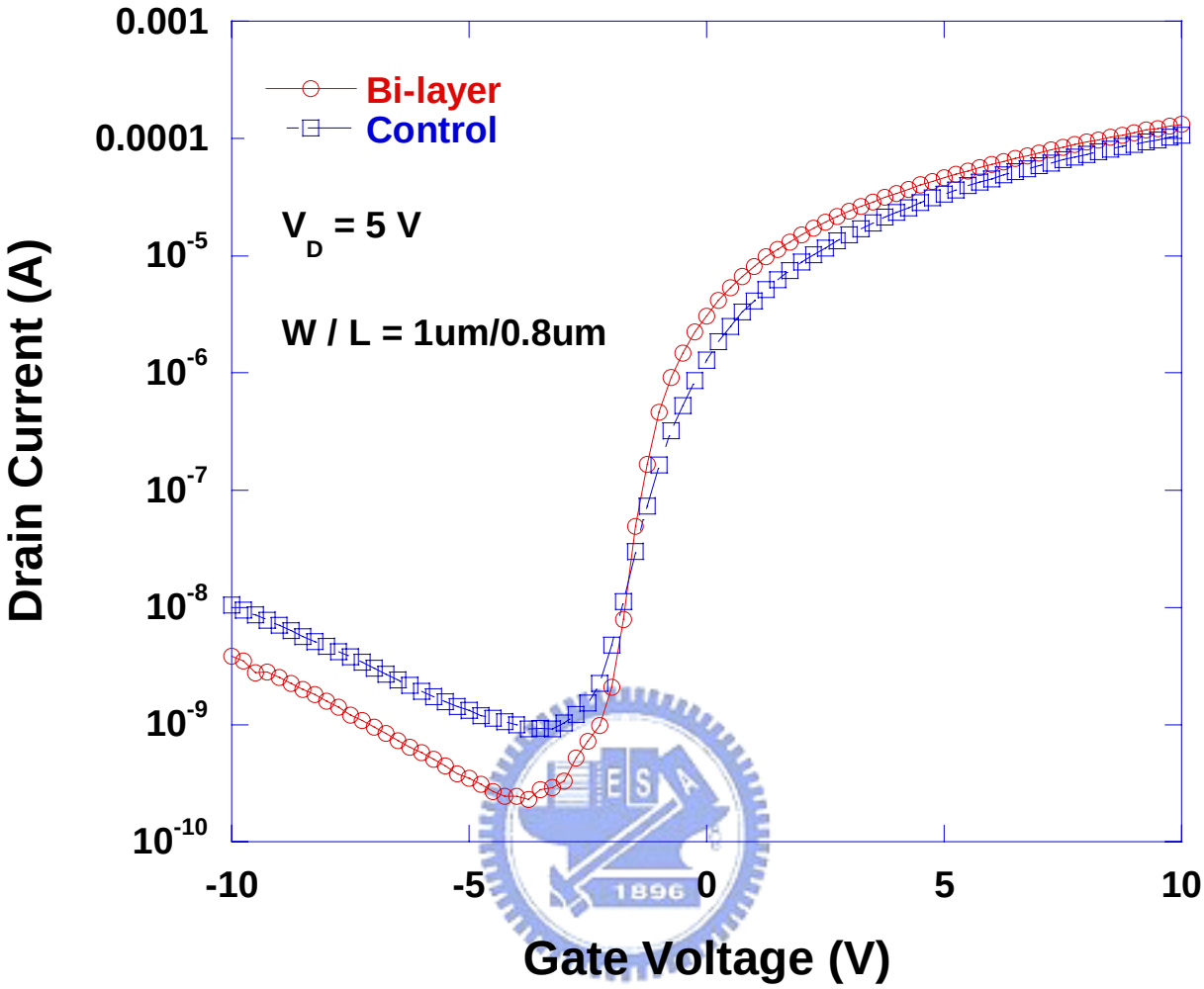


Fig. 2-4(a) Transfer characteristics of the Control and the Bi-layer poly-Si TFTs with V_{DS}=5V.

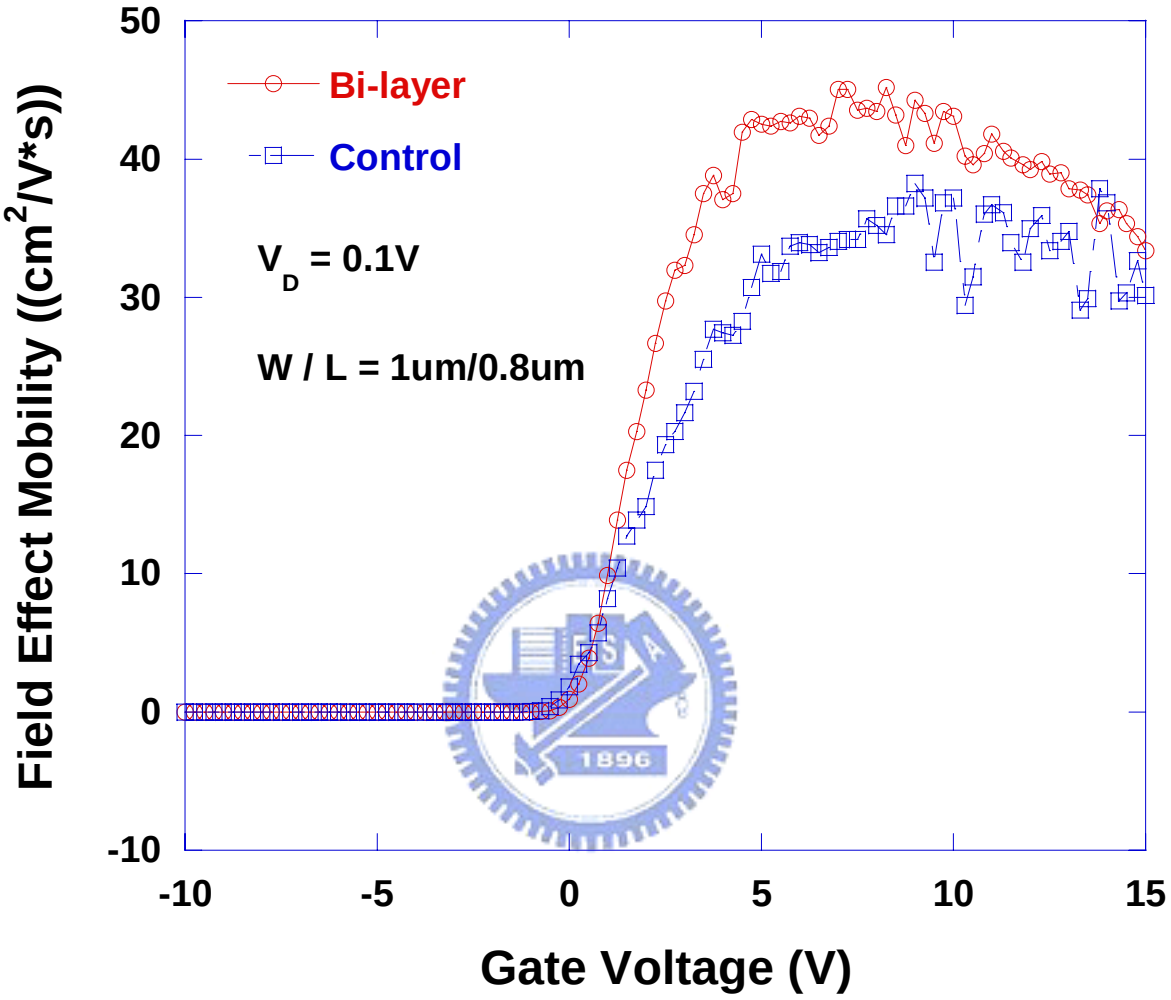


Fig. 2-4(b) Field effect mobility of the Control and the Bi-layer poly-Si TFTs with V_{DS}=0.1V.

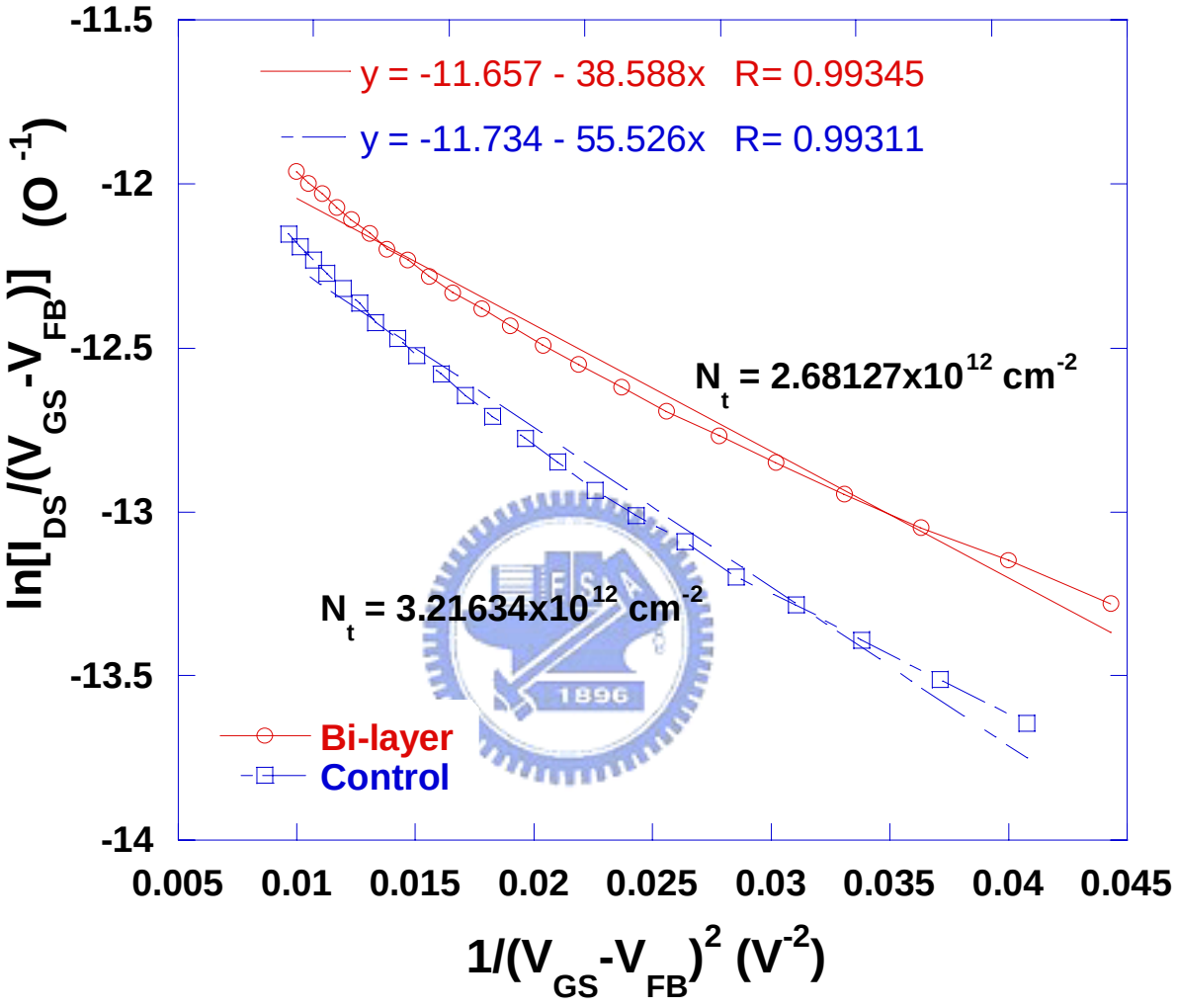


Fig. 2-5 Trap state density extraction of the Control and the Bi-layer poly-Si TFTs.

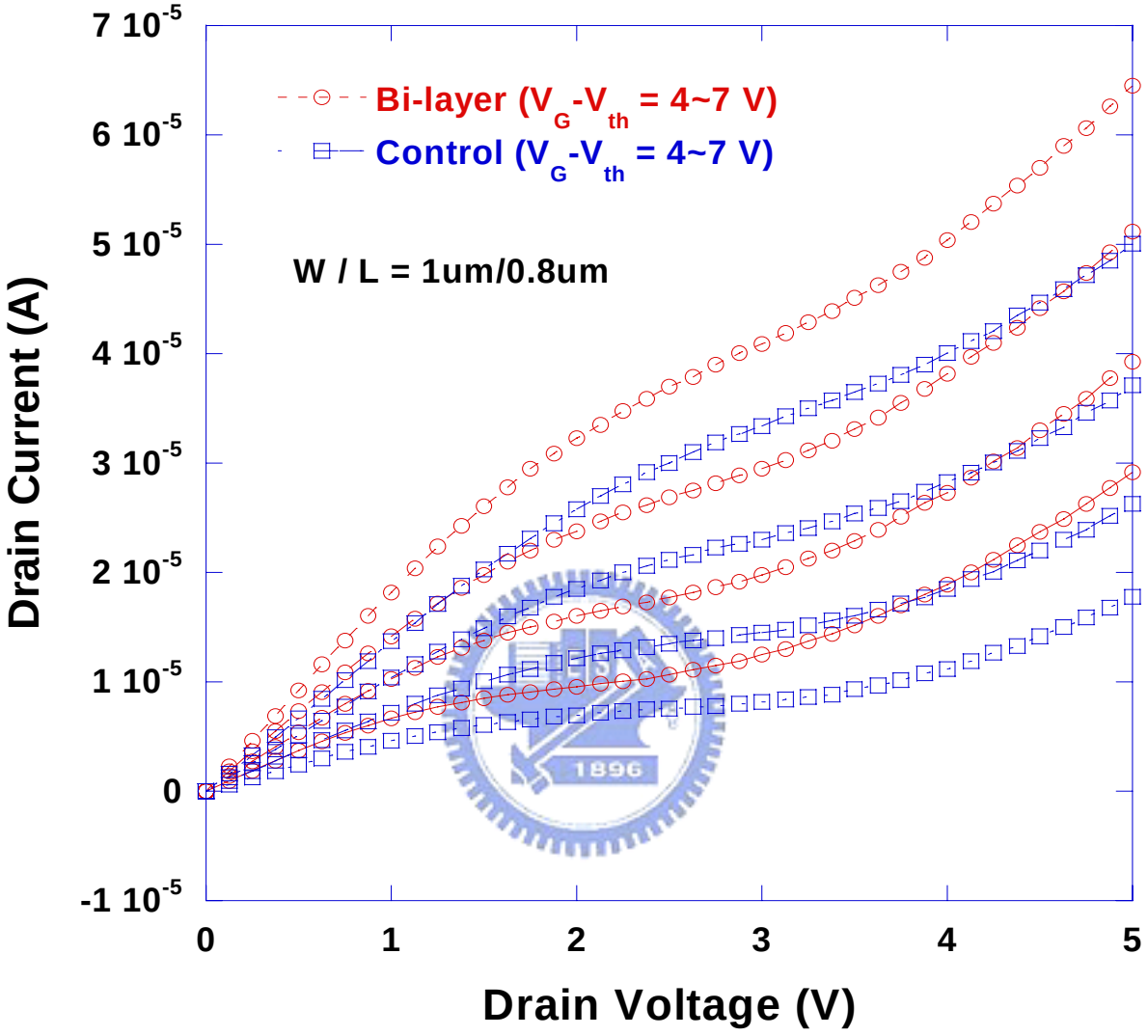
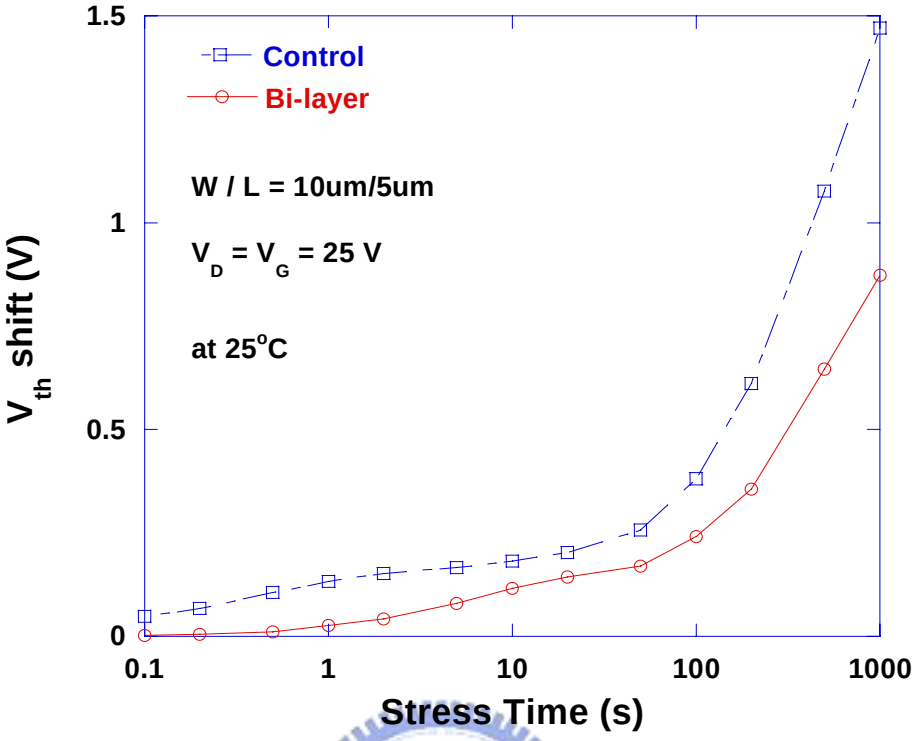


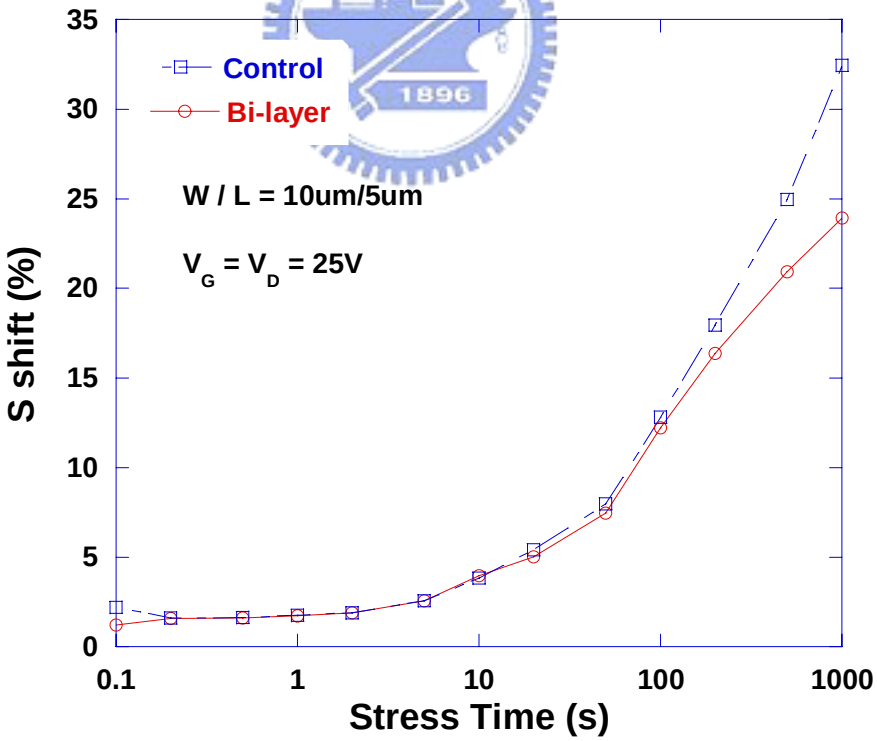
Fig. 2-6 Output characteristic of the Control and the Bi-layer poly-Si TFTs.

Table 2-2 Comparison of device characteristics of the Control and the Bi-layer poly-Si TFTs.

	Control	Bi-layer
V_{th} (V)	0.48	0.26
S (V/dec.)	1.05	0.71
μ_{FE} ($cm^2/V*s$)	38	45
I_{on} @ V_G=10 V, V_D= 5 V (A)	1.07×10^{-4}	1.33×10^{-4}
I_{off} @ V_G=-10V, V_D = 5V (A)	1.05×10^{-8}	3.84×10^{-9}
I_{on}/I_{off}	1.02×10^{4}	3.46×10^{4}
N_t (cm^{-2})	3.22×10^{12}	2.68×10^{12}

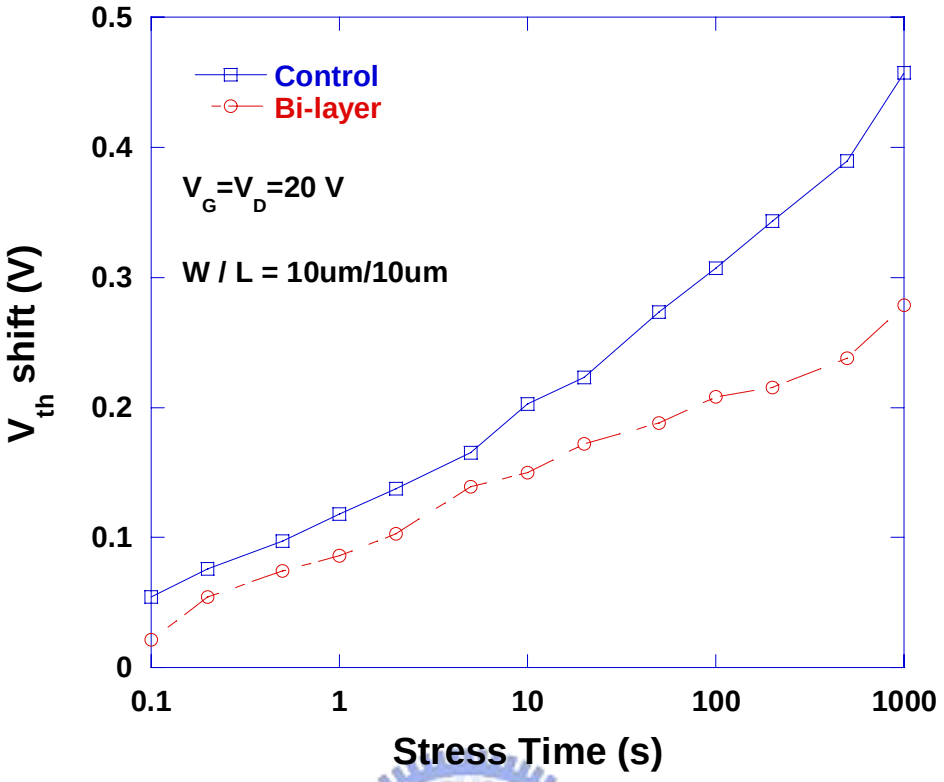


(a) Threshold voltage degradation versus the stress time

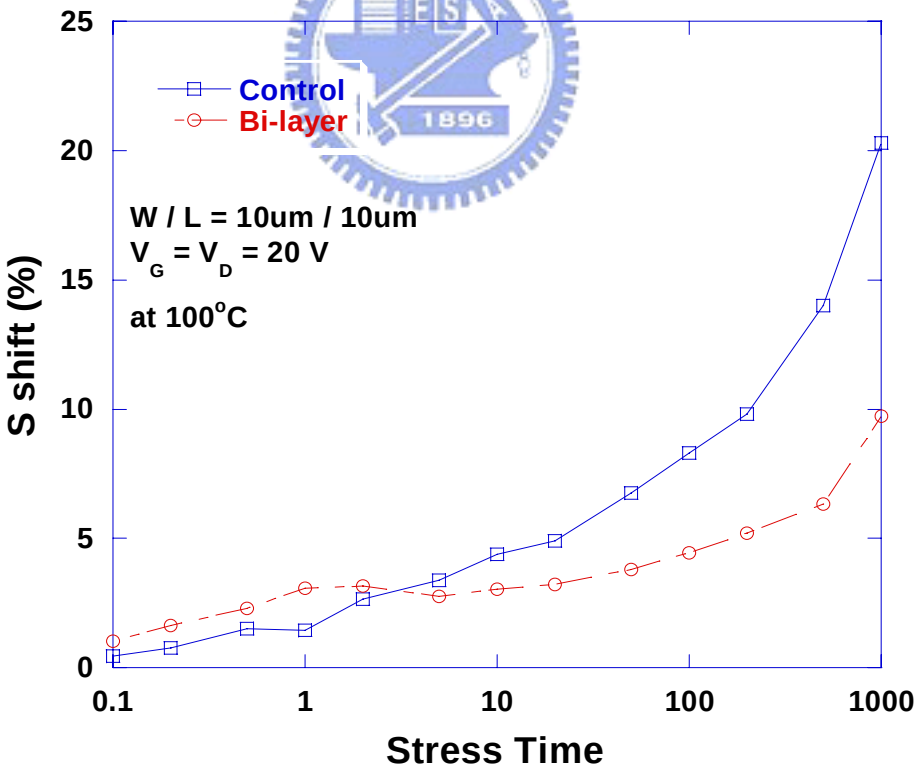


(b) Subthreshold swing degradation versus stress time

Fig. 2-7 (a) Threshold voltage and (b) subthreshold swing degradation versus the stress time under hot-carrier stress at room temperature



(a) Threshold voltage degradation versus stress time



(b) Subthreshold swing degradation versus stress time

Fig. 2-8 (a) Threshold voltage and (b) subthreshold swing degradation versus the stress time under hot-carrier stress at 100 °C.

Chapter 3

Degradation Mechanisms of NBTI and PBTI in Low-Temperature Poly-Si Thin-Film Transistors

3.1 Introduction

Recently, low temperature polycrystalline silicon thin-film transistors (LTPS TFTs) have attracted much attention due to the high potential of realizing system on panel (SOP) [1], the possibility of realizing the integration of peripheral circuit, and applications in active matrix liquid crystal displays (AMLCDs)[2][3]. Inevitably, the stability of poly-Si TFTs is of significant importance from the fabrication technology point of view and as a long-term reliability concern [2]. In p-channel MOSFETs, negative bias temperature instability (NBTI) has been found to be an important reliability concern [3][4][5], while positive bias temperature instability (PBTI) been found to be an important problem to n-channel MOSFETs. Both the influences of NBTI to p-channel MOSFETs and PBTI to n-channel MOSFETs have been widely investigated. It was found that the degradation mechanisms for NBTI and PBTI were quite different. The degradation due to NBTI is mainly responsible for the generation of interface states and fixed oxide charge, as a result, NBTI could be thermally and electrically activated by elevated stress temperature and voltage [6]. Unlike NBTI, n-channel MOSFETs with high-*k* gate insulators have attracted much attention. PBTI only exist in the formation of donor-like interface states and charge de-trapping from the gate insulators [7].

In LTPS TFTs, due to the poor thermal conductivity of the glass substrates and high operation voltages, we supposed NBTI and PBTI would be important in the

reliability of LTPS TFTs. Additionally, the LTPS TFT driving circuit is designed using the CMOSFET structure, we speculate that the effects of NBTI and PBTI will degrade the reliability of p-channel and n-channel TFTs, respectively. Some researches have pointed out BTI stress caused the performance degradation in poly-Si TFTs as well as in MOSFETs [8]. Moreover, the degradation mechanism of BTI stress in poly-Si TFTs, due to the grain boundaries in the channel region, may be different from MOSFETs. Some studies have indicated that BTI stress on poly-Si TFTs may generate trap states in the grain boundaries [9]. However, the effects of NBTI and PBTI on the reliability of LTPS TFTs have not been explored.

In this chapter, the reliability of the LTPS TFTs was studied by applying NBTI and PBTI stress on TFTs. The NBTI stress was applied to the p-channel LTPS TFTs, while the PBTI stress was applied to the n-channel LTPS TFTs. By varying the stress voltages and temperatures, the basic devices parameters were extracted and analyzed to explain the degradation mechanisms.

3.2 Experimental

The p- and n-channel LTPS TFTs were fabricated on glass substrates. A 40nm-thick amorphous-Si layer was first deposited by PECVD on a buffer layer and crystallized into poly-Si film by excimer laser annealing. For the p-channel TFTs, the gate dielectric was deposited with an equivalent 100nm-thick SiO_2 layer after defining the active region. Mo was then deposited and patterned as the gate electrode. Self-align source/drain was formed by plasma doping. Fig. 3-1 shows the schematic diagram of fabrication process. For the n-channel devices, the source and drain were first formed after defining the active region. The gate dielectric and metal film were deposited and patterned as the gate electrode. Following that, self-aligned

lightly-deped soruce and drain were formed. Then, the inter-layer dielectric was deposited on all the devices and densified. The dopants were activated during the densification of the inter-layer dielectric. Finally, inter-connection metal was deposited and patterned. The channel length (L) and channel width (W) of the device used in this study were 10 and 20 μm, respectively.

During NBTI stress, the glass substrate was heated to the stress temperature ranging from 25 to 150^{o}C, and the stress voltage in the range of -15 to -30 V was applied the gate with the source/drain grounded. The schematic cross-section diagrams of the LTPS TFTs and stress setup is shown in Fig. 3-2. The stress was periodically stopped to measure the basic characteristics of the device to characterize the NBTI effect. All the measurements were taken at the stress temperature. Fowler-Nordheim current was not pronounced at these bias conditions; therefore, the extra trap state generation and device instability caused by the small current can be neglected.

3.3 Results and Discussion

Fig. 3-3(a) and 3-3(b) show the influence of NBTI and PBTI stress on the transfer characteristics of the p- and n-channel TFTs, respectively. In both case, the absolute values of threshold voltages ($|V_{th}|$) increase after NBTI or PBTI stress. The subthreshold swing (S) degrades after NBTI stress for p-channel TFT, wihle it remains almost unchanged after PBTI stress for n-channel TFT. This indicates that NBTI stress generate more interface trap states in the deivce. Besides, the field-effect mobily (μ_{FE}) is found to decrease under NBTI stress; however, it is worth notint that the μ_{FE} increases after PBTI stress.

Fig. 3-4(a) and 3-4(b) show the time dependence of the threshold voltage shift (ΔV_{th}) of the p- and n-channel TFTs, respectively. The stress was performed at 150^{o}C

with various stress gate voltages. In our study, the gate voltage at a specified threshold drain current (I_{DS}), ± (W/L) × 10 nA for V_{DS} = ±0.1 V, is taken as the threshold voltage. In both cases, the $|\Delta V_{th}|$ increases as the absolute value of the stress gate voltage increases, indicating that both NBTI and PBTI can be electrically activated. Besides, the $|\Delta V_{th}|$ shows a power law dependence on the stress time ($|\Delta V_{th}| \sim t^{n}$). The exponent factor *n* is around 0.25 to 0.30 for p-channel TFTs under NBTI stress, which is similar to the results previously reported for poly-Si TFTs [10][11] and bulk MOSFETs [10]. It has been reported that the exponent factor between 1/3 to 1/4 can be explained by the diffusion-controlled electrochemical reactions [7][12]. However, for the n-channel TFT under PBTI stress, the *n* value is below 0.12, indicating the PBTI-degradation mechanism is different to that of NBTI.

Fig. 3-5(a) and 3-5(b) show the time dependence of the $|\Delta V_{th}|$ of p- and n-channel TFTs, respectively, under various stress temperatures with stress gate voltage of -30 V. As the stress temperature increases, the $|\Delta V_{th}|$ increases under NBTI stress; however, it shows almost temperature independent under PBTI stress. It has been reported that the NBTI-degradation in MOSFETs is mainly attributed to the generation of interface trap states and fixed oxide charges, and it can be thermally and electrically activated [3][5][6]. However, the PBTI-degradation mechanism is generally explained by the charge trapping in the gate dielectric. Therefore, the NBTI- and PBTI-degradation show different dependent on the stress temperature.

Fig. 3-6(a) and 3-6(b) show the μ_{FE} variation as a function of the stress voltage for p- and n-channel TFTs, respectively. It has been reported that the subthreshold swing is more closely related to the trap states located near the midgap (deep states), while the mobility is more associated with the trap states located near the band edge (tail states) [11]. For the p-channel TFTs, the NBTI stress rarely changes the μ_{FE}, indicating that the generation of the tail states can be neglected under NBTI stress. For

the n-channel TFTs, the μ_{FE} increases with the stress voltage or temperature, implying that the tail states can be passivated during PBTI stress.

Fig. 3-7(a) and 3-7(b) show the drive current degradation as a function of the stress voltage for p- and n-channel TFTs, respectively. For the p-channel TFTs, the drive current degrades as the stress voltage or temperature increases. This is because that NBTI can be electrically or thermally activated, leading to the V_{th} shift and drive current degradation. For the n-channel TFTs, the drive current variation exhibits two regimes: in the low stress voltage regime, the drive current increases with the stress voltage; in the high stress voltage regime, the drive current decreases as the stress voltage increases. In the low stress voltage regime, the drive current increase is due to the μ_{FE} enhancement. In the high stress voltage regime, the ΔV_{th} becomes so large that the effect of mobility enhancement is screened; therefore, the drive current decreases with the stress voltage. The comparison of the effects of NBTI and PBTI on the TFT performance is shown in Table 3-1.

3.4 Summary

In this study, the mechanisms of NBTI and PBTI in LTPS TFTs were analyzed. The $|\Delta V_{th}|$ increases with the stress gate voltage. However, as the stress temperature increase, the $|\Delta V_{th}|$ increases under NBTI stress but almost unchanged under PBTI stress. Furthermore, the μ_{FE} is rarely changed under NBTI stress but increases under PBTI stress. From our analysis, the NBTI-degradation mechanism in p-channel LTPS TFTs is attributed to the diffusion-controlled electrochemical reactions, while the PBTI-degradation in n-channel LTPS TFTs is arisen from the charge trapping in the gate dielectric.

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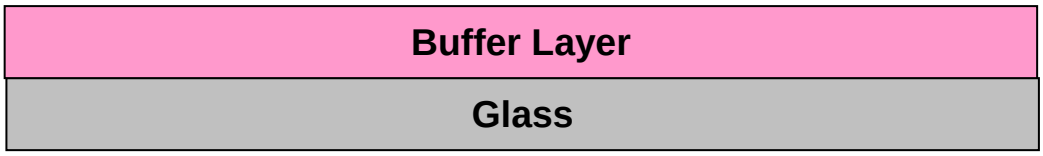
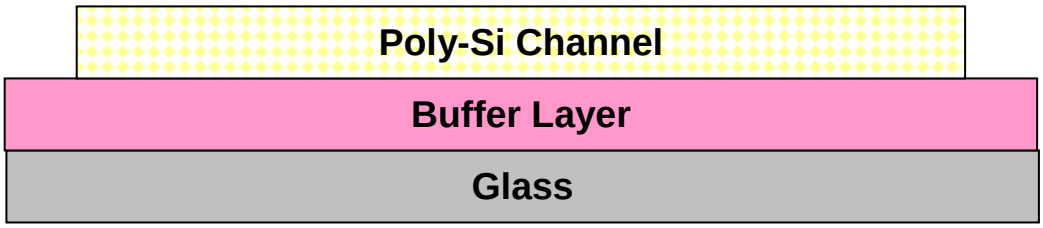
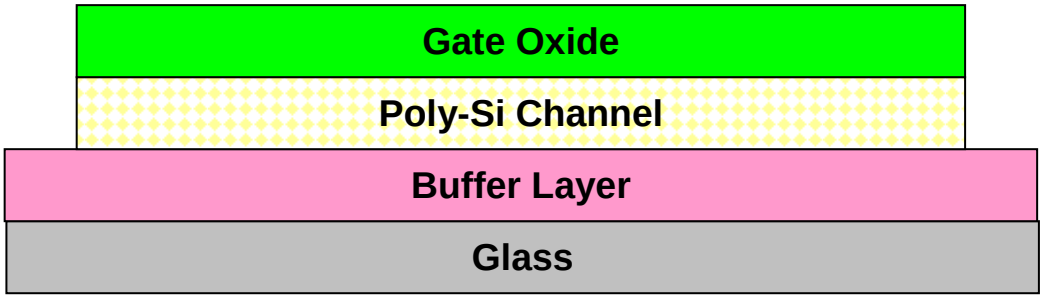


(a) Buffer layer deposition on glass substrate.

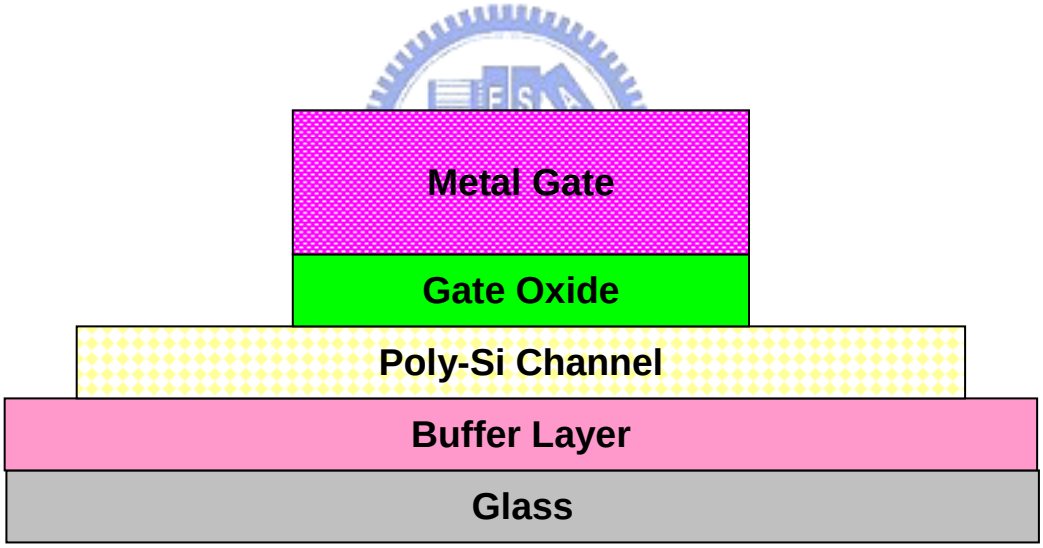
(b) Amorphous Si (a-Si) deposited by PECVD.



(c) Crystallization of a-Si film into poly-Si film by excimer laser annealing, and active region defined.

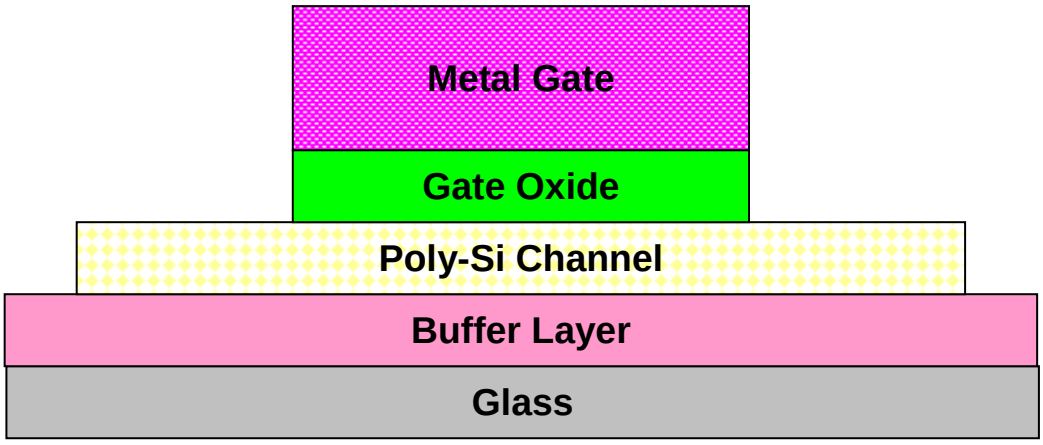


(d) Deposition .of gate oxide by PECVD

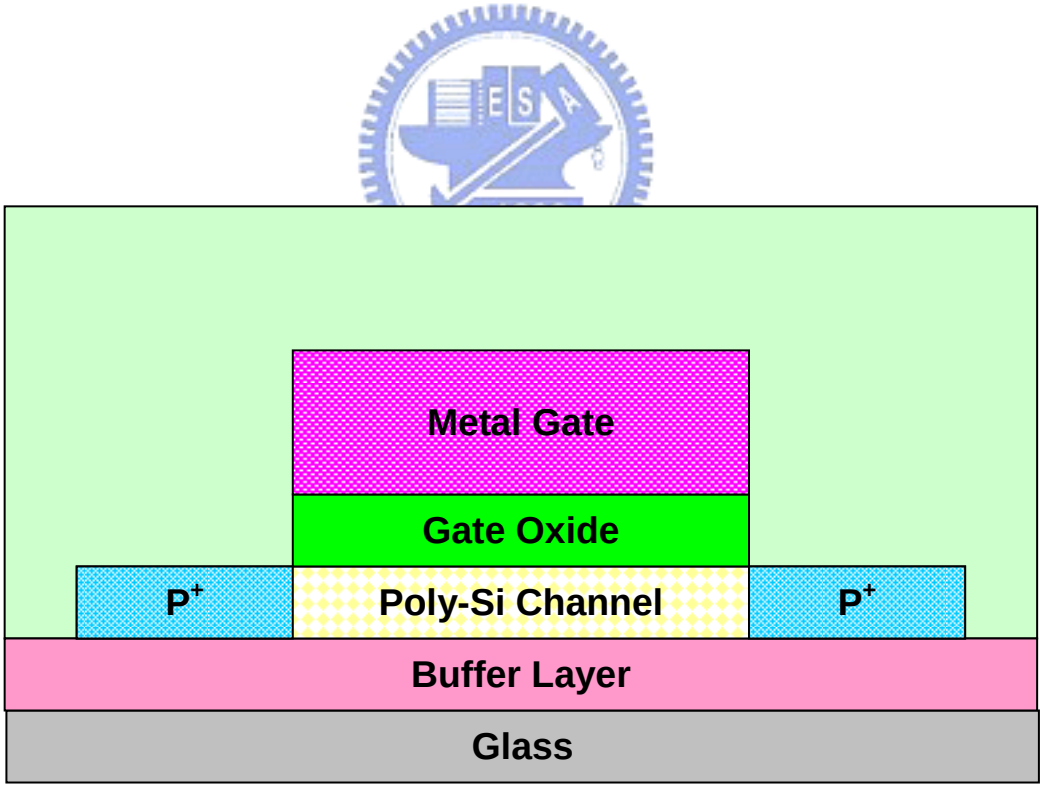


(e) Deposition Mo as the gate electrode.

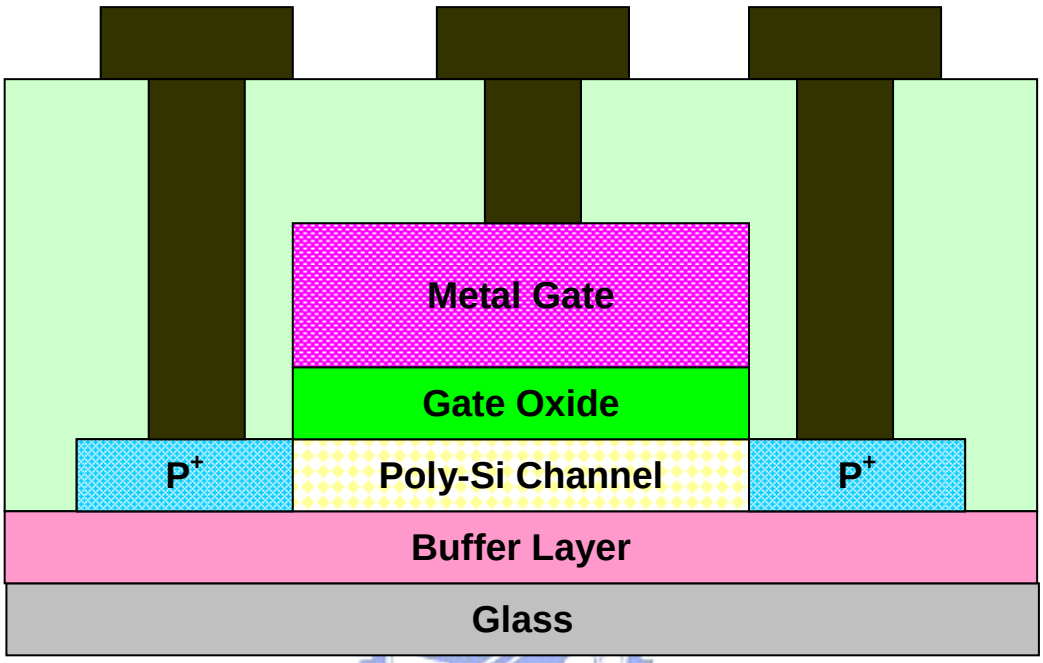
Plasma Doping



(f) Self-align Source/Drain was formed.



(g) Interface layer deposition and dopant activation.



(h) Contact holes were opened and inter-connection metal was deposited and patterned.

Fig. 3-1 Process flow of the poly-Si TFT.

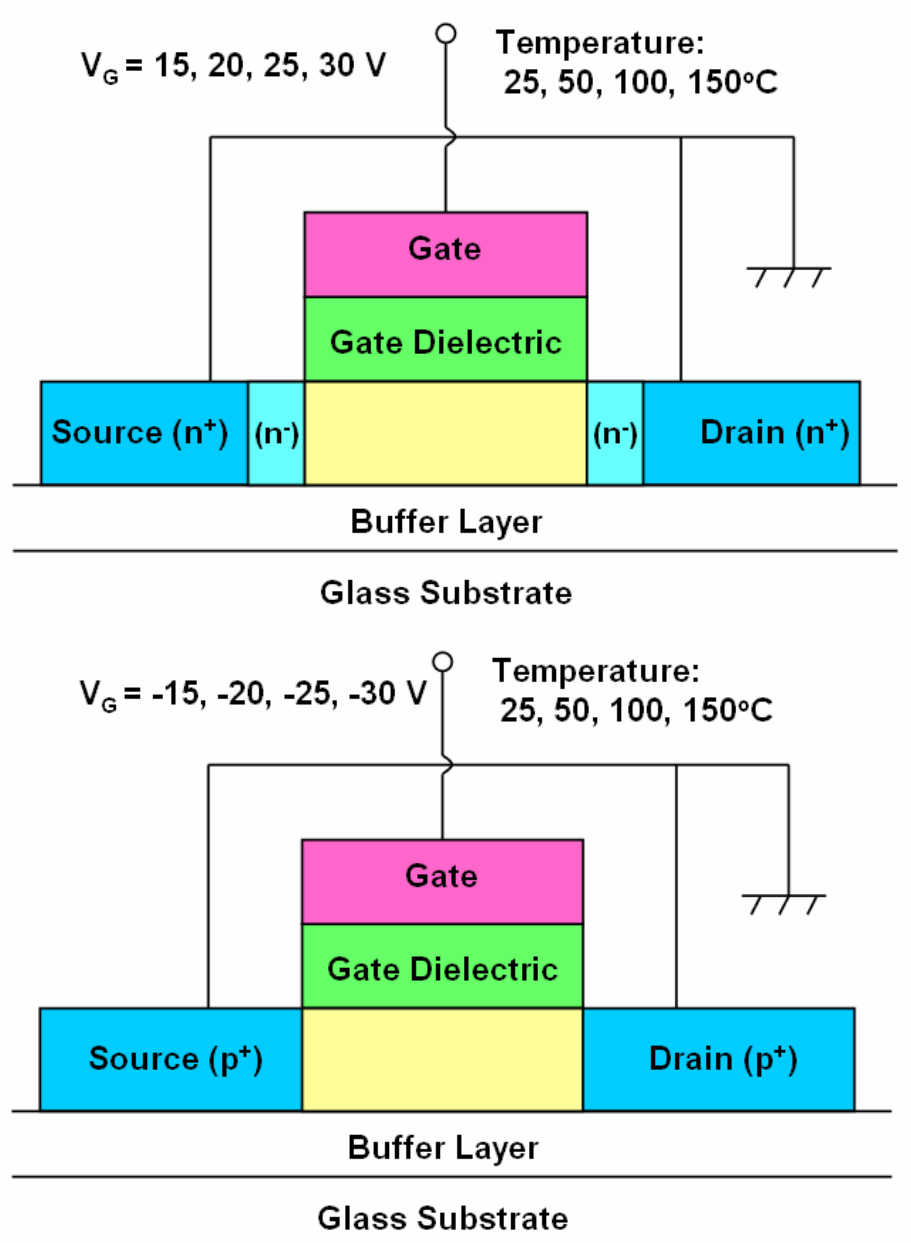


Fig. 3-2 Schematic cross-section diagram of LTPS TFT and NBTI stress setup. The stress temperature was performed from 25°C to 150°C, and the stress gate voltage was applied in the range of -15V to -30V with source and drain grounded.

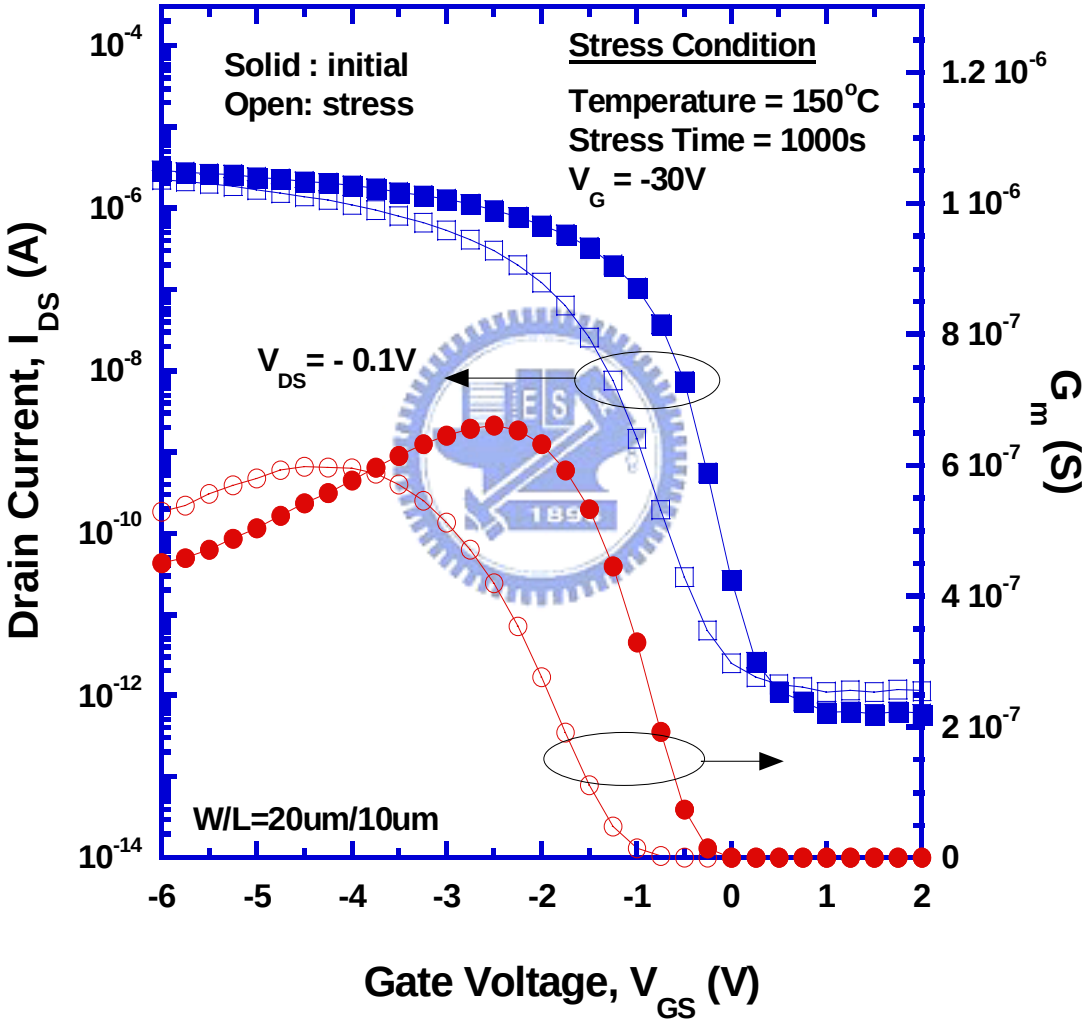


Fig. 3-3 (a) Transfer characteristics of LTPS TFT before and after 1000sec NBTI stress at 100°C with the stress voltage of -30V.

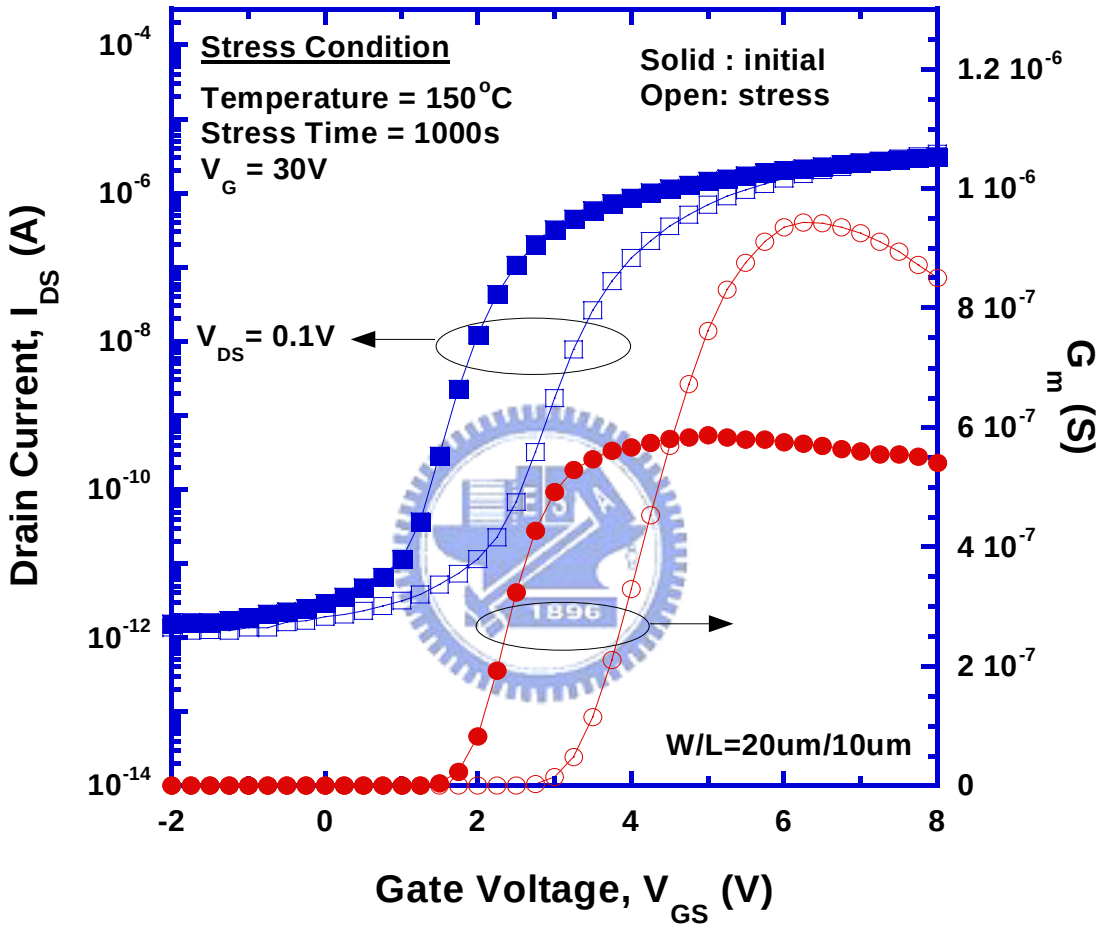


Fig. 3-3(b) Output characteristics of LTPS TFT before and after 1000sec NBTI stress at 100°C with the stress voltage of -30V.

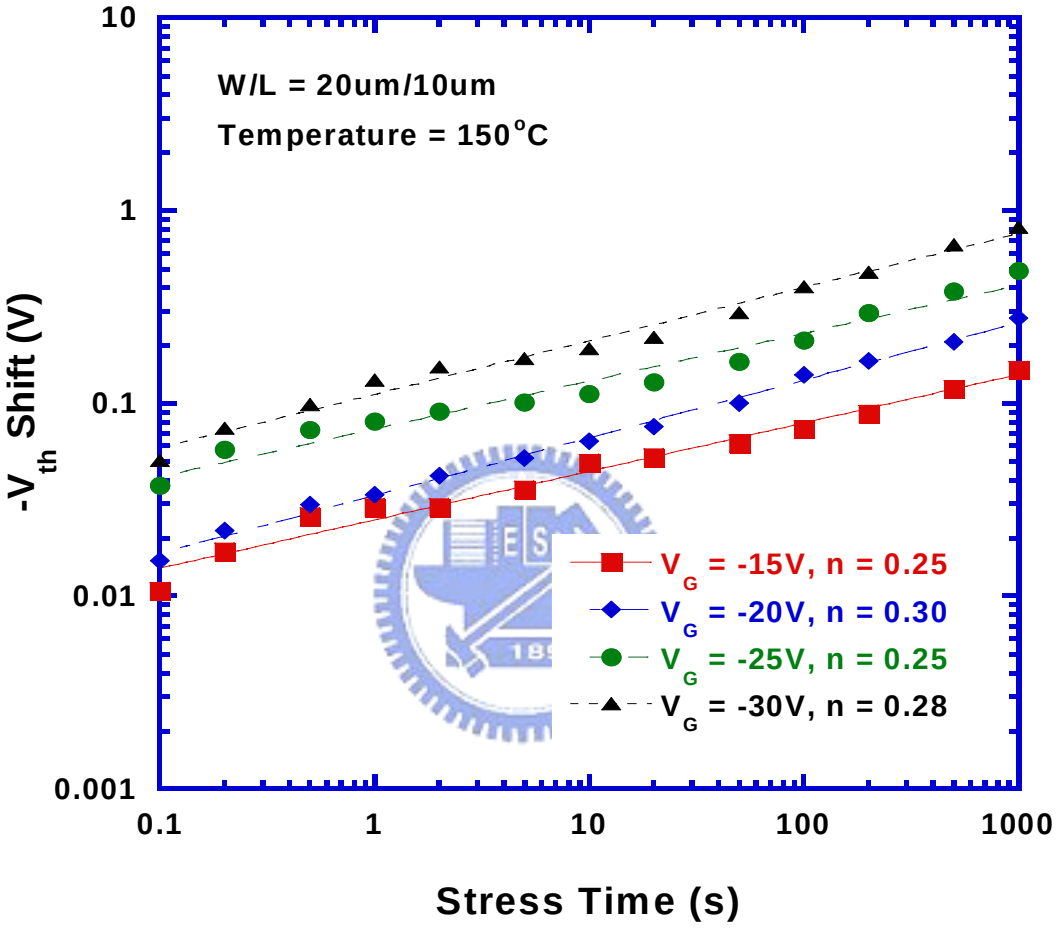


Fig. 3-4(a) Dependences of threshold voltage shift on the stress time of LTPS TFTs under various stress conditions

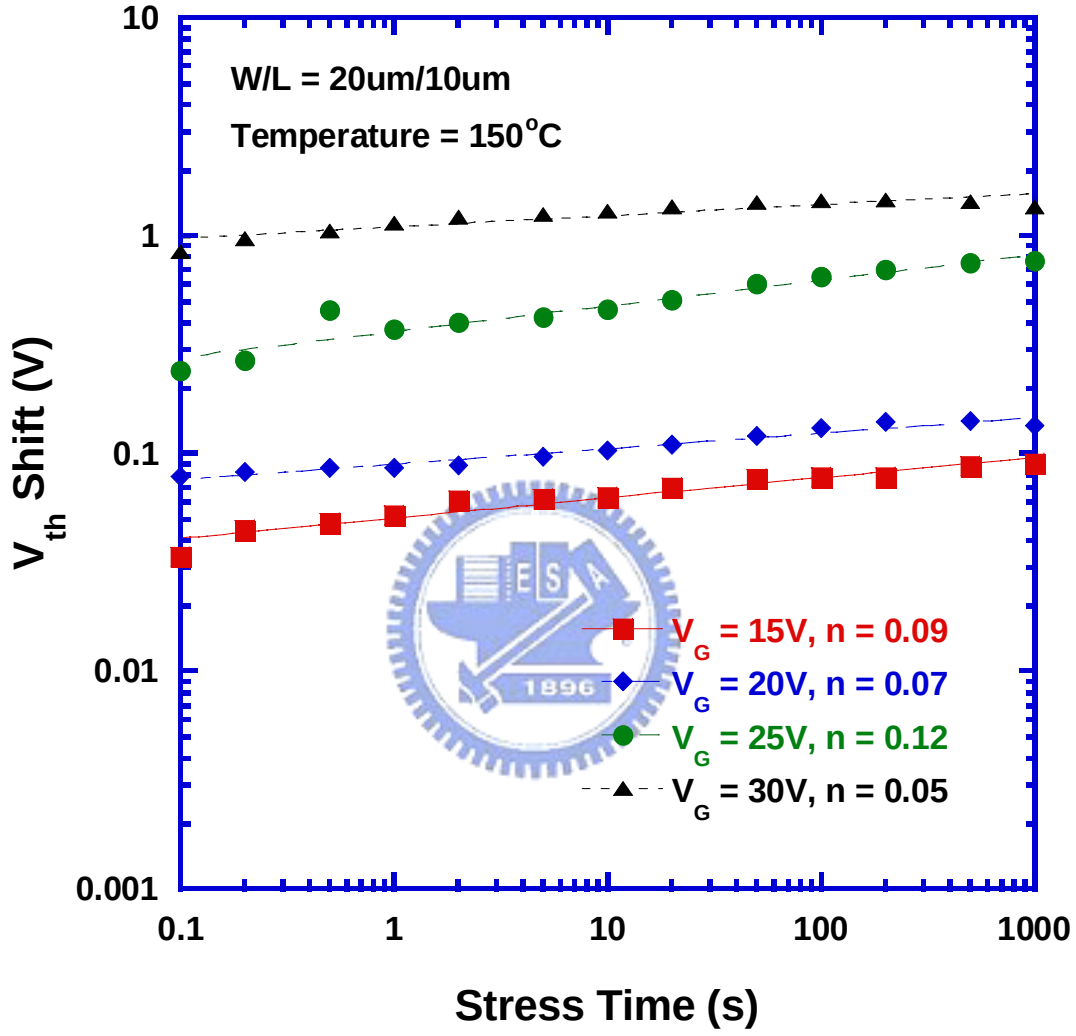


Fig. 3-4(b) Dependences of threshold voltage shift on the stress voltage of LTPS TFTs under various stress conditions

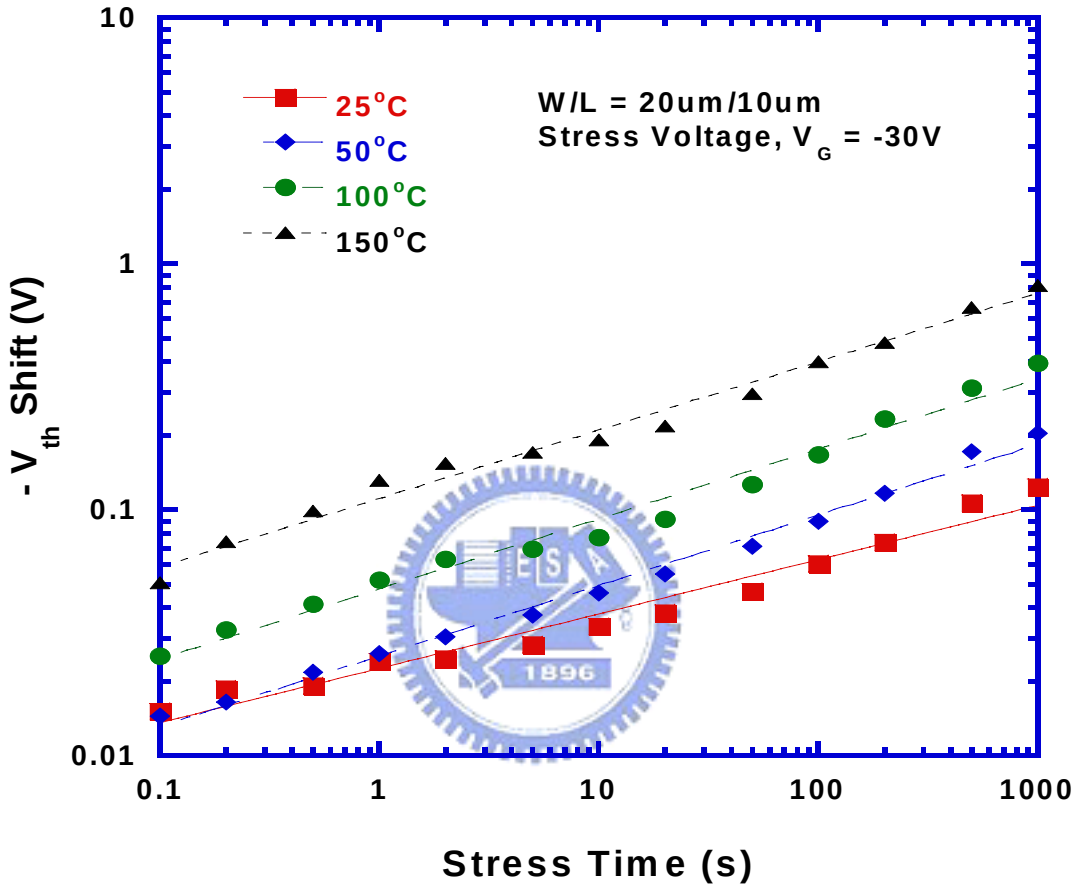


Fig. 3-5(a) Time dependence of the ΔVth of p-channel and under various stress temperatures.

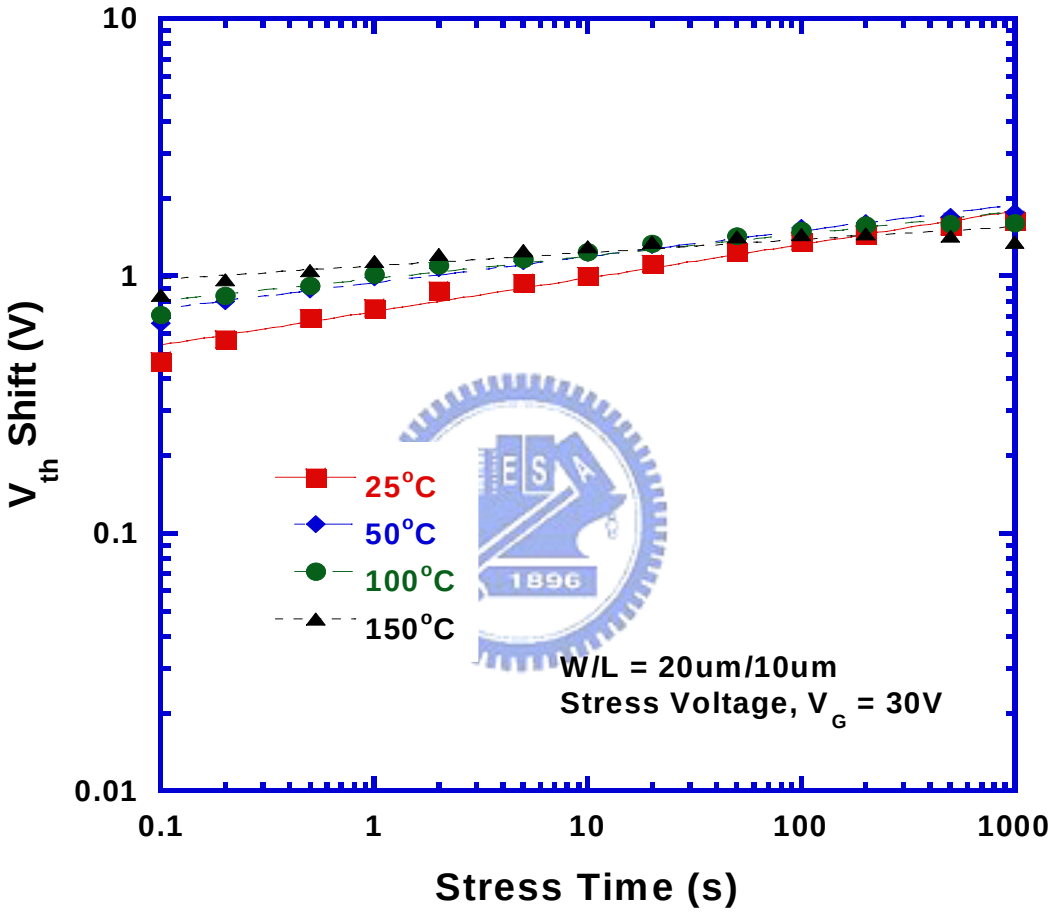


Fig. 3-5(b) Time dependence of the ΔVth of n-channel TFTs under various stress temperatures..

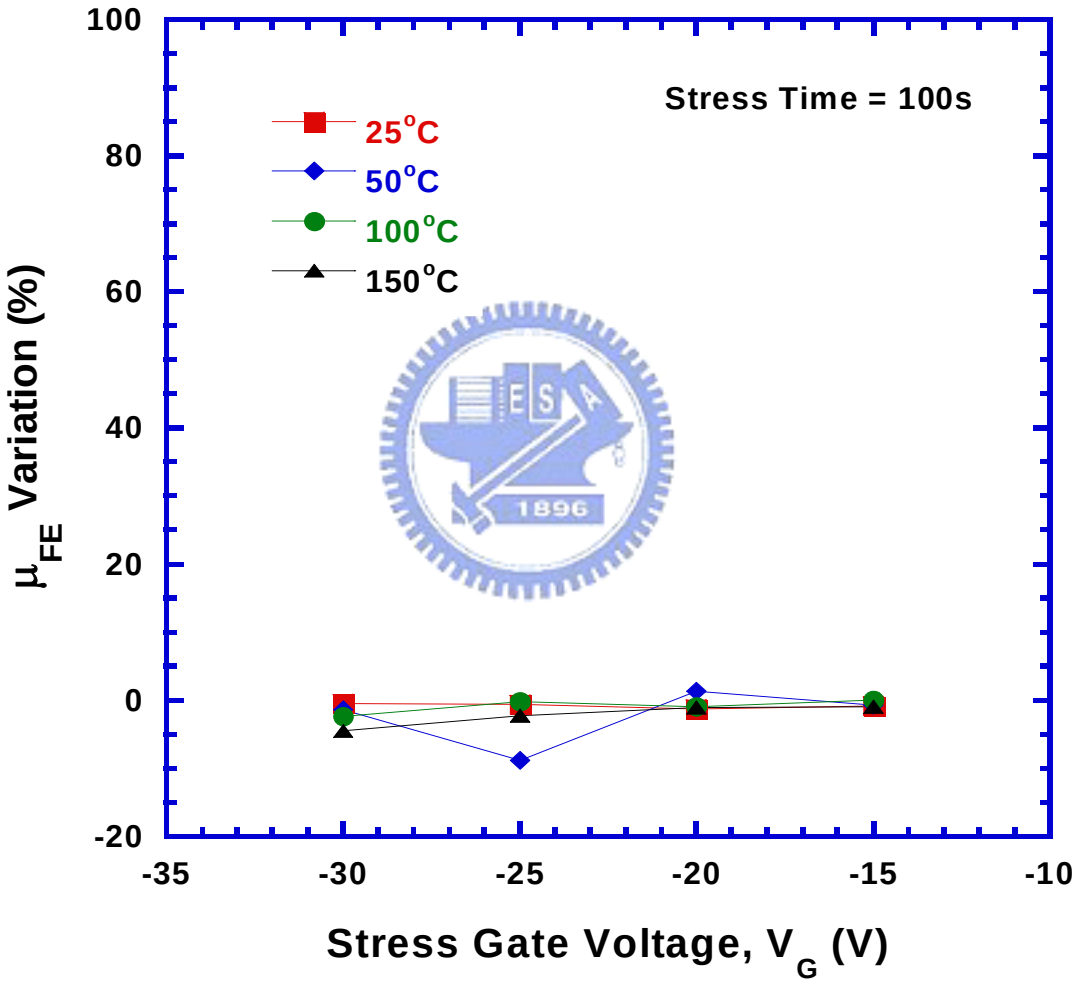


Fig. 3-6(a) Correlation between the degradation of subthreshold swing, and threshold voltage shift of p-channel LTPS TFTs after NBTI stress.

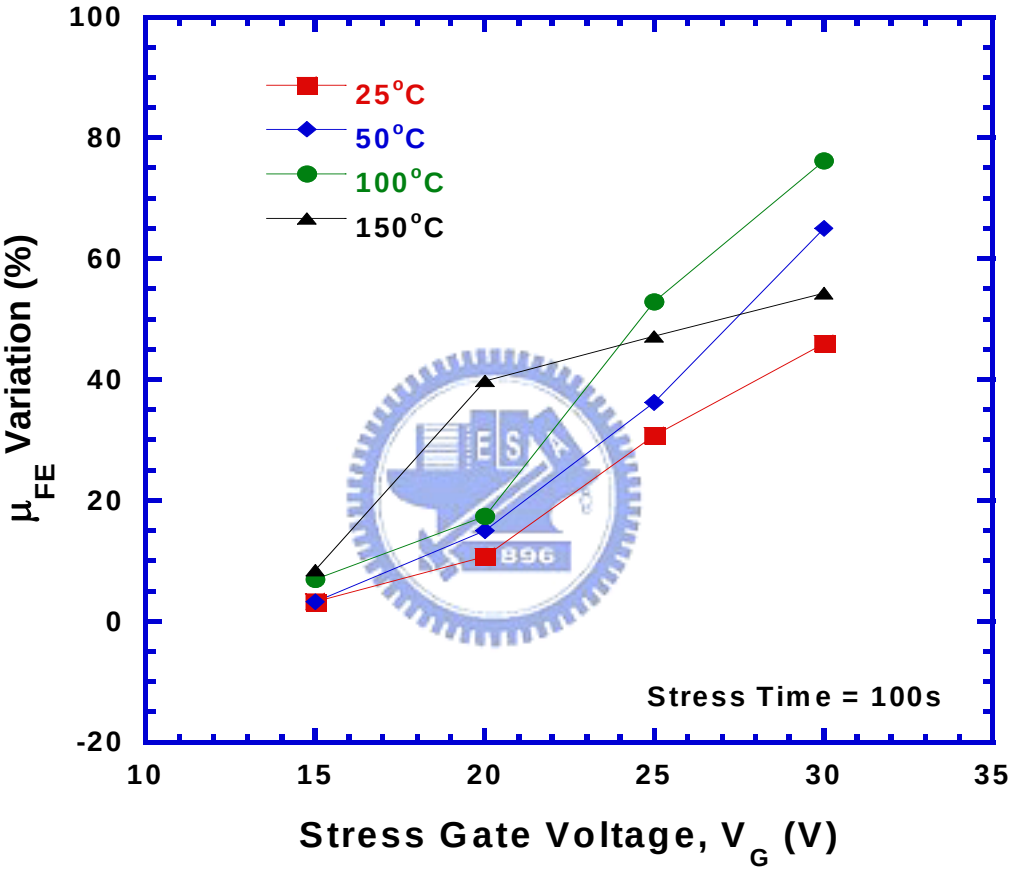


Fig. 3-6(b) Correlation between the degradation of maximum transconductance, and threshold voltage shift of n-channel LTPS TFTs after NBTI stress.

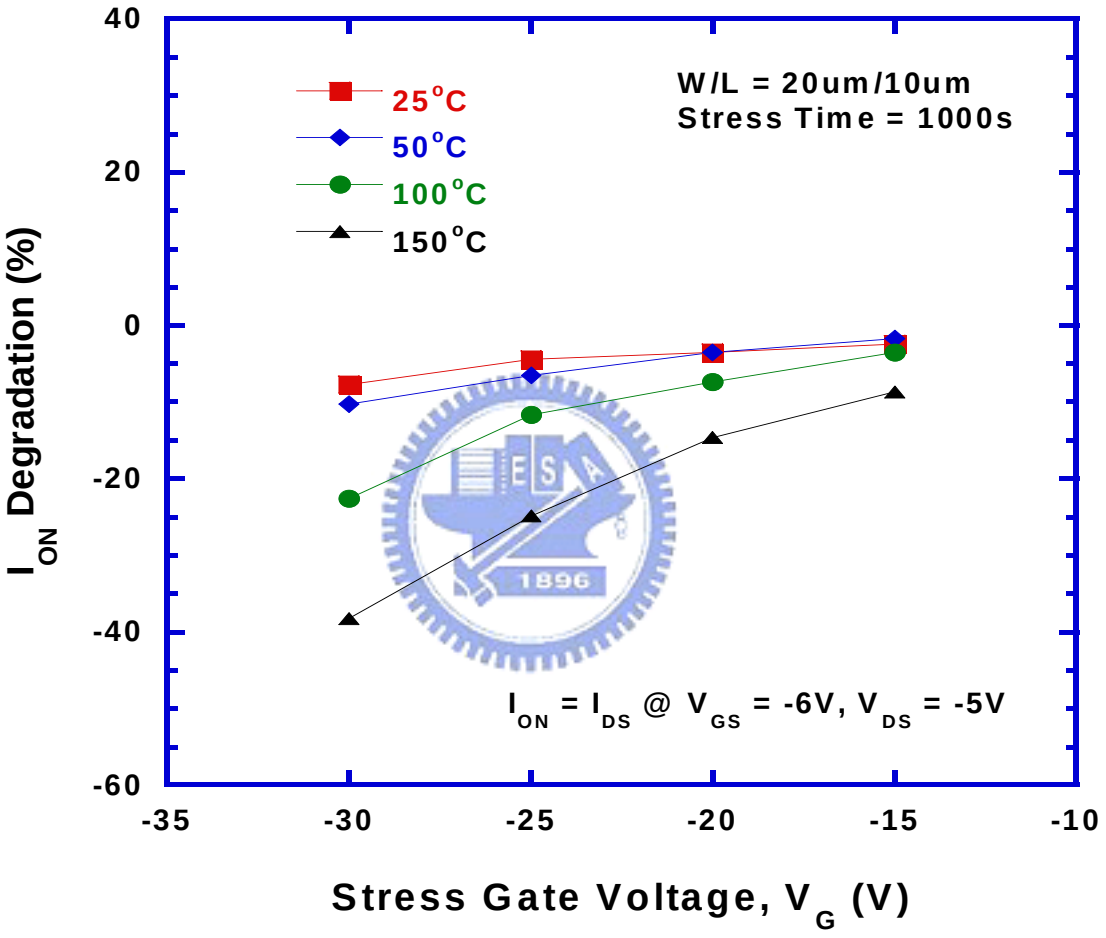


Fig. 3-7 (a) Drive current variation as a function of the stress voltage for p-channel LTPS TFTs.

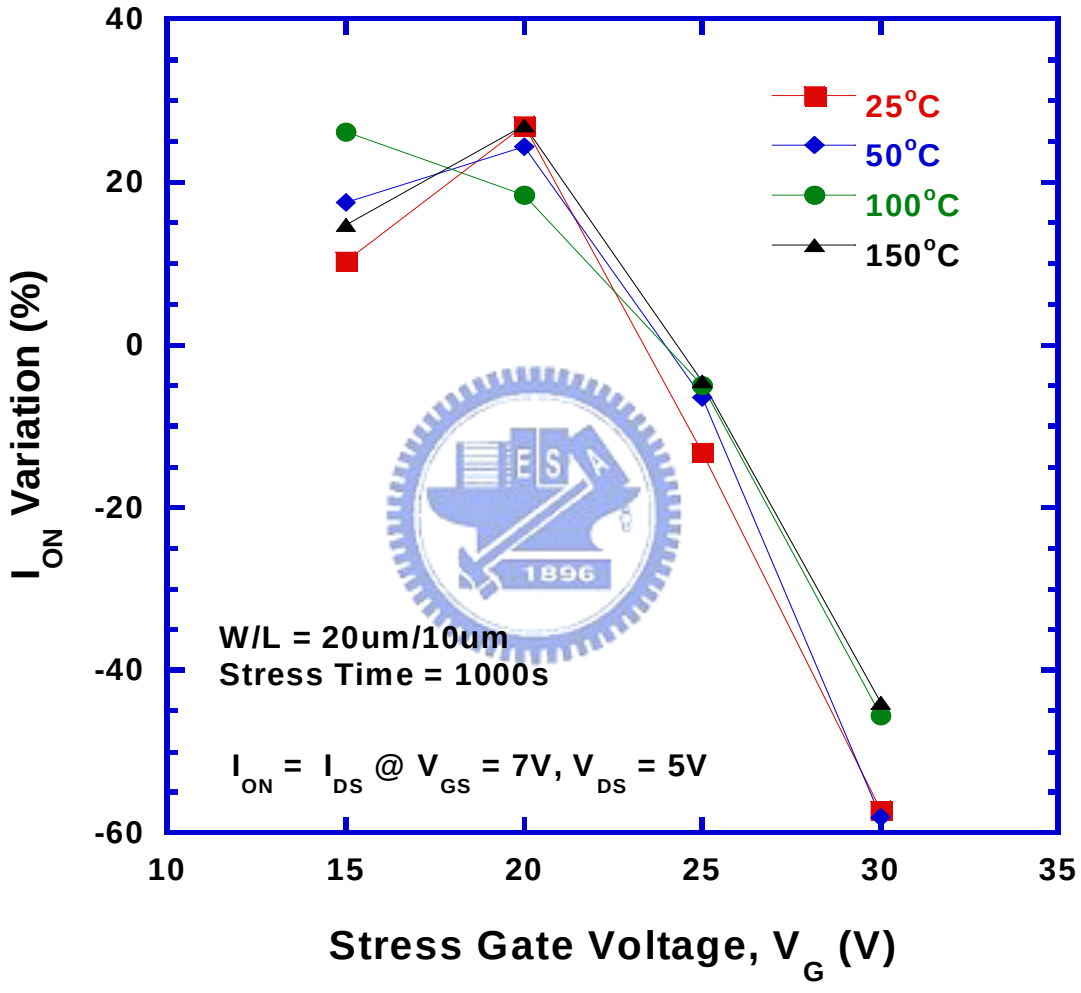


Fig. 3-7 (b) Drive current variation as a function of the stress voltage for n-channel LTPS TFTs.

Table 3-1 Comparison of the effects of NBTI and PBTI on the TFT performance.

	PBTI			NBTI		
	$\|\Delta V_{th}\|$	μ_{FE}	I_{ON}	$\|\Delta V_{th}\|$	μ_{FE}	I_{ON}
| Vg | ↑	↑	↑	↑↓	↑	=	↓
T↑	=	↑	=	↑	=	↓
n	0.05~0.12			0.25~0.30		

Chapter 4

Dynamic Negative Bias Temperature Instability of Low-Temperature Poly-Silicon Thin-Film Transistors

4.1 Introduction

Low temperature poly-Si thin film transistors (LTPS TFTs) are now widely investigated for their potential application in active matrix liquid crystal displays (AMLCDs) [1]-[3] and realization of system on panel (SOP) [4]. For the LTPS TFTs to be used for advanced analog and mixed signal circuit, the electrical stability becomes an important issue. In the pervious studies, NBTI induced device parameter degradation is a serious reliability concern in advanced analog and mixed signal technologies [5]-[8]. NBTI induced threshold voltage shifts in p-channel TFTs is a critical issue for these analog circuits. To determine maximum threshold voltage (V_{th}) shift in an analog circuit over its operating lifetime, several factors that influence the conventional DC lifetime projection method have been widely investigated. With the continuous scaling of the dimensions of transistors, negative bias temperature instability (NBTI) stress in p-MOS transistors has become one of the most critical reliability issues which determine the lifetime of CMOS devices [9]-[12]

A negative bias applied to the gate electrode of p-MOSFET at elevated temperatures with grounded source and drain was performed in conventional NBTI research. However, p-MOSFETs for a CMOS inverter application, the applied gate bias is alternating from “high” to “low”, followed by “low” to “high” over and over. Therefore, it is necessary to investigate the dynamic pulse condition of application.

Former researches show that there was a passivation mechanism during “high” bias condition, and this passivation mechanism would prolong the lifetime of the p-MOSFET of CMOS inverter [13]-[16]. It was found that a large portion of interface states generated during “low” state would be passivated during “high” state. With this passivation effect, p-MOSFET operating in CMOS inverters would have prolonged lifetime.

In this chapter, we assumed that former researches upon static NBTI effect on p-TFTs had the same drawback as that of p-MOSFETs. Therefore, we applied different DC gate stress voltages under different temperatures to derive the threshold voltage shift of static NBTI. Then, we used different gate voltages from 0V to 20V after 1000 seconds static NBTS to investigate the passivation effect. After the investigation of static NBTI, we applied AC biases to the gate electrodes by varying stress voltages and frequencies under different temperatures to investigate the DNBTI effect. The degradation and passivation abilities for devices with different lengths were also investigated in this chapter.

4.2 Experimental

P-channel LTPS TFTs fabricated on glass substrates were used in this work. A 40nm-thick amorphous silicon layer was deposited on a buffer layer by PECVD at 300^{o}C. The silicon layer was then crystallized into polycrystalline silicon film by excimer laser annealing. Gate dielectric was deposited with an equivalent 100nm-thick SiO_2 layer and followed by Mo deposition as the gate electrode. After gate patterning, source and drain were doped by plasma doping. Then, the inter-layer dielectric was deposited and densified. Finally, inter-connection metal was deposited and patterned. Both the channel length (L) and width (W) of the device used in this work were 20μm.

The static NBTS was performed with V_G of -20V, and the stress temperature was kept at 50 or 100 or 150 ^{o}C for 3000 seconds. V_G = 0V, 10V, and 20V with durations of 1000 seconds right after a 1000-second static NBTS were used to show the passivation effect which would prolong the lifetime of p-MOSFETs during dynamic stress conditions. Then we used pulsed gate biases with different values, different frequencies, and different duty ratios. At last, we used devices with different gate lengths from 5 μm to 20 μm while the gate widths kept the same as 20 μm to investigated the influence of device dimension. The threshold voltage (V_{th}) was measured under the criterion of I_{DS} = (W/L) × 10nA at V_{DS} = -0.1V. The schematic cross-section view of the LTPS TFT and the stress setup is shown in Fig. 4-1.

4.3 Results and Discussion

Fig. 4-3 to Fig. 4-5 show the threshold voltage shift of the devices under stress-passivation-stress process with same stress biases but different passivation biases at different temperatures. During the stress step, the threshold voltage shifts to be more negative. The shift of the threshold voltage also follows a power dependence on the stress time with an exponent factor of 1/3 to 1/4, and this can be explained by the diffusion controlled chemical reactions. The shift of the threshold voltage can be explained by the generation of the interface trap states, including the generation of grain-boundary trap states and fixed oxide charges. When the stress gate voltage switched to zero or positive, the threshold voltage shift was significantly reduced especially when a large gate bias was applied. The threshold voltage recovery was due to the passivation of trap states. Besides, the recovery of the threshold voltage, likes the threshold voltage shift under stress, also follows a power law dependence on the stress time. Fig. 4-6(a) shows the temperature dependence of threshold voltage degradation for static NBTI case while Fig. 4-6(b) shows the stress-passivation-stress

case. The long term threshold voltage degradation and recovery ability of threshold voltage are shown in Fig. 4-7. The lower the temperature was, the larger recovery rate was while the passivation voltage stayed the same as 20V. Fig. 4-8 shows the time dependence of the threshold voltage shift of the devices under dynamic gate bias stress with different frequencies. The threshold voltage exhibits significant frequency dependence, which decreases as the frequency increases. Besides, the threshold voltage shift decreases when the duty ratio of the gate pulse is reduced, shown in Fig. 4-10. To explain the degradation mechanism, we propose a physical model. The Si—H bonds at the SiO_2/Si interface break, followed by the hydrogen species diffuse into the gate oxide during negative bias stressing. Under the passivation condition, the hydrogen species move back to the interface and passivate the dangling bonds there. Therefore, from the experimental results, the degradation mechanism of dynamic negative bias temperature instability can be identified and which may be useful for circuit design. Moreover, we found that channel length of the LTPS TFTs did affect the degradation and passivation effect of threshold voltage shift during NBTI stress and passivation conditions, respectively. With a larger channel length, the device degraded seriously under stress condition and was passivated strongly under passivation condition. We propose that the degradation and passivation were mainly occur near the source and drain regions.

4.4 Summary

Dynamic negative bias temperature instability of p-channel LTPS TFTs has been studied in this article, and we have proved NBTI is important in the reliability of LTPS TFTs. It is found that the threshold voltage of LTPS TFT degraded during static NBTI stress especially under elevated temperature but recovered when zero or positive bias was applied to the gate electrode. The device degradation caused by

NBTI stress increases with temperature and electric field in gate insulator, indicating NBTI can be thermally and electrically activated. Moreover, the recovery of threshold voltage implied that the lifetime of LTPS TFTs would be underdetermined. We found that the either the degradation or the recovery mainly occurred near the SiO_2/Si interface near both the source and drain regimes. In this study, it was proved that the threshold voltage shift was closely related to the grain boundary trap state generation, because both the two physical quantities follow almost the same power low dependence on the stress time; moreover, exponential dependence on the stress voltage and reciprocal of the ambient temperature. The exponent value of the power law dependence on the stress time is about 1/4 to 1/3, which is explained by the diffusion-controlled electrochemical reactions. From the experimental results, we concluded that under stress process of stress-passivation-stress test, the degradation was caused by the generation of fixed oxide charges, interface states and grain boundary trap states in LTPS TFTs, and these generated states resulted in the threshold voltage shift. However, these states were passivated under passivation process and result to the threshold voltage recovery. The rate of state-generation and state-recovery while stress and passivation processes, correspondingly, were strongly dependent on temperature and applied bias. Moreover, we found that the degradation of device was strongly dependent on the frequency of the applied dynamic gate bias. Although static NBTS is a good method to determine the reliability of p-channel LTPS TFTs, it is much better for LTPS TFTs used in inverters to be tested under particular dynamic bias condition, including bias frequencies and magnitudes to approach their real lifetime. Furthermore, a physical model is proposed and verified by the experimental results.

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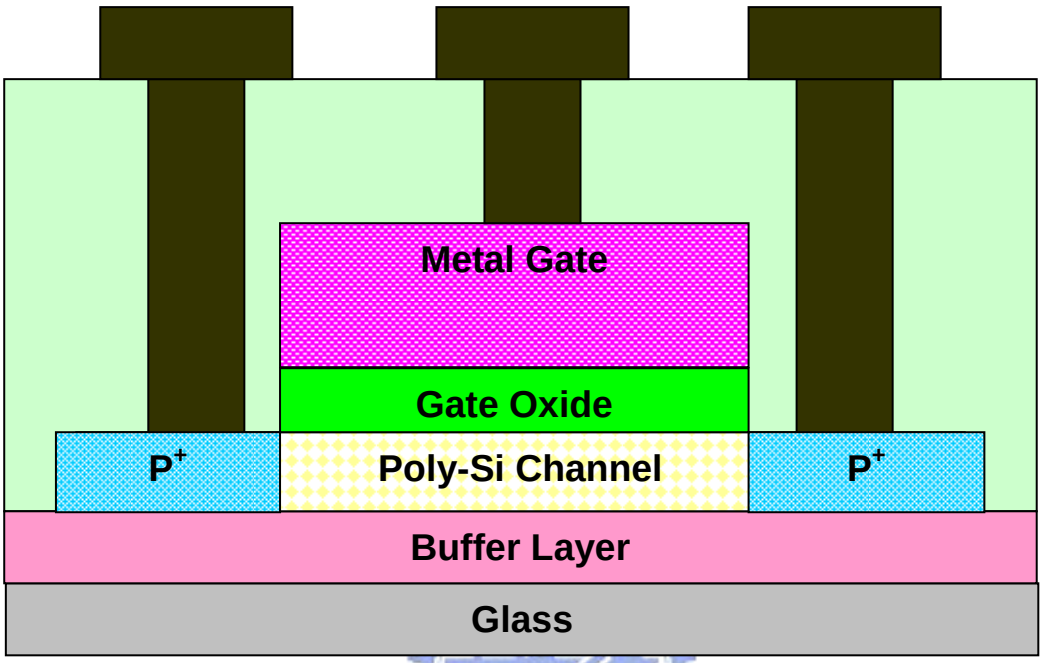


Fig. 4.1 The schematic cross-section diagram of the test LTPS TFT structure.

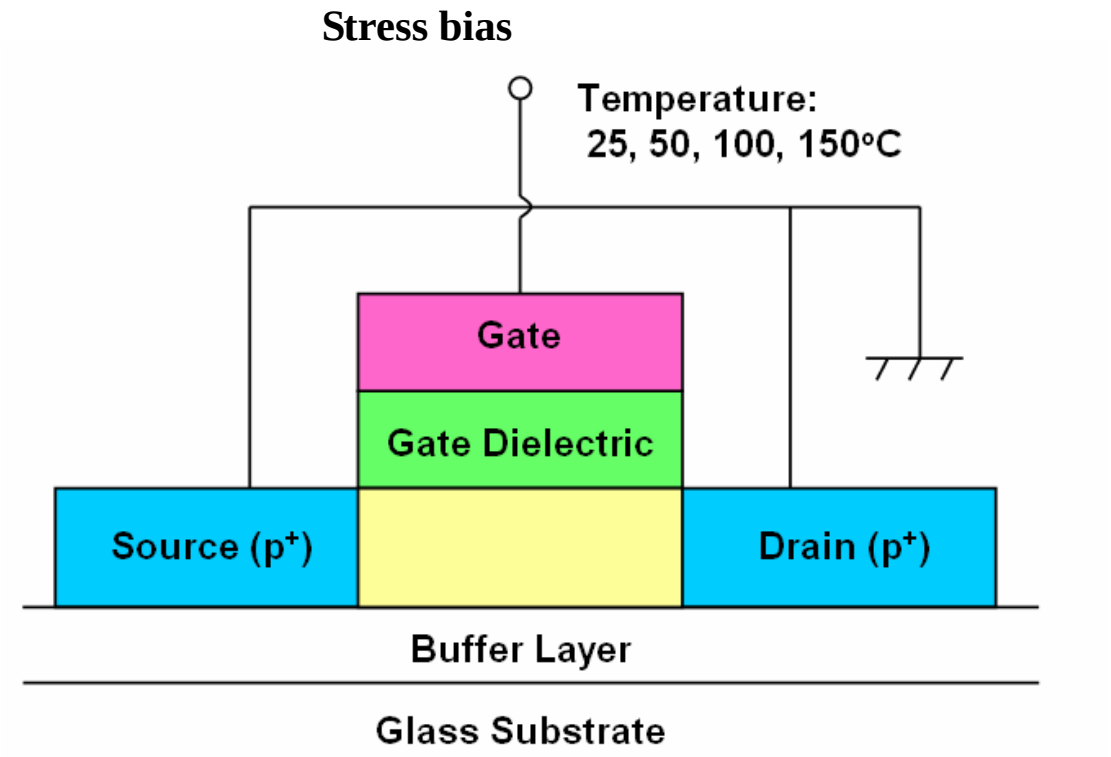
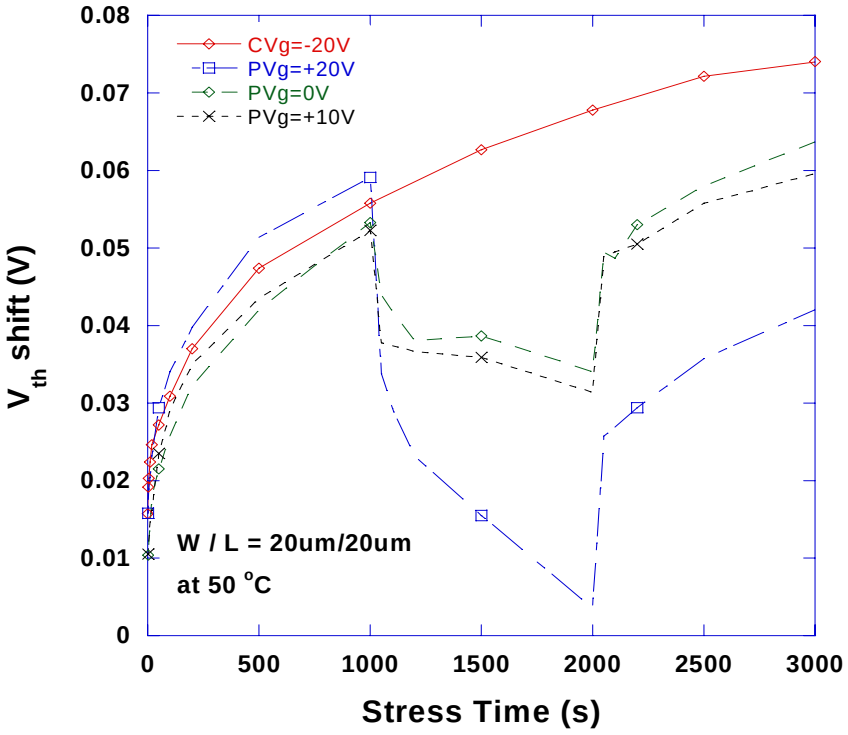
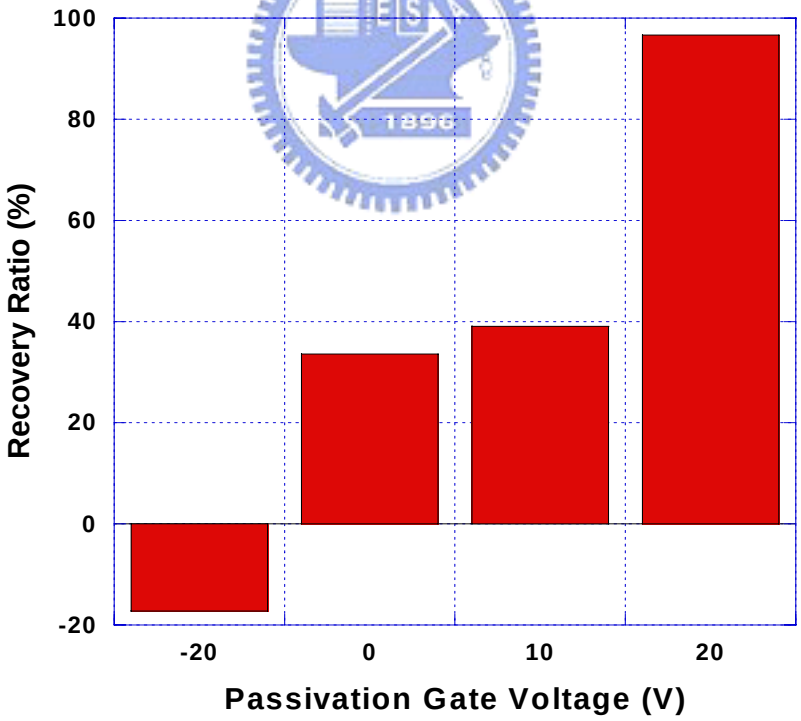


Fig. 4-2 Shcematic cross-section diagram of LTPS TFT and DNBTI stress setup. The stress temperature was performed from 25°C to 150°C, and the stress bias was applied to the gate electrode while source and drain electrodes were grounded.

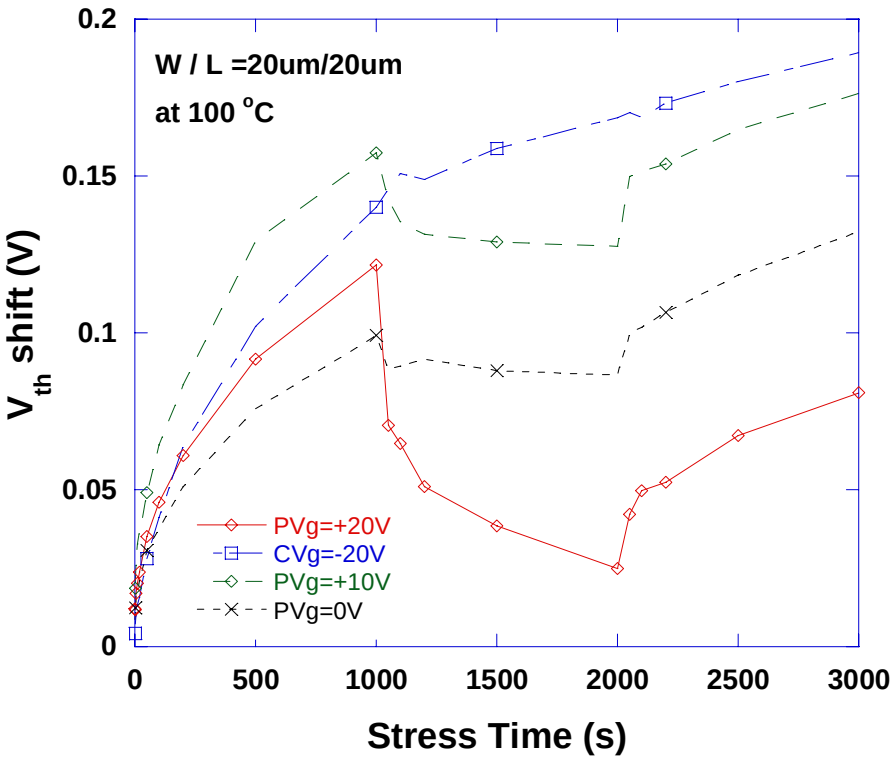


(a) Threshold voltage shift during stress-passivation-stress process with different passivation voltage at 50°C.

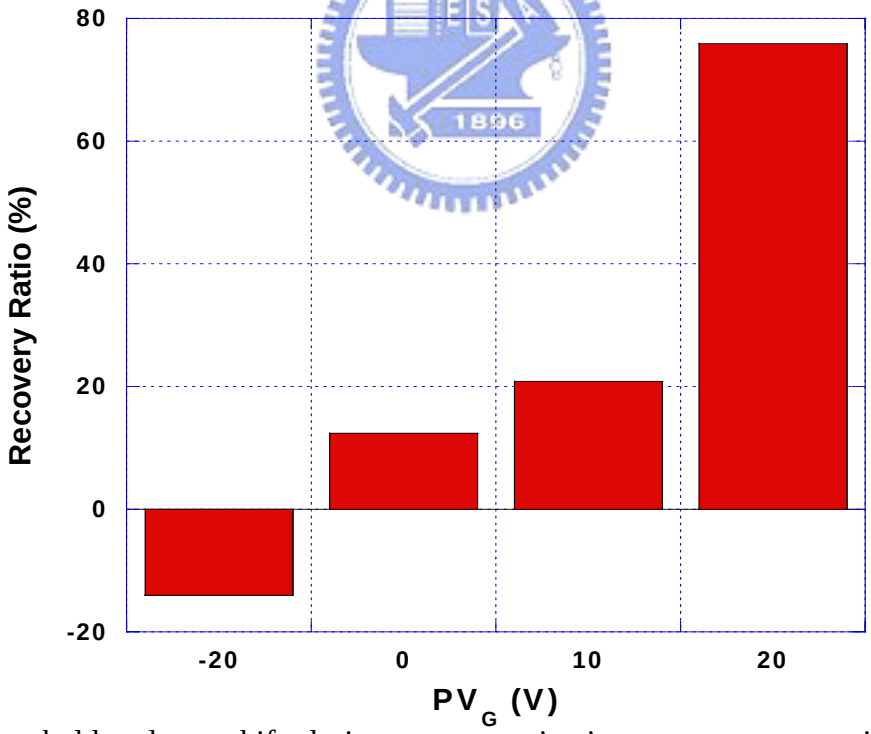


(b) Threshold voltage recovery ratio during stress-passivation-stress process with different passivation voltage at 50°C.

Fig. 4-3 Threshold voltage degradation and recovery under different passivation biases at 50°C

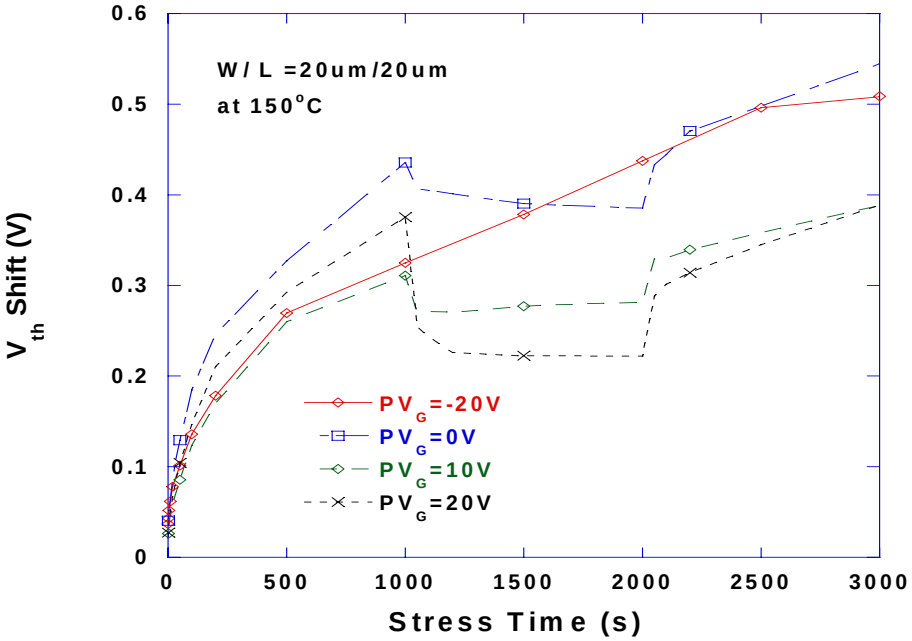


(a) Threshold voltage shift during stress-passivation-stress process with different passivation voltage at 100°C.

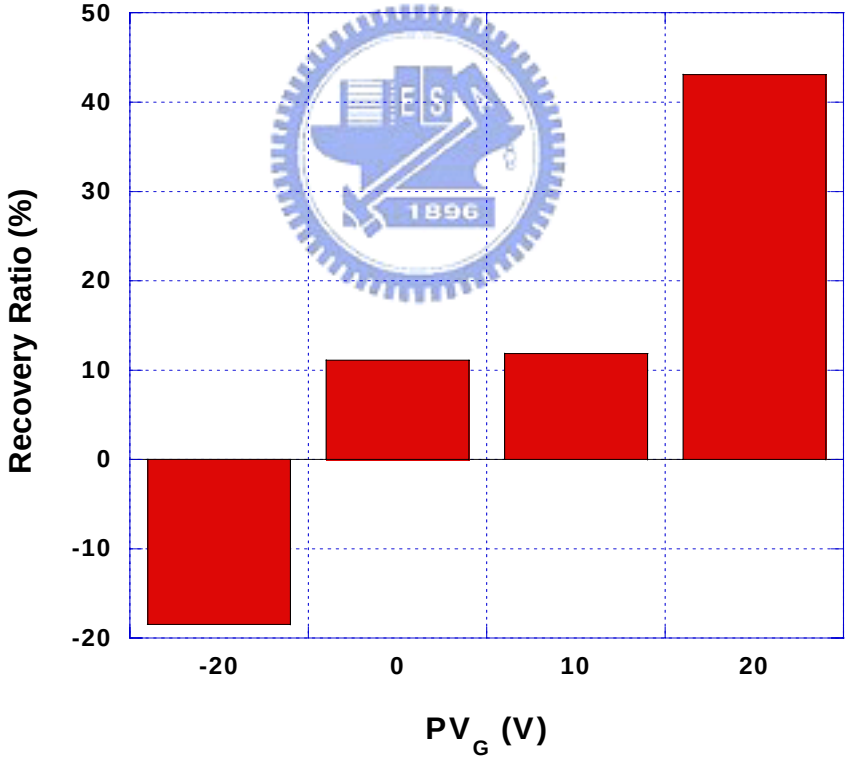


(b) Threshold voltage shift during stress-passivation-stress process with different passivation voltage at 100°C.

Fig. 4-4 Threshold voltage degradation and recovery under different passivation biases at 100°C

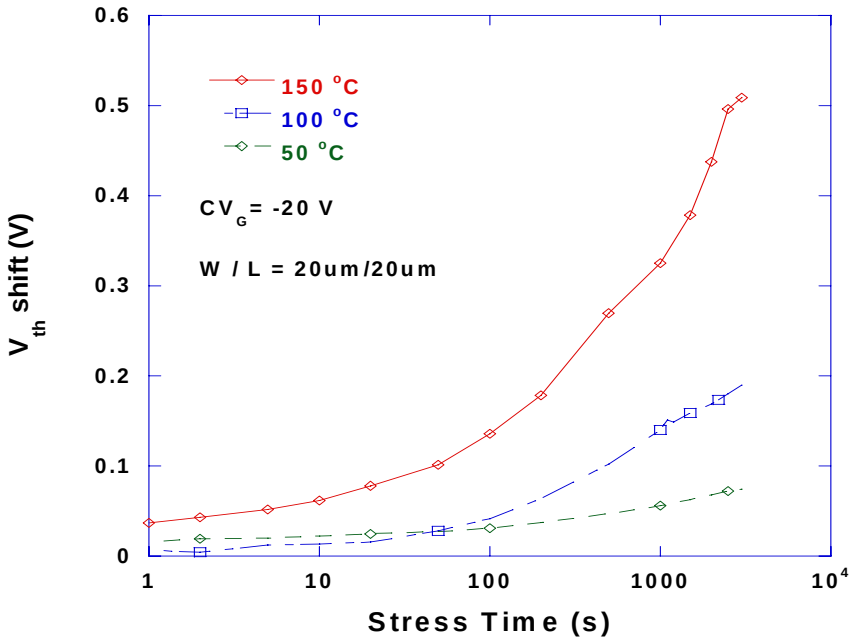


(a) Threshold voltage shift during stress-passivation-stress process with different passivation voltage at 150°C.

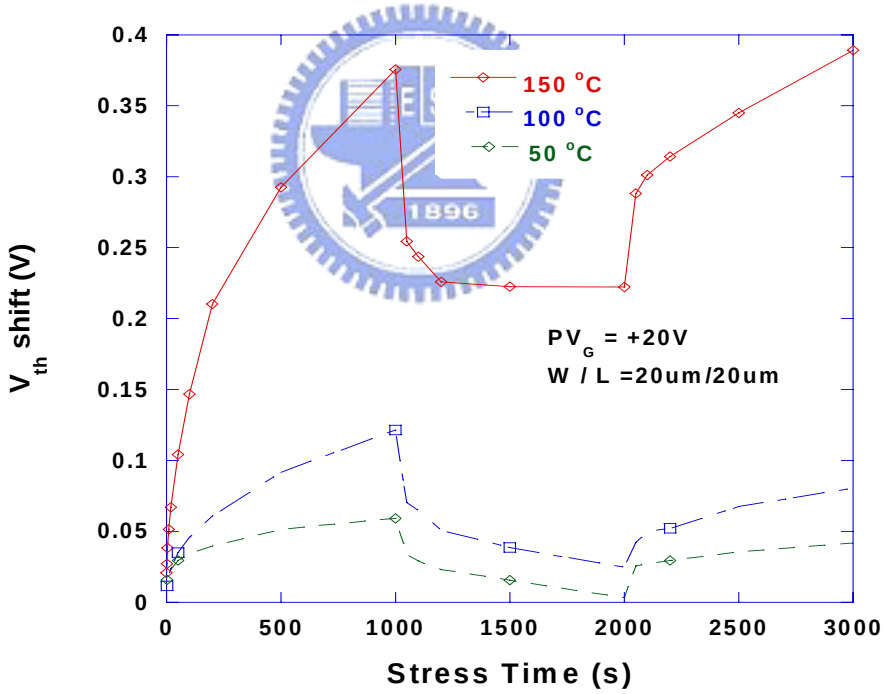


(b) Threshold voltage shift during stress-passivation-stress process with different passivation voltage at 150°C.

Fig. 4-5 Threshold voltage degradation and recovery under different passivation biases at 150°C



(a) Threshold voltage shift during static NBTS under different temperatures



(b) Threshold voltage degradation and recovery under different temperatures

Fig. 4-6 NBTI degradation and recovery during long-period stress and passivation.

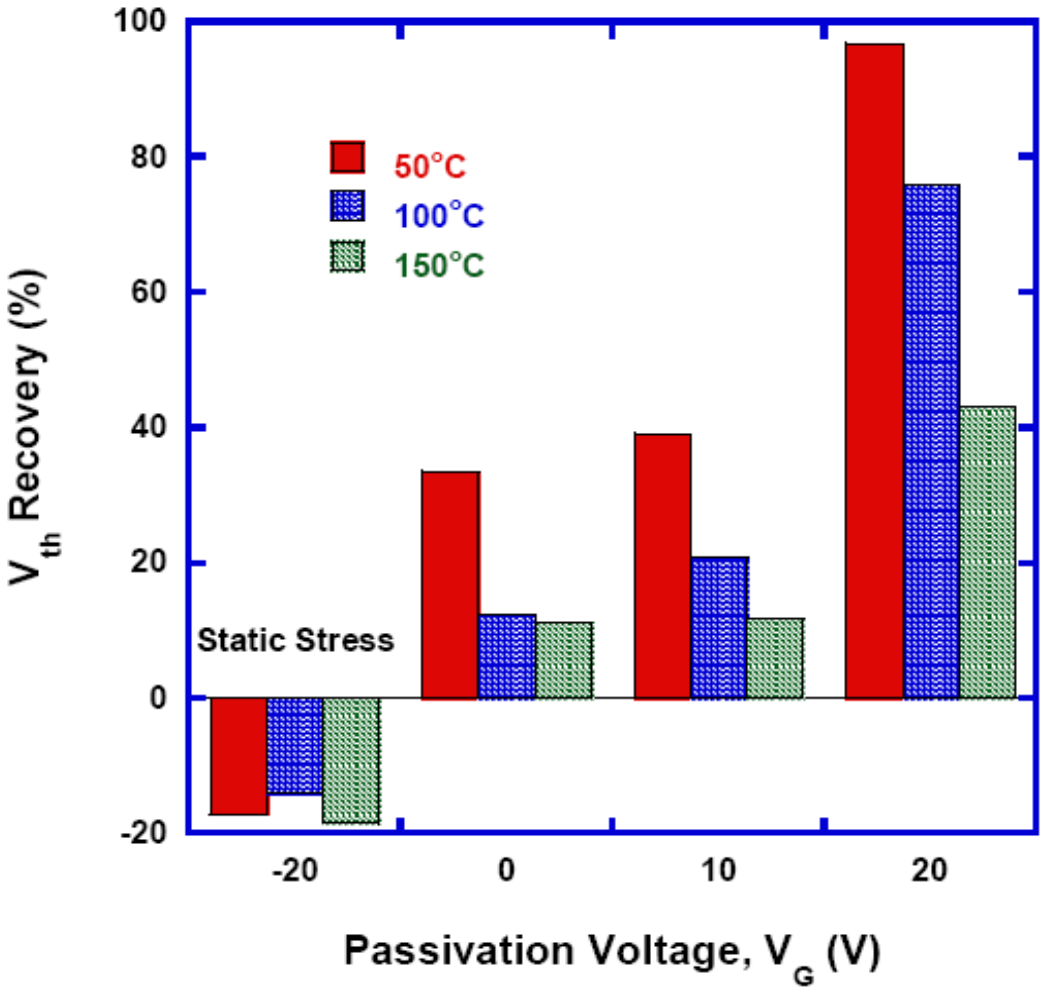


Fig. 4-7 Comparison of threshold voltage recovery dependence on temperature and passivation voltage

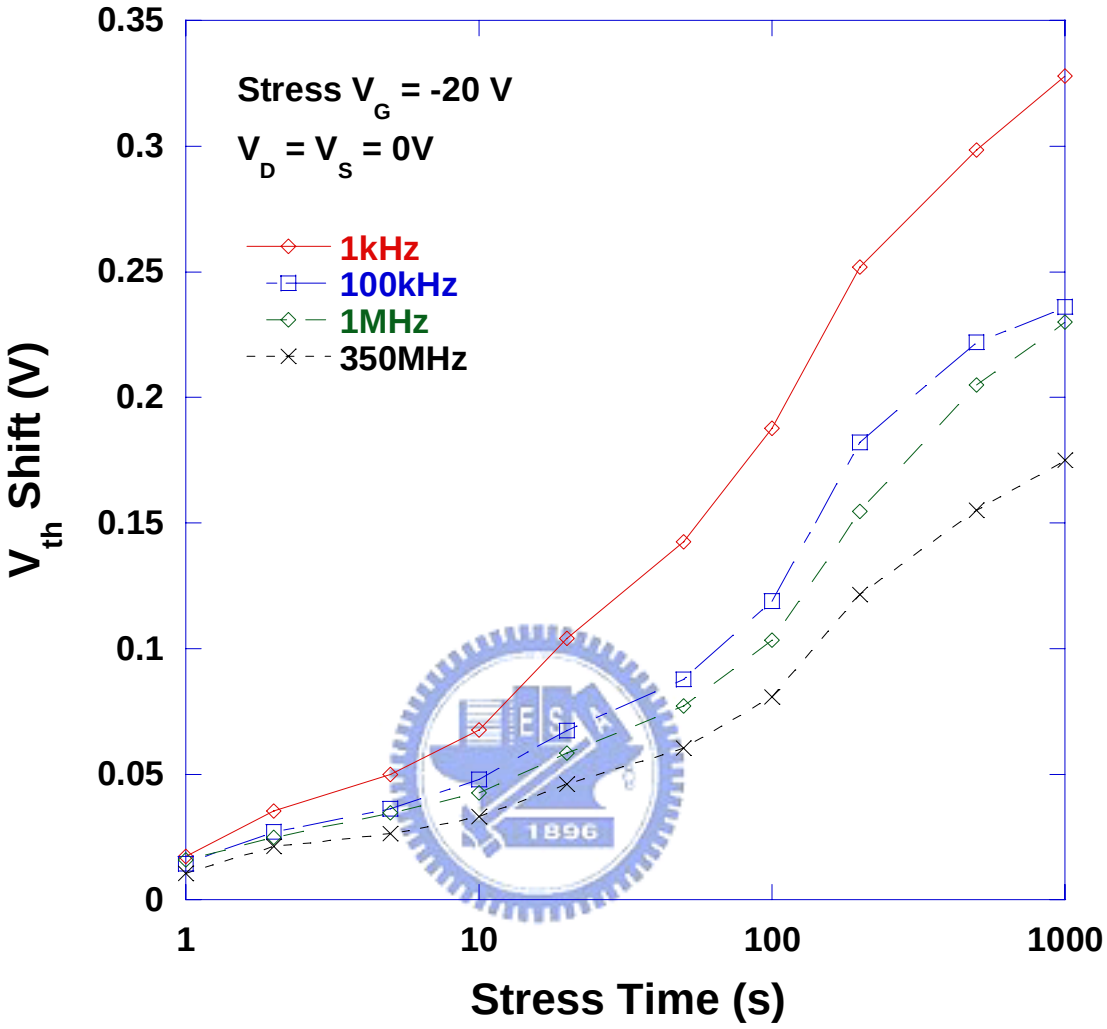


Fig 4.8 Threshold voltage shift during DNBTI with different stress frequencies

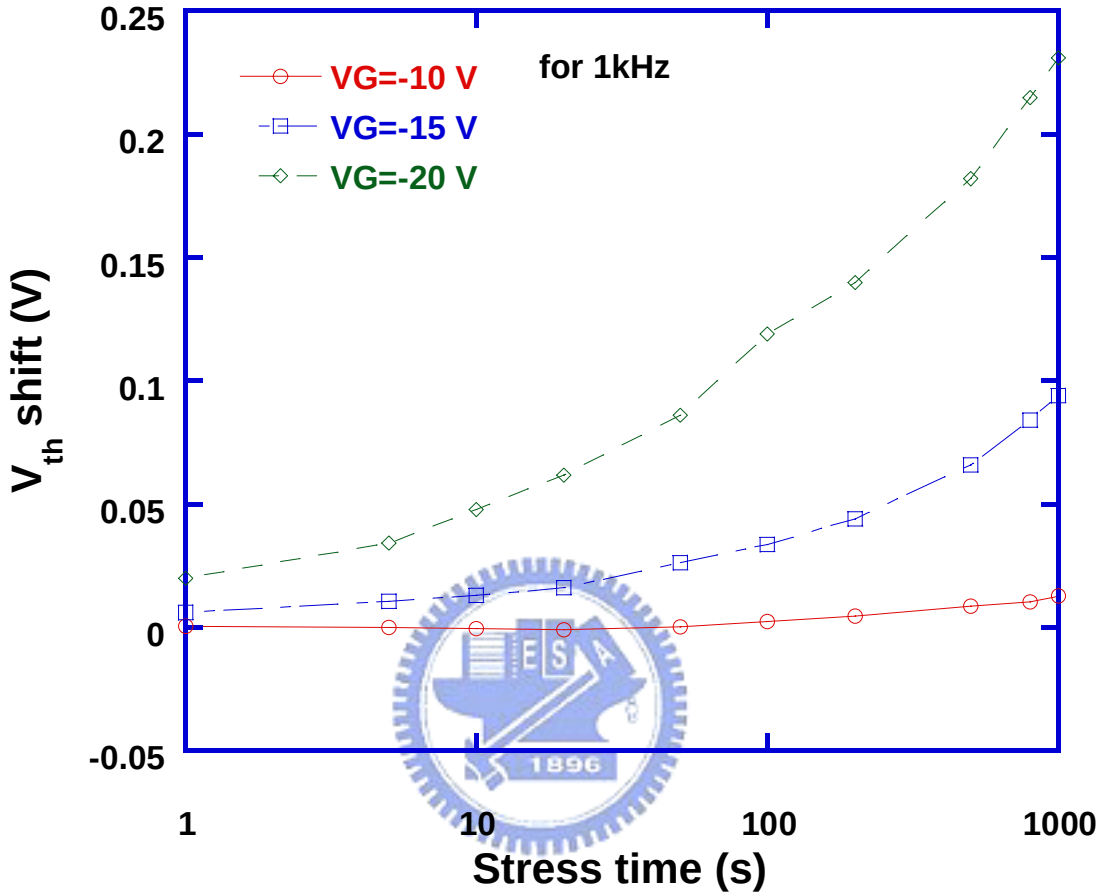


Fig 4.9 Threshold voltage shift during DNBTS with different stress biases

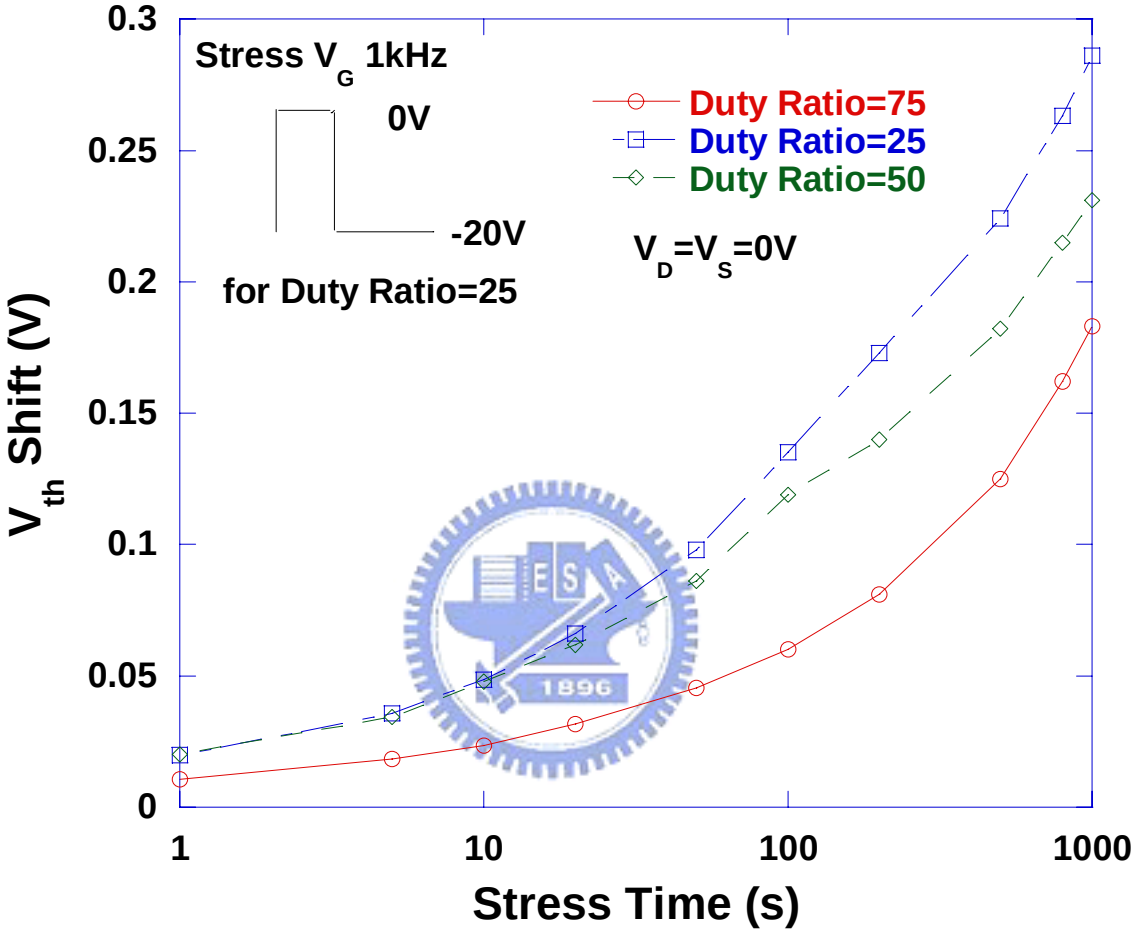
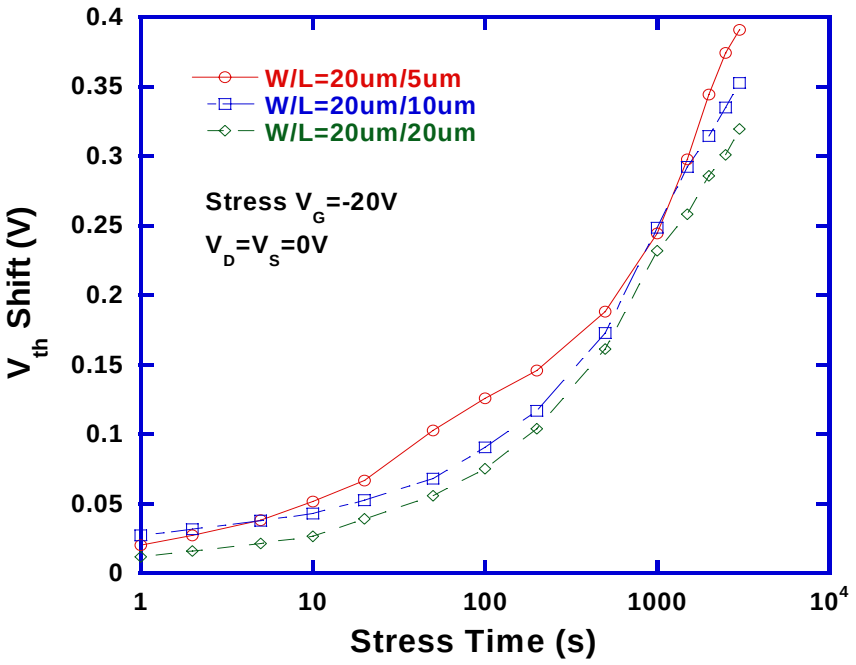
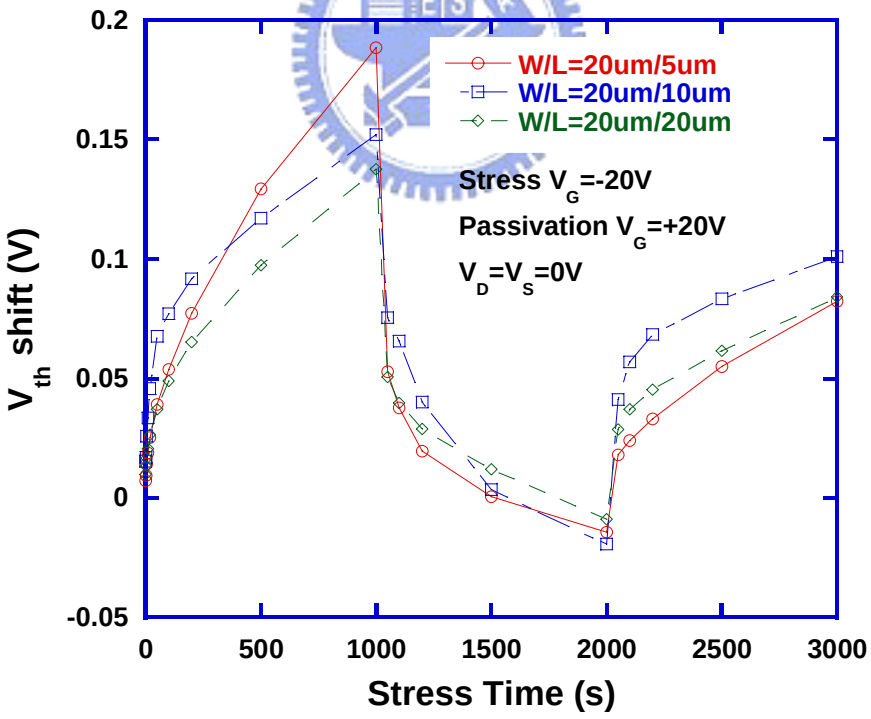


Fig 4.10 Threshold voltage shift during DNBTI stress with different duty ratio



(a) Threshold voltage shift during NBTS of different-dimension devices



(c) Threshold voltage degradation and recovery during stress-passivation-stress process for different-dimension devices

Fig 4.11 Dependence of device dimension to threshold voltage and recovery during NBTS

Chapter 5

Conclusions

In this thesis, first, two simple and process-compatible methods used to fabricate poly-Si TFTs were proposed. The post-anneal procedure after the deposition of gate oxide with oxygen ambient under high temperature could result in much better reliability and performance. This improvement was mainly attributed to the reduction of the trap states in the gate oxide layer. Additionally, we used relatively low temperature and pressure to deposit a buffer Si layer, which had more oxygen inside, to derive a significant improvement in performance of the poly-Si channel of our proposed device. With this buffer layer, about 20 % improvement had shown in the field-effect mobility and the ON-state current, while the OFF- state current was less than half of the conventional poly-Si TFT. The deposition condition of the buffer Si layer must to be optimized to derive the optimized poly-Si channel. However, it might be tough to maintain the optimized condition during mass productions.

Then, negative bias temperature instability of p-channel LTPS TFTs was studied and compared with positive bias temperature instability of n-channel LTPS TFTs. We have proved that NBTI and PBTI are both important issues in the reliability of LTPS TFTs. The degradation of the threshold voltage, field-effect mobility and drive current of LTPS TFTs degrade after NBTI and PBTI stress were shown in our study. The device degradation caused by NBTI stress increases with temperature and electric field, indicating NBTI can be thermally and electrically activated. Due to the grain boundaries in the channel regions of LTPS TFTs, the grain boundaries trap state

generation must be considered during NBTI stress. However, the device degradation of LTPS TFTs during PBTI stress had negligible dependence on temperature. In this study, the mechanisms of NBTI and PBTI in LTPS TFTs were analyzed. The $|\Delta V_{th}|$ increases with the stress gate voltage. However, as the stress temperature increase, the $|\Delta V_{th}|$ increases under NBTI stress but almost unchanged under PBTI stress. Furthermore, the μ_{FE} is rarely changed under NBTI stress but increases under PBTI stress. From our analysis, the NBTI-degradation mechanism in p-channel LTPS TFTs is attributed to the diffusion-controlled electrochemical reactions, while the PBTI-degradation in n-channel LTPS TFTs is arisen from the charge trapping in the gate dielectric.

Finally, dynamic negative bias temperature instability of p-channel LTPS TFTs has been studied. We have proved NBTI is an important issue in the reliability of LTPS TFTs. However, trap states could be passivated when a zero or positive bias was applied to the gate electrode during NBS. From the experimental results, we concluded that under stress process of stress-passivation-stress test, the degradation was caused by the generation of fixed oxide charges, interface states and grain boundary trap states in LTPS TFTs, and these generated states resulted in the threshold voltage shift. Owing to the passivation of trap states, the device lifetime would be significantly underdetermined under conventional NBTS, which a static stress bias is applied. As a result, it is necessary to use dynamic NBTS to derive the appropriate device lifetime of p-MOS transistor used in CMOS inverter. In our study, we have shown several factors which might play a large part in DNBTS. We also found that either the degradation or the recovery mainly occurred near the SiO_2/Si interface near both the source and drain regimes. Moreover, we found that the degradation of device was strongly dependent on the frequency of the applied dynamic gate bias. Although static NBTS is a good method to determine the reliability

of p-channel LTPS TFTs, it is much better for LTPS TFTs used in inverters to be tested under particular dynamic bias condition, including bias frequencies and magnitudes to approach their real lifetime.

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