Chapter 1
Introduction

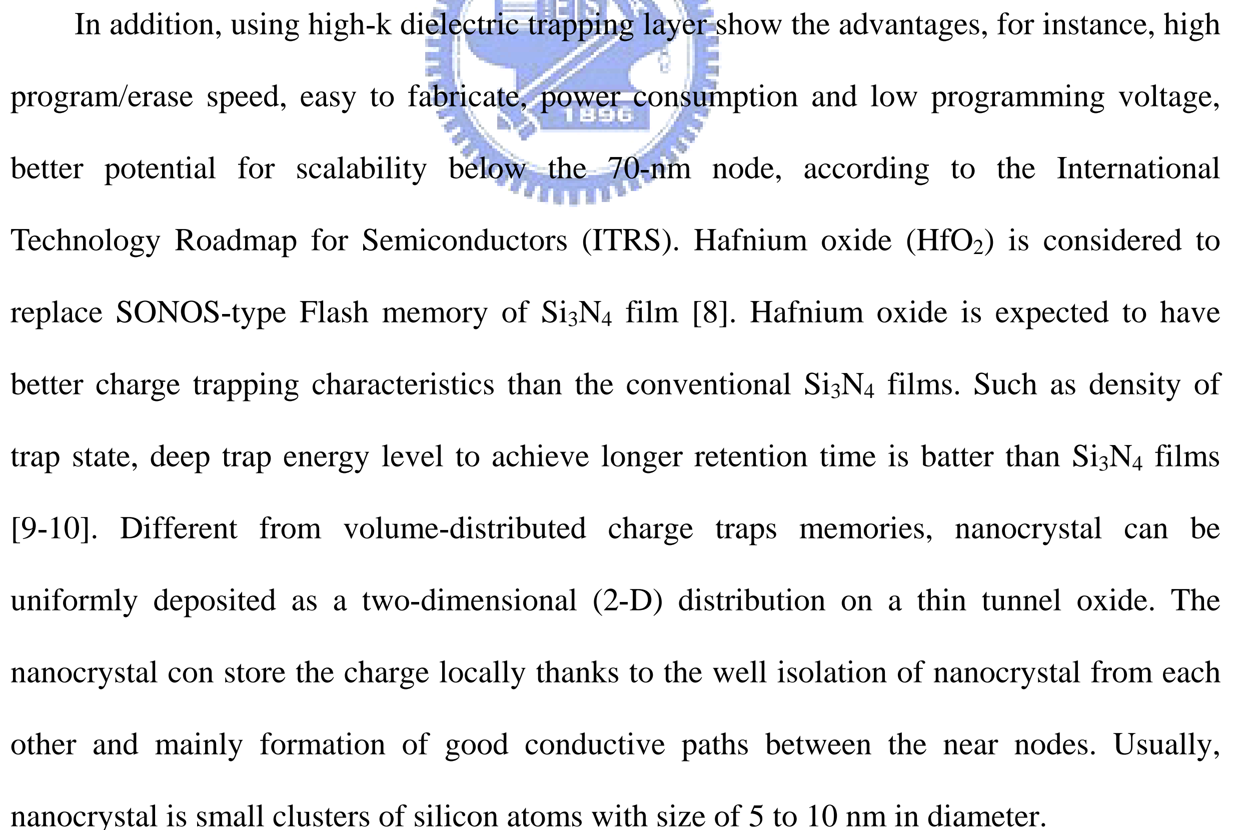
1.1 Overviews

Recently, memory technologies which driven by the more and more increasing demand for mobile capabilities, Personal Digital Assistant (PDA), computer, and some electric consumer products, have developed rapidly for the need in the people's subsistence. Memories can be divides into two main classes by whether the storage data can be affected by the power supply. One is volatile memory, and the other is non-volatile memory.

In 1967, D. Kahng and S. M. Sze invented the first floating-gate(FG) nonvolatile semiconductor memory at Bell Labs[1], nonvolatile memory device have been extensively used in integrated circuits such as the electrically alterable read-only memory(EAROM), the erasable-programmable read-only memory(EPROM), electrically erasable and programmable read-only memory(EEPROM),and the nonvolatile random-access memory(NVRAM), Flash memories have good ability of program/erase (P/E) operation, smaller area, and low cost. So far, the most far-flung nonvolatile memory array is the Flash memory. It has a byte-selectable programming operation joint with a sector erasing at the one time. Recently, the nonvolatile semiconductor memory devices play an important role in memory applications because of its low-voltage and low-power features for portable commercial devices.

The famous commercial Flash memory is Intel ETOX (EPROM Tunnel Oxide) structure [2]. The ETOX are "written" and "erase" by Channel-Hot-Electron programming and Folwler-Nordheim(FN) or Band to Band Hot Hole (BTBHH)[3],respectively. The threshold voltage (VT) shift between the programmed and erase states that it is call memory windows. With the semiconductor technology scale down to nano scale, the ultra-thin oxide quality has been improved. Such as polysilicon-oxide-nitride-oxide- silicon (SONOS)[4-5], and metal nitride oxide silicon (MNOS)[6]. The ONO (oxide-nitride-oxide) type gate dielectric stack

has been improved charge leakage through the control gate for ON (oxide-nitride) type. The electron injection to nitride layer (charge storage layer) method by FN-tunneling, directing tunnel and Frenkel-Poole emissions. Similarly, the trap electron inject to channel from nitride layer. When the control gate is to apply positively bias, electrons will tunnel from the channel thought the SiO_2 into the nitride layer. On the other part, when the control gate is to apply negatively bias, the trap electrons are ejected into the channel. In next generation nonvolatile memories, the SONOS-type Flash memories have attracted much attention for the application in electrical product. According to the International Technology Roadmap for Semiconductors (ITRS) [7], high-k dielectric materials would be able to maintain an equivalent potential difference form the floating gate to the device body for a larger thickness compared to SiO_2. The charge leakage of trap layer would be minimized and the scaling limits would be extended.



In addition, using high-k dielectric trapping layer show the advantages, for instance, high program/erase speed, easy to fabricate, power consumption and low programming voltage, better potential for scalability below the 70-nm node, according to the International Technology Roadmap for Semiconductors (ITRS). Hafnium oxide (HfO_2) is considered to replace SONOS-type Flash memory of Si_3N_4 film [8]. Hafnium oxide is expected to have better charge trapping characteristics than the conventional Si_3N_4 films. Such as density of trap state, deep trap energy level to achieve longer retention time is batter than Si_3N_4 films [9-10]. Different from volume-distributed charge traps memories, nanocrystal can be uniformly deposited as a two-dimensional (2-D) distribution on a thin tunnel oxide. The nanocrystal con store the charge locally thanks to the well isolation of nanocrystal from each other and mainly formation of good conductive paths between the near nodes. Usually, nanocrystal is small clusters of silicon atoms with size of 5 to 10 nm in diameter.

Due to its low voltage, low power and high speed programming features, p-channel flash memories [1-2] have been evolved as a promising cell for real applications in the future. In a

certain design of p-channel flash cells, programming of the cell can be achieved either by channel-hot-hole impact ionization induced channel-hot-electron injection (CHE) or by band-to-band (BTB) tunneling induced hot-electron injection at the drain side. Erasing of the cell can be accomplished by electron channel Fowler-Nordheim(F-N) ejection from the floating gate. Here, both Programming schemes, CHE and BTB, will generate the so-call oxide damages, which include the interface state Nit and the oxide trap charge Qox. In Steve S. Chung et. al.[3] paper, for the first time, a comparative study of p-channel flash memory performance and reliability have been presented in details for two different programming schemes. In Jao-Hsian Shiue et. al.[4] paper. The interface trap density (Dit) generated under these kinds of Fowler-Nordheim (FN) stress and Substrate-hot-hole stress. The injection of impact-ionization-generated hot holes is found to be the most important reason for interface trap generation under Vg<0 FN stress at high oxide field. The generated interface-trap density under Substrate-hot-hole stress increases with increasing gate oxide field. It is also found that the Substrate-hot-hole stress induces more interface traps than Substrate-hot-electron stress.

Instead of using N-channel cells, P-channel cells[5]-[13], known for the high injection efficiency and low programming drain current, are quite suitable for low-voltage and low-power applications. The developing trend of Flash memory has gone in the way of multi-level storages. The most important issue is to precisely control a tight threshold voltage distribution at different levels. To achieve tight threshold voltage distribution in multi-level Flash memory, the bit-by-bit verification which slows down the programming speed can be performed. The multi-level applications of P-channel Flash memory was first proposed in [14-15]. In this paper, the multi-level p-channel Flash memory cell by employed FN tunneling and CHEI operations simultaneously to achieve a Self-convergent programming process and used BBHE as an erase method. The multi-level p-channel Flash memory characteristics are also reported. Development, abundant reports [16]-[19] focused on providing self-convergent programming and erase in N-channel flash memory. Different programming mechanisms

were studied, such as channel-electron-induced-avalanche -hot-carrier (CHIA-HC) by Tamada et. al[16]. band-to-band-tunneling-induced-hot-electron by D.-P. Shum et al[17], punch-through-induced-hot-carrier and parasitic-bipolar-induced -hot-carrier by Chi et al.[18]. substrate-current-induced-hot-electron (SCIHE) injection by Hu et al.[19].

1.2 Motivation

The high density flash memories for stand-alone data storage application require device with device size minimizations. in the feature, with device size scale down, the high-k trapping layer of SONOS type structure can improved electrostatic control of the channeling region in lee et al. has reported high-k silicate materials. The high-k nanocrystal charge-trapping layer can be fabricated by annealing method, such as $HfSi_xO_y$. It is SiO_2 around the HfO_2 nanocrystal. In the charge storage state, it will be trapped in nanocrystal side or around nanocrystal, the storage charge isolated by silicon dioxides. Hence, less chance of charge loss is expected and a local defect of tunnel oxide will not cause a severe charge loss. The charge-trapping layers by nanocrystal structure improve on retention of nonvolatile memories. On account of above, we want to fabricate a device with HfO_2 nanocrystal as charge trapping layer. And the device show large memory windows, good program/erase speed, good retention, and good endurance.

1.3 Organization of the Thesis

In the follower section, we will show our research efforts. In chapter 2, the electrical characteristics and fabrication process of SiGe channel flash memory with HfO_2 trapping layer will be proposed. The experiment results reveal that the program/erase speed and endurance of our device have good performance. In chapter 3, the electrical characteristics and fabrication process of SiGe channel flash memory with HfO_2 nanocrystal trapping layer

will be proposed. The experiment results reveal that the program/erase speed and endurance of our device have good performance. In chapter 4, the electrical characteristics and fabrication process of P-channel SONOS-type memories by HfO_2 nanocrystal trapping layer will be proposed. The experiment results reveal that the program/erase speed, large memory window and retention of our device have good performance.

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