Chapter 2
Characteristics of HfO_2 Trap Layer Nonvolatile Flash Memory with SiGe Channel

2-1 Introduction

For advanced Si/SiGe device fabrication, in recent years, research into the growth of strained-layer superlattices has greatly simulated the development of heteroepitaxy because of the applications made possible using band-gap engineering. A low-temperature process is desirables for minimizing problems associated with lattice mismatch and inter diffusion. Molecular beam epitaxy is known as one of the most popular low-temperature epitaxial growth techniques, and that, due to its use of solid sources, this technique suffers from microclustering and compositional grading. In addition to MBE, other techniques, such as limited reaction process chemical vapor deposition and plasma enhanced CVD techniques, were also demonstrated to have the capability of growing high quality Si/SiGe film at low temperatures. On the other hand, ultrahigh vacuum/chemical vapor deposition techniques have significantly advanced the field of Si/SiGe film. In Ultra high vacuum chemical vapor deposition

(UHVCVD) SiH_4 and GeH_4 are the sources and the growth pressure is about 1mTorr. This technique is a chemical/molecular epitaxial process. The technique has advantages of a CVD process, such as simplicity, high purity, and high throughput [1]. Complementary metal-oxide-semiconductor (CMOS) technology requires a high drive current to increase circuit speed. Both the gate capacitance and carrier mobility can improve the drive current. In CMOS fabricating process, a primary consideration is the ability to form a high-quality gate dielectric. Oxides of SiGe alloys are generally a poor substitute for SiO_2 because of the

tendency for germanium to reject from the growing oxide resulting in a high interface state density [2].

The SONOS-type Flash memories have important operation for achieving high program/erase speed, low programming voltage, low power performance, large memory window, excellent retention, endurance, and disturbance characteristics [3-6]. Hafnium oxide (HfO_2) is considered to be a promising candidate for the charge trapping layer for SONOS-type Flash memory instead of Si_3N_4 film [7-8]. The high-k dielectric film HfO_2 is expected to have better charge trapping characteristics than the conventional Si_3N_4 films for sufficient density of trap states and deep trap energy level to achieve longer retention time [9].

In this work, we fabricate a high performance nonvolatile memory with a high-k charge-trapping layer. The high-k dielectric material is HfO_2. These materials provide high trapping state densities, therefore the charge-trapping efficiency can by improved and larger operation window can be achieved. The application of high-k materials can further reduce the operation voltage and potentially can help memory device scaling. It has good characteristics in terms of considerably large memory window, high speed program/erase, good endurance, good disturbance, and good retention.

2-2 Experimental

Figure 2-1 (a)-(g) schematically depicts the process flow of the proposed flash memory. The fabrication process of the HfO_2 memory devices involved the LOCOS isolation process on P-type, 5-10Ωcm, (100) 150mm silicon substrates. First, SiGe channel was grown by Ultra high vacuum chemical vapor deposition system (UHVCVD). After that, a 3-nm-thick tunnel silicon nitride (Si_3N_4) was chemical vapor deposition in horizontal furnace system. After that, the sample went through RTA treatment in O_2 ambient at 900 for 30 sec. The trapping layer of amorphous HfO_2 layer was deposited by E-gun Method with Hafnium (Hf) targets. After that, the samples went through RTA treatment in O_2 ambient at 900 for 1 minute. A blocking

oxide of about 10-nm-thick was then deposited by low pressure chemical vapor deposition system (LPCVD) for TEOS oxide. After that, the sample went through RTA treatment in O_2 ambient at 900 for 1 minute. Then, a 200-nm-thick poly-silicon was deposited to serve as the gate electrode by low pressure chemical vapor deposition system (LPCVD). then, gate electrode was patterned and the source/drain and gate were doped by self-aligned phosphorous ion implantation at the dosage and energy of 5×10^{15} ion/cm^{-2} and 20 KeV, then the substrate contact was patterned and the sub-contact was implanted with BF_2 at the dosage and energy of 5×10^{15} ions/cm^{-2} and 40 KeV. After these implantations, the dopes were activated at 900 for 30 sec. The rest of the subsequent standard CMOS procedures were complete for fabricating the HfO_2 high k memory devices.

2-3 Results and Discussions

2.3.1 Characteristics of flash devices

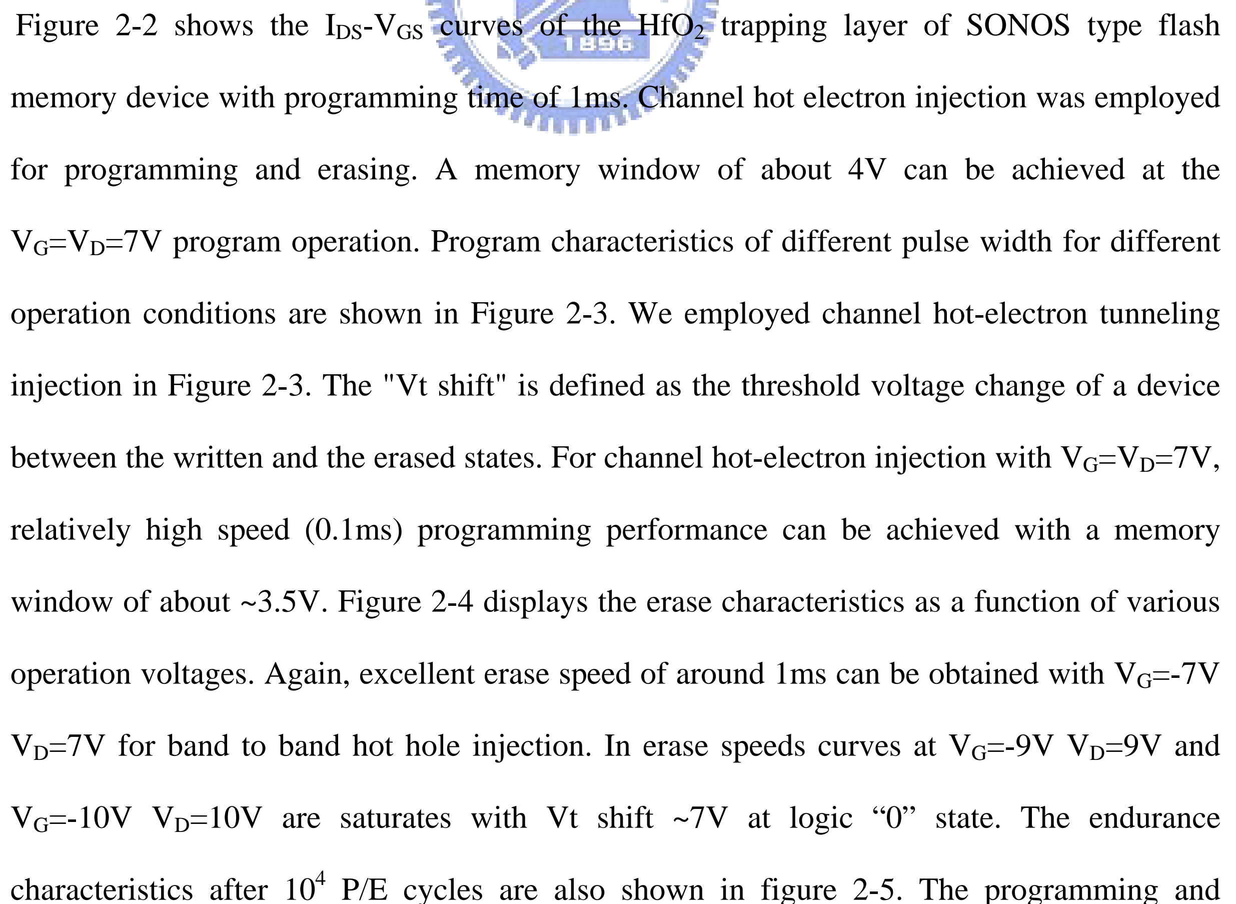


Figure 2-2 shows the I_{DS}-V_{GS} curves of the HfO_2 trapping layer of SONOS type flash memory device with programming time of 1ms. Channel hot electron injection was employed for programming and erasing. A memory window of about 4V can be achieved at the V_G=V_D=7V program operation. Program characteristics of different pulse width for different operation conditions are shown in Figure 2-3. We employed channel hot-electron tunneling injection in Figure 2-3. The "Vt shift" is defined as the threshold voltage change of a device between the written and the erased states. For channel hot-electron injection with V_G=V_D=7V, relatively high speed (0.1ms) programming performance can be achieved with a memory window of about ~3.5V. Figure 2-4 displays the erase characteristics as a function of various operation voltages. Again, excellent erase speed of around 1ms can be obtained with V_G=-7V V_D=7V for band to band hot hole injection. In erase speeds curves at V_G=-9V V_D=9V and V_G=-10V V_D=10V are saturates with Vt shift ~7V at logic “0” state. The endurance characteristics after 10^4 P/E cycles are also shown in figure 2-5. The programming and

erasing conditions are $V_G=V_D=7V$ for 0.1ms and $V_G=-10V$ $V_D=7V$ for 1ms, respectively. Slight memory window narrowing has been display and the individual threshold voltage shifts in program and erase states become visible after 100 cycles. The memory window is closed at 10000 cycles. This trend indicates the formation of operation-induced trapped electrons. Certainly, this is intimately related to the use of thick tunnel oxy-nitride and very minute amount of residual charges in the HfO_2 after cycling. The retention characteristics of the HfO_2 trapping layer memory device different tunnel layer thickness at room temperature (T=25℃) are illustrated in Figure 2-6. The thin oxy-nitride tunnel layer memory device retention time have charge loss at the start. The thick tunnel layer memory device charge loss with the retention time increasing. We guess is that some charge trapping at tunnel layer.

2.3.2 Disturbances

Drain disturbance may occur during programming for the cells sharing a common bit-line while one of the cells is being programmed and gate disturbance may occur during programming for the cells sharing a common word-line while one of the cells is being programmed as in Figure 2-7 (a)-(b). Three different drain voltages (V_D=2V, 3V and 4V) were applied in the programming drain disturbance measurements at room temperatures. Figure.2-8 Shown the programming drain disturbance of our HfO_2 trapping layer flash memory. We observed that a 0.3V drain disturb was observed after programming at a value of V_D of 2V under T=25℃ and after stressing for 1000 seconds. Figure 2-9 Show the gate disturbance characteristics in the programming state. Gate disturbance may occur during programming for the cells sharing a common word-line while one of the cells is being programmed. We observed a threshold voltage shift of <0.1V under the following conditions: $V_G=10V$, $V_S=V_D=V_{Sub}=0V$; stressed for 1000 seconds. The good drain disturbance and gate disturbance was due to optimized process, such as thinner blocking oxide and tunneling oxy-nitride.

2-4 Summary

In this chapter, we propose a novel, sample, low process temperature, reproducible and reliable technique for the design of HfO_2 trapping memory cells. It has good characteristics in terms of large memory window, high speed program /erase, good retention time.

Reference

[1] T.C. Chang "characterization of Si/SiGe strained-layer superlattices grown by an ultrahigh vacuum/chemical vapor deposition technique". *JJAP* vol.33 (1994) pp.1787-1792

[2] Robert J. P. Lander, Youri V. Ponomarev, Jurgen G. M. van Berkum, and Wiebe B. de Boer, "High Hole Mobilities in Fully-Strained Si1xGex Layers (0:3 < x < 0:4) and their Significance for SiGe PMOSFET Performance" *IEEE Transactions on Electron Devices*, VOL. 48, NO. 8, August 2001

[3] T. S. Chen, K. H. Wu, H. Chung, and C. H. Kao, "performance improvement of SONOS memory by bandgap engineer of charge-trapping layer", *IEEE Electron Device Lett*., vol.25, no.4, pp. 205-207, Apr. 2002.

[4] Marvin H. White, Yang (Larry) Yang, Ansha Purwar, Margaret L. French，" A Low Voltage SONOS Nonvolatile Semiconductor Memory Technology ", *IEEE transactions on components, packaging, and manufacturing technology*—PART A, VOL. 20, NO. 2, JUNE 1997.

[5] Shin-ichi Minami and Yoshiaki Kamigaki," A Novel MONOS Nonvolatile Memory Device Ensuring 10-Year Data Retention after 107 Erase/Write Cycles ", *IEEE Transactions on Electron Devices*, VOL. 40, NO. 11, NOVEMBER 1993.

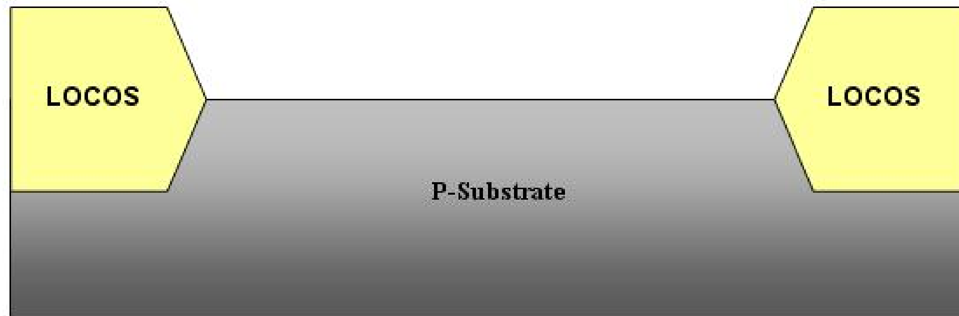
[6] Chih-Chieh Yeh, TahuiWang,Wen-Jer Tsai, Tao-Cheng Lu, Ming-Shiang Chen, Yi-Ying Liao, Wenchi Ting, Yen-Hui Joseph Ku, and Chih-Yuan Lu," A Novel PHINES Flash Memory Cell with Low Power Program/Erase, Small Pitch, Two-Bits-Per-Cell for Data Storage Applications" *IEEE Transactions on Electron Devices*, VOL. 52, NO. 4, APRIL 2005

[7] T. Sugizaki, M. Kohayashi, M. Ishidao, H. Minakata, M. Yamaguchi, Y. Tamura, Y. Sugiyama, T. Nakanishi, and H. Tanaka," Novel Multi-bit SONOS Type Flash Memory Using a Highk Charge Trapping Layer", *Symposium on VLSl Technology Digest of*

Technical Papers 2003.

[8] Marvin H. White, Dennis A. Adams, James R. Murray, StephenWrazien, Yijie (Sandy) Zhao, Yu (Richard) Wang, Bilal Khan, Wayne Miller, Rajiv Mehrotra1 ，” Characterization of Scaled SONOS EEPROM Memory Devices for Space and Military Systems* ”, *IEEE* 2004

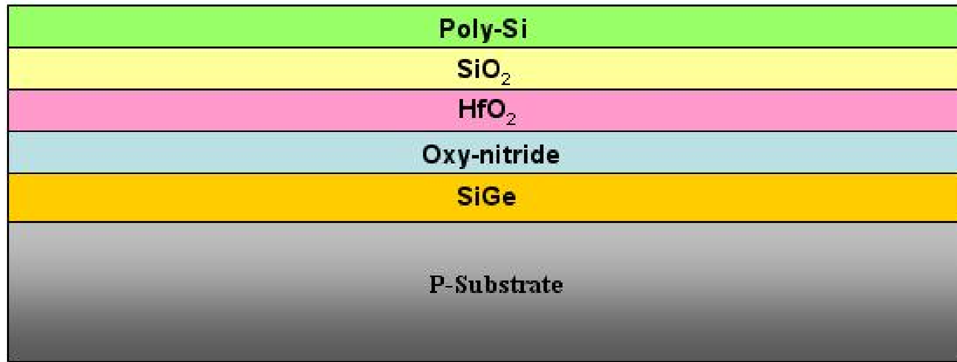
[9] G. D. Wilk, R. M. Wallace, J. M. Anthony, ”High-k gate dielectrics: Current status and materials properties considerations ”, *Applied Physics Review*, vol.89, no.10,pp.5243-5275, Nay 2001.



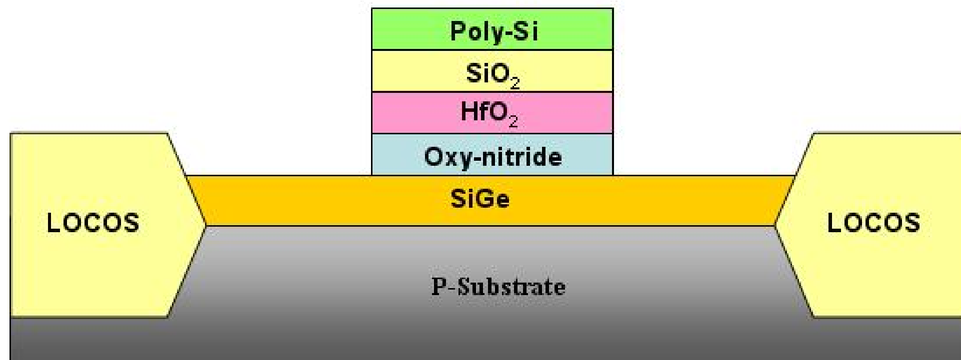
(a)

(b)

Figure 2-1. Schematically depicts the process flow of the HfO_2 flash memory cell structure.

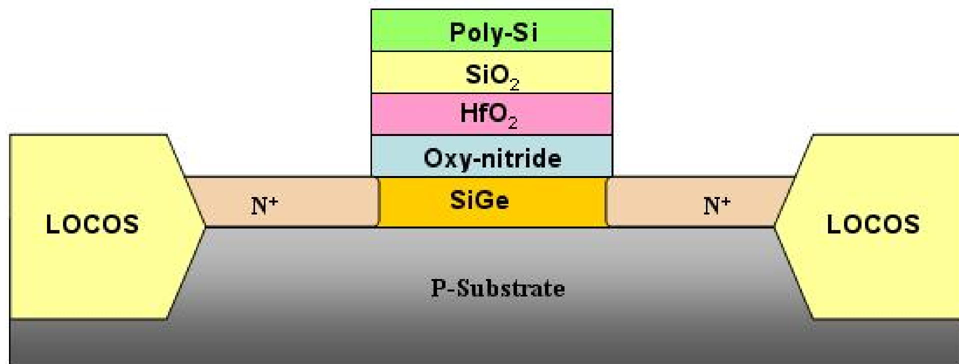


(c)

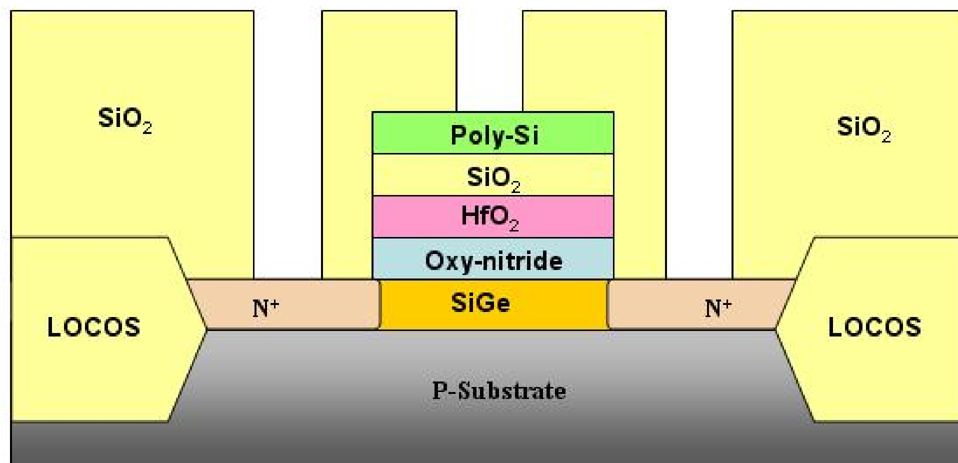


(d)

Figure 2-1. Schematically depicts the process flow of the HfO_2 flash memory cell structure.

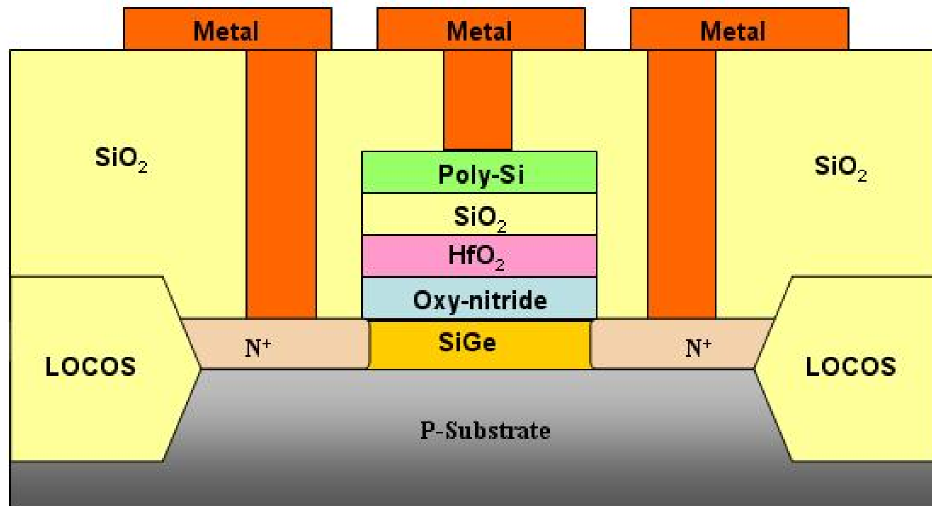


(e)



(f)

Figure 2-1. Schematically depicts the process flow of the HfO_2 flash memory cell structure.



(g)

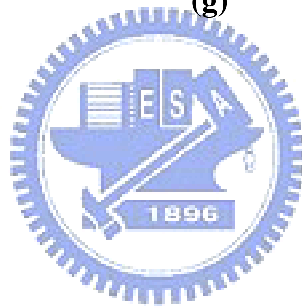


Figure 2-1. Schematically depicts the process flow of the HfO_2 flash memory cell structure.

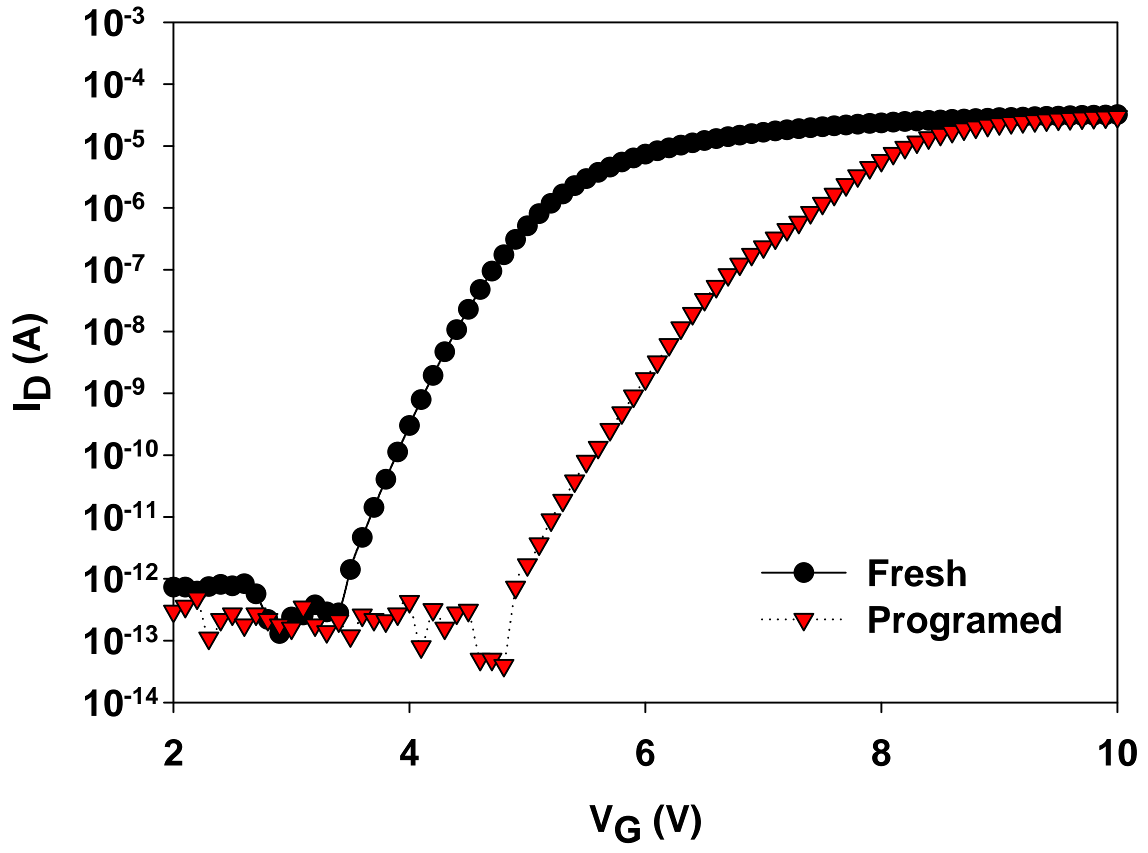


Figure 2-2. I_{DS}-V_{GS} of the HfO_2 flash memory cell structure.

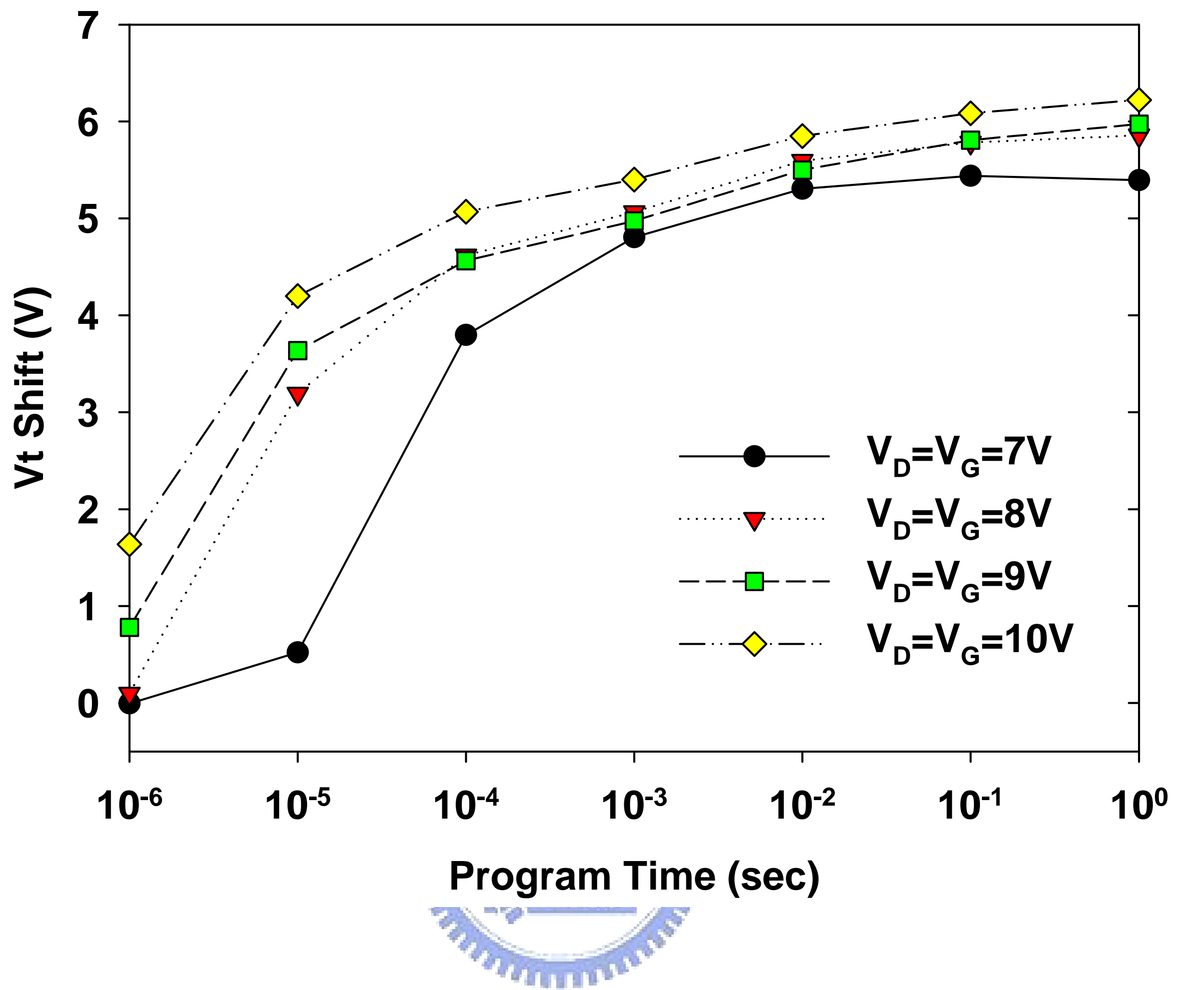


Figure2-3. Program characteristics of HfO_2 flash memory device with different programming conditions.

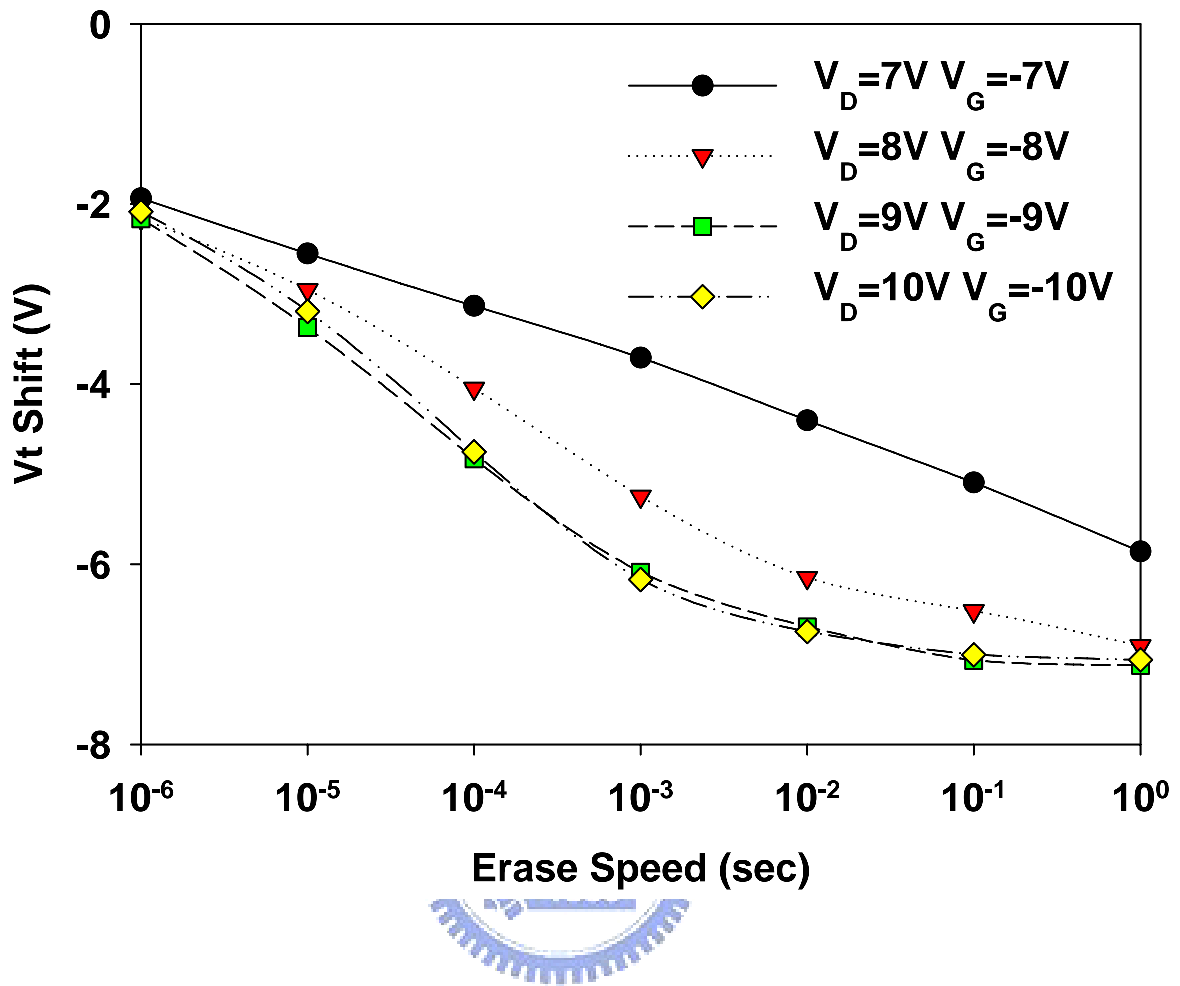


Figure 2-4. Erase characteristics of HfO_2 flash memory device with different erasing conditions.

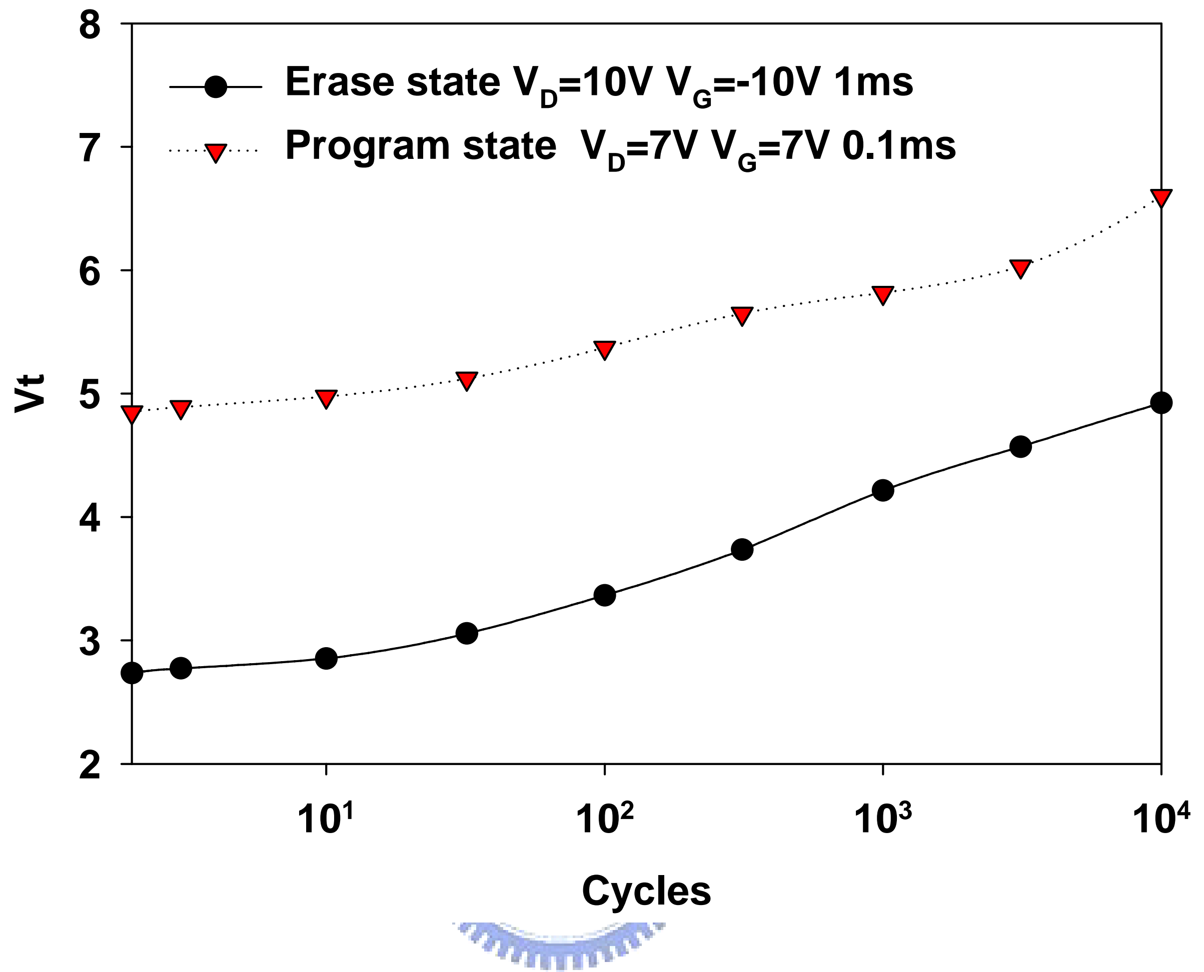
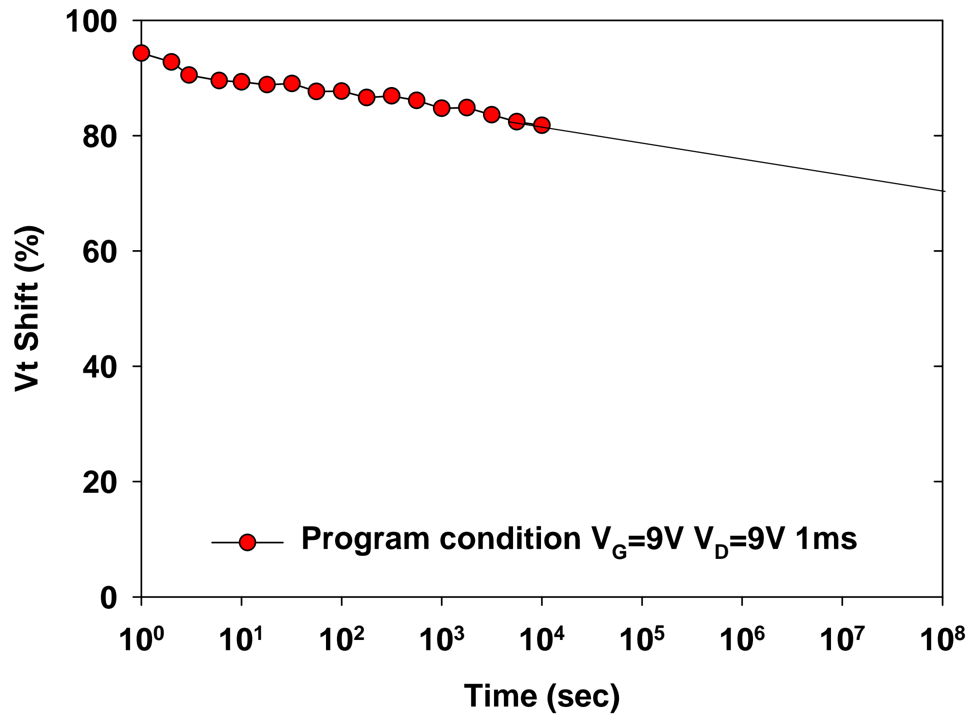
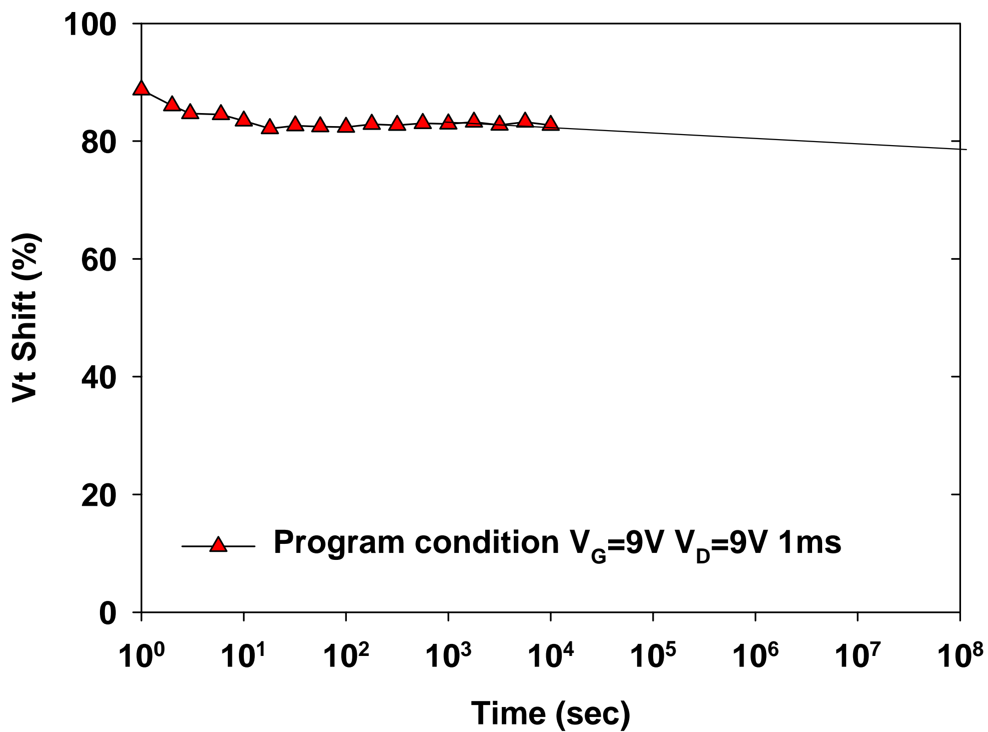


Figure2-5. Endurance characteristic of HfO_2 flash memory device.

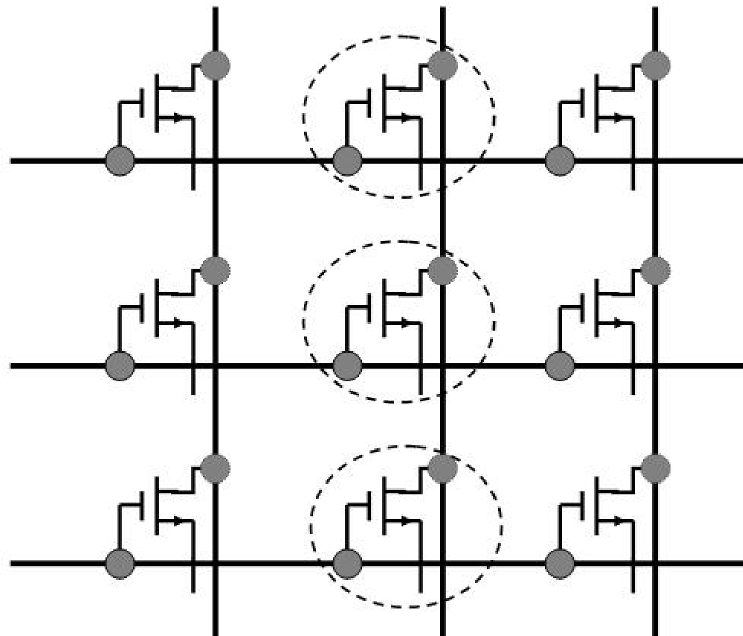


(a)Thick Tunnel Layer

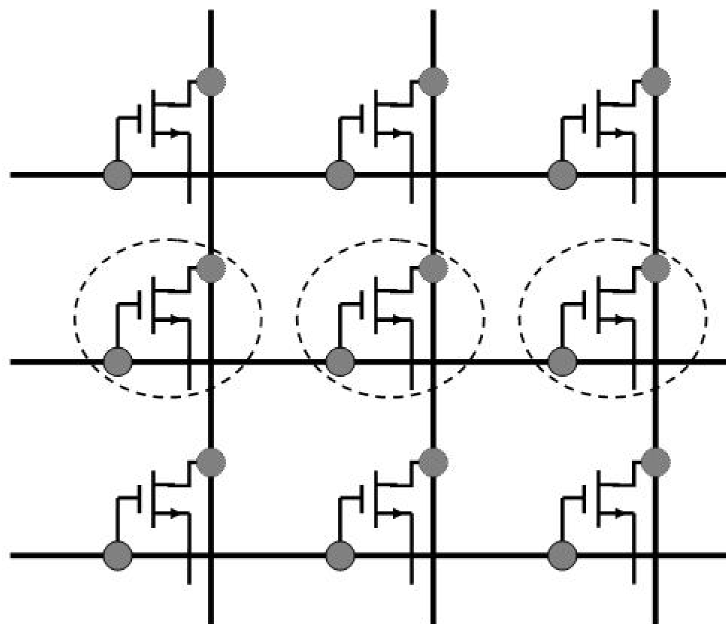


(b)Thin Tunnel Layer

Figure 2-6. Retention characteristics of HfO_2 flash memory devices at T=25 ℃ with different tunnel layer thickness.



(a) Drain disturbance characteristics of memory cells.



(b) Gate disturbance characteristics of memory cells.

Figure 2-7. Disturbances characteristics of memory cells

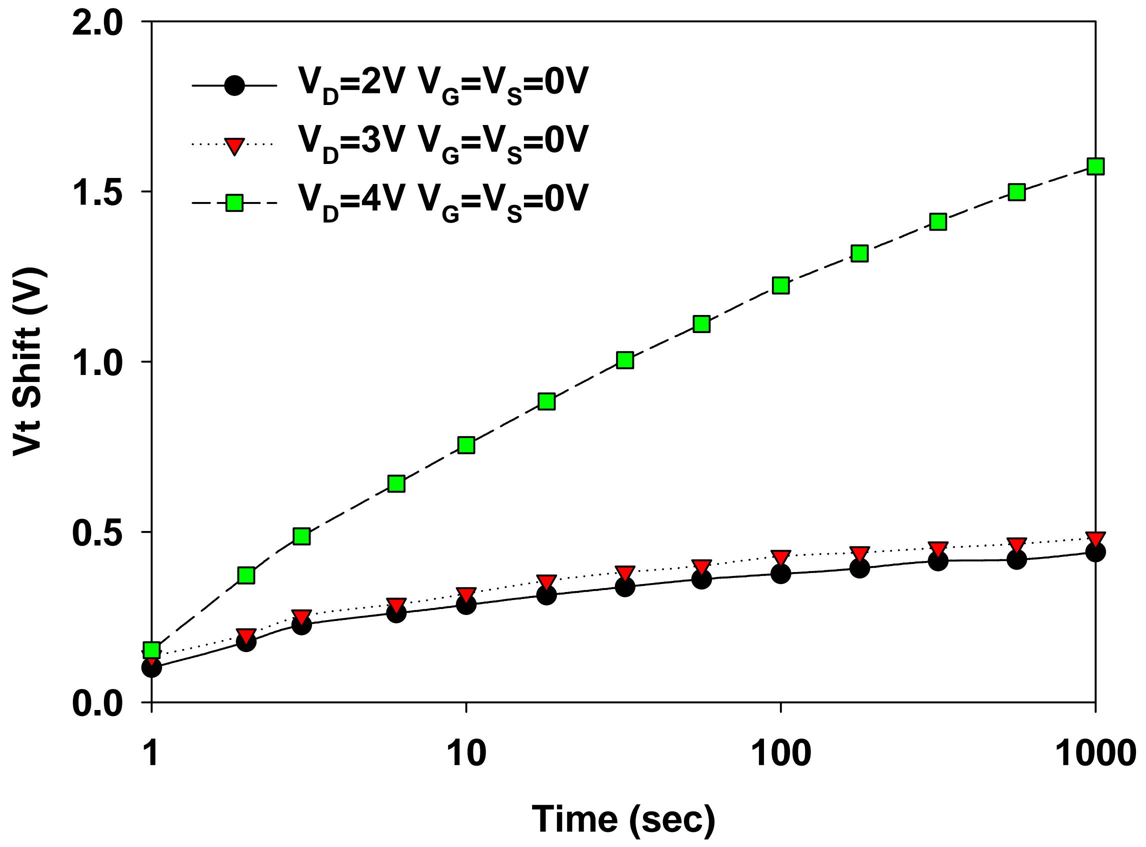


Figure 2-8. Drain disturbance characteristics of the HfO_2 flash memory cells.

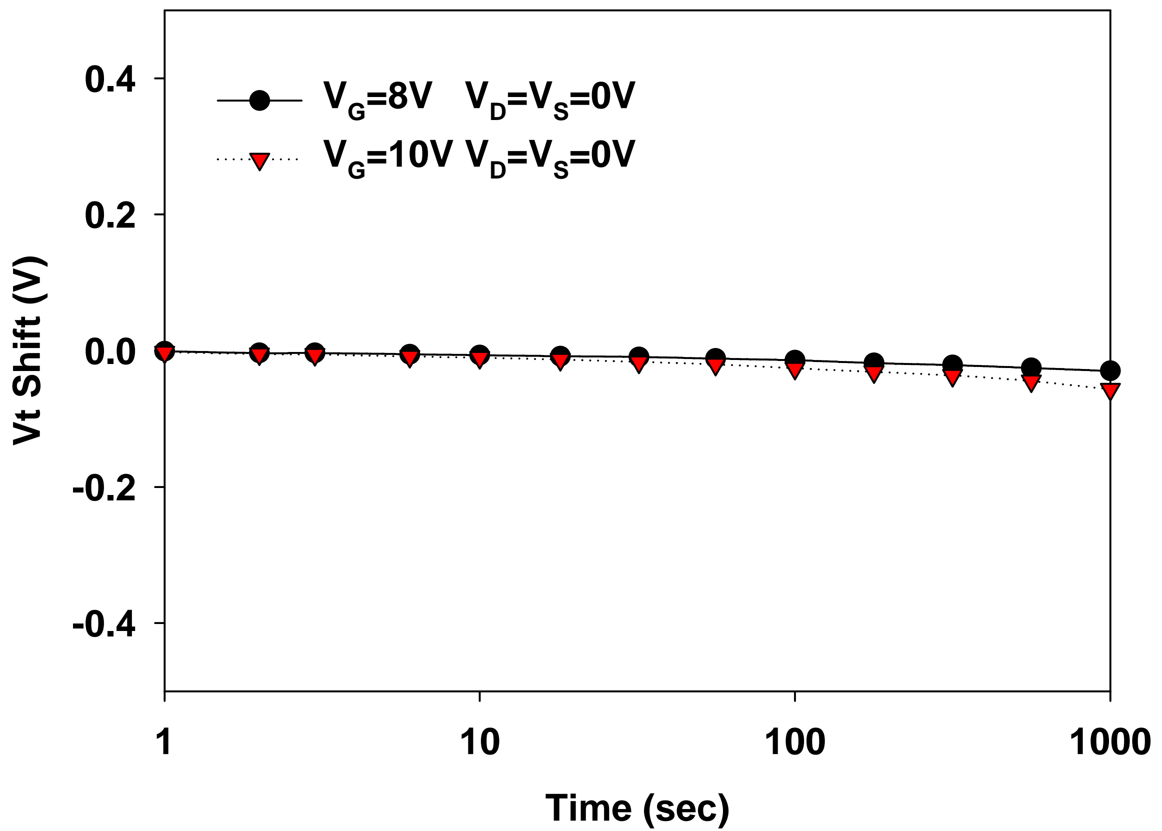


Figure 2-9. Gate disturbance characteristics of the HfO_2 flash memory cells.