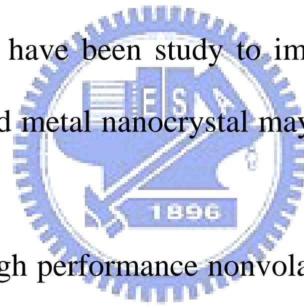
Chapter 3
Characteristics of HfO_2 Nanocrystal Nonvolatile Flash Memory with SiGe Channel

3.1 Introduction

Poly-Si/Oxide/Nitride/Oxide–Silicon (SONOS)-type structure memories, which include nitride and nanocrystal memories, have recently attracted much attention for their application in the next-generation nonvolatile memories [1]–[10]. Alternatively, conventional floating gate Flash memories adopt the multilevel-cell concept to increase its density based on the same process technology [11-14]. In recent years, change ONO processing technology and choice trapping layer material have been study to improve the cell data retention. Such as high-k, silicon, germanium, and metal nanocrystal may by used to provide charge storage for nonvolatile memories.



In this work, we fabricate a high performance nonvolatile memory with a high-k nanocrystal charge-trapping layer. The nanocrystal material is HfO_2. This high-k nanocrystal was replaces the continuous high-k layer in the SOHOS structure. These nanocrystal provide high trapping state densities and deep trapping levels, therefore they can enhance the retention of nonvolatile memories. The larger operation window can be improved, and charge-trapping efficiency can be improved. The application of nanocrystal materials can further reduce the operation voltage and potentially can help memory device scaling. It has good characteristics in terms of considerably high speed program/erase, large memory windows, good retention time, good endurance, good disturbance, and good retention.

3.2 Experimental

Figure 3-1(a)-(g) schematically depicts the process flow of the proposed flash memory. The

fabrication process of the HfO_2 nanocrystal memory devices involved the LOCOS isolation process on a P-type, 5-10Ωcm, (100) 150mm silicon substrates. First, SiGe channel was grown by Ultra High Vacuum Chemical Vapor Deposition system (UHVCVD). After that, a 3-nm-thick tunnel silicon nitride was chemical vapor deposition in horizontal furnace system. After that, the sample went through RTA treatment in O_2 ambient at 900 for 30 sec. The trapping layer of amorphous HfSiOx silicate layer was deposited by co-sputtering method with pure Hafnium (99.9% pure) and pure Silicon in the Oxygen and argon gas ambient. After that, the samples went through RTA treatment in O_2 ambient at 900 for 1 minute. A blocking oxide of about 10-nm-thick was then deposited by LPCVD for TEOS oxide. After that after that, the sample went through RTA treatment in O_2 ambient at 900 for 1 minute. Then, a 200-nm-thick poly-silicon was deposited to serve as the gate electrode by LPCVD. then, gate electrode was patterned and the source/drain and gate were doped by self-aligned phosphorous ion implantation at the dosage and energy of 5×10^{15} ion/cm^{-2} and 20 Kev, then the substrate contact was patterned and the sub-contact was implanted with BF_2 at the dosage and energy of 5×10^{15} ions/cm^{-2} and 40 Kev. After these implantations, the dopes were activated at 900 for 30 sec. The rest of the subsequent standard CMOS procedures were complete for fabricating the HfO_2 high k memory devices.

3.3 Results and Discussions

3.3.1 Characteristics of flash devices

Figure 3-2 shows the I_{DS}-V_{GS} curves of the HfO_2 trapping layer of SONOS type flash memory device with programming time of 0.1ms. Channel hot electron injection was employed for programming and erasing. A memory window of about 3V can be achieved at the V_G=9V，V_D=9V program operation. Program characteristics of different pulse width for different operation conditions are shown in Figure 3-3. We employed channel hot-electron tunneling injection in figure 3-3. The "Vt shift" is defined as the threshold voltage change of a

device between the written and the erased states. For channel hot-electron injection with V_G=9V V_D=9V, relatively high speed (0.1ms) programming performance can be achieved with a memory window of about 3V. The SiGe channel device is batter than Si channel device in program/erase operation. Figure 3-4 displays the erase characteristics as a function of various operation voltages. Again, excellent erase speed of around 1ms can be obtained with V_G=-9V V_D=9V for band to band hot hole injection. The endurance characteristics after 10^4 P/E cycles are also shown in figure 3-5 with different thickness oxy-nitride tunnel layer. The programming and erasing conditions are V_G=5V V_D=9V for 0.1ms and V_G=-5V V_D=9V for 1ms, respectively. Slight memory window narrowing has been display and the individual threshold voltage shifts in program and erase states become visible after 1000 cycles. This trend indicates the formation of operation-induced trapped electrons. Certainly, this is intimately related to the use of thick tunnel oxy-nitride and very minute amount of residual charges in the HfO_2 after cycling. The retention characteristics of the HfO_2 trapping layer memory device at room temperature (T=25℃) and higher temperature (T=85℃) are illustrated in Figure 3-6. The retention time can be up to 10^8 seconds for 80% charge loss at room temperature. And that retention time can be up to 10^8 seconds for 40-50% charge loss for the 85℃ conditions and after 10000 cycles P/E.

3.3.2 Characteristics of 2-bit operation

Figure 3-7 demonstrates the feasibility of performing two-bit operation with our HfO_2 trapping layer memories through forward and reverse read scheme in single cell. From the I_{DS}-V_{GS} curves, it is clear that we could employ forward and reverse reads to detect the information stored in the programmed bit 1 and bit 2, respectively. Table 2-1 summarizes the bias conditions for two-bit operation.

3.3.3 Disturbances

Figure 3-8 Shown the programming drain disturbance of our HfO_2 nanocrystal trapping layer flash memory. Drain disturbance may occur during programming for the cells sharing a

common bit-line while one of the cells is being programmed and Three different drain voltages (V_D=2V, 3V, 4V) were applied in the programming drain disturbance measurements at room temperatures. We observed that a 0.3V drain disturb was observed after programming at a value of V_D of 3V under T=25℃ and after stressing for 1000 seconds. Figure 3-9 show the gate disturbance characteristics in the erasing state. Gate disturbance may occur during programming for the cells sharing a common word-line while one of the cells is being programmed. We observed a threshold voltage shift of -0.18V under the following conditions: V_G=10V, V_S=V_D=V_{Sub}=0V; stressed for 1000 seconds. The good drain disturbance and gate disturbance was due to optimized process, such as thinner blocking oxide and tunneling oxy-nitride. Finality, for 2-bit operation we shown read disturbance characteristics in figure 3-10. The nanocrystal trapping device read-disturb characteristic with different drain voltage. The applied bit-line voltage in a reverse-read scheme must be sufficiently large (>2V) to be able to read through the trapped charge in the neighboring bit. The results demonstrate clearly that almost no read disturbance occurred in our memory device under reading condition of V_G=3V and V_D=2V.

3.4 Summary

In this chapter, we have proposed a novel, sample, low process temperature, reproducible, reliable technique for high density HfO_2 nanocrystal memory. It has good characteristics in terms of large memory window, high speed program/erase, good retention, endurance and 2 bit operation.

Reference

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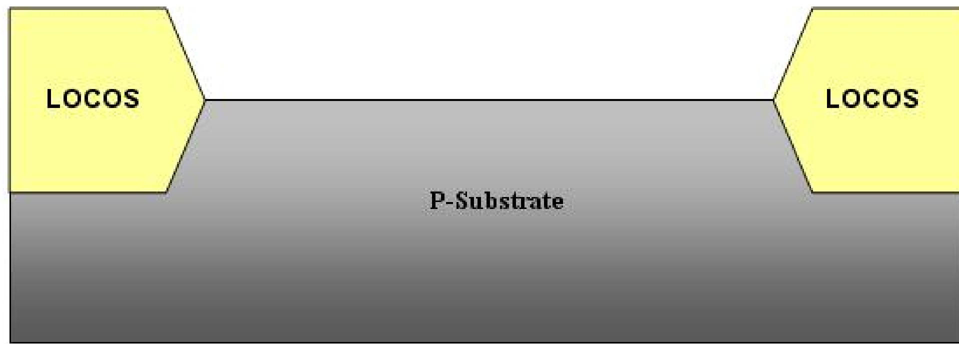
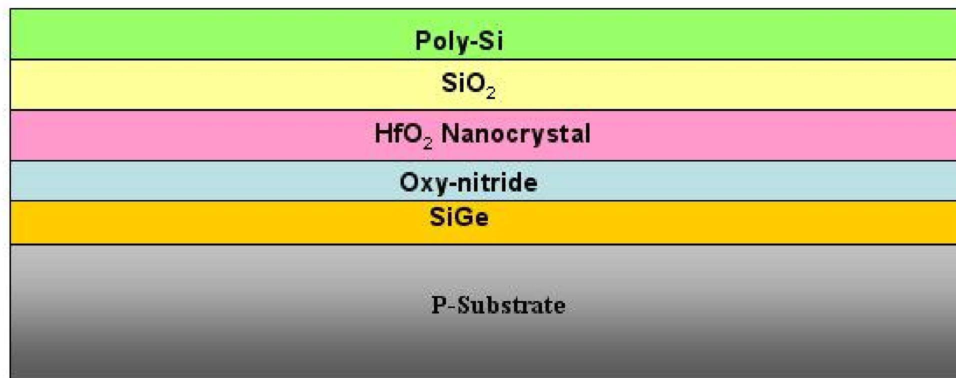


(a)

(b)

Figure 3-1. Schematically depicts the process flow.



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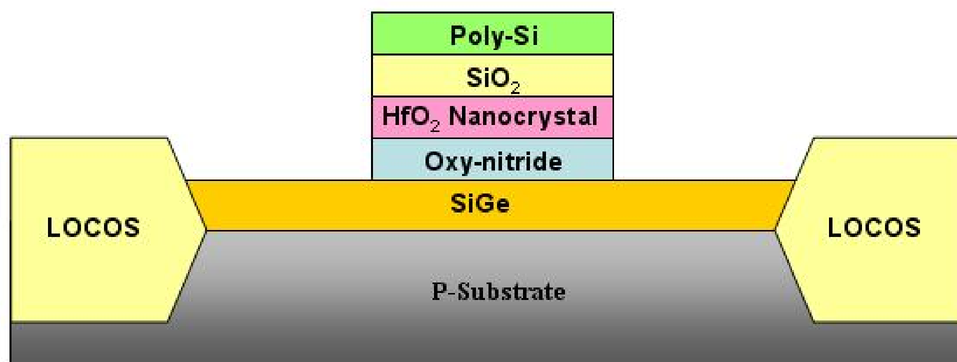
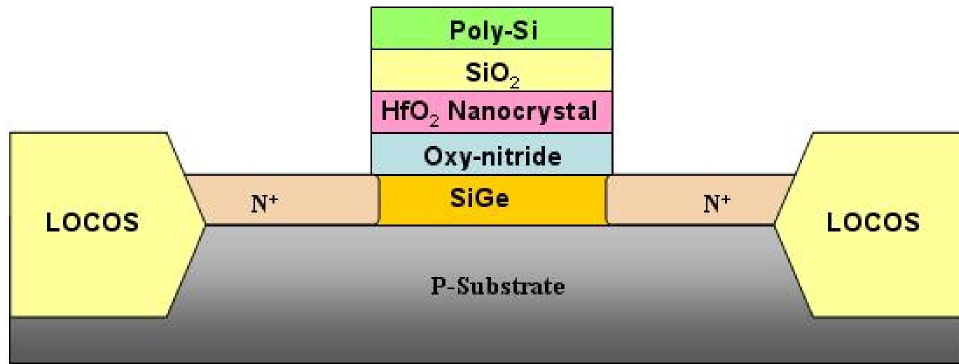


(d)

Figure 3-1. Schematically depicts the process flow.



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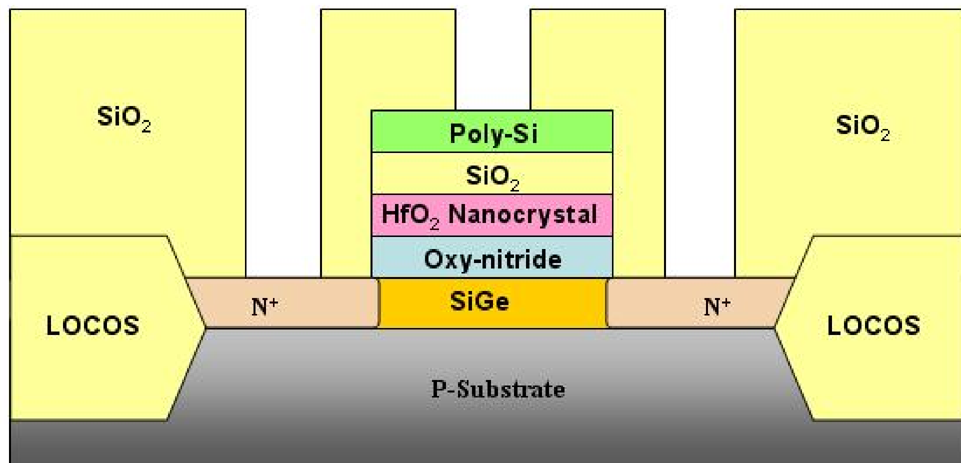
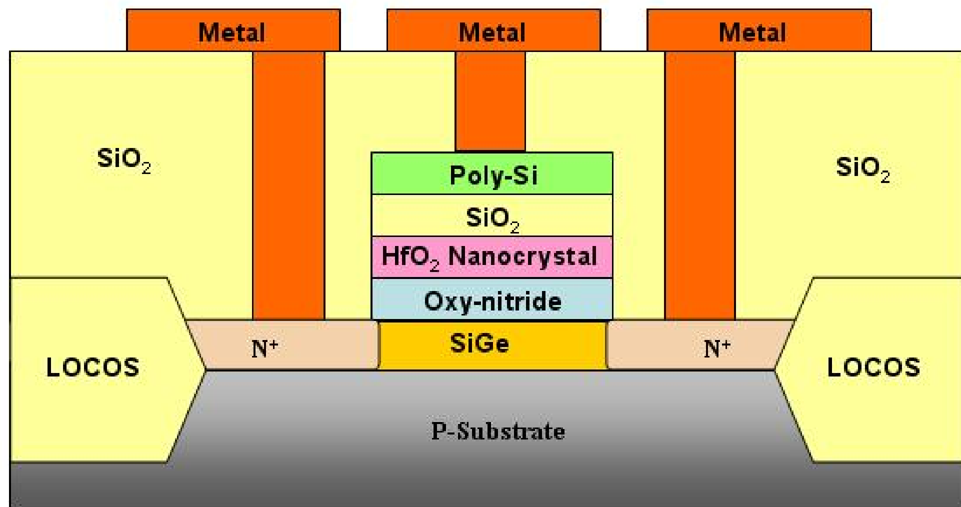


(f)

Figure 3-1. Schematically depicts the process flow.



(g)

Figure 3-1. Schematically depicts the process flow.

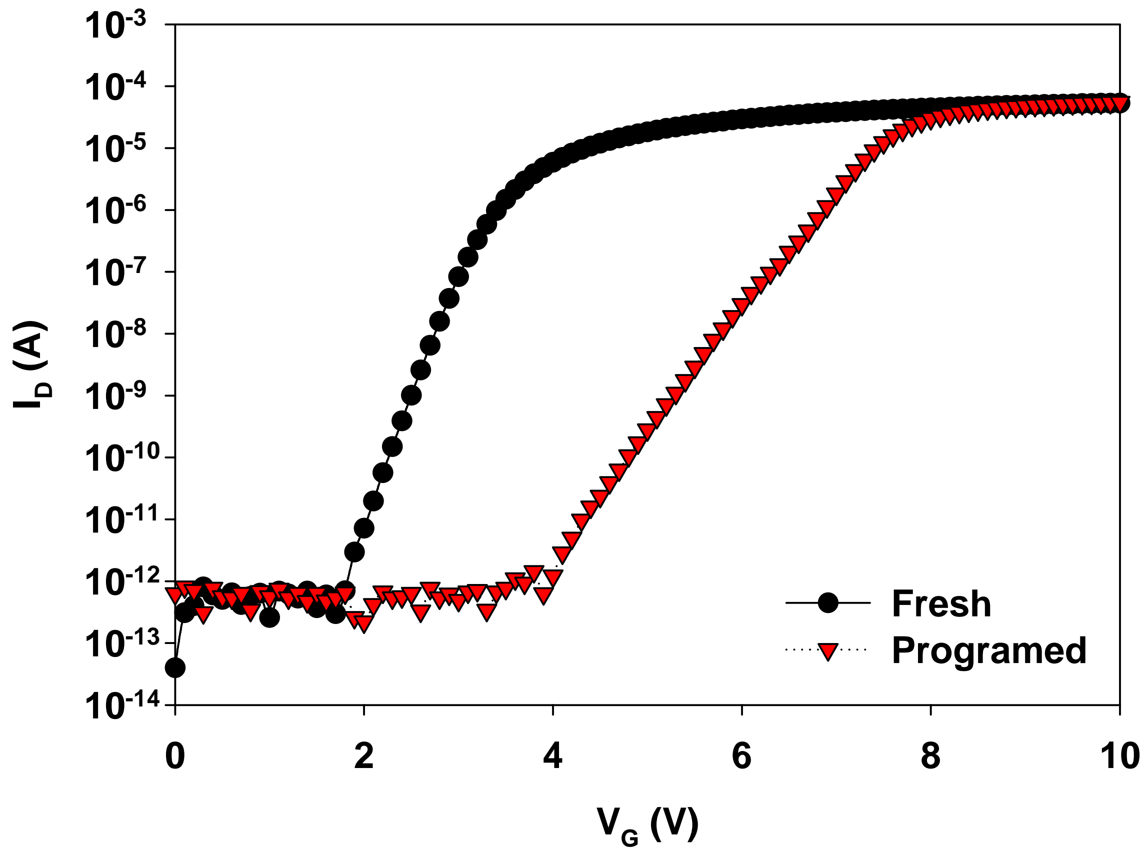


Figure 3-2. I_{DS}-V_{GS} characteristic of HfO_2 nanocrystal memory device.

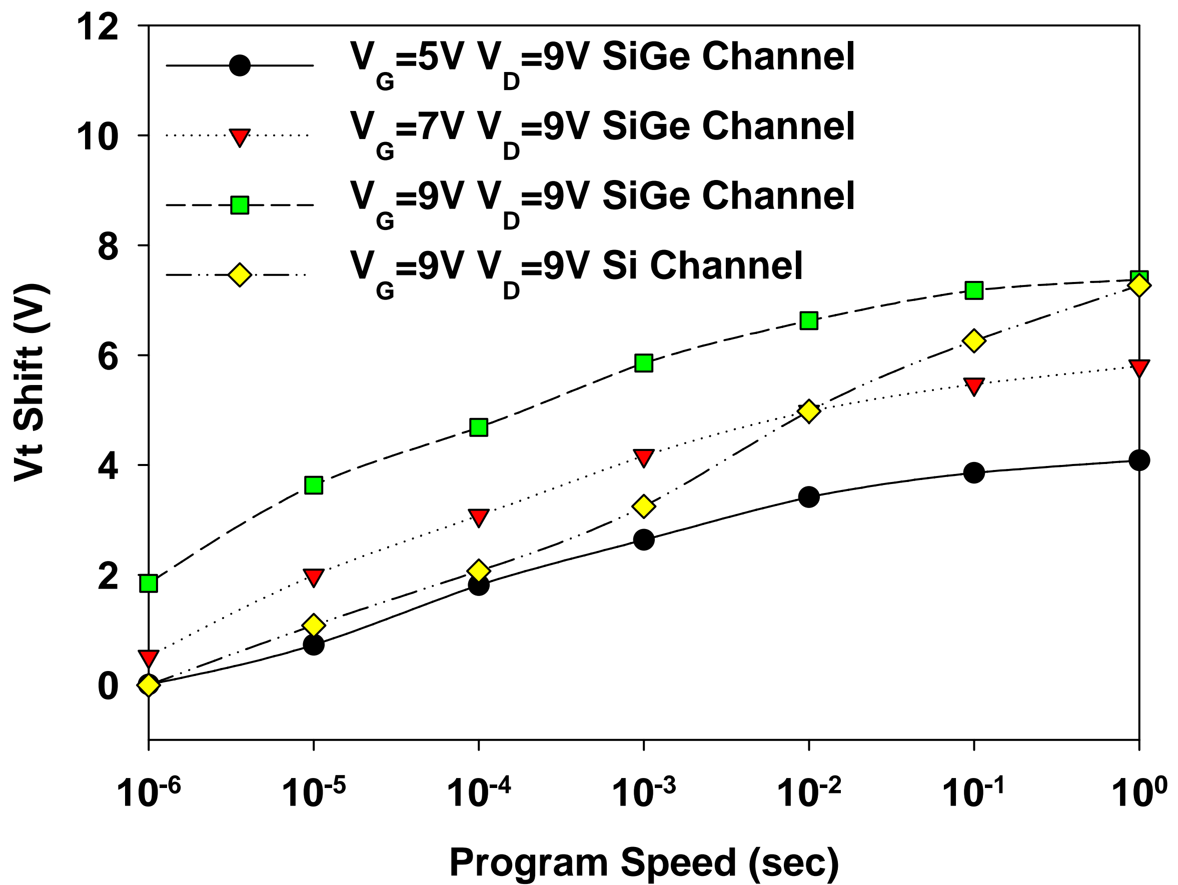


Figure 3-3. Program characteristics of HfO_2 nanocrystal memory device with different programming conditions.

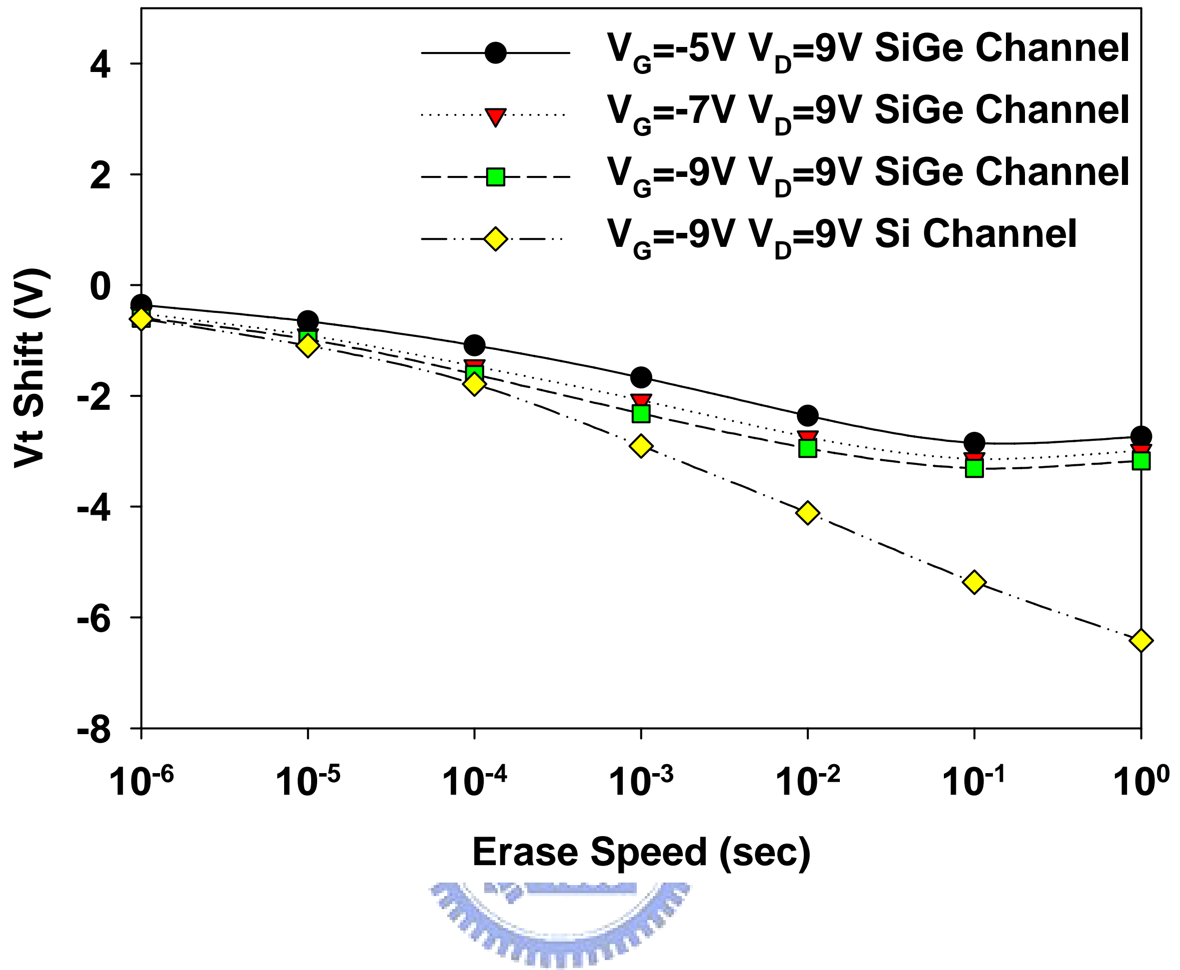
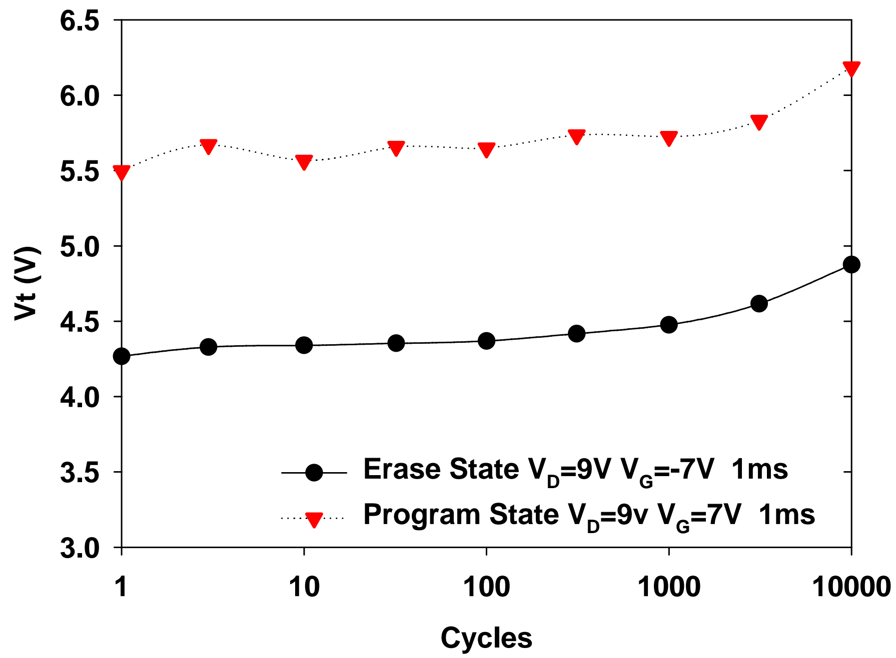
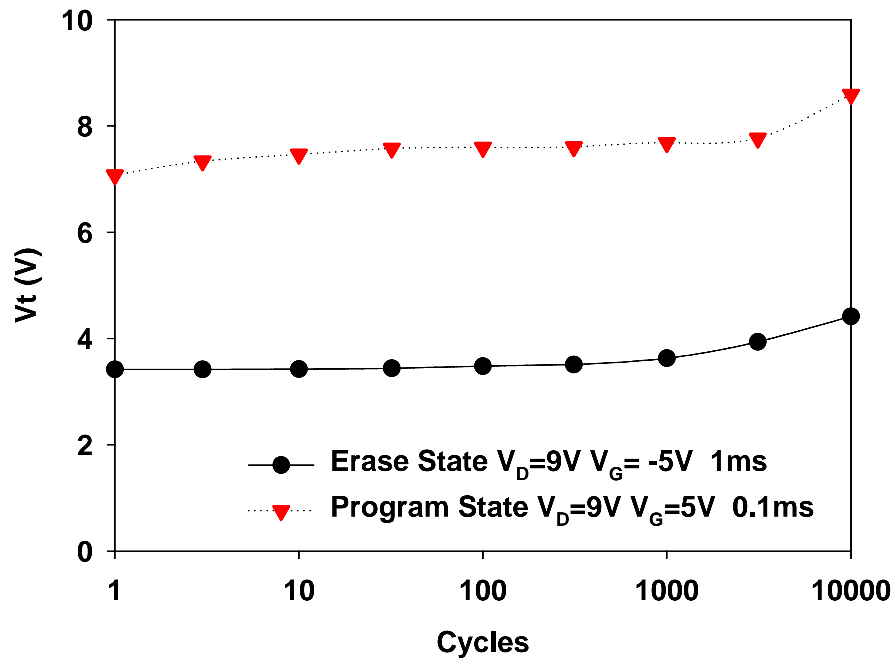


Figure 3-4. Erase characteristics of HfO_2 nanocrystal memory device with different erasing conditions.



(a) Thick Tunnel Layer



(a) Thin Tunnel Layer

Figure 3-5. Endurances characteristics of HfO_2 nanocrystal memory device with different tunneling layers.

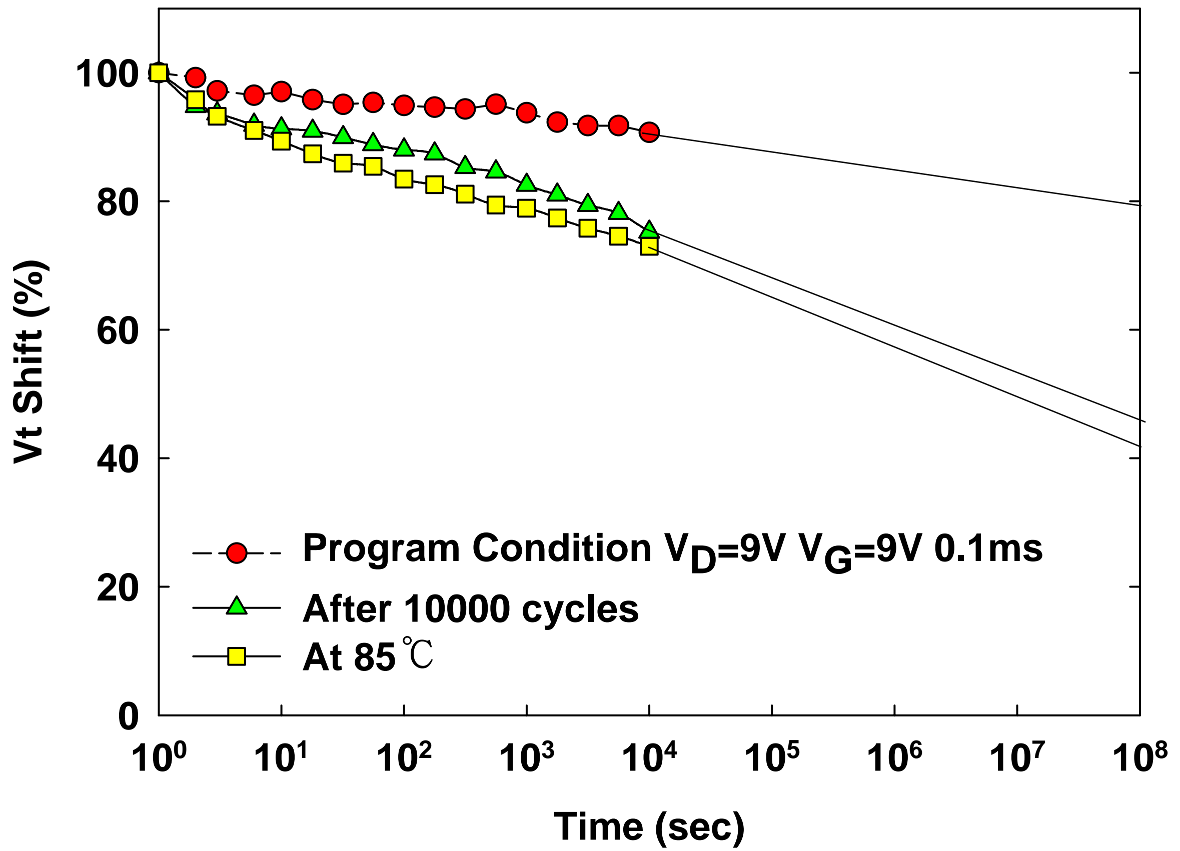


Figure 3-6. Retention characteristics of HfO_2 nanocrystal memory devices at T=25℃, 85℃ and after 10000 cycles.

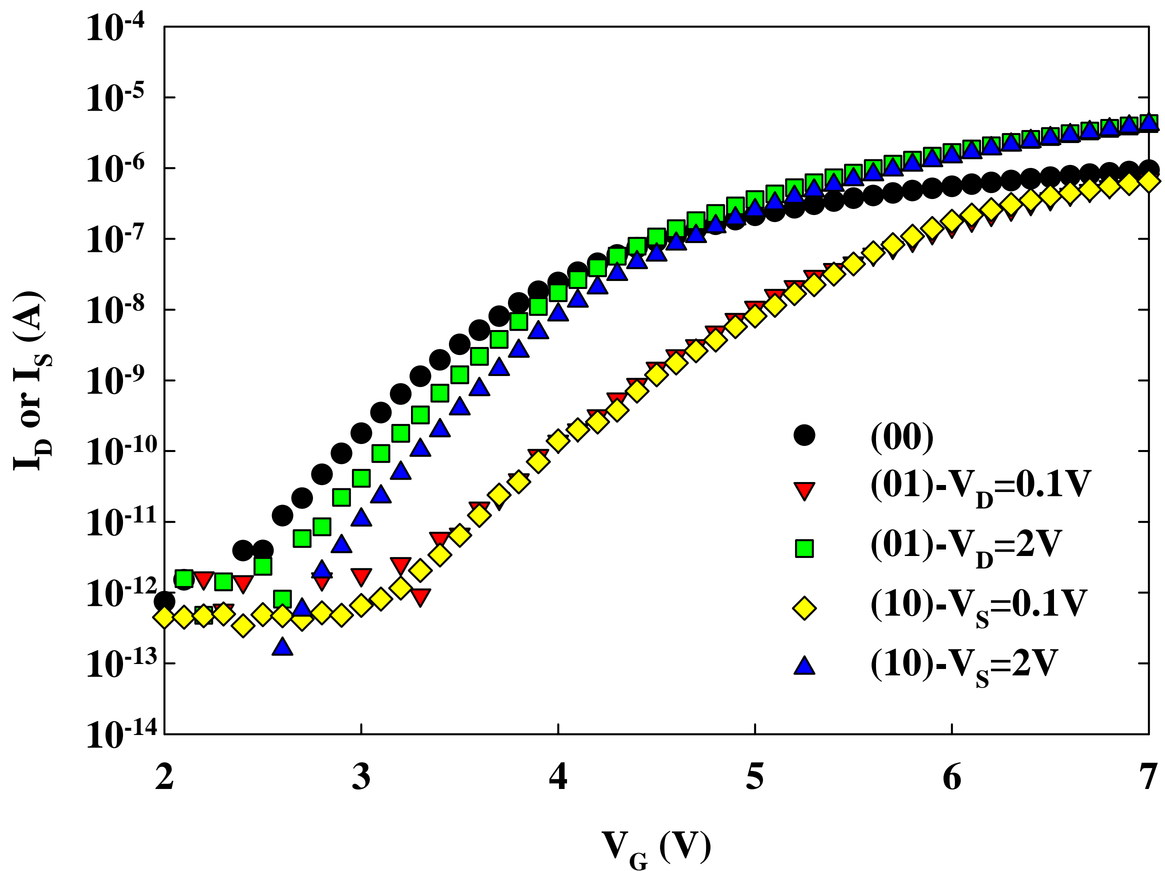


Figure 3-7. I_{DS}-V_{GS} curves of the two-bit memory in a cell; forward read and reverse read for programmed bit1 and programmed bit2.

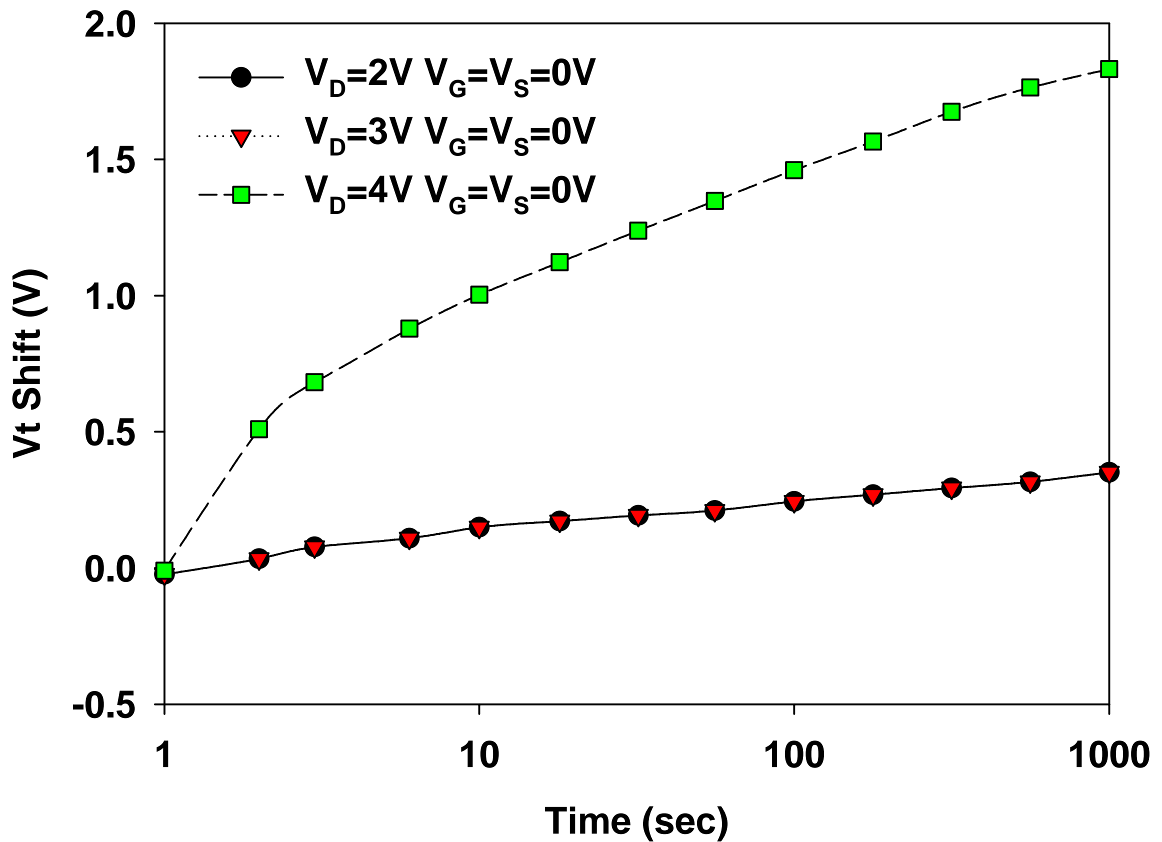


Figure 3-8. Drain disturbance characteristics of the HfO_2 nanocrystal memory cells.

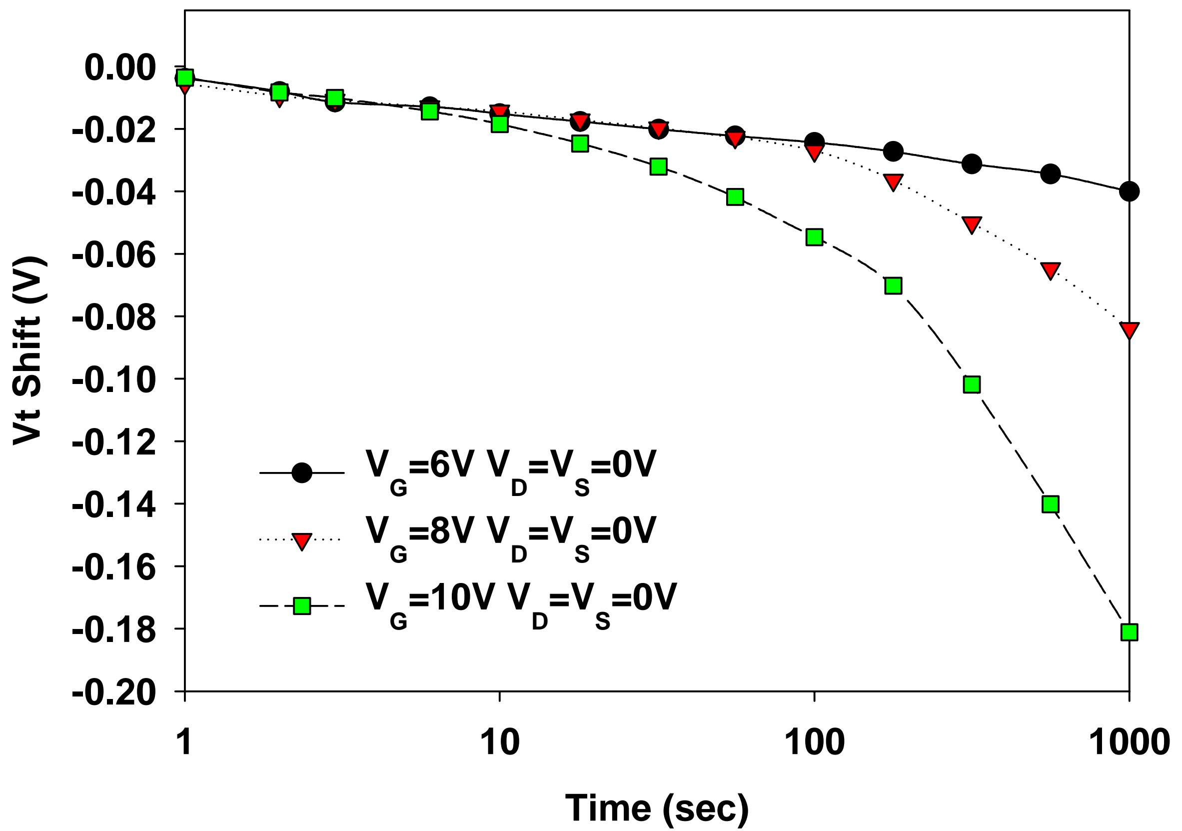


Figure 3-9. Gate disturbance characteristics of the HfO_2 nanocrystal memory cells.

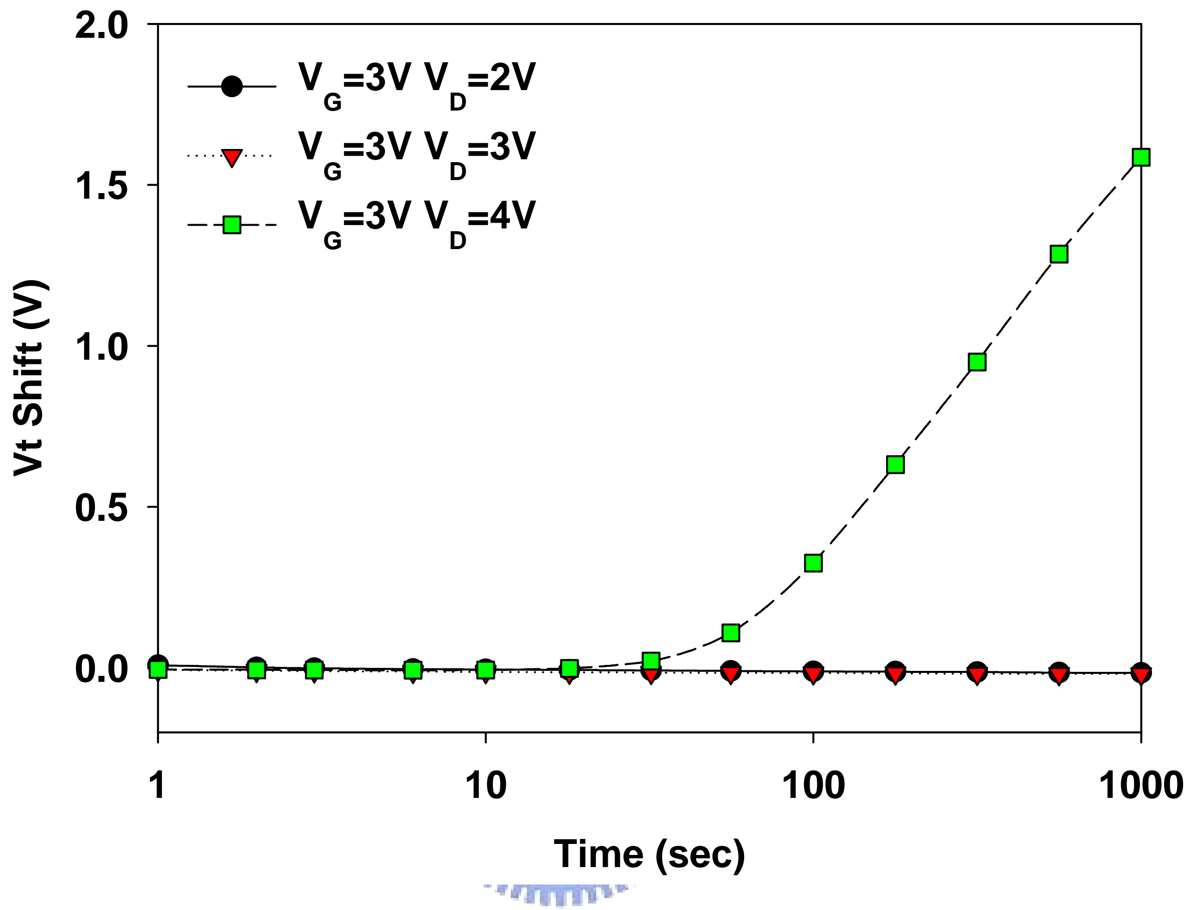


Fig 3-10. Read disturbance characteristics of the HfO_2 nanocrystal memory cells.