Chapter 4

Characteristics of P-Channel SONOS-type Flash Memory by using HfO_2 Nanocrystal Trapping Layer

4.1 Introduction

Due to its low voltage, low power and high speed programming features, p-channel flash memories [1-2] have been evolved as a promising cell for real applications in the future. In a certain design of p-channel flash cells, programming of the cell can be achieved either by band-to-band (BTB) tunneling induced hot-electron injection at the drain side or by channel-hot-hole impact ionization induced channel-hot-electron injection (CHE) (Figure 4-1(a)-(b)). Erasing of the cell can be accomplished by electron channel Fowler-Nordheim(F-N) ejection from the floating gate. Here, both Programming schemes, CHE and BTB, will generate the so-call oxide damages, which include the interface state Nit and the oxide trap charge Q_{ox}. in Steve S. Chung et. al.[3] paper, for the first time, a comparative study of p-channel flash memory performance and reliability have been presented in details for two different programming schemes. In Jao-Hsian Shiue et. al. [4] paper. The interface trap density (Dit) generated under these kinds of Fowler-Nordheim (FN) stress and Substrate-hot-hole stress. The injection of impact-ionization-generated hot holes is found to be the most important reason for interface trap generation under $V_G<0$ FN stress at high oxide field. The generated interface-trap density under Substrate-hot-hole stress increases with increasing gate oxide field. It is also found that the Substrate-hot-hole stress induces more interface traps than Substrate-hot-electron stress.

Instead of using N-channel cells, P-channel cells[5]-[13], known for the high injection efficiency and low programming drain current, are quite suitable for low-voltage and low-power applications. The developing trend of Flash memory has gone in the way of

multi-level storages. The most important issue is to precisely control a tight threshold voltage distribution at different levels. To achieve tight threshold voltage distribution in multi-level Flash memory, the bit-by-bit verification which slows down the programming speed can be performed. The multi-level applications of P-channel Flash memory was first proposed in [14-19].

In this work, we fabricate a high performance P-channel nonvolatile memory with a high-k nanocrystal charge-trapping layer. The nanocrystal material is HfO_2. This high-k nanocrystal was replaces the silicon nitride layer in the SONOS structure. These nanocrystal provide high trapping state densities and deep trapping levels, therefore they can enhance the retention of nonvolatile memories. The larger operation window can be improved, and charge-trapping efficiency can be improved. The application of nanocrystal materials can further reduce the operation voltage and potentially can help memory device scaling. It has good characteristics in terms of considerably high speed program/erase, large memory windows and good retention.

4.2 Experimental

Figure 4-2(a)-(f) schematically depicts the process flow of the proposed flash memory. The fabrication process of the HfO_2 nanocrystal memory devices involved the LOCOS isolation process on N-type, 5-10 Ω cm, (100) 150mm silicon substrates. First, a 3-nm-thick tunnel silicon dioxide was chemical vapor deposition in horizontal furnace system. After that, the sample went through RTA treatment in O_2 ambient at 900 for 30 sec. The trapping layer of amorphous $HfSiO_x$ silicate layer was deposited by co-sputtering method with pure Hafnium (99.9% pure) and pure Silicon in the Oxygen and argon gas ambient. After that, the samples went through RTA treatment in O_2 ambient at 900 for 1 minute. A blocking oxide of about 10-nm-thick was then deposited by LPCVD for TEOS oxide. After that after that, the sample went through RTA treatment in O_2 ambient at 900 for 1 minute. Then, a 200-nm-thick

poly-silicon was deposited to serve as the gate electrode by LPCVD. Then, gate electrode was patterned and the source/drain and gate were doped by self-aligned BF_2 ion implantation at the dosage and energy of 5×10^{15} ions/cm^{-2} and 20 Kev, then the substrate contact was patterned and the sub-contact was implanted with Phosphorous at the dosage and energy of 5×10^{15} ions/cm^{-2} and 40 Kev. After these implantations, the dopes were activated at 900 for 20 sec. The rest of the subsequent standard CMOS procedures were complete for fabricating the HfO_2 high k memory devices.

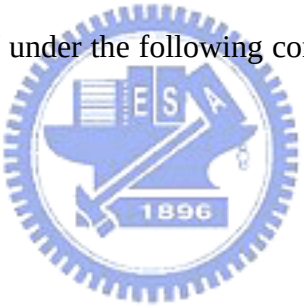
4.3 Results and Discussions

4.3.1 Characteristics of flash devices

Figure 4-3 shows the I_{DS}-V_{GS} curves of the HfO_2 nanocrystal trapping layer of SONOS type flash memory device. Band to Band hot electron injection and channel hot hole was employed for programming and erasing, respectively. A memory window of about 2V can be achieved at the V_G=7V,V_D=-7V program operation. Program characteristics of different pulse width for different operation conditions are shown in Figure 4-4. We employed channel hot-electron tunneling injection in figure 4-4. The "V_t shift" is defined as the threshold voltage change of a device between the written and the erased states. For band to band hot-electron injection with V_G=7V V_D=-7V, relatively high speed (1us) programming performance can be achieved with a memory window of about 2V. Figure 4-5 displays the erase characteristics as a function of various operation voltages. Again, excellent erase speed of around 1ms can be obtained with V_G=-10V V_D=-10V for channel hot hole injection. The retention characteristics of the HfO_2 trapping layer memory device at room temperature (T=25℃) is illustrated in Figure 4-6. The retention time can be up to 10^8 seconds for 10-15% charge loss at room temperature.

4.3.2 Disturbances

Figure 4-7 show the programming drain disturbance of our HfO_2 trapping layer flash memory. Drain disturbance may occur during programming for the cells sharing a common bit-line while one of the cells is being programmed and gate disturbance may occur during programming for the cells sharing a common word-line while one of the cells is being programmed. Three different drain voltages (V_D=-2V, -3V and -4V) were applied in the programming drain disturbance measurements at room temperatures. We observed that a -1V drain disturb was observed after programming at a value of V_D of -4V under T=25℃ and after stressing for 1000 seconds. Figure 4-8 show the gate disturbance characteristics in the erasing state and programming state. Gate disturbance may occur during programming for the cells sharing a common word-line while one of the cells is being programmed. We observed a threshold voltage shift of ±0.3V under the following conditions V_G=6V and V_G=-6V; stressed for 1000 seconds.



4.4 Summary

In this chapter, we have investigated the memory effect on the performance of the p-channel HfO_2 nanocrystal trapping layer of SONOS type flash memories. It has good characteristics in terms of large memory window, high program/erase speed and good retention.

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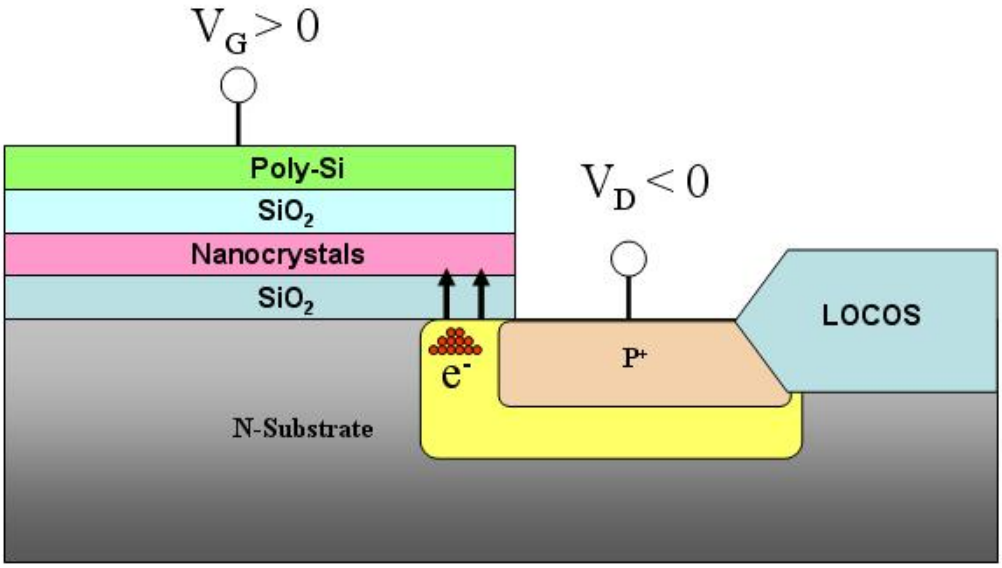
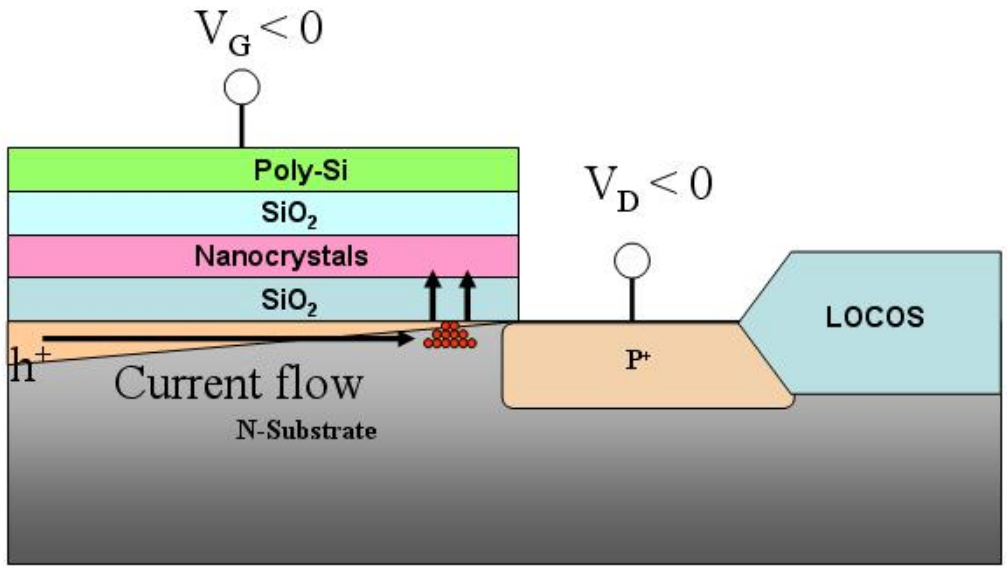
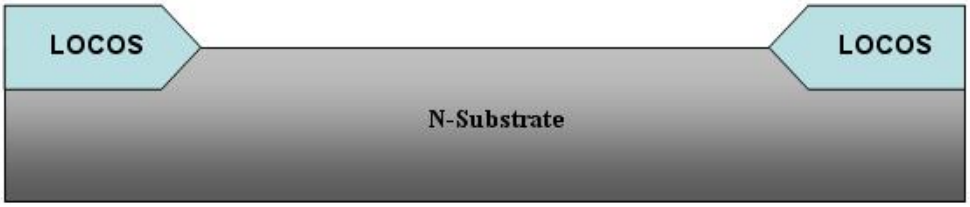


(a)Band to Band hot carrier injection

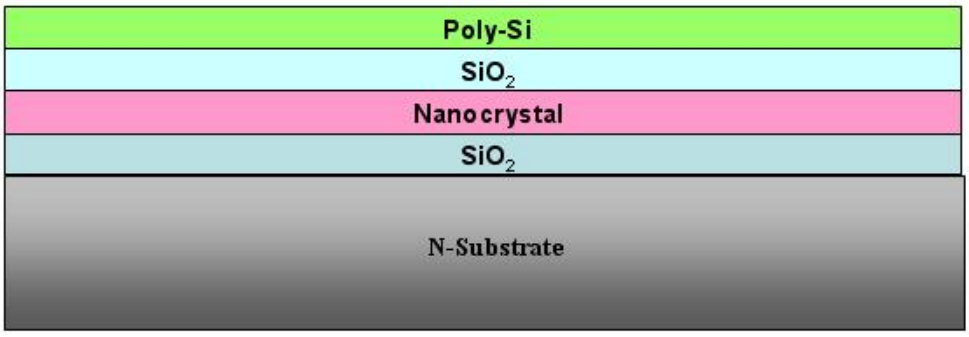


(b)Channel Hot carrier injection

Figure 4-1. Band to Band Hot carrier and Channel hot carrier injections.

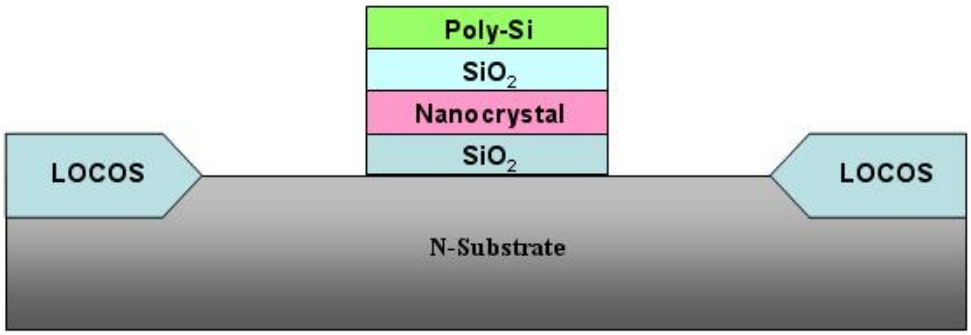


(a)

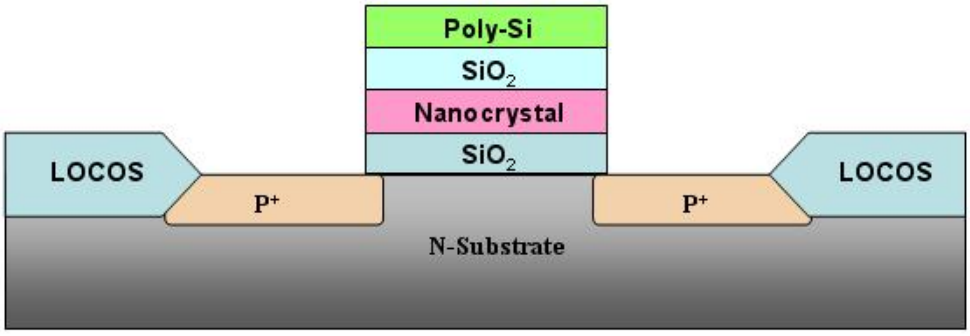


(b)

Figure 4-2. Schematically depicts the process flow of the proposed flash memory.

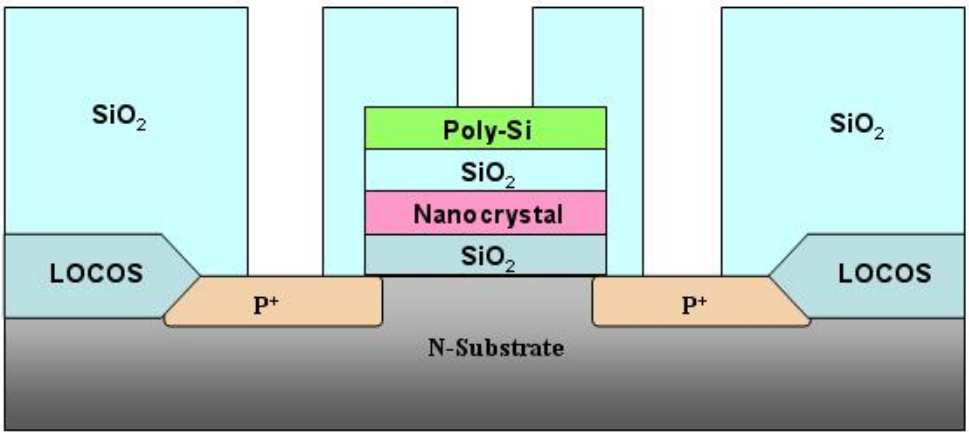


(c)

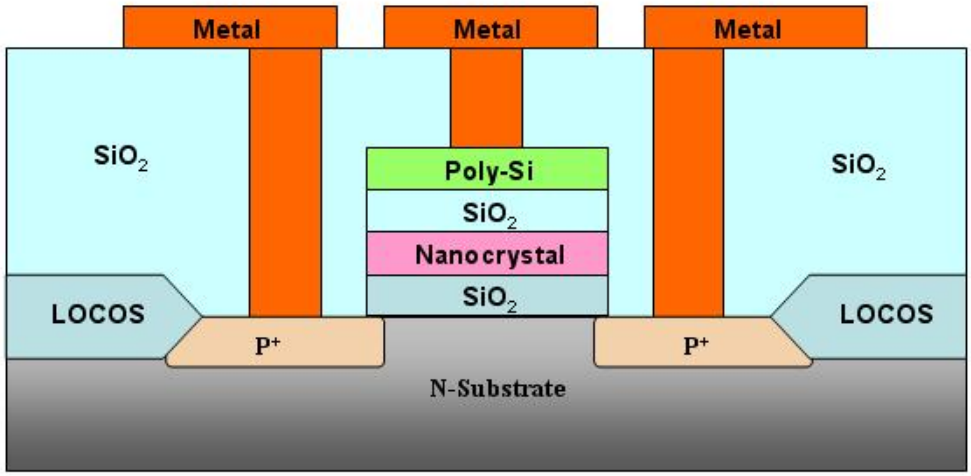


(d)

Figure 4-2. Schematically depicts the process flow of the proposed flash memory.



(e)



(f)

Figure 4-2. Schematically depicts the process flow of the proposed flash memory.

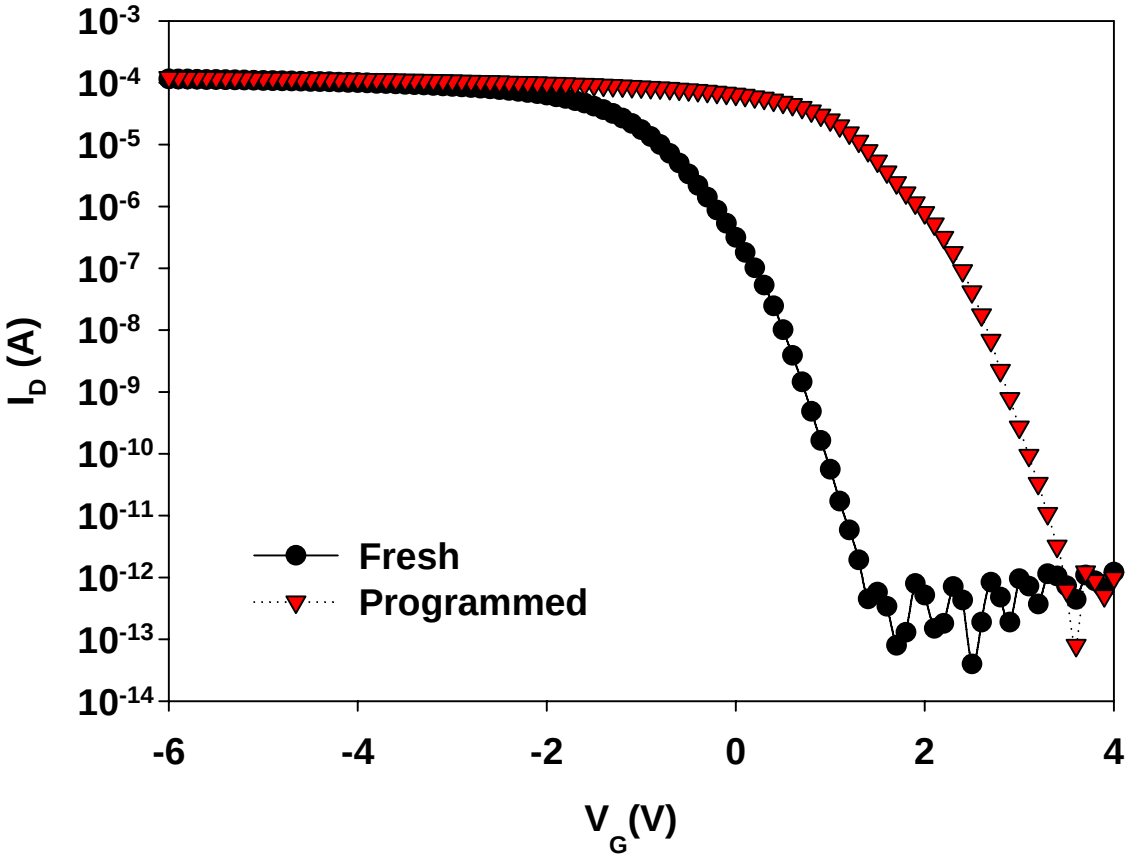


Figure 4-3. I_{DS}-V_{GS} characteristics of P-Channel HfO_2 nanocrystal memory devices.

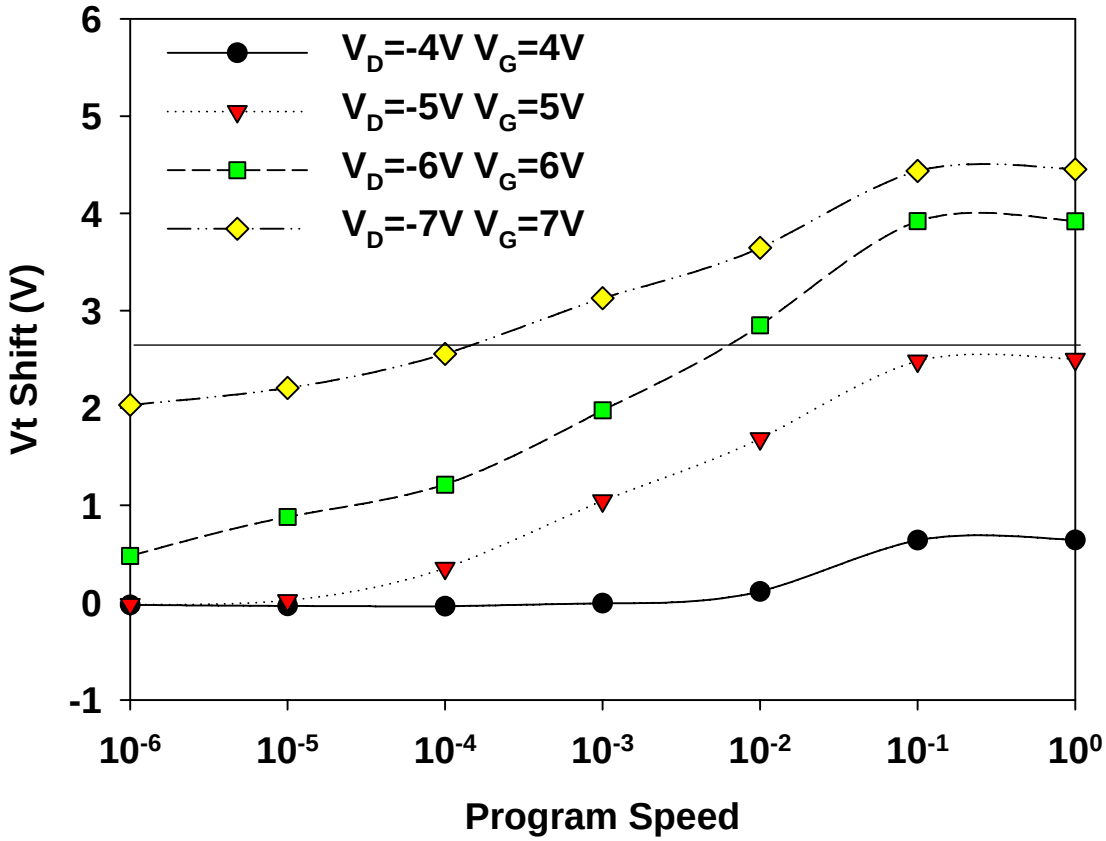


Figure 4-4. Program characteristics of P-channel HfO_2 nanocrystal memory device with different programming conditions.

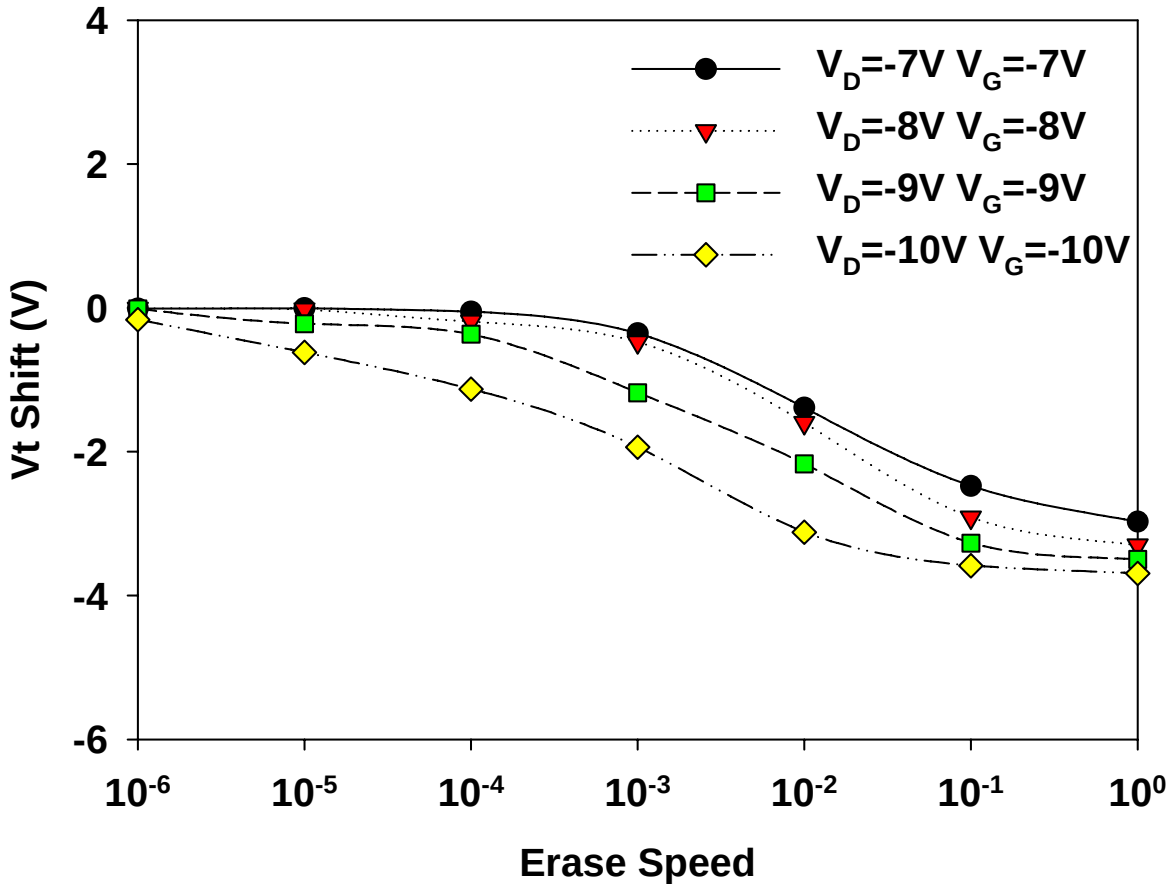


Figure 4-5. Erase characteristics of HfO_2 nanocrystal memory device with different erasing conditions.

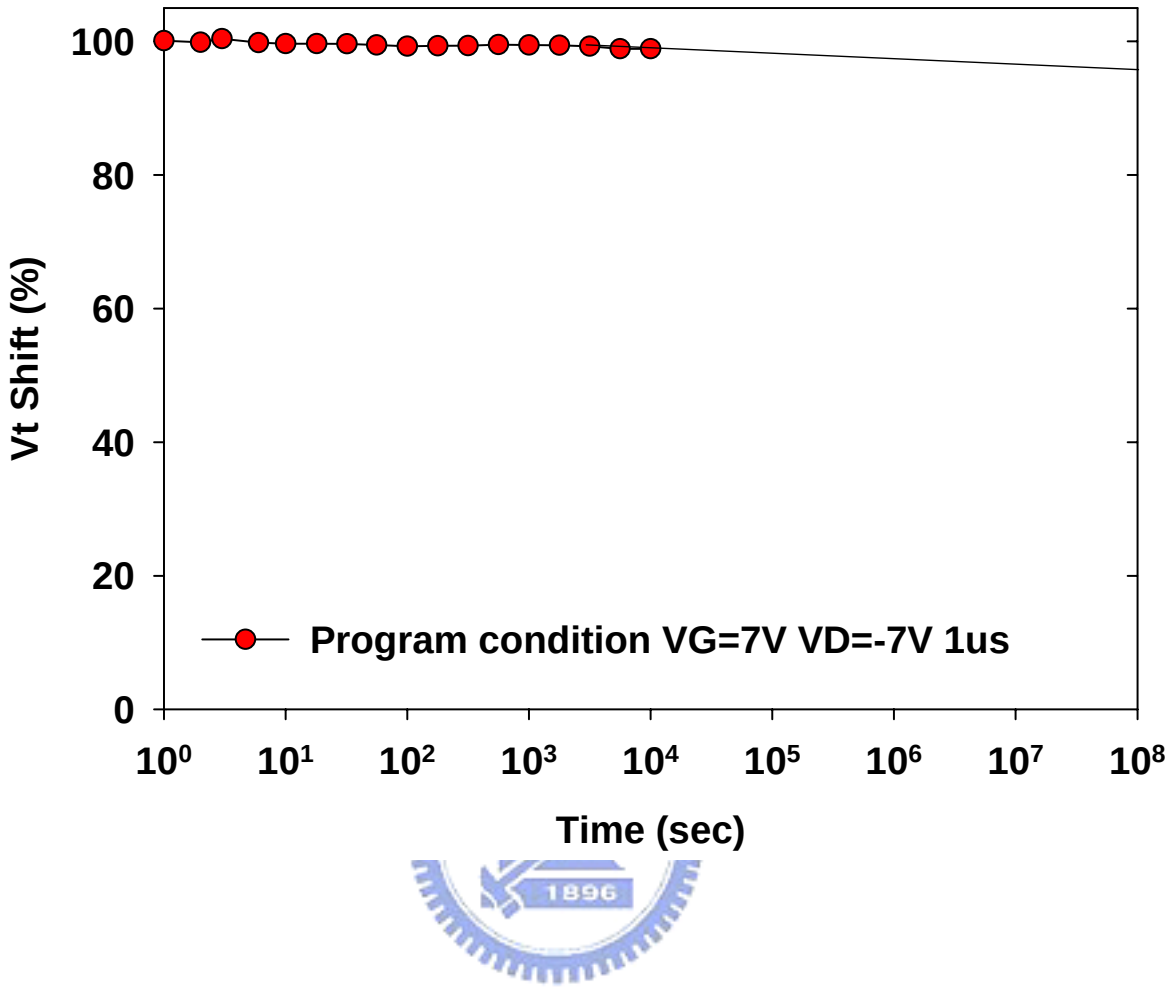


Figure 4-6. Retention characteristic of HfO_2 nanocrystal memory devices at T=25℃

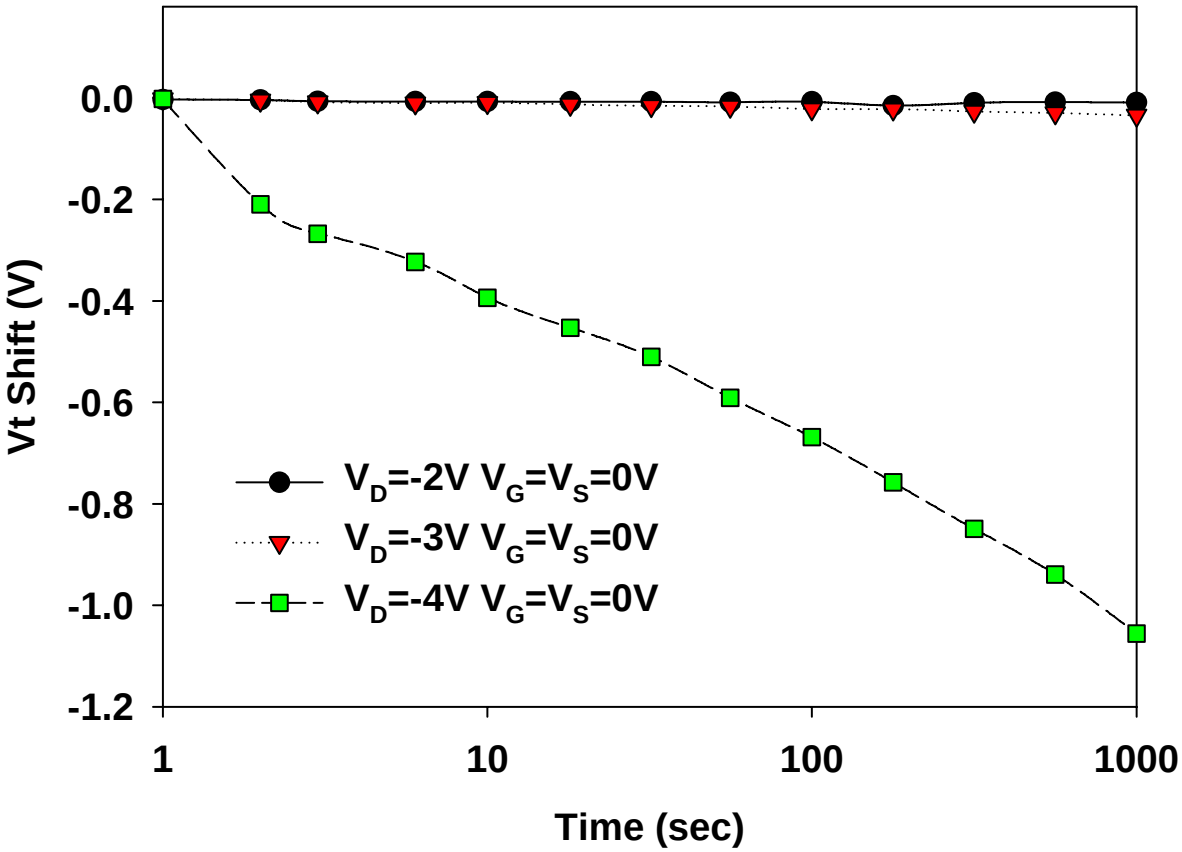


Figure 4-7. Drain disturbance characteristics of the HfO_2 nanocrystal memory cells.

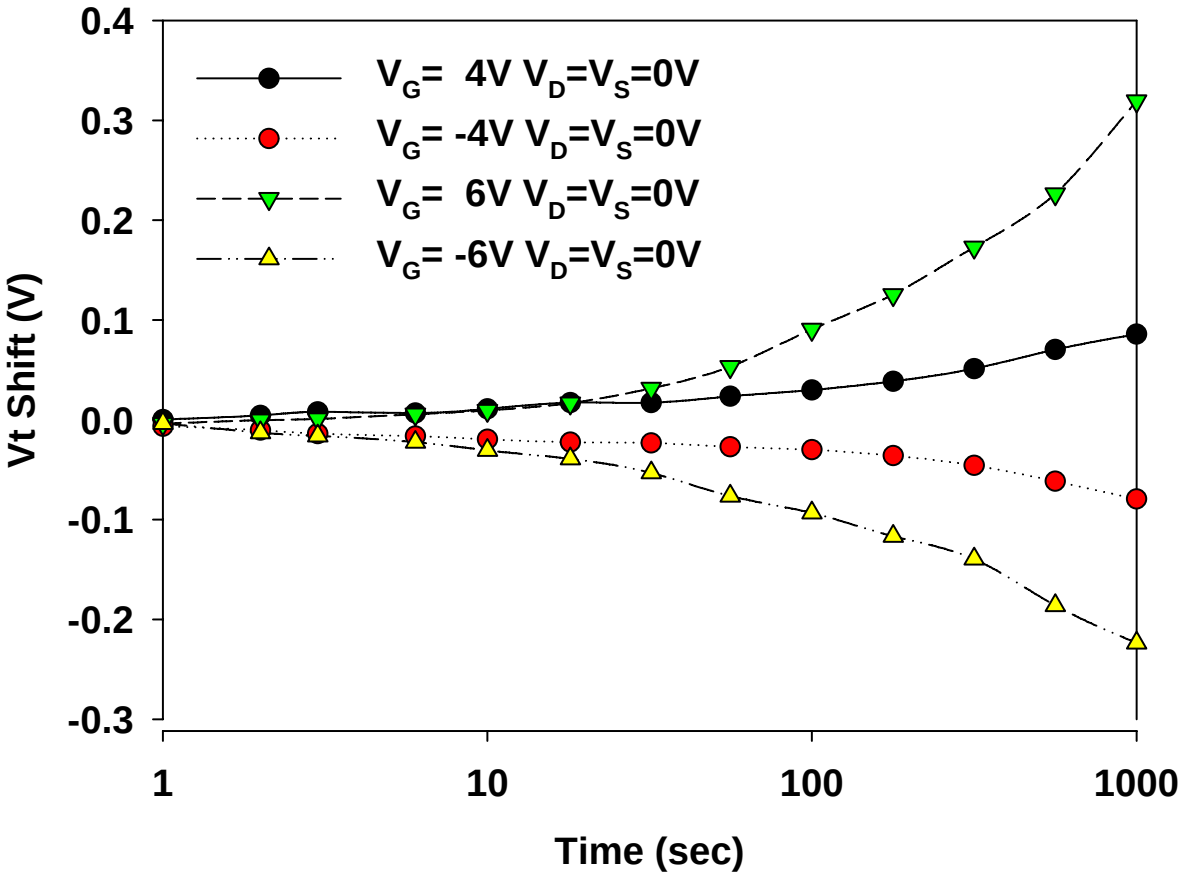


Figure4-8. Gate disturbance characteristics of the HfO_2 nanocrystal memory cells.