

## Contents

**Contents ..... v**

**Content of Picture ..... vii**

**Content of Table ..... xii**

**Chapter 1 Introduction ..... 1**

1.1 Brief Introduction ..... 1

1.2 Organization of the Thesis ..... 4

**Chapter 2 History of Image Sensor & others research 5**

2.1 Photoelectric effect ..... 5

2.1.1 Light versus Electromagnetic Waves ..... 7

2.1.2 Theorem of Photoelectric Effect ..... 11

2.2 Photo Detector ..... 14

2.2.1 Photodiodes ..... 16

2.2.2 Phototransistors ..... 20

2.3 CCD & CMOS ..... 23

2.4 Wide Dynamic Range research ..... 27

2.4.1 Dual Sampling [25] ..... 28

2.4.2 Logarithm Conversion [26] ..... 29

2.4.3 Capacitance Modulation Conversion [21][27] ..... 30

2.4.4 Pixel Level ADC with Multi-Sampling [22][28] ..... 31

2.4.5 Pixel Level Analog Processing [8][29][30][31][32][33] ..... 32

2.5 Differential Difference Amplifier ( DDA ) [9][34] ..... 34

2.6 Temperature Compensated Circuit [10] ..... 36

2.7 Bandgap Circuit 【3】【13】 ..... 39

**Chapter 3 Wide Dynamic Range & Temperature**

**Compensated Gain CMOS Image Sensor in**

**Automotive Application.....43**

3.1 System Architecture ..... 43

3.2 Circuit Design ..... 44

3.2.1 Analog Memory in Active Pixel Sensor ( AMAPS ) ..... 44

3.2.2 Correlated Double Sampling Circuit ..... 51

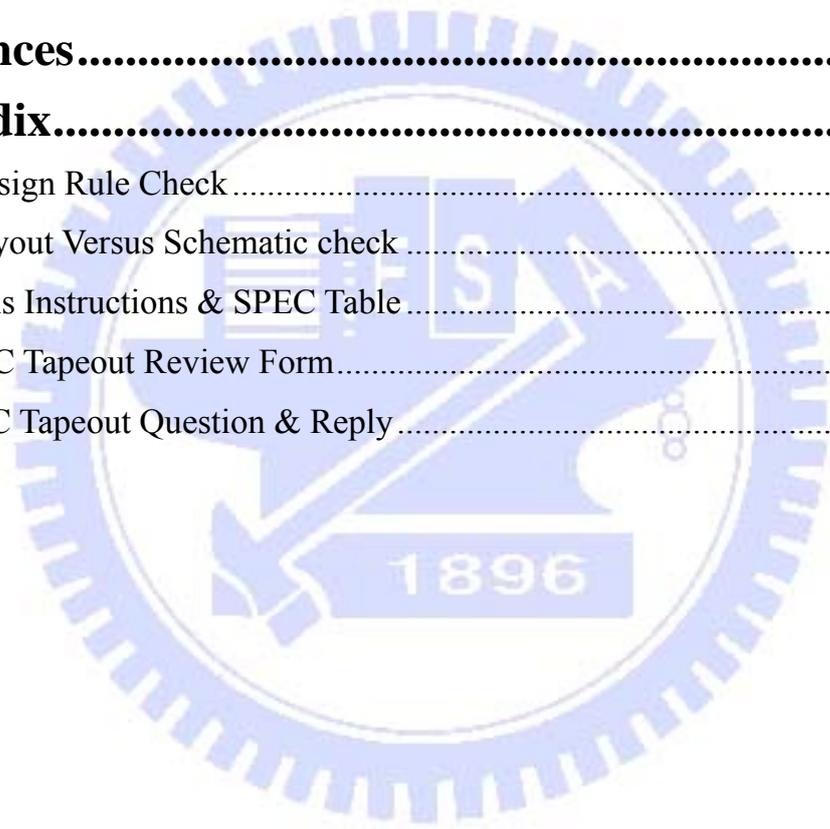
3.2.3 Temperature Compensated Differential Difference Amplifier ( TCDDA )

..... 51

3.2.4 Bandgap Reference ..... 55

3.2.5 Large Analog System Bias Circuit 【3】 ..... 58

3.2.6 Timing Generator .....	59
<b>Chapter 4 Implementation, Test Platform &amp; Result ..</b>	<b>61</b>
4.1 Chip Design Flow & Implementation .....	61
4.2 Chip Layout.....	62
4.3 Test Platform Design .....	68
4.4 Result.....	71
<b>Chapter 5 Conclusion .....</b>	<b>74</b>
5.1 Conclusion.....	74
5.2 Future Work.....	74
<b>References.....</b>	<b>76</b>
<b>Appendix.....</b>	<b>80</b>
A. Design Rule Check.....	80
B. Layout Versus Schematic check.....	83
C. Pins Instructions & SPEC Table.....	84
D. CIC Tapeout Review Form.....	85
E. CIC Tapeout Question & Reply.....	89



# Content of Picture

<b>FIG. 1.1-1 THE CROSS-SECTIONAL VIEW OF DIGITAL CAMERA SONY-A100 EXTRACTED FROM ARENA NIKKEIBP REPORT &lt; 1 &gt;</b> .....	1
<b>FIG. 1.1-2 FRAME QUALITY ON CMOS IMAGE SENSOR WHICH IN 65°C,85°C AND 105°C EXTRACTED FROM M. SCHANZ, C. NITTA, A. BUBANNM, B. J. HOSTICKA, R. K. WERTHEIMER, "A HIGH-DYNAMIC-RANGE CMOS IMAGE SENSOR FOR AUTOMOTIVE APPLICATIONS", IN IEEE JSSC, VOL. 35,NO.7, PP.932~938, JULY 2000. [5]</b> .....	3
<b>FIG. 1.1-3 FOUR INTEGRATION TIME WITH THREE DIFFERENT GAIN TO SOLVE FRAME PROBLEM EXTRACTED FROM B. J. HOSTICKA, W. BROCKHERDE, A. BUBANNM, T. HEIMANN, R. JEREMIAS, A. KEMNA, C. NITTA, O. SCHREY, "CMOS IMAGING FOR AUTOMOTIVE APPLICATIONS", IN IEEE TRANS. ELECTRON DEVICES, VOL. 50, No.1, PP.173~183, JANUARY 2003. [6]</b> .....	3
<b>FIG. 1.1-4 LEAKAGE CURRENT ON DIFFERENCE VOLTAGE(A) IN N+/N-WELL/PSB(B)N+/P-WELL ,1000/T VERSUS <math>n_i</math> AND <math>n_i^2</math> VARIATION (<math>n_i</math> : INTRINSIC CONCENTRATION )</b> EXTRACTED FROM N. V. LOUKIANOVA, H. O. FOLKERTS, J. P. V. MAAS, D. W. E. VERBURGT, A. J. MIEROP, W. HOEKSTRA, E. ROKS, A. J. P. THEUWISSEN, "LEAKAGE CURRENT MODELING OF TEST STRUCTURES FOR CHARACTERIZATION OF DARK CURRENT IN CMOS IMAGE SENSORS", IN IEEE TRANS. ELECTRON DEVICES, VOL. 50, No.1, PP.77~83, JANUARY 2003. [7] .....	4
<b>FIG. 2.1-1 SNAPSHOT OF ELECTROMAGNETIC WAVE EXTRACTED FROM MONOS LAB IN LEIDEN UNIVERSITY, NETHERLANDS &lt; 3 &gt;</b> .....	6
<b>FIG. 2.1-2 DEFINITION OF WAVELENGTH EXTRACTED FROM MONOS LAB IN LEIDEN UNIVERSITY, NETHERLANDS &lt; 3 &gt;</b> .....	6
<b>FIG. 2.1-3 ELECTROMAGNETIC WAVE SPECTRUM EXTRACTED FROM PHYSICS DEMO LAB IN NTNU &lt; 2 &gt;</b> ..	7
<b>FIG. 2.1-4 INFRARED RAY APPLICATION EXTRACTED FROM DIPOL WEBSITE &lt; 4 &gt;</b> .....	8
<b>FIG. 2.1-5 WHITE LIGHT EXTEND BY PRISM EXTRACTED FROM DHD MULTIMEDIA GALLERY &lt; 5 &gt;</b> .....	9
<b>FIG. 2.1-6 INFRARED X-RAY OF HAND EXTRACTED FROM COLORXRAYS.COM &lt; 6 &gt;</b> .....	10
<b>FIG. 2.1-7 LENARD PHOTON EXPERIMENT (GET PLATE) EXTRACTED FROM MICHAEL FOWLER, "THE PHOTOELECTRIC EFFECT"&lt; 7 &gt;</b> .....	12
<b>FIG. 2.1-8 LENARD PHOTON EXPERIMENT (DON'T GET PLATE) EXTRACTED FROM MICHAEL FOWLER, "THE PHOTOELECTRIC EFFECT"&lt; 7 &gt;</b> .....	13
<b>FIG. 2.2-1 JUNCTION DEVICES AVAILABLE IN A STANDARD N-WELL CMOS PROCESS FOR LIGHT DETECTION. THE COMPLEMENTARY STRUCTURES ARE OBTAINED IN A P-WELL PROCESS. THE ACTIVE JUNCTION IS SHADED FOR EACH DEVICE. (A) WELL/SUBSTRATE (<math>n^- / p^-</math>) DIODE; (B) DIFFUSION/SUBSTRATE (<math>n^+ / p^-</math>) DIODE; (C) DIFFUSION/WELL (<math>p^+ / n^-</math>) DIODE; (D) (<math>p^+ / n^- / p^-</math>) VERTICAL BIPOLAR TRANSISTOR;</b> EXTRACTED FROM TAMÁS ROSKA, ÁNGEL RODRÍGUEZ – VÁZQUEZ, "TOWARDS THE VISUAL MICROPROCESSOR – VLSI DESIGN AND THE USE OF CELLULAR NEURAL NETWORK UNIVERSAL MACHINES" CHAPTER 5 LIGHT-SENSITIVE DEVICES IN CMOS PAGE 185 [4] .....	15
<b>FIG. 2.2-2 PHOTO-GENERATION OF CARRIERS IN A PHOTODIODE. ELECTRON-HOLE PAIRS WHICH ARE CREATED IN THE DEPLETION REGION OF THE REVERSE BIASED JUNCTION CAN BE DETECTED AS AN INCREASE IN THE REVERSE CURRENT (PHOTOCONDUCTIVE MODE OF OPERATION) OR AS A CHANGE IN THE VOLTAGE ACROSS IT (PHOTOVOLTAIC MODE OF OPERATION) ; (A) CROSS-SECTION OF THE DEVICE STRUCTURE; (B) ENERGY BAND DIAGRAM; (C) ELECTRICAL REPRESENTATION OF THE PHOTODIODE</b> EXTRACTED FROM TAMÁS ROSKA, ÁNGEL RODRÍGUEZ – VÁZQUEZ, "TOWARDS THE VISUAL MICROPROCESSOR – VLSI DESIGN AND THE USE OF CELLULAR NEURAL NETWORK UNIVERSAL MACHINES" CHAPTER 5 LIGHT-SENSITIVE DEVICES IN CMOS PAGE 186 [4] .....	16
<b>FIG. 2.2-3 QUANTUM EFFICIENCY FOR A SILICION <math>p^+ / n^-</math> PHOTODIODE AS A FUNCTION OF THE WAVELENGTH OF THE INCIDENT LIGHT</b> EXTRACTED FROM TAMÁS ROSKA, ÁNGEL RODRÍGUEZ – VÁZQUEZ, "TOWARDS THE VISUAL MICROPROCESSOR – VLSI DESIGN AND THE USE OF CELLULAR NEURAL NETWORK UNIVERSAL MACHINES" CHAPTER 5 LIGHT-SENSITIVE DEVICES IN CMOS PAGE 187 [4] .....	17
<b>FIG. 2.2-4 SPECTRAL RESPONSE OF <math>n^- / p^-</math> AND <math>p^+ / n^-</math> DIODES AS MEASURED BY DELBRÜCK IN A BiCMOS PROCESS</b> EXTRACTED FROM TAMÁS ROSKA, ÁNGEL RODRÍGUEZ – VÁZQUEZ, "TOWARDS THE VISUAL MICROPROCESSOR – VLSI DESIGN AND THE USE OF CELLULAR NEURAL NETWORK UNIVERSAL	

**FIG. 2.2-5 PHOTO-GENERATION OF CARRIERS IN A PHOTOTRANSISTOR. ELECTRON-HOLE PAIRS CREATED IN THE DEPLETION REGION OF THE REVERSE BIASED BASE/COLLECTOR JUNCTIONS WILL INDUCE A BASE CURRENT,  $I_{ph}$ , WHICH WILL BE AMPLIFIED BY THE GAIN OF THE TRANSISTOR, RESULTING IN AN EMITTER CURRENT WHICH IS  $(1 + \beta_F)$  TIMES THE DETECTED CURRENT. (A) CROSS-SECTION OF THE DEVICE STRUCTURE; (B) ENERGY BAND DIAGRAM; (C) ELECTRICAL REPRESENTATION OF THE PHOTOTRANSISTOR** EXTRACTED FROM TAMÁS ROSKA, ÁNGEL RODRÍGUEZ – VÁZQUEZ, "TOWARDS THE VISUAL MICROPROCESSOR – VLSI DESIGN AND THE USE OF CELLULAR NEURAL NETWORK UNIVERSAL MACHINES" CHAPTER 5 LIGHT-SENSITIVE DEVICES IN CMOS PAGE 192 [4] ..... 20

**FIG. 2.2-6 SPECTRAL RESPONSE OF  $n^-/p^-$  AND  $p^+/n^-$  DIODES AND  $p^+/n^-/p^-$  VERTICAL TRANSISTOR AS MEASURED BY DELBRÜCK IN A BICMOS PROCESS** EXTRACTED FROM TAMÁS ROSKA, ÁNGEL RODRÍGUEZ – VÁZQUEZ, "TOWARDS THE VISUAL MICROPROCESSOR – VLSI DESIGN AND THE USE OF CELLULAR NEURAL NETWORK UNIVERSAL MACHINES" CHAPTER 5 LIGHT-SENSITIVE DEVICES IN CMOS PAGE 194 [4] ..... 22

**FIG. 2.3-1 (A) READOUT ARCHITECTURES OF INTERLINE TRANSFER CCD AND (B) CMOS IMAGE SENSORS** EXTRACTED FROM ABBAS EL GAMAL, HELMY ELTOUKHY, "CMOS IMAGE SENSORS", IEEE CIRCUITS AND DEVICES MAGAZINE, PP. 6-20 MAY/JUNE 2005 [18]..... 23

**FIG. 2.3-2 THE DEFERENCE OF CCD & CMOS ON CAMERA SYSTEM MODULE** EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION ..... 24

**FIG. 2.3-3 CCDS' SIGNAL TRANSFER THEOREM** EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION ..... 24

**FIG. 2.3-4 CIRCUIT CHAIN FROM PIXEL TO CDS** EXTRACTED FROM KAZUYA YONEMOTO, HIROFUMI SUMI, "A NUMERICAL ANALYSIS OF A CMOS IMAGE SENSOR WITH A SIMPLE FIXED-PATTERN-NOISE-REDUCTION TECHNOLOGY", IN IEEE TRANS. ELECTRON DEVICES, VOLUME 49, ISSUE 5, PP.746~753, MAY 2002[20] ..... 25

**FIG. 2.3-5 (A) NIKON D100 CCD (B) CANON EOS 350D CMOS IMAGE SENSOR** EXTRACTED FROM MR. OH DIGITAL COURSE CHAP. 2 "SENSOR DEVICES: CCD & CMOS" < 8 > ..... 26

**FIG. 2.4-1 COMPARISON OF CMOS DPS IMAGER VERSUS CCD IMAGER USING A HDR SCENE** EXTRACTED FROM ABBAS EL GAMAL, HELMY ELTOUKHY, "CMOS IMAGE SENSORS", IN IEEE CIRCUITS AND DEVICES MAGAZINE, PP. 6-20 MAY/JUNE 2005 [18]..... 27

**FIG. 2.4-2 SCHEMATIC ILLUSTRATION OF DUAL-SAMPLE, DUAL OUTPUT IMAGER ARCHITECTURE** EXTRACTED FROM O. Y. PETCH., E. R. FOSSUM, "WIDE INTERSCENE DYNAMIC RANGE SMOS APS USING DUAL SAMPLING," IN IEEE TRANS. ELECTRON DEVICES, VOL. 44, NO. 10, PP. 1721~1723, 1997.[25] ... 28

**FIG. 2.4-3 LOGARITHM CONVERSION PIXEL CIRCUIT** EXTRACTED FROM 萩原義雄,ほか,"対数変換形 CMOS エエリア固体撮像素子",映像情報メディア学会誌, VOL.54, NO.2, PP.224~228, 2000.[26] ..... 29

**FIG. 2.4-4 (A) CAPACITANCE MODULATION PIXEL CIRCUIT (B) SIGNAL VALUE VERSUS CAPACITANCE MODULATION** EXTRACTED FROM S. J. DECKER, R. D. MCGRATH, K. BREHMER, AND C. G. SODINI, "A 256 × 256 CMOS IMAGING ARRAY WITH WIDE DYNAMIC RANGE PIXELS AND COLUMN PARALLEL DIGITAL OUTPUT," IN ISSCC, DIG. TECH. PAPERS, PP.176~177, 1998.[27] ..... 30

**FIG. 2.4-5 (A) EMBEDDED A/D PIXEL BLOCK AND COLUMN SENSE AMPLIFIER CIRCUIT (B) ILLUMINATION TO OUTPUT DIGITAL NUMBER TRANSFER CURVE** EXTRACTED FROM D. YANG, A. EL GAMAL, B. FOWLER, AND H. TIAN, "A 640X512 CMOS IMAGE SENSOR WITH ULTRAWIDE DYNAMIC RANGE FLOATING-POINT PIXEL-LEVEL ADC," IN IEEE JSSC, VOL.34, PP. 1821~1834, DEC. 1999.[22] ..... 31

**FIG. 2.4-6 IMAGE SENSOR BLOCK DIAGRAM** EXTRACTED FROM Y. MURAMATSU, S. KUROSAWA, M. FURUMIYA, H. OHKUBO, Y. NAKASHIBA. "A SIGNAL-PROCESSING CMOS IMAGE SENSOR USING A SIMPLE ANALOG OPERATION", IEEE JSSC, VOL. 38, NO.1, JANUARY 2003[8]..... 32

**FIG. 2.4-7 WIDE DYNAMIC-RAGE READOUT (A) TIMING CHART (B) POTENTIAL DIAGRAM AT HIGH INCIDENT LIGHT (C) POTENTIAL DIAGRAM AT LOW INCIDENT LIGHT** EXTRACTED FROM Y. MURAMATSU, S. KUROSAWA, M. FURUMIYA, H. OHKUBO, Y. NAKASHIBA., "A SIGNAL-PROCESSING CMOS IMAGE SENSOR USING A SIMPLE ANALOG OPERATION", IN IEEE JSSC, VOL. 38, NO. 1, PP.101~106, JANUARY 2003.[8] ..... 33

**FIG. 2.5-1 (A) SYMBOL OF DDA (B) BLOCK DIAGRAM OF DDA** EXTRACTED FROM S. C. HUANG, M. ISMAIL, S. R. ZARABADI, "A WIDE RANGE DIFFERENTIAL DIFFERENCE AMPLIFIER: A BASIC BLOCK FOR ANALOG SIGNAL PROCESSING IN MOS TECHNOLOGY", IN IEEE TRANS. C.A.S.-II : ANALOG AND DIGITAL SIGNAL

PROCESSING, VOL. 40, NO.5, PP. 289~301, MAY 1993.[34] .....	34
<b>FIG. 2.5-2 SINGLE ENDED DDA WITH CLASS AB REALIZATION</b> EXTRACTED FROM H. ALZAHER, M. ISMAIL, "A CMOS FULLY BALANCED DIFFERENTIAL DIFFERENCE AMPLIFIER AND ITS APPLICATIONS", IN IEEE TRANS. C.A.S.-II : ANALOG AND DIGITAL SIGNAL PROCESSING, VOL. 48,NO. 6, PP.614~620, JUNE 2001.[9] .....	36
<b>FIG. 2.6-1 TEMPERATURE STABLE DIFFERENTIAL PAIR ARCHITECTURE</b> EXTRACTED FROM J. A. S. DIAS, W. B. DE MORAES, "CMOS TEMPERATURE- STABLE LIBERALIZED DIFFERENTIAL PAIR", IN ELECTRONICS LETTERS, VOL.28 NO.25, PP.2350~2351 3 <sup>RD</sup> DECEMBER 1992. [10] .....	37
<b>FIG. 2.6-2 (A) GM WITHOUT TEMPERATURE STABLE CIRCUIT, 3350PPM/°C (0-100°C) (B) GM WITH TEMPERATURE STABLE CIRCUIT, 95PPM/°C (0-100°C)</b> EXTRACTED FROM J. A. S. DIAS, W. B. DE MORAES, "CMOS TEMPERATURE- STABLE LIBERALIZED DIFFERENTIAL PAIR", IN ELECTRONICS LETTERS, VOL.28 NO.25, PP.2350~2351 3 <sup>RD</sup> DECEMBER 1992. [10] .....	39
<b>FIG. 2.7-1 GENERATION OF PTAT VOLTAGE</b> EXTRACTED FROM BEHZAD RAZAVI, "DESIGN OF ANALOG CMOS INTEGRATED CIRCUITS", MCGRAW-HILL COMPANIES, INC. 2004. [3] .....	41
<b>FIG. 2.7-2 BANDGAP REFERENCE THEOREM</b> EXTRACTED FROM PROF. G. A. RINCÓN-MORA, "BANDGAP VOLTAGE REFERENCE", ANALOG INTEGRATED CIRCUIT HANDOUT [13] .....	41
<b>FIG. 2.7-3 ACTUAL IMPLEMENT OF THE CONCEPT OF TEMPERATURE INDEPENDENT VOLTAGE</b> EXTRACTED FROM BEHZAD RAZAVI, "DESIGN OF ANALOG CMOS INTEGRATED CIRCUITS", MCGRAW-HILL COMPANIES, INC. 2004. [3] .....	42
<b>FIG. 3.1-1 SYSTEM ARCHITECTURE</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....	43
<b>FIG. 3.2-1 PIXEL SCHEMATIC DIAGRAM (FD RESET TYPE SENSOR)</b> EXTRACTED FROM N. AKAHANE, S. SUGAWA, S. ADACI, K. MORI, T. ISHIYUKI, K. MIZOBUCHI, "A SENSITIVITY AND LINEARITY IMPROVEMENT OF A 100-DB DYNAMIC RANGE CMOS IMAGE SENSOR USING A LATERAL OVERFLOW INTEGRATION CAPACITOR", IN IEEE JSSC, VOL. 41, ISSUE 4, PP.851~858, APRIL 2006.[33] .....	45
<b>FIG. 3.2-2 POTENTIAL DIAGRAM(FD RESET TYPE SENSOR)</b> EXTRACTED FROM N. AKAHANE, S. SUGAWA, S. ADACI, K. MORI, T. ISHIYUKI, K. MIZOBUCHI, "A SENSITIVITY AND LINEARITY IMPROVEMENT OF A 100-DB DYNAMIC RANGE CMOS IMAGE SENSOR USING A LATERAL OVERFLOW INTEGRATION CAPACITOR", IN IEEE JSSC, VOL. 41, ISSUE 4, PP.851~858, APRIL 2006.[33] .....	45
<b>FIG. 3.2-3 APS + ANALOG MEMORY+ CDS CIRCUITS DIAGRAM</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION.....	46
<b>FIG. 3.2-4 SIMULATION OF SENSOR OUTPUT SIGNAL IN VOLTAGE VARIATION</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....	46
<b>FIG. 3.2-5 SIMULATION OF CDS OUTPUT SIGNAL IN VOLTAGE VARIATION WITH DIFFERENT INCIDENT LIGHT</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....	47
<b>FIG. 3.2-6 DYNAMIC RANGE SIMULATION</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....	47
<b>FIG. 3.2-7 CDS OUTPUT VOLTAGE V.S PROCESS VARIATION IN 90% VDD</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION.....	48
<b>FIG. 3.2-8 CDS OUTPUT VOLTAGE V.S PROCESS VARIATION IN 110% VDD</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION.....	48
<b>FIG. 3.2-9 DYNAMIC RANGE V.S PROCESS VARIATION</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....	49
<b>FIG. 3.2-10 DYNAMIC RANGE V.S TEMPERATURE VARIATION(25°C ,45°C ,65°C, 85°C)</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION.....	49
<b>FIG. 3.2-11 (A)READOUT CIRCUIT OF CMOS PHOTO-GATE ACTIVE PIXEL IMAGE SENSOR (B)RELATED OPERATION TIMING</b> EXTRACTED FROM Y. DEĞERLI, F. LAVERNHE, P. MAGNAN, J. A. FARRÉ, "ANALYSIS AND REDUCTION OF SIGNAL READOUT CIRCUITRY TEMPORAL NOISE IN CMOS IMAGE SENSORS FOR LOW-LIGHT LEVELS", IEEE TRANS. ON ELECTRON DEVICES, VOL. 47, NO.5, PP. 949~962, MAY 2000.[36] .....	51
<b>FIG. 3.2-12 TEMPERATURE COMPENSATED DIFFERENTIAL DIFFERENCE AMPLIFIER CIRCUIT</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION.....	52
<b>FIG. 3.2-13 GAIN VARIATION WITHOUT TEMPERATURE COMPENSATION CIRCUIT, GAIN DECREASE 0.69DB (0°C~125°C) ,AVERAGE VARIATION 661.437PPM/°C</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION.....	53
<b>FIG. 3.2-14 GAIN VARIATION WITH TEMPERATURE COMPENSATION CIRCUIT, GAIN DECREASE 0.117DB (0°C~125°C) ,AVERAGE VARIATION 135.612PPM/°C</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG	

HUNG. 'S ) COORDINATION .....	53
<b>FIG. 3.2-15 TCDDA TRANSFER LINEARITY V.S PROCESS VARIATION (TT, FF, SS, SE, FS) EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....</b>	<b>54</b>
<b>FIG. 3.2-16 TCDDA OUTPUT VOLTAGE LEVEL V.S VDDA VARIATION, TEMPERATURE VARIATION (ALMOST CAN'T RECOGNIZED THE TEMPERATURE VARIATION EFFECT) EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....</b>	<b>54</b>
<b>FIG. 3.2-17 TCDDA FREQUENCY RESPONSE WITHIN 12.529dB@25°C, PM 97.13° EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....</b>	<b>55</b>
<b>FIG. 3.2-18 LOW VOLTAGE BANDGAP VOLTAGE REFERENCE EXTRACTED FROM K. N. LEUNG, P. K. T. MOK, "A SUB-1-V 15-PPM/°C CMOS BANDGAP VOLTAGE REFERENCE WITHOUT REQUIRING LOW THRESHOLD VOLTAGE DEVICE", IN IEEE JSSC, VOL 37, NO.4, PP., PP.526~530, APRIL 2002. [11] .....</b>	<b>55</b>
<b>FIG. 3.2-19 1V BANDGAP REFERENCE VOLTAGE, VARIATION IN 9.6PPM/°C (0°C~125°C) EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....</b>	<b>56</b>
<b>FIG. 3.2-20 BANDGAP REFERENCE PROCESS VARIATION V.S TEMPERATURE VARIATION EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION.....</b>	<b>56</b>
<b>FIG. 3.2-21 BANDGAP REFERENCE VDDA VARIATION (2.5-3.5V) V.S TEMPERATURE VARIATION EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION.....</b>	<b>57</b>
<b>FIG. 3.2-22 BANDGAP START-UP TEST V.S PROCESS VARIATION EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....</b>	<b>57</b>
<b>FIG. 3.2-23 (A) VOLTAGE MODE BIAS CIRCUIT (B) CURRENT MODE BIAS CIRCUIT EXTRACTED FROM BEHZAD RAZAVI, "DESIGN OF ANALOG CMOS INTEGRATED CIRCUITS", MCGRAW-HILL COMPANIES, INC. 2004 [3] .....</b>	<b>58</b>
<b>FIG. 3.2-24 CURRENT MODE BIAS CIRCUITS EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION.....</b>	<b>58</b>
<b>FIG. 3.2-25 TIMING GENERATOR EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....</b>	<b>59</b>
<b>FIG. 3.2-26 TIMING GENERATOR SIMULATION IN MODELSIM(PRE-SIMULATION) EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....</b>	<b>59</b>
<b>FIG. 3.2-27 TIMING GENERATOR SIMULATION IN MODELSIM(POST-SIMULATION) EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....</b>	<b>60</b>
<b>FIG. 3.2-28 SINGLE PIXEL OPERATION SIGNALS WITH TIMING GENERATOR SIMULATION IN MODELSIM(PRE-SIMULATION) EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION.....</b>	<b>60</b>
<b>FIG. 3.2-29 SINGLE PIXEL OPERATION SIGNALS WITH TIMING GENERATOR SIMULATION IN MODELSIM(POST-SIMULATION) EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION.....</b>	<b>60</b>
<b>FIG. 4.1-1 MIX - MODE CIRCUIT DESIGN FLOW EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION.....</b>	<b>62</b>
<b>FIG. 4.2-1 PIXEL LAYOUT DIAGRAM: AREA 62.65 × 43.425 UM<sup>2</sup>, FILL FACTOR 34.2% EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION.....</b>	<b>62</b>
<b>FIG. 4.2-2 CDS LAYOUT DIAGRAM: C<sub>reg</sub> 200fF EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION.....</b>	<b>63</b>
<b>FIG. 4.2-3 TCDDA LAYOUT DIAGRAM EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION.....</b>	<b>63</b>
<b>FIG. 4.2-4 BANDGAP LAYOUT DIAGRAM EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION.....</b>	<b>64</b>
<b>FIG. 4.2-5 ANALOG PART LAYOUT DIAGRAM EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION.....</b>	<b>64</b>
<b>FIG. 4.2-6 FULL PLAN CHIP (SMART809) LAYOUT DIAGRAM EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....</b>	<b>65</b>
<b>FIG. 4.2-7 CHIP LAYOUT AND OUTPUT PIN DESCRIPTION EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....</b>	<b>66</b>
<b>FIG. 4.2-8 SIDE BRAZE 24-PIN LEAD BOUNDING DIAGRAM EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....</b>	<b>67</b>
<b>FIG. 4.2-9 CHIP PACKAGE DIAGRAM EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S )</b>	

COORDINATION .....	67
<b>FIG. 4.3-1 ELECTRICAL TEST PLATFORM ( FIRST STAGE )</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....	68
<b>FIG. 4.3-2 DISPLAY TEST PLATFORM ( SECOND STAGE )</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....	69
<b>FIG. 4.3-3 DIGITAL TEMPERATURE SENSOR BOARD IN 3D VIEW</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION.....	70
<b>FIG. 4.4-1 MICROGRAPH OF THE SMART809</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION.....	71
<b>FIG. 4.4-2 CIRCUIT DIAGRAM FOR THE TEST PLATFORM</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....	72
<b>FIG. 4.4-3 FLOOR PLAN FOR ELECTRICAL TEST PLATFORM</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....	72
<b>FIG. 4.4-4 FIBER OPTIC ILLUMINATOR MLC-150C</b> EXTRACTED FROM MOTIC COOPERATION < 10 >.....	73
<b>FIG. 4.4-5 OUTPUT SIGNAL WHILE ILLUMINATION ON 100,000 LUX</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION.....	73
<b>FIG. 5.2-1 CMOS SENSOR APPLICATION &amp; TECHNOLOGY</b> EXTRACTED TSMC CMOS IMAGE SENSOR TECHNOLOGY INFORMATION DOCUMENT 【18】 .....	74
<b>FIG. 5.2-2 CAPSULE ENDOSCOPY ( A ) OUTLOOK ( B ) ARCHITECTURE</b> EXTRACTED MAYO CLINIC INC. " CAPSULE ENDOSCOPY", MAYO CLINIC MEDICAL SERVICE< 9 >.....	75
<b>FIG. A-1 CALIBRE DRC RESULTS</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....	80
<b>FIG. A-2 CALIBRE DRC SUMMARY</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....	80
<b>FIG. A-3 THE EMAIL ANSWER FOR AMS.1.M4 DRC ERROR, JULY 27</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION.....	81
<b>FIG. A-4 THE EMAIL ANSWER FOR LATI.3 DRC ERROR, OCTOBER 26</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION.....	82
<b>FIG. B-1 CALIBRE LVS RESULTS</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....	83
<b>FIG. B-2 CALIBRE LVS LAYOUT MATCH SMILE FIGURE</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....	83
<b>FIG. E-1 未添加溫度補償電路時，增益隨溫度之變化圖</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....	89
<b>FIG. E-2 添加溫度補償電路時，增益隨溫度之變化圖</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....	90
<b>FIG. E-3 可提供 1V 之參考電壓，溫度變化係數 9.6PPM/°C( 從 0°C~125°C 計算 )</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....	90
<b>FIG. E-4 MICRON MT9V022 車用影像感測器 DATASHEET</b> EXTRACTED FROM MICRON MT9V022 AUTOMOTIVE CMOS IMAGE SENSOR DATASHEET 【19】 .....	93

## Content of Table

<b>TABLE 2.1.1-1 VISIBLE LIGHT'S FREQUENCY AND WAVELENGTH</b> EXTRACTED FROM <i>PHYSICS DEMO LAB IN NTNU &lt; 2 &gt;</i> .....	9
<b>TABLE 2.1.2-1 MAIN PROPERTIES OF THE DIFFERENT PHOTO-DETECTORS AVAILABLE IN A STANDARD CMOS PROCESS</b> EXTRACTED FROM TAMÁS ROSKA, ÁNGEL RODRÍGUEZ – VÁZQUEZ, "TOWARDS THE VISUAL MICROPROCESSOR – VLSI DESIGN AND THE USE OF CELLULAR NEURAL NETWORK UNIVERSAL MACHINES" CHAPTER 5 LIGHT-SENSITIVE DEVICES IN CMOS PAGE 189 <b>[4]</b> .....	22
<b>TABLE 2.1.2-1 COMPARISON TABLE ON FEATURE AND PERFORMANCE ON CCD &amp; CMOS</b> EXTRACTED FROM 米本和也 原著；陳榕庭、彭美桂 翻譯，“CCD/CMOS 影像感測器之基礎與應用”，全華科技圖書股份有限公司，2005 年初版。 <b>[1]</b> .....	26
<b>TABLE C-1 CHIP PINS INSTRUCTIONS AND SIGNAL ILLUSTRATION</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION.....	84
<b>TABLE C-2 CHIP SPEC TABLE</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .	84
<b>TABLE E-1 預計規格列表</b> EXTRACTED FROM THIS THESIS' (SHAO-HANG HUNG. 'S ) COORDINATION .....	92

