Chapter 3
Wide Dynamic Range & Temperature Compensated Gain CMOS Image Sensor in Automotive Application

Like the introduction said, we can recognize the problem would be suffered on image sensor in automotive application. We can summarize them and define the goal of application in three points. First, we should overcome the abominable environment that automotive applications have to concerned, like high contrast illuminations, inferring image quality affected by temperature variation. Second, in order to support certain automotive algorithms, like digital image stable technique, lane line detection, vehicle side collision warning system, etc, we need an exactly image which no longer define by our eyes. Third, for the reason to reduce the operation loading of automotive embedded processor, certain effects which both could be solved on digital signal processing or analog circuits, have to process on analog part. That makes system can focus its performance on important judgment.

3.1 System Architecture

The system consists of six parts shown in Fig. 3.1-1. They are active pixel sensor with analog memory (AMAPS), column correlated double sampling circuit (CDS), differential difference amplifier with temperature compensate circuit (TMDDA), bandgap voltage reference, large bias circuit, and timing generator circuit (TG).

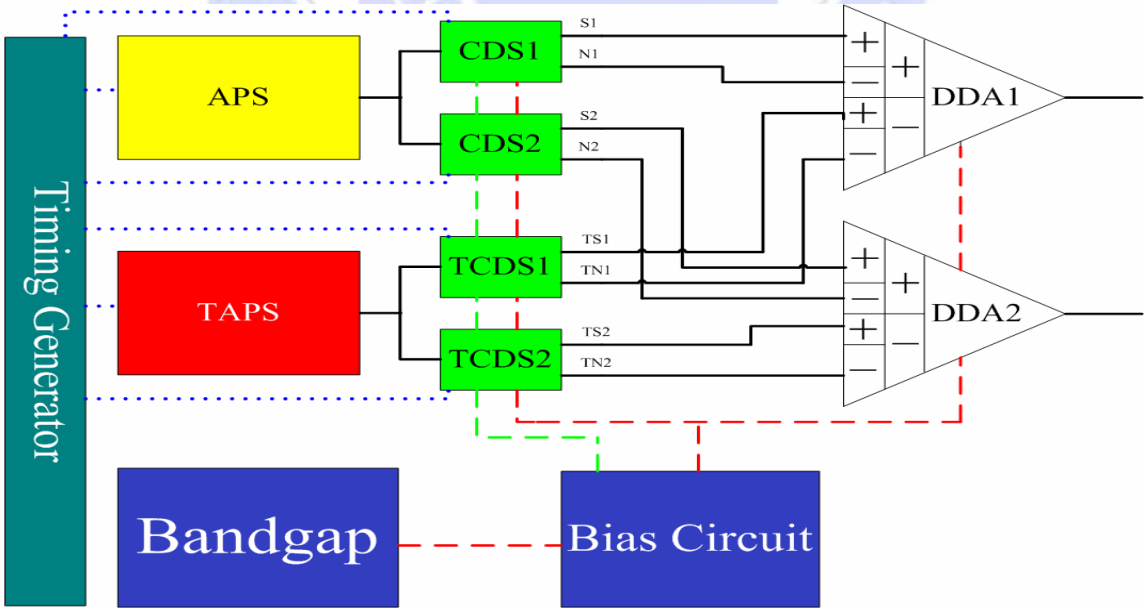


Fig. 3.1-1 System Architecture

extracted from this thesis'（Shao-Hang Hung. 's ）coordination

We want to get the pure signal transfer from light, instead of thermal signal, but both illumination and thermal may cause discharge of photo detector, like Eq.（34）shows. If we take cover at the same sensor architecture on the same chip, the pure thermal signal can be transferred like Eq.（35）. Take the difference from those two signals as Eq.（36）, we can finally get the pure illumination signal. In addition of the original signal processing, pre-charge signal minus illuminated signal, we need double difference on the system architecture.

$$Signal_{APS} = Signal_{illumination} + Signal_{Thermal}, \quad (34)$$

$$Signal_{TAPS} = Signal_{Thermal}, \quad (35)$$

$$Signal_{APS} - Signal_{TAPS} = Signal_{illumination}, \quad (36)$$

Concerning the application requirement, we've designed a bandgap reference to supply a steady voltage reference. The bias circuit has also been designed for large analog circuits. Finally, the controlling time generated by digital circuits. We would introduce them on next sections.

3.2 Circuit Design

3.2.1 Analog Memory in Active Pixel Sensor （AMAPS）

The research in analog memory in active pixel sensor has not going down after Yoshinori's paper [8]. In 2005, S. Sugawa's team present a serious paper "A 100dB Dynamic Range CMOS Image Sensor Using a Lateral Overflow Integration Capacitor" [31][32][33], which achieves no degradation of the sensitivity in low light, keeps the sensitivity in very bright light and realizes high S/N in low and very bright lights. Within the controlling of analog memory in active pixel sensor, we can get the two kinds of charged electron numbers to satisfy different intensity of photocurrent. Fig. 3.2-1 shows the pixel schematic diagram, and Fig. 3.2-2 is the potential diagram. The standard correlated double sampling circuit has been used to avoid the mistake in signal fetch, and we would discuss it on section 3.2.2. The two channel CDS circuit supposed the sensor can generate two exposure times. The overall architecture demonstrated in Fig. 3.2-3. Fig. 3.2-4 to Fig. 3.2-10 are the simulation chart within architecture as Fig. 3.2-1. To ensure the sensitivity, we replace the photo detector in phototransistor which has higher photocurrent than photodiode as mention in Chapter 2. We have successfully verify their architecture in wide dynamic range function.

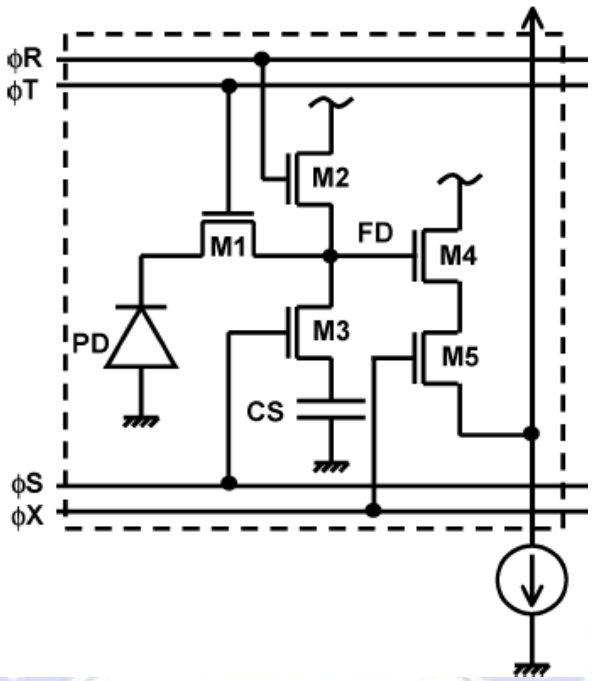


Fig. 3.2-1 Pixel schematic diagram（FD reset type sensor）

extracted from N. Akahane, S. Sugawa, S. Adaci, K. Mori, T. Ishiyuki, K. Mizobuchi, "A sensitivity and linearity improvement of a 100-dB dynamic range CMOS image sensor using a lateral overflow integration capacitor", in IEEE JSSC, Vol. 41, Issue 4, pp.851~858, April 2006.[33]

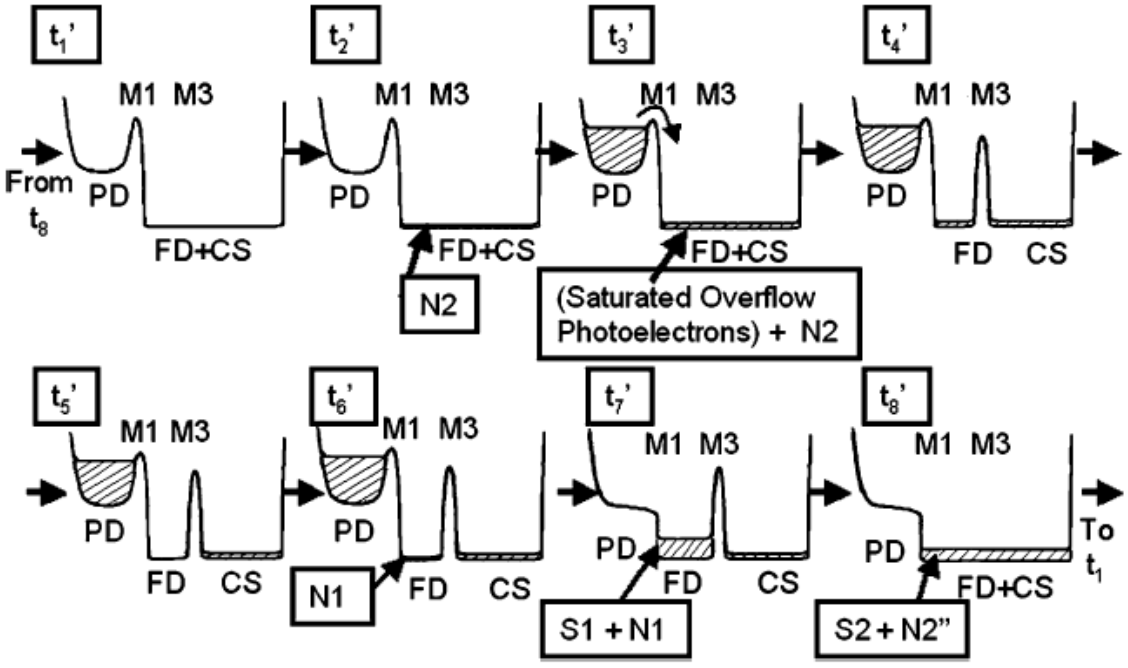


Fig. 3.2-2 Potential diagram（FD reset type sensor）

extracted from N. Akahane, S. Sugawa, S. Adaci, K. Mori, T. Ishiyuki, K. Mizobuchi, "A sensitivity and linearity improvement of a 100-dB dynamic range CMOS image sensor using a lateral overflow integration capacitor", in IEEE JSSC, Vol. 41, Issue 4, pp.851~858, April 2006.[33]

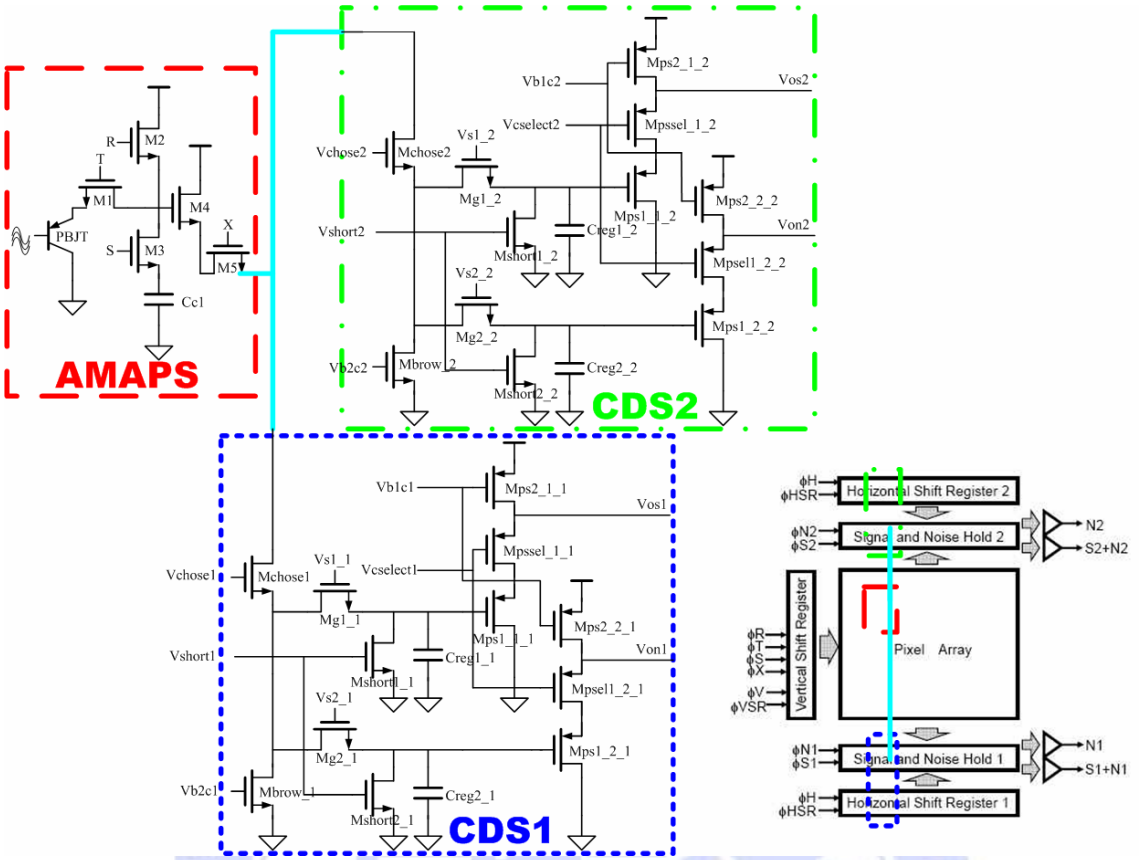


Fig. 3.2-3 APS + Analog Memory+ CDS Circuits diagram

extracted from this thesis'（Shao-Hang Hung. 's ）coordination

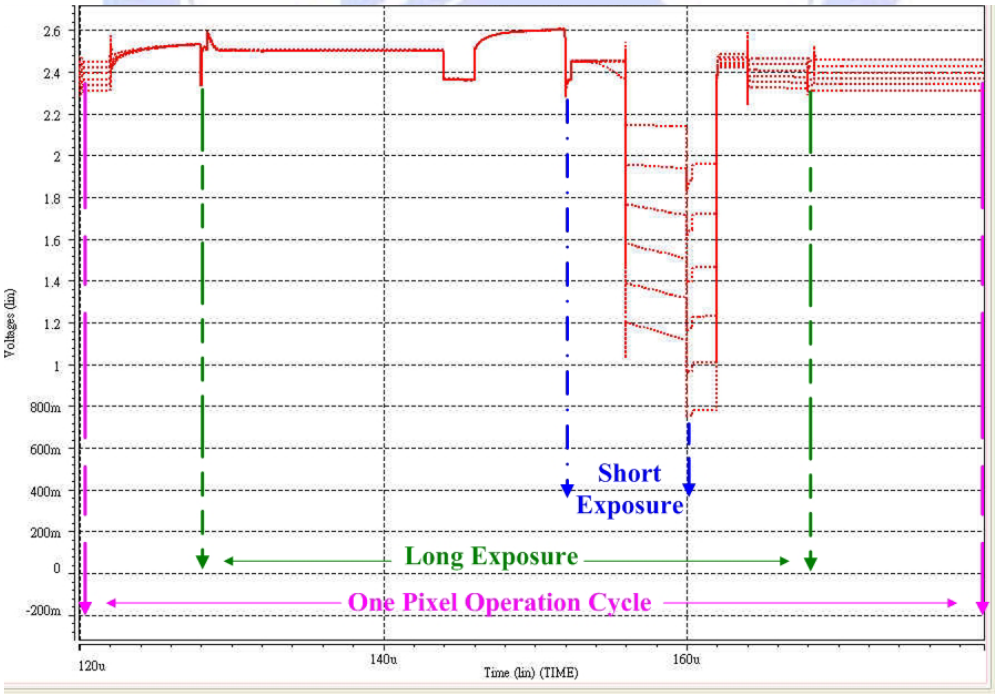


Fig. 3.2-4 Simulation of sensor output signal in voltage variation

extracted from this thesis'（Shao-Hang Hung. 's ）coordination

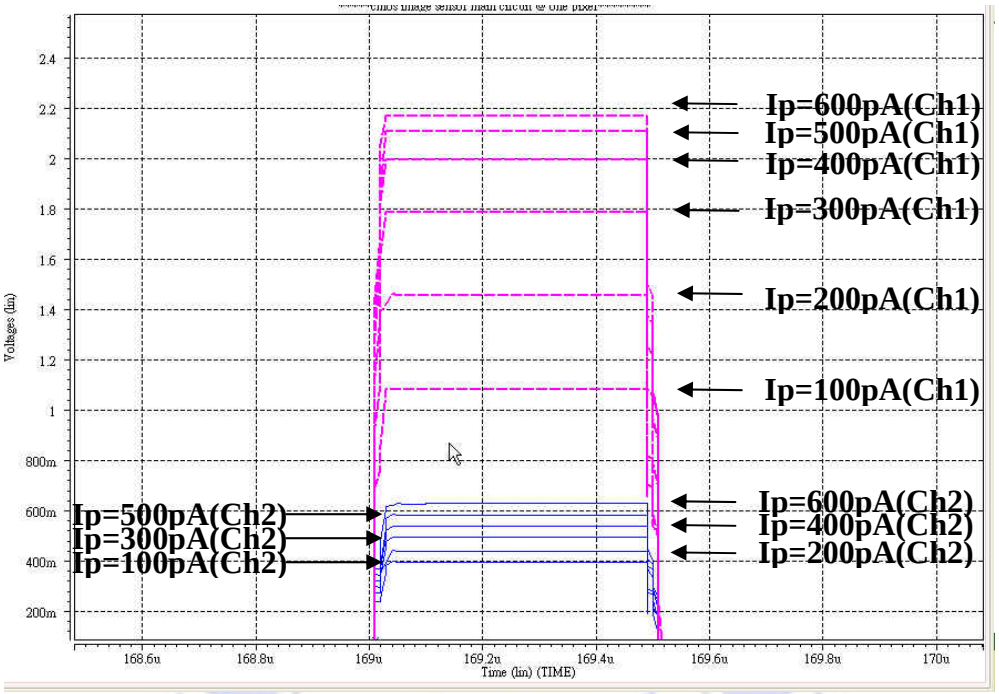


Fig. 3.2-5 Simulation of CDS output signal in voltage variation with different incident light

extracted from this thesis'（Shao-Hang Hung. 's ）coordination

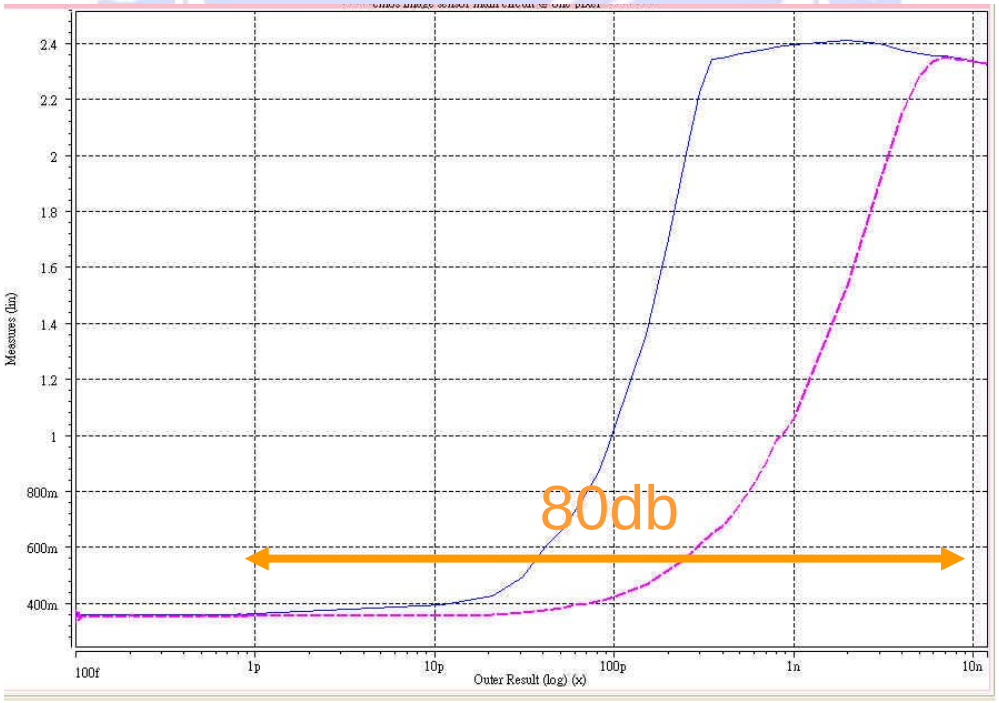


Fig. 3.2-6 Dynamic Range Simulation

extracted from this thesis'（Shao-Hang Hung. 's ）coordination

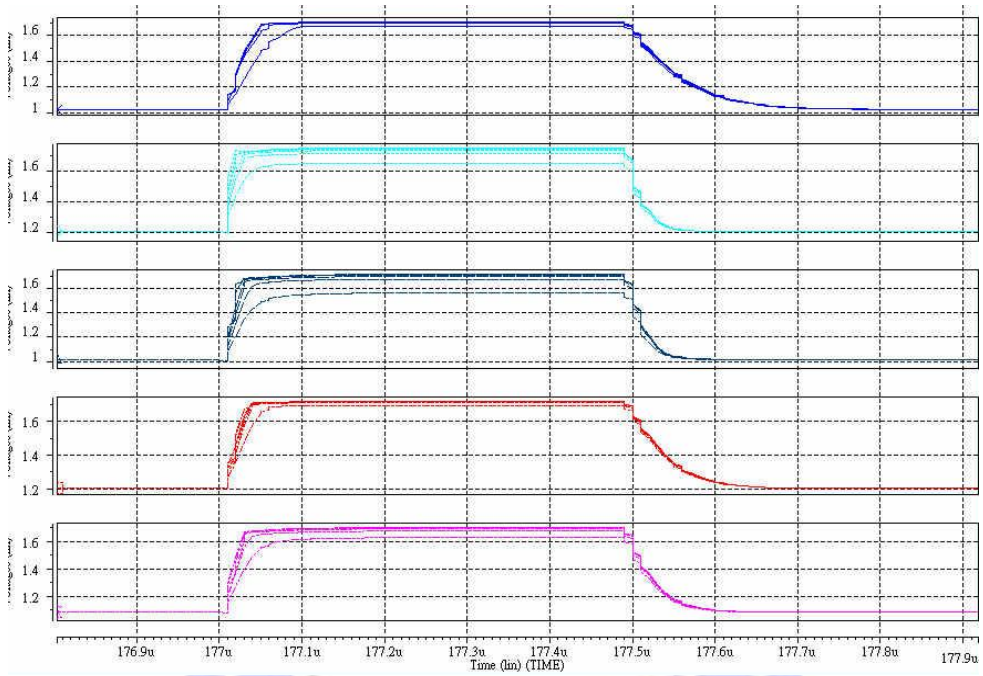


Fig. 3.2-7 CDS output voltage v.s process variation in 90% VDD
extracted from this thesis'（Shao-Hang Hung. 's ）coordination

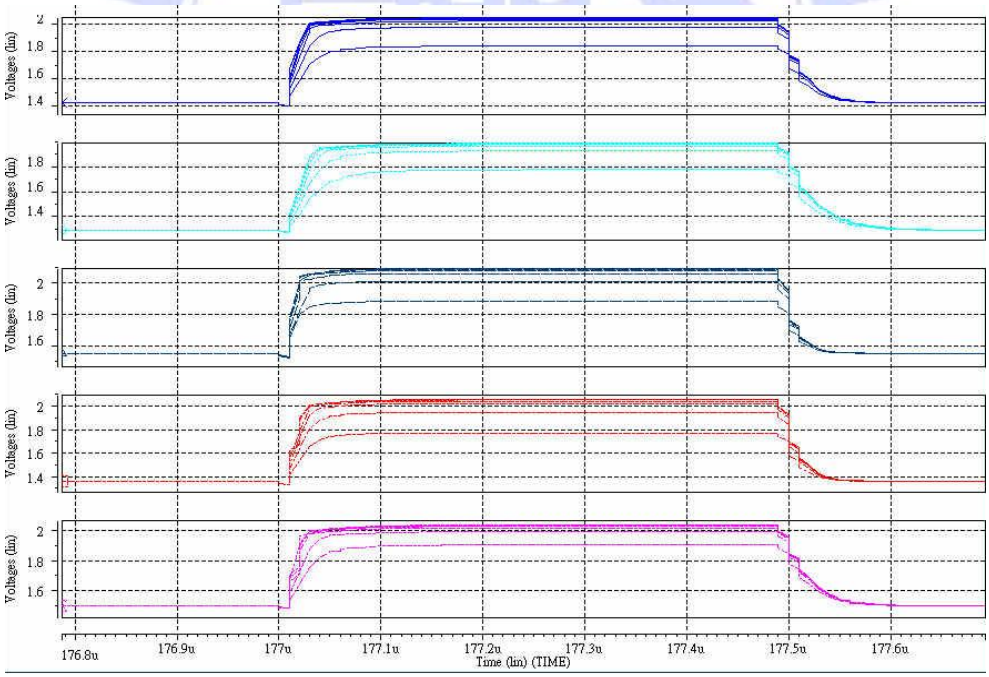


Fig. 3.2-8 CDS output voltage v.s process variation in 110% VDD
extracted from this thesis'（Shao-Hang Hung. 's ）coordination

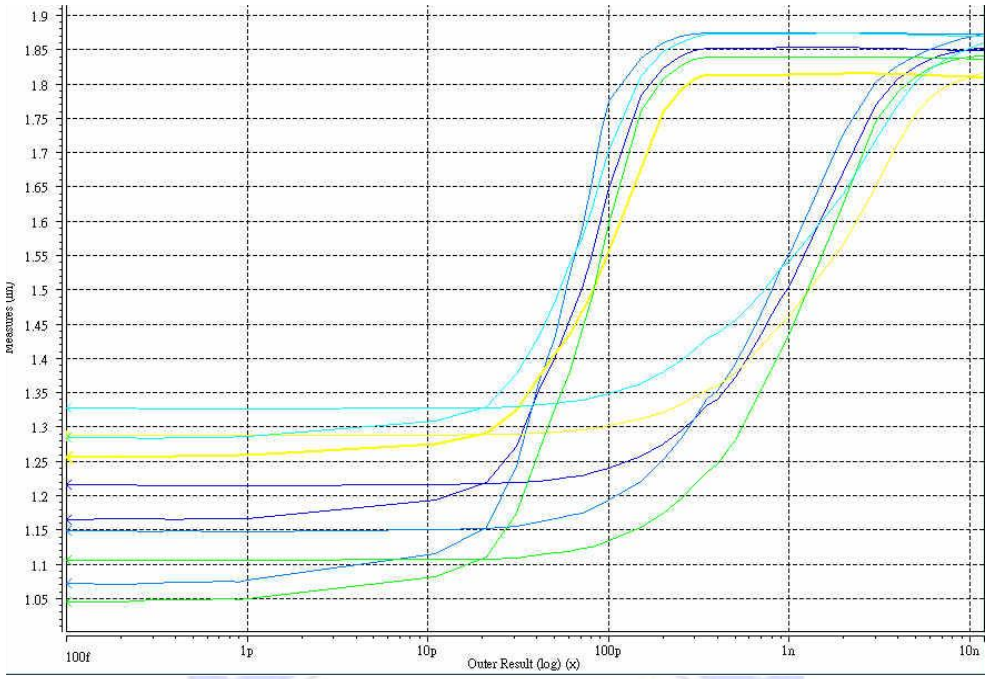


Fig. 3.2-9 Dynamic Range v.s process variation
extracted from this thesis'（Shao-Hang Hung. 's ）coordination

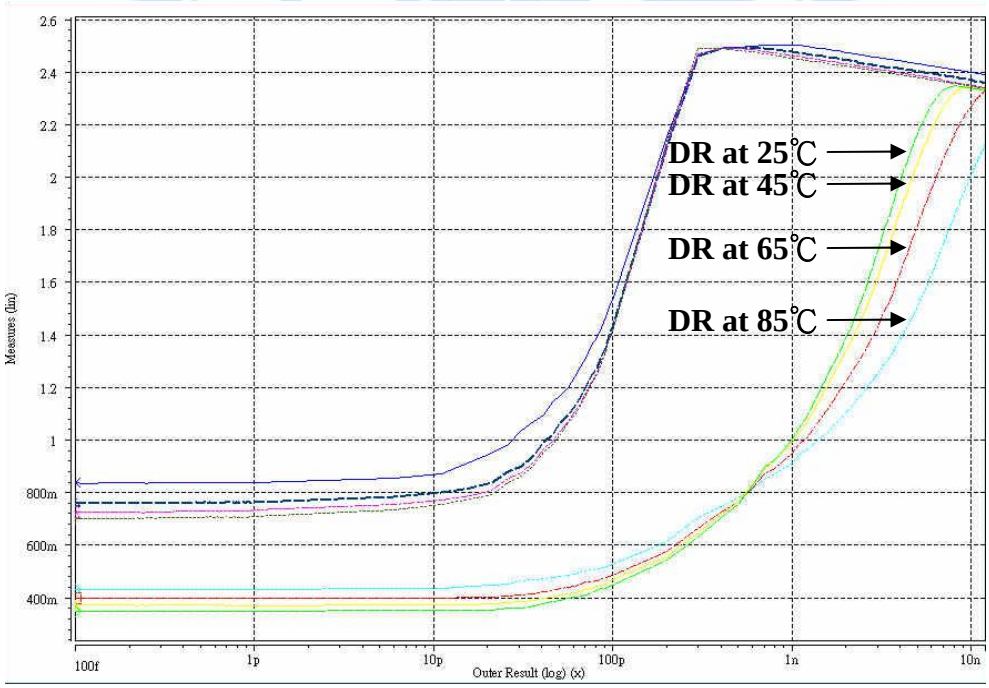


Fig. 3.2-10 Dynamic Range v.s temperature variation(25°C ,45°C ,65°C, 85°C)
extracted from this thesis'（Shao-Hang Hung. 's ）coordination

On the Fig.3.2-10, we found an interesting result which never been discussed in paper. As the result we introduced in chapter 1, M. Schanz et al declare in their paper" A High-Dynamic-Range CMOS Image Sensor for Automotive Applications" [5], which dynamic range would decay amount 10dB when heating from 65˚C to 85˚C in general

3T APS architecture. Our result presented on Fig. 3.2-10 shows that AMAPS architecture has effectively defense the dynamic range decay in heating system.

On paper published by N. Akahane et al. "*A sensitivity and linearity improvement of a 100-dB dynamic range CMOS image sensor using a lateral overflow integration capacitor*" [33], the dynamic range（DR） can define as Eq. （37）

$$DR = 20\log\left(\frac{V_{SAT2}\cdot\dfrac{C_{FD}+C_{CS}}{C_{FD}}}{V_{\eta}}\right), \tag{37}$$

where the essential approaches to extend the dynamic range are a higher S2 saturation voltage V_{SAT2}, with a higher ratio of $\left(C_{FD}+C_{CS}\right)/C_{FD}$ and a lower residual noise V_{η}. V_{η} has the relation with Q_{η}, which corresponds to the input conversion charges, in the formula as $V_{\eta}=qQ_{\eta}/C_{FD}$. Assume the swell factor α, and linear swell Eq.（38）

$$\Delta L = \alpha L \Delta T, \tag{38}$$

where the ΔL variation length of material, L is the length in original standard, and ΔT is the temperature variation. The area swell Eq.（39） could be inference as

$$\Delta A \approx 2\Delta L = 2\alpha L \Delta T, \tag{39}$$

The capacitance with swell function should related with area size that

$$C = \frac{\varepsilon_r\left(1+2\alpha\Delta T\right)A}{d}, \tag{40}$$

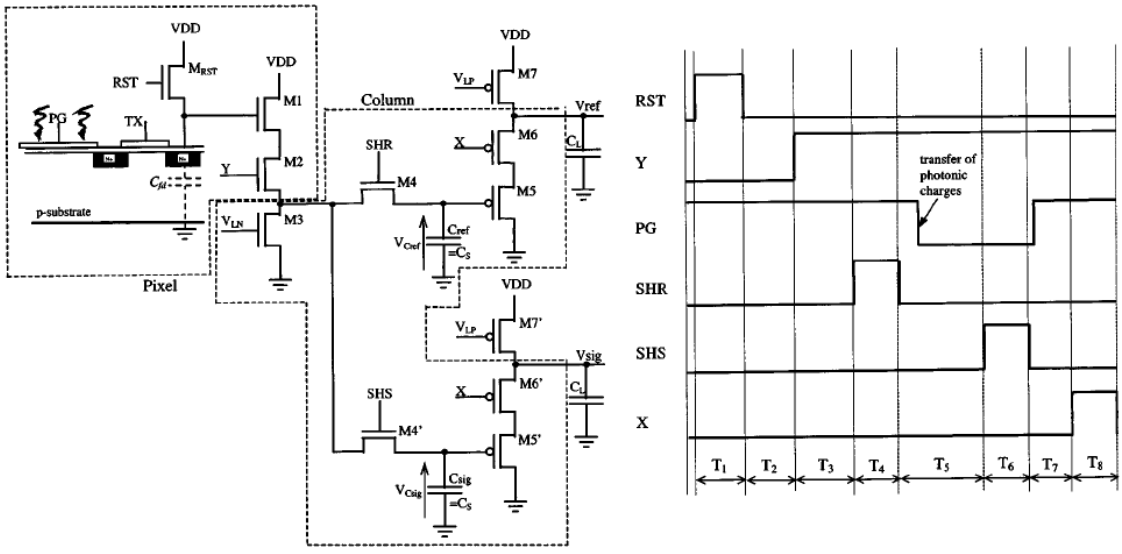
where ε_r is the relative permittivity and general value $\varepsilon_r \approx \varepsilon_0 \approx 8.84\cdot10^{-12}\left(F/m\right)$. For the different swell factor in silicon $\alpha_{Si}\approx 5\times10^{-7}$; in poly1-poly2 capacitance $\alpha_{C_{PO1-PO2}}\approx 2.1558\times10^{-5}$; in and in aluminum $\alpha_{Al}\approx 2.07\times10^{-5}$. Set these parameter into Eq.（37）, that is

$$DR = 20\log\left(\frac{V_{SAT2}\cdot\left(1+\delta\dfrac{\left(1+2\alpha_{CS}\Delta T\right)}{\left(1+2\alpha_{FD}\Delta T\right)}\right)}{V_{\eta}}\right), \tag{41}$$

where $\delta = (d_{FD}/d_{CS})$, if we choose certain material which made $\alpha_{CS} > \alpha_{FD}$, the DR would increase with heating system. On VLSI technology, we can easily find the material match the characteristic.

3.2.2 Correlated Double Sampling Circuit

On CDS circuit, we've taken the architecture which presented by Yavuz Değerli in 2000,"Analysis and Reduction of Signal Readout Circuitry Temporal Noise in CMOS Image Sensors for Low-Light Levels" [36]. The architecture has been the popular ones, with both low-frequency noise and thermal noises are considered. The reset noise, the influence of floating diffusion capacitance on output noise and the detector charge-to-voltage conversion gain are also considered. Their result really helpful for our design and the Fig. 3.2-3 also demonstrate the CDS circuit.



（a） （b）

Fig. 3.2-11 （a）Readout circuit of CMOS photo-gate active pixel image sensor （b）related operation timing

extracted from Y. Değerli, F. Lavernhe, P. Magnan, J. A. Farré,*" Analysis and Reduction of Signal Readout Circuitry Temporal Noise in CMOS Image Sensors for Low-Light Levels"*, *IEEE Trans. On Electron Devices*, Vol. 47, No.5, pp. 949~962, May 2000.*[36]*

3.2.3 Temperature Compensated Differential Difference Amplifier（TCDDA）

In Section 3.1, we have declared that we need double difference function in system architecture. We took the basic amplifier architecture published by Hussain, 2000,"A

CMOS Fully Balanced Differential Difference Amplifier and Its Applications" [9]. We basis from the single output ended differential difference amplifier, reduce the gain stage since the gain do not need very high in CMOS Image Sensor's application. We only used transconductance g_m in differential pair as the main gain stage. As the section 2.6 discussed, temperature variation would influence the performance of the amplifier. Focus on compensation circuit in input stage, combination the design theorem of presented by J. A. S.Dias"CMOS Temperature-Stable Linearised Differential Pair", 1992 [10]. Thus, in order to ensure the circuit would successfully drive the enough output impedance, we set the parameters which as the values in the oscilloscope input impedance and designed a Class A output stage. Therefore the Class A output stage is the most energy exhausted stage in overall system. Fig. 3.2-12 is the architecture of Temperature Compensated Differential Difference Amplifier(TCDDA). Fig. 3.2-12~17 are the other simulation which is needed for amplifier design. Finally, our result in TCDDA with gain variation 135.662ppm/˚C(0°C~125°C),amplifier gain in 12.529dB at 25°C, Phase Margin in 97.13°

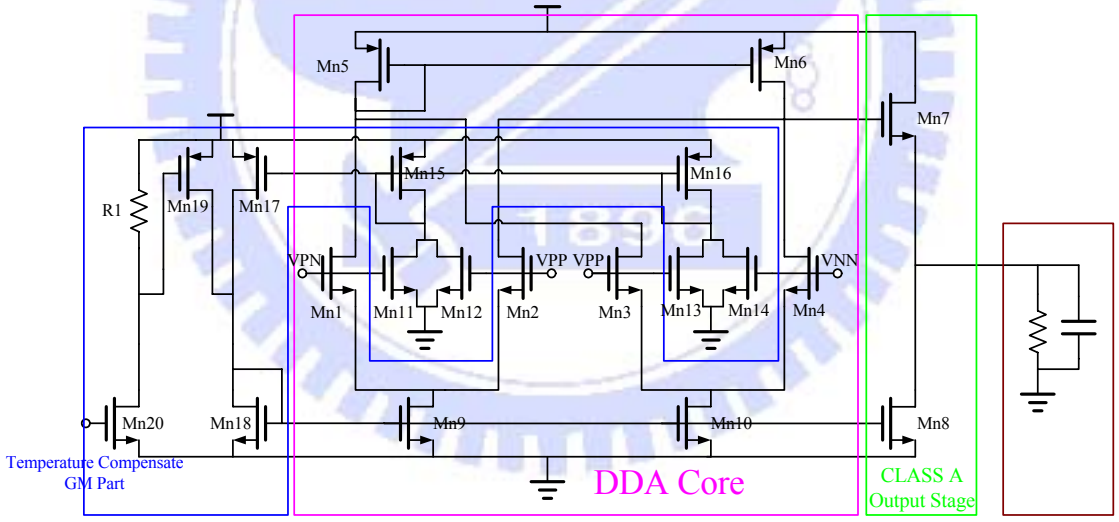


Fig. 3.2-12 Temperature Compensated Differential Difference Amplifier circuit
extracted from this thesis'（Shao-Hang Hung. 's ）coordination

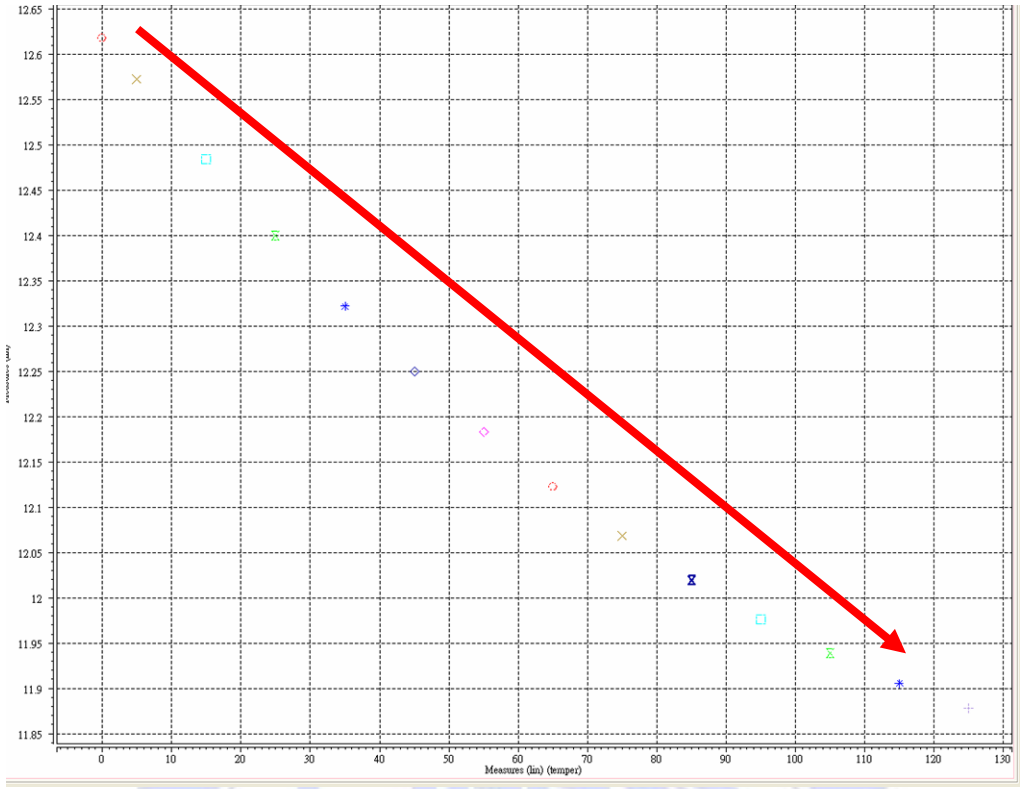


Fig. 3.2-13 Gain variation without temperature compensation circuit, gain decrease 0.69dB（0˚C~125˚C）,average variation 661.437ppm/˚C

extracted from this thesis'（Shao-Hang Hung. 's ）coordination

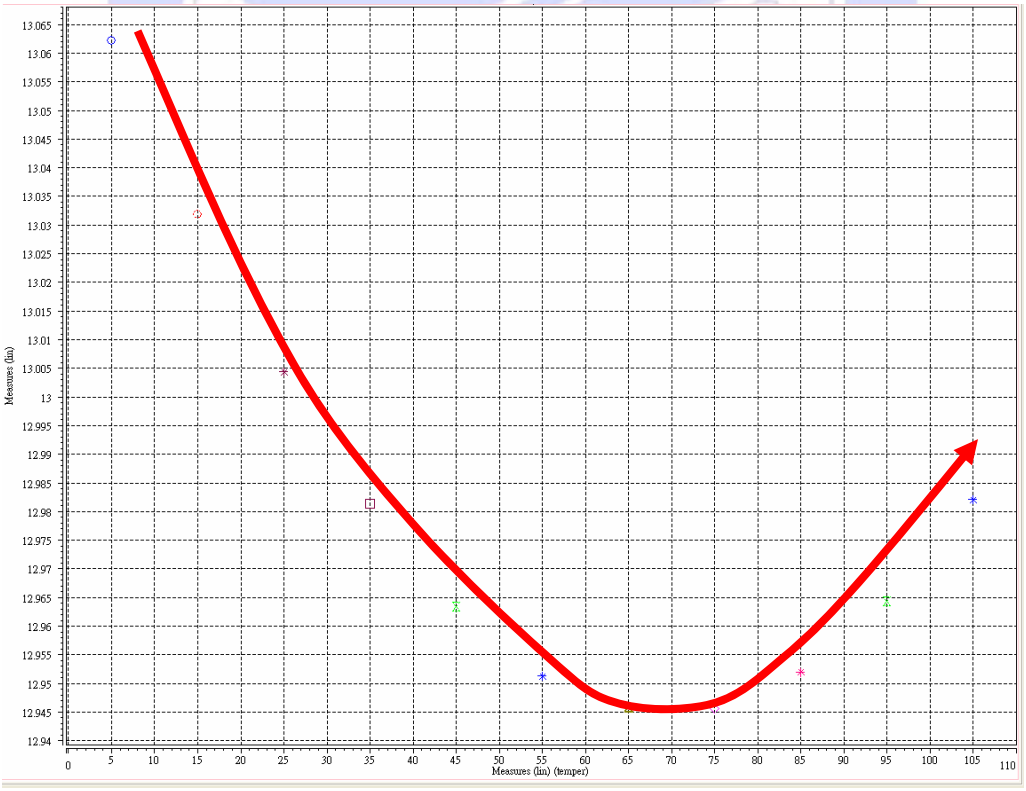


Fig. 3.2-14 Gain variation with temperature compensation circuit, gain decrease 0.117dB（0˚C~125˚C）,average variation 135.612ppm/˚C

extracted from this thesis'（Shao-Hang Hung. 's ）coordination

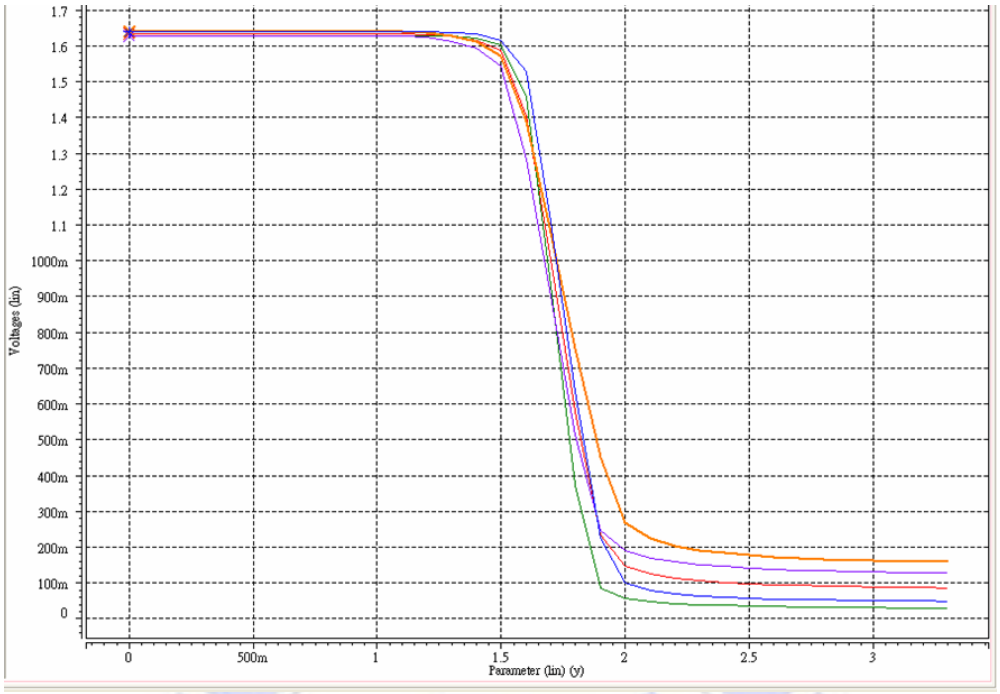


Fig. 3.2-15 TCDDA Transfer Linearity v.s Process Variation (TT, FF, SS, SF, FS)
extracted from this thesis'（Shao-Hang Hung. 's ）coordination

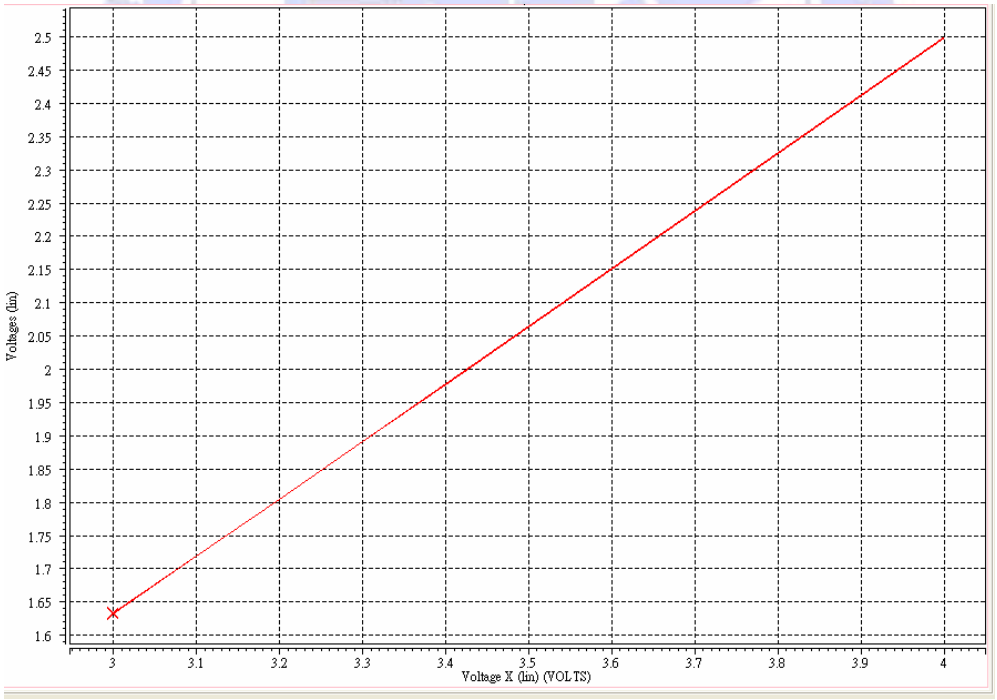


Fig. 3.2-16 TCDDA output voltage level v.s VDDA Variation, Temperature Variation （almost can't recognized the temperature variation effect）
extracted from this thesis'（Shao-Hang Hung. 's ）coordination

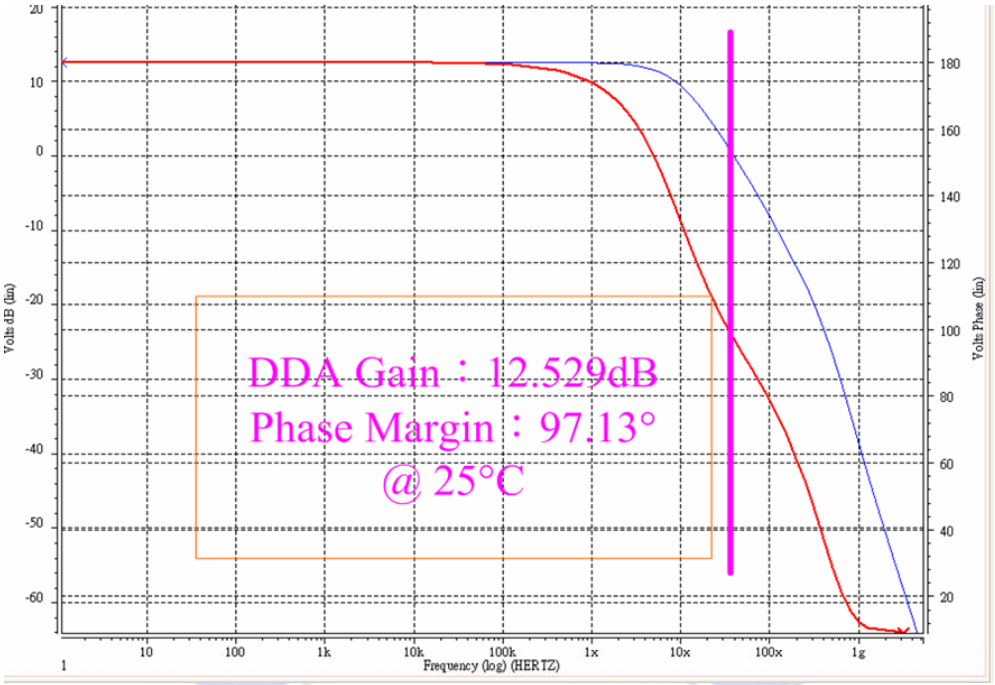


Fig. 3.2-17 TCDDA frequency response within 12.529dB@25˚C, PM 97.13°

extracted from this thesis'（Shao-Hang Hung. 's ）coordination

3.2.4 Bandgap Reference

The thesis refers to K. N. Leung's paper "A Sub-1-V 15-ppm/˚C CMOS Bandgap Voltage Reference Without Requiring Low Threshold Voltage Device"[11], 2002. The circuit provide 1v reference voltage, variation in 9.6ppm/˚C（0˚C~125˚C）

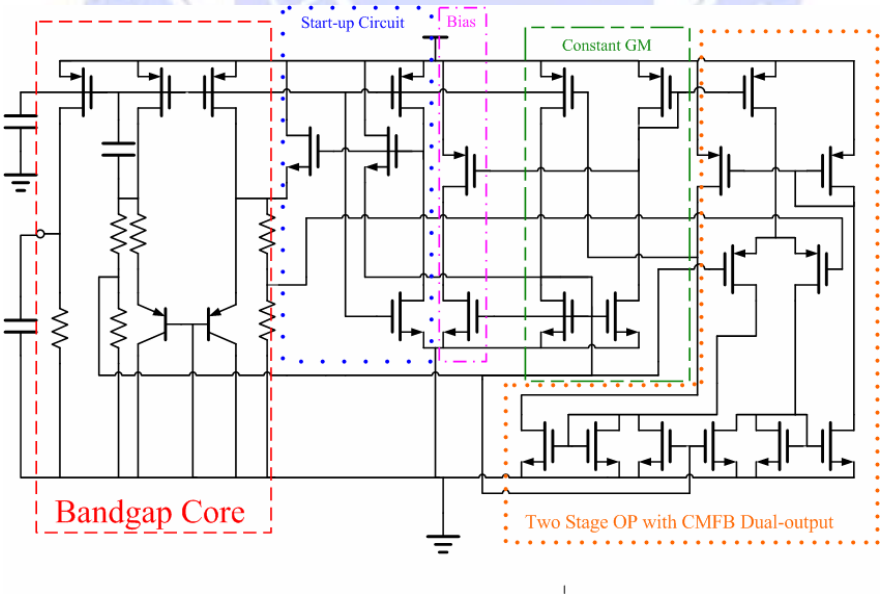


Fig. 3.2-18 low voltage bandgap voltage reference

extracted from K. N. Leung, P. K. T. Mok, "A Sub-1-V 15-ppm/°C CMOS Bandgap Voltage Reference Without Requiring Low Threshold Voltage Device", in IEEE JSSC, Vol 37, No.4, pp., pp.526~530, April 2002.[11]

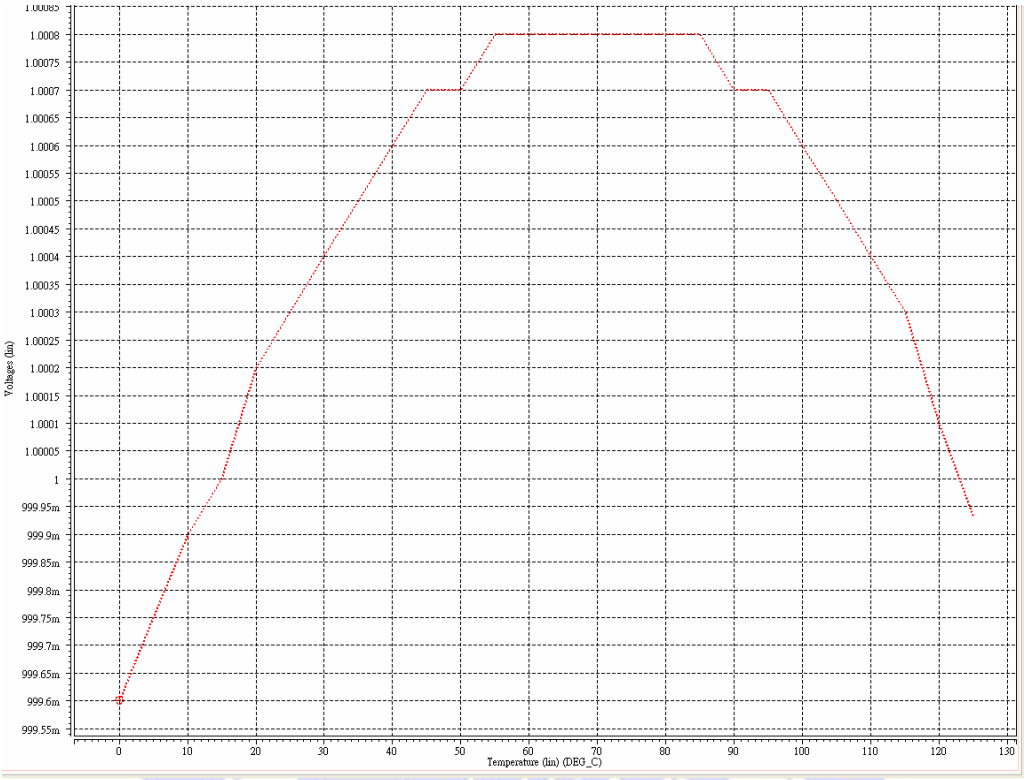


Fig. 3.2-19 1V Bandgap reference voltage, variation in 9.6ppm/°C（0°C~125°C）

extracted from this thesis'（Shao-Hang Hung. 's ）coordination

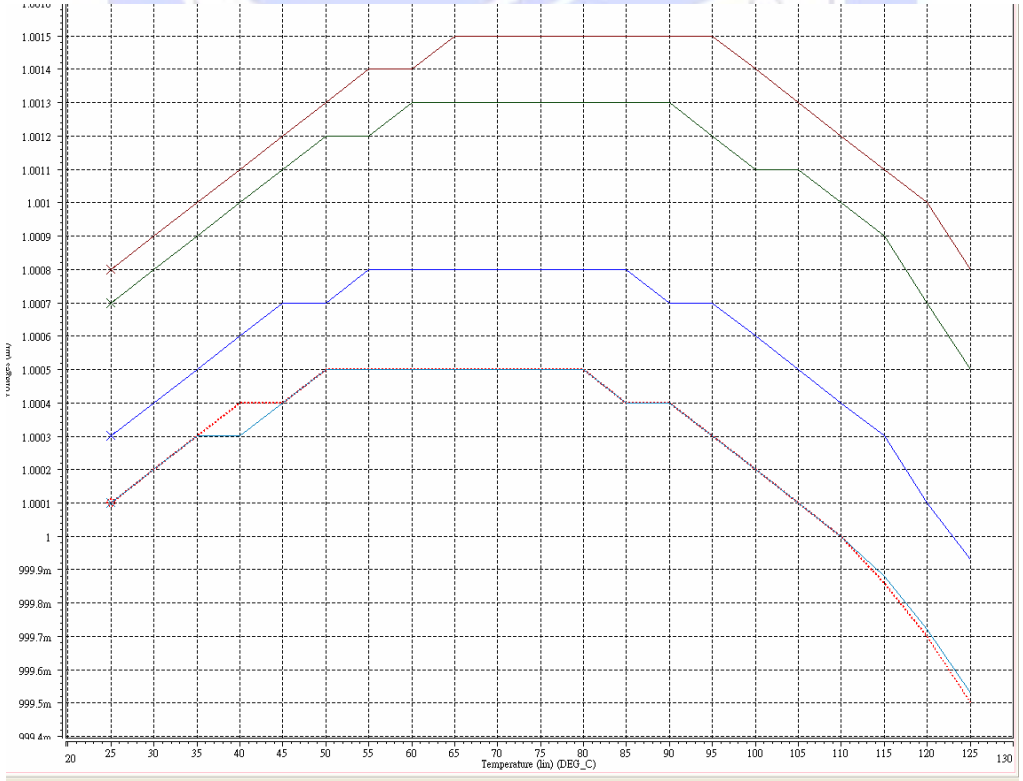


Fig. 3.2-20 Bandgap reference process variation v.s temperature variation

extracted from this thesis'（Shao-Hang Hung. 's ）coordination

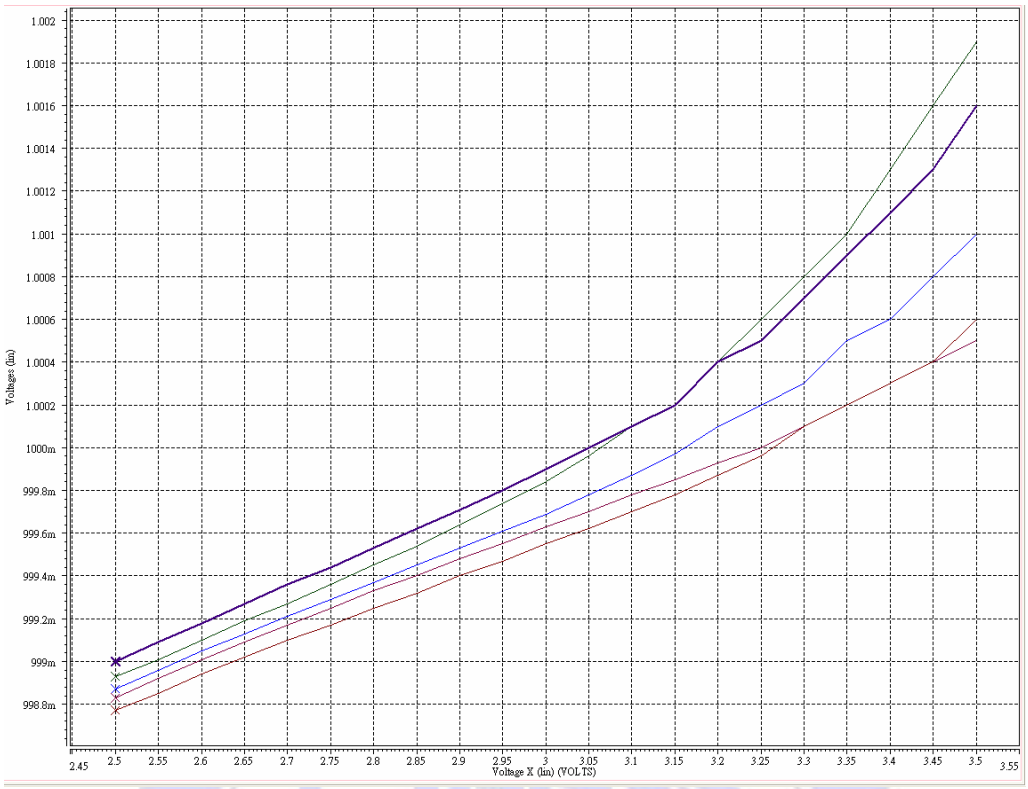


Fig. 3.2-21 Bandgap reference VDDA variation （2.5-3.5V）v.s temperature variation

extracted from this thesis'（Shao-Hang Hung. 's ）coordination

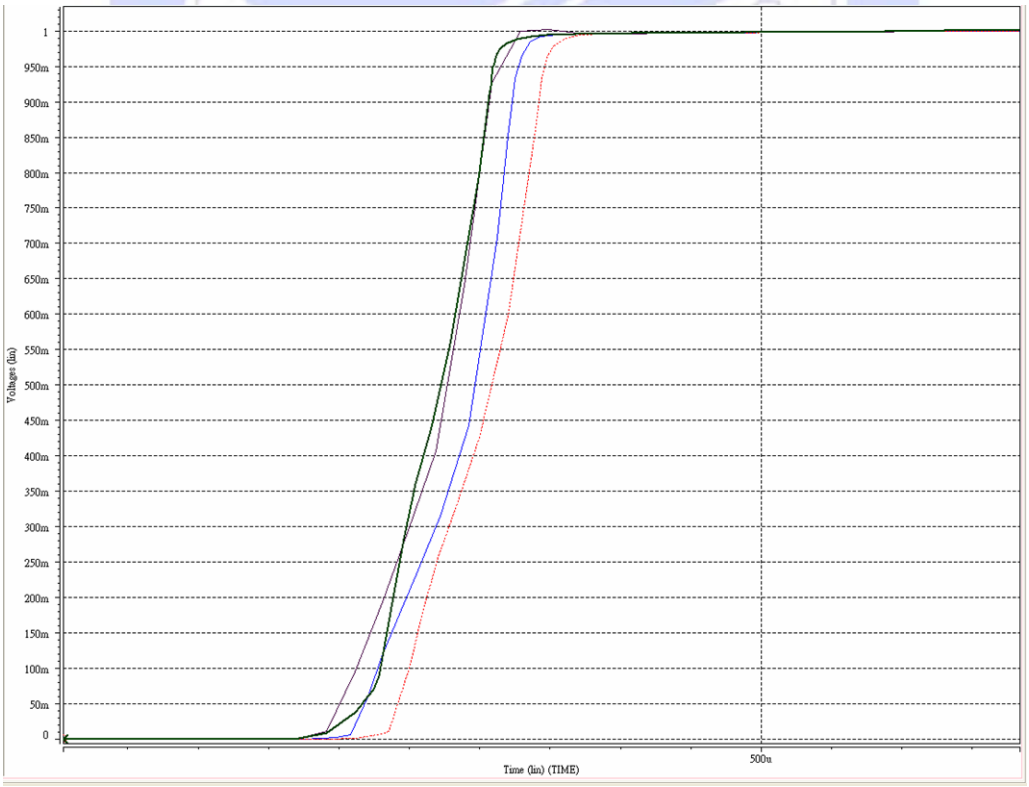
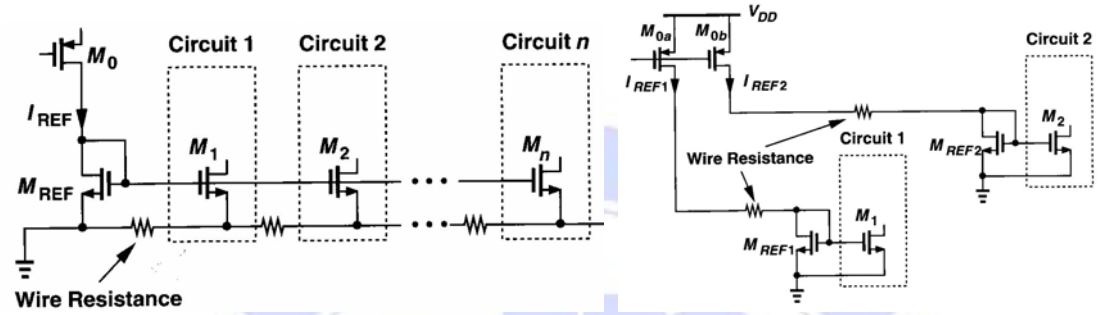


Fig. 3.2-22 Bandgap start-up test v.s process variation

extracted from this thesis'（Shao-Hang Hung. 's ）coordination

3.2.5 Large Analog System Bias Circuit【3】

Since the full circuit would comprise very large chip area, if we use the traditional voltage mode bias current as Fig. 3.2-23, the responsibility of circuit would delay for the wire resistance. The error could be resolved in current mode to transfer bias signal with less delay and lower power consumption since the current has less defect on wire resistance. Fig. 3.2-24 shows the current mode bias circuit in the thesis' chip, where the bias root gathered up together and transfer the current to each branch component.



（a） （b）

Fig. 3.2-23 （a）voltage mode bias circuit（b）current mode bias circuit
extracted from Behzad Razavi, "Design of Analog CMOS Integrated Circuits", McGraw-Hill Companies, Inc. 2004【3】

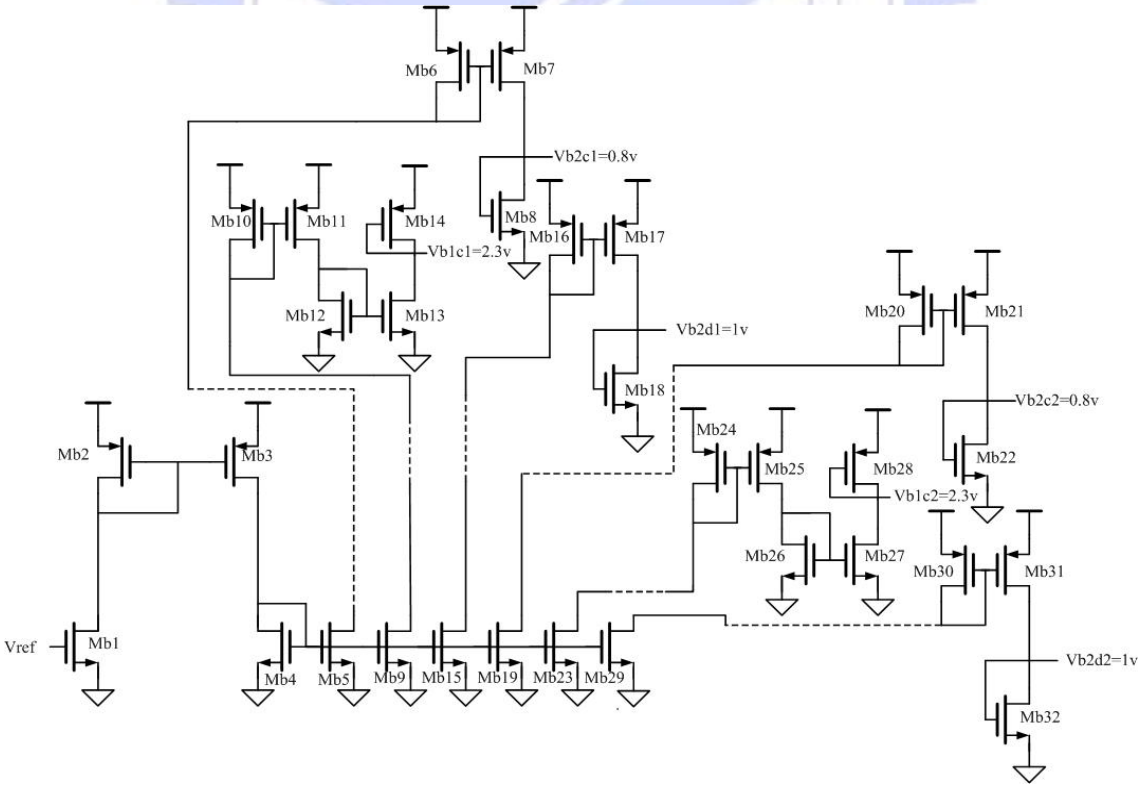


Fig. 3.2-24 Current mode bias circuits
extracted from this thesis'（Shao-Hang Hung. 's ）coordination

3.2.6 Timing Generator

The most difference between CCD technology and CMOS technology is integrated ability. CCD needs another Digital Signal Processor to drive the change of image array, and CMOS can integrate timing generator digital circuit on the same chips. It can reduce the input signal only need reset and clock cycle. Since the variations in each pixel or CDS are the same, we can generate the control signal in the same counter with a multiplexer to achieve each row and column in HDL language writing. Fig. 3.2-24 demonstrated the block diagram of Timing Generator.

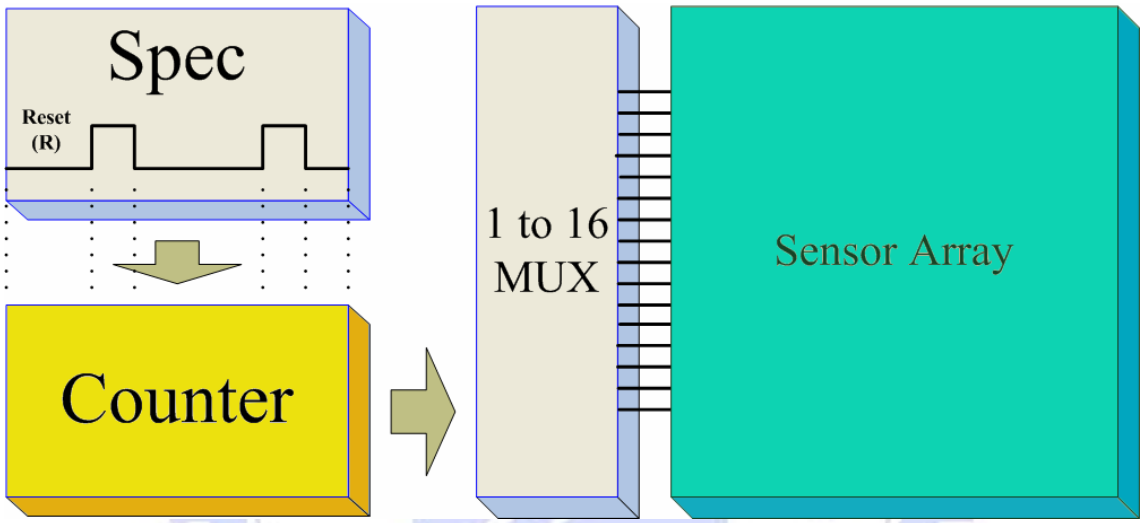


Fig. 3.2-25 Timing Generator
extracted from this thesis'（Shao-Hang Hung. 's ）coordination

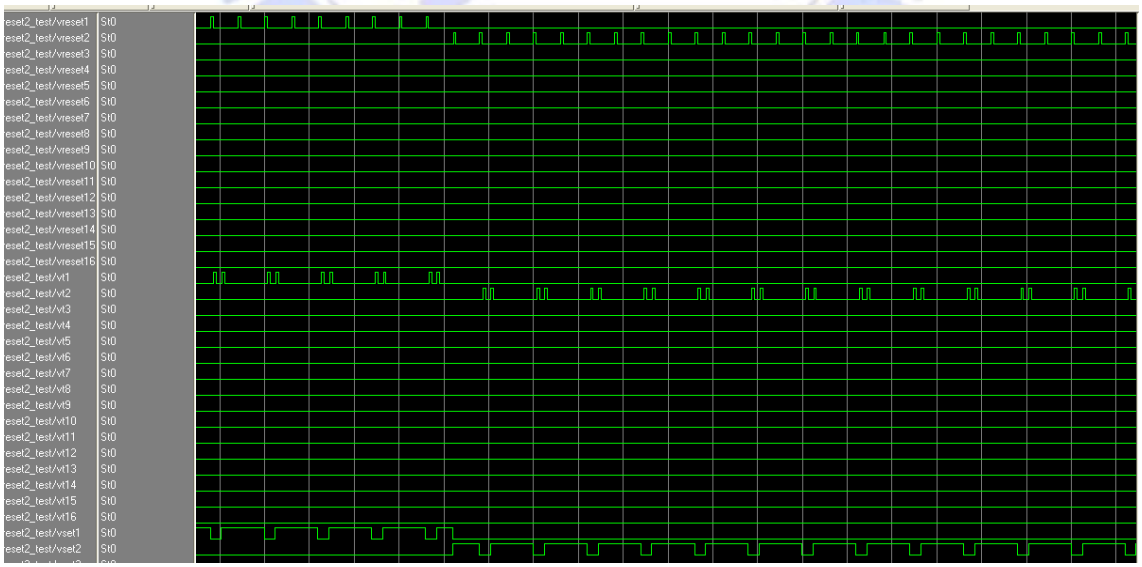


Fig. 3.2-26 Timing Generator simulation in ModelSim(Pre-simulation)
extracted from this thesis'（Shao-Hang Hung. 's ）coordination

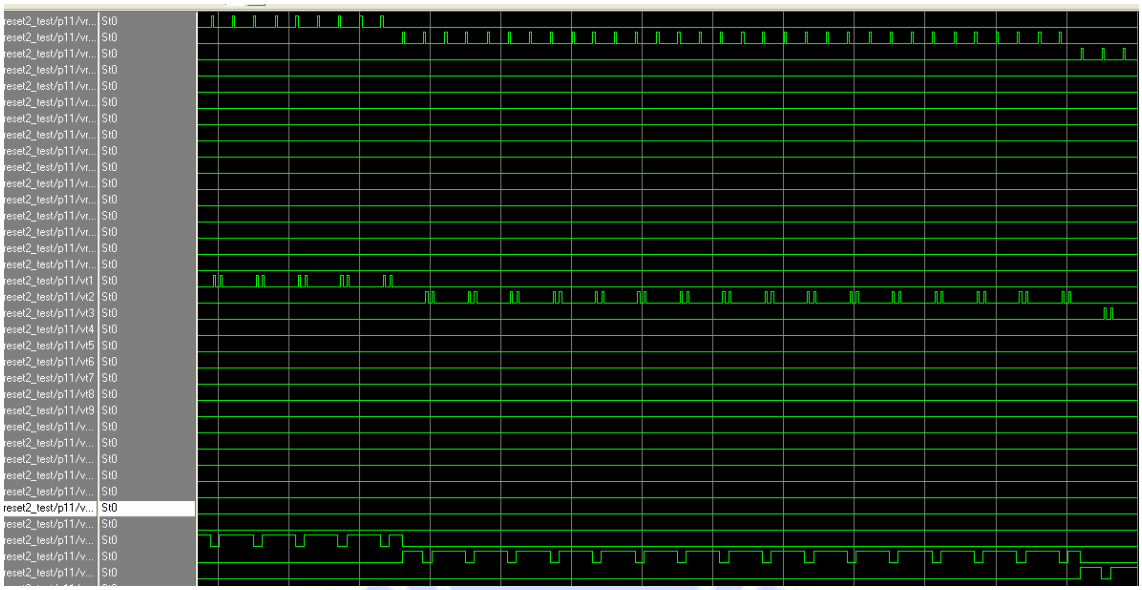


Fig. 3.2-27 Timing Generator simulation in ModelSim(Post-simulation)

extracted from this thesis'（Shao-Hang Hung. 's ）coordination

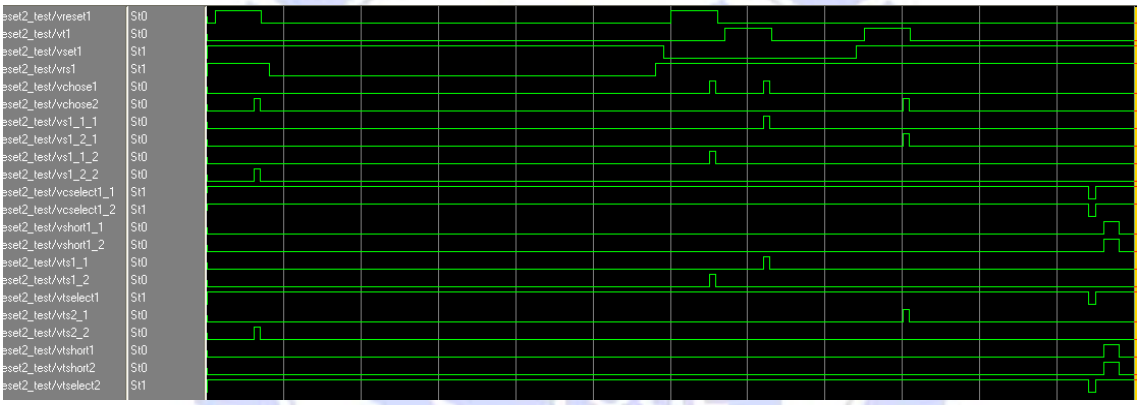


Fig. 3.2-28 Single pixel operation signals with Timing Generator simulation in ModelSim(Pre-simulation)

extracted from this thesis'（Shao-Hang Hung. 's ）coordination

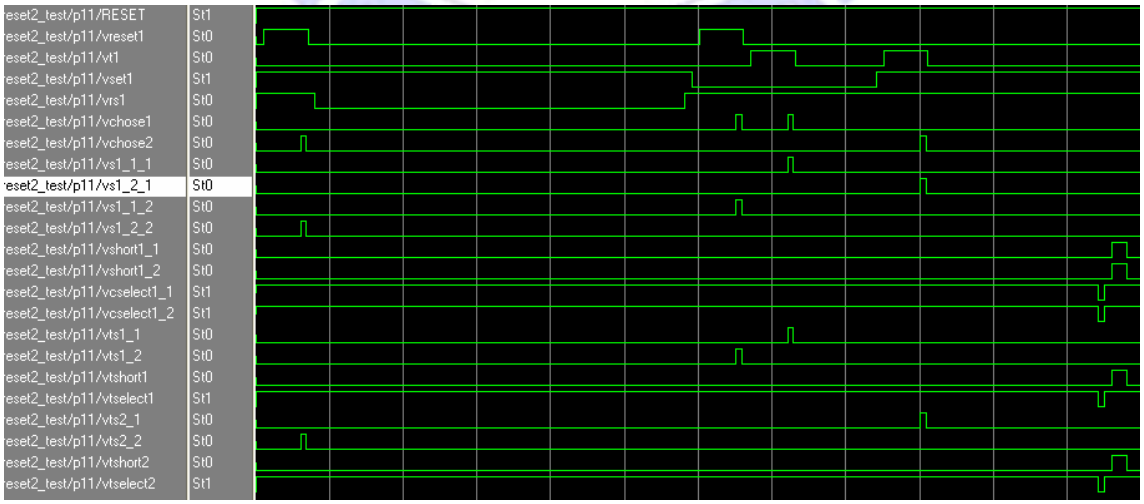


Fig. 3.2-29 Single pixel operation signals with Timing Generator simulation in ModelSim(Post-simulation)

extracted from this thesis'（Shao-Hang Hung. 's ）coordination