Chapter 4
Implementation, Test Platform & Result

On this chapter, we would introduce this chip's implement procedures. On the circuit layout, we would exhibit them in each part, and the chip's full-plan. Finally, the test platform plan would be demonstrated.

4.1 Chip Design Flow & Implementation

The chip was implemented in mix-mode chip design flow, as Fig. 4.1-1 shown. First of all, we should survey the related paper, define the final goal and set the chip spec including analog and digital parts. Second, simulation software H-spice has been used in pre-simulation for the overall circuit. After the procedure on analog design, we sketch the circuit layout in SpringSoft Inc.'s software － Laker. On the verify procedure, we still trust the Design Rule Check（DRC）and Layout Vs. Schematic（LVS）software － Calibre, which is Mentor Inc.'s production. After confirmed the circuit layout, we need to draw out the RC value to enter the post simulation. While finish the analog circuit design, the gds file should transfer to LEF file with Abstract, also the product of Calibre, to compose with the digital circuit part. On digital design flow, we write behavior level hardware description language（HDL）- Veilog in Mentor Graphics ModelSim. Then, transfer the behavior level pass by Register Transfer Level（RTL）,and last to the gate level by Cadence's Design Compiler. Next, Cadence SOC encounter would combine the full circuit including analog and digital part. Finally, we still use Calibre DRC and LVS for our final check.

In the general layout consideration, we can't only concern in digital circuit view. The process mismatch can minimize in dummy cells, especially on the poly layer. The guard ring should also round in each passive device such as capacitor and resistors, and the signal path devices in double layer. Double guard ring would draw to different potential, GD and GS, and should separate with other source like analog power and digital power.

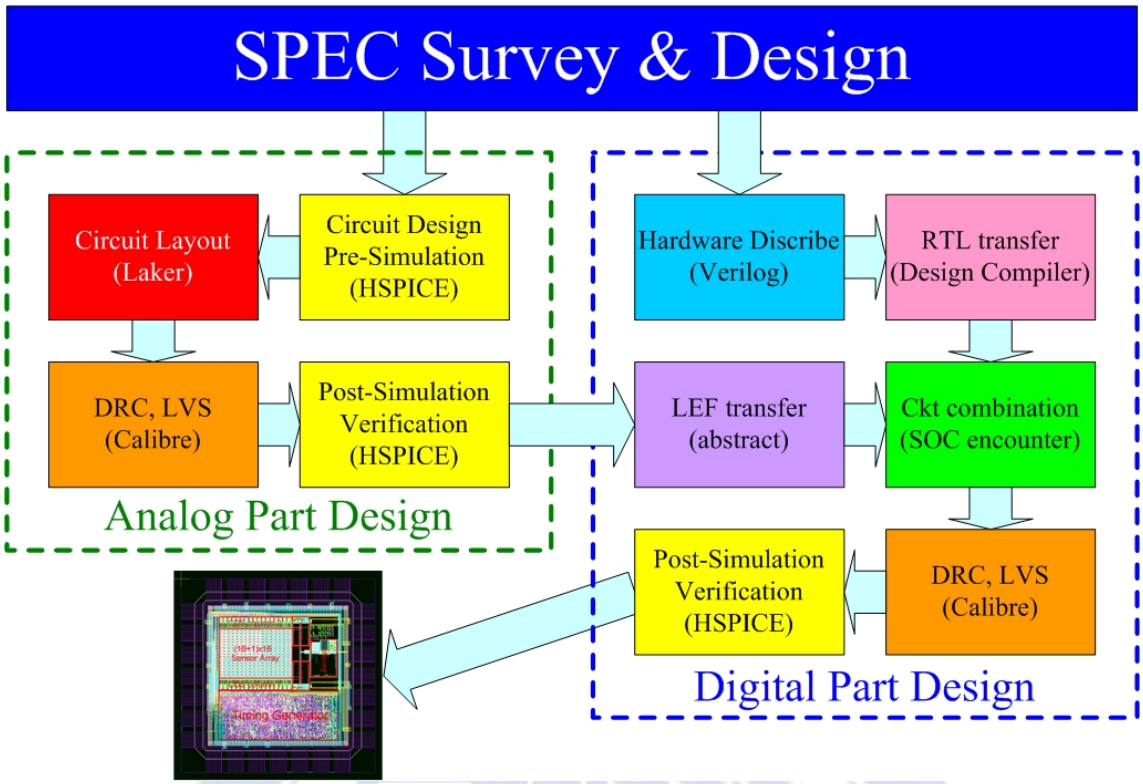

Fig. 4.1-1 Mix - Mode Circuit Design Flow

extracted from this thesis'（Shao-Hang Hung. 's ）coordination

4.2 Chip Layout

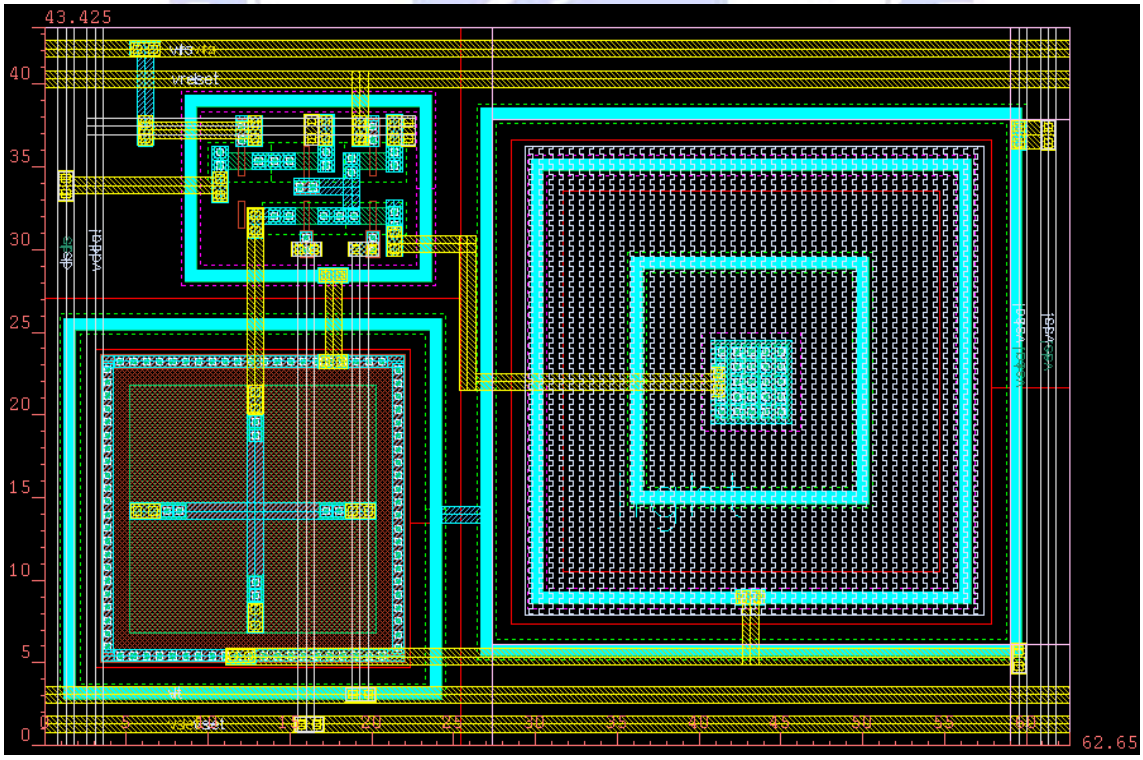

Fig. 4.2-1 Pixel layout diagram: area 62.65 × 43.425 um², fill factor34.2%

extracted from this thesis'（Shao-Hang Hung. 's ）coordination

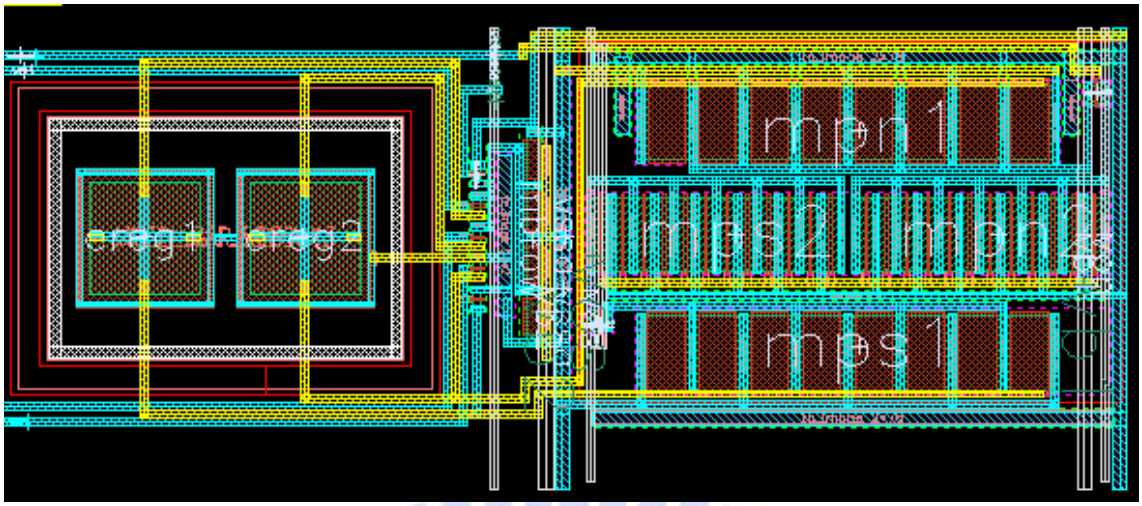

Fig. 4.2-2 CDS layout diagram: C_{reg} 200fF

extracted from this thesis'（Shao-Hang Hung. 's ）coordination

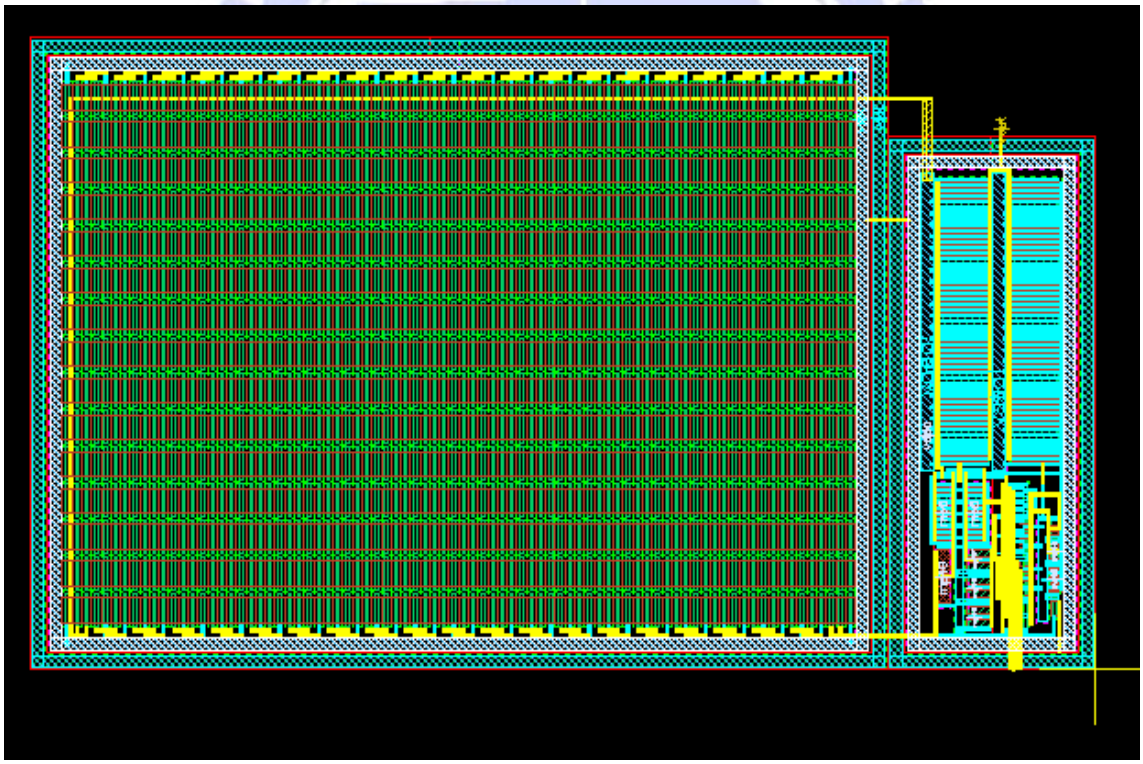

Fig. 4.2-3 TCDDA layout diagram

extracted from this thesis'（Shao-Hang Hung. 's ）coordination

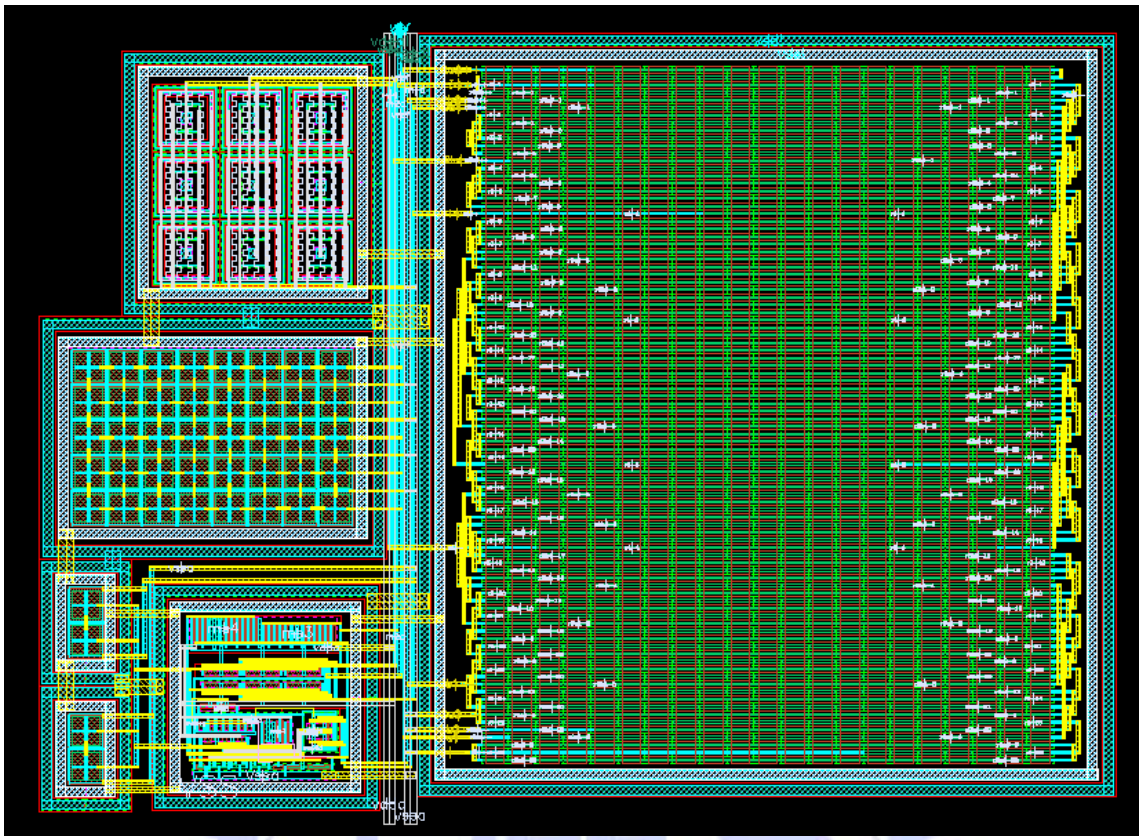

Fig. 4.2-4 Bandgap layout diagram

extracted from this thesis'（Shao-Hang Hung. 's ）coordination

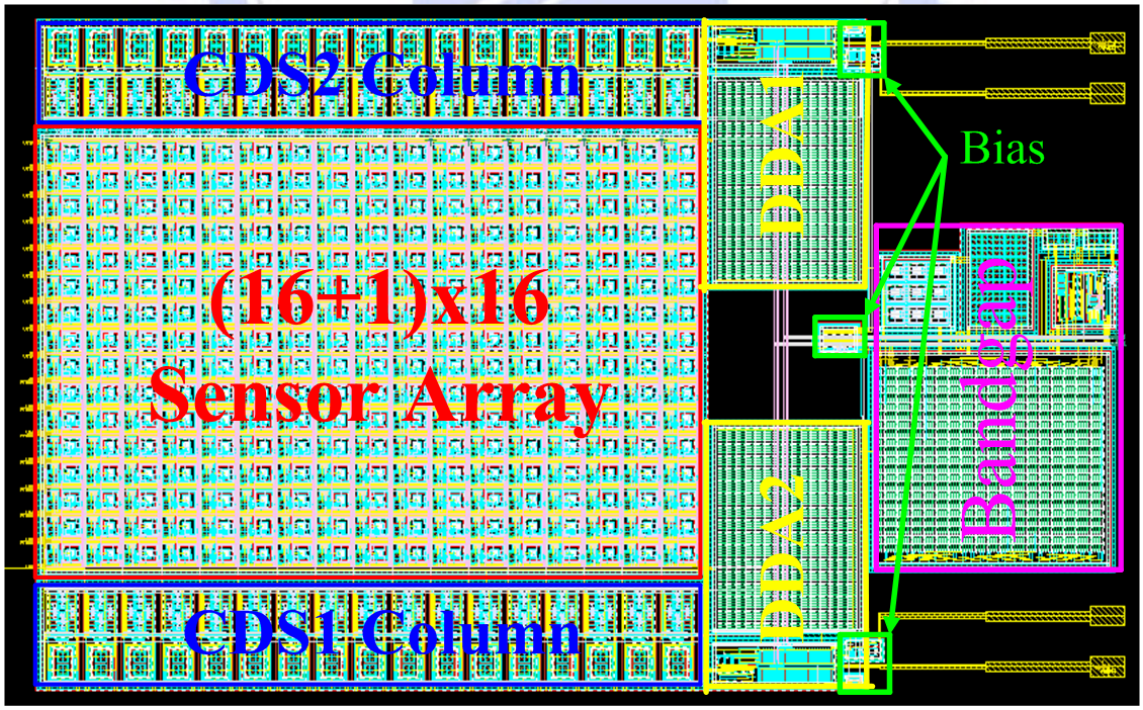

Fig. 4.2-5 Analog Part layout diagram

extracted from this thesis'（Shao-Hang Hung. 's ）coordination

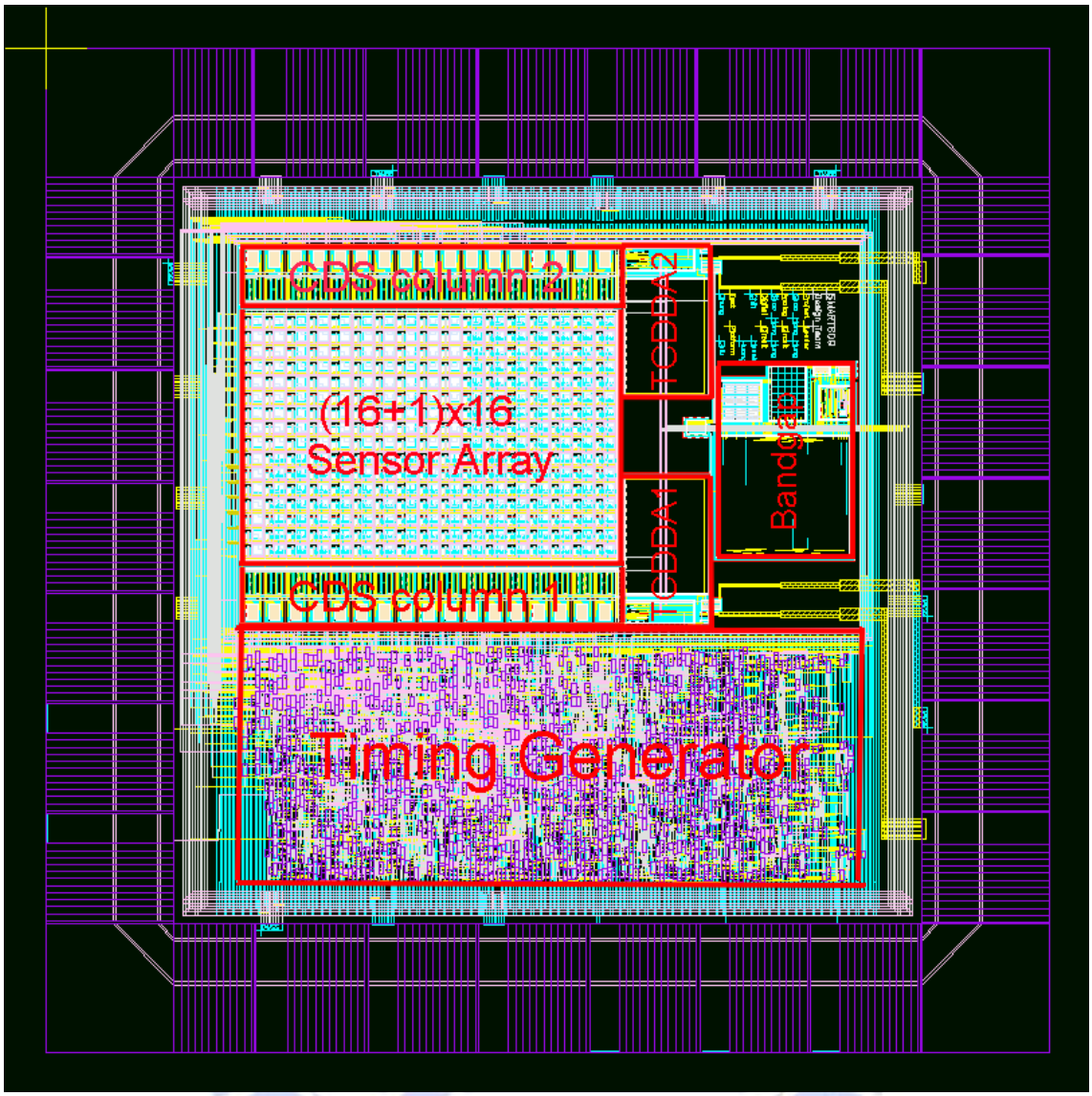

Fig. 4.2-6 Full plan chip（SMART809） layout diagram

extracted from this thesis'（Shao-Hang Hung. 's ）coordination

CKT name : Wide Dynamic Range & Temperature Compensated Gain CMOS Image Sensor in automotive applications

Technoloy : TSMC 0.35um 2P4M CMOS Mix Mode Technology

Package : SB24

Chip Size : 2.826 × 2.826 mm^2

Power Dissipation : 167.7mW（Including Analog & Digital Circuit）

Max. Frequency : 10MHz

Testing Results :☐Function work ☐Partial work ☐Fail

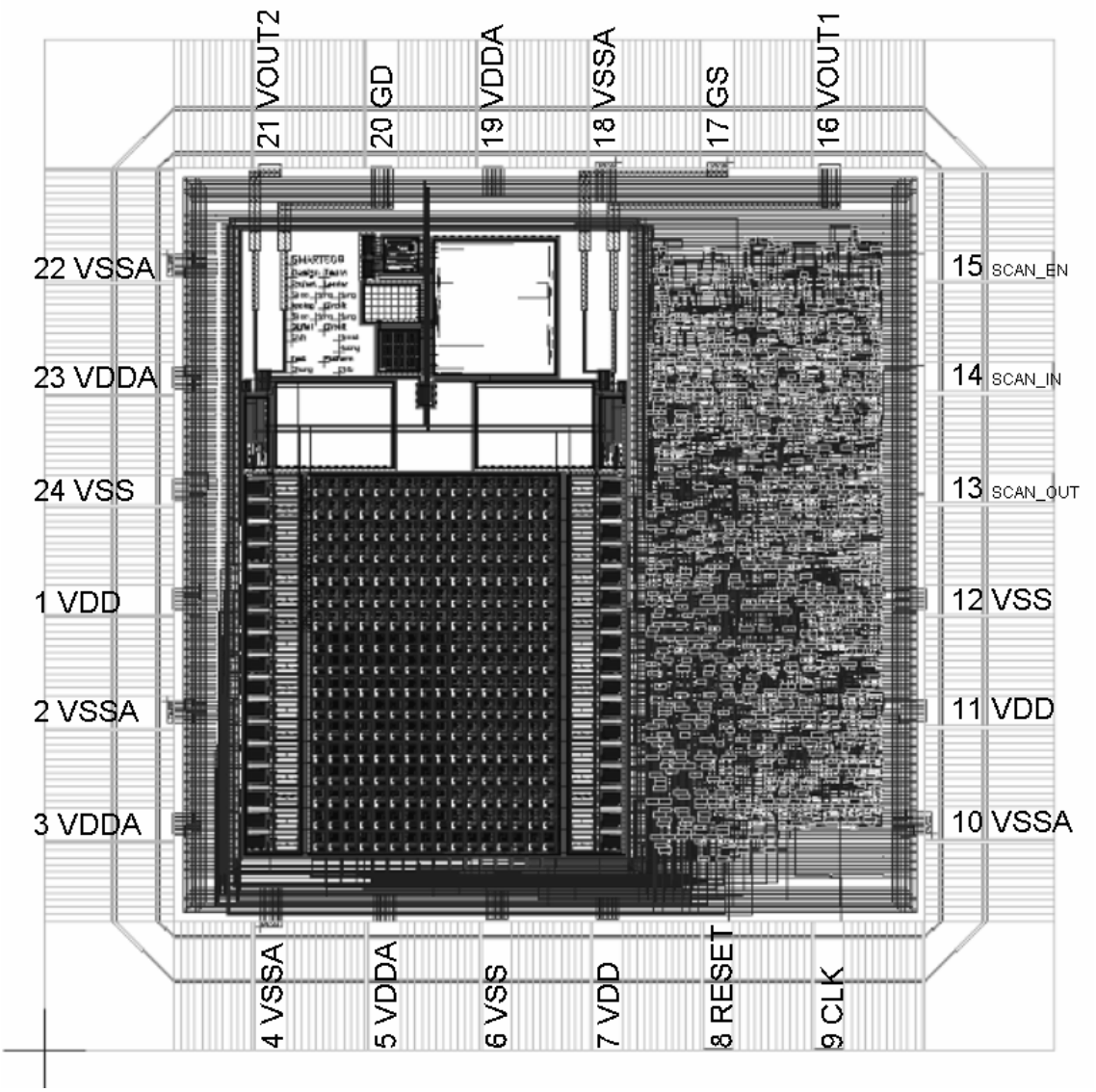

Fig. 4.2-7 Chip Layout and Output Pin Description

extracted from this thesis'（Shao-Hang Hung. 's ）coordination

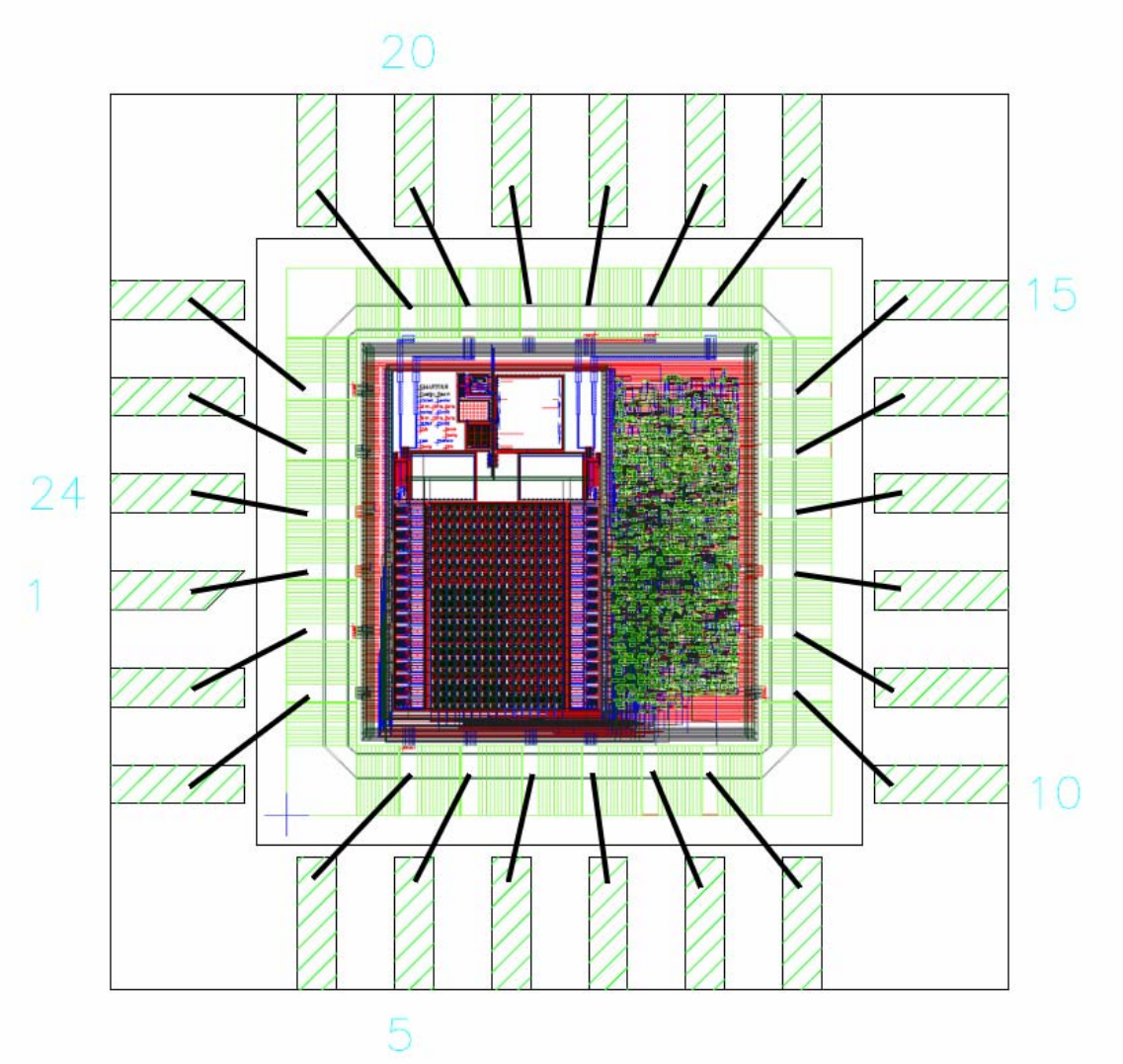

Fig. 4.2-8 Side Braze 24-pin lead Bounding Diagram
extracted from this thesis'（Shao-Hang Hung. 's ）coordination

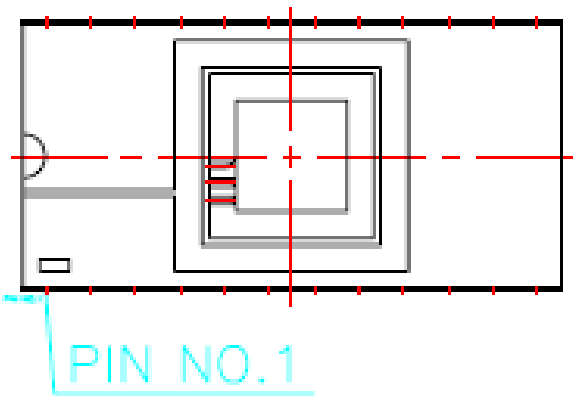

Fig. 4.2-9 Chip Package Diagram
extracted from this thesis'（Shao-Hang Hung. 's ）coordination

4.3 Test Platform Design

We have two test stages for this chip. First stage we would have the electrical test to confirm right DC operation level and AC signal. In the second stage platform, commercial ADC will convert the signal into digital type. We would try our best to display image by DSP system, and heat it in different temperature to confirm the theorem. Fig.4.3-1 is the electrical test platform, and Fig. 4.3-2 is the display platform

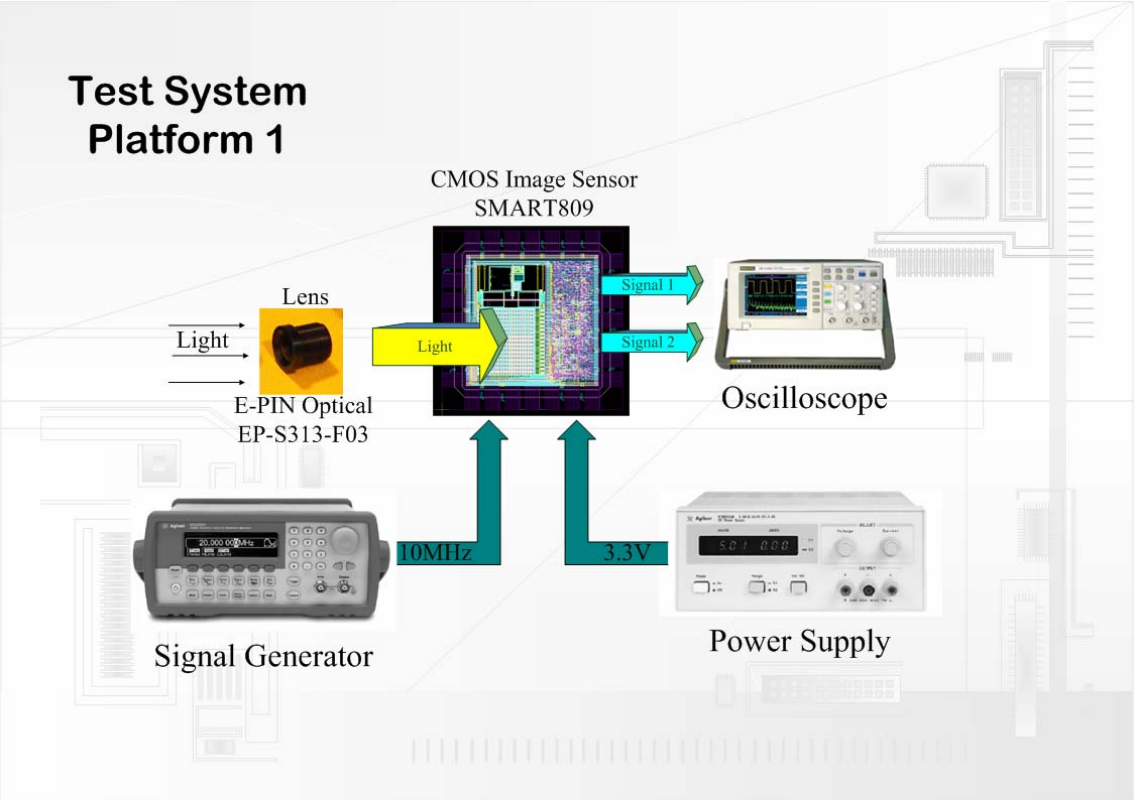

Fig. 4.3-1 Electrical test platform（First Stage）

extracted from this thesis'（Shao-Hang Hung. 's ）coordination

Equipment：

Signal Generator, Oscilloscope, Power Supply

Test Procedure：

1、Set Power Supply in 3.3V, and connected to analog source VDDA, digital source VDD, and guard source GD. The three sources should divided by Ferrote Bead prevent the noise from power source.

2、Generate 10MHz clock to driven digital circuit in SMART809

3、Input the RESET signal to reset digital circuit

4、On Siganl 1 and Signal 2 port we can measure a 12MHz pulse signal with 1V DC level on oscilloscope.

5、If we can measure the signal, the chip can declare function work.

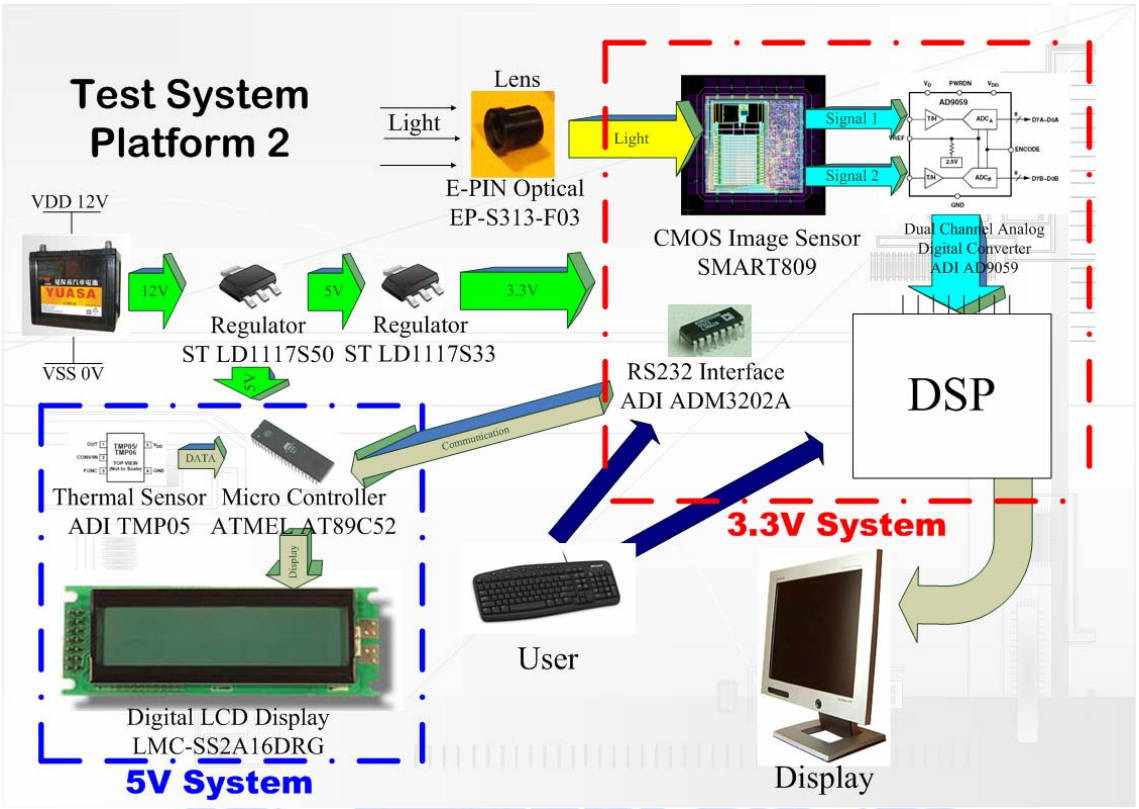

Fig. 4.3-2 Display test platform（Second Stage）

extracted from this thesis'（Shao-Hang Hung. 's ）coordination

Equipment：

1、 Digital Temperature Sensor Board（Fig. 4.3-3）

(1)Digital output Temerature Sensor：Analog Devices Inc. TMP05

(2)Display Micro Controller：ATMEL AT89C52

(3)RS232 interface chip：Maxim MAX232

(4)Digital LCD Display：LMC-SS2A16DRG

2、 Image Display platform

(1)Optical Lens：E-pin Optical EP-S313-F03

(2)Analog Digital Converter：ADI AD9059 dual channel ADC

(3)DSP processor

(4)LCD Display：Benq FP731

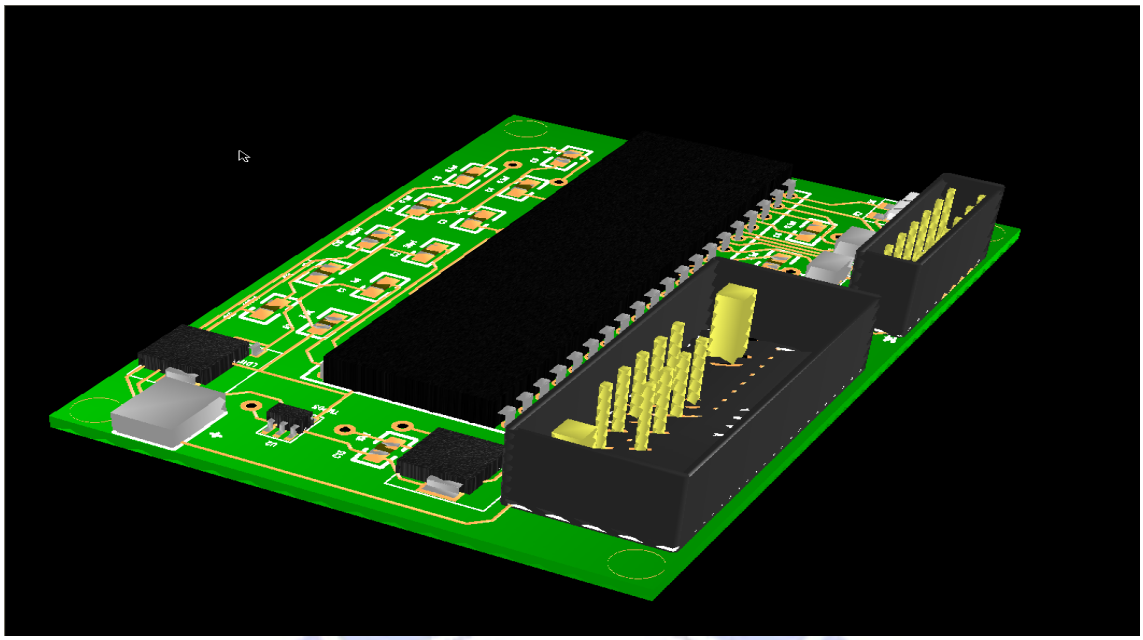

Fig. 4.3-3 Digital Temperature Sensor board in 3D view
extracted from this thesis'（Shao-Hang Hung. 's ）coordination

Test Procedure：

1、After pass the first electrical test platform and make sure the function work of chip, it can put on the display platform which were prepared before.

2、Writing DSP languages not only control the reset signal of SMART809, and stake the pixel gray level signal into 16 by 16 image array. That would be the successful display.

3、Recording the frame in general temperature, and compare the image with different temperature. We supposed to verify image in 65°C and 85°C. As the theorem in this thesis, we would get the better dynamic range value while in higher temperature, and the frame quality would not be affected by temperature variation.

4.4 Result

From three months fabrication, the chip has been implemented by TSMC Inc. and the micrograph has been shown on Fig. 4.4-1. As the design expect, the DC operation level would be set on 1V volt. We can measure amount 10us pulse signal on oscilloscope with 1V Vpp maximum signal swing. If get such result, we can declare this chip is function work. Passing this procedure, we can go through to the display procedure.

In order to reduce the noise effect from power source and connection path, we should make a specific test platform. Fig. 4.4-2 shows the circuit diagram for the test platform. The 100uF polarized capacitances which connected between power source and ground are designed to filter the pick noise from power source. The 0.1uF general capacitances which were parallel connected with polarized ones play the filer to reject noise from signal side. Other circuit has been explained on Section 4.3, and the floor plan for the test platform demonstrated on Fig. 4.4-3.

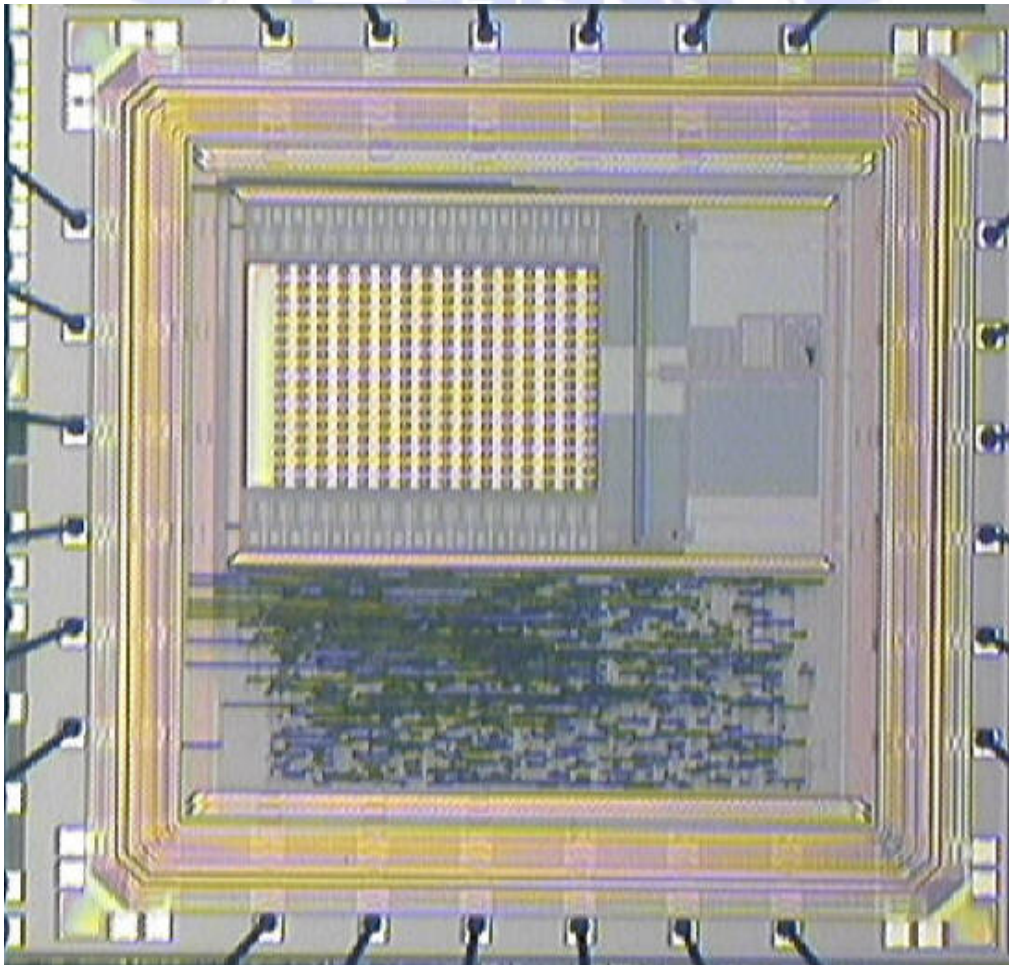

Fig. 4.4-1 Micrograph of the SMART809
extracted from this thesis'（Shao-Hang Hung. 's ）coordination

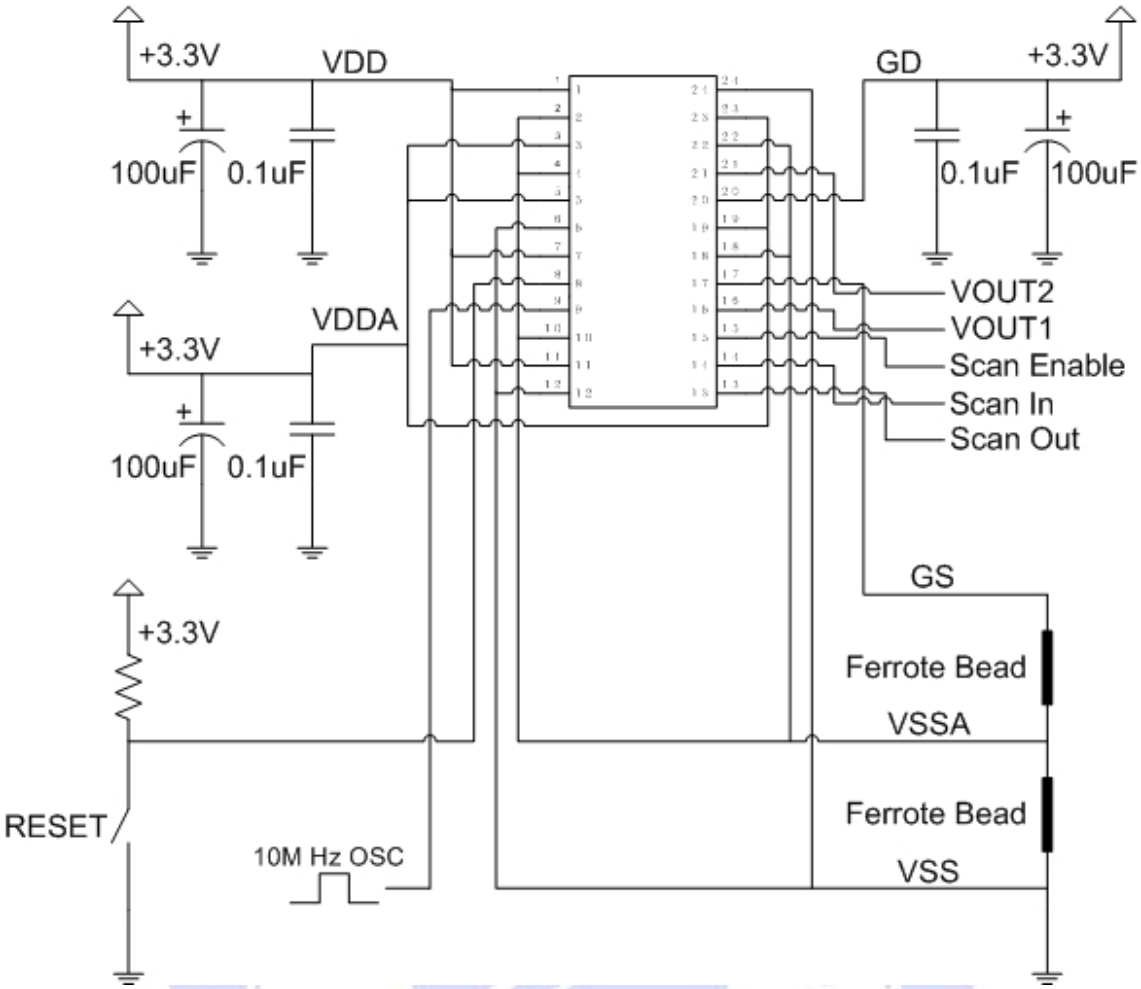

Fig. 4.4-2 Circuit diagram for the Test Platform

extracted from this thesis'（Shao-Hang Hung. 's ）coordination

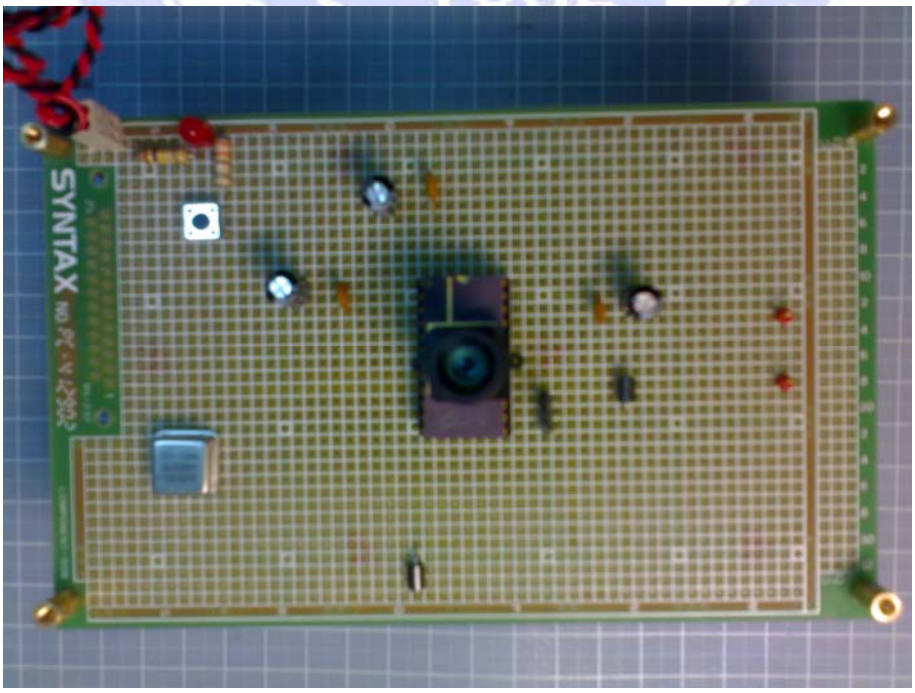

Fig. 4.4-3 Floor plan for Electrical Test Platform

extracted from this thesis'（Shao-Hang Hung. 's ）coordination

Our test light source uses MLC-150c, which shows on Fig. 4.4-4, is the production from Motic Company. The fiber optic illuminator system can emit intensity up to 120,000 lux with a color temperature ranging between 2500K - 3500K. Fig. 4.4-5 demonstrates the output signal at illumination in 100,000 lux. Finally, we measure the operation DC level is 1.1V with 7us pulse signal. Maximum illumination signal swing is 980mV Vpp. As a result, we can finally define the chip is function work.

Fig. 4.4-4 Fiber optic illuminator MLC-150C
extracted from Motic Cooperation < 10 >

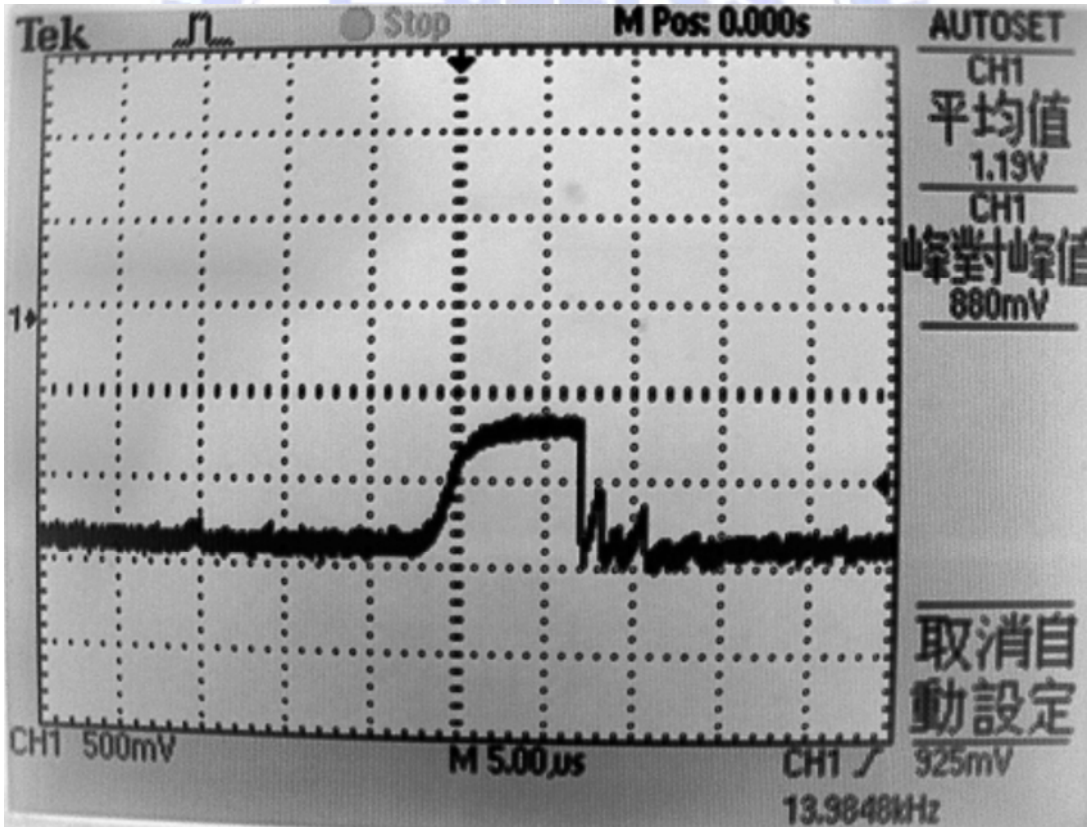

Fig. 4.4-5 Output signal while illumination on 100,000 lux
extracted from this thesis'（Shao-Hang Hung. 's ）coordination