國立交通大學

電機學院IC設計產業研發碩士班

碩士論文

寬頻混頻器暨24GHz鎖相迴路之
互補式金氧半導體射頻積體電路研製

CMOS RFIC Design of
Wideband Mixer and 24GHz Phase-Locked Loop

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摘　　要

本論文分為寬頻混頻器與鎖相迴路兩個部份。利用標準 TSMC 0.18μm RF CMOS 製程完成本論文中所設計的電路。

第一部份設計兩種適用於超寬頻系統的寬頻混頻器與一種用於超寬頻頻率合成器中的單旁波帶混頻器。第一種寬頻混頻器的頻寬是從 2.4 到 10.7 GHz，此寬頻混頻器採用的電路架構為 LC 摺疊疊接方式與一個高線性轉導器。第二種寬頻混頻器的頻寬是從 2 到 11.5 GHz，此寬頻混頻器採用的設計方法為第一種寬頻混頻器的架構與一個寬頻巴倫，輸入訊號可以單端輸入經過巴倫後產生雙端平衡輸出。最後設計了一種可以使用於超寬頻頻率合成器中的單旁波帶混頻器。

第二部份設計兩種可應用於 24GHz 汽車防撞雷達系統之壓控振盪器與一種可應用於 24GHz 防撞雷達系統之鎖相迴路。第一種振盪器採用的設計方法為電流再利用架構、二倍頻過濾、與二次諧波 LC tank。模擬結果頻率可調範圍為 23.32GHz～24.92GHz，功率消耗為 10mW，相位雜訊在 1MHz offset 為 -111.3dBc/Hz，輸出功率約-0.35dBm。第二種振盪器採用的設計方法為電流再利用架構、二倍頻過濾、與 T 型濾波器。模擬結果頻率可調範圍為 23.32GHz～24.78GHz，功率消耗為 9.9mW，相位雜訊在 1MHz offset 為-111.6dBc/Hz，輸出功率約-0.68dBm。最後，設計的鎖相迴路輸出頻率為 24GHz，模擬結果頻率可調範圍為 22.78GHz～26.91GHz，功率消耗為 26mW，相位雜訊在 1MHz offset 為 -102dBc/Hz，PLL 輸出功率約-12dBm。

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Wideband Mixer and 24GHz Phase-Locked Loop

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ABSTRACT

The thesis consists of two parts: wideband mixer and phase-locked loop. These proposed circuits are fabricated using a standard TSMC 0.18μm RF CMOS process technology.

The first part designs two kinds of wideband mixer for UWB systems and one kind of single-sideband mixer for UWB synthesizer. The bandwidth of the first wideband down conversion mixer is from 2.4 to 10.7 GHz. This mixer adopts a LC folded cascode structure and a feedforward compensated high-linearity differential transconductor. The bandwidth of the second wideband mixer is designed from 2 to 11.5 GHz. The adoption of broadband active balun allows providing balance signals for mixer core from single input. Finally, the single-sideband mixer designed for UWB synthesizer is presented.

The second part designs two kinds of 24 GHz voltage-controlled oscillator and one kind of 24 GHz phase-locked loop for collision avoidance radar system. The first VCO adopted current-reuse topology, tail filtering inductor, and 2nd harmonic LC tank. The simulation result shows the achieved phase noise of -111.3 dBc/Hz at 1MHz offset. The tuning range is from 23.32GHz to 24.92GHz. The second VCO adopted current-reuse topology, tail filtering inductor, and T-structure filter. The simulation result shows the achieved phase noise of -111.6 dBc/Hz at 1MHz offset. The tuning range is from 23.32GHz to 24.782GHz. Finally, a 24 GHz fully integrated PLL is designed. The simulated closed-loop lock time is 2us. The PLL output power is -12dBm with a power dissipation of 26 mW, while exhibiting a phase noise of -102 dBc/Hz at 1MHz offset from the carrier.

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Chapter 1 *Introduction*

1.1 Motivation

Recently the wireless communication becomes more and more popular. The wireless communication systems must be portable, low cost, high performance, highly integration, low power and small size. All of these constraints combine to make the design quite challenging. One approach to reach the requirements for wireless communication is CMOS technology. The CMOS circuits have many drawbacks such as noisy and low current driving capability. But with the rapid scaling of CMOS process technologies, it has dramatically improved CMOS performance and achieving frequency of gigahertz. In addition, CMOS offers low power and highly integration. For these reasons, many papers of CMOS RF circuits have been published. Based on the CMOS RFIC advantages of integrated with baseband circuits, more transceiver circuits are realized by using CMOS process. Therefore, CMOS RFIC becomes a new trend for the wireless communication system.

The goal of this thesis is to research the radio frequency circuits in CMOS process technology. In this thesis, we focus on mixer, voltage-controlled oscillator (VCO), and phase-locked loop (PLL). A modified mixer is used to minimize the nonlinear distortion. The main problem of VCO is to improve phase noise. We will describe how to improve it in later chapters. PLL has played an important role in

wireless communication receivers. PLL is used in many different applications such as clock and data recovery, synchronization, frequency synthesis, modulator, and demodulator. The PLL often consumes a large percentage of the total power in wireless communication receivers. Hence, a CMOS PLL with on-chip LC-tank VCO will be discussed in this thesis.

1.2 Research Results in RFIC Design

The research results in RFIC design are as below table. This thesis is focus on these circuits. These circuits are simulated using Agilent ADS and fabricated in tsmc 0.18μm RF CMOS process.

Tapeout Number	Circuit Name	Chip Size (mm^2)
T18-95B-49	A Wideband Down-Conversion Mixer in 0.18-μm CMOS Technology for Ultra-wideband Applications	0.70 X 0.58
T18-95C- 117	A UWB Single-Sideband Mixer for Frequency Synthesizer	0.62 X 0.69
T18-95D- 57	A Wideband CMOS Down Conversion Mixer with Broadband Active Balun	0.85 X 0.57
T18-95E- 116	Design of 24GHz VCO for Collision Avoidance Radar	1.03 X 0.92
T18-96A- 41	A 24GHz Current-Reuse CMOS Differential LC-VCO	0.90 X 0.93
T18-96A- 114	Design of 24GHz PLL	1.25 X 1.15

1.3 Thesis Organization

This thesis is organized into 5 chapters. This chapter is the first one. In Chapter 2, we will introduce the fundamentals of mixer, voltage-controlled oscillator, and phase-locked loop. Chapter 3 is a main chapter that has the implement of the wideband mixer and broadband active balun. This chapter encompasses the detailed analysis of the proposed circuits. The simulation and measurement results will be included. Chapter 4 is focus on design of the voltage-controlled oscillator and phase-locked loop. Also, the simulation results will be included. At last, the conclusion is made in chapter 5.

Chapter 2 *General Backgrounds*

In this chapter, we will introduce the fundamentals of direct conversion receiver, mixer, active balun, voltage-controlled oscillator, phase-locked loop, and 24GHz radar system.

2.1 The Direct Conversion Receiver

Because of the rapid growth in demand for broadband wireless communications, wireless local area networks (WLAN) are becoming more attractive not only to exchange large amount of data locally but also as access points for the cellular infrastructure. The superheterodyne has been the architecture of choice for wireless transceivers for many years. On the other hand, due to the increase of the integration level of RF front-ends, alternative architectures, targeting reduced power consumption and minimization of the number of off-chip components, have been considered, in the recent past. Among them, the direct conversion receiver (DCR) or zero-IF receiver has increasingly gained widespread attention due to its potentially of low power consumption, lower complexity, low manufacturing costs, and easy integrating with the baseband circuits [1]-[5]. Fig. 2.1 shows the block diagram of the direct conversion RF front-end, where the LO frequency is equal (or approximate) to input carrier frequency and the LO will translate the center of the desired signal to zero IF or low IF.

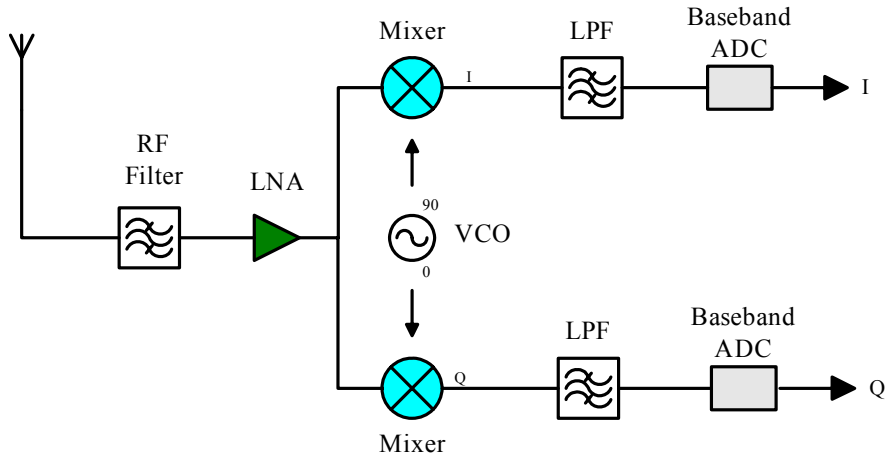

Fig. 2.1. Block diagram of direct conversion receiver architecture.

The most important advantage of the direct conversion receiver is that the intermediate frequency (IF) passband filter can be neglected and replaced by a low pass filter. Low pass filter is much easier to integrate in standard semiconductor technology. However, some issues which do not exist or are not serious in the heterodyne architecture become critical in the direct conversion receiver. These drawback include DC offset, flicker noise, even order distortion, I/Q mismatch, and so on. Among these the DC offset generated by self-mixing is the most critical. The DC offset is caused by carrier leakage from the local oscillator to the mixer input and to the antenna as shown in Fig. 2.2. Interferer leakage will also cause a DC offset at the mixer output as shown in Fig. 2.3. To overcome the drawback of DC offset, the improving isolation between LO and RF ports is important. The second-order intermodulation distortion (IMD2) is a fundamental problem, because the second-order intermodulation term interferes the reception of the wanted signal as shown in Fig. 2.4. In a perfectly balanced Gilbert cell mixer, the IMD2 is a common-mode signal and therefore does not a serious problem. However, due to the mismatch of device, the balance between the negative and positive branch of the mixer is degraded and the IMD2 becomes a problem. About I/Q mismatch, if the modulation is complex modulation, the I/Q mismatch can equal to image interferer. This mismatches between the amplitudes of the I and Q signal corrupt the constellation of the down converted signal. Therefore influences the bit error rate. Finally, flicker noise or l/f-noise may be a problem in the mixer and subsequent filter because the signal is converted directly to baseband.

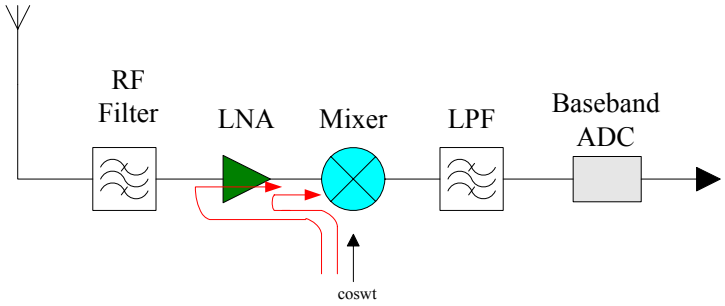

Fig. 2.2. LO signal leakage.

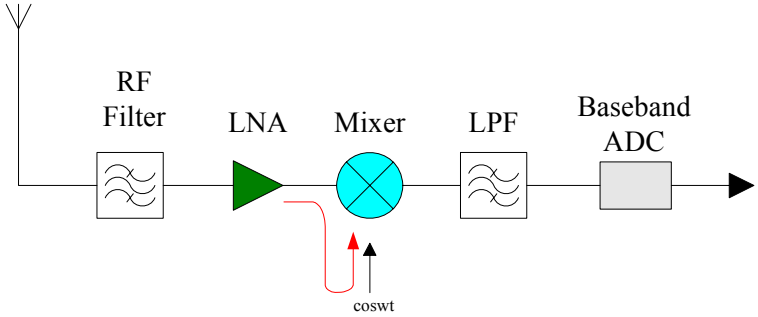

Fig. 2.3. A strong interferer signal leakage.

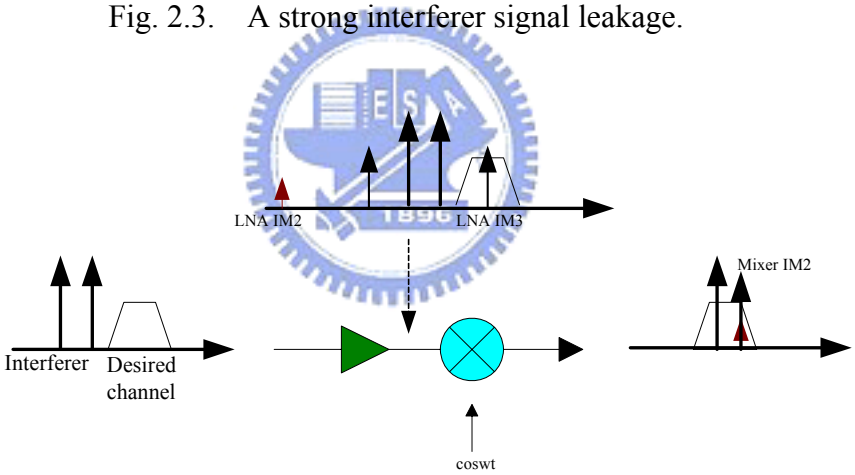

Fig. 2.4. Even order distortion.

2.2 Mixer Fundamentals

2.2.1 Principles of Mixer

The mixer is an essential building block in the receivers, which is responsible for frequency up-conversion and down-conversion. It is also an important component associated with the linearity of the front-end receivers. The first stage of mixer must have high linearity to handle the large input signals from LNA without significant intermodulation. Nonlinearity causes many problems, such as cross modulation,

desensitization, harmonic generation, and gain compression, but even-order nonlinearity can be easily reduced by differential architecture. However, odd-order nonlinearity is difficult to be reduced, especially the third-order intermodulation distortion (IMD3). IMD3 is the dominant part of the odd-order nonlinearity.

Mixer is a three ports circuit, which are the RF port, the LO port and the IF port. It is a multiplication of two signals which are the RF signal amplified from the low noise amplifier and the signal from the local oscillator (LO) to achieve the function of frequency transformation. This is depicted by equation (2.1). Then the RF signal is down-converted to the intermediate frequency (IF).

$$\left(A\cos\omega_1 t\right)\left(B\cos\omega_2 t\right)=\frac{AB}{2}\left[\cos\left(\omega_1+\omega_2\right)t+\cos\left(\omega_1-\omega_2\right)t\right] \tag{2.1}$$

From the equation (2.1), the multiplication of two signals at the frequencies of ω1 and ω2 together produce signals at the sum (ω1+ω2) and difference (ω1-ω2) frequencies. The amplitudes are proportional to the RF and LO amplitudes. The multiplications in the time domain would result in convolutions in the frequency domain. Thus, the mixer can responsible for frequency translation. In equation (2.1), signals at the frequency of (ω1+ω2) can be easily filtered out because they are far away from desired frequency in the frequency domain. The signals at the frequency of (ω1-ω2) are our desired outputs. In circuit implementations, the multiplication can be achieved by passing the input signal $A\cos\omega t$ from RF through a switch driven by another signal $B\cos\omega t$ from LO. If the LO amplitude is constant, any amplitude modulation in the RF signal is transferred to the IF signal.

The most important parameters for determining the performance of a mixer are power conversion gain, and linearity. We will describe these parameters in the subsequent contents.

2.2.2 Performance Parameters

2.2.2.1 Conversion Gain

One of important parameters of mixer's characteristics is conversion gain, which is defined as the ratio of the desired IF output to the value of the RF input as shown in equation (2.2). In general, the conversion gain of the mixer has two types: one is voltage conversion gain and the other is power conversion gain.

$$Conversion\ \ Gain = \frac{The\ \ desired\ \ output\ \ IF\ \ power}{The\ \ input\ \ RF\ \ power} \tag{2.2}$$

Assuming input a sinusoidal signal and the output would include signals at integer multiples of the frequencies of the input signal as equation (2.3). In equation (2.3), the terms with the input frequency are called the fundamental signal, and the higher order terms are called the harmonics. The harmonics would cause performance degradations.

$$\begin{aligned} V_{OUT}(t) &= \alpha_1(A\cos\omega t) + \alpha_2(A\cos\omega t)^2 + \alpha_3(A\cos\omega t)^3 + ... \\ &= \alpha_1(A\cos\omega t) + \frac{\alpha_2 A^2}{2}(1+\cos 2\omega t) + \frac{\alpha_3 A^3}{4}(3\cos\omega t + \cos 3\omega t) + ... \end{aligned} \tag{2.3}$$

The output function of mixers is a compressive function of input levels. When the input level grows sufficiently high, the output eventually saturates and the conversion gain begins decreasing. If α3 holds a negative value, this phenomenon will happen. At small values of input level A, the second term is negligible and the gain remains constant. The gain starts decreasing when the input level gets large as shown in equation (2.4).

$$Gain = \alpha_1 + \frac{\alpha_3 A^2}{4} \tag{2.4}$$

2.2.2.2 Linearity

The mixers are assumed to be linear and time-invariant. The linearity is a significant parameter in the mixer design. Here we will introduce two parameters of linearity: P1dB and IIP3.

The IF output is proportional to the RF input signal amplitude ideally. However, as the input signal becomes large, the output signal fails to exhibit this characteristic. We use the value departing the ideal linear curve 1 dB as the referenced point, 1 dB compression point, shown in Fig. 2.5. The dashed line in Fig. 2.5 shows our desired output characteristics. The solid line shows the real characteristic. The 1dB compression point characterizes the input level where the output level is 1dB less than our desired output level. A higher 1dB compression point stands for a better linearity performance.

The linearity of a mixer can also be evaluated by intermodulations. The two-tone third-order intercept is often used to characterize mixer linearity. Ideally, each of two

different RF input signals will be translated without interacting with each other, and we can only gain the desired IF signal from the output port. However, practical mixers will always exhibit some intermodulation effects. This is because that two or more different frequencies of input signals will degrade the linear region of the system. The third intercept point (IP3) is measured with two tone test. Two tones are closely placed and injected as input simultaneously. If we consider the region where the input level is small, the output characteristic is approximately linear. The third-order intercept is the intersection of these two curves as illustrated in Fig. 2.6 which is the extrapolation of the signal line and the third-order harmonic line. The higher intercept, the more linear.

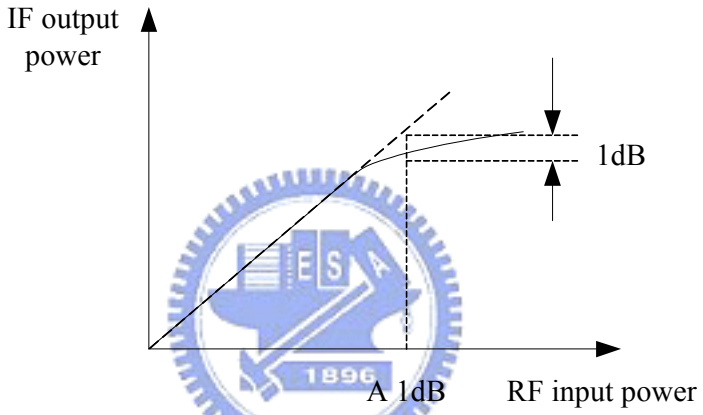

Fig. 2.5. P1dB.

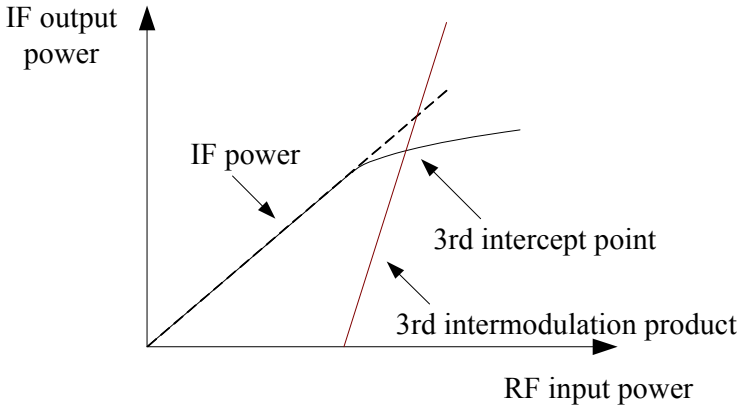

Fig. 2.6. IIP3.

2.2.2.3 Isolation

Another important parameter of mixer is isolation, which shows the interaction among RF, IF and LO ports. The isolation between each two ports of the mixer is

important. The LO to RF feedthrough is means the LO leakage to the LNA and (or) leakage to the antenna. The RF to LO feedthrough allows strong interferers in the RF path to interact with the LO driving the mixer. The LO to IF feedthrough is also important. If substantial LO signal exists at the IF output, the following stage may be desensitized. The feedthrough can be reduced largely by use double balanced mixers. The RF to IF isolation means the signal in the RF path directly appears in the IF. In the homodyne receivers, this is a critical issue with respect to the IMD2 problem.

2.2.3 Mixer Architecture

The implementation of CMOS down-conversion mixer can be passive or active. The simple passive mixer is shown in Fig. 2.7. It is usually using MOS transistor as a switch to modulate the RF signal by LO signal and down convert to IF band. Because passive mixer operates in the linear region, it has high linearity and excellent IIP3. But it provides poor conversion gain and noise figure. The simple active mixer is presented in Fig. 2.8. The active mixer provides better conversion gain than passive mixer. Its conversion gain is decided by the product of the input conductance g_m and load impedance to suppress the noise contributed by the subsequent stages. But the linearity of an active mixer is worse than that of a passive mixer.

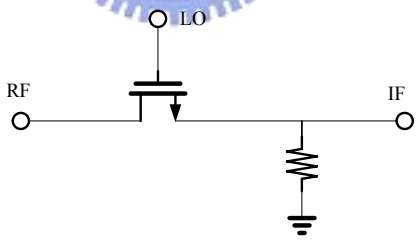

Fig. 2.7. Passive mixer.

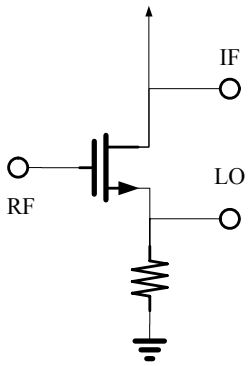

Fig. 2.8. Active mixer.

The Gilbert cell topology is a typical type used in active mixers. The advantages of this topology are the high conversion gain, low LO power, and low offset voltage. The Gilbert cell mixer consists of three stages: transconductor stage, switching stage, and load stage. The linearity of Gilbert mixer is dominated by the transconductor stage as shown in Fig. 2.9.

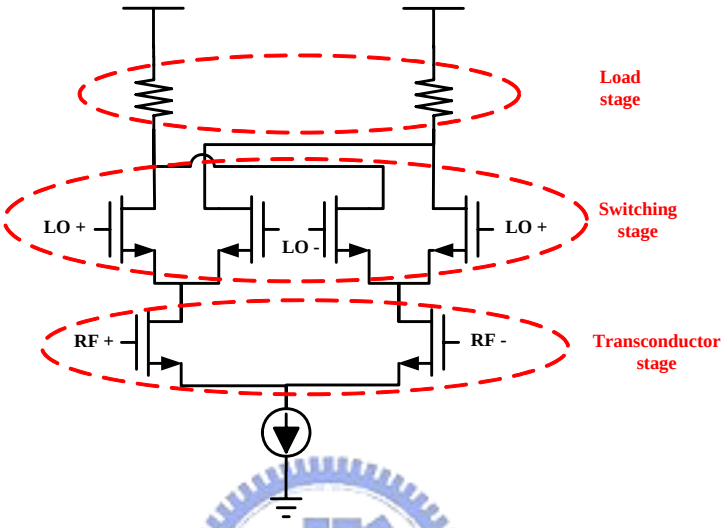

Fig. 2.9 The prototype of the CMOS Gilbert mixer

The function of three stages is described as follow. RF input stage is a differential pair that converts the RF voltage to current. The transconductance of this stage directly affects the linearity and the gain of the mixer. LO switch stage usually applies two differential pairs as modulated switch to construct double balanced structure. To achieve the goal that this two differential pairs completely switch the input power of the LO port must be larger. The value of the LO port also affects the conversion and the noise figure of the system. The output stage is load stage.

If the switching stage is ideal switches, the linearity of Gilbert mixer is dominated by the transconductor stage. Third-order input intercept point (IIP3), second-order input intercept point (IIP2), and input 1-dB compression point (P1dB) are the important parameters of linearity. IIP3 and IIP2 are the effects of intermodulation terms in the nonlinear circuits. P1dB is the ceiling of the input power. To improve linearity in Gilbert mixer, many methods have being used such as adding source degeneration resistors below the gain stage [24], bisymmetric Class-AB input stage [23], multiple gated transistor [22], and common-source and common-emitter RF transconductors [25].

2.3 Active Balun Fundamentals

Double balanced Gilbert mixer needs balanced RF, LO, and IF signals for its optimum operation such as higher conversion gain, good isolation, better dynamic and static offsets, and help improve the second and third order intermodulation rejection [6]–[8]. Therefore, it needs to provide differential signals into double balanced Gilbert mixer. Differential balun (or phase splitter) circuits are the critical block to generate a pair of differential output signals which have balanced amplitude and phase from a single-ended input. There are passive and active baluns in RFICs. Passive components have been used to implement the balun. Passive balun consume no DC power. But the LC networks need many spiral inductors and MIM capacitors. It is unsuitable in integrated circuits due to larger physical size. Since LC networks are narrow band and area consuming, it limits the use of passive baluns. Active baluns are wideband and compact size. It can be used in integrated circuits.

Active baluns techniques have been reported in past research. Several types of active balun topologies have already been proposed. There are three configurations normally employed for implementation of active balun circuits: single FET circuits [9],[10], common-gate common-source (CGCS) circuits [11]–[13], and differential amplifier circuits [7],[14]–[17]. The challenge in the active balun design is to maintain the 180^{O} phase difference and 0dB gain difference at high frequency.

The common-source single-FET balun is the simplest as shown in Fig. 2.10. Input signal into the gate, ideally the output signals at the drain and source will be out of phase by 180 degrees and have equal amplitude. The common-source single-FET balun has too much phase difference as a result of circuit parasitics. A common-gate cascaded with a common-source circuit provides equal amplitudes split with 180^{0} phase difference. The CGCS structure provides adequate isolation and accurate phase difference as shown in Fig. 2.11. For a differential topology, an RF signal applied at the input of one of the differential transistors and thereby providing an 180^{0} phase shift and equal amplitude between the two output signals as shown in Fig. 2.12.

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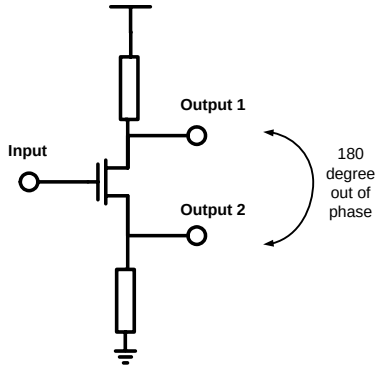


Fig. 2.10. Common source topology.

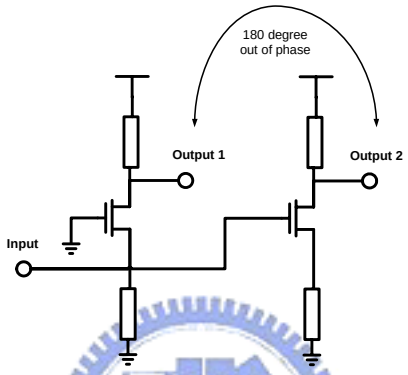


Fig. 2.11. Common gate cascaded with common source.

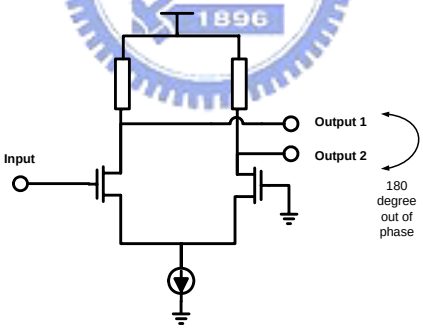


Fig. 2.12. Differential topology.

There are three simple types of differential to single-ended balun. First, a differential amplifier balun as shown in Figure 2.13. The gain of balun is determined by transconductances, output resistor and degeneration resistor R1. The degeneration resistor introduces noise and consumes some voltage headroom, but its advantage is that improves linearity of the balun. A multi-tanh doublet type balun is shown in Figure 2.14. The push-pull balun consists of a common source and the common drain as shown in Figure 2.15. The degeneration resistor R3 influences the gain. The resistor R2 is included for output impedance matching.

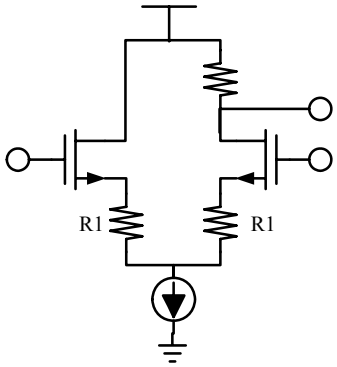


Fig. 2.13. Differential amplifier balun.

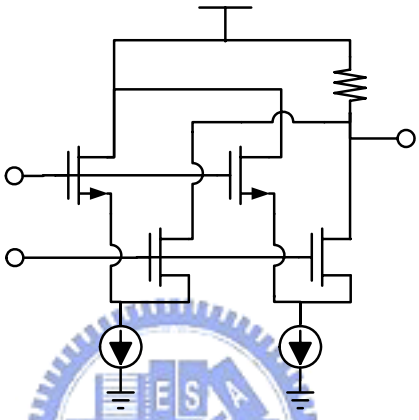


Fig. 2.14. Multi-tanh doublet balun.

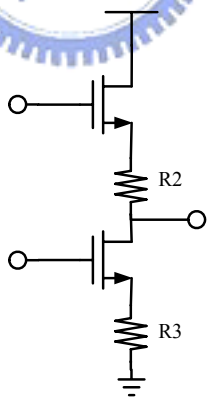


Fig. 2.15. Push-pull balun.

2.4 Voltage-Controlled Oscillator

2.4.1 Principles of VCO

Voltage controlled oscillator is essential building block in communication systems. The VCO is used as local oscillator to up-conversion or down-conversion

signals. The phase noise is the main critical parameters for VCO. Therefore, how to get better phase noise is the most important.

Oscillator can transfer DC power to AC power. Oscillator is an energy transfer device. For steady oscillation, the self-oscillating system must be satisfied Barkhausen's criteria: $|H(j\omega_0)|=1$ and $\angle H(j\omega_0)=0^0$ (or 180^0 of dc feedback is negative). There are two types of analysis methods: positive feedback and negative resistance. In the design of oscillator, the important performance parameters are phase noise, output power, tuning range, and thermal stability. Among these parameters, the most important is the phase noise. Phase noise will influence the signal quality in receiver as shown in Fig. 2.16. When a strong unwanted adjacent channel signal and a weak wanted signal input receiver, worse phase noise will interfere other signal and intermodulation to IF. This interfere the weak wanted signal. Thus, phase noise is the most important in VCO design.

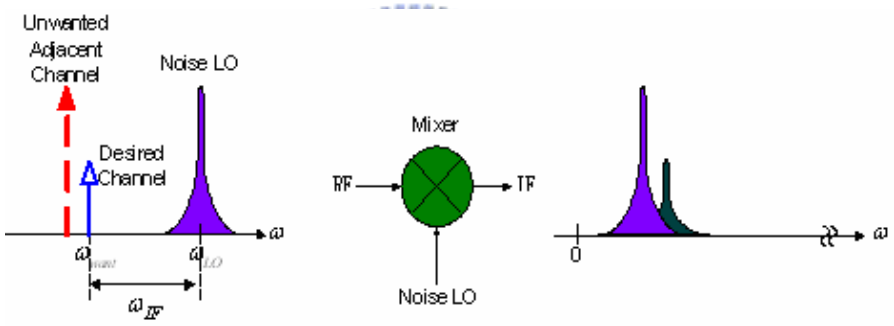


Fig. 2.16. Phase noise in receiver.

LC tank voltage-controlled oscillator and ring oscillator are the two most popular circuits in VCO design. LC tank voltage-controlled oscillator has better phase noise, but tuning range is narrow. Ring oscillator has wider tuning range, but phase noise is worse. We will introduce these two types as following section.

2.4.1.1 LC Tank Voltage-Controlled Oscillator

The concept of LC tank VCO is using negative resistance of active circuit to cancel the resistance of LC tank as shown in Fig. 2.17. Fig. 2.18 shows series transfer to parallel. Fig. 2.19 shows its equivalent resonant model. LC tank oscillator is called negative-Gm oscillator.

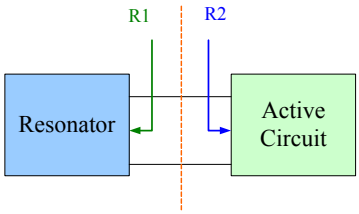


Fig. 2.17. Negative resistance and LC tank resistance.

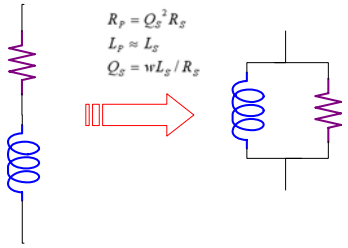


Fig. 2.18. Series to parallel.

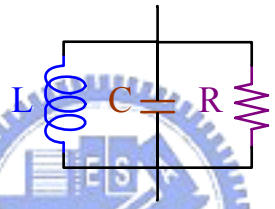


Fig. 2.19. Equivalent resonant model.

The negative resistance is produced from cross-coupled pair which is positive feedback. In Fig. 2.20, we can calculate the impedance seen at the drain of M1 and M2. The impedance is $R_{in} = -2/g_m$. Generally speaking, the phase noise of PMOS-cross coupled pair is better than NMOS-cross coupled pair.

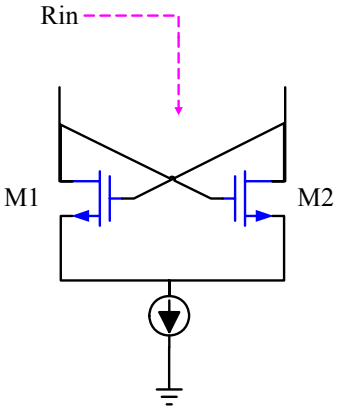


Fig. 2.20. Input impedance of NMOS cross-coupled pair.

Fig. 2.21 shows the complementary cross-coupled pair. Compare with NMOS-cross coupled pair or PMOS-cross coupled pair in the same power consumption, the g_m of complementary cross-coupled pair is larger. Larger gm means faster switching. The rise-time and fall-time of output waveform are more symmetric and the phase noise is better.

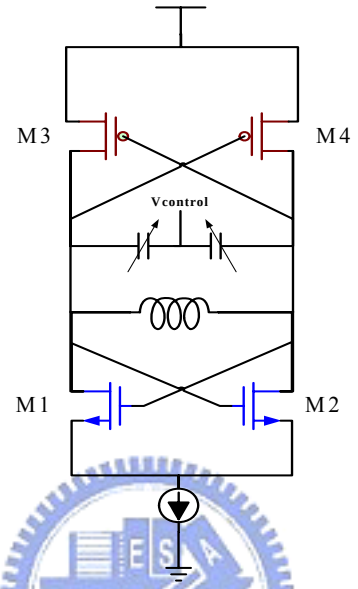


Fig. 2.21. Complementary cross-coupled pair.

2.4.1.2 Ring Oscillator

Fig. 2.22 shows the ring oscillator. It is cascade of N stages with an odd number of inverters is placed in a feedback loop. The period of ring oscillator is equal to 2NTd and the oscillation frequency is $f_0 = \frac{1}{2NT_d}$. There are three advantages of the ring oscillator: high integrated with PLL, smaller die size than LC-tank VCO, and full output voltage swing.

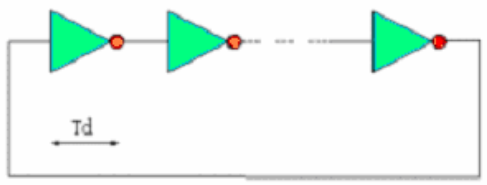


Fig. 2.22. Ring oscillator.

2.4.2 Performance Parameters

2.4.2.1 Phase Noise

An ideal output spectrum of oscillator has only one impulse at the fundamental frequency as shown in Fig. 2.23(a). In an actual oscillator, the frequency spectrum consists of an impulse exhibits skirts around the carrier frequency as show in Fig. 2.23(b). These skirts are called phase noise due to the influence of several kinds of noises. The noise sources such as shot noise, flicker noise and thermal noise. These noises are caused by the resistors, capacitors, inductors, and transistors. Noise injected into an oscillator by noise sources may influence the frequency and the amplitude of the output signal. These phenomenon are called AM, PM and FM noises.

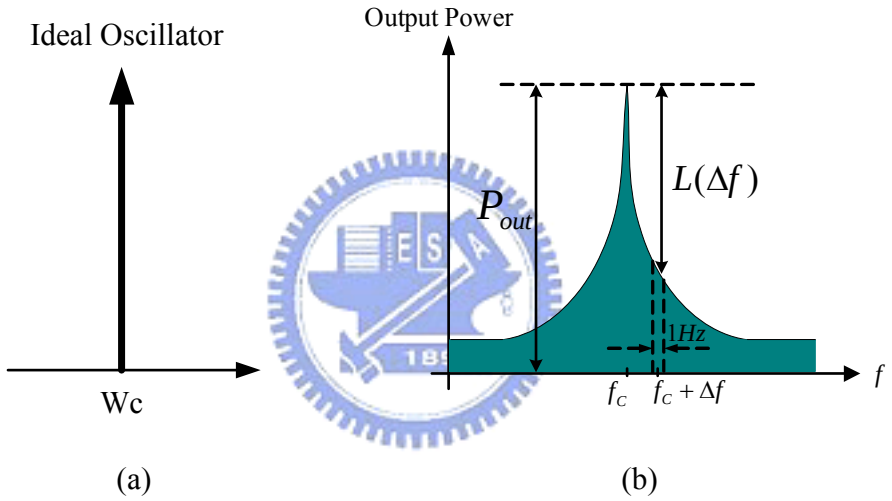


Fig. 2.23. Output spectrum of ideal and actual oscillators.

Fig. 2.24 shows the Lesson's phase noise model. We can express by

$$L(\Delta\omega) = 10\log\left[\frac{1}{2}\frac{FkT}{P_s}\left\{1+\left[\frac{\omega_o}{2Q\Delta\omega}\right]^2\right\}\right]\left[1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right] \tag{2.5}$$

This equation is from the curve fitting after measured results of VCO. Therefore, $\Delta\omega_{1/f^3}$ is from measured results.

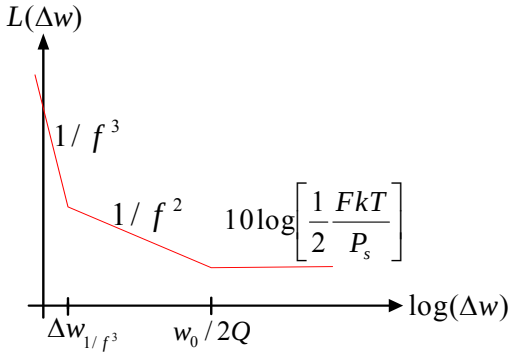


Fig. 2.24. Lesson's phase noise model.

If the output waveform is odd-symmetry, It can suppress $1/f$ noise effetely. This will lower $\Delta w_{1/f^3}$. From equation (2.5), increase Q factor of LC tank and output power can improve phase noise.

2.4.2.2 Frequency Tuning Range

Frequency variation is an important parameter when designing VCO. Because a CMOS oscillator must be designed with a large tuning ranges to overcome process variations. The simplest way to do so is with a varator such as diode varator and MOS varator. The NMOS cross-coupled pair VCO has higher tuning range than double cross-coupled VCO topology for equal effective tank transconductance.

When control voltage change, the bias voltage of transistor will also change. S parameter and Γ_{in} will change according to dc current variation. This will cause output frequency shift. This is called pushing effect. To avoid pushing effect, we can use high quality resonator to reduce the pushing effect. We can also using regulator to overcome pushing effect such as band gap circuits.

Loading effect is another problem. When loading change, its impedance is also change. This will cause output frequency shift. This is called load pulling effect. To avoid this problem, we can use buffer circuit to overcome load pulling effect.

2.4.3 Noise Model of VCO

Phase noise is the most important parameter in the VCO design. There are two models: Leeson's model and Hajimiri model. Lesson has developed a time invariant model to describe the noise of oscillators. Hajimiri proposed a linear time varying phase noise model. The below sections will introduce these two phase noise model.

2.4.3.1 Time Invariant Model

In this section, phase noise analysis is described by using time invariant model. Time invariant means whenever noise sources injection, the phase noise in VCO is the same. In other words, phase shift of VCO caused by noise is the same in any time. Therefore, it's no need to consider when the noise is coming. Suppose oscillator is consists of amplifier and resonator. The transfer function of a bandpass resonator is written as

$$H(j\omega)=\frac{j\omega(1/RC)}{(1/LC)+j\omega(1/RC)-\omega^2} \tag{2.6}$$

The transfer function of a common bandpass is written as

$$H(j\omega)=\frac{j\omega(\omega_o/Q)}{\omega_o^2+j\omega(\omega_o/Q)-\omega^2} \tag{2.7}$$

Compare equation (2.6) with (2.7). Thus,

$$\omega_o=1/LC \quad \text{and} \quad \text{Q}=\omega_o RC \tag{2.8}$$

The frequency $\omega=\omega_o+\Delta\omega$ which is near oscillator output frequency. If $\omega_o \gg \Delta\omega$, we can use Taylor expansion for only first and second terms. Hence

$$H(j\omega)\approx 1+\frac{2}{j(\omega_o/Q)}\cdot\Delta\omega \tag{2.9}$$

The close-loop response of oscillator is expressed by

$$G(j\omega)=\frac{1}{1-H(j\omega)}\approx\frac{-j(\omega_o/Q)}{2\cdot\Delta\omega} \tag{2.10}$$

When input noise density is $S_i(\omega)$, the output noise density is

$$S_o(\omega)=S_i(\omega)\left|G(\omega)\right|^2=FkT\left(\frac{\omega_o}{2Q\Delta\omega}\right)^2 \tag{2.11}$$

The above equation is double sideband noise. The phase noise faraway center frequency $\Delta\omega$ can be expressed by

$$L(\Delta\omega)=10\log\left[\frac{2FKT}{P_s}\cdot\left(\frac{\omega_o}{2Q\Delta\omega}\right)^2\right] \tag{2.12}$$

where P_s is the output power. From equation (2.12), increasing power and higher Q factor can get better phase noise. Increasing power means increasing the power of amplifier. This will decrease noise figure (F) and improve phase noise.

From equation (2.12), we can briefly understand phase noise. But the equation

and actual measured result are different. The VCO spectrum is shown as Fig. 2.24. The phase noise equation can be modified as

$$L(\Delta\omega) = 10\log\left[\frac{2FKT}{P_s}\cdot\left\{1+\left(\frac{\omega_o}{2Q\Delta\omega}\right)^2\right\}\left(1+\frac{\omega_{1/f^3}}{|\Delta\omega|}\right)\right] \tag{2.13}$$

The above equation is called Leeson's model.

2.4.3.2 Time Variant Model

In this section, we use the Hajimiri model to explain the phase noise. At first, we assume that an impulse current injects into a lossless LC tank as illustrated in Fig. 2.25. If the impulse happens to coincide with a voltage maximum as shown in top of Fig. 2.26. The amplitude increase ΔV=ΔQ/C, but the timing of the zero crossings does not change. An impulse injected at any other time displaces the zero crossings as shown in bottom of Fig. 2.26. Hence, an impulsive input produces a step in phase, so that integration is an inherent property of the impulse to phase transfer function. Because the phase displacement depends on when the impulse is applied, the system is time-varying.

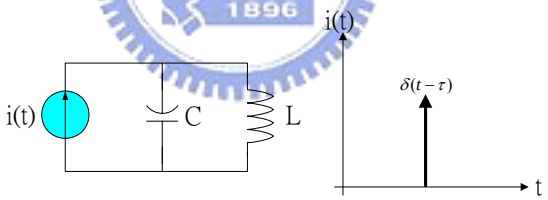


Fig. 2.25. Impulse current injects into LC tank.

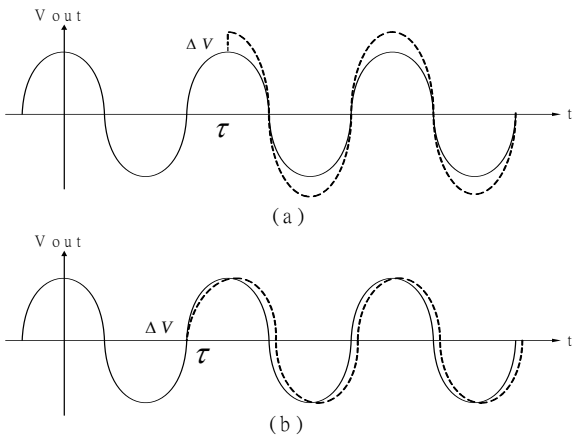


Fig. 2.26. Waveforms for impulse excitation.

Hajimiri proposed a linear time-varying phase noise model which is different from the Lesson's model. The impulse response can be written as

$$h\phi(t,\tau) = \frac{\Gamma(\omega_o\tau)}{q_{\max}}u(t-\tau) \tag{2.14}$$

where $q_{\max}$ is the maximum charge displacement across the capacitor and u(t) is the unit step. The function $\Gamma(x)$ is called the impulse sensitivity function (ISF), and is a frequency and amplitude independent function that is periodic in 2π. Once the ISF has been determined, we may compute the excess phase through use of the superposition integral. Hence

$$\phi(t) = \int_{-\infty}^{\infty} h_\phi(t,\tau)i(\tau)d\tau = \frac{1}{q_{\max}}\int_{-\infty}^{t}\Gamma(\omega_o\tau)i(\tau)d\tau \tag{2.15}$$

This equation can be expanded as a Fourier series:

$$\Gamma(\omega_o\tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_o\tau + \theta_n) \tag{2.16}$$

where the coefficients c_n are real and θ_n is the phase of nth harmonic of the ISF. We assume that noise components are uncorrelated, so that their relative phase is irrelevant, we will still ignore θ_n. Equation (2.16) can be rewritten as

$$\phi(t) = \frac{1}{q_{\max}}\left[\frac{c_0}{2}\int_{-\infty}^{t} i(\tau)d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i(\tau)\cos(n\omega_o\tau)d\tau\right] \tag{2.17}$$

Equation (2.17) allows us to compute the excess phase caused by an arbitrary noise current injected into the system, once the Fourier coefficients of the ISF have been determined. Now we consider the injection of a sinusoidal current whose frequency is near an integer multiple m of the oscillation frequency, so that

$$i(t) = I_m \cos\left[(m\omega_o + \Delta\omega)t\right] \tag{2.18}$$

Substituting (2.18) into (2.17) where $\Delta\omega \ll \omega_o$ and n=m. We can simplify Equation (2.17) as

$$\phi(t) \approx \frac{I_m c_m \sin(\Delta\omega t)}{2q_{\max}\Delta\omega} \tag{2.19}$$

$$V_{out}(t) = \cos\left[\omega_o t + \phi(t)\right] \tag{2.20}$$

Substituting (2.19) into (2.20). Suppose $\frac{I_m c_m}{2q_{\max}\Delta\omega} < 1$. Therefore, the sideband

power relative to the carrier is given by

$$P_{SBC}(\Delta\omega) \approx 10\log\left(\frac{I_m c_m}{4q_{\max}\Delta\omega}\right)^2 \tag{2.21}$$

In general, a noise signal can be separated into two type noise source: white noise and flicker noise. First, input an noise current only with the white noise and its noise power spectral density is $\frac{\overline{i_n^2}}{\Delta f}$. The total single sideband phase noise spectral density in dB below the carrier per unit bandwidth is given by

$$C_{SSB}(\Delta\omega) \approx 10\log\left(\frac{\frac{\overline{i_n^2}}{\Delta f}\sum_{m=0}^{\infty} c_m^2}{4q_{\max}^2\Delta\omega^2}\right) \tag{2.22}$$

According to Parseval's theorem. Thus,

$$\sum_{m=0}^{\infty} c_m^2 = \frac{1}{\pi}\int_0^{2\pi} |\Gamma(x)|^2 dx = 2\Gamma^2_{rms} \tag{2.23}$$

Therefore we can use quantitative analysis to analyze the phase noise sideband power due to the white noise source as following equation

$$L(\Delta\omega) \approx 10\log\left(\frac{\frac{\overline{i_n^2}}{\Delta f}\Gamma^2_{rms}}{2q^2_{\max}\Delta\omega^2}\right) \tag{2.24}$$

where $q_{\max} = CV_{\max}$, $V_{\max}$ is the largest amplitude of VCO, and $\frac{\overline{i_n^2}}{\Delta f} = \frac{4kT}{R}$. Substituting these relations into (2.24). We have

$$L(\Delta\omega) \approx 10\log\left(\frac{4kT}{P_s}\Gamma^2_{rms}\left(\frac{\omega_o}{Q\Delta\omega}\right)^2\right) \tag{2.25}$$

If input noise of VCO is 1/f noise, the power spectral density is written as

$$\overline{i^2_{n,1/f}} = \overline{i_n^2}\frac{\omega_{1/f}}{\Delta\omega} \tag{2.26}$$

where $\omega_{1/f}$ is the 1/f corner frequency of 1/f noise. This equation represents the phase noise spectrum of an arbitrary oscillator in $1/f^2$ region of the phase noise spectrum. Quantitative analysis for the relationship between the device corner 1/f and the $1/f^3$ corner of the phase noise can be illustrated by following equation.

$$L(\Delta\omega) \approx 10\log\left(\frac{\frac{\overline{i_n^2}}{\Delta f}c_0^2}{8q_{\max}^2\Delta\omega^2}\cdot\frac{\omega_{1/f}}{\Delta\omega}\right) \tag{2.27}$$

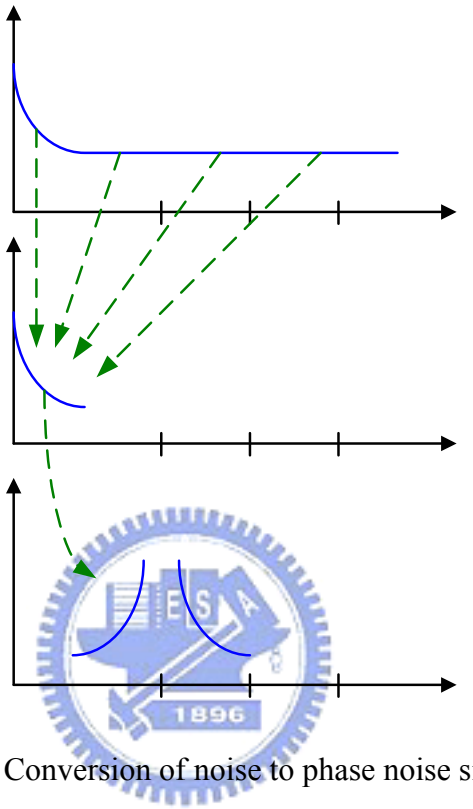


Fig. 2.27. Conversion of noise to phase noise sidebands.

Here we consider the case of a random noise current $i_n(t)$ whose power spectral density has both a flat region and a 1/f region as shown in Fig. 2.27. Noise components located near integer multiples of the oscillation frequency are transformed to low frequency noise sidebands for $S_\Phi(\omega)$ and it's become phase noise in the spectrum of $S_V(\omega)$ as illustrated in Fig. 2.27. It can be seen that the total $S_\Phi(\omega)$ is given by the sum of phase noise contributions from device noise of the integer multiples of ω_o and weighted by the coefficients c_n. The theory predicts the existence of $1/f^2$, $1/f^3$, and flat regions for the phase noise spectrum. The low frequency noise sources are weighted by the coefficient c_0 and show a dependence on the offset frequency. The white noise terms are weighted by other c_n coefficients and give rise to the $1/f^2$ region of phase noise spectrum. From Fig. 2.27, it is obviously that if the original noise current i(t) contains $1/f^n$ low frequency noise terms, they can appear in the phase noise spectrum as $1/f^{n+2}$ regions.

2.5 Phase-Locked Loop Fundamentals

2.5.1 Principles of PLL

Phase-locked loop is a negative feedback loop which the phase of a local oscillator is tracing and locking the phase of the reference frequency. PLL consists of phase-frequency detector, charge pump, loop filter, voltage-controlled oscillator, frequency divider, and reference frequency. It is important to understand each functional block in a PLL. A basic PLL is shown in Fig. 2.28.

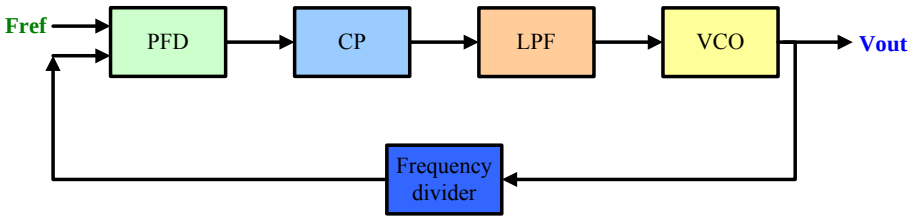


Fig. 2.28. Block diagram of a basic PLL

The phase-frequency detector compares the phase and frequency difference between the reference signal and the signal fed back by the frequency divider then sends a signal to charge pump. According to this signal, the charge pump charges or discharges the loop filter. The filter suppresses unwanted frequency and supplies the VCO with a DC control voltage. The voltage-controlled oscillator converts voltage signal to frequency output. Finally, output signal is fed back to Phase Detector through an integer frequency divider. PLL divides its output frequency by an integer number and adjusts the output frequency to equal to the reference frequency.

These sub-circuits will be presented in the subsequent sections.

2.5.1.1 Voltage-Controlled Oscillator Basics

In a PLL system, voltage-controlled oscillator is the most important component. The frequency of most RF oscillators must be adjustable. So we need an oscillator whose frequency can be varied by a voltage. The transfer function is shown in Fig. 2.29.

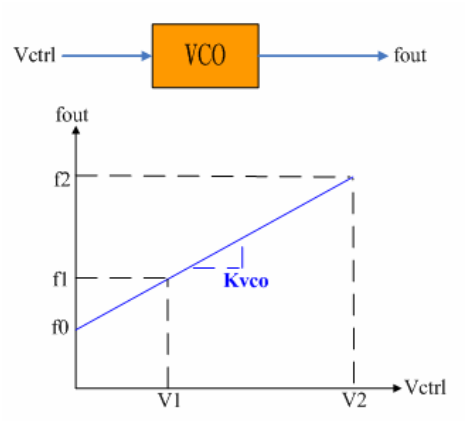


Fig. 2.29. Ideal transfer function of the VCO

An ideal VCO is a circuit that generates a periodic output whose frequency is a linear function of a control voltage. It can expressed as

$$f_{out} = f_0 + K_{vco} \times V_{ctrl} \tag{2.28}$$

where f_0 is the free-running frequency and K_{vco} is the gain of the VCO (specified in rad/s/V). f1 to f2 is the tuning Range. The output of a sinusoid VCO can expressed as

$$v(t) = A \times \cos[2\pi f_o t + 2\pi K_{vco} \int V_{ctrl}(t)dt] \tag{2.29}$$

If control voltage is a fixed voltage, the output can rewritten as

$$v(t) = A \times \cos[(2\pi f_o + 2\pi K_{vco} V)t + \phi_o] \tag{2.30}$$

where ϕ_o represents the initial value of the phase. Thus, if control voltage is constant, the frequency is simply shifted by $(K_{vco} \times V_{ctrl})$.

In a PLL, VCO is a linear varying system. Control voltage is the input and phase is the output. The value is $\left(2\pi \times K_{vco} \times \int V_{ctrl}(t)dt\right)$. Thus, the transfer function of VCO can expressed as

$$\frac{\phi_{out}}{V_{ctrl}}(s) = \frac{2\pi K_{vco}}{s} \tag{2.31}$$

2.5.1.2 Phase Frequency Detector

The operation of a typical PFD is shown in Fig. 2.30. If the input frequency A is leading input B. The output signal Q_A changes to the positive level and Q_B remains at low level. Inversely, if the input frequency of signal A is lagging signal B, then positive pulse appears at Q_B and Q_A keeps at low.

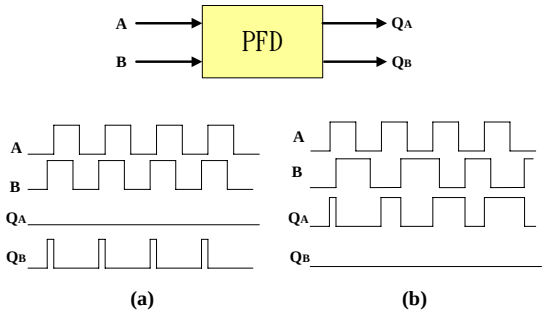


Fig. 2.30. PFD response.

When the frequencies of two input signals are equal, the circuit generates pulses at either QA or QB. Thus, the frequency or phase difference between signal QA and signal QB can be considered as the average value of QA-QB. The output QA and QB are usually called UP and DOWN signals.

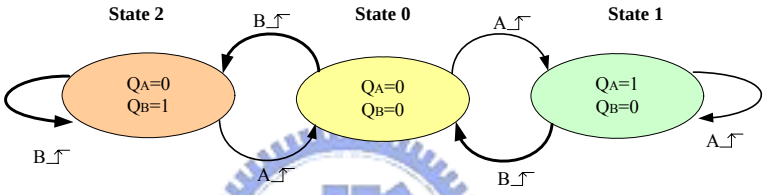


Fig. 2.31. PFD state diagram.

To implement a circuit with the above behavior, at least three logical states are required: QA=QB=0 (State 0), QA=1, QB=0 (State 1), and QA=0, QB=1 (State 2). An edge-triggered sequential circuit is used to avoid dependence of the output upon the duty cycle of the inputs. We assume the circuit can change state only on the rising transitions of A and B. The operations of PFD can be summarized as a state diagram in Fig. 2.31. At the beginning, the PFD is in the State 0, QA=QB=0. If there is a positive edge trigger at the input A, the PFD will transform into the State 1 (QA=1, QB=0). The circuit remains in this state until a positive edge trigger occurs on the input B0. The switching sequence between State 0 and State 2 is similar.

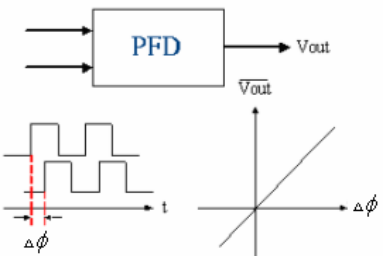


Fig. 2.32. Characteristic of an ideal phase detector.

An ideal PFD produces an output signal whose dc value is linearly proportional to the difference between the phases of two periodic inputs as shown in Fig. 2.32. The relationship can be written as

$$\overline{V_{out}} = K_{PD} \times \Delta\phi \tag{2.32}$$

Where K_{PD} is the gain of the phase-frequency detector and its unit is V/rad. $\Delta\phi$ is the input phase difference.

2.5.1.3 Charge Pump

A charge pump consists of switches and current sources, which is convert the two digital output signals Q_A and Q_B from PFD into charge current. Fig. 2.33 shows the ideal action of a PFD with charge pump. When PFD output UP, S1 is ON and CP charge. When PFD output DOWN, S2 is ON and CP discharge. When locking, PFD don't output UP or DOWN and CP will not charge or discharge. To avoid mismatch, the current I1= I2 = I. The charge current is proportional to the phase error. The relation is $I_p = I \times \frac{\phi_e}{2\pi}$, where ϕe is the phase error and can be written as $\phi_e = \phi_A - \phi_B$.

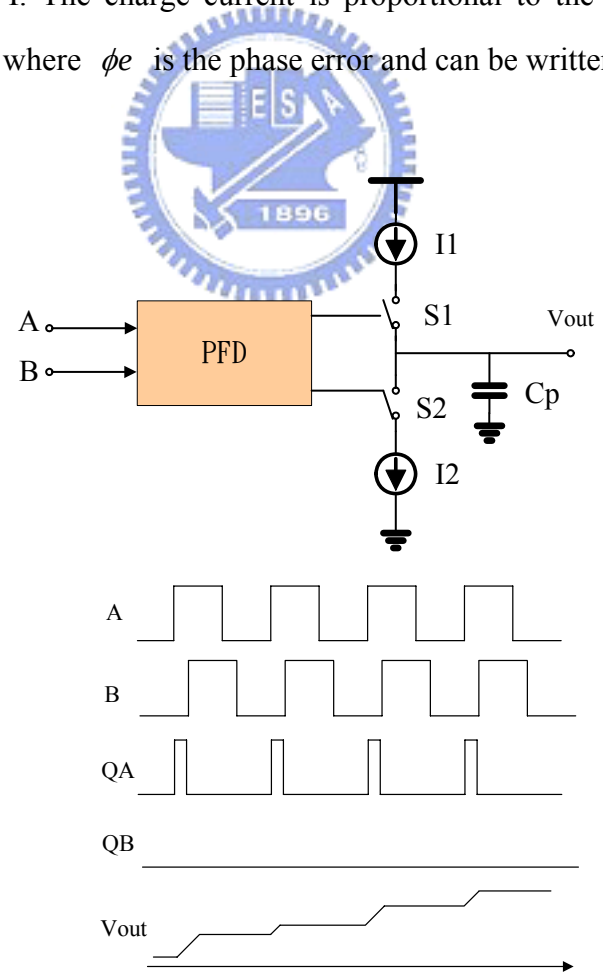


Fig. 2.33. PFD with CP

2.5.1.4 Loop Filter

The standard passive loop filter for a current mode charge pump PLL is shown in Fig. 2.34. We use a second order loop filter to reduce the ripple. A low-pass filter removes the useless messages and provides a stable voltage to the VCO.

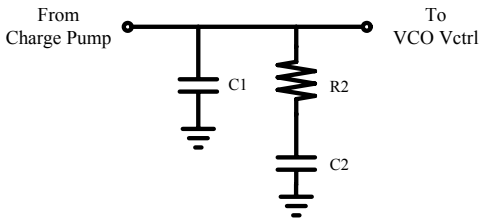


Fig. 2.34. Schematic of second order loop filter.

The PFD's current source outputs charge pump into the loop filter. Then it converts the charge into the VCO's control voltage. The shunt capacitor C1 is to avoid discrete voltage steps at the control port of the VCO due to the instantaneous changes in the charge pump current output. The impedance of the second order filter in Fig. 2.34 is

$$Z(s)=\frac{s(C_2R_2)+1}{s^2(C_1C_2R_2)+s(C_1+C_2)} \tag{2.33}$$

2.5.2 Noise Model in the PLL System

To analyze the noise in the PLL system, we add noise source at the PLL. So we can discuss the influence over the whole system about noise as shown in Fig. 2.35. The input noise sources include the reference frequency (θ_{nin}), VCO (θ_{nvco}), PFD, CP (n_{cp}), LF (n_F) and divider.

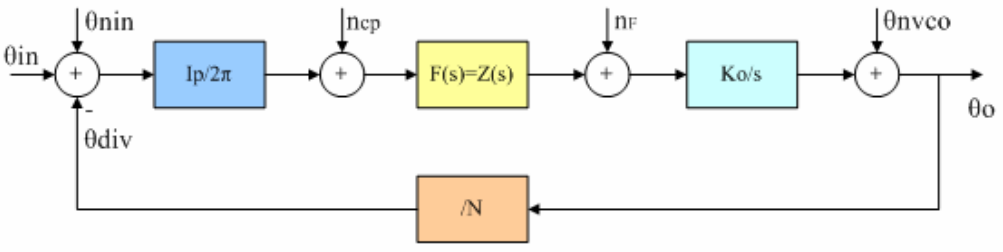


Fig. 2.35. Noise source of PLL.

In Fig. 2.35, $\frac{I_p}{2\pi} = K_d$ is the transfer function of PFD, $Z(s)$ is the transfer function of LF, and $\frac{K_o}{s}$ is the transfer function of VCO. We will discuss the influence of noises over the whole system in the following sections.

2.5.2.1 Phase Noise of PLL with PI Filter

In VCO, the transfer function can be written as

$$\frac{\theta_o}{\theta_{nvco}} = \frac{1}{1 + K_d F(s) \frac{K_o}{s} \frac{1}{N}} \tag{2.34}$$

If PI filter is adopted as shown in Fig. 2.36, the transfer function F(s) is written as

$$F(s) = K_h \frac{(s + \omega_2)}{s} \tag{2.35}$$

where $K_h = R_2 / R_1$, then (2.34) can be rewritten as

$$\begin{aligned} \frac{\theta_o}{\theta_{nvco}} &= \frac{1}{1 + K_d K_h \frac{(s+\omega_2)}{s} \frac{K_o}{s} \frac{1}{N}} = \frac{s^2}{s^2 + Ks + K\omega_2} \\ &\cong \frac{s^2}{(s+K)(s+\omega_2)} \left(\omega_2 \ll K = \frac{K_d K_h K_o}{N}\right) \end{aligned} \tag{2.36}$$

From equation 2.36, the transfer function is a high pass filter as shown in Fig. 2.37(a).

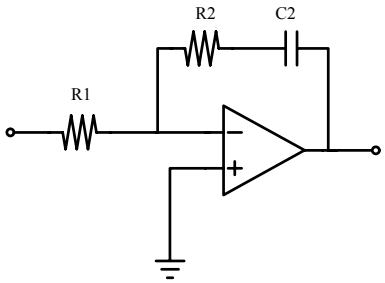


Fig. 2.36. PI type.

In reference frequency, the transfer function can be written as

$$\frac{\theta_o}{\theta_{nin}} = \frac{K_d F(s) \frac{K_o}{s}}{1 + K_d F(s) \frac{K_o}{s} \frac{1}{N}} \tag{2.37}$$

If PI filter is adopted, the transfer function is

$$F(s) = K_h \frac{(s+\omega_2)}{s} \tag{2.38}$$

Thus

$$\frac{\theta_o}{\theta_{nin}} = \frac{K_d K_h \frac{s+\omega_2}{s}\frac{K_o}{s}}{1 + K_d K_h \frac{(s+\omega_2)}{s}\frac{K_o}{s}\frac{1}{N}} = \frac{NK(s+\omega_2)}{s^2 + Ks + K\omega_2}$$
$$\cong \frac{NK}{(s+K)} (\omega_2 \ll K = \frac{K_d K_h K_o}{N}) \tag{2.39}$$

The transfer function is a low pass filter as shown in Fig. 2.37(b).

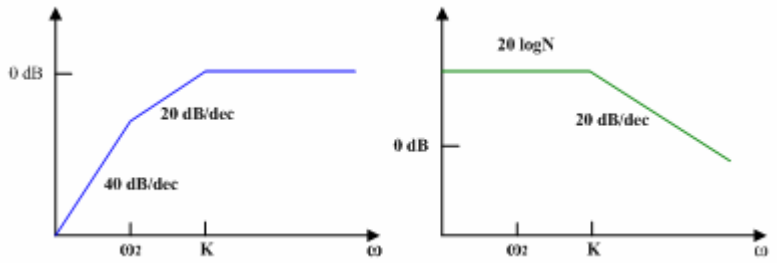


Fig. 2.37. Transfer function: (a)VCO (b)reference frequency

2.5.2.2 Phase Noise of PLL with Charge Pump

PI filter need one operation amplifier. It's more complicate and expensive than charge pump. Therefore, charge pump is more popular than PI filter. Charge pump has the same function as operation amplifier does. If we adopts charge pump, the transfer function of first order R_2C_2 filter can be written as

$$Z(s) = K_h \frac{(s+\omega_2)}{s} \tag{2.40}$$

where $K_h = R_2$. If we adopt second order filter as shown in Fig. 2.38, the transfer function is written as

$$Z(s) = K_h \frac{(s+\omega_2)}{s(\frac{s}{\omega_3}+1)} \tag{2.41}$$

where $K_h = \frac{C_2 R_2}{C_1 + C_2}$, $\omega_2 = \frac{1}{C_2 R_2}$, and $\omega_3 = \frac{C_1 + C_2}{C_1 C_2 R_2}$.

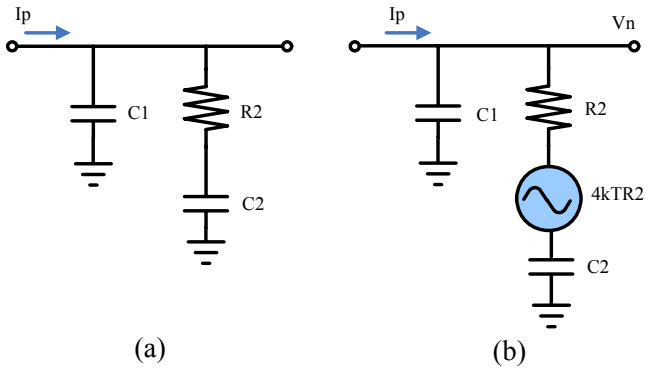


Fig. 2.38. Second order loop filter.

In reference frequency, the transfer function can be written as

$$\frac{\theta_o}{\theta_{nin}} = \frac{\frac{I_p}{2\pi} Z(s) \frac{K_o}{s}}{1 + \frac{I_p}{2\pi} Z(s) \frac{K_o}{s} \frac{1}{N}} \tag{2.42}$$

In VCO, the transfer function can be written as

$$\frac{\theta_o}{\theta_{nvco}} = \frac{1}{1 + \frac{I_p}{2\pi} Z(s) \frac{K_o}{s} \frac{1}{N}} \tag{2.43}$$

In CP, the transfer function can be written as

$$\frac{\theta_o}{n_{cp}} = \frac{Z(s) \frac{K_o}{s}}{1 + \frac{I_p}{2\pi} Z(s) \frac{K_o}{s} \frac{1}{N}} \tag{2.44}$$

In LF, the transfer function can be written as

$$\frac{\theta_o}{n_F} = \frac{T_1(s) \frac{K_o}{s}}{1 + \frac{I_p}{2\pi} Z(s) \frac{K_o}{s} \frac{1}{N}} \tag{2.45}$$

where n_F is the thermal noise of R_2, and $T_1 = V_n / \sqrt{4kTR_2}$. V_n is the output voltage of loop filter. T1 is expressed as

$$T_1 = \frac{\frac{1}{sC_1}}{R_2 + \frac{1}{sC_1} + \frac{1}{sC_2}} \tag{2.46}$$

From equation (2.42), the phase noise contributed from crystal is written as

$$L_{crystal}\{s\} = \left(\frac{\phi_n^2}{\Delta\omega}\right)_{crystal} \cdot \left[\frac{\frac{I_p}{2\pi} Z(s) \frac{2\pi K_{vco}}{s}}{1 + \frac{I_p}{2\pi} Z(s) \frac{2\pi K_{vco}}{s} \frac{1}{N}}\right]^2 \tag{2.47}$$

where $\left(\frac{\phi_n^2}{\Delta\omega}\right)$ is the phase noise of crystal, $2\pi K_{vco} \equiv K_o$, and s represents $j\omega_m$ 。

From equation (2.43), the phase noise contributed from VCO is written as

$$L_{vco}\{s\} = \left(\frac{\phi_n^2}{\Delta\omega}\right)_{vco} \cdot \left[\frac{1}{1 + \frac{I_p}{2\pi} Z(s) \frac{2\pi K_{vco}}{s} \frac{1}{N}}\right]^2 \tag{2.48}$$

where $\left(\frac{\phi_n^2}{\Delta\omega}\right)$ is the phase noise of VCO.

The phase noise contributed from charge pump must calculate the noise of each transistor. For simplify calculation, charge or discharge is using one transistor. Derived as

$$L_{cp}\{s\} = \sum\left(\frac{\overline{i_n^2}}{\Delta\omega}\right) \frac{\Delta t}{T_{ref}} \cdot \frac{1}{2} \cdot \left[\frac{Z(s) \frac{2\pi K_{vco}}{s}}{1 + \frac{I_p}{2\pi} Z(s) \frac{2\pi K_{vco}}{s} \frac{1}{N}}\right]^2 \tag{2.49}$$

where $\frac{\overline{i_n^2}}{\Delta\omega} = \frac{4KT\gamma g_m}{2\pi}$, γ is 2.5, Δt is the charge and discharge time when system is locking, T_{ref} is periodic of reference signal, and 1/2 is double sideband.

The phase noise contributed from R2, it can be derived as

$$L_{R_2}\{s\} = \frac{4KTR_2}{2\pi} \cdot \frac{1}{2} \cdot \left[\frac{\frac{1}{sC_1}}{\frac{1}{sC_1} + R_2 + \frac{1}{sC_1}}\right]^2 \left[\frac{\frac{2\pi K_{vco}}{s}}{1 + \frac{I_p}{2\pi} Z(s) \frac{2\pi K_{vco}}{s} \frac{1}{N}}\right]^2 \tag{2.50}$$

where $\frac{4KTR_2}{2\pi}$ is the thermal noise of R2 and 1/2 is double sideband.

2.6 The 24 GHz Radar System

The advanced sensing and automatic control is the trend for recent vehicle developments. To achieve collision avoidance, Radar sensor must detect distance and speed. Sometimes Radar sensor also must detect many objects simultaneous. In recent research, there are many specifications such as 10, 18, 24, 38, and 77 GHz for different applications. Among these, 24 GHz is short-ranging radar and it may become the next product in automobile market. Fig. 2.39 shows the block diagram of 24GHz Radar sensor system. This system responsible for signal receives and transmits. It includes antenna, BPF, LNA, mixer, VCO, amplifier, DSP, network transceiver, and linear ramp controller. MCU receive instruction from DSP and produce linear ramp to control VCO.

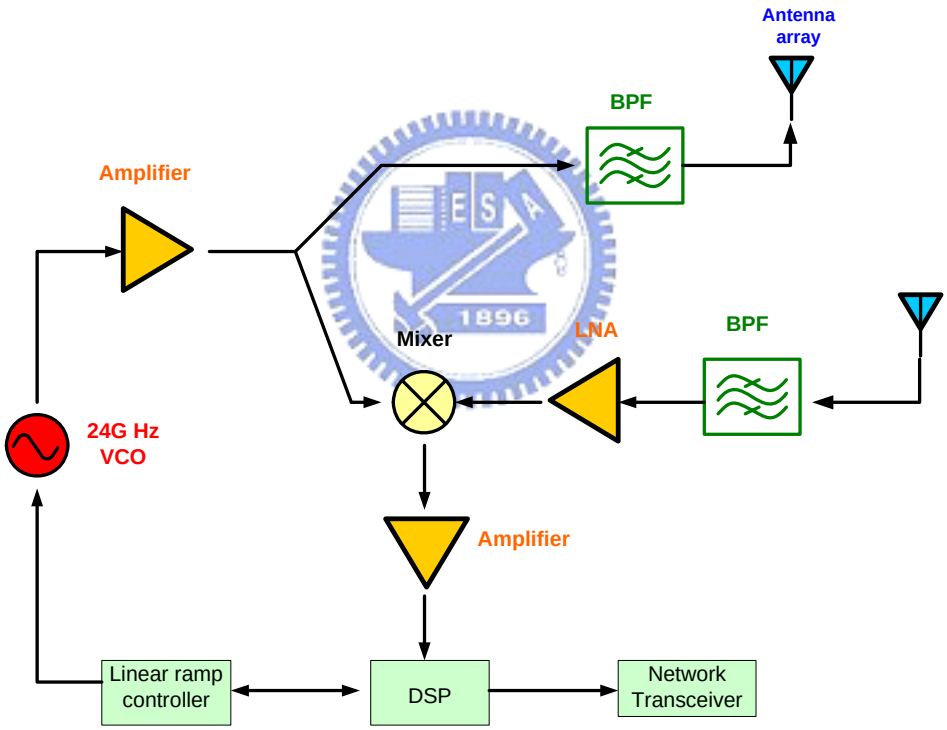


Fig. 2.39. Block diagram of 24GHz Radar system.

Chapter 3 *The Design of Wideband Mixer*

In this chapter, two kinds of wideband down conversion mixers for ultra-wideband applications and one kind of single-sideband mixer for UWB synthesizer are presented.

3.1 The Design of Wideband Down Conversion Mixer

In this section, a wideband mixer for multi-band orthogonal frequency division multiplexing ultra-wideband applications is designed. First, the operating principle of the feedforward compensated high-linearity differential transconductor is introduced. Then, we explain the operating theory of the proposed wideband mixer. Finally, the simulation and measurement results are discussed.

3.1.1 Feedforward Compensated Differential Tansconductor Analysis

3.1.1.1 Modified Differential Transconductor Circuit

The first stage of mixer must have high linearity to handle the large input signals from LNA without significant intermodulation [23]. To improve linearity in Gilbert

mixer, many methods have being used such as adding source degeneration resistors below the gain stage [24], bisymmetric Class-AB input stage [23], multiple gated transistor [22], and common-source and common-emitter RF transconductors [25].

The designed mixer adopting modified feedforward compensated differential transconductor, as like as the transconductor stage in Gilbert mixer, is shown in Fig. 3.1. The transconductor consists of degenerate common-source stages (M1, M2) and degenerate common-gate stages (M3, M4). The input stage is the degenerate common-source stages and compensated by degenerate common-gate stages, which can achieve feedforward distortion linearization [26]-[27]. The feedforward compensated differential transconductor provides accurate input impedance and high intermodulation intercepts. The modified feedforward compensated differential transconductor has less distortion than Class-AB [19], multi-tanh [20], degenerated differential pair, and cascode compensation [21].

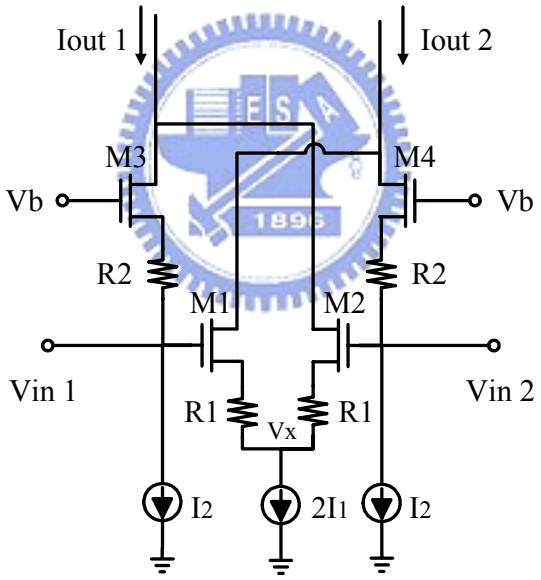


Fig. 3.1. Modified differential transconductor.

3.1.1.2 Modified Differential Transconductor Analysis

In order to appreciate the reduction of nonlinearity obtained by modified feedforward compensated differential transconductor, let us consider the harmonic distortion cancellation in Fig. 3.1. Assuming the circuit is symmetric. All MOS are saturated and $\lambda=0$. A harmonic balance analysis is then used to express the harmonics.

Using one-half of the degenerate common-source (M2) and degenerate common-gate (M3) in Fig. 3.1. Suppose a single tone signal $V_m \cos \omega t$ is applied to input. The voltage of $Vin1 = V_{dc} + V_m \cos \omega t$ and $Vin2 = V_{dc} - V_m \cos \omega t$. Where V_{dc} denotes the DC level, V_m denotes the amplitude of the sinusoidal signal, and ω is the frequency of the sinusoidal signal. We can write the drain current of M3 by

$$I_{ds3} = \frac{1}{2}\mu_n C_{OX} \frac{W_3}{L_3}\left[V_b - \left(I_2 R_2 + V_{dc} + V_m \cos \omega t\right) - V_{TH}\right]^2 = I_2 \tag{3.1}$$

Equation (3.1) can be expressed as

$$R_2^2 I_2^2 + \left[2R_2 V_m \cos \omega t - 2R_2\left(V_b - V_{TH} - V_{dc}\right) - \frac{1}{K_3}\right] I_2 - 2V_m \cos \omega t\left(V_b - V_{TH} - V_{dc}\right) + \left(V_b - V_{TH} - V_{dc}\right)^2 + V_m^2 \cos^2 \omega t = 0 \tag{3.2}$$

where

$$K_3 = \frac{1}{2}\mu_n C_{OX} \frac{W_3}{L_3} \tag{3.3}$$

From equation (3.2), the drain current of M3 can be found by Taylor series and examining only the first three harmonics.

The result is

$$\begin{aligned} I_2 = {} & \frac{1}{R_2^2 K_3} + \frac{2\left(V_b - V_{TH} - V_{dc}\right)}{R_2} - K_3\left(V_b - V_{TH} - V_{dc}\right)^2 + 2R_2 K_3^2\left(V_b - V_{TH} - V_{dc}\right)^3 + \left[3R_2 K_3^2\left(V_b - V_{TH} - V_{dc}\right) - \frac{K_3}{2}\right] V_m^2 \\ & + \left[2K_3\left(V_b - V_{TH} - V_{dc}\right) - 6R_2 K_3^2\left(V_b - V_{TH} - V_{dc}\right)^2 - \frac{2}{R_2} - \frac{3R_2 K_3^2 V_m^2}{2}\right] V_m \cos \omega t \\ & + \left[3R_2 K_3^2\left(V_b - V_{TH} - V_{dc}\right) - \frac{K_3}{2}\right] V_m^2 \cos 2\omega t \\ & - \frac{R_2 K_3^2 V_m^3}{2} \cos 3\omega t \end{aligned} \tag{3.4}$$

The drain current of M2 is given by

$$I_{ds2} = \frac{1}{2}\mu_n C_{OX} \frac{W_2}{L_2}\left[V_{dc} - V_m \cos \omega t - \left(I_1 R_1 + V_x\right) - V_{TH}\right]^2 = I_1 \tag{3.5}$$

Equation (3.1) can be expressed as

$$R_1^2 I_1^2 + \left[2R_1 V_m \cos \omega t + 2R_1\left(V_x + V_{TH} - V_{dc}\right) - \frac{1}{K_2}\right] I_1 + 2V_m \cos \omega t\left(V_x + V_{TH} - V_{dc}\right) + \left(V_x + V_{TH} - V_{dc}\right)^2 + V_m^2 \cos^2 \omega t = 0 \tag{3.6}$$

where

$$K_2 = \frac{1}{2}\mu_n C_{OX}\frac{W_2}{L_2} \tag{3.7}$$

From equation (3.6), the drain current of M2 can be found by Taylor's series expansion and examining only the first three harmonics.

The result is

$$\begin{aligned} I_1 = {} & K_2\left(V_x + V_{TH} - V_{dc}\right)^2 + 2R_1K_2^2\left(V_x + V_{TH} - V_{dc}\right)^3 + \left[\frac{K_2}{2} + 3R_1K_2^2\left(V_x + V_{TH} - V_{dc}\right)\right]V_m^2 \\ & + \left[2K_2\left(V_x + V_{TH} - V_{dc}\right) + 6R_1K_2^2\left(V_x + V_{TH} - V_{dc}\right)^2 + \frac{3R_1K_2^2}{2}V_m^2\right]V_m\cos\omega t \\ & + \left[\frac{K_2}{2} + 3R_1K_2^2\left(V_x + V_{TH} - V_{dc}\right)\right]V_m^2\cos 2\omega t \\ & + \frac{R_1K_2^2}{2}V_m^3\cos 3\omega t \end{aligned} \tag{3.8}$$

The total output current can be written as $Iout_1 = I_1 + I_2$. After substituting (3.4) and (3.8) into $Iout_1 = I_1 + I_2$. The coefficients of fundamental tone, 2nd harmonic, and 3rd harmonic for the output1 current can be written as (3.9), (3.10), and (3.11). A_F means the amplitude of the fundamental tone. A_{HD2} means the amplitude of the second harmonic. A_{HD3} means the amplitude of the third harmonic.

$$A_F = \left\{2\left[K_3\left(V_b - V_{TH} - V_{dc}\right) + K_2\left(V_x + V_{TH} - V_{dc}\right)\right] + 6\left[R_1K_2^2\left(V_x + V_{TH} - V_{dc}\right)^2 - R_2K_3^2\left(V_b - V_{TH} - V_{dc}\right)^2\right] - \frac{2}{R_2} + \left[\frac{3}{2}V_m^2\left(R_1K_2^2 - R_2K_3^2\right)\right]\right\}V_m \tag{3.9}$$

$$A_{HD2} = \left[3R_2K_3^2\left(V_b - V_{TH} - V_{dc}\right) + 3R_1K_2^2\left(V_x + V_{TH} - V_{dc}\right) + \frac{K_2}{2} - \frac{K_3}{2}\right]V_m^2 \tag{3.10}$$

$$A_{HD3} = \left(\frac{R_1K_2^2}{2} - \frac{R_2K_3^2}{2}\right)V_m^3 \tag{3.11}$$

From (3.10), the second-order distortion cancellation can be realized. If it follows that

$$3R_2K_3^2\left(V_b - V_{TH} - V_{dc}\right) - \frac{K_3}{2} = -3R_1K_2^2\left(V_x + V_{TH} - V_{dc}\right) - \frac{K_2}{2} \tag{3.12}$$

If we choose the proper values of R1, R2, W2, W3, L2, L3, Vb, Vx, and Vdc. The second-order distortion can be cancelled and we have

$$\left(V_x + V_{TH} - V_{dc}\right) = -\left(V_b - V_{TH} - V_{dc}\right) + \frac{K_3}{6R_1K_2^2} - \frac{K_2}{6R_1K_2^2} \tag{3.13}$$

From (3.11), the third-order distortion cancellation is possible. If

$$R_1 K_2^2 = R_2 K_3^2 \tag{3.14}$$

Then the third-order distortion coefficient A_{HD3} can be zero. This condition can be realized by proper selection R1, R2, W2, W3, L2, and L3.

If second-order and third-order distortion cancellation were done, we can substituting (3.13) and (3.14) into (3.9) and the fundamental tone can be expressed as

$$A_F = \left[\frac{K_3 - K_2}{3R_1 K_2} + \frac{(K_3 - K_2)^2}{6R_1 K_2^2} - \frac{2}{R_2} \right] V_m \tag{3.15}$$

From equation (3.12) and (3.14), distortion cancellation is achieved by the proper selection of bias voltage and degeneration resistance. On the other way, the values of R1, R2, W2, W3, L2, L3, Vb, Vx, and Vdc are important when designing.

The degenerate common-source pair compensated by a pair of degenerate common-gate providing distortion reduced is derived. The modified feedforward compensated differential transconductor offers better linearity over a wideband frequency. This circuit is suitable for wideband mixer as a transconductor to lower distortion.

3.1.2 LC Folded Cascode Mixer

The mixer gain is proportional to g_m, and higher overdrive voltage means higher gain. To use feedforward compensated differential transconductor in Gilbert mixer, the supply voltage is critical to keep the driver FETs always in saturation region. In order to overcome this problem, LC folded cascode circuit can be used to get larger voltage headroom. Therefore, it can keep the driver FETs always in saturation region [22],[24],[28],[29]. The operation of the LC folded cascode mixer is similar to the Gilbert mixer. A LC folded cascode mixer with an added resistance is shown in Fig. 3.2. The parallel RLC tank is a tuned load that can be used to provide larger output swing. At DC, inductor is shorted and no voltage drop across the tuned load. Therefore, the more voltage headroom is provided. At resonating frequency of the parallel RLC tank, the inductor and capacitor are open circuit at output frequency while consuming no voltage drops. The resonating frequency and 3dB bandwidth can be given by

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{3.16}$$

$$BW = \frac{1}{RC} \tag{3.17}$$

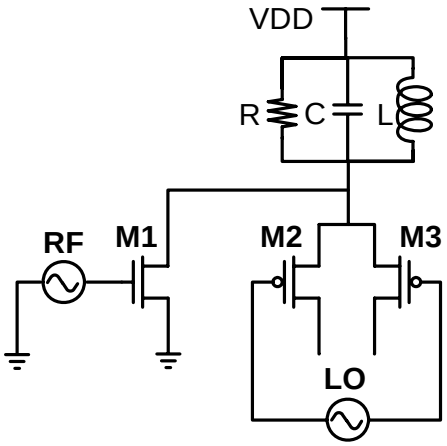


Fig. 3.2. LC folded cascode mixer with an added resistance.

3.1.3 Proposed Mixer Design

Fig. 3.3 shows the proposed mixer, which is composed of an LC folded cascode mixer, a feedforward compensated differential transconductor, and common-source amplifiers.

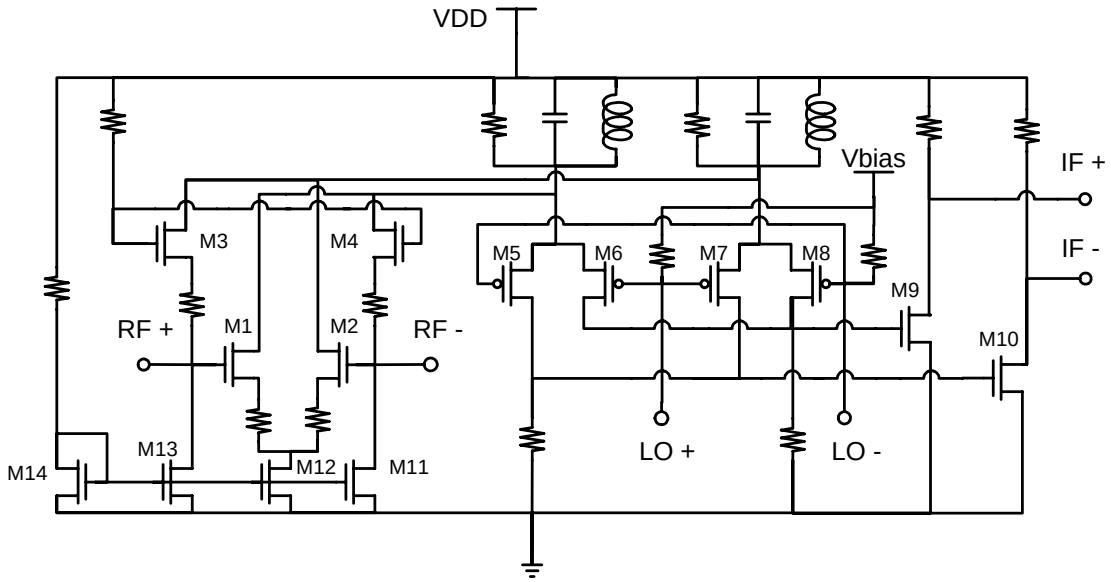


Fig. 3.3. Schematic of the proposed mixer.

Functionally, input differential signal into the feedforward compensated differential transconductor to amplify the input signal firstly. The small-signal voltage is converted to a small-signal current at this stage. The current signal is down-converted by the switching pair. Then the load stage provides loading to preceding stages and converts the current signals back to voltage signals. Finally, common sources are used as output buffers for testing and matching purposes.

3.1.4 Simulation and Measurement Results

In this section, we show the measurement setups and results of the proposed mixer. The measurements were performed with the chip directly mounted on a 28×28 mm^2 and thickness of 20 mil RO4003 microwave substrate with SMA connectors. Fig. 3.4 shows the test board with die mounted on RO4003 printed circuit board (PCB). Fig. 3.5 shows the PCB layout. The chip layout and microphotograph are shown in Fig. 3.6 and Fig. 3.7. The die size is 0.70×0.58 mm^2 including pads. Fig. 3.8 shows the measurement setup of power conversion gain. The DC power supplier provide 1.8V&1.2V dc source to mixer in measurement. The connectors and lines both result in loss in measurement.

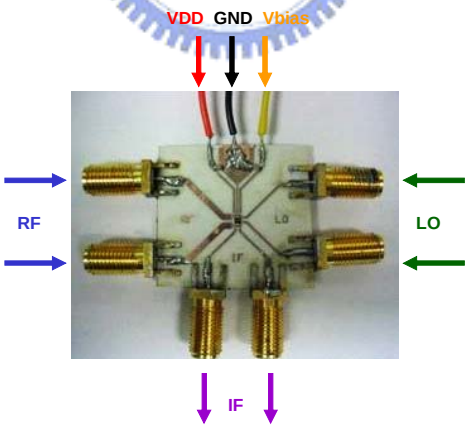


Fig. 3.4. Die bonded to the PCB.

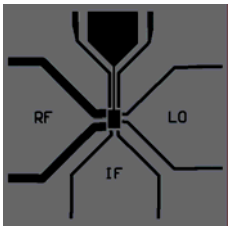


Fig. 3.5. PCB layout of the proposed mixer.

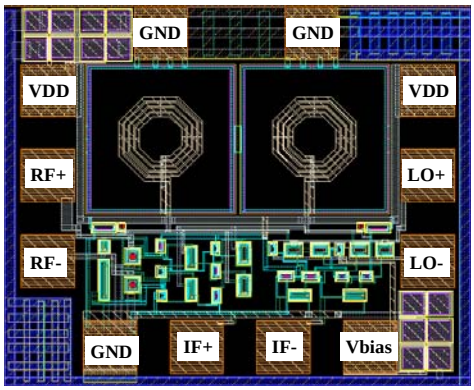


Fig. 3.6. The chip layout of the proposed mixer.

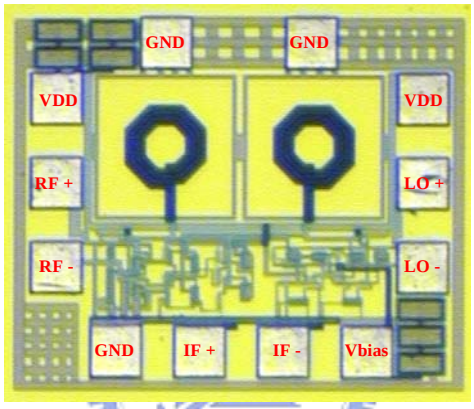


Fig. 3.7. Microphotograph of the proposed mixer.

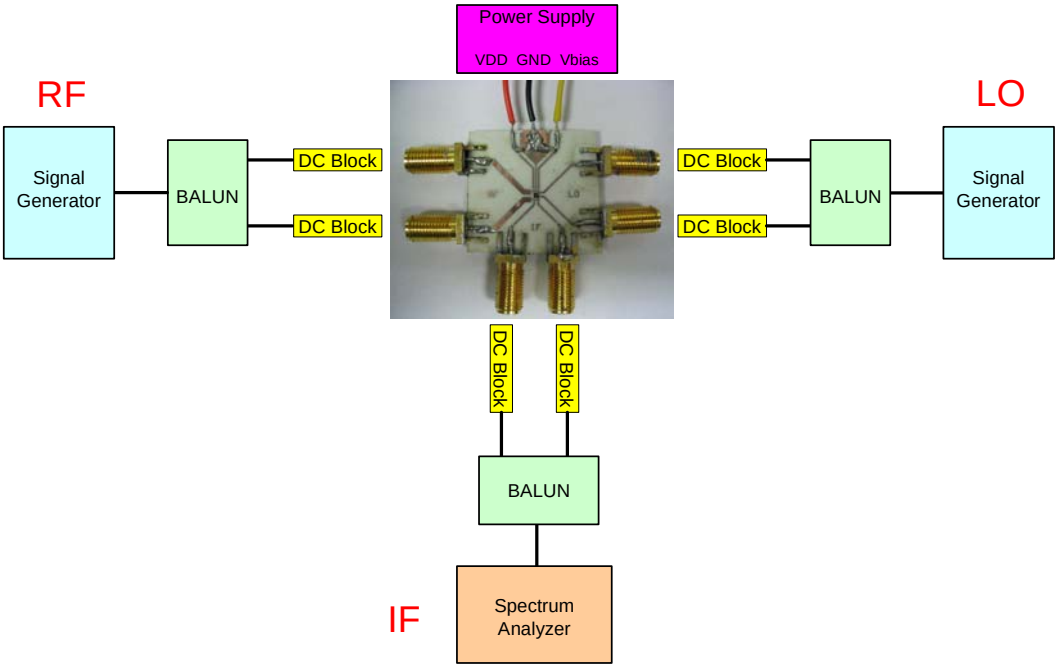


Fig. 3.8. Measurement setup of power conversion gain.

The mixer is designed using TSMC 0.18μm CMOS technology. All measurements were done at 1.8 V and 1.2 V supply voltage and the power consumption is 14.4 mW including the output buffer. Fig. 3.9 illustrates the conversion gain versus the RF frequency with both RF and LO ports swept in frequency from 2 to 12 GHz, a fixed IF frequency of 50 MHz, RF power of -30 dBm, and LO power of -5 dBm. The conversion gain is 3.3 ± 1.5dB with a bandwidth of 2.4 to 10.7 GHz. Simulation1 means the bond wire equivalent model is using 20mil. But it's not 20mil actually. Simulation2 is the practical bond wire length approximate calculated from the chip. The measured RF return loss is better than 10 dB with a bandwidth of 2.4 to 10.7 GHz as shown in Fig. 3.10. The measured IF return loss is better than 10 dB at 50MHz as shown in Fig. 3.11. The measured RF-to-IF, LO-to-IF and RF-to-LO isolation shown in Fig. 3.12 are better than 20 dB. Fig. 3.13 and Fig. 3.14 show the linearity of the mixer as a function of frequency. The measured IIP3 is 4 ~ 6.9 dBm and P1dB is -2.8 ~ -5.8 dBm in the bandwidth of 2.4 to 10.7 GHz. Table 3.1 shows the performance summary of simulated and measured results.

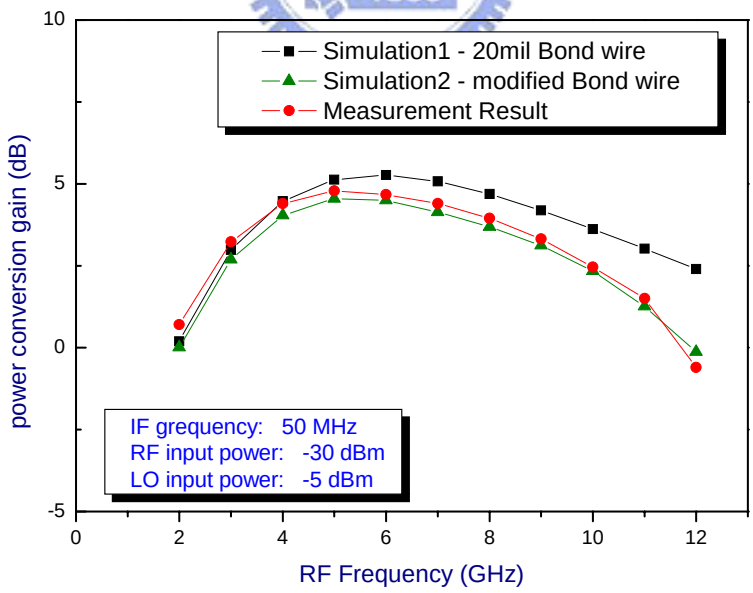


Fig. 3.9. Simulated and measured power conversion gain versus RF frequency with the IF frequency is 50MHz, RF power is -30dBm, and LO power is -5 dBm.

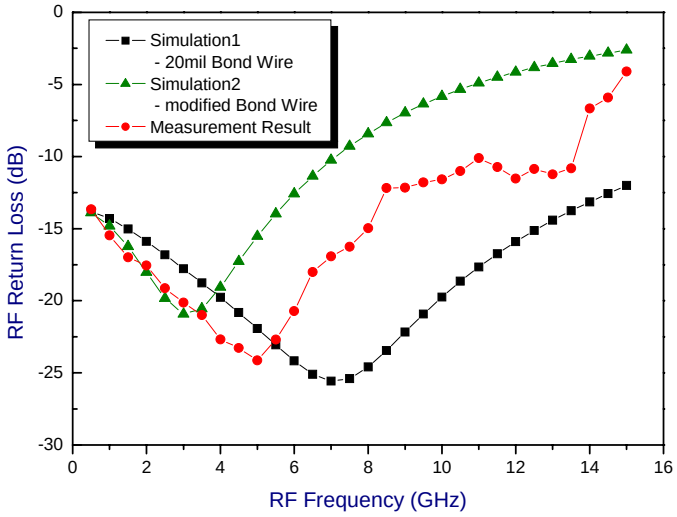


Fig. 3.10. Simulated and measured RF return loss versus RF frequency.

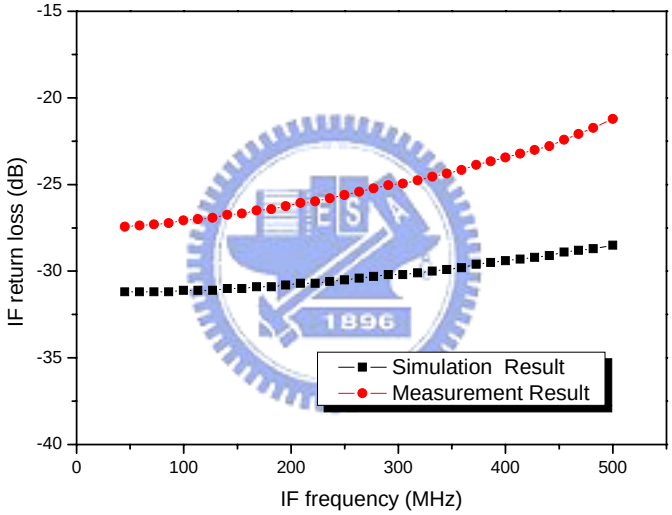


Fig. 3.11. Simulated and measured IF return loss versus IF frequency.

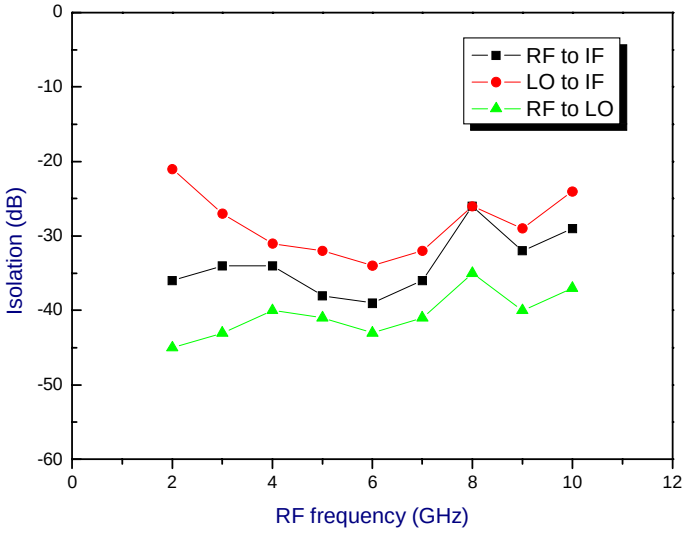


Fig. 3.12. Measured Isolation versus RF frequency.

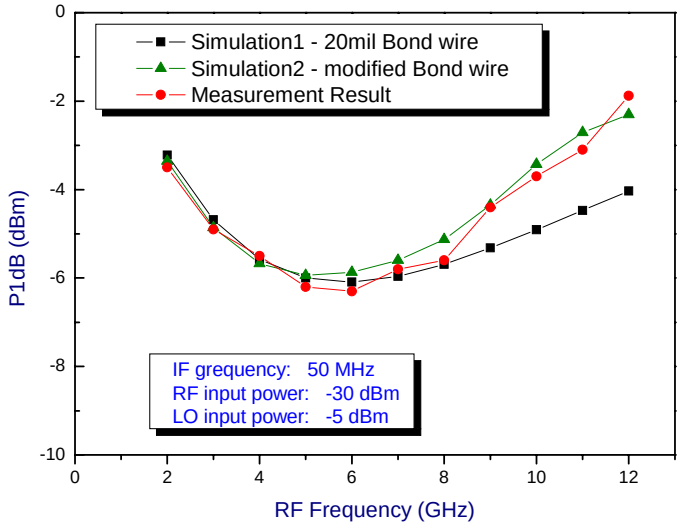


Fig. 3.13. Simulated and measured P1dB versus RF frequency.

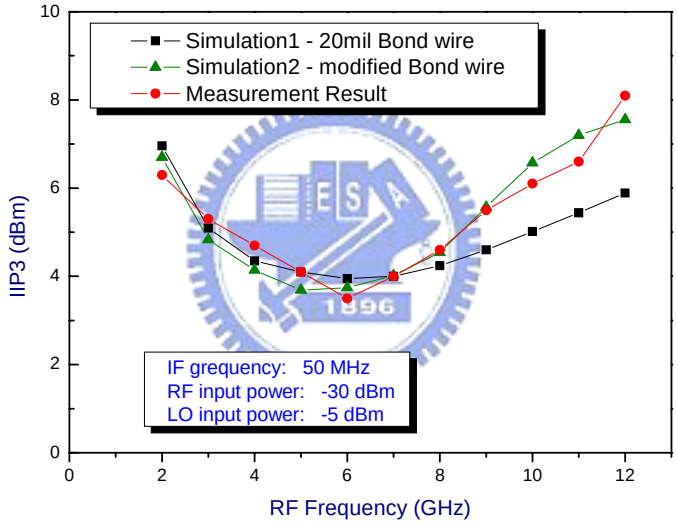


Fig. 3.14. Simulated and measured IIP3 versus RF frequency.

Parameters	Simulation results	Measurement results
Process	TSMC 0.18um CMOS	
Frequency (GHz)	2.2 ~ 12.5	2.4 ~ 10.7
IF Frequency (MHz)	50	
Supply voltage (V)	1.8	
Power conversion gain (dB)	3.7 ± 1.5	3.3 ± 1.5
RF Input Return Loss (dB)	< -10	< -10
Input P1dB (dBm)	-6.0 ~ -3.1	-5.8 ~ -2.8
IIP3 (dBm)	3.9 ~ 7.0	4 ~ 6.9
LO power (dBm)	-5	
Die area (mm^2)	0.70X0.58	
Power Consumption (mW)	11	14

Table 3.1 Summary of simulation and measurement results

3.1.5 Comparison and Summary

The comparison of the proposed mixer against recently reported wideband mixer is shown in Table 3.2, it indicates that the proposed mixer provides better linearity, more compact chip size, and acceptable conversion gain and power consumption. In Ref. [32], the power consumption of mixer core is 71mW and the RF input return loss is better than 10dB for frequency from 10GHz to 21GHz.

Ref.	[30]	[31]	[32]	[33]	this work
Technology	1.4um GaInP/ GaAs	1.4um GaInP/ GaAs	0.18um CMOS	0.18um CMOS	0.18um CMOS
IF frequency (MHz)	150	350	10	528	50
Frequency (GHz)	DC ～ 9	DC～8	0.3 ～ 25	3.1 ～ 8.72	2.4 ～ 10.7
CG (dB)	10.5 ± 1.5	9.5 ± 1.5	11 ± 1.5	3.75 ± 1.25	3.3 ± 1.5
IIP3 (dBm)	2	-7	---	5	6.9
P1dB (dBm)	-4	-17	-5	---	-2.8
LO Power (dBm)	-8	-2	-1	9	-5
Pdis (mW)	25	---	71	10.4	14.4
Supply voltae (V)	5	5	5	1.8	1.8
Die area (mm^2)	---	---	0.8X1	1.4X1.16	0.70X0.58

Table 3.2 Summary of the comparison

In this section, a 2.4 to 10.7 GHz wideband mixer for multi-band orthogonal frequency division multiplexing ultra-wideband (MB-OFDM UWB) applications is designed using a TSMC 0.18μm CMOS technology. The designed mixer uses a LC folded cascode structure and a feedforward compensated high-linearity differential transconductor. The LC folded cascode method is used to get enough voltage headroom to work with, and the modified feedforward compensated differential transconductor is adopted to achieve broadband impedance matching and lower the overall distortion. The measured results reveal that the proposed mixer achieves power conversion gain of 3.3 ± 1.5 dB, third-order input intercept point (IIP3) of 6.9 dBm, and input 1-dB compression point (P-1dB) of -2.8 dBm in the power consumption of 14.4mW from a 1.8V power supply. The chip area is 0.70 × 0.58 mm^2.

This wideband down-conversion mixer is accepted for publication on the IEEE International Symposium on Circuits and Systems (ISCAS) 2007.

3.2 The Design of Wideband Down-Conversion Mixer with Broadband Active Balun

In this section, a wideband mixer with broadband active balun is presented. The proposed mixer employs a LC folded cascode structure and a feedforward compensated differential transconductor. The broadband active balun is used in the RF and LO ports. The design and analysis of broadband active balun is described in this section. Finally, the simulated and measured results are discussed.

3.2.1 Broadband Active Balun Design

3.2.1.1 Broadband Active Balun Circuit Description

In this section, a broadband active balun is analyzed and designed. The schematic of the proposed broadband active balun is shown as Fig. 3.15. It is improved from common-gate cascaded with common-source. The output1 is from common-source (MN1) stage and output2 is from two PMOS common-gate cascode (MP1 & MP2). The PMOS is used to reduce power consumption instead of NMOS. The purpose of cascode two PMOS is to reduce phase difference.

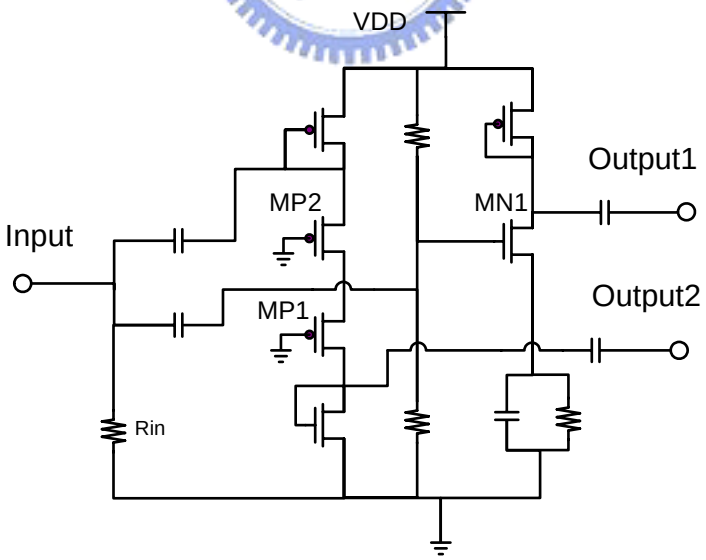


Fig. 3.15. Schematic of the proposed broadband active balun.

There are three kinds of matching circuits: LC matching, active matching and resistive matching. LC matching has lower noise, higher Q and filtering performance. LC matching takes more die area than the other two matching. Active and resistive

matching have wideband performance. Active matching needs extra dc current and resistive matching is lossy and noisy. Based on these considerations, a compromise is made. Rin is used as input matching in order to save the die area. The Input impedance matching is shown as Fig. 3.16.

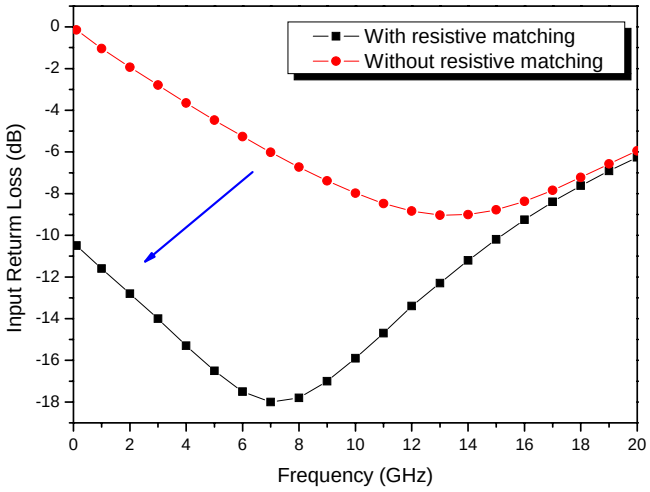


Fig. 3.16. Input impedance matching.

The simulated amplitude balance and phase difference of the proposed active balun combine with mixer core are shown in Fig. 3.17. ADS simulated data show that the bandwidth is 11 GHz. The gain difference is less than 2 dB (-0.7 ～ -1.9) and phase difference is less than 4 degrees (178 ～ 182) with a bandwidth from 2GHz to 13GHz while consuming 1.8mW.

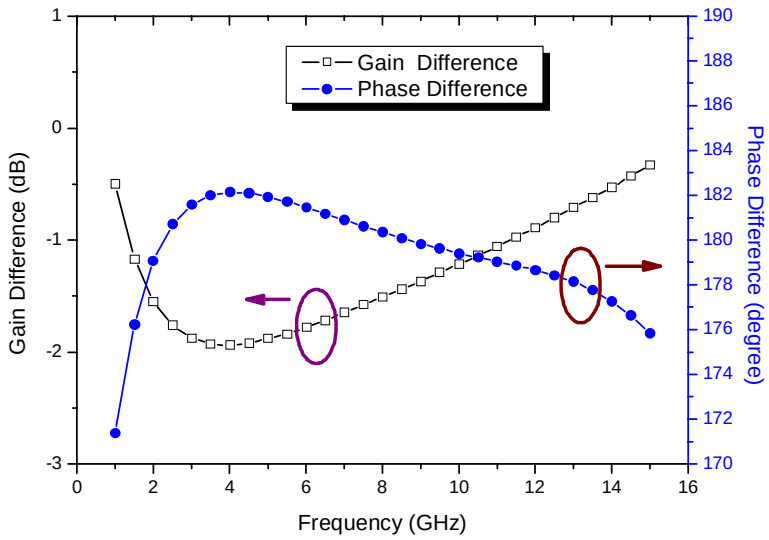


Fig. 3.17. Simulated amplitude balance and phase difference.

Comparison of recently reported CMOS active Baluns with this study is shown as Table 3.3. The three references are measured results. Ref. [14] is the best CMOS active Balun in recently published papers.

Ref.	[18]	[7]	[14]	This Work
Process	0.18-um CMOS	0.25-um CMOS	0.18-um CMOS	0.18-um CMOS
Architecture	Differential	Differential	Differential	CSCG
Frequency (GHz)	5.1 ～ 5.9	5.4 ～ 5.8	0 ～ 8	2 ～13
Gain difference (dB)	0.02	0.5	2	2
Phase difference (Degrees)	0.58	1	3	4
Power (mW)	9.17	---	1.44	1.8
Chip area (mm)	---	---	0.57X0.68	0.1X0.1

Table 3.3 Comparison of CMOS active baluns

3.2.1.2 Phase Difference Analysis

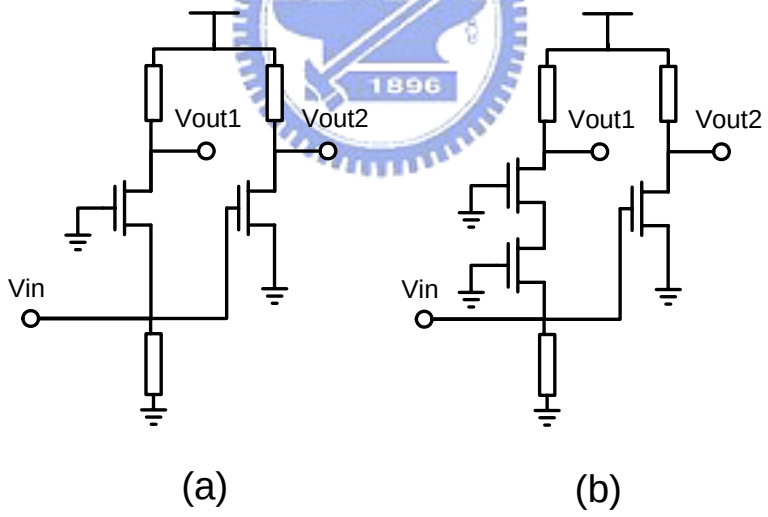


Fig. 3.18. Circuits of (a) the conventional CSCG Balun and (b) the Cascode CG & CS Balun.

Fig. 3.18(a) illustrates the conventional CSCG Balun. It's consists of common-gate and common-source. Fig. 3.18(b) illustrates the cascode CG & CS Balun. It's consists of common-gate cascode with common-gate and common-source. The phase difference of Fig. 3.18(a) and Fig. 3.18(b) are derived as below.

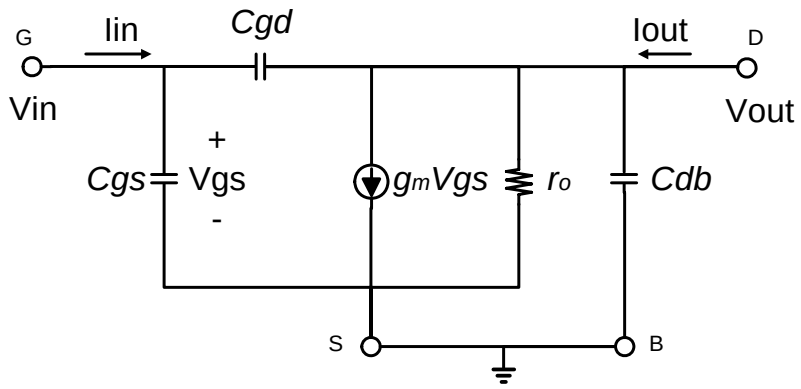


Fig. 3.19. Small-signal equivalent circuit model of common-source.

Fig. 3.19 illustrates the small-signal equivalent circuit model of common-source. Assuming that all ports are terminated in the characteristic impedance Z0.

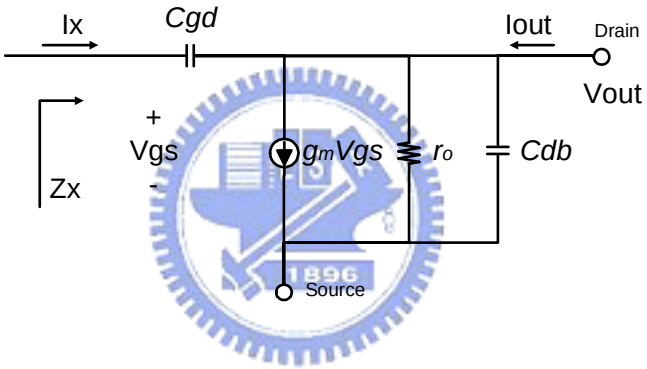


Fig. 3.20. Small-signal equivalent model neglecting Cgs.

To derive Zin, we consider Zx in Fig. 3.20 firstly. We have

$$\frac{I_x}{sC_{gd}} + (I_x - g_m V_x)(r_o \,||\, \frac{1}{sC_{db}}) = V_x \tag{3.18}$$

From (3.18)

$$Z_x = \frac{V_x}{I_x} = \frac{1 + r_o s(C_{db} + C_{gd})}{sC_{gd}(1 + g_m r_o + r_o sC_{db})} \tag{3.19}$$

Assume $\left| r_o s(C_{db} + C_{gd}) \right| \ll 1$ *and* $\left| r_o sC_{db} \right| \ll 1 + g_m r_o$, therefore

$$Z_x = \frac{1}{sC_{gd}(1 + g_m r_o)} \tag{3.20}$$

Then Zin is given by

$$Z_{in} = Z_x \| \frac{1}{sC_{gs}} = \frac{1}{s[C_{gd}(1+g_m r_o)+C_{gs}]} \tag{3.21}$$

Let us now calculate the relationship of Vin and Vout. We can sum the currents at the output node：

$$\frac{(V_{out}-V_x)}{\frac{1}{sC_{gd}}} + g_m V_x + \frac{V_{out}}{r_o \| Z_0 \| \frac{1}{sC_{db}}} = 0 \tag{3.22}$$

Obtaining

$$\frac{V_{out}}{V_{in}} = \frac{V_2}{V_1} = \frac{V_{out}}{V_x} = \frac{sC_{gd}-g_m}{sC_{gd}+sC_{db}+\frac{1}{r_o}+\frac{1}{Z_0}} \tag{3.23}$$

The S21 of common source can be written as

$$S_{21} = \left.\frac{V_2^-}{V_1^+}\right|_{V_2^+=0} = \frac{V_2}{V_1^+} = \frac{V_2}{V_1}\frac{}{1+S_{11}} \tag{3.24}$$

where

$$S_{11} = \left.\frac{V_1^-}{V_1^+}\right|_{V_2^+=0} = \frac{Z_{in}-Z_0}{Z_{in}+Z_0} \tag{3.25}$$

Then substituting (3.21), (3.23), and (3.25) into (3.24). The amplitude and phase of S21 can be derived as (3.26) and (3.34).

$$S_{21} = k(1+j\omega\theta) \tag{3.26}$$

where

$$k = \frac{2(D+\omega^2 BE)}{C(1+A)} \tag{3.27}$$

$$\theta = \frac{E-BD}{D+\omega^2 BE} \tag{3.28}$$

$$A = \omega^2 Z_0^2[(1+g_m r_o)C_{gd}+C_{gs}]^2 \tag{3.29}$$

$$B = Z_0[(1+g_m r_o)C_{gd}+C_{gs}] \tag{3.30}$$

$$C = (\frac{1}{r_o}+\frac{1}{Z_0})^2 + \omega^2(C_{gd}+C_{db})^2 \tag{3.31}$$

$$D = \omega^2 C_{gd}(C_{gd} + C_{db}) - g_m(\frac{1}{r_o} + \frac{1}{Z_0}) \tag{3.32}$$

$$E = C_{gd}(\frac{1}{r_o} + \frac{1}{Z_0}) + g_m(C_{gd} + C_{db}) \tag{3.33}$$

Thus,

$$\angle S_{21} = \tan^{-1}(\omega \frac{[C_{gd}(\frac{1}{r_o}+\frac{1}{Z_0}) + g_m(C_{gd}+C_{db})] - \{Z_0[(1+g_m r_o)C_{gd} + C_{gs}]\}\left[\omega^2 C_{gd}(C_{gd}+C_{db}) - g_m(\frac{1}{r_o}+\frac{1}{Z_0})\right]}{\left[\omega^2 C_{gd}(C_{gd}+C_{db}) - g_m(\frac{1}{r_o}+\frac{1}{Z_0})\right] + \omega^2\{Z_0[(1+g_m r_o)C_{gd}+C_{gs}]\}[C_{gd}(\frac{1}{r_o}+\frac{1}{Z_0}) + g_m(C_{gd}+C_{db})]}) \tag{3.34}$$

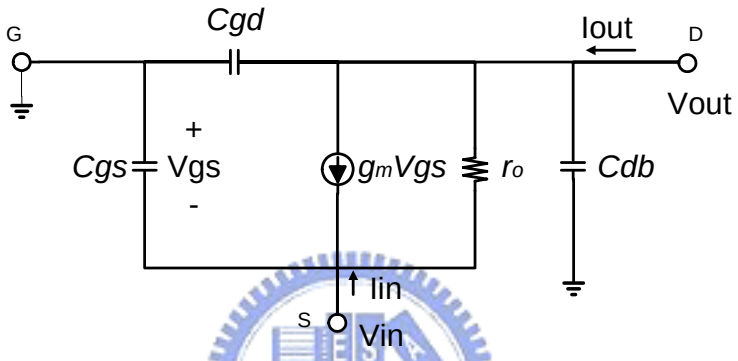


Fig. 3.21. Small-signal equivalent circuit model of common-gate.

Fig. 3.21 illustrates the small-signal equivalent circuit model of common-gate. To derive Zin, we calculate Zx which is seen into Cgd at G node. We have

$$Z_x = \frac{1}{g_m} + \frac{1}{sC_{gd}sC_{db} + g_m r_o}\frac{1}{g_m} \approx \frac{1}{g_m} \tag{3.35}$$

Then Zin is given by

$$Z_{in} = Z_x \parallel \frac{1}{sC_{gs}} = \frac{1}{g_m + sC_{gs}} \tag{3.36}$$

Let us now calculate the relationship of Vin and Vout. We can sum the currents at the output node：

$$\frac{-V_{out}}{Z_0 \parallel \frac{1}{sC_{gd}} \parallel \frac{1}{sC_{db}}} - g_m(-V_1) = \frac{V_{out} - V_1}{r_o} \tag{3.37}$$

Thus

$$\frac{V_2}{V_1}=\frac{V_{out}}{V_1}=\frac{1+g_m r_o}{1+r_o(\frac{1}{Z_0}+sC_{gd}+sC_{db})} \tag{3.38}$$

The S21 of common gate can be written as

$$S_{21}=(\frac{2}{1+\frac{Z_o}{Z_{in}}})(\frac{V_2}{V_1})=(\frac{2}{1+(g_m+sC_{gs})Z_0})(\frac{1+g_m r_o}{1+r_o(\frac{1}{Z_0}+sC_{gd}+sC_{db})}) \tag{3.39}$$

The amplitude and phase of S21 can be derived as (3.40) and (3.49).

$$S_{21}=k(1+j\omega\theta) \tag{3.40}$$

$$k=\frac{2(BE-\omega^2 CF)}{AD} \tag{3.41}$$

$$\theta=\frac{BF+CE}{\omega^2 CF-BE} \tag{3.42}$$

$$A=(1+\frac{r_o}{Z_0})^2+\omega^2 r_o^2(C_{gd}+C_{db})^2 \tag{3.43}$$

$$B=(1+\frac{r_o}{Z_0})-r_o s(C_{gd}+C_{db})+g_m r_o(1+\frac{r_o}{Z_0}) \tag{3.44}$$

$$C=g_m r_o^2(C_{gd}+C_{db}) \tag{3.45}$$

$$D=(1+g_m Z_0)^2+\omega^2 C_{gs}^2 Z_0^2 \tag{3.46}$$

$$E=1+g_m Z_0 \tag{3.47}$$

$$F=C_{gs}Z_0 \tag{3.48}$$

Thus,

$$\angle S_{21}=\tan^{-1}(\omega\frac{\left[(1+\frac{r_o}{Z_0})-r_o s(C_{gd}+C_{db})+g_m r_o(1+\frac{r_o}{Z_0})\right](C_{gs}Z_0)+\left[g_m r_o^2(C_{gd}+C_{db})\right](1+g_m Z_0)}{\omega^2\left[g_m r_o^2(C_{gd}+C_{db})\right](C_{gs}Z_0)-\left[(1+\frac{r_o}{Z_0})-r_o s(C_{gd}+C_{db})+g_m r_o(1+\frac{r_o}{Z_0})\right](1+g_m Z_0)}) \tag{3.49}$$

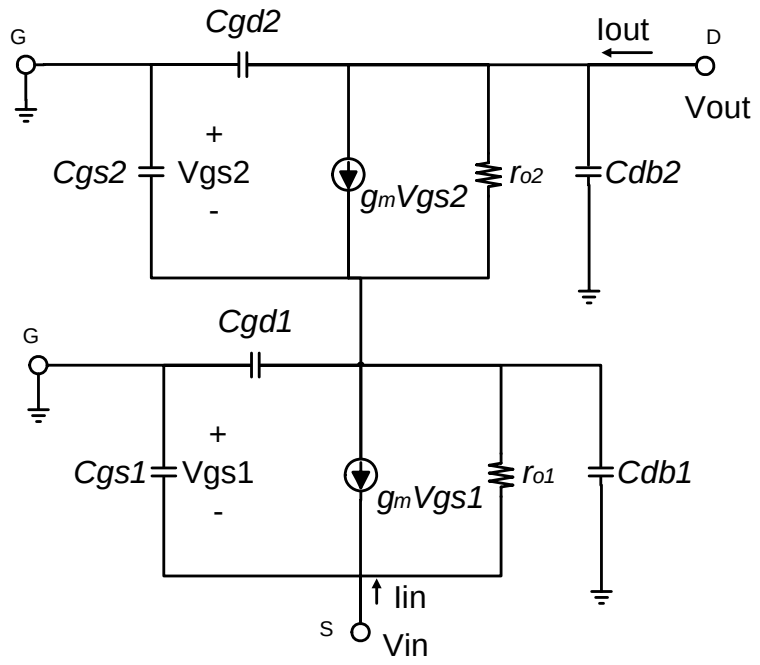


Fig. 3.22. Small-signal equivalent circuit model of cascode common-gate.

Fig. 3.22 illustrates the small-signal equivalent circuit model of cascade common-gate. We calculate Zin which is seen into S node at bottom. We have

$$Z_{in} \approx \frac{1}{g_m + sC_{gs}} \tag{3.50}$$

Let us now calculate the relationship of Vin and Vout. Let Vx denotes the voltage in the center of these two common-gate. We have

$$V_x = -\left(\frac{V_{out}}{Z_0 \parallel \frac{1}{sC_{gd2}} \parallel \frac{1}{sC_{db2}}} + I_{in}\right)\left(\frac{1}{sC_{gd1}} \parallel \frac{1}{sC_{db1}}\right) \tag{3.51}$$

Then Id2 is written as

$$I_{D2} = g_{m2}V_{gs2} = g_{m2}(-V_x) = g_{m2}\left(\frac{V_{out}}{Z_0 \parallel \frac{1}{sC_{gd2}} \parallel \frac{1}{sC_{db2}}} + I_{in}\right)\left(\frac{1}{sC_{gd1}} \parallel \frac{1}{sC_{db1}}\right) \tag{3.52}$$

Then

$$V_{out} = r_{o2}\left(\frac{-V_{out}}{Z_0 \parallel \frac{1}{sC_{gd2}} \parallel \frac{1}{sC_{db2}}} - I_{D2}\right) + \left(\frac{-V_{out}}{Z_0 \parallel \frac{1}{sC_{gd2}} \parallel \frac{1}{sC_{db2}}} - I_{in}\right)\left(\frac{1}{sC_{gd1}} \parallel \frac{1}{sC_{db1}}\right) \tag{3.53}$$

We have

$$\frac{V_{out}}{I_{in}} = -\frac{g_{m2}r_{o2}+1}{sC_{gd1}+sC_{db1}} \frac{1}{1+\left(g_{m2}r_{o2}+1\right)\dfrac{\dfrac{1}{Z_0}+sC_{gd2}+sC_{db2}}{sC_{gd1}+sC_{db1}} + r_{o2}\left(\dfrac{1}{Z_0}+sC_{gd2}+sC_{db2}\right)} \tag{3.54}$$

For $g_{m2}r_{o2} \gg 1$ *and* $g_{m2}r_{o2}\dfrac{\dfrac{1}{Z_0}+sC_{gd2}+sC_{db2}}{sC_{gd1}+sC_{db1}} \gg 1$, hence

$$\frac{V_{out}}{I_{in}} \approx -\frac{g_{m2}}{sC_{gd1}+sC_{db1}} \frac{1}{\dfrac{\dfrac{1}{Z_0}+sC_{gd2}+sC_{db2}}{sC_{gd1}+sC_{db1}} g_{m2} + \left(\dfrac{1}{Z_0}+sC_{gd2}+sC_{db2}\right)} \tag{3.55}$$

Therefore, we know the relationship of Vin and Vout as the below equation.

$$\frac{V_2}{V_1} = \frac{V_{out}}{V_{in}} = \frac{I_{in}}{V_{in}}\frac{V_{out}}{I_{in}} = g_{m1}\frac{V_{out}}{I_{in}} \tag{3.56}$$

The S21 is $S_{21} = (\dfrac{2}{1+\dfrac{Z_o}{Z_{in}}})(\dfrac{V_2}{V_1})$. Substituting Zin and $\dfrac{V_2}{V_1}$ into it. Then S21 is derived.

The amplitude and phase of S21 can be derived as (3.57) and (3.65).

$$S_{21} = k(1+j\omega\theta) \tag{3.57}$$

$$k = \frac{2(AD-\omega^2 BE)}{C(A^2+\omega^2 B^2)} \tag{3.58}$$

$$\theta = \frac{AE+BD}{\omega^2 BE - AD} \tag{3.59}$$

$$A = 1+g_m Z_0 \tag{3.60}$$

$$B = C_{gs}Z_0 \tag{3.61}$$

$$C = g_m{}^2 + (C_{gd1}+C_{db1})^2 \tag{3.62}$$

$$D = -g_{m1}g_{m2}\omega^2(C_{gd1}+C_{db1})^2 \tag{3.63}$$

$$E = g_{m1}g_{m2}{}^2(C_{gd1}+C_{db1}) \tag{3.64}$$

Thus,

$$\angle S_{21} = \tan^{-1}(\omega \frac{(1+g_m Z_0)\left[g_{m1}{g_{m2}}^2(C_{gd1}+C_{db1})\right]+(C_{gs}Z_0)\left[-g_{m1}g_{m2}\omega^2(C_{gd1}+C_{db1})^2\right]}{\omega^2(C_{gs}Z_0)\left[g_{m1}{g_{m2}}^2(C_{gd1}+C_{db1})\right]-(1+g_m Z_0)\left[-g_{m1}g_{m2}\omega^2(C_{gd1}+C_{db1})^2\right]}) \quad (3.65)$$

Therefore, the phase difference of Fig. 4.4(a) is given by (3.34) substrate (3.49) and the phase difference of Fig. 4.4(b) is given by (3.34) subtract (3.65). The phase mismatch is give by

$$Phase\_a = \left| \pi - [\angle S_{21}|_{CS} - \angle S_{21}|_{CG}] \right| \quad (3.66)$$

$$Phase\_b = \left| \pi - [\angle S_{21}|_{CS} - \angle S_{21}|_{CGCG}] \right| \quad (3.67)$$

From equation (3.66) and (3.67), we conducted simulation tests on TSMC 0.18μm CMOS process. Assuming L=0.18μm, W=2μm, Finger=15, and Id=1mA, we can obtain the simulated phase differences of the cascode common gate and the conventional active balun as shown in Fig. 3.23. Phase mismatch is means the degree away from 180. The result demonstrated the cascode common gate can improve phase performance.

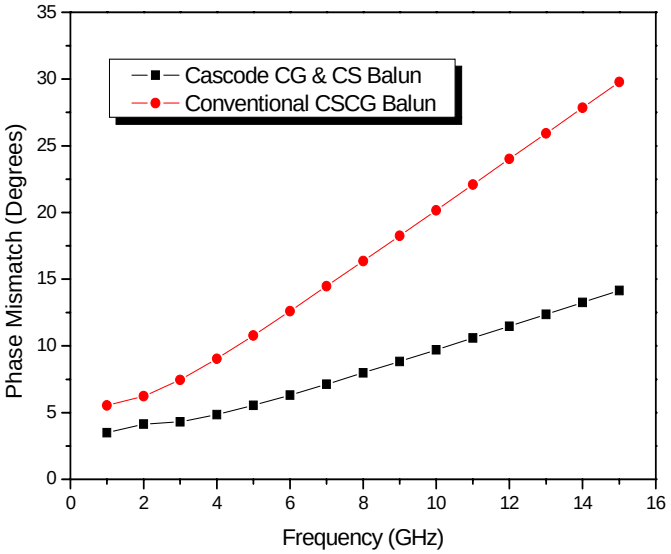


Fig. 3.23. Simulated phase differences.

3.2.2 Design of the Wideband Mixer with Broadband Active Balun

3.2.2.1 Mixer Core

Fig. 3.24. shows the mixer core, which is composed of an LC folded cascode mixer and a feedforward compensated differential transconductor. Their design and analysis is described in section 3.1.

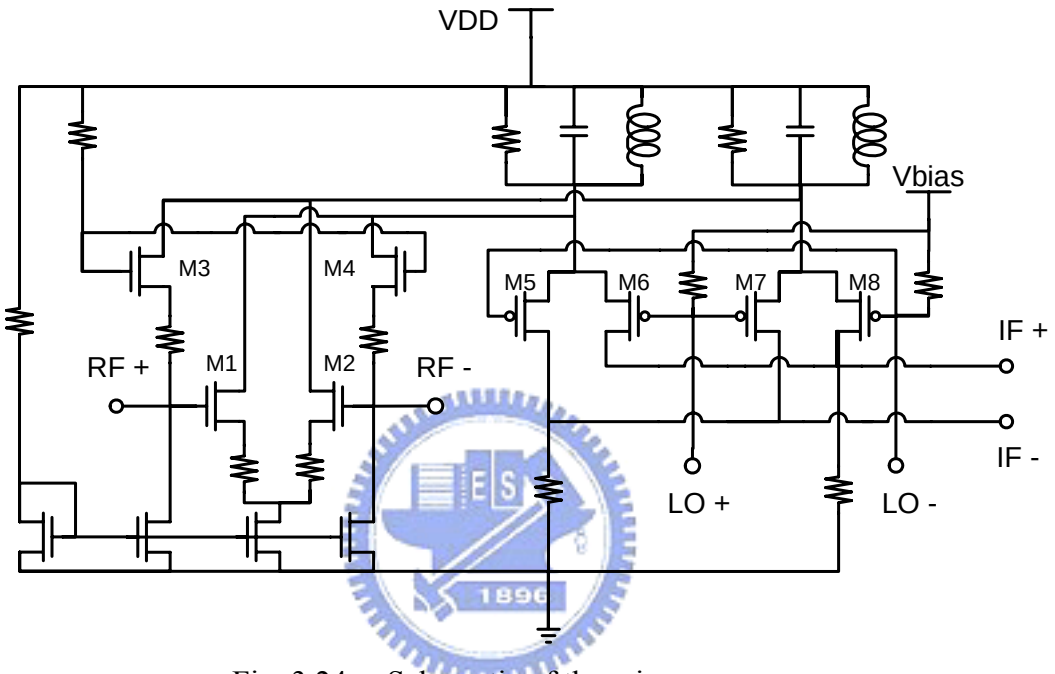


Fig. 3.24. Schematic of the mixer core.

3.2.2.2 Proposed Wideband Mixer Topology

Fig. 3.25 illustrates the block diagram of the proposed wideband mixer. It includes mixer core, active baluns, and output buffer. Mixer core is the LC folded cascode mixer with modified differential transconductor. Active baluns are modified CSCG balun for generating balanced RF and LO signals to double balanced Gilbert mixer. Output buffer is differential amplifier and common-source amplifier for testing and matching purposes. All ports are single input and single output. This circuit can directly combine with frond-end and back-end circuits. The circuit schematic of the proposed wideband mixer is shown in Fig. 3.26.

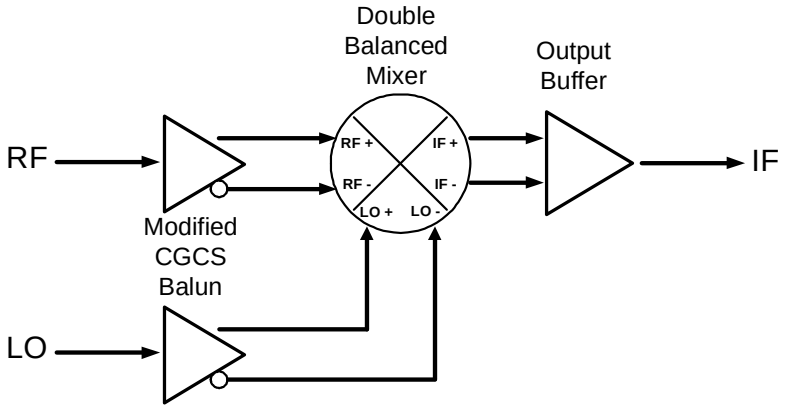


Fig. 3.25. Block diagram of the proposed wideband mixer.

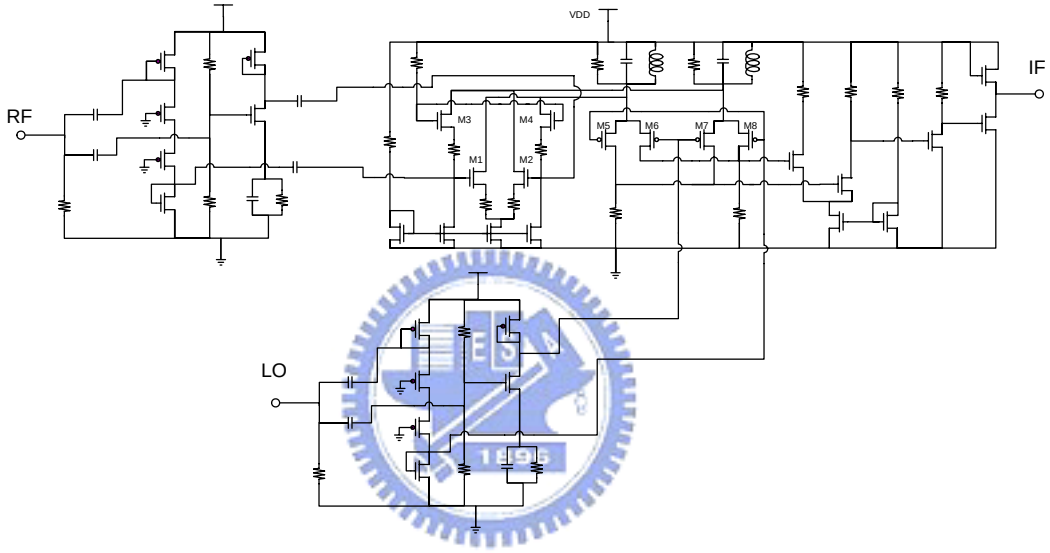


Fig. 3.26. Complete Schematic of the proposed wideband mixer.

3.2.3 Simulation and Measurement Results

In this section, we show the measurement setups and results of the proposed mixer. The measurements were performed with the chip directly mounted on a 26×26 mm^2 and thickness of 20 mil RO4003 microwave substrate with SMA connectors. Fig. 3.27 shows the test board with die mounted on RO4003 printed circuit board (PCB). Fig. 3.28 shows the PCB layout. The chip layout and microphotograph are shown in Fig. 3.29 and Fig. 3.30. The die size is 0.85×0.57 mm2 including pads. Fig. 3.31 shows the measurement setup of power conversion gain. The DC power supplier provide 1.8V dc source to mixer in measurement. The connectors and lines both result in loss in measurement.

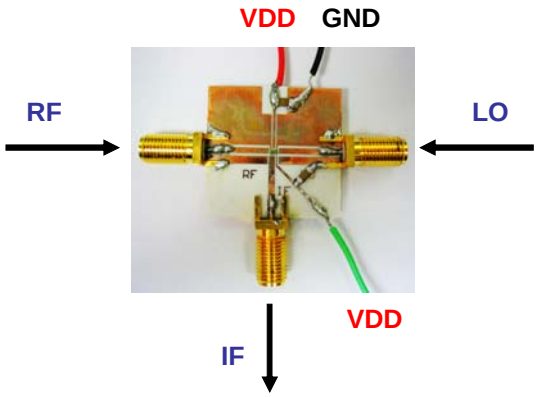


Fig. 3.27. Die bonded to the PCB.

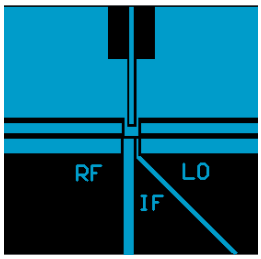


Fig. 3.28. PCB layout of the proposed mixer.

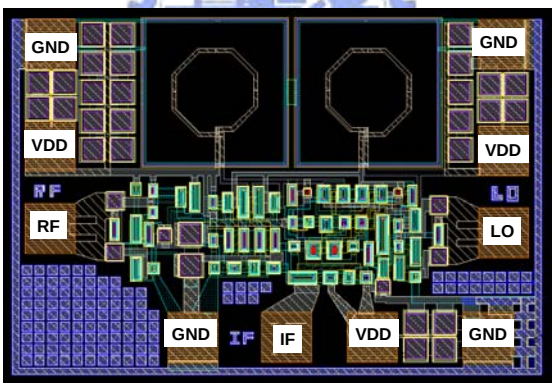


Fig. 3.29. The chip layout of the proposed mixer.

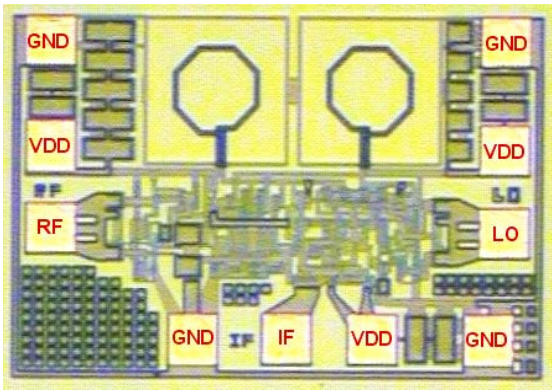


Fig. 3.30. Microphotograph of the proposed mixer.

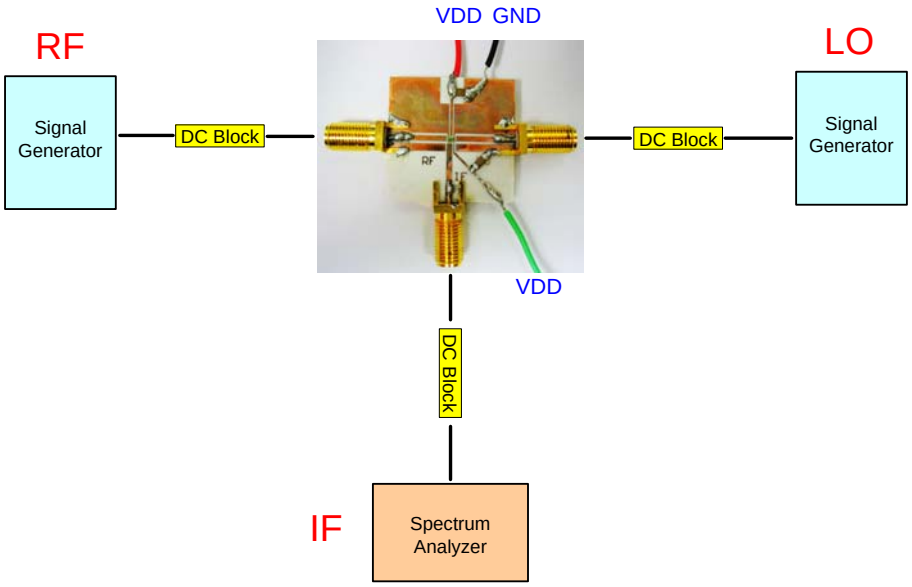


Fig. 3.31. Measurement setup of power conversion gain.

The mixer is designed using TSMC 0.18μm CMOS technology. All measurements were done at 1.8 V supply voltage and the power consumption is 25.7 mW including the output buffer. The power consumption of output buffer is 14.5 mW. Fig. 3.32 illustrates the conversion gain versus the RF frequency with both RF and LO ports swept in frequency from 2 to 12 GHz, a fixed IF frequency of 50 MHz, RF power of -30 dBm, and LO power of -5 dBm. The flat conversion gain is 6.9 ± 1.5dB with a bandwidth of 2 to 11.5 GHz. Simulation1 means the bond wire equivalent model is using 20mil. But it's not 20mil actually. Simulation2 is the practical bond wire length approximate calculated from the chip. The measured RF return loss is better than 10 dB as shown in Fig. 3.33. The measured LO and IF return loss are also better than 10dB as shown in Fig. 3.34 and Fig. 3.35. The measured RF-to-IF, LO-to-IF and RF-to-LO isolation shown in Fig. 3.36. are better than 20 dB. Fig. 3.37 and Fig. 3.38 are P1dB and IIP3 when RF frequency is 8GHz. Fig. 3.39 and and Fig. 3.40 show the linearity of the mixer as a function of frequency. The measured IIP3 is 1.8 ~ 6.5 dBm and P1dB is -3.5 ~ -8.5 dBm in the bandwidth of 2 to 11.5 GHz. Table 3.4 shows the performance summary of simulated and measured results.

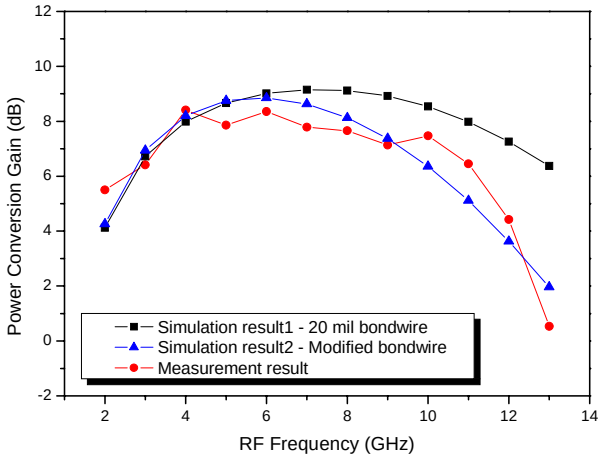


Fig. 3.32. Simulated and measured power conversion gain versus RF frequency with the IF frequency is 50MHz, RF power is -30dBm, and LO power is -5 dBm.

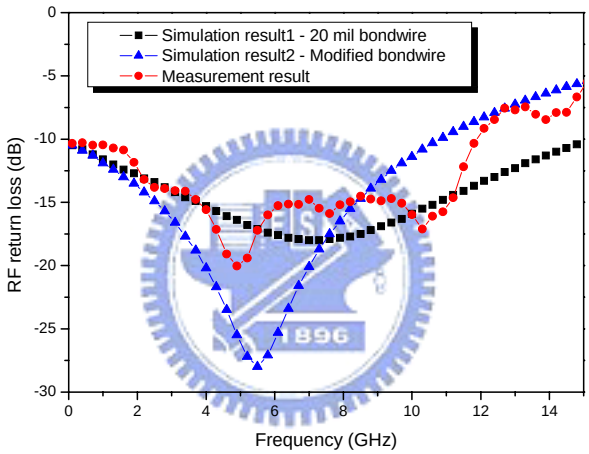


Fig. 3.33. Simulated and measured RF return loss versus RF frequency.

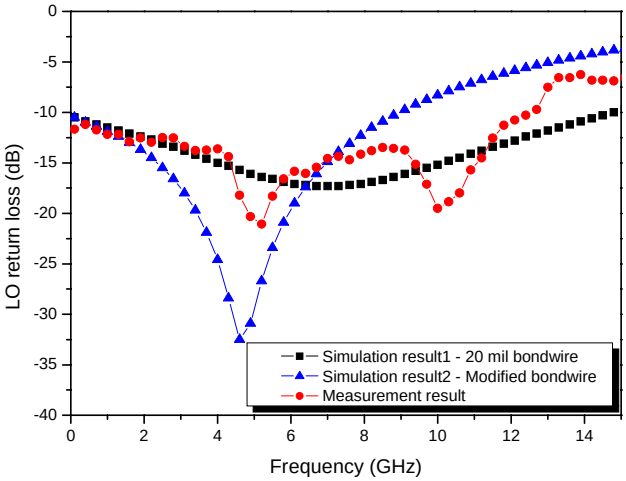


Fig. 3.34. Simulated and measured LO return loss versus LO frequency.

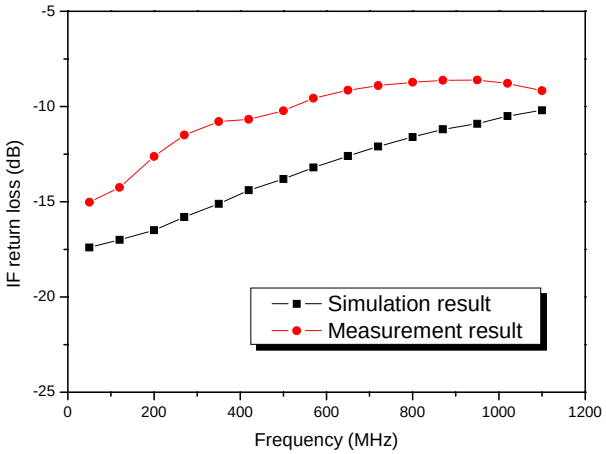


Fig. 3.35. Simulated and measured IF return loss versus IF frequency.

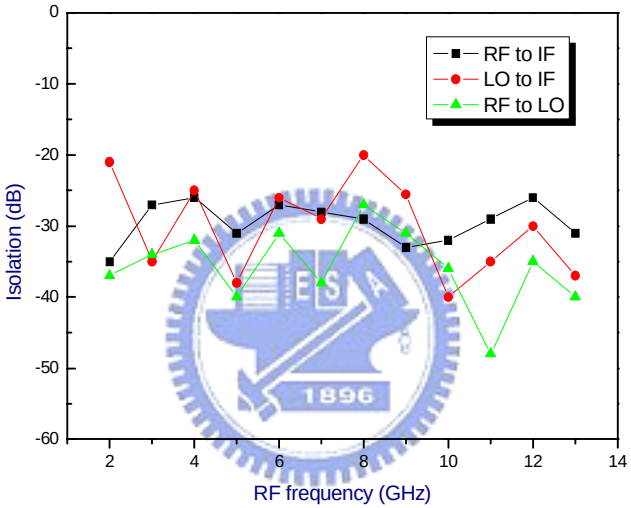


Fig. 3.36. Measured Isolation versus RF frequency.

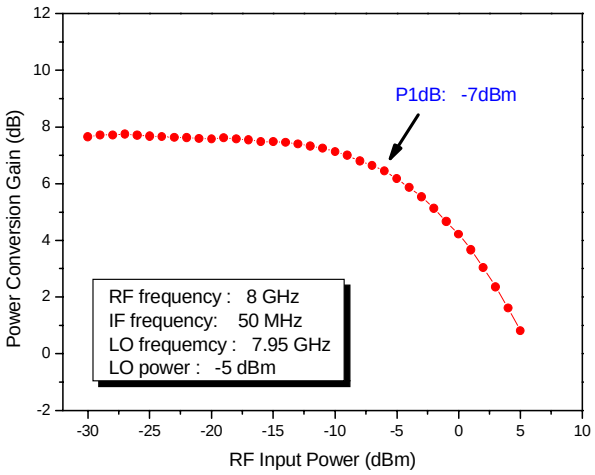


Fig. 3.37. Measured Power Conversion Gain versus RF input power, RF: 8GHz, LO: 7.95GHz.

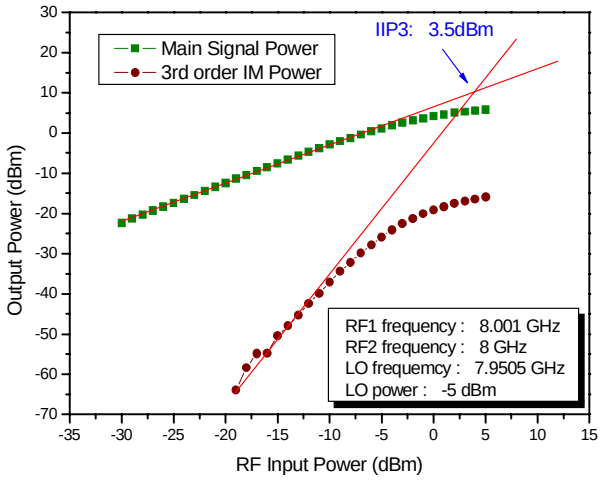


Fig. 3.38. Measured IIP3 curves, gain:+7.6dB, RF: 8 and 8.001 GHz, LO: 7.9505 GHz -5dBm. The input referred IP3 is +3.5dBm.

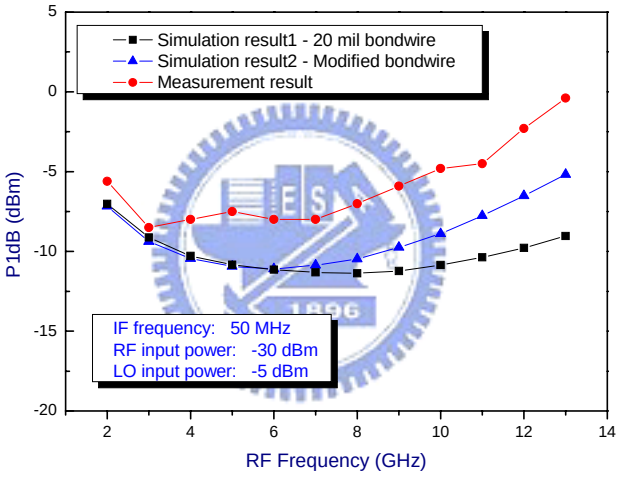


Fig. 3.39. Simulated and measured P1dB versus RF frequency.

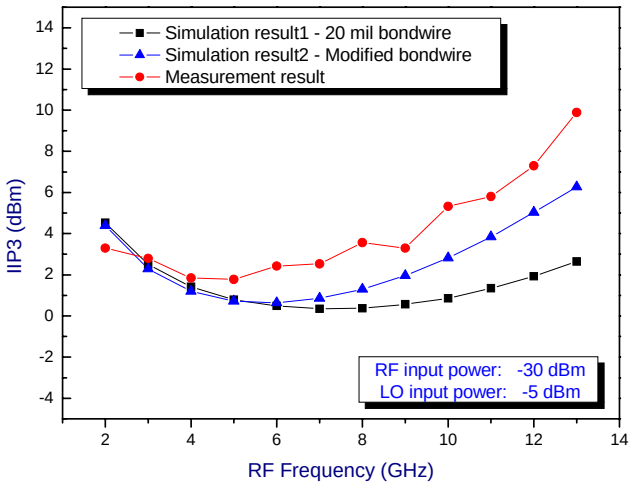


Fig. 3.40. Simulated and measured IIP3 versus RF frequency.

Parameters	Simulation result	Measurement result
Process	0.18um CMOS	
Frequency (GHz)	2.6 ～ 13.4	2 ～ 11.5
IF Frequency (MHz)	50	
Supply voltage (V)	1.8	
Power conversion gain (dB)	7.6 ± 1.5	6.9 ± 1.5
RF Input Return Loss (dB)	< -10	< -10
Input P1dB (dBm)	-11.3 ～ -8.4	-8.5 ～ -3.5
IIP3 (dBm)	-1.6 ～ 1.2	1.8 ～ 6.5
LO power (dBm)	-5	
Die area (mm^2)	0.85X0.57	
Power Consumption (mW)	Mixer core：7.1 Active Balun：3.6 Buffer：11 Total：21.7	Mixer & Balun：11.2 Buffer：14.5 Total：25.7

Table 3.4 Summary of simulation and measurement results

3.2.4 Comparison and Summary

The comparison of the proposed mixer against recently reported wideband mixer is shown in Table 3.5, it indicates that the proposed mixer provides better linearity, more compact chip size, and acceptable conversion gain and power consumption. In Ref. [32], the power consumption of mixer core is 71mW and the RF input return loss is better than 10dB for frequency from 10GHz to 21GHz.

Ref.	[30]	[31]	[32]	[33]	this work
Technology	1.4um GaInP/ GaAs	1.4um GaInP/ GaAs	0.18um CMOS	0.18um CMOS	0.18um CMOS
IF frequency (MHz)	150	350	10	528	50
Frequency (GHz)	DC ～ 9	DC～8	0.3 ～ 25	3.1 ～ 8.72	2 ～ 11.5
CG (dB)	10.5 ± 1.5	9.5 ± 1.5	11 ± 1.5	3.75 ± 1.25	6.9 ± 1.5
IIP3 (dBm)	2	-7	---	5	6.5
P1dB (dBm)	-4	-17	-5	---	-3.5
LO Power (dBm)	-8	-2	-1	9	-5
Pdis (mW)	25	---	71	10.4	25.7
Supply voltae (V)	5	5	5	1.8	1.8
Die area (mm^2)	---	---	0.8X1	1.4X1.16	0.85X0.57

Table 3.5 Summary of the comparison

In this section, a 2 to 11.5 GHz wideband mixer using LC folded cascode mixer topology, modified feedforward compensated differential transconductor, and broadband active balun in TSMC 0.18μm CMOS technology is presented. The LC folded cascode method is used to get enough voltage headroom to work with, and the modified feedforward compensated differential transconductor is adopted to achieve broadband impedance matching and lower the overall distortion. The adoption of broadband active balun in the designed wideband mixer allows providing balance signals for mixer core from single input. The measured results reveal that the proposed mixer achieves power conversion gain of 6.9± 1.5 dB, third-order input intercept point of 6.5 dBm, and input 1-dB compression point of -3.5 dBm in the power consumption of 25.7mW from a 1.8V power supply. The chip area is 0.85 × 0.57 mm^2. The designed mixer is suitable in the receiver front end of ultra-wideband system.

3.3 The Design of Single-Sideband Mixer for UWB Synthesizer

In this section, a single-sideband (SSB) mixer for UWB synthesizer is designed. It is important to devise a SSB mixer to generate multi-band carrier signals for frequency translation with electronic band selection capability. The SSB mixer can provide either upper or lower sideband output through an electronic control.

3.3.1 Principle of SSB Mixer

Fig. 3.41 shows the block diagram of frequency summation, which consists of four mixers and two output combiner. Fig. 3.42 shows the block diagram of difference, which consists of four mixers and two output combiner. In the ideal case, the SSB mixer only generates either upper (w1+w2) or lower (w1-w2) sideband component. In practice, both sidebands are present due to non-quadrature phase or amplitude imbalance.

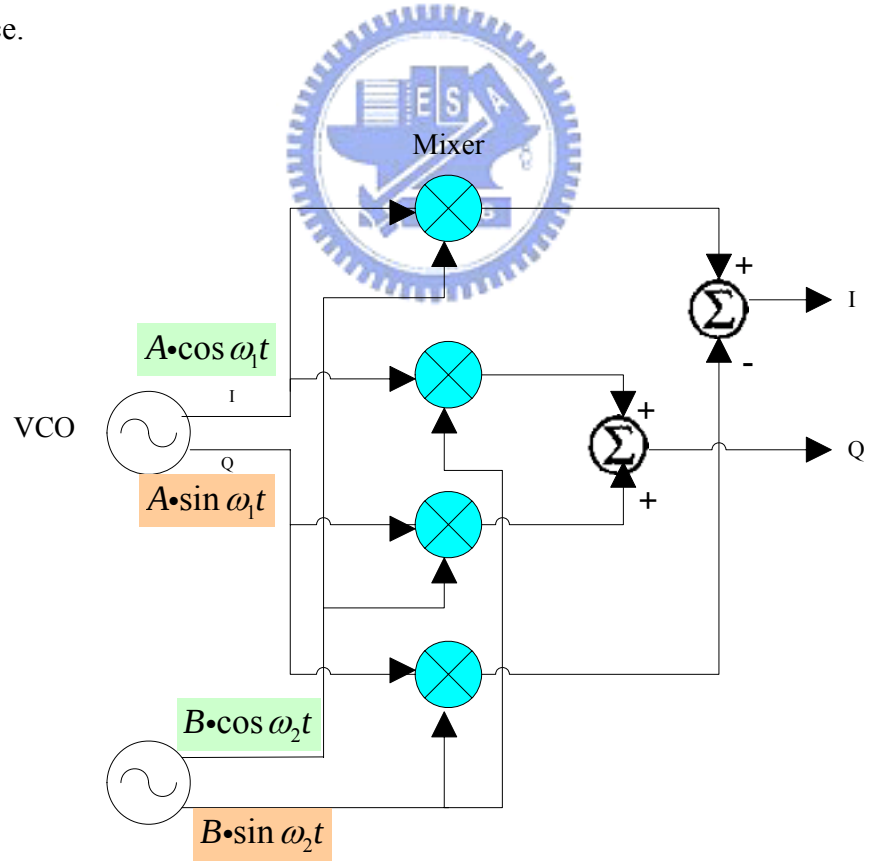


Fig. 3.41. Principle of SSB mixer: frequency summation.

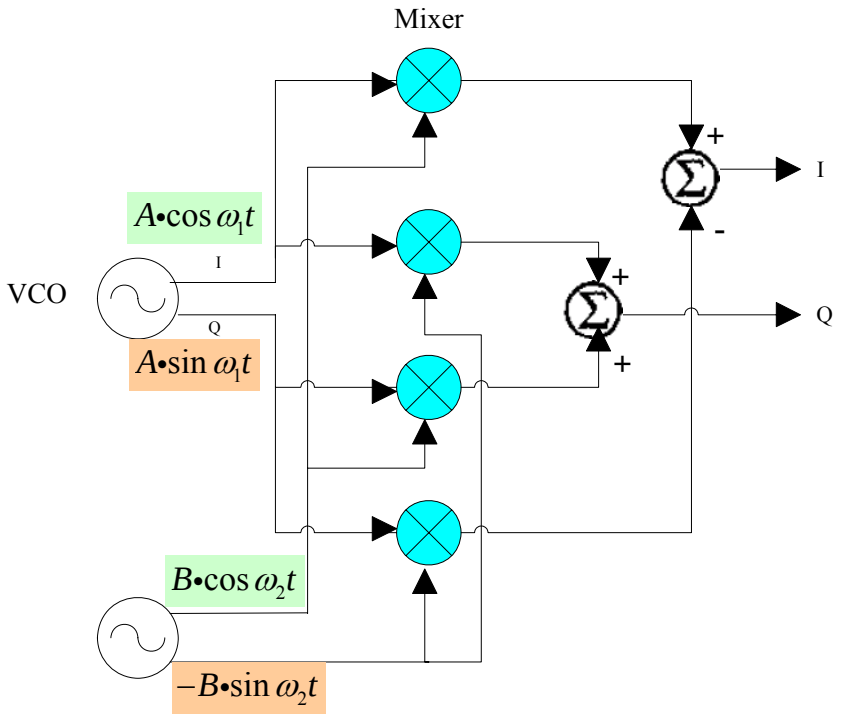


Fig. 3.42. Principle of SSB mixer: frequency difference.

The I/Q signals of Fig. 3.41 can derived as equation (3.68) and (3.69). We can see the frequency summation results from these two equations. The I/Q signals of Fig. 3.42 can derived as equation (3.70) and (3.71). We can see the frequency difference results from these two equations.

$$I: \quad (A\cos\omega_1 t)\cdot(B\cos\omega_2 t)-(A\sin\omega_1 t)\cdot(B\sin\omega_2 t)=AB\cos(\omega_1 t+\omega_2 t) \quad (3.68)$$

$$Q: \quad (A\cos\omega_1 t)\cdot(B\sin\omega_2 t)+(A\sin\omega_1 t)\cdot(B\cos\omega_2 t)=AB\sin(\omega_1 t+\omega_2 t) \quad (3.69)$$

$$I: \quad (A\cos\omega_1 t)\cdot(B\cos\omega_2 t)-(A\sin\omega_1 t)\cdot(-B\sin\omega_2 t)=AB\cos(\omega_1 t-\omega_2 t) \quad (3.70)$$

$$Q: \quad (A\cos\omega_1 t)\cdot(-B\sin\omega_2 t)+(A\sin\omega_1 t)\cdot(B\cos\omega_2 t)=AB\sin(\omega_1 t-\omega_2 t) \quad (3.71)$$

If we consider the SSB principle from frequency domain, Fig. 3.43 shows the lower side-band suppression. Using I/Q mixers to remove lower side-band signal as shown in Fig. 3.44. Fig. 3.45 shows the upper side-band suppression and Fig. 3.46 shows the remove of upper side-band signal. If summation or difference combining is performed at the SSB mixer output, it can be shown that the lower band or upper band is produced.

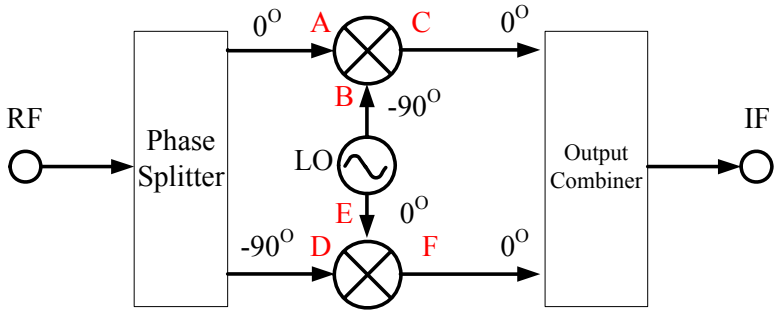


Fig. 3.43. Lower side-band suppression.

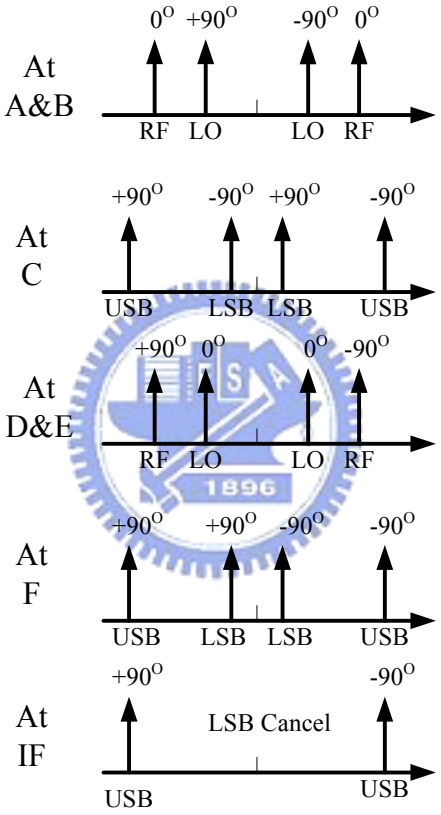


Fig. 3.44. LSB remove.

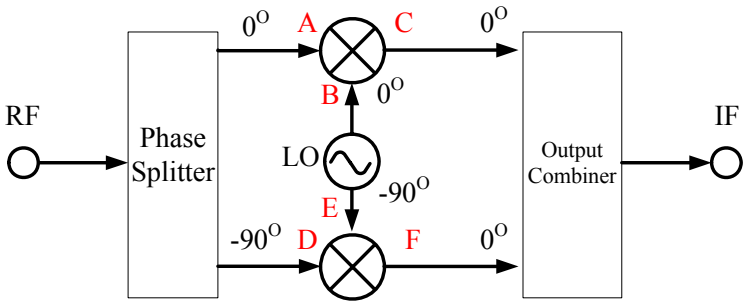


Fig. 3.45. Upper side-band suppression.

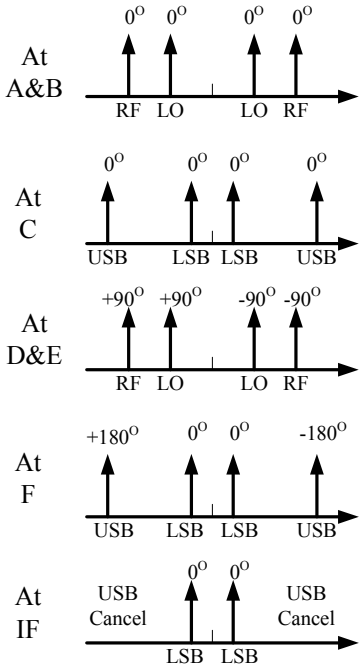


Fig. 3.46. USB remove.

3.3.2 SSB Mixer Circuit Design

3.3.2.1 UWB SSB Mixer Architecture

The block diagram of the UWB SSB mixer implementation is shown in Fig. 3.47, which consists of four mixers, two baluns, negative gain block, and two output combiner. This architecture finally achieve I+/I-/Q+/Q- signals of UWB 14 bands as shown in Table 3.6. Totally power consumption is 10 mW.

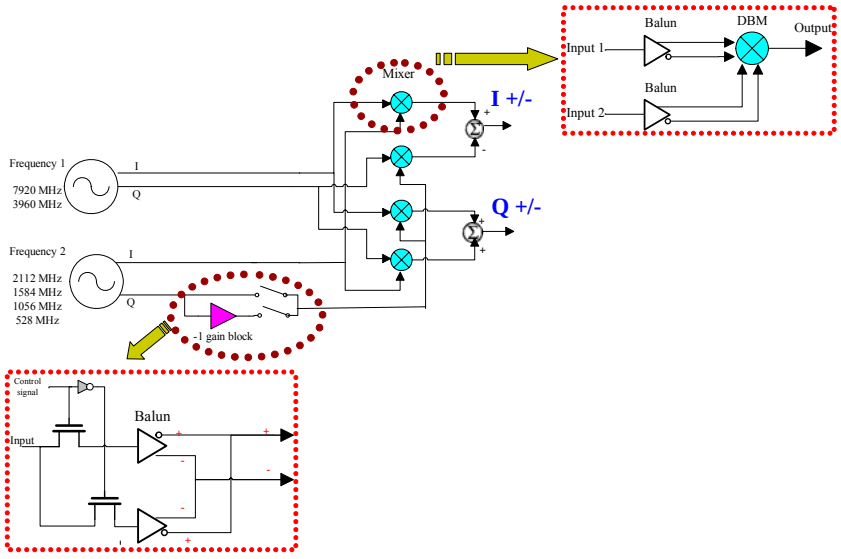


Fig. 3.47. UWB SSB mixer architecture.

Group	Band	Frequency (MHz)	IN2 & IN1 (MHz)
A	1	3432	3960-528
A	2	3960	3960+DC
A	3	4488	3960+528
B	4	5016	3960+1056
B	5	5544	3960+1584
B	6	5808	7920-2112
C	7	6336	7920-1584
C	8	6804	7920-1056
C	9	7392	7920-528
C	10	7920	7920+DC
D	11	8448	7920+528
D	12	8976	7920+1056
D	13	9504	7920+1584
D	14	10032	7920+2112

Table 3.6 Allocation of UWB 14 bands.

In Fig. 3.47, the structure of DBM is shown as Fig. 3.48 and its simulation summary is as Table 3.7. The structure of balun is shown as Fig. 3.49. The simulation results of phase difference and amplitude difference are shown as Fig. 3.50, Fig. 3.51, Fig. 3.52, and Fig. 3.53. Simulation summary of CGCS balun is as Table 3.8.

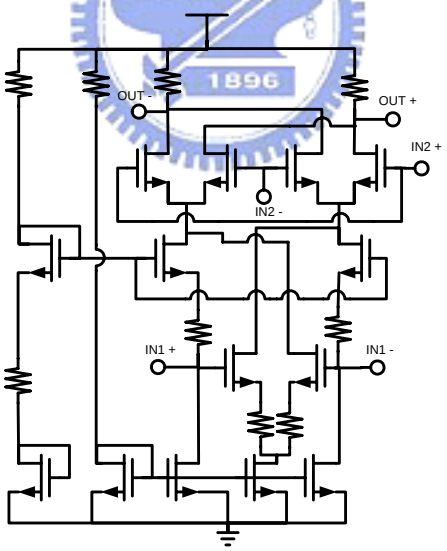


Fig. 3.48. Schematic of double balanced mixer.

Vin1 & Vin2 power (dBm)	-5						
Vin1 & Vin2 Frequency (MHz)	2112/ 7920	1584/ 7920	1056/ 7920	528/ 7920	1584/ 3960	1056/ 3960	528/ 3960
Power conversion gain (dB)	1.867	2.037	2.267	2.512	3.219	3.629	3.965
P 1dB (dBm)	-7.2	-7.3	-7.1	-6.9	-7	-6.8	-6.8
IIP3 (dBm)	0.83	0.91	1.263	1.602	0.727	1.082	1.461
Power consumption (mW)	1.12						

Table 3.7 Simulation summary of DBM

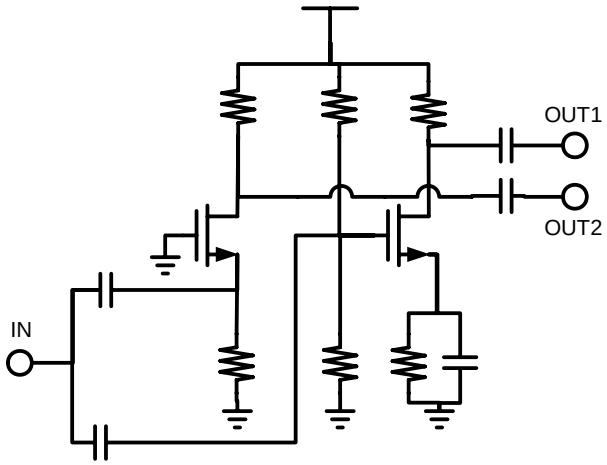


Fig. 3.49. Schematic of CGCS Balun.

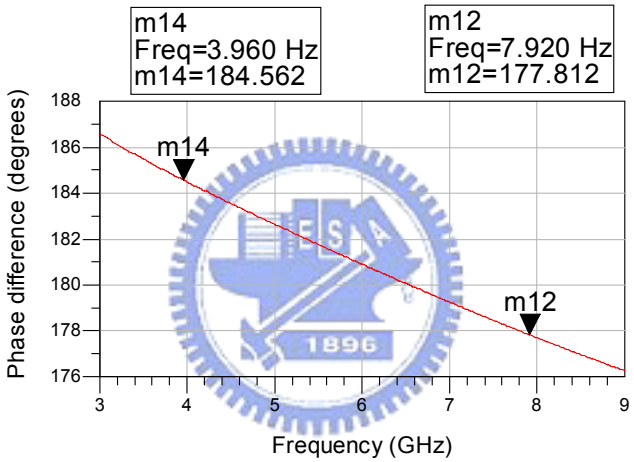


Fig. 3.50. Phase difference of 3.96 GHz and 7.92 GHz.

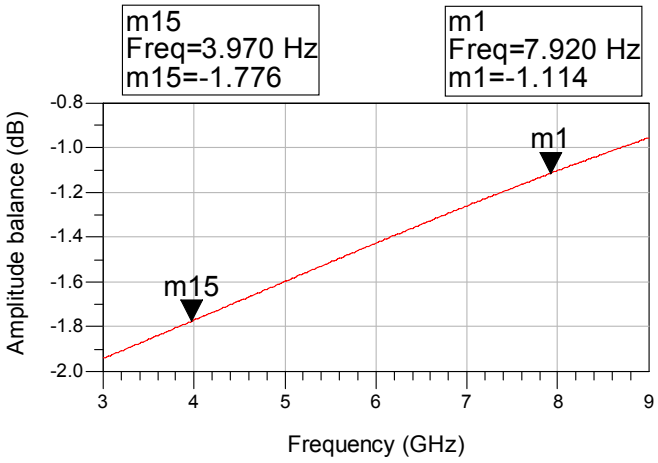


Fig. 3.51. Amplitude difference of 3.96 GHz and 7.92 GHz.

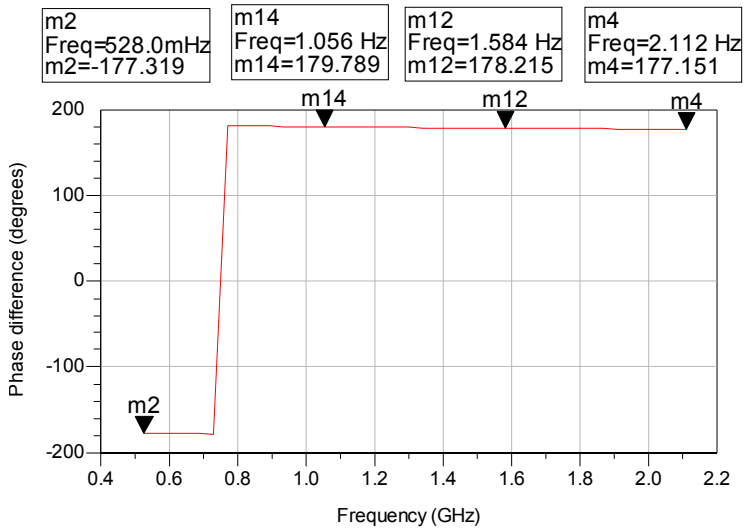


Fig. 3.52. Phase difference of 528MHz, 1.056GHz, 1.584GHz, and 2.112GHz.

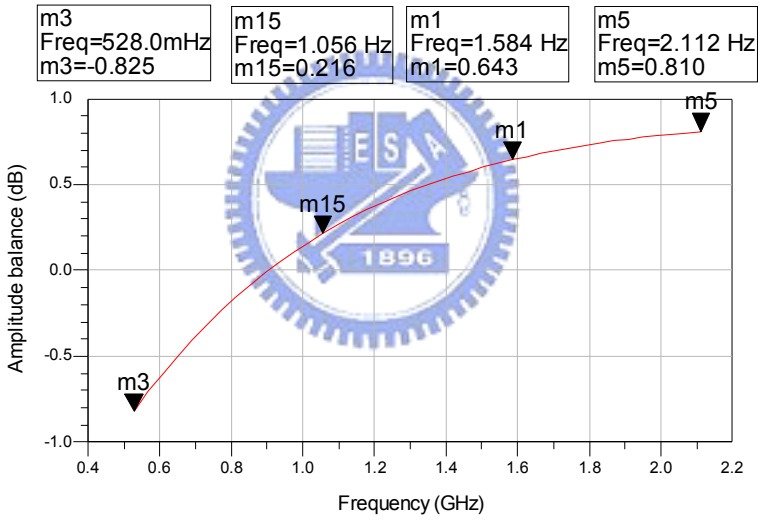


Fig. 3.53. Amplitude difference of 528MHz, 1.056GHz, 1.584GHz, and 2.112GHz

Parameters \ Frequency	528MHz	1056MHz	1584MHz	2112MHz	3960MHz	7920MHz
Phase difference (degree)	177.319	179.789	178.215	177.151	184.562	177.812
Amplitude difference (dB)	0.825	0.216	0.643	0.81	1.777	1.114

Table 3.8 Simulation summary of balun

3.3.2.2 Simulated and Measured Results

In this section, we show the measurement results of the SSB mixer. The measurements were performed with the chip directly mounted on FR4 PCB with SMA connectors. Fig. 3.54 shows the test board with die mounted on printed circuit board (PCB). Fig. 3.55 shows the PCB layout. The chip layout and microphotograph are shown in Fig. 3.56 and Fig. 3.57. The die size is 0.620×0.693 mm2 including pads. The DC power supplier provide 1.8V dc source to mixer in measurement. This circuit need another DC source to switch negative gain. Power consumption is 10mW.

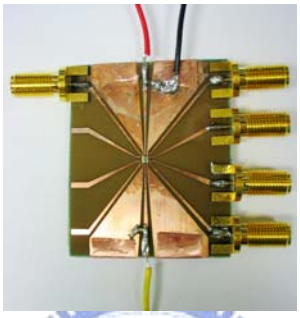


Fig. 3.54. Die bonded to the PCB.

Fig. 3.55. PCB layout.

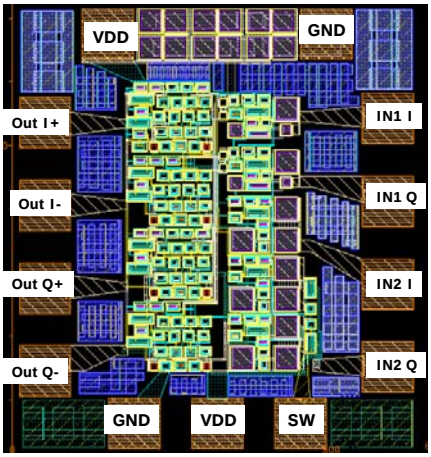


Fig. 3.56. The chip layout of SSB mixer.

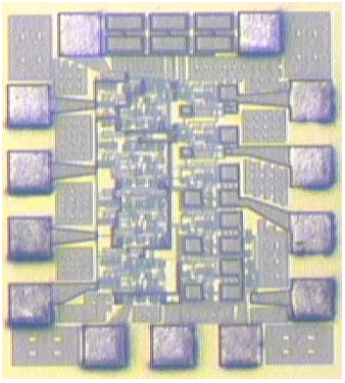


Fig. 3.57. Microphotograph of SSB mixer.

We simulated the overall 14 bands of UWB. List two of them as below. In band 7 (6336MHz：7920-1584 MHz), the sideband rejection ratio is 48dB and carrier rejection ratio is 25dB. In band 13 (9504MHz：7920+1584 MHz), the sideband rejection ratio is 48dB and carrier rejection ratio is 25dB.

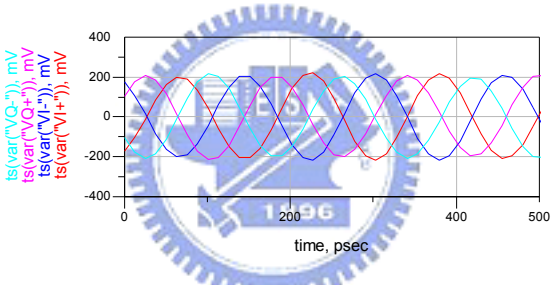


Fig. 3.58. Output waveform of band 7.

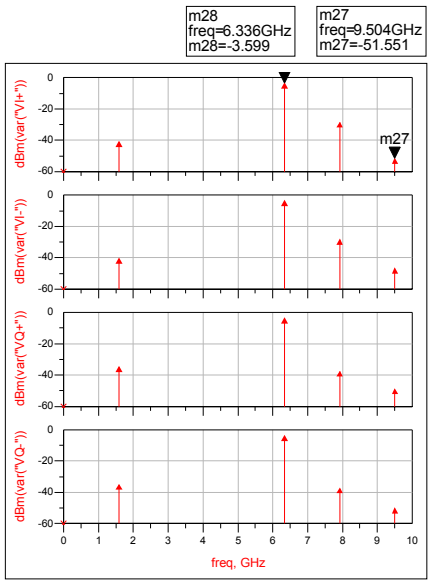


Fig. 3.59. Output spectrum of band 7.

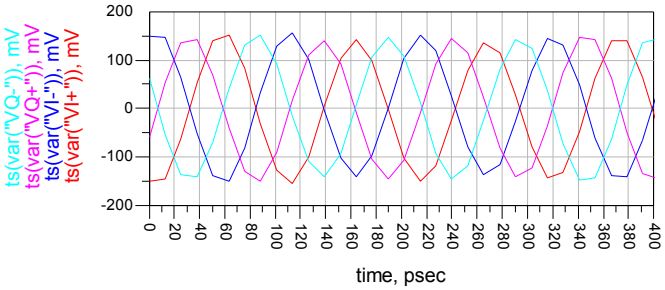


Fig. 3.60. Output waveform of band 13.

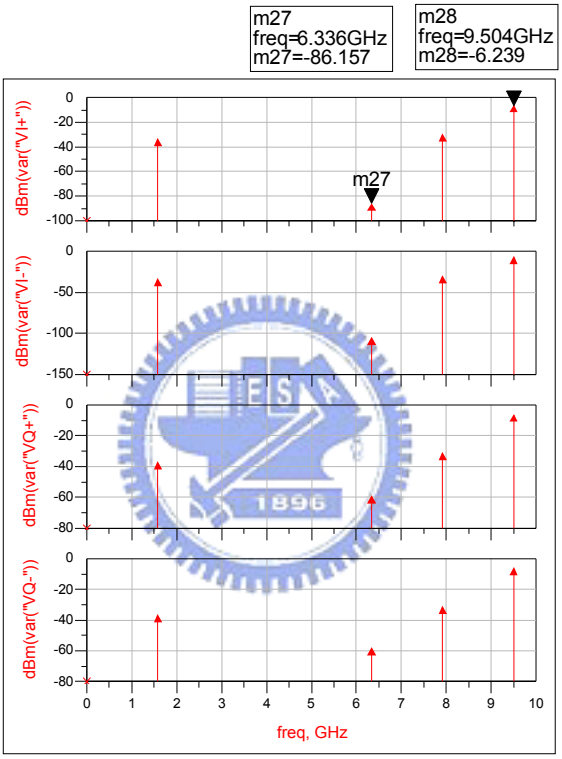


Fig. 3.61. Output spectrum of band 13.

Finally, the overall 14 bands output spectrums of UWB are measured. The DC power supplier provides two 1.8V dc source to VDD and switch in measurement. Fig. 3.62 shows the measurement setup of SSB mixer. The microstrip quadrature hybrid of 528MHz, 3960MHz, and 7920MHz are simulated by IE3D and made as shown in Fig. 3.63, Fig. 3.64, and Fig. 3.65. The quadrature hybrid of 2112 MHz, 1584 MHz, and 1056 MHz are provided by CIC (1~12.4G/ 90^{O} KRYTAR/ Model 1230). List measured output spectrum as shown in Fig. 3.66, Fig. 3.67, Fig. 3.68, and Fig. 3.69.

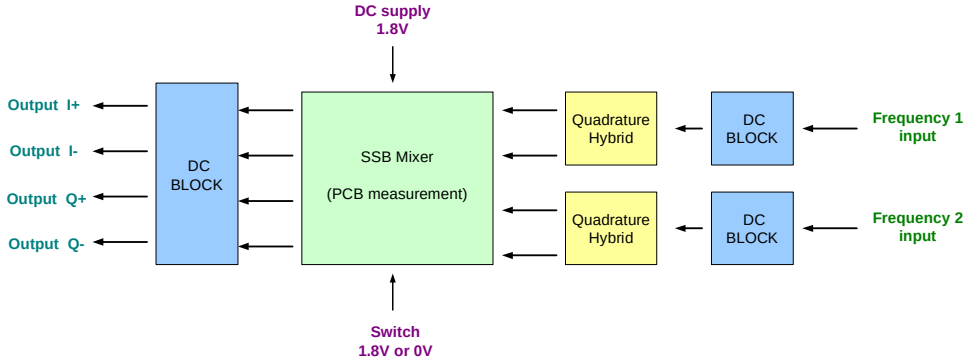


Fig. 3.62. Measurement setup of SSB mixer.

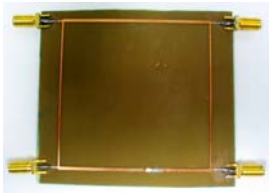


Fig. 3.63. The quadrature hybrid of 528MHz.

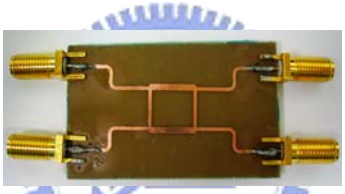


Fig. 3.64. The quadrature hybrid of 3960MHz.

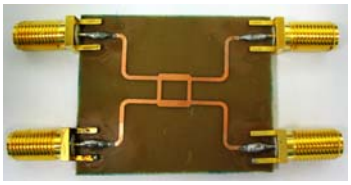


Fig. 3.65. The quadrature hybrid of 7920MHz.

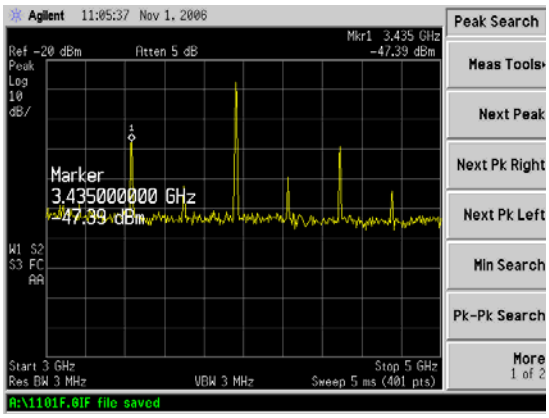


Fig. 3.66. Output spectrum of band 1.

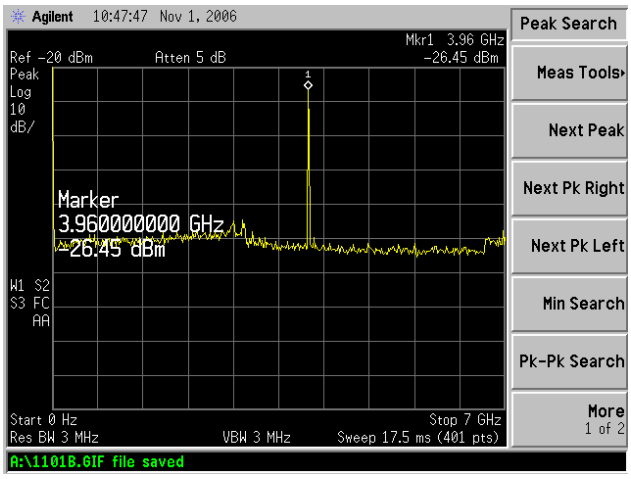


Fig. 3.67. Output spectrum of band 2

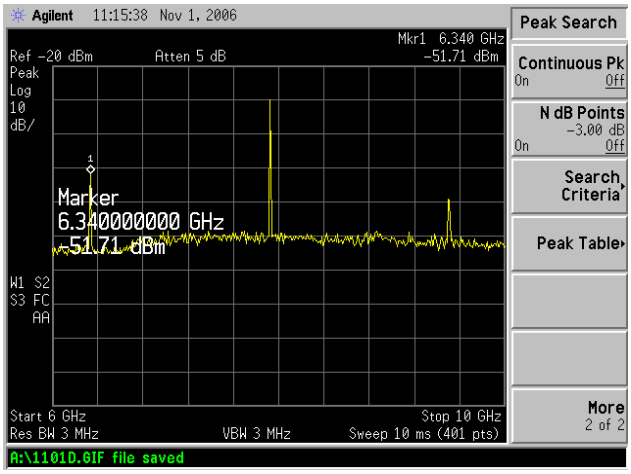


Fig. 3.68. Output spectrum of band 7.

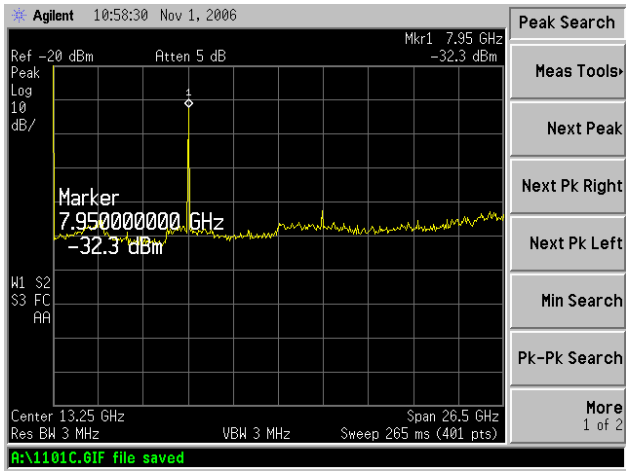


Fig. 3.69. Output spectrum of band 10.

3.3.3 Performance Summary

The single side band mixer using CMOS TSMC 0.18um is designed. This circuit is designed for UWB synthesizer. In this design, we use high linearity transconductor to improve linearity, and use the SSB mixer architecture to suppress side band. We adopt negative gain block to select upper side band or lower side band. From measurement results, output signal is too small and the input feedthrough to output is serious. The simulation and measurement summary is shown as Table 3.9. The sideband rejection performance is worse. This seems cause by unmatched off-chip output buffer.

Parameters	Simulation	Measurement
Process	TSMC 0.18um CMOS	
Supply voltage	1.8 V	
Ouptut frequency	UWB Band 1 ~ Band 14	
Spurious	< -20 dBc	< -10 dBc
Sideband suppression	Worst case ：48dBc	Worst case ：10dBc
Power consumption	10.278 mW	10.8mW
Die area (mm2)	0.620 X 0.693 (active area: 0.303 X 0.456)	

Table 3.9 Simulation and measurement summary

Chapter 4 *The Design of 24 GHz Voltage-Controlled Oscillator and Phase-Locked Loop*

In this chapter, two kinds of 24 GHz voltage-controlled oscillator (VCO) and one kind of 24 GHz phase-locked loop (PLL) for collision avoidance radar system are presented.

4.1 The Design of 24 GHz VCO 01

In this section, design, implementation, and simulation of 24 GHz LC VCO with differential signal generation is presented. First, the design and analysis of the proposed VCO is introduced. Then, the simulation results are discussed. Finally, comparison and summary are presented.

4.1.1 Circuit Topology

4.1.1.1 The Current-Reuse LC VCO

Several LC VCO topologies have been proposed in past and present literature, such as NMOS-pair cross-coupled LC VCO, PMOS-pair cross-coupled LC VCO, and NMOS-pair & PMOS-pair cross-coupled LC VCO. Fig. 4.1, Fig. 4.2, and Fig. 4.3 show three such kinds of VCOs with a current source. The symmetric topologies have

the advantage that they create the symmetric waveforms and could reduce the l/f noise up conversion [37]. If there is no current source in VCO, the VCO has the benefit of better phase noise. A widely known oscillator is the conventional differential negative-Gm oscillator that is shown in Fig. 4.1. The topology consists of two identical half circuits composed of switching transistors, inductors, and varactors. A signal feeds back from the drain of M1 to the gate of M2 which acts as an active buffer, and vice versa. The topology of Fig. 4.3 consumes more voltage headroom, larger MOS sizes are needed to get enough transconductance to lower the overdrive voltage. But the parasitic capacitances will increase and thus the tuning range will reduced. The transconductance of the topologies are determined by the current consumption and the sizes of devices. The cross-coupled MOS pair forms the positive feedback and the input impedance Rin = (-2/g_{mn}) + (-2/g_{mp}) in Fig. 4.3. The VCOs in Fig. 4.1 and Fig. 4.2 have the larger voltage headroom and the wider tuning range. The related smaller geometry of the devices is sufficient to get enough transconductance to start the oscillation. The input impedance of cross-coupled pair is Rin = -2/g_{mn} or -2/g_{mp} in Fig. 4.1 or Fig. 4.2. Therefore, these three topologies have their own trade-offs.

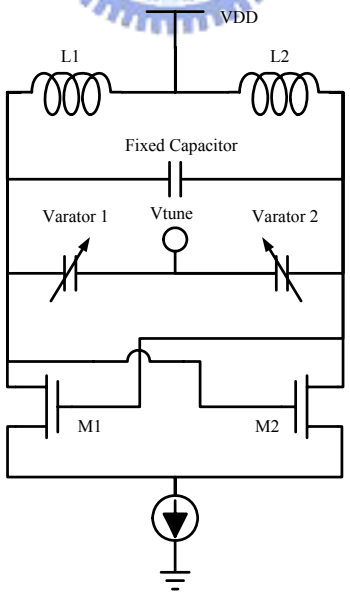


Fig. 4.1. NMOS-pair cross-coupled LC VCO.

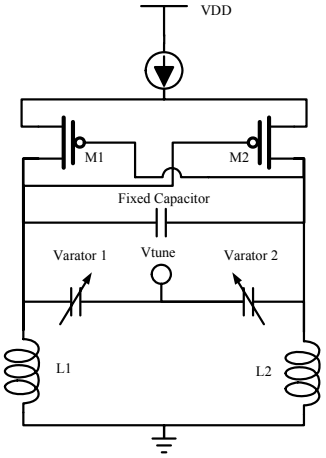


Fig. 4.2. PMOS-pair cross-coupled LC VCO.

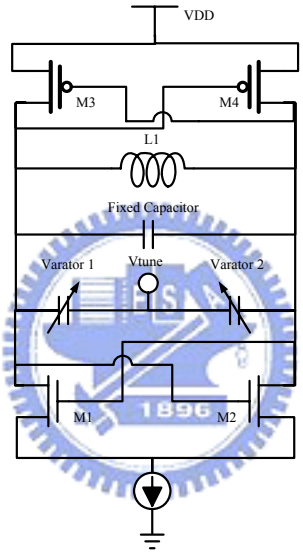


Fig. 4.3. NMOS-pair & PMOS-pair cross-coupled LC VCO.

In Fig. 4.4, this topology uses both NMOS and PMOS transistors as a negative conductance generator, which is improved from conventional NMOS-pair & PMOS-pair cross-coupled LC VCO. The series stacking of NMOS and PMOS allows the supply current to be reduced by half compared to that of the conventional LC VCO while providing the same negative conductance. This structure drives the current in the half of period and let the LC tank discharge in another half period to create the oscillation [38]. Because the NMOS & PMOS pair operates in triode region near the peak of the voltage swing, the voltage swing is only limited by the power supply. Recently, three current-reuse CMOS LC VCO has been published [38],[39],[40]. Two types of low power current-reuse CMOS differential LC VCO are shown in Fig. 4.5 and Fig. 4.6.

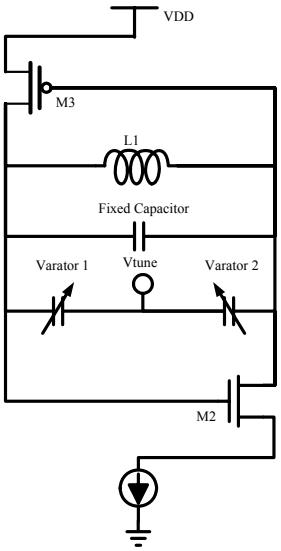


Fig. 4.4. NMOS & PMOS pair LC VCO.

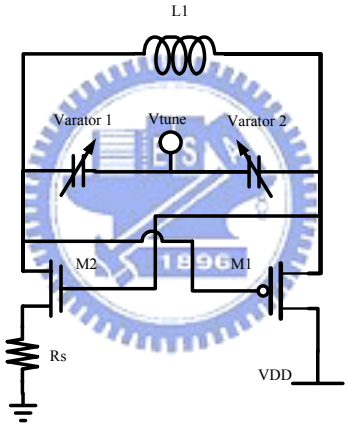


Fig. 4.5. Current-reuse LC VCO by Seok-Ju Yun [38].

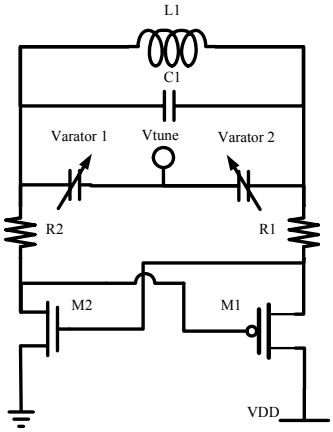


Fig. 4.6. Current-reuse LC VCO by Zheng Wang [39].

4.1.1.2 Noise Filtering Technique

As published by Leeson [41], the phase noise of an LC VCO can be described as equation 4.1. In Leeson's equation, Δf is offset frequency, Q is loaded quality factor of the LC tank, Ao is voltage swing amplitude, F is excess noise factor, $\Delta f_{1/f^3}$ is corner frequency of device's flicker noise, and f_0 is oscillation frequency. This equation describes that the most effective way to lower phase noise to improve the loaded quality factor of the LC tank. In order to reduce the phase noise of VCO, the research has been focus on improving the quality factor of the LC tank and suppressing the harmonics inside the VCO core.

$$L(f_0) = \frac{2kTR_{eq}F}{A_0^2}\left(\frac{f_0}{2Q\Delta f}\right)^2\left(1+\frac{\Delta f_{1/f^3}}{\Delta f}\right) \tag{4.1}$$

$$\overline{i_{1/f}^2} = \frac{K_f}{fC_{ox}LW}\Delta f \tag{4.2}$$

Low frequency bias noise would be up converted into phase noise through the switching action of the cross-coupled transistors [46]. The high-frequency bias noise is usually grounded by the large junction capacitances of the bias transistors. PMOS device is preferred to bias the circuit than NMOS device because PMOS has lower corner frequency of flicker noise. From equation 4.2, large device size is used since the flicker noise is related to the device size. The nonlinear of the transistors will generate harmonic distortion at the VCO tank output nodes. Second and third harmonics of the fundamental current flow into the lower impedance side of the LC tank. Reducing device sizes means more low frequency flicker noise would be up converted into phase noise. Therefore the optimum device sizing is a tradeoff between AM-PM conversion factor and switching device's flicker noise.

Noise Frequencies around the second harmonic down convert to the oscillation frequency, and up convert to around the third harmonic. We can use parallel inductor and capacitor at the output node of bias transistor to provide high impedance at the second harmonic. Thus parallel LC can suppress the second harmonic leaking from the LC tank across the oscillation as shown in Fig. 4.7. A noise filter in the tail tuned to the second harmonic. This circuit oscillates with the largest possible amplitude because there is no current-source in series with the differential pair to consume

voltage headroom. In other words, the noise filter consumes zero voltage headroom and outputs the largest possible amplitude.

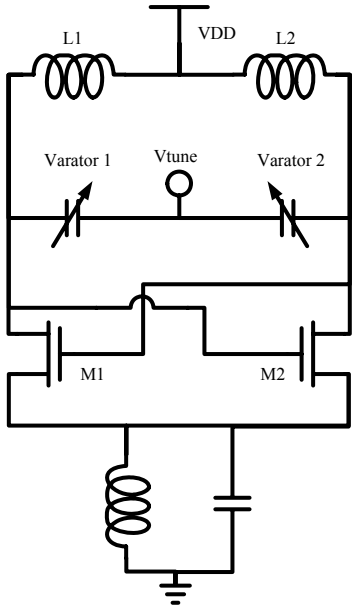


Fig. 4.7. Voltage-biased VCO with noise filter.

$$F = 2 + \frac{8\gamma IR}{\pi V_o} + \gamma \frac{8}{9} g_{mbias} R \tag{4.3}$$

Phase noise is scaled by a specific noise factor F. The noise factor is given by [47] as equation 4.3 where I is the bias current, γ is the channel noise coefficient of the transistor, R is the load resistance, g_{mbias} is the transconductance of the current source transistor, and Vo is the voltage across the resonator and is proportional to the slope at the zero crossing voltage of the switching cell [47]. The first and second terms in equation 4.3 describe the phase noise contributions from the resonator loss and differential pair transistors. The third term in equation 4.3 represents the phase noise produced by down conversion of the CS noise component at the second harmonic of the oscillation frequency. The second term can be reduced by increasing Vo. To realize the concept, we have employed a second harmonic LC tank.

4.1.1.3 The Proposed 24 GHz VCO 01

Fig. 4.8 shows the proposed VCO. It consists of current-reuse VCO structure, filtering inductor, main LC tank, and second harmonic LC tank. The two output buffer employ common source amplifier for testing purpose.

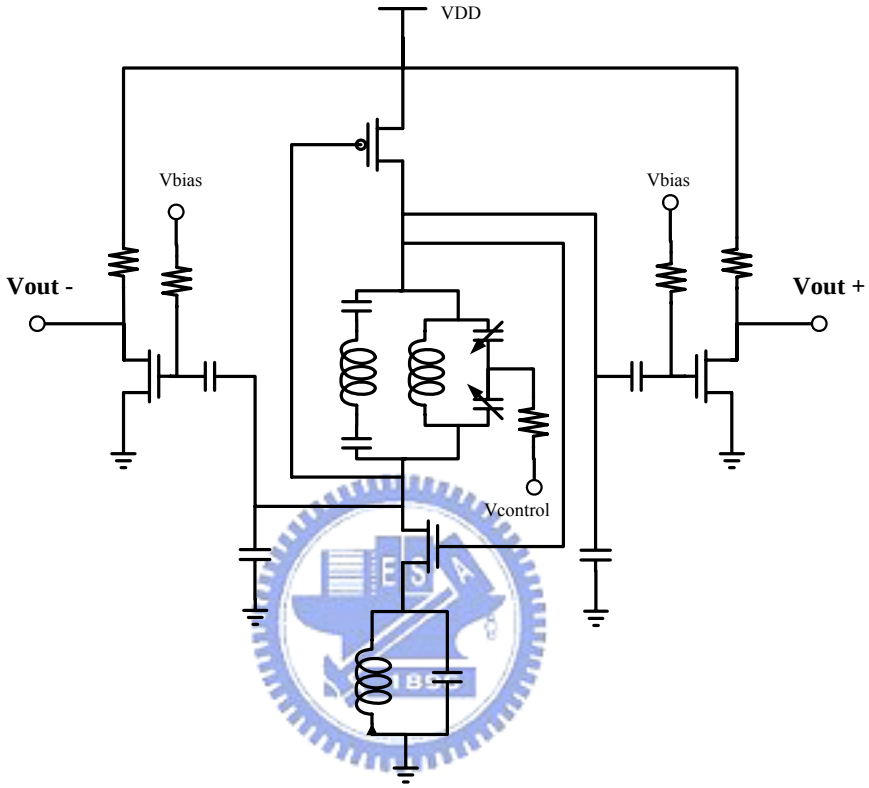


Fig. 4.8. Proposed 24 GHz VCO 01.

In CMOS VCO, the integration of a high-Q LC tank is not easy due to the low resistivity of the silicon substrate, and this greatly affects the phase-noise performance. The phase noise reduction is achieved by circuit design techniques in CMOS LC VCO. In Fig. 4.8, we use second harmonic LC tank which is open at the fundamental frequency and short at the second harmonic to suppress the down conversion of the noise around the second harmonic. The second harmonic LC tank can suppress the phase noise from various noise sources including the negative g_m core transistors. Fig. 4.9 shows the two tanks connected with 50Ω terminations. Fig. 4.10 is the simulated result of the magnitude of the S-parameter of main and second harmonic LC tanks. Fig. 4.11 is the simulated result of the magnitude of the S-parameter of total LC tank.

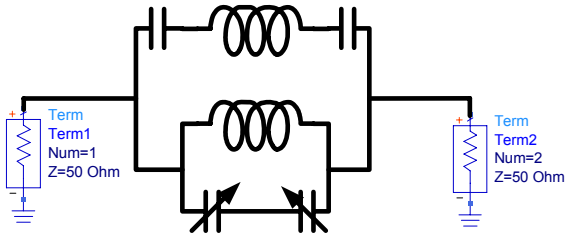


Fig. 4.9. Main LC tank and 2nd LC tank.

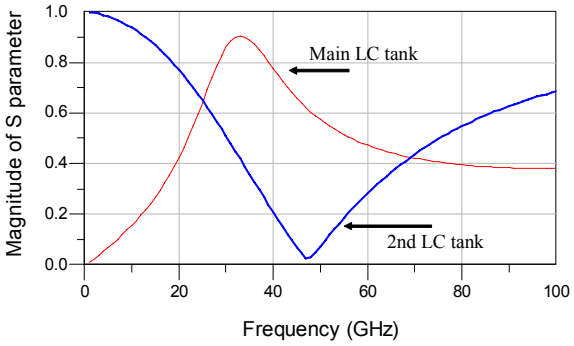


Fig. 4.10. Simulated results of main and second harmonic LC tanks.

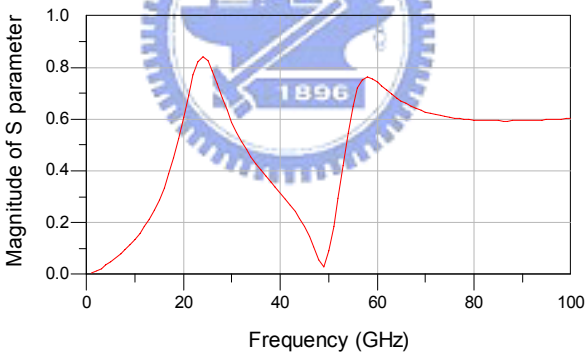


Fig. 4.11. Simulated result of total LC tank.

4.1.2 Simulated Performance

Fig. 4.12 shows the layout of the proposed VCO 01. The size of the layout is 1.03mm by 0.93mm including pads. Considering the layout effect, take the long layout line as shown in Fig. 4.13. Running EM simulation by ADS Momentum and obtain the layout effect model. Then, using ADS simulated with layout effect. Fig. 4.14 shows the output spectrum at 24GHz when control voltage is 0.75V. From output spectrum, second harmonic is 71dBc lower than fundamental tone. Fig. 4.15 shows

the phase noise performance for a carrier frequency of 24GHz. Phase noise at 1MHz offset from the carrier is -111.3 dBc/Hz. Fig. 4.16 shows the transient responses of the VCO differential output outside the buffer. The single-ended output amplitude is 280mV, which translates into -0.35dBm output power with a standard 50Ω load. The tuning range is 1.6GHz as shown in Fig. 4.17. The output power variation is 1.1dB as shown in Fig. 4.18. The simulated phase noise results for each technique in Fig. 4.19 show the phase noise reduction effect of each technique independently and the combined case for a carrier frequency of 24GHz and same power consumption. The phase noise of standard LC VCO is -101 dBc/Hz. The phase noise of filtering inductor is -105 dBc/Hz. The phase noise of 2nd harmonic LC tank is -106 dBc/Hz. Combined two techniques can improve phase noise about 10dB. Table 4.1 summarizes the VCO performance of simulated results.

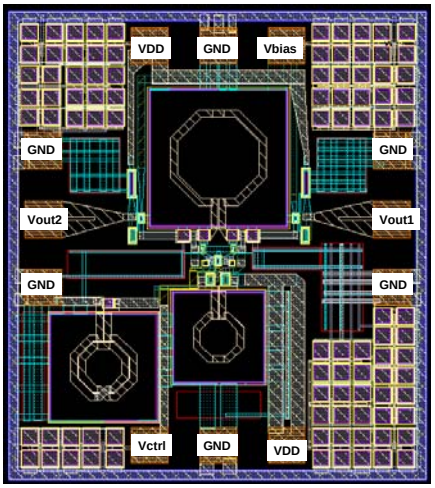


Fig. 4.12. Layout of the proposed VCO 01.

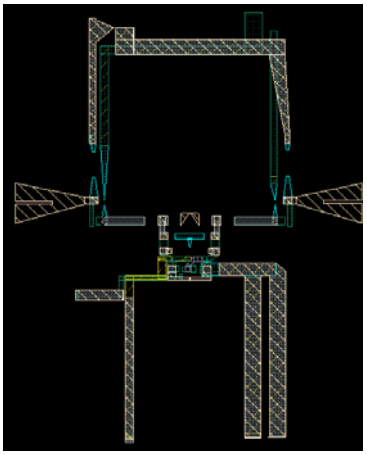


Fig. 4.13. EM consideration.

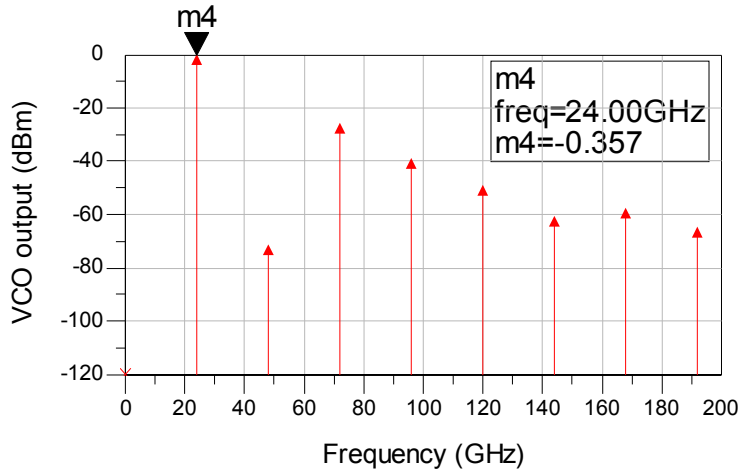


Fig. 4.14. Output spectrum at 24GHz.

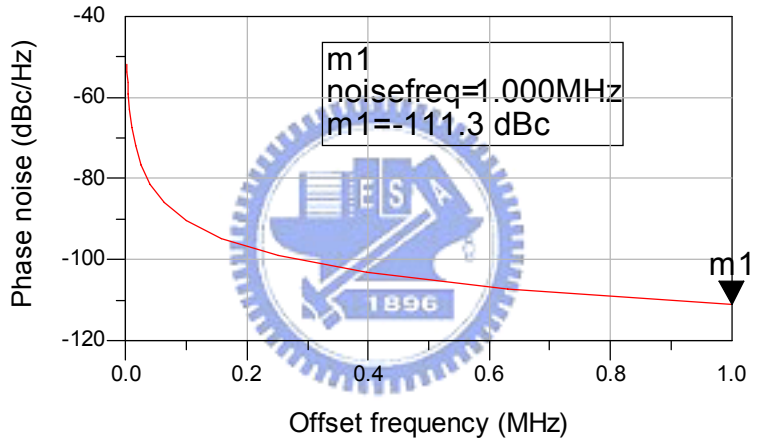


Fig. 4.15. Phase noise of the VCO at 24GHz.

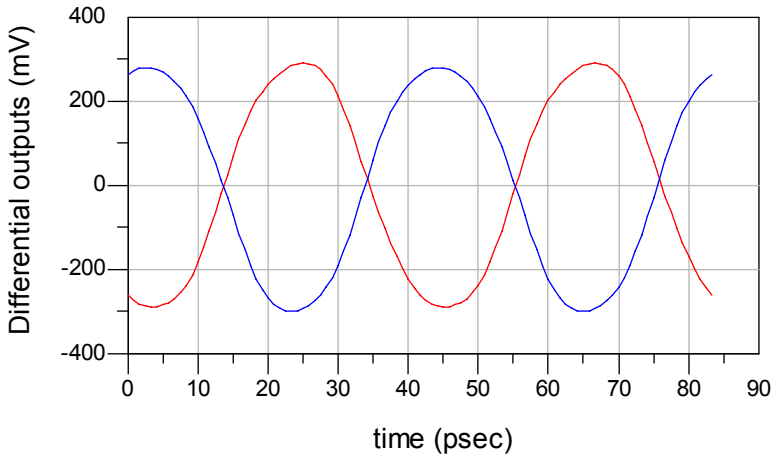


Fig. 4.16. Transient response of the VCO.

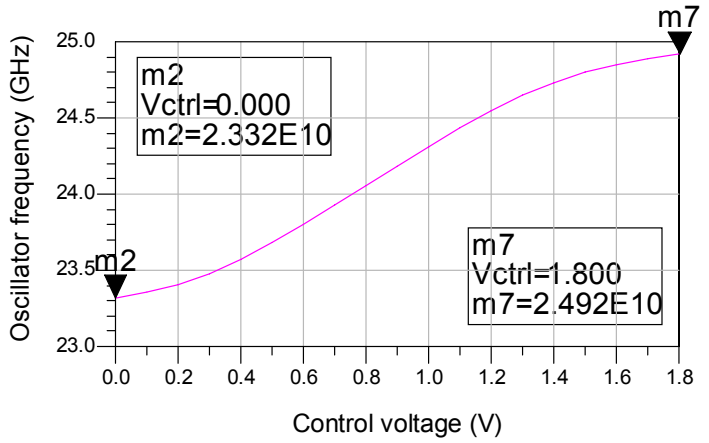


Fig. 4.17. Control voltage versus output frequency.

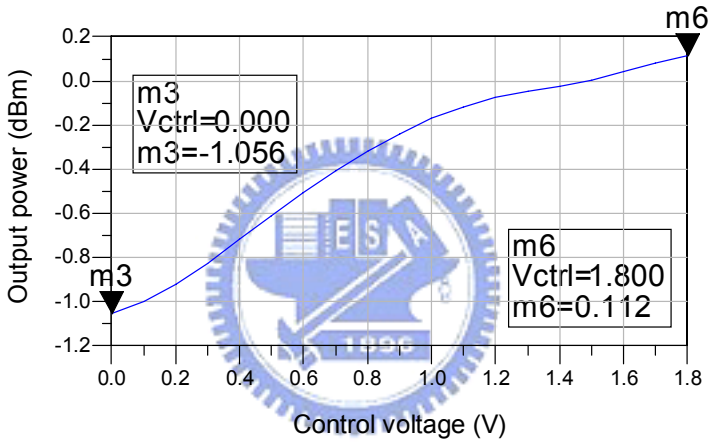


Fig. 4.18. Control voltage versus output power.

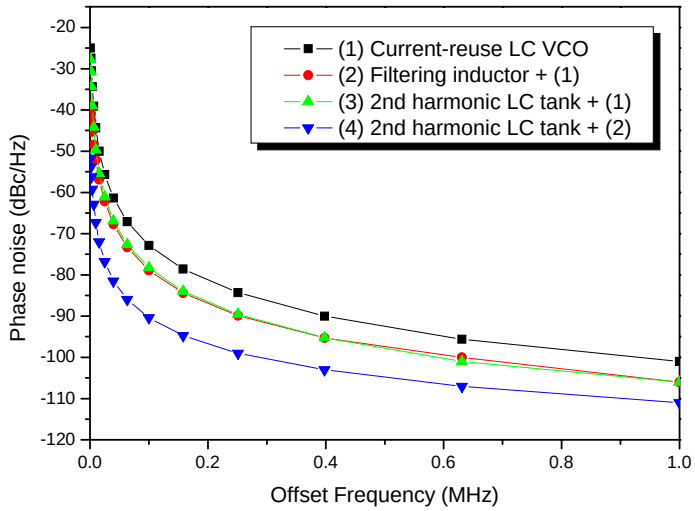
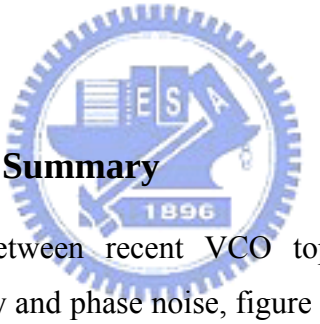


Fig. 4.19. Simulated phase noise results for each technique.

Parameters	Simulation result
Technology	TSMC 0.18um CMOS
Center frequency (GHz)	24
Supply voltage (V)	1.8
Core Current (mA)	5.5
Tuning Range (GHz)	23.32 ～ 24.92
Vtune (V)	0 ～ 1.8
Output Power (dBm)	-0.357
Phase Noise @1MHz offset (dBc/Hz)	-111
Chip area (mm^2)	1.03 X 0.93
Power Consumption (mW)	10

Table 4.1 Summary of VCO 01 simulation results



4.1.3 Comparison and Summary

For the comparisons between recent VCO topologies in terms of power consumption, carrier frequency and phase noise, figure of merit (FOM) expression for 1MHz offset is used as equation 4.3 Where fo is the carrier frequency, Δf is the offset, L(Δf) is the phase noise, and P is the power consumption by the VCO.

$$FOM = -L(\Delta f) + 20\log\left(\frac{f_0}{\Delta f}\right) - 10\log(P) \tag{4.3}$$

The comparison of the proposed VCO against recently reported high frequency VCOs (Frequency > 20GHz) is shown in Table 4.2. It can be seen that this simulated VCO achieves better phase noise due to second harmonic filtering. The FOM of proposed VCO is -189. It's better than recently reported CMOS VCOs. Ref. [52] is designed at 24GHz and using 8GHz VCO cascaded with frequency tripler. Ref. [53] is using ring oscillator structure. The first one of Ref. [56] is designed at 24GHz and using 12GHz VCO cascaded with mixer. The second of Ref. [56] is designed at 24GHz and using 24GHz stand-alone VCO.

PERFORMANCE OF REPORTED HIGH FREQUENCY VCOs (Frequency > 20 GHz)

Ref.	Technology	fosc [GHz]	Tuning range [GHz]	Output power [dBm]	Phase Noise [dBc/Hz]	Offset frequency	Supply voltage [V]	Power dissipation [mW]	FOM [dBc/Hz]
[48]	GaAs	60	1.6	-4	-93	1MHz	3.5	158	-167
[49]	GaAs	25	0.42	-1	-130	1MHz	3.5	90	-195
[50]	0.25um SiGe	21.5	1.06	-6	-113	1MHz	3.2	130	-178
[51]	0.35um SiGe	42	10.9	3.5	-110	1MHz	5.5	280	-179
[52]	SiGe	23.5	0.42	-10	-100	1MHz	3.3	180	-165
[53]	0.12um SiGe	24.3	6.5	-14	-105	10MHz	3.3	105	-152
[54]	0.25um SiGe	32	2	-19	-97	1MHz	5	215	-163
[55]	0.12um SOI CMOS	44	4	-6	-101	1MHz	1.5	7.5	-185
[56]	0.18um CMOS	25.1	3	-18.8	-100	1MHz	2.2	11	-177
[56]	0.18um CMOS	21.6	1.6	-4.2	-102	1MHz	3	45	-172
[57]	0.25um CMOS	19.4	5	-20.4	-101	1MHz	4.5	9	-177
This work	0.18um CMOS	24	1.6	-0.3	-111	1MHz	1.8	10	-189

Table 4.2. Summary of the comparison

This section presents current-reuse voltage-controlled oscillator (VCO) topologies by stacking switching transistors in series like a cascode. The VCOs can operate with only half the amount of dc current compared to those of the conventional VCO topologies. A filtering inductor was used at the source node of the NMOS transistor to improve phase noise. The second harmonic LC tank is used to suppress the second harmonic as well as leaking from the LC tank across the oscillation. These two techniques can improve phase noise more than 10dB totally at the carrier frequency of 24GHz. A 24GHz LC VCO was fabricated in a 0.18um CMOS process. The simulation result shows the achieved phase noise of -111 dBc/Hz at 1-MHz offset while the VCO core draws 5.5mA from a 1.8V supply. The tuning range is from 23.32GHz to 24.92GHz. The size of the layout is 1.03mm by 0.93mm including pads.

4.2 The Design of 24 GHz VCO 02

In this section, another 24 GHz LC VCO is presented. First, the design and analysis of the proposed VCO is introduced. Then, the simulation results are discussed. Finally, comparison and summary are discussed.

4.2.1 Circuit Topology

Fig. 4.20 shows the proposed VCO. It consists of current-reuse VCO structure, filtering inductor, main LC tank, and T-structure filter. The two output buffer employ common source amplifier for testing purpose.

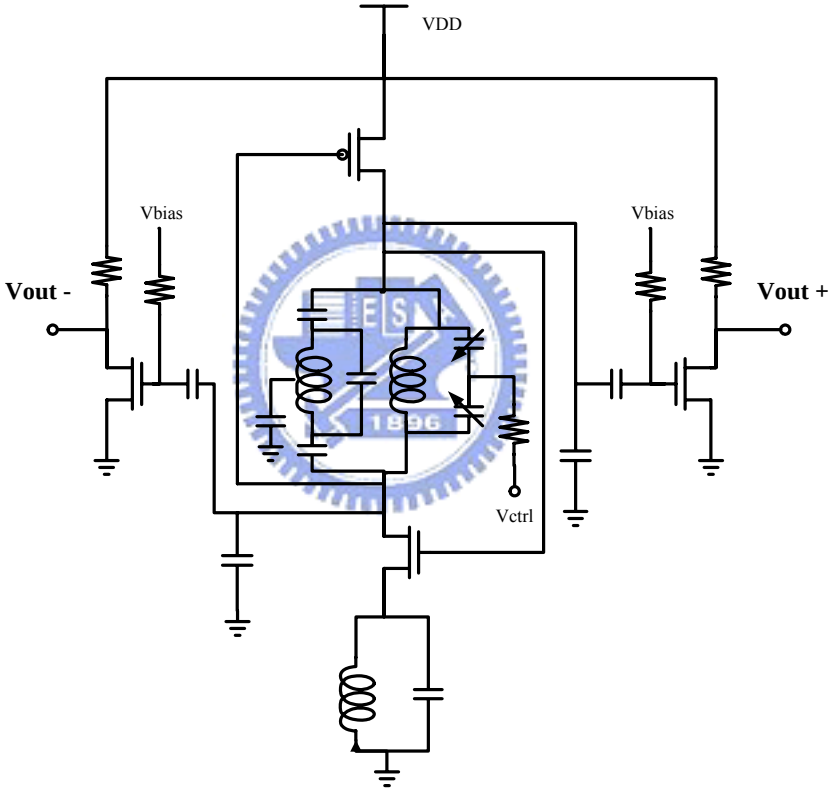


Fig. 4.20. Proposed 24 GHz VCO 02.

In Fig. 4.20, we use T-Structure filter to suppress effect of harmonics. The T-Structure filter consists of L and C is shown in Fig. 4.21. It's a 2^{nd} order filter and the 4^{th} order transfer function is shown as equation 4.4. The T-Structure filter is added parallel with main LC tank. From the transfer function, we have the zero as equation 4.5. The zero frequency is designed at the desired frequency. The Q of this filter is as equation 4.6. Fig. 4.22 shows the two tanks connected with 50Ω terminations. Fig. 4.23 is the simulated result of the magnitude of the S-parameter of T-Structure filter

and main LC tank. There are two poles at 48GHz and 72GHz.

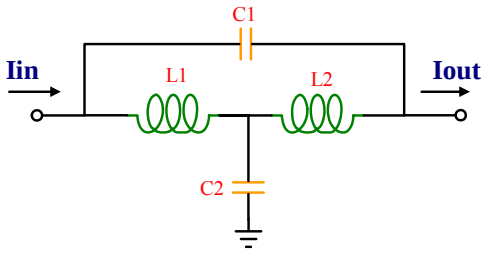


Fig. 4.21. T-Structure filter consists of LC.

$$\frac{I_{out}}{I_{in}} = T(s) = \frac{S^4 + S^2(\frac{1}{L_1 + L_2})\frac{1}{C_2} + \frac{1}{C_1 C_2 L_1 L_2}}{S^4 + S^2(\frac{1}{C_2 L_1} + \frac{1}{C_2 L_2} + \frac{1}{C_1 L_2}) + \frac{1}{C_1 C_2 L_1 L_2}} \tag{4.4}$$

$$f_{zero} = \frac{1}{\sqrt[4]{L_1 L_2 C_1 C_2}} \tag{4.5}$$

$$Q = [\frac{\sqrt{L_1 L_2 C_1 C_2}}{C_2}(\frac{1}{L_1} + \frac{1}{L_2})]^{-1} \tag{4.6}$$

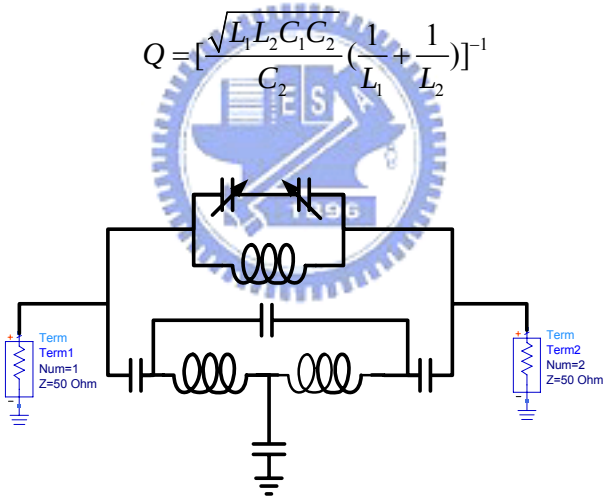


Fig. 4.22. Main LC tank and T structure filter.

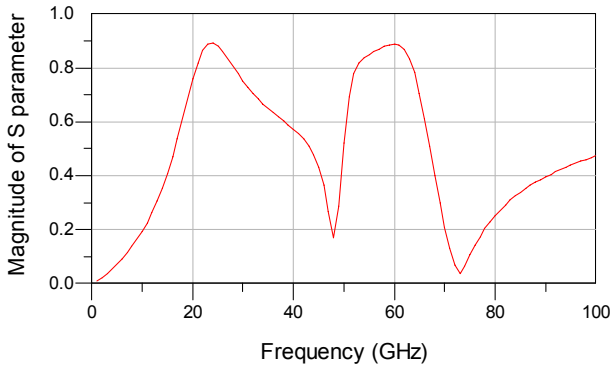


Fig. 4.23. Simulated result of magnitude of the S parameter.

4.2.2 Simulated Performance

Fig. 4.24 shows the layout of the proposed VCO 02. The size of the layout is 0.90mm by 0.93mm including pads. Considering the layout effect, take the long layout line as shown in Fig. 4.25. Running EM simulation by ADS Momentum and obtain the layout effect model. Then, using ADS simulated with layout effect. Fig. 4.26 shows the output spectrum at 24GHz when control voltage is 0.75V. Fig. 4.27 shows the phase noise performance for a carrier frequency of 24GHz. Phase noise at 1MHz offset from the carrier is -111.6 dBc/Hz. Fig. 4.28 shows the transient responses of the VCO differential output outside the buffer. The single-ended output amplitude is 280mV, which translates into -0.68dBm output power with a standard 50Ω load. The tuning range is 1.56GHz as shown in Fig. 4.29. The output power variation is 1.3dB as shown in Fig. 4.30. The simulated phase noise results for each technique in Fig. 4.31 show the phase noise reduction effect of each technique independently and the combined case for a carrier frequency of 24GHz and same power consumption. The phase noise of standard LC VCO is -101 dBc/Hz. The phase noise of filtering inductor is -105 dBc/Hz. The phase noise of T structure filter is -106 dBc/Hz. Totally combined two techniques can improve phase noise about 10dB. Table 4.3 summarizes the VCO performance of simulated results.

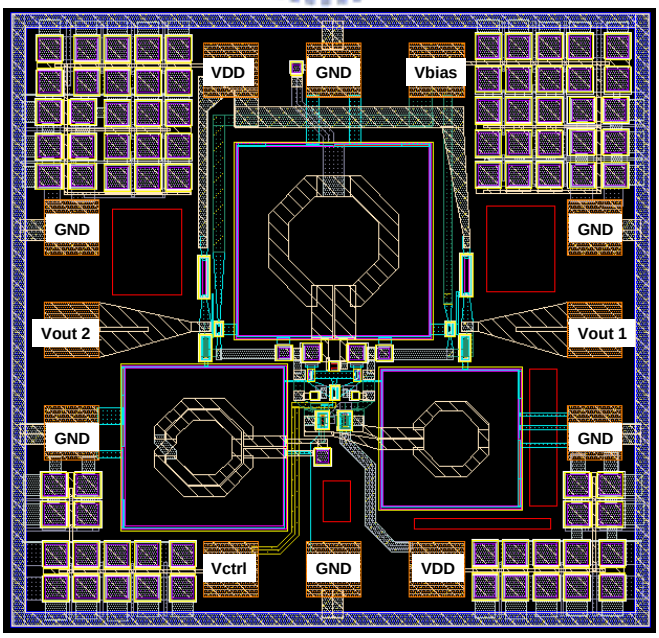


Fig. 4.24. Layout of the proposed VCO 02.

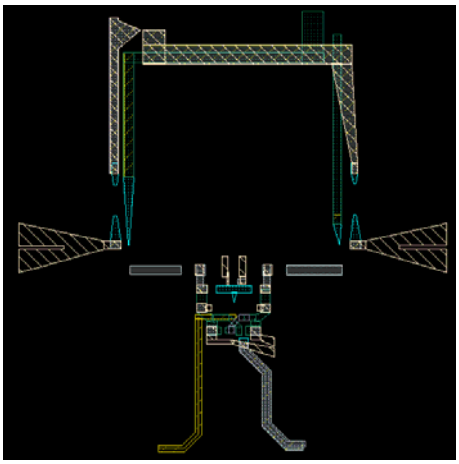


Fig. 4.25. EM consideration.

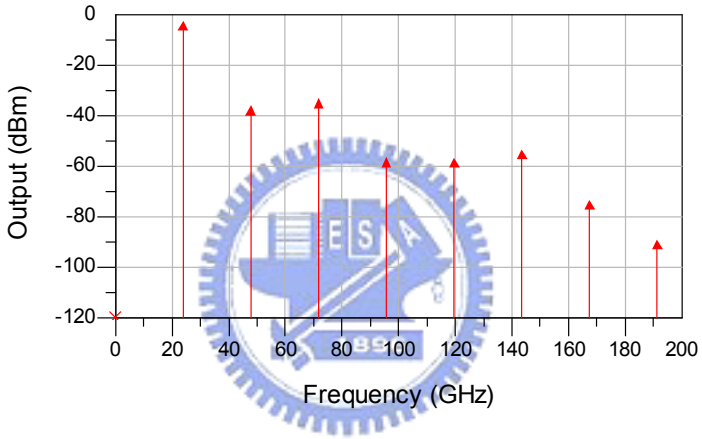


Fig. 4.26. Output spectrum at 24GHz.

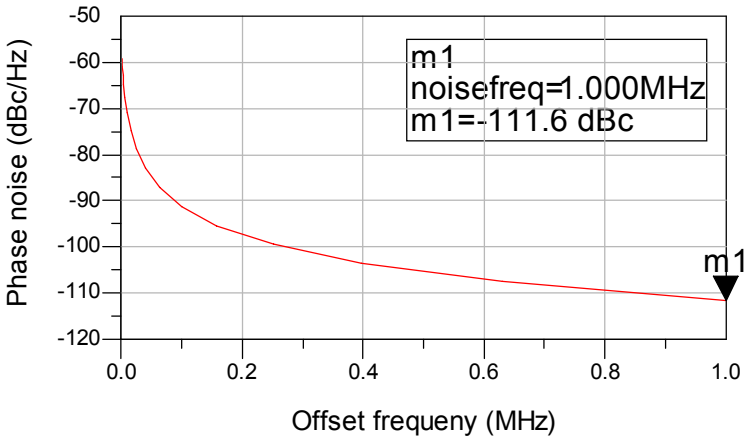


Fig. 4.27. Phase noise of the VCO at 24GHz.

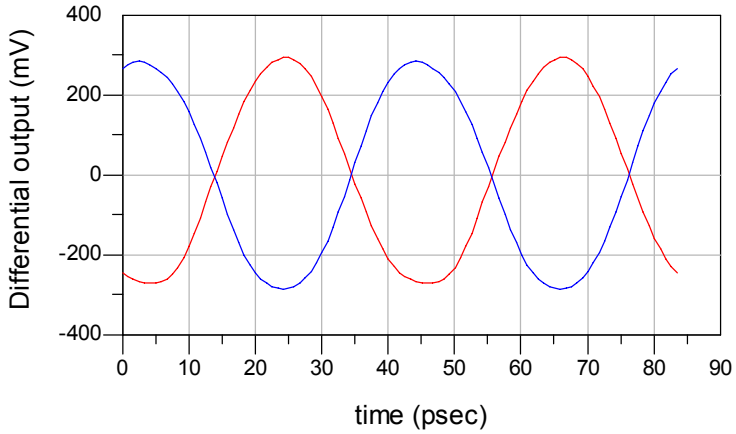


Fig. 4.28. Transient response of the VCO.

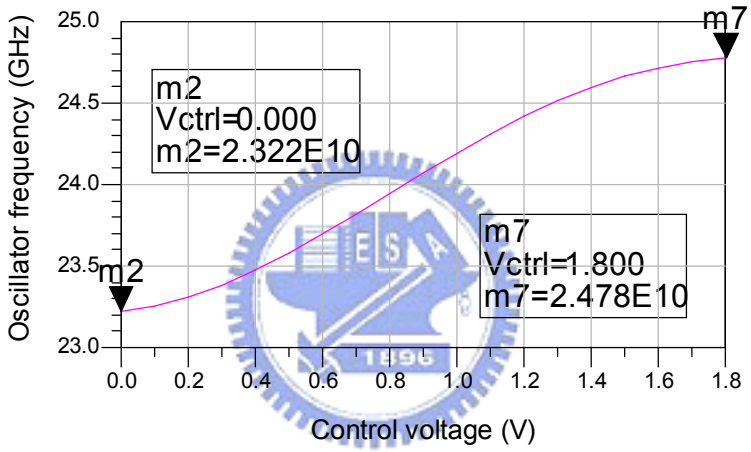


Fig. 4.29. Control voltage versus output frequency.

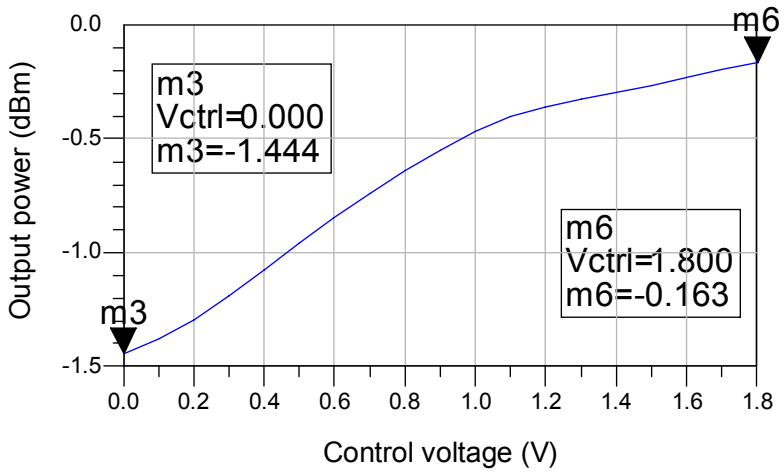


Fig. 4.30. Control voltage versus output power.

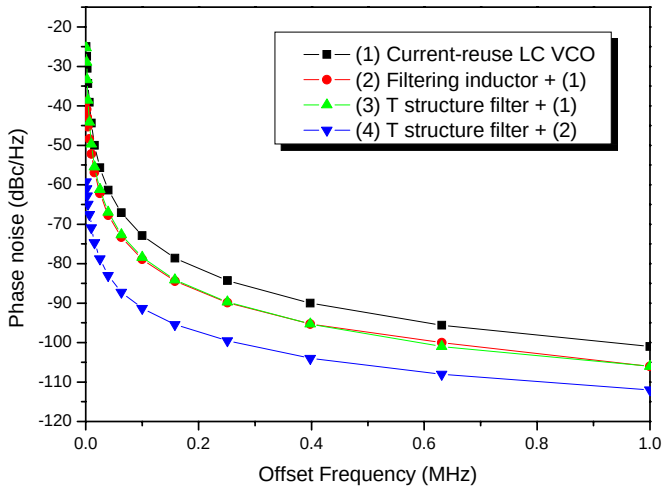


Fig. 4.31. Simulated phase noise results for each technique.

Parameters	Simulation result
Technology	TSMC 0.18um CMOS
Center frequency (GHz)	24
Supply voltage (V)	1.8
Core Current (mA)	5.5
Tuning Range (GHz)	23.22 ~ 24.78
Vtune (V)	0 ~ 1.8
Output Power (dBm)	-0.68
Phase Noise @1MHz offset (dBc/Hz)	-111.6
Chip area (mm^2)	0.90 X 0.93
Power Consumption (mW)	9.9

Table 4.3 Summary of VCO 02 simulation results

4.2.3 Comparison and Summary

The comparison of the proposed VCO against recently reported high frequency CMOS VCOs (Frequency > 20GHz) is shown in Table 4.4. The FOM of proposed VCO is -189. It's better than recently reported CMOS VCOs. Fig. 4.32 shows the simulated summary of phase noise reduction technique. In this figure, (5) is VCO01 and (6) is VCO02.

PERFORMANCE OF REPORTED HIGH FREQUENCY CMOS VCOs (Frequency > 20 GHz)

Ref.	Technology	fosc [GHz]	Tuning range [GHz]	Output power [dBm]	Phase Noise [dBc/Hz]	Offset frequency	Supply voltage [V]	Power dissipation [mW]	FOM [dBc/Hz]
[56]	0.18um CMOS	25.1	3	-18.8	-100	1MHz	2.2	11	-177
[56]	0.18um CMOS	21.6	1.6	-4.2	-102	1MHz	3	45	-172
[57]	0.25um CMOS	19.4	5	-20.4	-101	1MHz	4.5	9	-177
This work	0.18um CMOS	24	1.56	-0.68	-111.6	1MHz	1.8	9.9	-189

Table 4.4 Summary of the comparison

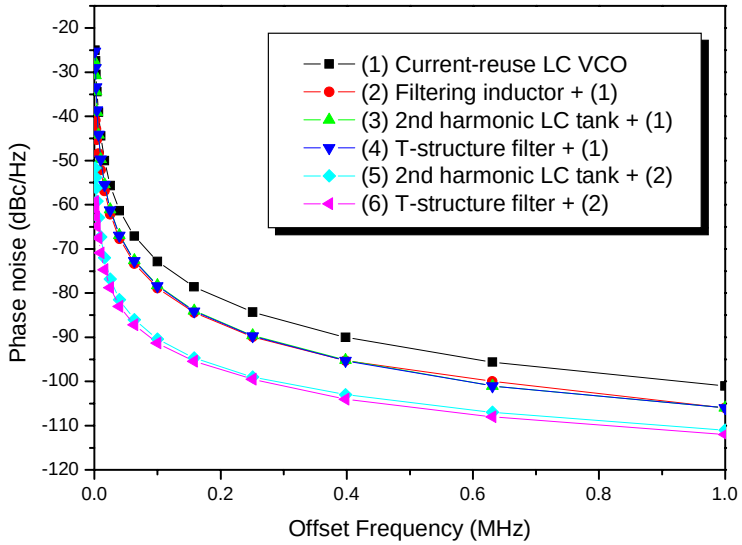


Fig. 4.32. Simulated summary of phase noise reduction technique.

This section presents current-reused voltage-controlled oscillator topologies by stacking switching transistors in series like a cascode. The VCOs can operate with only half the amount of dc current compared to those of the conventional VCO topologies. A filtering inductor was used at the source node of the NMOS transistor to improve phase noise. The T-structure is used to suppress harmonics as well as leaking from the LC tank across the oscillation. These two techniques can improve phase noise more than 10dB totally at the carrier frequency of 24GHz. A 24GHz LC VCO was fabricated in a 0.18um CMOS process. The simulation result shows the achieved phase noise of -111 dBc/Hz at 1-MHz offset while the VCO core draws 5.5mA from a 1.8V supply. The tuning range is from 23.32GHz to 24.782GHz. The size of the layout is 0.90mm by 0.93mm including pads.

4.3 The Design of 24 GHz PLL

In this section, a 24 GHz Phase-Locked Loop (PLL) for collision avoidance radar system are presented. First, the design of the proposed PLL is described. Then, the simulation results are discussed. Finally, summary are presented.

4.3.1 Phase-Locked Loop Design

4.3.1.1 Proposed PLL Architecture

In this design, we have chosen to synthesize directly the 24 GHz signal without frequency multiplication. Despite the difficulties of designing the VCO and the prescaler at so high frequencies, we have chosen this solution to achieve 24 GHz PLL. Phase-locked loop is a circuit in which the phase of a local oscillator is tracing and locking the phase of a reference frequency. PLL consists of phase frequency detector, charge pump, loop filter, voltage-controlled oscillator, prescaler and frequency divider. The PLL schematic is shown Fig. 4.33. The phase detector is a precharge-type PFD. The phase detector output is connected to a charge pump. The latter is followed by a passive type II filter for better rejection at higher frequencies. The VCO output supplies the prescaler and the PLL output. The prescaler is followed by a divider-by-256. The following sections will introduce the details of the proposed PLL architecture.

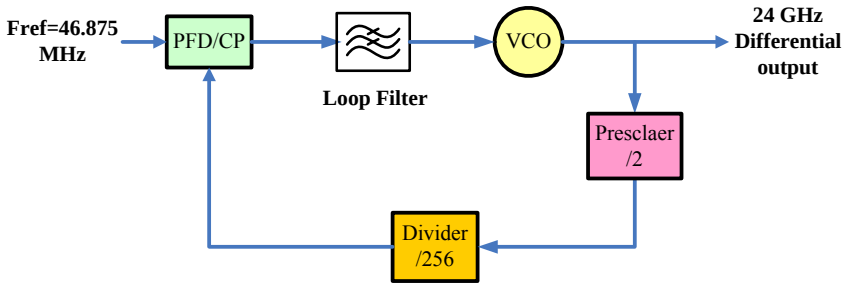


Fig. 4.33. Proposed PLL architecture.

4.3.1.2 Low Power VCO

The VCO is the most important block of the PLL because it works at a high frequency and requires a low phase noise. There are several ways to build a VCO. In this work, we adopted the NMOS-pair cross-coupled LC tank VCO with filtering

inductor and substrate resistors. Here we adopted filtering inductor and substrate resistors to improve phase noise. The VCO schematic is shown in Fig.4.34. The two output buffers employ common source amplifiers for testing purpose. VDD is 0.6V for low power purpose and power consumption of VCO core is 0.8mW.

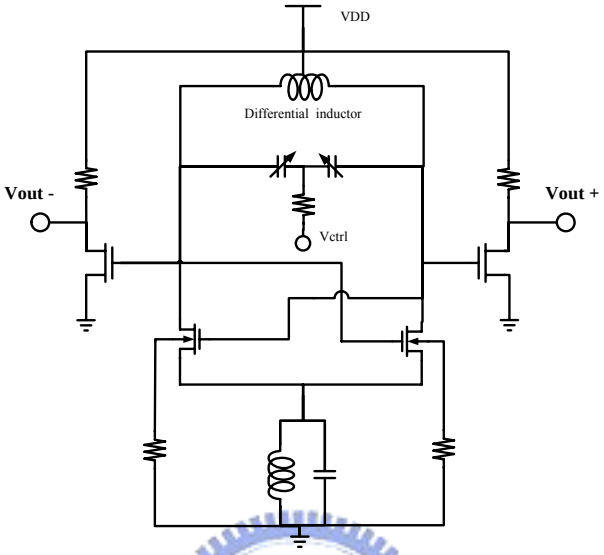


Fig. 4.34. VCO core schematic.

4.3.1.3 Divide-by-2 Prescaler

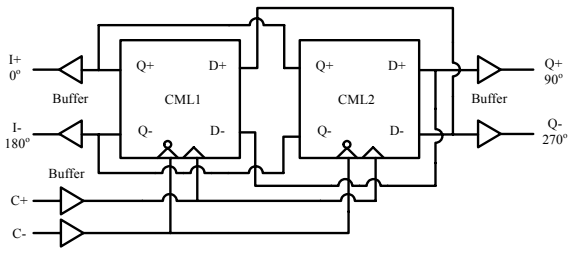


Fig. 4.35. Block diagram of the Prescaler.

In this work, the prescaler follows the VCO which is operates at 24 GHz. The topology of the static frequency divider including input and output buffers is shown in Fig. 4.35. The divider core consists of a differential CML D-flip-flop (DFF), where the output is inverted and fed back to the data input. The DFF is built of two latches (CML1 and CML2). If CML1 tracks then CML2 latches, and vice versa. As a result, the output of the DFF only changes at rising C+ clock transitions. In any other time the outputs are static. The same applies to the outputs of CML1 in the feedback

configuration. This type of frequency divider is called static frequency divider. The outputs of the two latches provide four phases at 0^0, 90^0, 180^0, and 270^0 of the divided reference clock. The output buffers are added to drive the 50ohm measurement equipment.

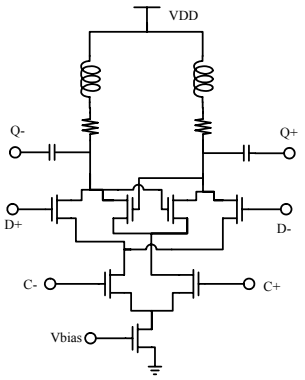


Fig. 4.36. Schematic of a CML latch.

The circuit schematic of the classical current mode logic (CML) latch is shown in Fig. 4.36. The latch circuit consists of two differential stages. Their current sources are controlled by the clock signals C+ and C-. If C- is high and C+ is low, the input signal D+ and D- appear amplified at the outputs Q+ and Q-. If the C- switches to low and C+ to high voltage levels, the input signals are turned off and then sensed by positive feedback. Resistive loads offer a lower parasitic capacitance than PMOS loads. The peaking inductors increase the bandwidth.

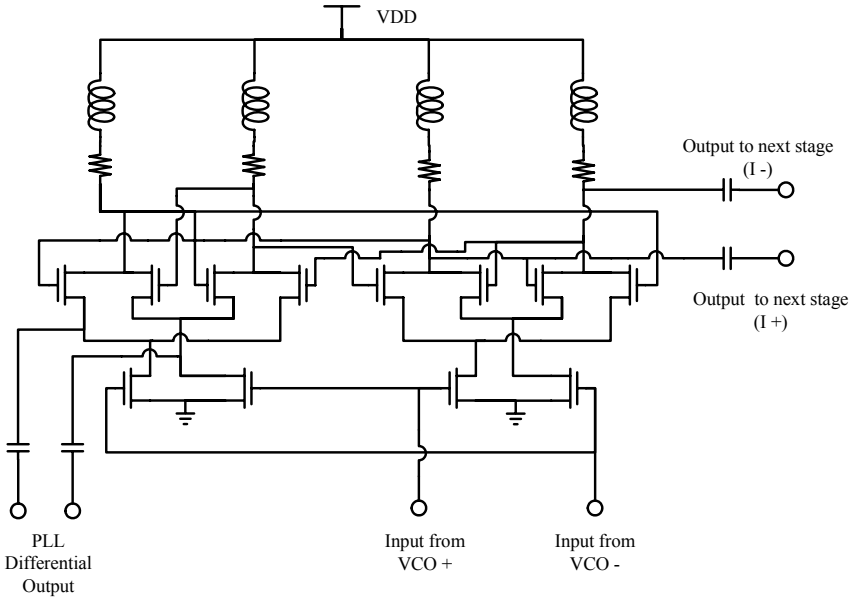


Fig. 4.37. Schematic of prescaler.

The prescaler is implemented by using static frequency divider which can provide quadrature outputs as shown in Fig. 4.37. The core divider circuit consists of two current-mode logic (CML) latches and consumes 2.88 mW from a 1.8V supply. The high division frequency is achieved by employing resistive loads, and inductive peaking in the latches. The presclaer as the first frequency divider in the PLL feedback can reduce the power consumption.

4.3.1.4 Divide-by-256 Divider

The block diagram of divider-by-256 is shown as Fig. 4.38 which is cascaded by one CML and seven TSPC circuits.

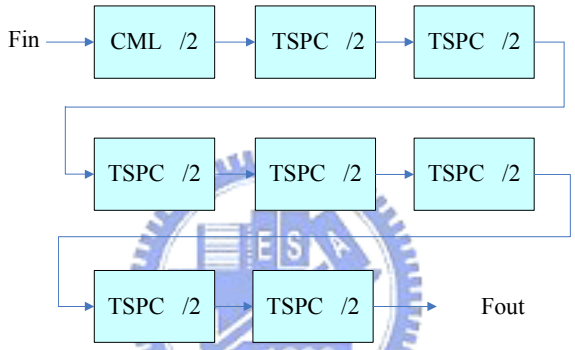


Fig. 4.38. Block diagram of divider-by-256.

The CML divider is using master-slave type as Fig. 4.39. Master-slave divider is differential input and then output four phase signals (0^o, 90^o, 180^o, 270^o). The purpose of divider-by-256 is to produce low frequency signal for compare with reference frequency to lock final frequency. Therefore, we choose the simplest circuit – True Single Phase Clock latches (TSPC). Fig. 4.40 shows the schematic of the improved TSPC. The modified TSPC only need one clock. The advantage is no need inverter clock and deduces circuit complexity. This circuit only needs 9 transistors. Compared to the SCL divider, TSPC has only nine transistors and the number of interconnections between them is highly reduced. Having each transistor a lower interconnection capacitance, the size can be close to the minimum value and than the power consumption is decreased.

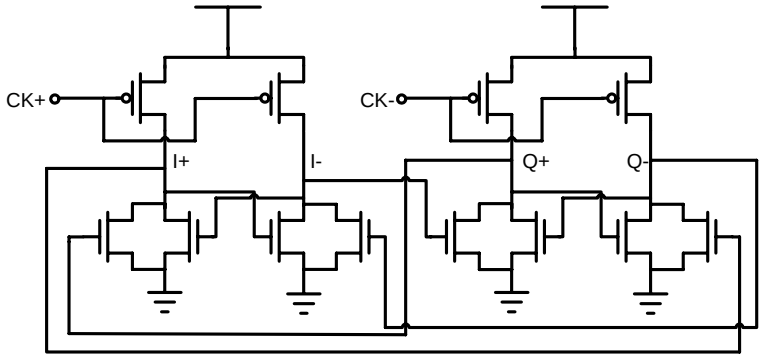


Fig. 4.39. Schematic of master-slave divider.

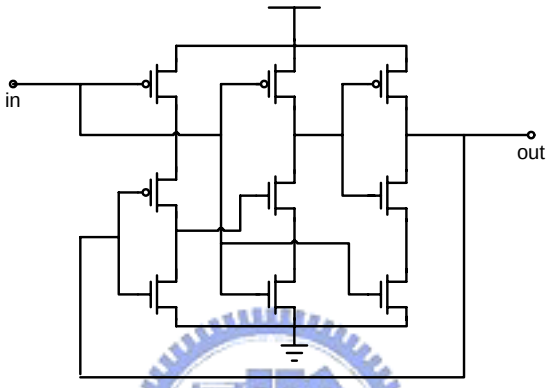


Fig. 4.40. Schematic of TSPC divider.

4.3.1.5 PFD

Phase detectors are a comparator which is providing an output signal whose DC component is proportional to the difference in phase between the two input signals. The simplest type of phase frequency detector (PFD) is shown as Fig. 4.41. The conventional PFD adopted DFF structure. The limitation of its maximum frequency operation and dead zone problem are the drawbacks. Due to the output load, the output signal of the PFD requires a period of time to change. If there is not enough to change the state of the output signals, the function of the PFD will not be accomplished. This phenomenon usually occurs when the phase difference of two input signals is so small that the output pulse width of AND gate is less than the needed rise time. This phenomenon is called dead zone. The dead zone influence locking time and locking status of overall PLL. Without careful design, the PFD will not work properly when the small input phase difference is applied.

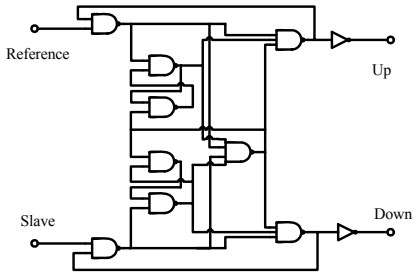


Fig. 4.41. Schematic of conventional PFD.

The designed PLL adopted precharge-type PFD shown as Fig. 4.42. The phase frequency detector compares the phase and frequency difference between the reference signal and the signal feedback by the frequency divider. Then PFD sends a signal UP or DOWN. The UP signal is high when the input reference signal is operating at a higher frequency than the VCO feedback signal. The charge pump forces current into the loop filter when the UP signal is high. This causes the VCO control voltage to rise. Then it increases the VCO frequency and brings the feedback signal to the same frequency as the reference signal. The DOWN signal is high when the input reference signal is operating at a lower frequency then the VCO feedback signal. The charge pump forces current out of the loop filter when the DOWN signal is high. This causes the VCO control voltage to fall. Then it decreases the VCO frequency and brings the feedback signal to the same frequency as the reference signal. Compare precharge-type PFD with conventional PFD, precharge-type PFD used less transistors and get smaller chip area. The precharge-type PFD not only reduce the dead zone problem and maximum frequency operation limitation but also lower chip size.

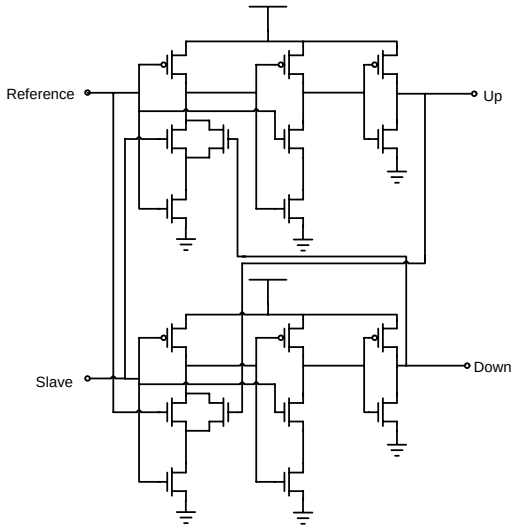


Fig. 4.42. Schematic of precharge-type PFD.

4.3.1.6 Charge Pump

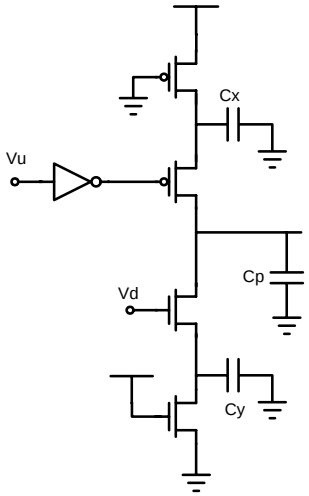


Fig. 4.43. Schematic of conventional CP.

A charge pump (CP) consists of two switched current source that charge into or out of the loop filter according to two logical inputs. Fig. 4.43 illustrates a conventional charge pump driven by a PFD and driving a capacitor. If the divider output is lagging the input of reference. CP activates the top current source. If the divider output is ahead, the bottom current source is activated and then drawing charge from the capacitor. The conventional charge pump has two disadvantages. First is the mismatch of UP and DOWN current source. Second is the charge sharing effect.

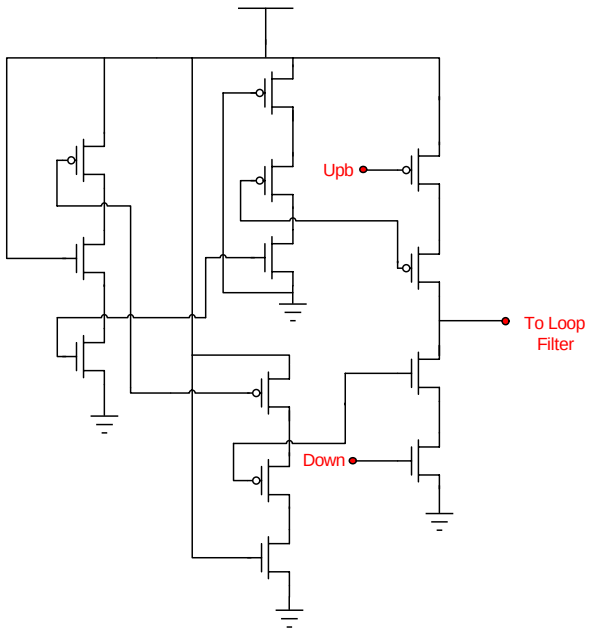


Fig. 4.44. Schematic of modified CP.

The designed PLL adopted CP shown as Fig. 4.44. CP activates the current source according to two logical inputs from PFD. Upb means UP followed by an inverter. This modified CP adopted switch on source. This can reduce charge sharing effect.

4.3.1.7 Loop filter

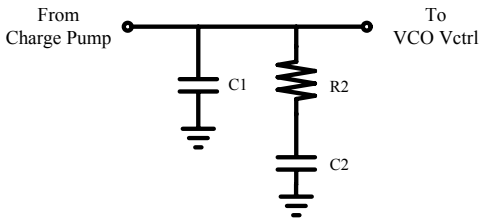


Fig. 4.45. Schematic of second order loop filter.

In designed PLL, we use a second order loop filter to reduce the ripple. The standard passive loop filter configuration for a current mode charge pump PLL is shown in Fig. 4.45. The PFD's current source outputs UP or DOWN into charge pump and then into the loop filter. Then LF converts the charge into the VCO's control voltage. The shunt capacitor C1 is recommended to avoid discrete voltage steps at the control port of the VCO due to the instantaneous changes in the charge pump current output. The impedance of the second order filter in Fig. 4.45 is

$$Z(s)=\frac{s(C_2R_2)+1}{s^2(C_1C_2R_2)+s(C_1+C_2)} \tag{4.7}$$

4.3.2 Simulated Results

4.3.2.1 Lower Power VCO

Fig. 4.46 shows the VCO output spectrum at 24GHz when control voltage is 0.49V. Fig. 4.47 shows the phase noise performance for a carrier frequency of 24GHz. Phase noise at 1MHz offset from the carrier is -102.3 dBc/Hz. Fig. 4.48 shows the transient response of the VCO differential output. The single ended output amplitude

is 450mV, which translates into 3.1dBm output power. The tuning range is 4.13GHz as shown in Fig. 4.49. The output power variation is 2.2dB as shown in Fig. 4.50. Table 4.5 summarizes the VCO performance of simulated results.

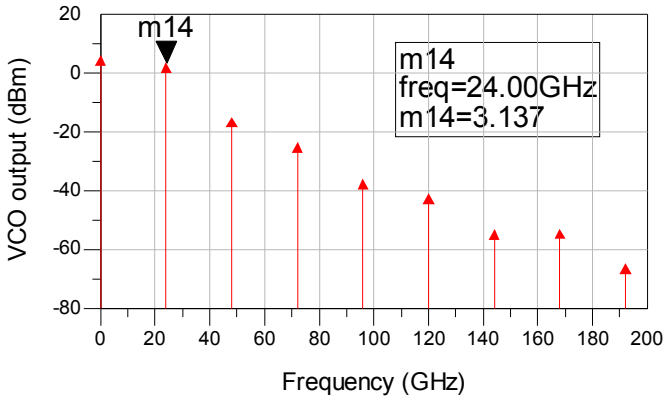


Fig. 4.46. Output spectrum at 24GHz.

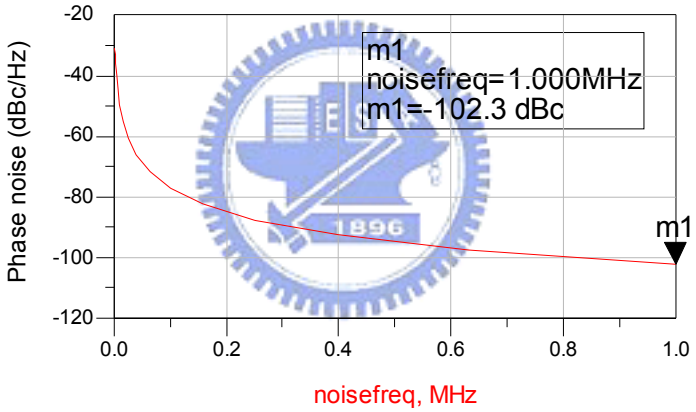


Fig. 4.47. Phase noise of the VCO at 24GHz.

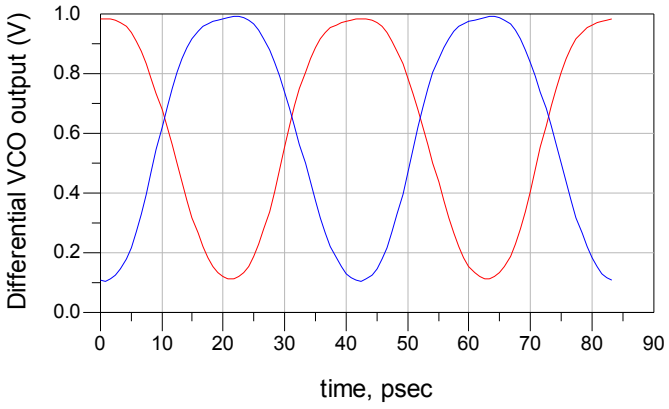


Fig. 4.48. Transient response of the VCO.

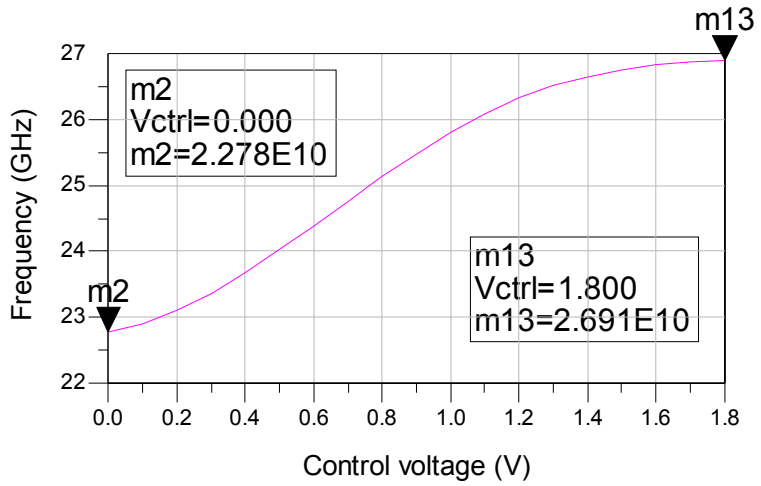


Fig. 4.49. Control voltage versus output frequency.

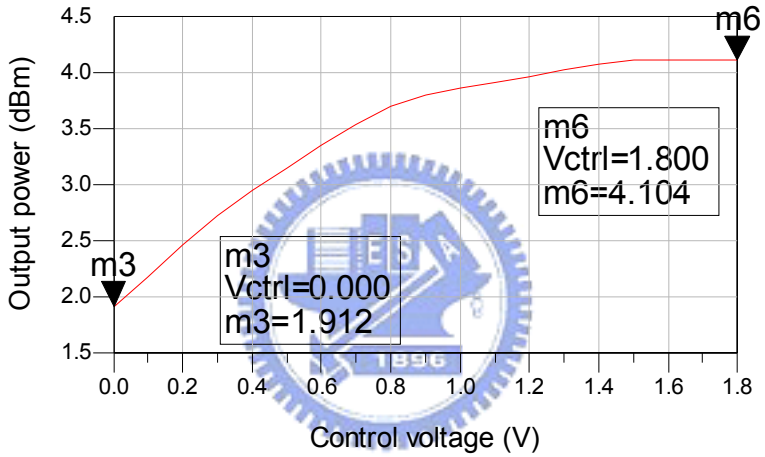


Fig. 4.50. Control voltage versus output power.

Parameters	VCO at VDD = 0.6 V (CornerCase=TT，Temperature=25°)
Frequency (GHz)	24
Core Current (mA)	1.34
Tuning Range (GHz)	22.78 ～ 26.91
Vtune (V)	0 ～ 1.8
Output Power (dBm)	3.1
Phase Noise @1MHz offset (dBc/Hz)	-102.3
Power Consumption (mW)	0.8
FOM (dBc/Hz)	-191

Table 4.5 Summary of simulation results

The comparison of the proposed VCO against recently reported high frequency CMOS VCOs (Frequency > 20GHz) is shown in Table 4.6. The FOM of proposed VCO is -191. It's better than recently reported CMOS VCOs.

PERFORMANCE OF REPORTED HIGH FREQUENCY CMOS VCOs (Frequency > 20 GHz)

Ref.	Technology	fosc [GHz]	Tuning range [GHz]	Output power [dBm]	Phase Noise [dBc/Hz]	Offset frequency	Supply voltage [V]	Power dissipation [mW]	FOM [dBc/Hz]
[56]	0.18um CMOS	25.1	3	-18.8	-100	1MHz	2.2	11	-177
[56]	0.18um CMOS	21.6	1.6	-4.2	-102	1MHz	3	45	-172
[57]	0.25um CMOS	19.4	5	-20.4	-101	1MHz	4.5	9	-177
This work	0.18um CMOS	24	4.2	-10.5	-104.4	1MHz	0.6	0.8	-191

Table 4.6 Summary of the comparison

4.3.2.2 Divide-by-2 Prescaler

Fig. 4.51 shows the spectrum after prescaler. Output frequency is 12 GHz and power is 1.5 dBm.

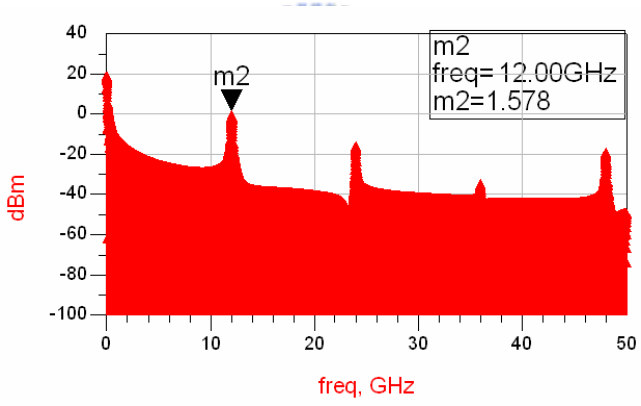
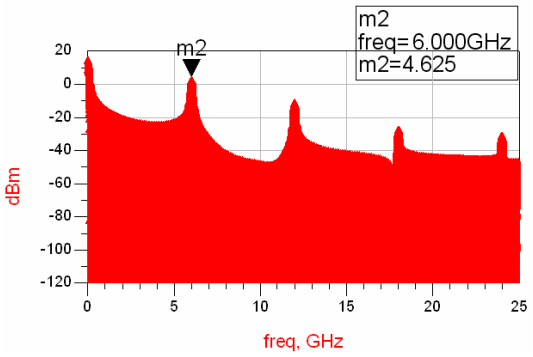


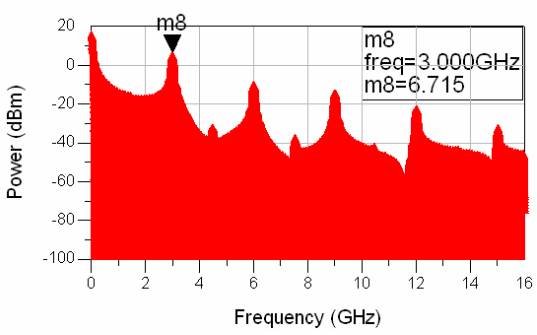
Fig. 4.51. Spectrum after prescaler.

4.3.2.3 Divide-by-256 Divider

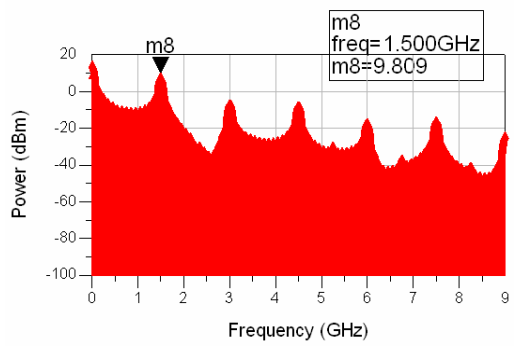
Fig. 4.52 shows the spectrum after each divider.



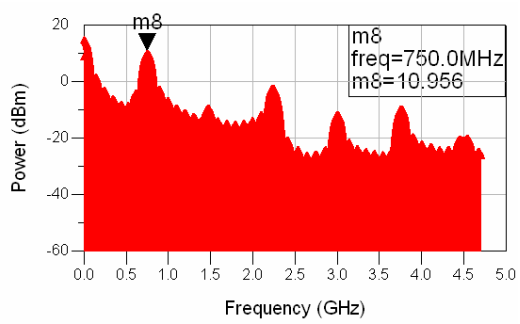
(a) 6 GHz



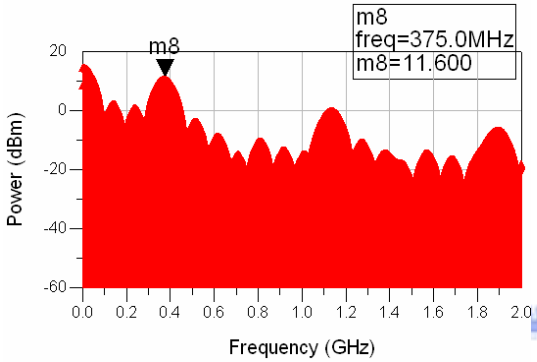
(b) 3 GHz



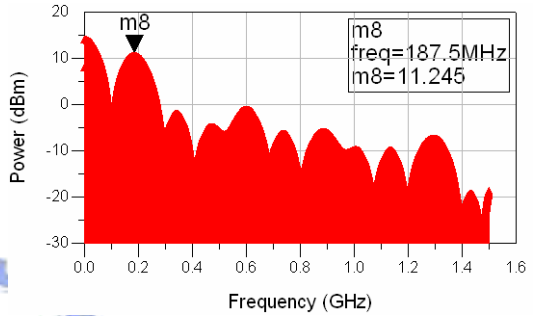
(c) 1.5 GHz



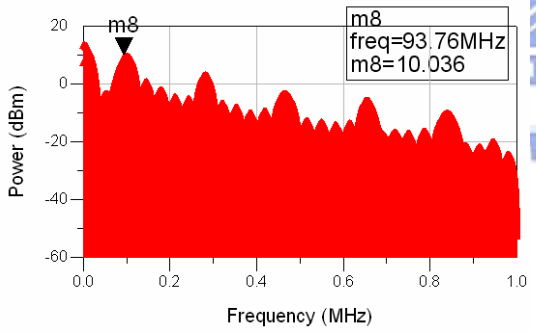
(d) 750 MHz



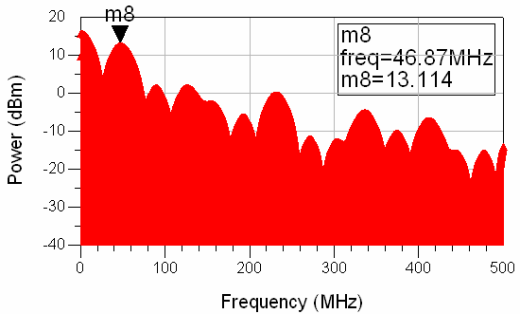
(e) 375 MHz



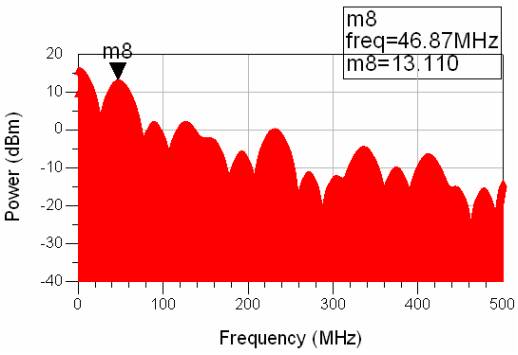
(f) 187.5 MHz



(g) 93.75 MHz



(h) 46.875 MHz



(h) Reference frequency: 46.875 MHz.

Fig. 4.52. Spectrum after each divider.

4.3.2.4 PLL Close-Loop Simulation

Because the PLL close-loop simulation with ADS takes a lot of time, we use MATLAB to verify and simulate the close loop firstly. A behavior model for the complete PLL is implemented in SIMULINK as shown in Fig. 4.53. Parameters we used are KVCO, resistance and capacitances of loop filter, current of charge pump, division ratio, and reference frequency. The lock time is about 3 us as show in Fig. 4.54. Fig. 4.55 shows the frequency settling to 24 GHz.

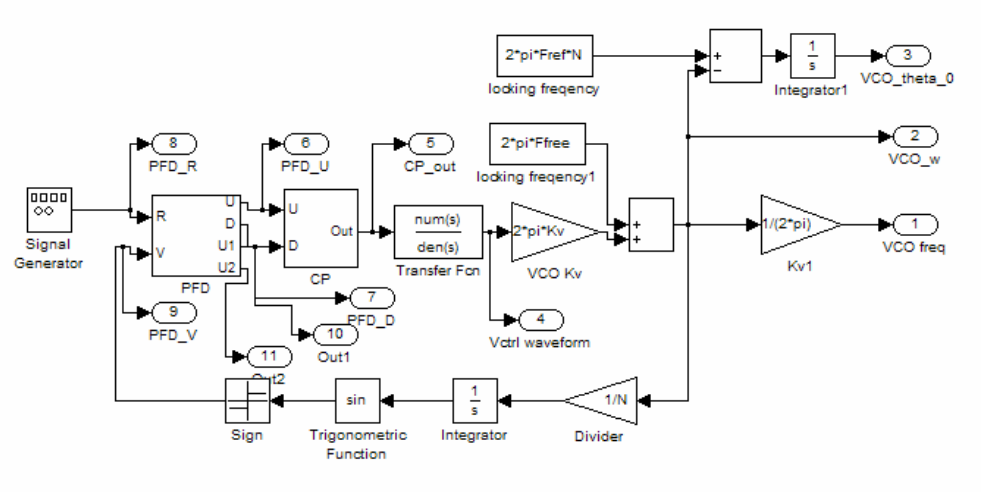


Fig. 4.53. The SIMULINK model for PLL architecture simulation.

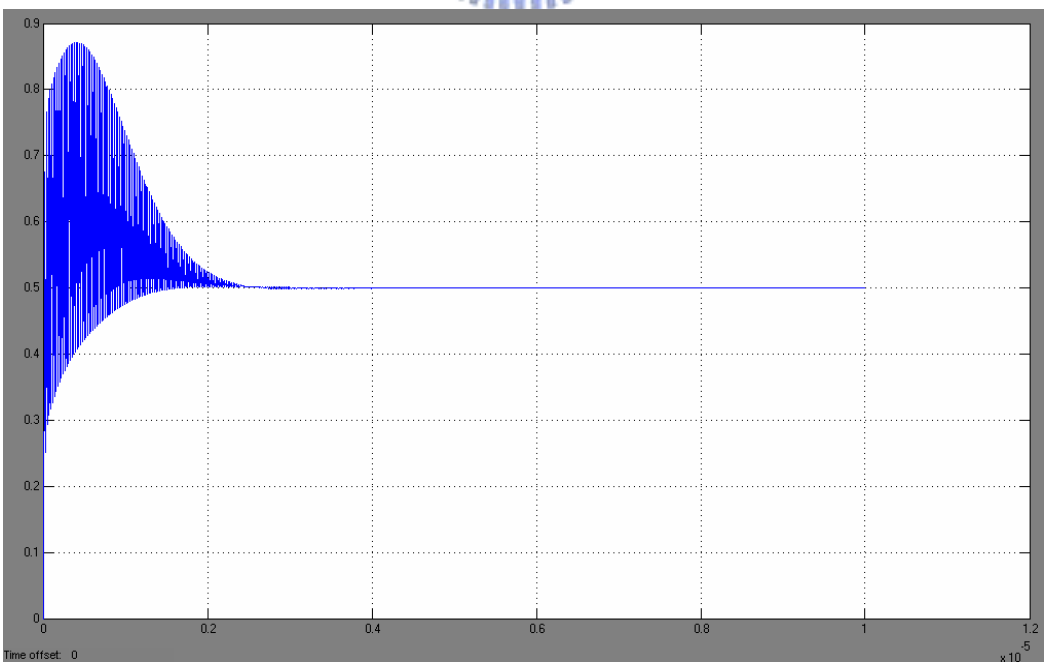


Fig. 4.54. Lock time simulation by Matlab SIMULINK.

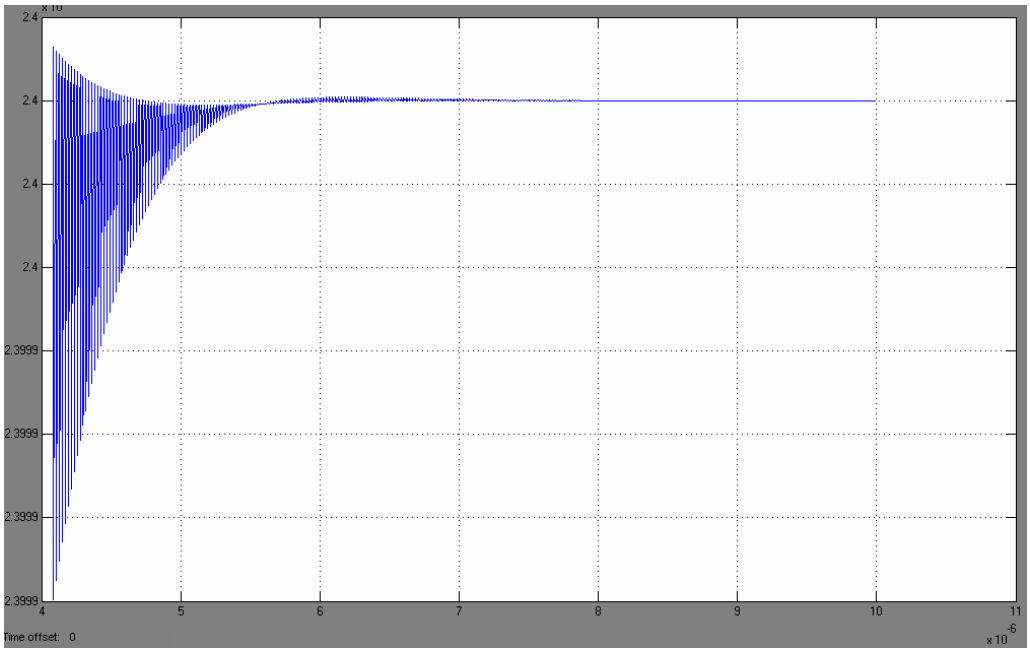


Fig. 4.55. Frequency settling time simulation by Matlab SIMULINK.

Then, we use the Advance Design System (ADS) to simulate the overall system. Fig. 4.56 shows the PLL output1 impedance matching at 24 GHz that return loss is -18 dB. Fig. 4.57 shows the PLL output spectrum, the power is -12 dBm at 24 GHz. Simulation result of lock time from free running frequency to 24GHz is shown in Fig. 4.58. The lock time is about 2us. Fig. 4.59 shows the variation of Vcontrol when Vcontrol is achieve a steady state. The variation is 11mV from 485mV to 496mV.

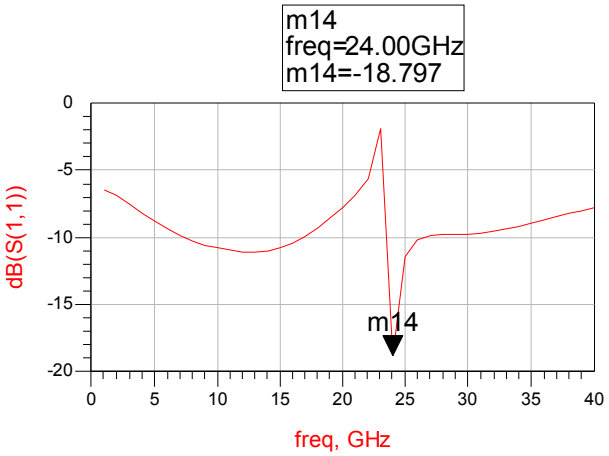


Fig. 4.56. PLL output1 return loss.

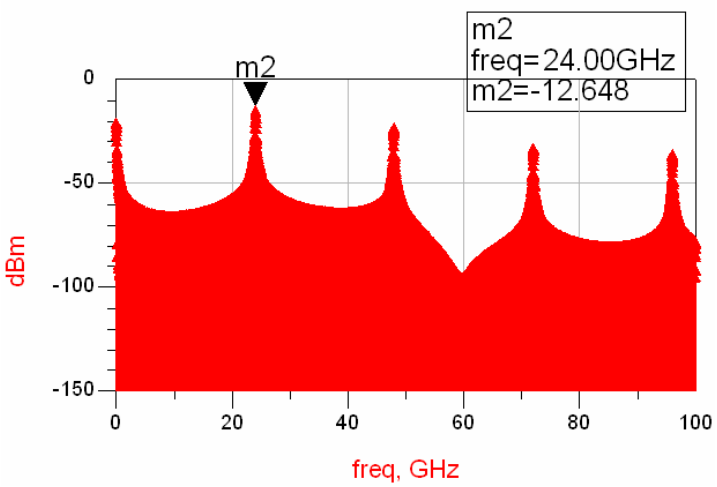


Fig. 4.57. Spectrum of the PLL's output as locking.

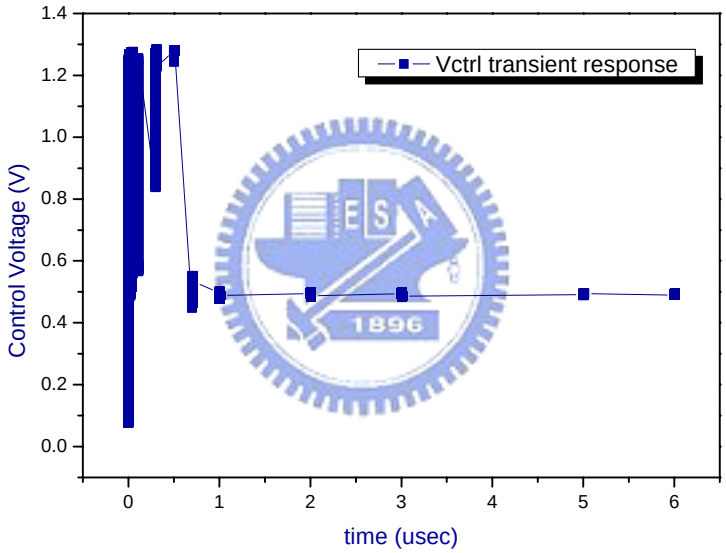


Fig. 4.58. Transistor level simulation of lock time.

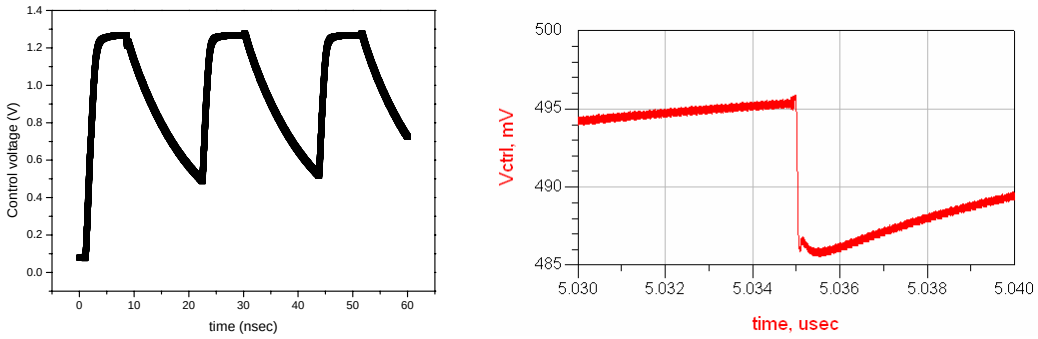


Fig. 4.59. Initial and steady state of control voltage.

4.3.2.5 Layout

After simulation by using ADS and ADS momentum. We use TSMC 0.18um RF model to implement this work. Fig. 4.60 shows the layout of 24 GHz PLL.

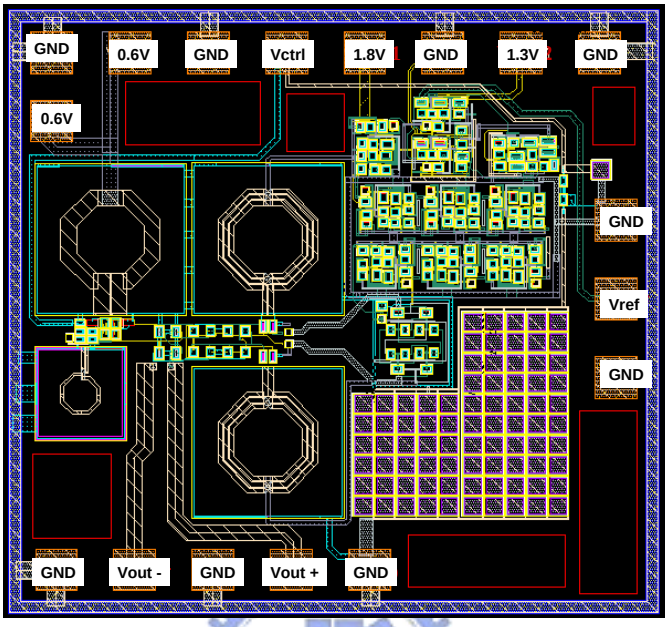


Fig. 4.60. The layout of 24 GHz PLL.

4.3.3 Summary

Parameter	Simulation Result	
Technology	TSMC 0.18μm CMOS	
Reference frequency	46.875 MHz	
Output frequency	24 GHz	
PLL output power	-12 dBm	
Divider ratio	512	
VCO Phase Noise @1MHz (dBc/Hz)	-102	
Lock time from free running	SIMULINK 3us ADS 2us	
Die area (mm^2)	1.25X1.15	
Power Comsumption (mW)	VCO	0.8
	Divider	24.5
	PFD&CP	1.26
	total	26.55

Table 4.7 Summary of simulation results.

This section presents the design and the simulation of a 24 GHz fully integrated PLL. Table 4.7 shows the summary of simulation results. The simulation results present total power consumption is 26.55mW. The power consumption of the VCO is only 0.8mW and PFD&CP is 1.26mW. The power consumption of the divider is 24.5mW. VCO supplied by 0.6V, divider supplied by 1.8V, and PFD&CP supplied by 1.3V. The PLL simulated frequency range is from 22.78 to 26.91 GHz with a power dissipation of 26 mW, while exhibiting a phase noise of -102 dBc/Hz at 1 MHz offset from the carrier. The gain of VCO is 2.3GHz/V. The complete 24GHz PLL is fabricated in TSMC 0.18μm CMOS process.

Chapter 5 *Conclusion*

In this thesis, we present mixers, 24GHz VCOs, and PLL. These proposed circuits are fabricated using a standard TSMC 0.18μm CMOS process.

In chapter 3, two kinds of wideband down conversion mixers for ultra-wideband applications and one kind of single-sideband mixer for UWB synthesizer are presented. The bandwidth of the first wideband down conversion mixer is from 2.4 to 10.7 GHz. This mixer uses a LC folded cascode structure and a feedforward compensated high-linearity differential transconductor. The LC folded cascode method is used to get enough voltage headroom to work with, and the modified feedforward compensated differential transconductor is adopted to achieve broadband impedance matching and lower the overall distortion. The measured results reveal that the proposed mixer achieves power conversion gain of 3.3 ± 1.5 dB, IIP3 of 6.9 dBm, and P-1dB of -2.8 dBm in the power consumption of 14.4mW from a 1.8V power supply. The chip area is 0.70 × 0.58 mm^2. The bandwidth of the second wideband mixer is designed from 2 to 11.5 GHz. This mixer adopting LC folded cascode mixer topology, modified feedforward compensated differential transconductor, and broadband active balun. The adoption of broadband active balun in the second wideband mixer allows providing balance signals for mixer core from single input. The measured results reveal that the proposed mixer achieves power conversion gain

of 6.9± 1.5 dB, IIP3 of 6.5 dBm, and P-1dB of -3.5 dBm in the power consumption of 25.7mW from a 1.8V power supply. The chip area is 0.85 × 0.57 mm^2. These two mixers are suitable in the receiver front end of ultra-wideband system. Finally, the single-sideband mixer using CMOS TSMC 0.18um is presented. This circuit is designed for UWB synthesizer. We use the SSB mixer architecture to suppress the unwanted sideband. The negative gain block is used to select upper side band or lower side band.

In chapter 4, two kinds of 24 GHz VCO and one kind of 24 GHz PLL for collision avoidance radar system are presented. The first VCO adopted current-reuse topology by stacking switching transistors in series like a cascode. The current-reuse VCO can operate with only half the amount of dc current compared to those of the conventional VCO topology. A tail filtering inductor was used at the source node of the NMOS to improve phase noise. The second harmonic LC tank is used to suppress the second harmonic as well as leaking from the LC tank across the oscillation. These two techniques can improve phase noise about 10dB totally at the carrier frequency of 24GHz. The simulation result shows the achieved phase noise of -111.3 dBc/Hz at 1-MHz offset while the VCO core draws 5.5mA from a 1.8V supply. The tuning range is from 23.32GHz to 24.92GHz. The size of the layout is 1.03mm by 0.93mm including pads. The second VCO adopted current reused topology and tail filtering inductor. The T-structure is used to suppress harmonics. The simulation result shows the achieved phase noise of -111.6 dBc/Hz at 1-MHz offset while the VCO core draws 5.5mA from a 1.8V supply. The tuning range is from 23.32GHz to 24.782GHz. The size of the layout is 0.90mm by 0.93mm including pads. Finally, a 24 GHz fully integrated PLL is designed. The simulation results present that the power consumption of the VCO is only 0.8mW and PFD&CP is 1.26mW. The power consumption of the divider is 24.5mW, which is the dominated part in PLL. VCO supplied by 0.6V, divider supplied by 1.8V, and PFD&CP supplied by 1.3V. The simulated tuning range of VCO is from 22.78 to 26.91 GHz, while exhibiting a phase noise of -102 dBc/Hz at 1-MHz offset from the carrier. The gain of VCO is 2.3GHz/V. The output power of PLL is -12dBm and lock time is about 2us with a power dissipation of 26 mW.

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