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新穎高介電常數材料與奈米微晶粒非揮發性記憶體之研究

Study on Novel Nonvolatile Memory with High-k Dielectric Materials and Nanocrystals

研 究 生 ：林 育 賢
指導教授 ：雷 添 福
簡 昭 欣

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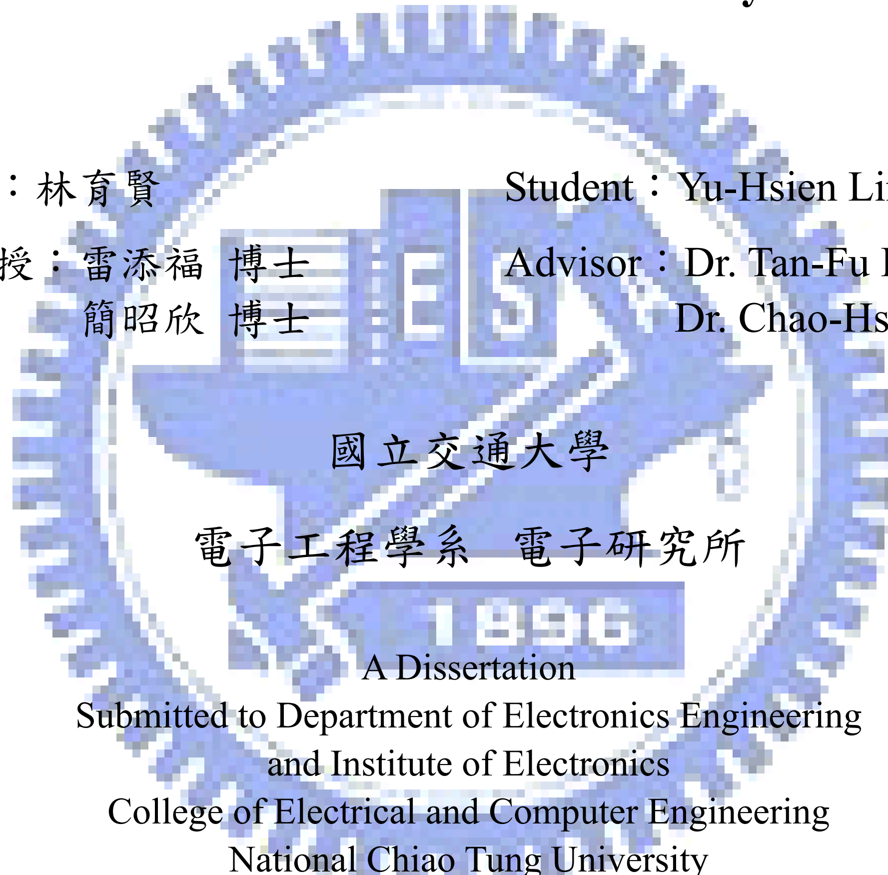

研究生：林育賢　　Student：Yu-Hsien Lin

指導教授：雷添福 博士　　Advisor：Dr. Tan-Fu Lei

簡昭欣 博士　　Dr. Chao-Hsin Chien

國立交通大學

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非揮發性記憶體之研究

學生：林 育 賢　　　　指導教授：雷 添 福 博士

簡 昭 欣 博士

國立交通大學

電子工程學系 電子研究所博士班

摘　要

此論文製作許多不同的非揮發性快閃記憶體，將使用數種材料、不同的製程方法及結構來製備捕陷電荷層，來取代現今傳統氮化矽 (Si_3N_4) 材料。再用不同的寫入/抹除的操作方式，在低電壓下來操作快閃記憶體。以達成電荷捕捉效率佳、有快速的寫入/抹除速度、大的記憶窗口、儲存資料持久性、以及寫入、清除操作造成的性能退化少的非揮發性快閃記憶體。

首先，我們利用氧化鉿 (HfO_2) 奈米微晶粒作為捕陷電荷層來製作新穎的SONOS型非揮發性快閃記憶體。此氧化鉿奈米微晶粒快閃記憶體在一萬次的寫入/抹除下，還是擁有好的儲存資料持久性、以及寫入、清除操作造成的性能退化少。其電荷儲存方式可以很區域性，使其一個單元儲存2個位元，並具有高密度之優點，可用於相關記憶體及半導體產業中。

再者，利用氧化鉿 (HfO_2)薄膜作為捕陷電荷層隨著後處理溫度的不同來製作 SONOS 型非揮發性快閃記憶體。我們發現到隨著退火的溫度愈高，記憶窗口愈大而儲存資料持久性愈差且寫入、清除操作造成的性能退化變多了。此為高溫

下結晶額外產生的淺能量的捕陷電荷所造成。之後我們也討論了溫度變化，以及其記憶體在一般操作時和其旁元件的電性影響。

接著，我們使用三種高介電常數材料成功的製作出了 SONOS 型非揮發性快閃記憶體於低溫多晶矽薄膜電晶體上，材料包含氧化鉿，氧化鉿矽化物以及氧化鋯矽化物。我們在其低溫製程中，達成電荷捕捉效率佳、有快速的寫入/抹除速度、大的記憶窗口、儲存資料持久性、以及寫入、清除操作造成的性能退化少的非揮發性快閃記憶體。而且，我們也成功的設計一個單元儲存 2 個位元的記憶體操作。

在論文的最後，我們製作出五十奈米的氧化鉿 (HfO_2) 奈米微晶粒記憶體在 SOI 的晶片上。此可以完全和現今 CMOS 的製程互相配合，來製作電荷非常有區域性的記憶體。如此一來，我們可以把現今的非揮發性快閃記憶體來縮小到七十個奈米以下，在次世代的小線寬記憶體的應用上將會完善。

Study on novel nonvolatile memory with high-k dielectric materials and nanocrystal

Student: Yu-Hsien Lin

Advisor: Dr. Tan-Fu Lei
Dr. Chao-Hsin Chien

Department of Electronics Engineering &
Institute of Electronics
National Chiao Tung University

ABSTRACT

In this thesis, we design various nonvolatile memory with a high-k charge-trapping layer and nanocrystals. This high-k layer replaces the silicon nitride layer in the SONOS structure. Different program/erase methods are also proposed for low power applications. This nonvolatile memory structure will have superior characteristics in terms of considerably large memory window, high speed program/erase, long retention time, and excellent endurance.

First, we present a novel nonvolatile SONOS-type flash memory that was fabricated using hafnium oxide (HfO_2) nanocrystals as the trapping storage layer. These HfO_2 nanocrystal memories exhibit excellent data retention, endurance, and

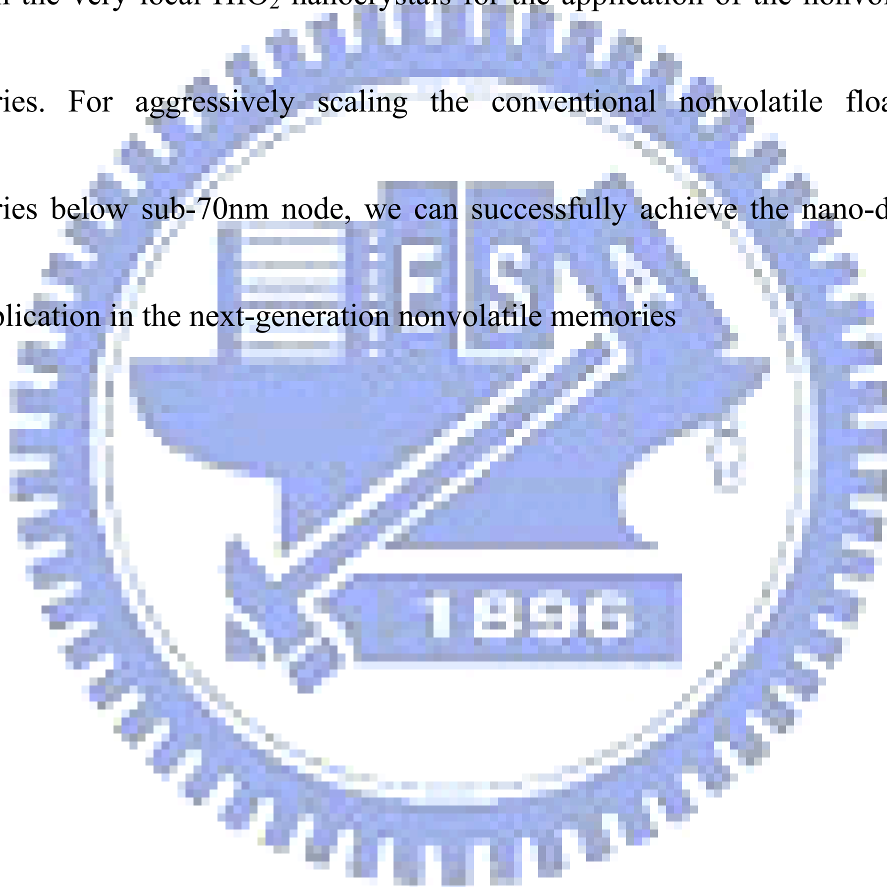
good reliability, even for the cells subjected to 10k P/E cycles. These features suggest that such cells are very useful for high-density two-bit nonvolatile flash memory applications.

Then, we demonstrate the effect of the post-deposition annealing for the HfO_2 trapping layer on the performance of the SONOS-type flash memories. It was found that the memory window becomes larger while the retention and endurance characteristics get worse as the annealing temperature increases. This was ascribed to the larger amount and the shallower energy levels of the crystallization-induced traps as compared to the traps presented in the as-fabricated HfO_2 film. Finally, in the aspect of disturbances, we show only insignificant read, drain and gate disturbances presented in the three samples in the normal operation.

Next, we have successfully fabricated SONOS-type poly-Si-TFT memories employing three kinds of high-k dielectrics, including HfO_2, Hf-silicate and Zr-silicate, as the trapping layer with low-thermal budget processing. It was demonstrated that the fabricated memories exhibit good performance in terms of relatively large memory window, high program/erase speed (1ms/10ms), long

retention time (>10^6s for 20% charge loss) and negligible read/write disturbances. In particular, 2-bit operation has been successfully demonstrated.

Finally, we demonstrate 50nm nonvolatile HfO_2 nanocrystal memory on SOI wafer. With this technique, which is fully compatible to current CMOS technologies, to form the very local HfO_2 nanocrystals for the application of the nonvolatile flash memories. For aggressively scaling the conventional nonvolatile floating gate memories below sub-70nm node, we can successfully achieve the nano-devices for the application in the next-generation nonvolatile memories



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最後，謝謝我的家人與我可愛的女友，感謝你們在我心情低落時給我打氣，在我需要溫暖時給我照顧，謝謝你們陪我一路走過這漫長的求學生涯。僅此論文獻給所有關心我的朋友。

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Fig. 6.8 Drain disturbance characteristics of the La_2O_3 SONOS-type memory. After 1000 s at 25 °C, only a 1V drain disturb margin was observed.

Fig. 6.9 Gate disturbance characteristics of the La_2O_3 SONOS-type memory. A threshold voltage shift of only 1 V occurred after stressing at V_g = 10 V and $V_s = V_d = V_{sub}$ = 0 V for 1000 s.

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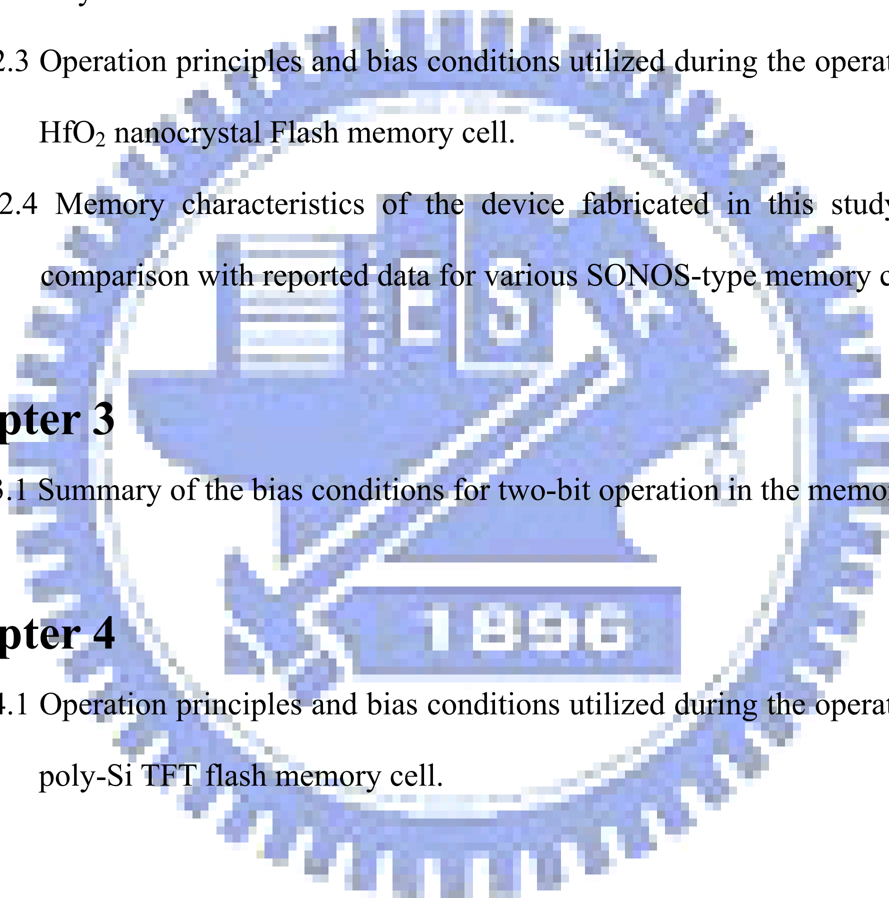

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Chapter 1

Introduction

1.1 Background

Recently, complementary metal-oxide-semiconductor (CMOS) memory technologies which driven by the more and more increasing demand for mobile capabilities, computer, and some electronic consumer products, have developed rapidly for the need in the people's livelihood.

Memories can be divided into two main categories by whether the storage data can be affected by the power supply. One is volatile memory, and the other is non-volatile memory. Volatile memory will lose stored information once the power supply is switched off. On the other hand, nonvolatile memory does not lose its data when the system or device is turned off, and offer low power and high storage density solutions to generic needs of data storage.

In 1967, *D. Kahng* and *S. M. Sze* invented the first floating-gate (FG) nonvolatile semiconductor memory at Bell Labs [1.1]. Recently, in order to improve the charge leakage and high power dissipation issues of volatile memory, the nonvolatile semiconductor memory devices play an important role in memory applications because of its low-voltage and low-power features for portable commercial devices. It stands out with its complementary metal oxide semiconductor (CMOS) compatibility and scalability to extremely high density. So far, the most widespread nonvolatile memory array is the so-called Flash memory, which has a byte-selectable programming operation combined with a sector erasing at the same time. In addition, as compared to the electrically programmable read-only memory (EPROM), and electrically erasable and programmable read-only memory (EEPROM), Flash memories have good flexibility of program/erase (P/E) operation, smaller area, and

low cost. The most well-known commercial Flash memory is Intel ETOX (EPROM Tunnel Oxide) structure (Figure 1.1(a)) [1.2]. The basic device is a Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSFET) with a modified gate stack structure that has a control gate (CG) and a floating gate (FG) embedded in a dielectric material such as silicon dioxide (SiO_2). The memory storage element is the isolated floating gate disconnected from terminal voltages between the control gate and the channel. Figure 1.1(b) shows the band diagram of programming and erasing operations. The ETOX is "written" when we programmed the electrons into the floating gate by Channel-Hot-Electron (CHE) programming then the threshold voltage (V_T) increases for the MOSFET. Otherwise, we erase the stored electrons and restoring V_T to its original value by Fowler-Nordheim (FN) tunneling or band to band hot hole (BTBTHH) injection from FG to source [1.3]. The V_T shift between the programmed and erased states is denoted by a quantity known as the "memory window." Figure 1.2 shows a typical current versus gate voltage characteristic of an erased ETOX device and its V_T shift when the device is programmed. The memory-state for the device can be determined by measuring the current in the MOSFET when a control gate bias is applied within the memory window.

Nevertheless, the ETOX cell has several main drawbacks. Firstly, the Flash memory needs thick tunnel oxide (8~11 nm) to provide superior retention and endurance characteristics, but it also causes higher operation voltage, slow P/E speed, and poor scalability issues. Secondly, because the polysilicon floating-gate is conductive, the total charges stored in the floating gate will be easily leaked directly through the tunnel oxide when the tunnel oxide is damaged during P/E cycles (Figure 1.3(a)). Third, scaling the ETOX cell below the 0.1 μm feature size will be difficult; the main problems are related to high field stressing and the leaky scaled-down oxide barrier during the P/E cycle. To circumvent these limitations mentioned above, new

memory-cell structures with discrete traps as the charge storage elements (figure1.3(b)), e.g. MNOS (Metal / Nitride / Oxide / Silicon) [1.4], SONOS (Silicon / Oxide / Nitride / Oxide / Silicon) [1.5-1.6], and nanocrystal memory [1.7-1.8], have been demonstrated as the promising candidates in the Flash memory application.

With the semiconductor technology continuously shrinks down to nano scale, the quality of ultra-thin tunnel oxide (<3nm) has been greatly improved. Therefore, nitride-related volume-distributed charge traps memories, such as metal nitride oxide silicon (MNOS) [1.4] and polysilicon oxide-nitride-oxide silicon (SONOS) [1.5-1.6], become more attractive in nonvolatile memory applications. However, for the MNOS devices, there have been shown an issue of charge leakage through the control gate. The top blocking oxide has to be introduced into the inter-layer between the control gate and the nitride layer, then the ONO (SiO_2-Si_3N_4-SiO_2) gate dielectric stack has been invent to improve the disadvantages. Therefore, the SONOS memory devices show greater retention and program/erase efficiency than MNOS counterparts. Figure 1.4 (a) illustrates the schematic of SONOS structure and the electron conduction paths. When the control gate is biased positively, electrons will tunnel from the channel through the SiO_2 into the nitride layer. On the other hand, when the control gate is biased negatively, the trapped electrons are ejected into the channel by tunneling process. However, for the stored electrons in nitride layer, some electron move toward the gate or the channel even though they are blocked by the top oxide or the tunnel oxide because the shallow trap level in the nitride layer [1.9]. The charge transport mechanisms involve FN-tunneling, direct tunneling and Frenkel-Poole emissions (Figure 1.4 (b)). (A Frenkel-Poole emission is the electric field-assisted and thermal excitation of trapped electrons in defects to the conduction band.) For the operation, SONOS devices can be written with less then 10 V in one micron-second. So far, SONOS memories have the huge market in the Flash memory application.

SONOS-type (poly-Si-oxide-nitride-oxide-silicon) Flash memories have recently attracted much attention for the application in the next-generation nonvolatile memories [1.10]. High-κ dielectric materials would be able to maintain an equivalent potential difference between the floating gate and the device body for a greater thickness compared to SiO_2. The leakage through the dielectric would be minimized and the scaling limits would be extended. Moreover, to achieve a memory window that can differentiate between stable program and erased states, using high-κ dielectric trapping layer can has sufficiently high node density for the memory. Using the high-k trapping layer exhibits many advantages, e. g., easy to fabricate, high program/erase speed, low programming voltage and power consumption, better potential for scalability below the 70-nm node, according to the International Technology Roadmap for Semiconductors (ITRS) [1.11]. Hafnium oxide (HfO_2) is considered to be a promising candidate for the charge trapping layer for the SONOS-type Flash memory instead of Si_3N_4 film [1.12]. The high-κ dielectric film, HfO_2, is expected to have better charge trapping characteristics than the conventional Si_3N_4 films for sufficient density of trap states and deep trap energy level to achieve longer retention time [1.13-1.14]. This feature makes HfO_2 be more helpful in scaling the tunnel oxide for enhancing the performance and more suitable for the development of the SONOS-type memory with multi-bit operation [1.15-1.16]. Unfortunately, many concerns still remain for this type of memories. For conventional SONOS memory, erase saturation and vertical stored charge migration [1.17-1.18] are two major drawbacks (Figure 1.5(a)(b)). So, nanocrystal memories have been invented because their very local charge storage.

Unlike volume-distributed charge traps memories, nanocrystals can be uniformly deposited as a two-dimensional (2-D) distribution on a thin tunnel oxide as illustrated in Figure 1.6(a). The nanocrystal can store the charge locally due to the well isolation

of nanocrystals from each other and effectively prevents formation of good conductive paths between the adjacent nodes (figure 1.6(b)). Generally, nanocrystals are small clusters of silicon atoms with size of 5 to 10 nm in diameter. By limiting nanocrystal deposition to just one layer and adjusting the thickness of top blocking oxide, charge leakages to the control gate from the storage nodes can be effectively prevented (figure 1.6(b)). In recent years, Si and Ge nanocrystals have been studied extensively. IBM researchers, *Tiwari et al.*, first proposed a Si nanocrystal nonvolatile memory with a granular floating gate in 1995 [1.7], and a higher P/E speed than Flash memory has been reported. In 1998, *King et al*. has published the Ge dot nanocrystal memory [1.8]. So far, Si and Ge nanocrystals can be fabricated by various techniques, including chemical vapor deposition [1.7][1.19], low energy ion implantation [1.20], annealing of silicon rich oxide [1.21], thermal oxidation of SiGe [1.22], and aerosol nanocrystal formation [1.23]. Moreover, *Lee et al.* has reported a new method to improve the memory characteristics of the Si nanocrystal memory devices by replacing the traditional SiO_2 with HfO_2 high-κ dielectrics [1.24]. In 2002, *Liu et al.* has proposed the self-assembled nanocrystal formation process and the design principles of the metal nanocrystal memories with Au, Ag, and Pt materials [1.25-1.26]. The nanocrystals are formed self-assembly by depositing an ultra-thin metal layer on the gate oxide and then annealing by rapid thermal annealing (RTA) system. In addition, the higher density of states, stronger coupling with the channel, better size scalability, and the design freedom of engineering the work function to optimize device characteristics are the advantages of metal nanocsrystals over their semiconductor counterparts.

Flash memories (SONOS memories, SONOS-like memories, and nanocrystal memory) have widest applications in nonvolatile memories due to their enhanced flexibility and higher effective speed and density. They provide single cell electrical

program and fast simultaneous block electrical erase. For combined with a fast in-system erase capability, these low-power and robust Flash systems are ideal for a myriad of portable applications such as cellular phones, pagers, digital cameras, digital voice recorders, personal data assistants to compact smart cards. They even may eventually replace the ubiquitous magnetic memory media and RAMs (Random Access Memories) in many compact electronic applications. As consumer electronics evolve towards ever-higher performance and multi-functionality, the System-On-Chip (SOC) concept for ultra-large scale integration (ULSI) of microelectronic devices is gaining momentum. This circuit-level integration concept broadly encompasses approaches where functionally distinct modules (e.g. digital logic, memory, analog components and signal processing) are intimately integrated on a single chip to increase system speed and capability. Since many of the device modules have very different material, thermal, and contamination process requirements, the search for compatible process recipes for these devices has major challenges.

1.2 Motivation

In this thesis, we have designed a high performance nonvolatile memory with HfO_2 nanocrystal charge-trapping layer and high-κ charge-trapping layer such as HfO_2 and La_2O_3. These high-κ layers replace the silicon nitride layer in the SONOS structure. Different program/erase methods are also proposed for low power applications. These nonvolatile memory structures will have superior characteristics in terms of considerably large memory window, high speed program/erase, long retention time, and excellent endurance.

High-κ dielectric materials, such as HfO_2, ZrO_2, La_2O_5, and Pr_2O_3, will be used to fabricate the charge-trapping layer. These materials provide high trapping state

densities and deep trapping levels, therefore they can enhance the retention of nonvolatile memories. The charge-trapping efficiency can be improved, and larger operation window can be achieved. The application of high-k materials can further reduce the operation voltage and potentially can help memory device scaling.

A novel nanocrystal charge-trapping layer can be fabricated by annealing high-κ silicate materials, such as $HfSi_xO_y$. After applying a rapid thermal anneal to the silicates, phase-separation happens. HfO_2 nanocrystals are formed and surrounded by SiO_2. With such a nanocrystal structure as the charge-trapping layer, the retention of nonvolatile memories can be further improved. The stored charges will be trapped in/around the nanocrystals and isolated by silicon dioxides. Less opportunity of charge loss is expected.

For the memory device operation, we use channel hot-electron injection for the programming and band-to-band hot-hole injection for the erase. Staying in oxide trapping states or high-k nanocrystals, the stored charges are separated at different trapping sites. A local defect of tunnel oxide won't cause a severe charge loss. Thus we can achieve 2 bits storage in one memory device by reversing source and drain. Using band-to-band hot-hole injection can alleviate the drawback of over-erase, which is a problem when FN-tunneling is utilized. We will study the influences of different program/erase operations on the reliability issues of nonvolatile memories.

Moreover, we also used three kinds of high-κ dielectrics, including HfO_2, Hf-silicate and Zr-silicate for the trapping layer of the poly-Si TFT memory. Polycrystalline silicon thin-film transistors (Poly-Si-TFT) have been widely used to integrate driver circuits for the application of AMLCD's [1.27]. The feasibility of integrating an entire system on top of the panel (SOP) is being actively pursued [1.28]. By employing low thermal cycle (600°C, 24hrs) for post high-κ deposition annealing and S/D activation, the proposed nonvolatile memory fabrication is fully compatible

with the current mass-production TFT processing. This makes the realization of producing the embedded nonvolatile memories on the panel becomes feasible.

The goal of this thesis is to find an optimized nonvolatile Flash memory in the application of congenital CMOS process and poly-Si-TFT process. By evaluating different materials and fabrication processes, we intend to find a replacement for silicon nitride as the charge-trapping layer. Therefore we can benefit from the low power operation and still maintain good reliabilities of nonvolatile memory devices. The high-k nanocrystals also has potential applications for CMOS and quantum devices.

1.3 Thesis Organization

We will propose a novel, simple, reproducible, and reliable technique for the design of high-density HfO_2 nanocrystal Flash memories through the spinodal decomposition of hafnium silicate in chapter 2. Then, in the chapter 3, we have investigated the effect of post-deposition annealing temperature on the performance of the resultant HfO_2 SONOS-type Flash memories. In the chapter 4, we have studied three kinds of high-k dielectrics, including HfO_2, Hf-silicate and Zr-silicate for the trapping layer of the low temperature poly-Si-TFT memory devices with two different thickness tunnel oxides. In chapter 5, 50nm nano scaled tri-gate HfO_2 nanocrystals Flash memories have been fabricated on SOI. In the chapter 6, we have investigated the La_2O_3 trapping layers for the SONOS-type Flash memories. Conclusions follow in chapter 7.

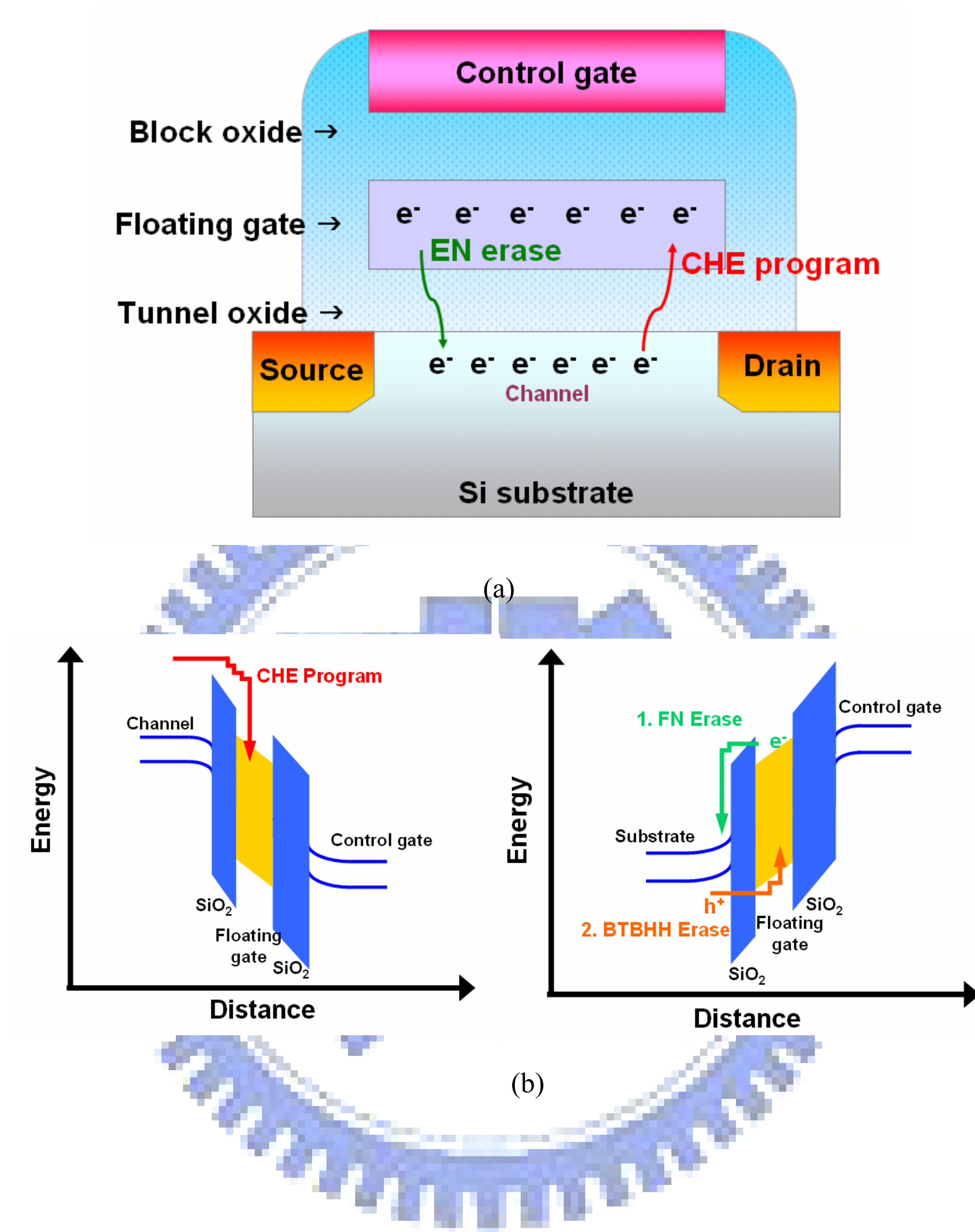


Fig. 1.1 (a)Schematic of a basic ETOX Flash memory device. (b) Electron flow (red arrows) during programming by CHE injection. Electron flow (green arrows) or hole flow (orange arrows) during erasing by FN tunneling or BTBTHH injection to the source. [1.2]

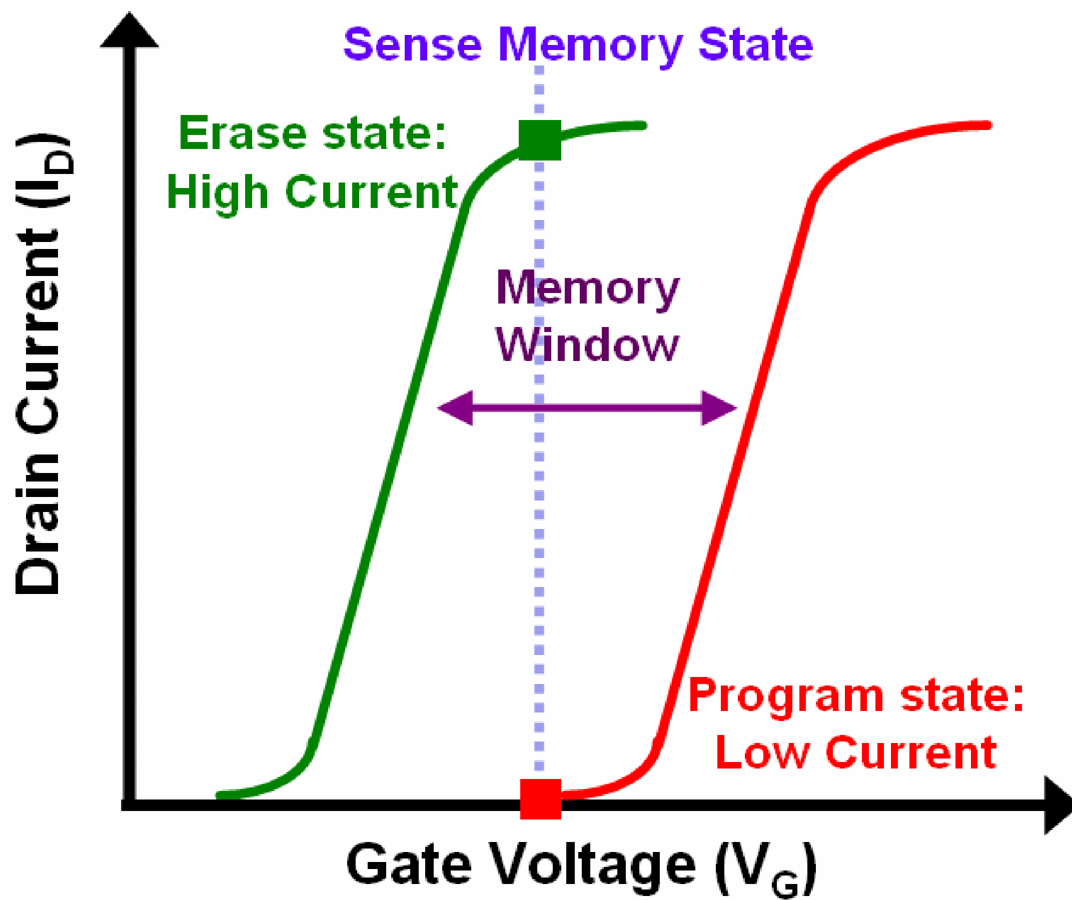
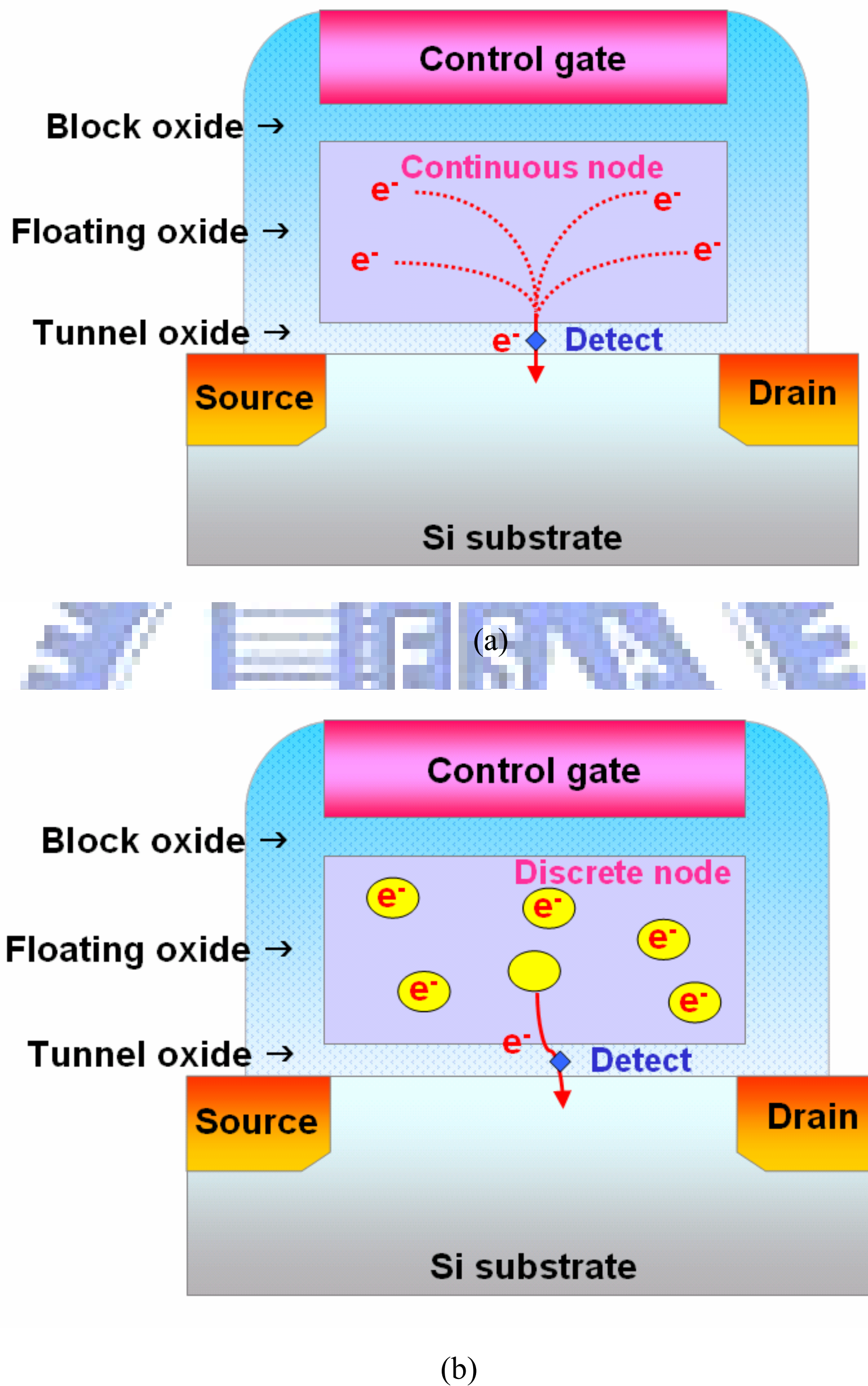
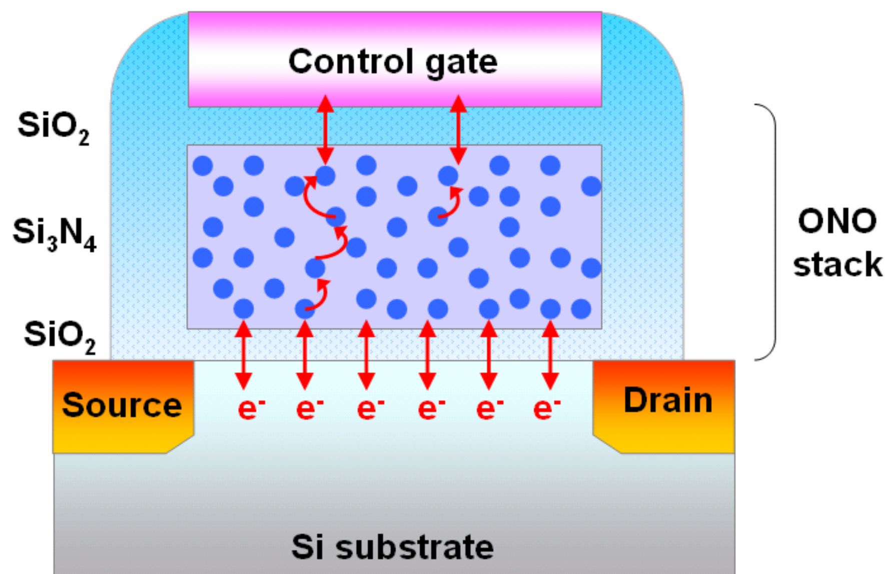


Fig. 1.2 Current-voltage characteristic of a memory device in the erased and programmed state, showing the VT shift and the memory window.

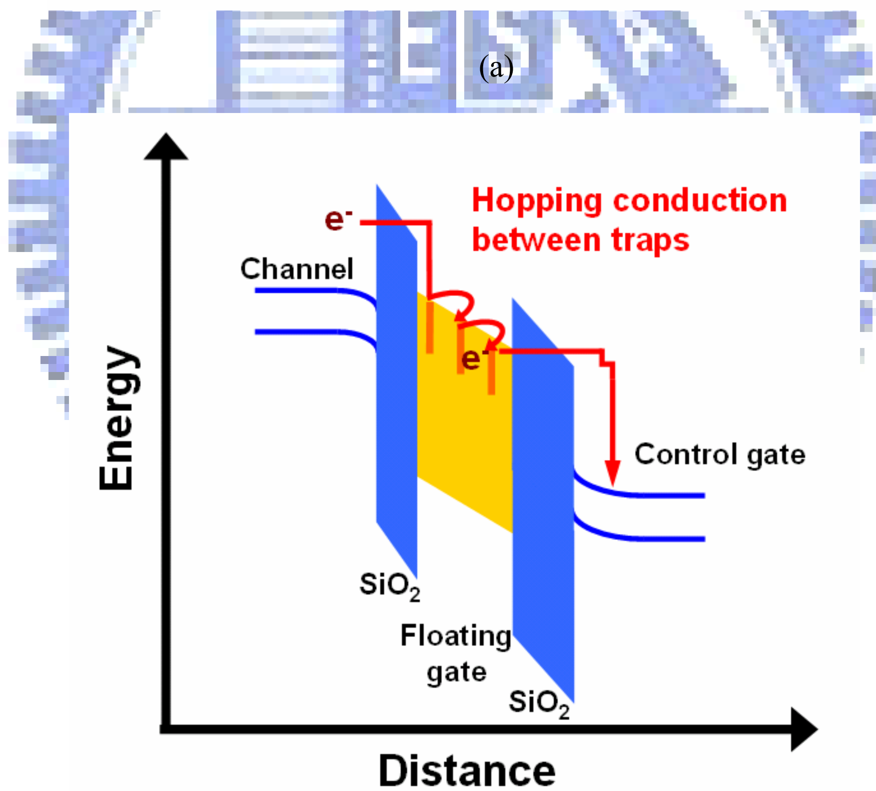


(b)

Fig. 1.3 (a) Charges in the dielectric stored in isolated storage nodes. (b) A schematic of a continuous FG structure with all the charges drained by an isolated defect in the dielectric.

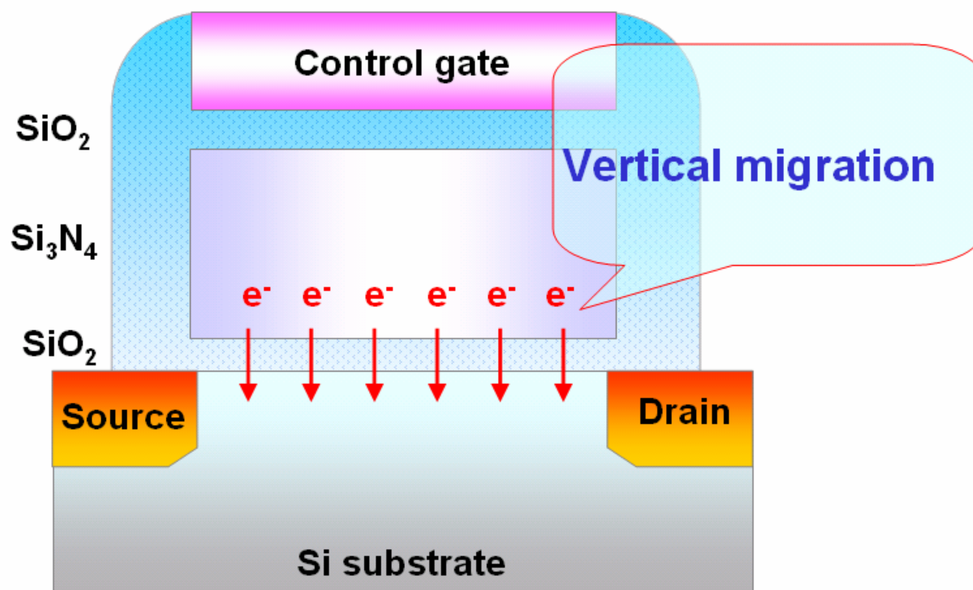


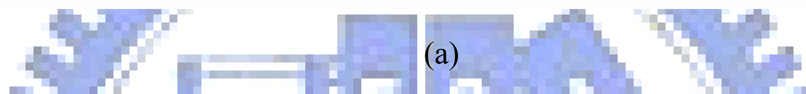
(a)



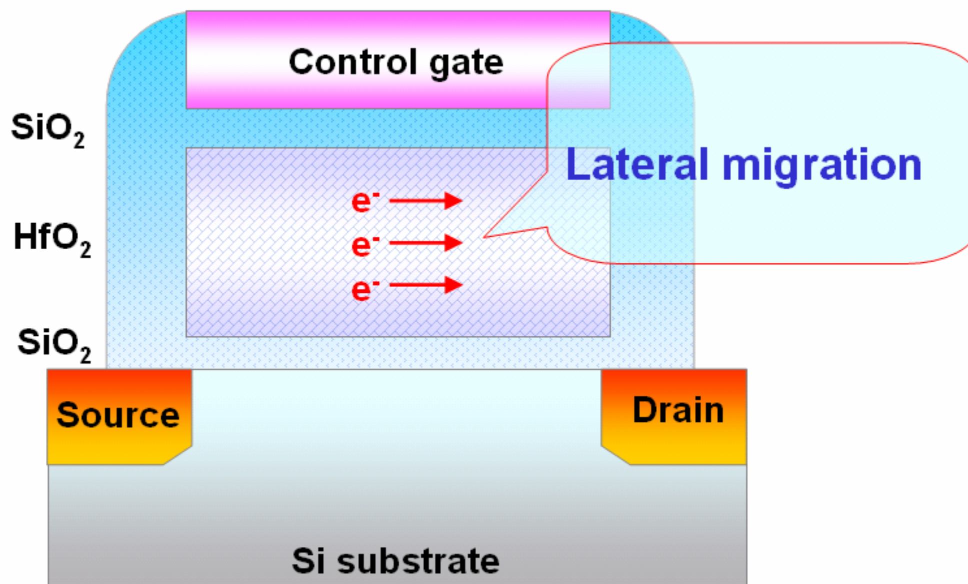
(b)

Fig. 1.4 (a) Basic SONOS memory device structure. Red arrows show paths of electron transport during memory operation. The electrons hop between trap. (b) Energy diagram illustrating the physical process of a typical SONOS program operation sites (blue dots) within the Si3N4 layer.





(a)



(b)

Fig. 1.5 (a) Vertical migration of the stored charge in the Si_3N_4 trapping layer in SONOS memory device structure. (b) Lateral migration of the stored charge in the HfO_2 trapping layer in SONOS memory device structure.

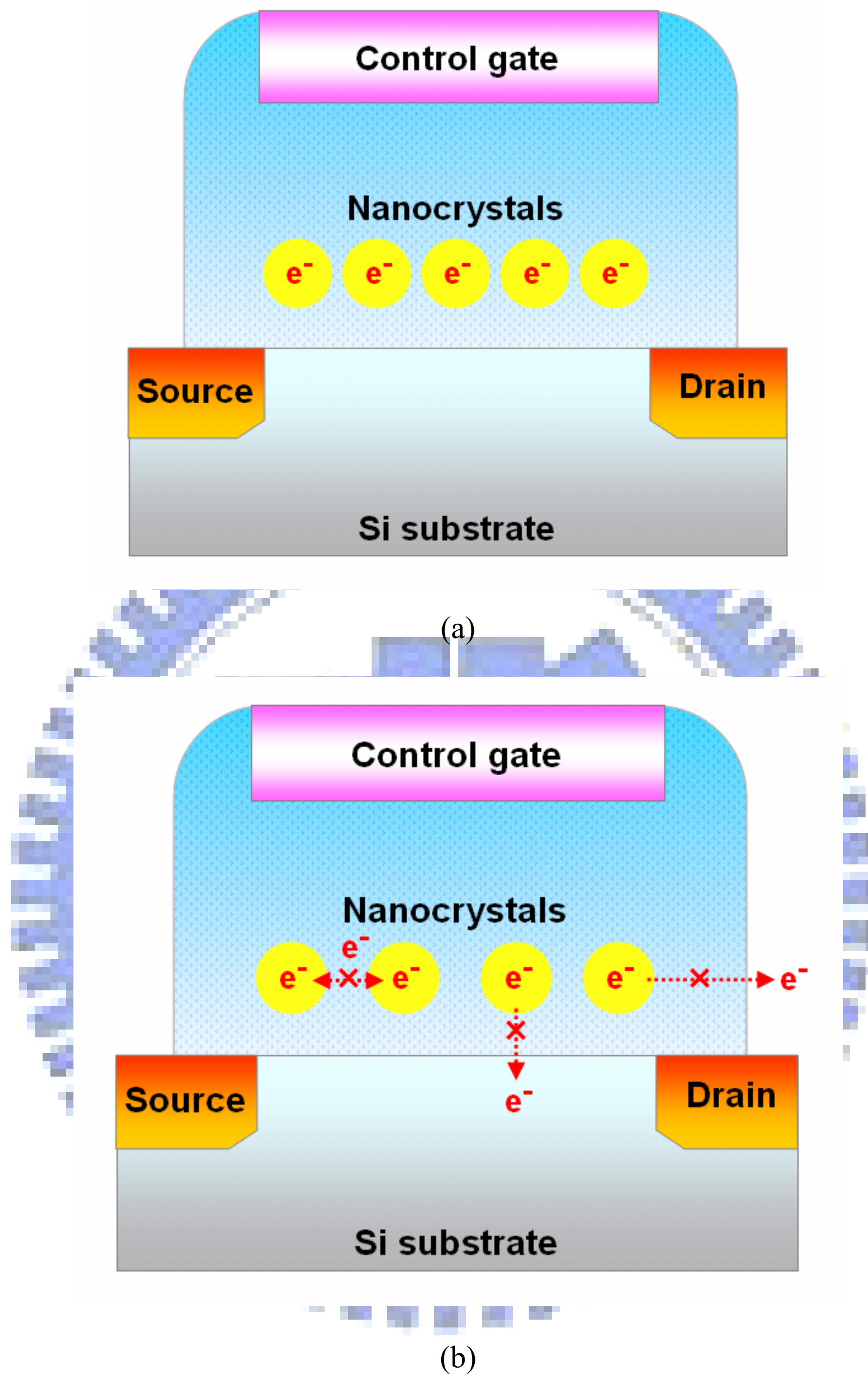


Fig. 1.6 (a) An illustration of a nanocrystal Memory. (b) The nanocrystal can store the charge locally due to the well isolation of nanocrystals from each other and effectively prevents formation of good conductive paths between the adjacent nodes

Chapter 2

Characteristics of HfO_2 Nanocrystal Nonvolatile Flash Memory

2.1 Introduction

SONOS-type (poly-Si-oxide-nitride-oxide-silicon) structure memories, which include nitride and nanocrystal memories, have recently attracted much attention for their application in the next-generation nonvolatile memories [2.1–2.10]. They exhibit many advantages, e. g., easy to fabricate, high program/erase speed, low programming voltage and power consumption, better potential for scalability below the 70-nm node, according to the International Technology Roadmap for Semiconductors (ITRS) [2.11]. Unfortunately, many concerns still remain for this type of memories. For conventional SONOS memory, erase saturation and vertical stored charge migration [2.7-2.8] are two major drawbacks. While, for nanocrystal memories, the most challenging tasks are how to maintain acceptable charge capability of the discrete storage nodes and fabricate nanocrystals with constant size, high density, and uniform distributions [2.9]. In recent years, various ONO processing technology [2.10] and alternative trapping layer material [2.12] have been investigated to improve the cell data retention. For example, the use of an Al_2O_3 trapping layer and $HfAlO_3$ to replace Si_3N_4 have been considered since their material bandgaps and high trap densities provide superior program/erase speed and data retention [2.12-2.13]. Moreover, various kinds of nanocrystals, such as silicon (Si), germanium (Ge), and metal nanocrystals, may be used to provide charge storage for nonvolatile memories [2.1-2.6].

In this chapter, we propose a novel technique which is fully compatible with the

current CMOS technologies, in forming very localized HfO_2 nanocrystals for application in high-density two-bit nonvolatile Flash memory. This approach utilizes spinodal decomposition of hafnium silicate after RTA treatment at a sufficiently high temperature [2.14-2.15]. Using this technique, we can readily isolate the HfO_2 nanocrystals from each other within a SiO_2-rich matrix. With a large band gap offset between HfO_2 and SiO_2, memory cell using HfO_2 nanocrystal may exhibit superior characteristics, such as a larger memory window, high program/erase speeds, long retention time, excellent endurance [2.16-2.17], and strong immunity against disturbance. In addition, by comparing to those published ones using Si, Ge, and metal nanocrystals [2.1-2.6], our HfO_2 nanocrystal memory possesses many advantages, such as larger memory window and better data retention. Moreover, high temperature process for the S/D activation is no longer detrimental because this step can help further stabilize the HfO_2 nanocrystal; while it will oxidize the other nanocrystals and lead to a decrease in memory window. The process is very simple, reproducible, and reliable with less metal contamination concern.

2.2 Experimental

An example of the fabrication process of the HfO_2 nanocrystal memory devices is demonstrated by a LOCOS isolation process on a p-type, 5–10 Ω cm, (100) 150-mm silicon substrate (Fig. 2.1). First, a 2nm tunnel oxide was thermally grown at 1000 °C in a vertical furnace system. Next, a 12nm amorphous $HfSiO_x$ silicate layer was deposited by co-sputtering with pure silicon (99.9999% pure) and pure hafnium (99.9% pure) targets in an oxygen gas ambient. The co-sputtering process was performed with 7.6×10^{-3} Torr at room temperature and with precursors of O_2 (3 sccm) and Ar (24 sccm); in which both dc sputter powers were set at 150 W. The

samples were then subjected to RTA treatment in an O_2 ambient at 900 °C for 1 min to convert the $HfSiO_x$ silicate film into the separated HfO_2 and SiO_2 phases. Their compositions were identified using both energy-dispersive spectroscopy (EDS) and X-ray photoelectron spectroscopy (XPS). A 8nm blocking oxide was then deposited through high-density-plasma chemical vapor deposition (HDPCVD), followed by a N_2 densification process at 900 °C for 1 min. Subsequently, poly-Si deposition, gate patterning, source/drain (S/D) implanting, and the remaining standard CMOS procedures were completed to fabricate the HfO_2 nanocrystal memory devices.

2.3 Results and Discussion

2.3.1 Material Analysis of HfO_2 Nanocrystals

Figure 2.2 shows planar-view high-resolution transmission microscopy (HRTEM) image of the HfO_2 nanocrystals. The average nanocrystal size was 5–8 nm; the density was as high as 0.9–1.9 $\times$ 10^{12} cm^{-2}. Clearly, the nanocrystals were well separated in two dimensions within the SiO_2; in which the average distance is >5 nm. This isolation of the nanocrystals prevents the formation of effective conductive paths between adjacent nodes. The mechanism responsible for the formation of HfO_2 nanocrystal is through the phase separation of hafnium silicate into a crystallized structure [2.14]. For the Hf-silicate layer, the compositions within metastable extensions of the spinodal are unstable and HfO_2 nanocrystal will be formed and wrapped up by SiO_2 after cooling down from RTA processing. In addition, it is clear from the diffraction patterns that the as-deposited film was amorphous and that the sample subjected to RTA was polycrystalline. The HfO_2 nanocrystals have monoclinic crystalline structures. Table 2.1 lists the original average concentrations of the individual elements in the as-deposited amorphous $HfSiO_x$ silicate layer, as

determined through EDS analysis at a spatial resolution less than 2.0 nm. We observe that the as-deposited $HfSiO_x$ layer comprised ca. 40 mol% HfO_2 and 60 mol% SiO_2; the average elemental concentrations of Hf, Si, and O were 12.61, 18.99, and 68.40%, respectively. At this elemental composition, we can readily reproduce high-density HfO_2 nanocrystal dots embodied within a SiO_2-rich matrix after RTA in an O_2 ambient.

Moreover, we also deposited 2nm and 6nm amorphous $HfSiO_x$ silicate layer by the same co-sputtering conditions. The samples were also subjected to RTA treatment in an O_2 ambient at 900 °C for 1 min to convert the $HfSiO_x$ silicate film into the separated HfO_2 and SiO_2 phases. Figure 2.3 (a) and 2.3 (b) show the planar-view high-resolution transmission microscopy (HRTEM) image of the HfO_2 nanocrystals for the different thickness samples. With the thickness increases, the better HfO_2 nanocrystals form, the HfO_2 nanocrystal size increases, but the nanocrystal destiny decreases. Table 2.2 shows the comparison table of the different thickness samples of $HfSiO_x$ silicate layers after 900°C-RTA-treated.

We have also performed X-ray photoelectron spectroscopy (XPS) measurements using an Al *K*α X-ray source (1486.6 eV photons) to determine the bonding environments of the Hf and Si atoms. Fig. 2.4(a) shows the Hf 4f photoemission peaks of the as-deposited Hf-silicate film before and after its PDA at 900 °C under O_2. In the as-deposited film we observe well-defined $4f_{5/2}$ and $4f_{7/2}$ feature peaks that correspond to Hf–O–Si bonding. We confirmed that HfO_2 nanocrystals formed after RTA through the observed shifts of these peaks to lower binding energies ($4f_{5/2}$: ca. 18.9 eV; $4f_{7/2}$: ca. 17.4 eV) [2.18-2.19]. Fig. 2.4(b) shows Si 2p XPS spectra of the as-deposited Hf-silicate film before and after RTA. Again, the Si–O bonds in SiO_2 network (104 eV) are prominent; their peak intensity increased after PDA. These results provide definite evidence for phase separation occurring in the PDA-treated

Hf-silicate film.

2.3.2 Characteristics of Fresh Devices and 2-bit operation

Figure 2.5 shows the I_{ds}-V_{gs} curves of the HfO_2 nanocrystal memory devices with programming time of 10μs for different programming conditions. Channel hot-electron injection and band-to-band hot-hole injection were employed for programming and erasing, respectively. All cells described in this chapter have dimensions of L/W = 1/2 μm. A relatively large memory window of about 3V can be achieved at the V_g=V_d=10V program operation. Program characteristics as a function of pulse width for different operation conditions are shown in Fig. 2.6(a). Both source and substrate terminals were biased at 0V. The "V_t shift" is defined as the threshold voltage change of a device between the written and the erased states. With V_d=V_g=9V, relatively high speed (10μs) programming performance can be achieved with a memory window of about 2.2V. Meanwhile, Fig. 2.6(b) displays the erase characteristics as a function of various operation voltages. Again, excellent erase speed of around 0.1 ms can be obtained. More important, there is only a very small amount of over-erase observed. The reason is owing to the fact that the vertical electric field decreases with decreasing amount of trapped electrons in the nanocrystals during erasing and the hole injection into the nanocrystals will reduce significantly due to the higher hole tunneling barrier presented in HfO_2/SiO_2 stack after all programmed charges are removed [2.20].

The retention characteristics of the HfO_2 nanocrystal memory devices at both room temperature (T=25°C) and higher temperature (T=125°C) are illustrated in Fig. 2.7. The retention time can be up to 10^8 seconds for 10% charge loss at room temperature. Only slight charge loss has been seen even at the temperature up to

125°C. We ascribe these results to the combining effects of the tight embrace of HfO_2 nanocrystals by SiO_2-rich matrix and the sufficiently deep trap energy level [2.20]. Therefore, albeit with a tunnel oxide down to 2nm in thickness, no significant lateral and vertical charge migrations occurred. As a result, superior retention characteristic of the charge storage can be procured. The endurance characteristics after 10^6 P/E cycles are also shown in Fig. 2.8. The programming and erasing conditions are V_g=V_d=9V for 10μs and V_g=-5V, V_d=10V for 1ms, respectively. No detectable memory window narrowing has been displayed. Moreover, the individual threshold voltage shifts in program and erase states only become visible after 10^5 cycles. This trend indicates that the amount of operation-induced trapped electrons is very tiny. Certainly, this is intimately related to the use of ultra-thin tunnel oxide and very minute amount of residual charges in the HfO_2 nanocrystals after cycling. Fig. 2.9 demonstrates the feasibility of performing two-bit operation with our HfO_2 nanocrystal memories through a reverse read scheme in a single cell. From the I_{ds}–V_{gs} curves, it is clear that we could employ forward and reverse reads to detect the information stored in the programmed bit1 and bit2, respectively. The read operation was achieved using a reverse read scheme. Table 2.3 summarizes the bias conditions for two-bit operation.

2.3.3 Migration of storage charges

One of the major advantages that HfO_2 nanocrystal Flash memory has over floating gate Flash EEPROM is its better data retention, which is attributed to its excellent capability of locally trapping charges with no significant lateral or vertical migration. We can measure the degrees of migration from the cells after the cycling. One method for characterizing the lateral extent of the trapped electrons is to monitor

the variation of the threshold voltage (V_t) for a programmed memory cell in the presence of a changing drain current (V_d) [2.19]. Fig. 2.10 shows a plot of the measured V_t versus V_d as a function of the measuring temperature in a programmed cell after 10k P/E cycling. Here, V_t is defined as the applied gate voltage at which the drain current is 1 μA. Since channel hot-electron injection is used for the cell programming, the trapped electrons in the HfO_2 nanocrystal trapping layer are more likely to be located near the n^+ drain junction. These trapped electrons will raise the potential barrier near the drain side and increase the value of V_t. The degree of the V_t shift is believed to be proportional to the trapped electron density if the drain terminal is maintained at a relatively low potential (e.g., V_d = 0.1 V). When a sufficiently high drain bias (e.g., V_d = 1.5 V) is applied, however, the drain depletion region will be extended toward the channel and, consequently, block the influence from the trapped electrons for the measured I_d–V_g characteristics [2.21]. Therefore, this proposed technique can detect the lateral profile of the trapped electrons. To enhance the storage charge movement in the HfO_2 nanocrystal trapping layer, the programmed samples were subjected to high-temperature baking at 80 and 125 °C for 2000 s, respectively. Remarkably, the V_t–V_d curves for the cycled device and the baked devices exhibit very little difference, suggesting that lateral migration of the storage charges in the HfO_2 nanocrystal trapping layer is rather insignificant. It was attributed to the effective isolation of each nanocrystal within the SiO_2 matrix. Next, we investigated the influence of the vertical field on charge retention, i.e., vertical migration. Fig. 2.11 shows the V_t variation over time for various stress conditions for the 10k P/E cycled cells. Visible charge loss was observed when the applied gate voltage and temperature were raised up to -5V and 125°C. We thought even though the trap energy level in the nanocrystal is quite deep, the generated defects and interface traps of the 2nm tunnel oxide after 10k P/E cycled stress will help stored

charges escape via trap-assisted tunneling. Therefore, vertical charge migration is more observable than lateral charge migration in our memory cell. We also calculated the activation energy for the traps of the HfO_2 nanocrystals in the new cells (Fig. 2.12). Activation energy tracing is used widely to characterize the Arrhenius relation extracted from the temperature dependence of charge loss from nonvolatile memory as a function of time. For a given charge loss threshold criterion (in our case, 20% is used), the failure rates obtained at high temperature (125–200 °C) can then be extrapolated to the nominal operating conditions. The model is based on a classical temperature-activated Arrhenius law, expressed in the form $t_R = t_0 \times e^{E_a/kT}$, where t_0 is the retention time corresponding to an infinite temperature, E_a is the activation energy, T is the temperature, and k is the Boltzmann constant [2.22]. The activation energy, determined from the slopes of five samples, lies in the range 2.1–3.3 eV, Obviously, it is higher than those values previously reported for conventional SONOS memories [2.23-2.25].

2.3.4 Disturbance

Figure 2.13 demonstrates the read disturbance induced erase-state threshold voltage instability in a localized HfO_2 nanocrystal trapping storage Flash memory cell under several operation conditions. For two-bit operation, the applied bitline voltage in a reverse-read scheme must be sufficiently large (>1.5 V) to be able to "read through" the trapped charge in the neighboring bit. The read-disturb effect is the result of two factors: the word-line and the bit-line. The word-line voltage during read may enhance room temperature (RT) drift in the neighboring bit [2.26]. On the other hand, a relatively large read bit-line voltage may cause unwanted channel hot-electron injection and, subsequently, result in a significant threshold voltage shift of the

neighboring bit. In our measurements, the gate and drain biases were applied and the source was grounded. The results demonstrate clearly that almost no read disturbance occurred in our HfO_2 nanocrystal Flash memory under low-voltage reading (V_g = 3 V; V_d = 2.5 V). For a larger memory window, we found that only a small read disturbance (ca. 0.3 V) can be observed after operation at V_d = 4 V after 1000 s at 25 °C.

Figure 2.14 shows the programming drain disturbance of our HfO_2 nanocrystal Flash memory. Two different drain voltages (V_d = 5 and 9 V) were applied in the programming drain disturbance measurements at two different temperatures (T = 25 and 125 °C). We observed that a sufficient programming drain disturb margin exists ($\Delta V_t < 0.4$ V), even after programming at a value of V_d of 9V under high temperature (T = 125 °C) and after stressing for 1000 s. Fig. 2.15 shows the gate disturbance characteristics in the erasing state. Gate disturbance may occur during programming for the cells sharing a common word-line while one of the cells is being programmed. We observed a threshold voltage shift of only 0.16 V, i.e., negligible disturbance, under the following conditions: V_g = 9 V; $V_s = V_d = V_{sub}$ = 0 V; stressed for 1000 s. It in interested to know why this memory can exhibit such excellent gate disturb characteristics with such a thin tunnel oxide; a non-negligible current will be present in the tunnel oxide when a voltage of 9 V is applied to the gate electrode. Using a serial capacitor voltage divider model, we estimated that the voltage drop at the tunnel oxide would be 0.98 V if the trapping layer is assumed to be a HfO_2 film, rather than nanocrystal. Even though a 0.98V drop will cause a significant leakage current through an individual 2nm oxide layer, the data retention in the memory cell is related not only to the direct tunneling leakage current induced by such a voltage but also to the total tunneling situation in the whole gate stack; i.e., the effect that the potential barrier presented by the high-k material has on the tunneling current must be taken

into account. In other words, it is incorrect to state that a large direct tunneling current will definitely exist in the interfacial layer and, in turn, that it will induce significant disturbance during programming.

2.3.5 Charge pumping characteristics

The charge pumping (CP) measurement was used to investigate the characteristics of our HfO_2 nanocrystal Flash memory. We used a trapezoidal gate pulse having a fixed pulse amplitude with a varying V_{gbl}. The substrate current (the so-called "charge pumping current," I_{cp}) as a function of V_{gbl} was measured. The gate pulse have a frequency of 1 MHz and a 50% duty cycle; the rising and falling times were both 2 ns. Fig. 2.16 shows plots of the program state charge pumping current I_{cp} versus V_{gbl} for our HfO_2 nanocrystal memory cell. Fowler–Nordheim tunneling was used to program the cell with V_t levels from 2.06 to 3.51 V. The open symbols represent the measured data. The program state I_{cp} curve shifted increasingly toward the right upon increasing the value of V_t as a result of an increase in the amount of injected charge in the HfO_2 nanocrystal trapping layer. Interestingly, a hump appeared in the left-hand edge of the curve in compliance with this shift. We decompose the resultant I_{cp} curve mathematically into two individual curves, A and B, in a fresh memory cell. We speculate that these two I_{cp} curves arise from interlacing of the SiO_2 matrix and HfO_2 nanocrystals within the trapping layer. In other words, the memory is composed of two kinds of devices that have different gate dielectric configurations. The extracted threshold voltage in curve A is larger than that in curve B, even for a fresh memory; because the value of EOT of the gate stack in the region containing SiO_2 matrix is larger than that in the part containing the HfO_2 nanocrystals. We believe that curve A is related to the SiO_2 matrix and curve B corresponds to the HfO_2

nanocrystals. With programming, it is clear that the I_{cp} curve arising from the region containing the SiO_2 matrix undergoes almost no shift and the resultant distortion appearing in the measured I_{cp} curve is caused mainly by the charging of the HfO_2 nanocrystal. This result implies that the programming charge was stored almost entirely within or around the HfO_2 nanocrystal, rather than in the SiO_2 matrix. To confirm this hypothesis, we traced the measured curve by adding curve A to a horizontally shifted curve B; that this approach works quite well. In addition, we also analyzed the devices formed from a pure HfO_2 trapping layer on top of a SiO_2 tunnel oxide structure. It was observed that only curve B shifted horizontally when programming (data not shown). Consequently, we conclude that HfO_2 nanocrystals can behave as an excellent local charge trapping centers.

2.3.6 Characteristics after P/E cycling

Figure 2.17 shows the endurance characteristics of the HfO_2 nanocrystal memory cell. The programming and erasing conditions were $V_g = V_d = 9$ V for 10 μs and $V_g = -5$ V, $V_d = 10$ V for 1 ms, respectively. Remarkably, the values of V_t in the program and erase states did not increase significantly up to 10^5 P/E cycles, while the memory window underwent a significant narrowing after 10^6 cyclic operations. The spatial distributions for electron and holes are localized during the channel hot-electron injection and band-to-band hot-hole injection for the programming and erasing, respectively, of our HfO_2 nanocrystal memory. If the electron distribution does not completely match that for the hole, then each P/E cycle will leave a few electrons in the trapping layer [2.27]. This so-called "hard-to-erase" phenomenon cannot be eliminated readily when using band-to-band hot-hole erasing. Obviously, this is not an issue for our memory because the enhanced local electric field across the thin tunnel

oxide in the region just beneath the nanocrystals can help in the injection of holes. Fig. 2.18 illustrates the retention characteristics of the HfO_2 nanocrystal memory devices for a 10k P/E stressed HfO_2 nanocrystal memory cell both at room temperature (T = 25 °C) and above (T = 125 °C). Relative to the fresh device, the device operated at room temperature retained its good retention time (up to 10^5 s) for 10% charge loss [16]. We ascribe this result to the combined effects of the tight embrace of the HfO_2 nanocrystals by the SiO_2-rich matrix and the sufficiently deep trap energy level of our memories (extracted activation energy: 2.1–3.3 eV). Therefore, despite the tunnel oxide having a thickness as low as 2 nm, no significant lateral or vertical charge migration occurred; as a result, the device displays superior retention characteristics for charge storage. At the temperature at 125 °C, we observed a more significant charge loss during the program state. This strong temperature-dependence was predictable from the large activation energy, but the detailed mechanism remains under further investigation. Table 2.4 presents a comparison of our results with those of recent investigations into new devices [2.2, 2.5, 2.8]. Our system shows a number of salient features. First, our HfO_2 nanocrystal memories exhibit larger memory windows than do the other systems because of the large trap density of the high-k dielectric materials. Second, with respect to the P/E speed, we obtained a high speed of operation because we used channel hot-electron programming and band-to-band hot-hole erasing. Finally, we observed good retention with no vertical or lateral migration as a result of the HfO_2 nanocrystals being isolated effectively within the SiO_2 matrix.

2.3.7 Characteristics of different tunnel oxide thickness

Figure 2.19 and 2.20 show the programming and erasing characteristics,

respectively, of the fabricated HfO_2 nanocrystal memory with three different tunnel oxide thicknesses, 2nm, 4nm and 6.1nm, respectively. We programmed with the bias condition at V_g = 10V and V_d = 10V and erased with the bias condition at V_g = 10V and V_d = -5V. We observed that the memory with thinner tunnel oxide exhibited slightly improved programming speed when they were operated with the short pulse widths and better erase performance. Fig. 2.21 illustrates the retention characteristic of the fresh HfO_2 nanocrystal memory with three different tunnel oxide thicknesses at different testing temperatures. For all cases, the retention times can be extrapolated up to more than 10^8 seconds for 15% charge loss at room temperature. Such good retention performance can be ascribed to the sufficiently deep trap energy levels in hafnium silicate. We also calculate the activation energy of the traps in the HfO_2 nanocrystals for the fresh device with different tunnel thickness in the figure 2.22. For a given charge–loss threshold criterion (in our case, 20%), the obtained failure rate can then be extrapolated to the nominal operating condition. The activation energy, determined from the slopes of five samples, lies in the range 2.1–3.3 eV, 2.46-3.11eV, and 2.95-3.26eV for the 2nm, 4nm, and 6.1nm samples, respectively. Therefore, we thought that the sample with thick tunnel oxide can be employed for achieving better charge keeping capability. For the thicker sample, the activation energy lies in the narrow range because more uniform tunnel oxide of 6.1nm. The thinner tunnel oxide of 2nm may have more leakage path for the charge during the temperature stress. Obviously, these values also lie in the higher ranges of those scattered values previously reported for the conventional SONOS memories. The endurance performances of the HfO_2 nanocrystal memory with different tunnel oxide thicknesses are shown in Fig. 2.23. Despite the occurrence of significant memory window narrowing, a memory window of about 2V sustained even after 10^5 P/E cycles. The origin of the narrowing over cycling might be due to two factors. First is the mismatch

between the localized spatial distributions for the injected electrons and holes by using channel hot-electron programming and band-to-band hot-hole erasing. The uncompensated electrons will then cause the V_t to increase gradually over P/E cycling. The other is the stress-induced electron traps generated in the tunnel oxide during cycling. We found that the rate of memory window narrowing increases upon increasing P/E cycles and the one with thick tunnel oxide had more serious memory window closure.

2.3.8 Vt distribution and realization of multi-bit operation

Four-level threshold voltage (V_{th}) distribution of multilevel programming is shown in Fig. 2.24. Sharp Vth distribution is observed for achieving reliable operation. From the Vth distribution, we can find that our HfO_2 nanocrystals are uniform. The Vth distribution between others still have 0.8V memory window to detect the information. It demonstrates the feasibility of performing four-bit operation with our HfO_2 nanocrystal memories through a reverse read scheme in a single cell. The read operation was achieved using a reverse read scheme.

2.4 Summary

In this chapter, we propose a novel, simple, reproducible, and reliable technique for the design of high-density HfO_2 nanocrystals through the spinodal decomposition of hafnium silicate. Our nanocrystal memory exhibits superior characteristics in terms of negligible lateral or vertical migration of stored charge and good disturbance characteristics. The cells after 10k P/E cycling also show a long retention time and excellent endurance. With these superior performance, we believe that HfO_2 nanocrystal Flash memory is quite suitable for the two-bit operation and that it has

great potential for replacing the ONO stack in conventional SONOS-type Flash memories.

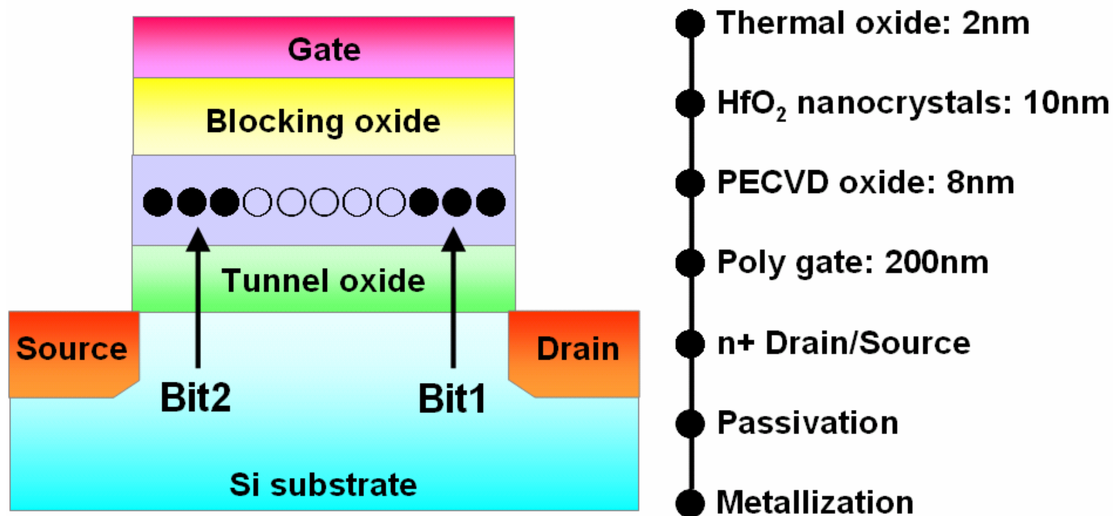


Fig. 2.1 Schematic representation of the HfO_2 nanocrystal Flash memory cell structure and localized charge storage.

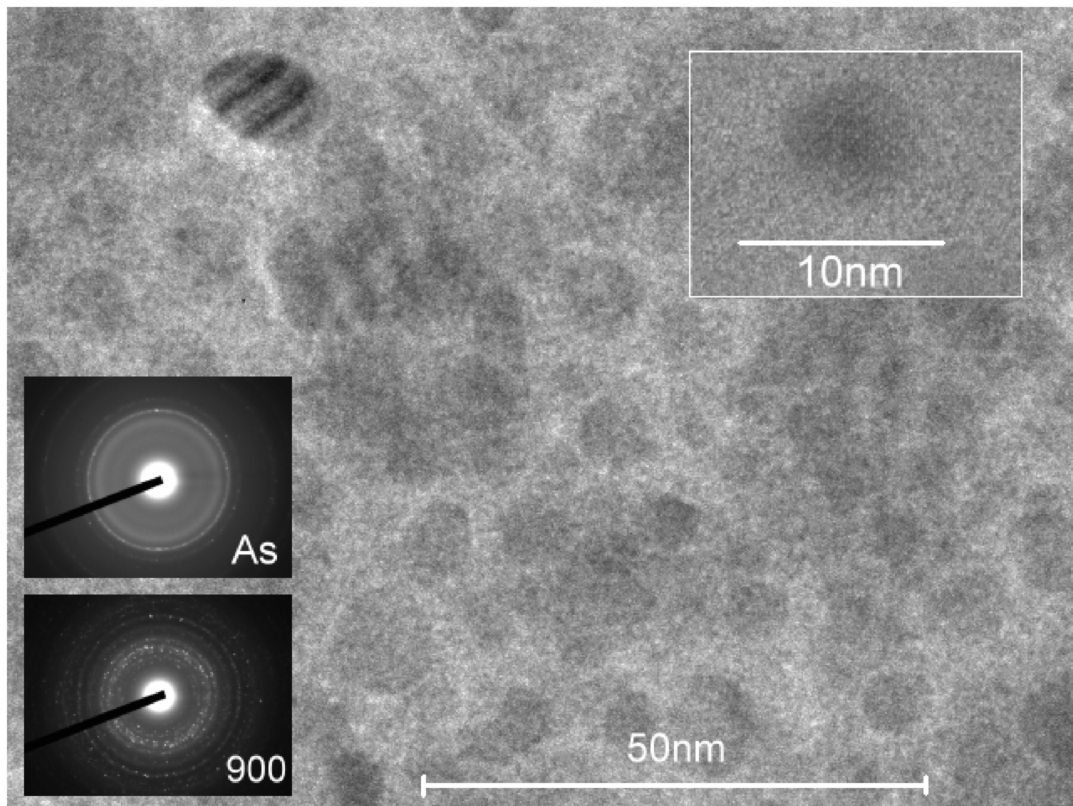


Fig. 2.2 Planar-view HRTEM image of the HfO_2 nanocrystals for the 10nm thickness sample. The cell size is 5-8 nm and the dot density is 0.9-1.9 × 10^{12} cm^{-2}. The inset shows the diffraction patterns of the as-deposited and 900°C-RTA-treated samples.

	Hf (%)	Si (%)	O (%)
Asdep	12.6	19	68.4
900°C inside	24.62	22.74	52.64
900°C outside	2.84	39.65	57.51

Table 2.1 Average elemental compositions in the $HfSiO_x$ silicate layers, as examined through EDS analysis of the as-deposited and 900°C-RTA-treated samples.

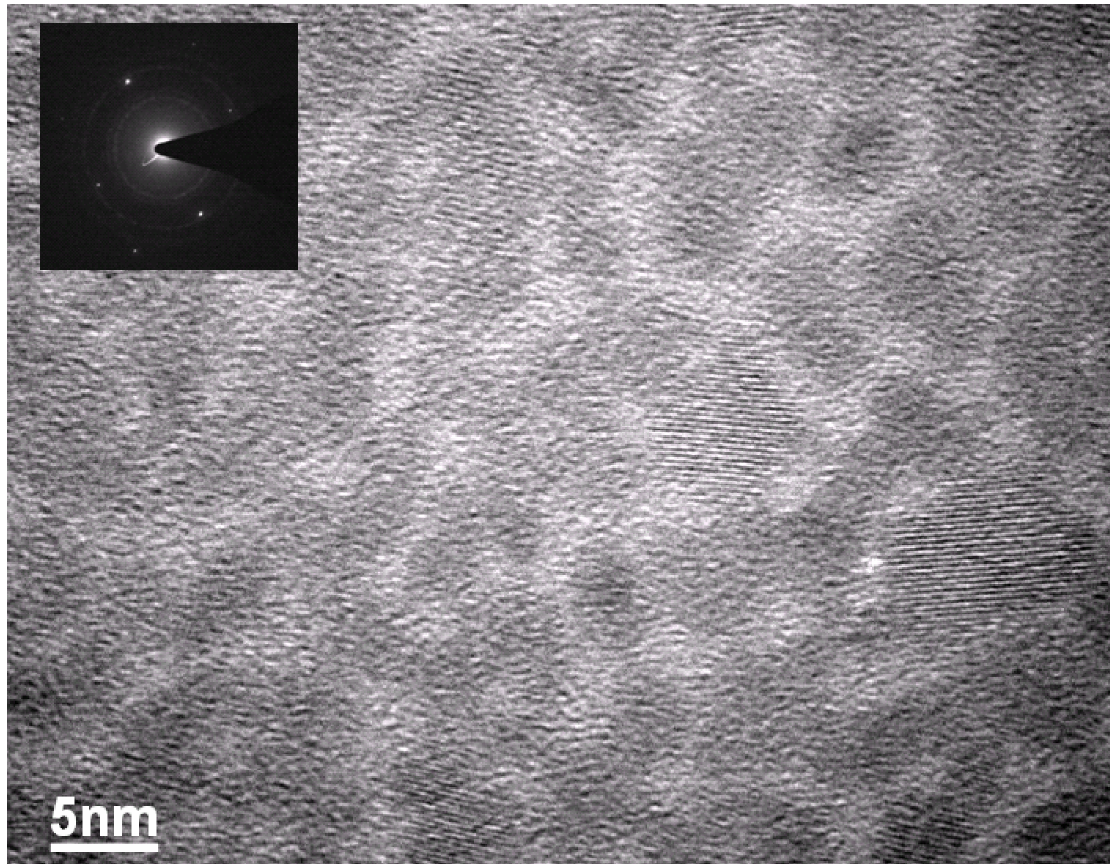


Fig. 2.3 (a) Planar-view HRTEM image of the HfO_2 nanocrystals for the 2nm thickness sample. The cell size is 3-7 nm and the dot density is 1.2-2.0 $\times$ 10^{12} cm^{-2}. The inset shows the diffraction pattern of the RTA-treated samples.

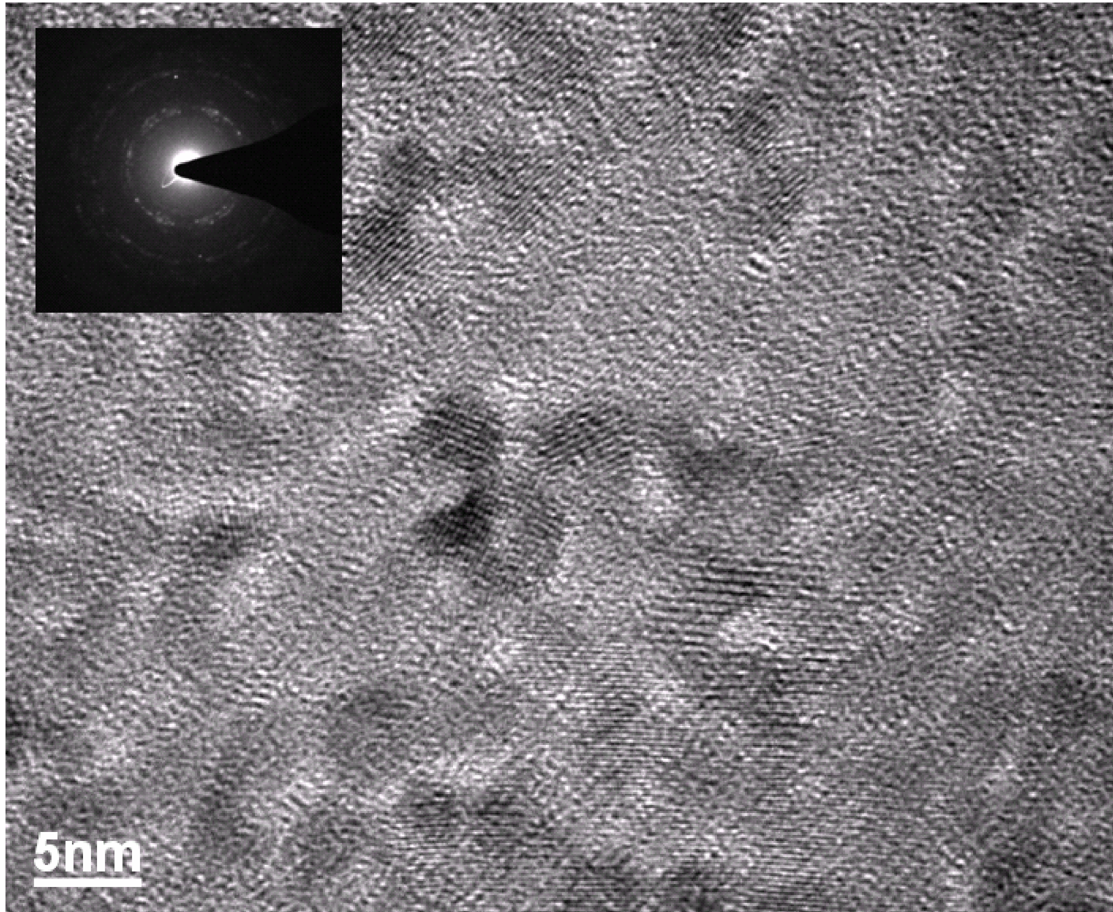


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Fig. 2.3 (b) Planar-view HRTEM image of the HfO_2 nanocrystals for the 2nm thickness sample. The cell size is 4-7 nm and the dot density is 2.1-3.2 $\times$ 10^{12} cm^{-2}. The inset shows the diffraction pattern of the RTA-treated sample.

	10nm	6nm	2nm
Nanocrystal size	5-8nm	4-7nm	3-7nm
Nanocrystal destiny	0.9-1.9 $\times 10^{12}$ cm^{-2}	1.2-2 $\times 10^{12}$ cm^{-2}	2.1-3.2 $\times 10^{12}$ cm^{-2}
Crystallization	Yes	Yes	Yes
Well formed	Excellent	Good	Good

Table 2.2 Comparison table of the different thickness samples of $HfSiO_x$ silicate layers after 900°C-RTA-treated.

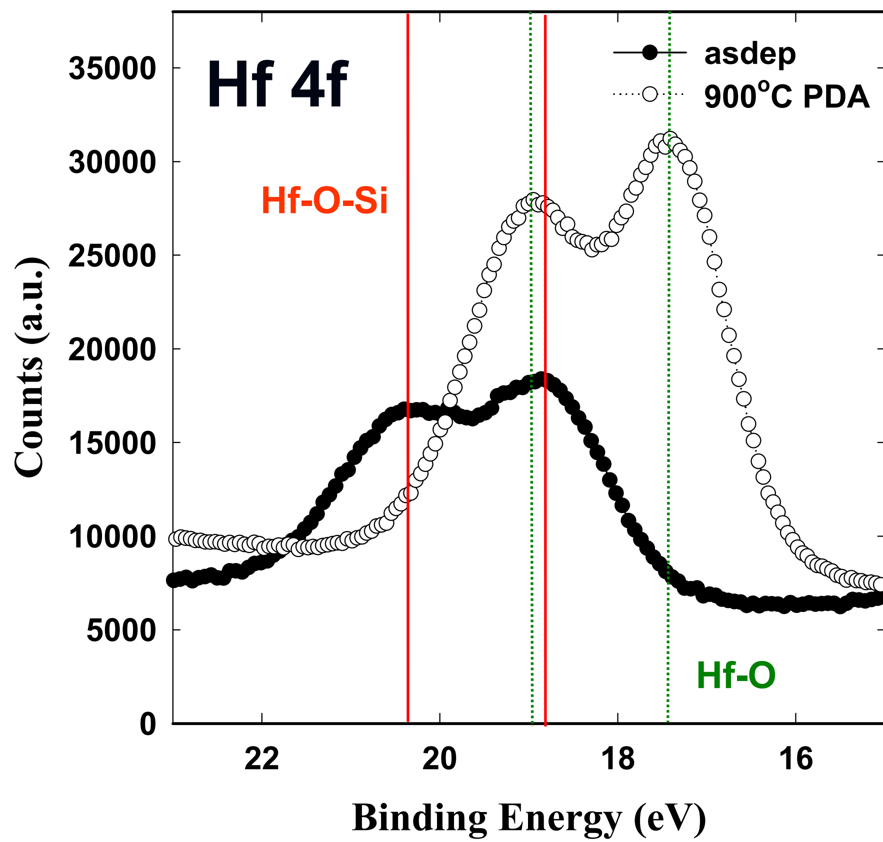


Fig. 2.4 XPS spectra of the as-deposited and 900°C-RTA-treated samples. (a) Hf 4f; (b) Si 2p. These spectra indicate that the Hf-silicate was fully converted to HfO_2 and SiO_2 through phase separation after PDA at 900 °C under O_2.

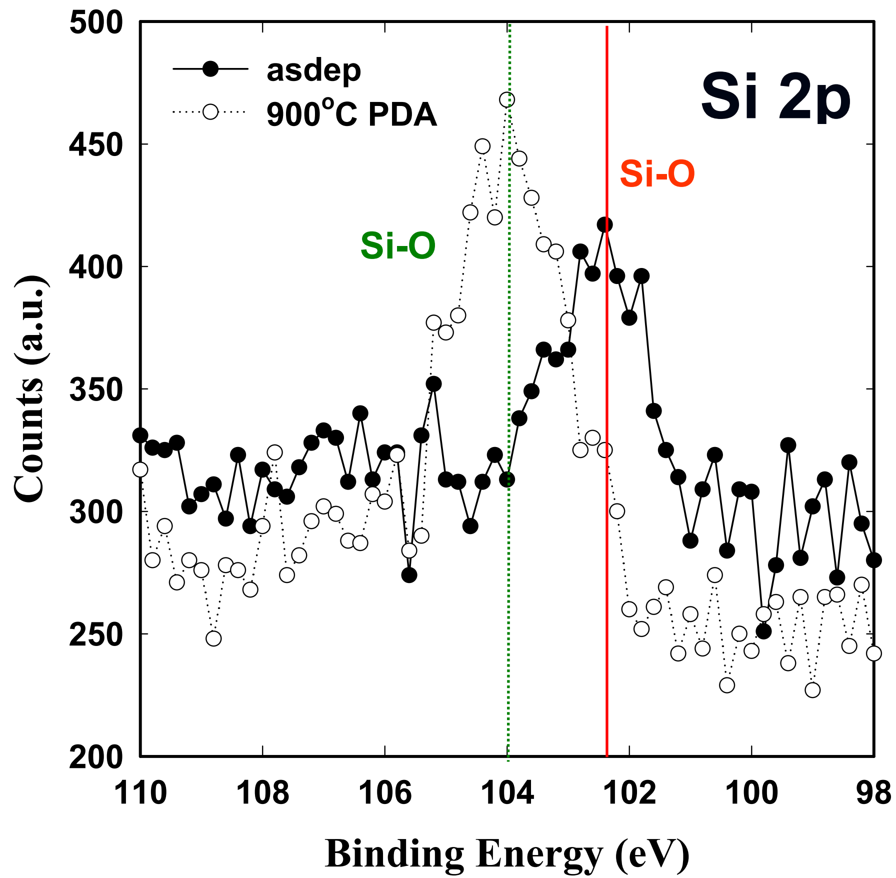


Fig. 2.4 XPS spectra of the as-deposited and 900°C-RTA-treated samples. (a) Hf 4f; (b) Si 2p. These spectra indicate that the Hf-silicate was fully converted to HfO_2 and SiO_2 through phase separation after PDA at 900 °C under O_2.

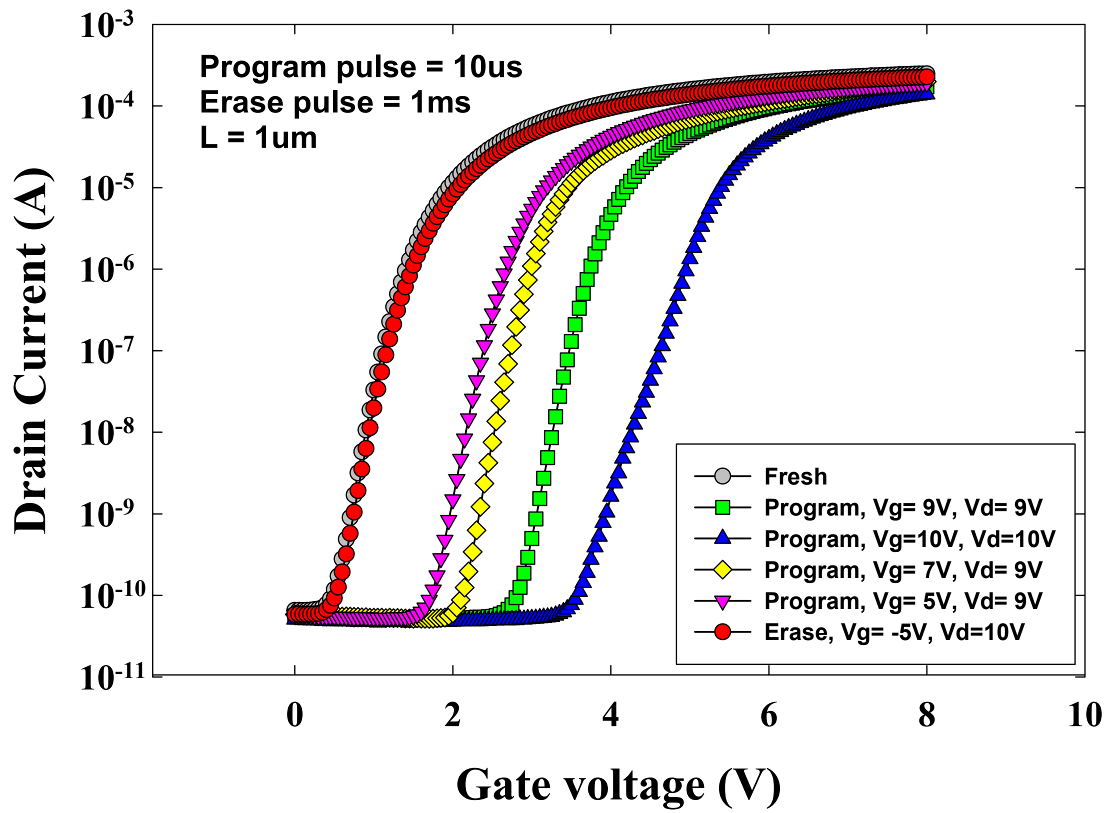


Fig. 2.5 I_{ds}-V_{gs} curves of programmed memories with different programming conditions. The programming time is 10μs. A memory window of larger than 3V can be achieved with V_g= V_d=10V programming operation.

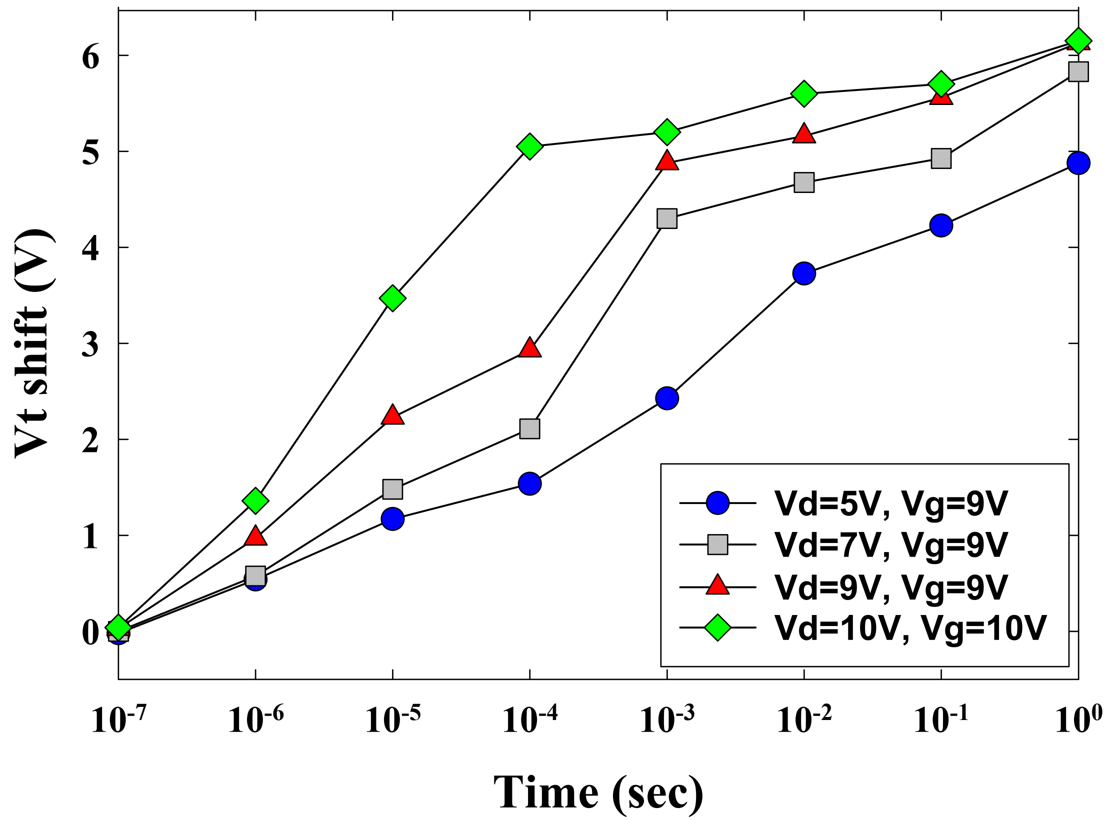
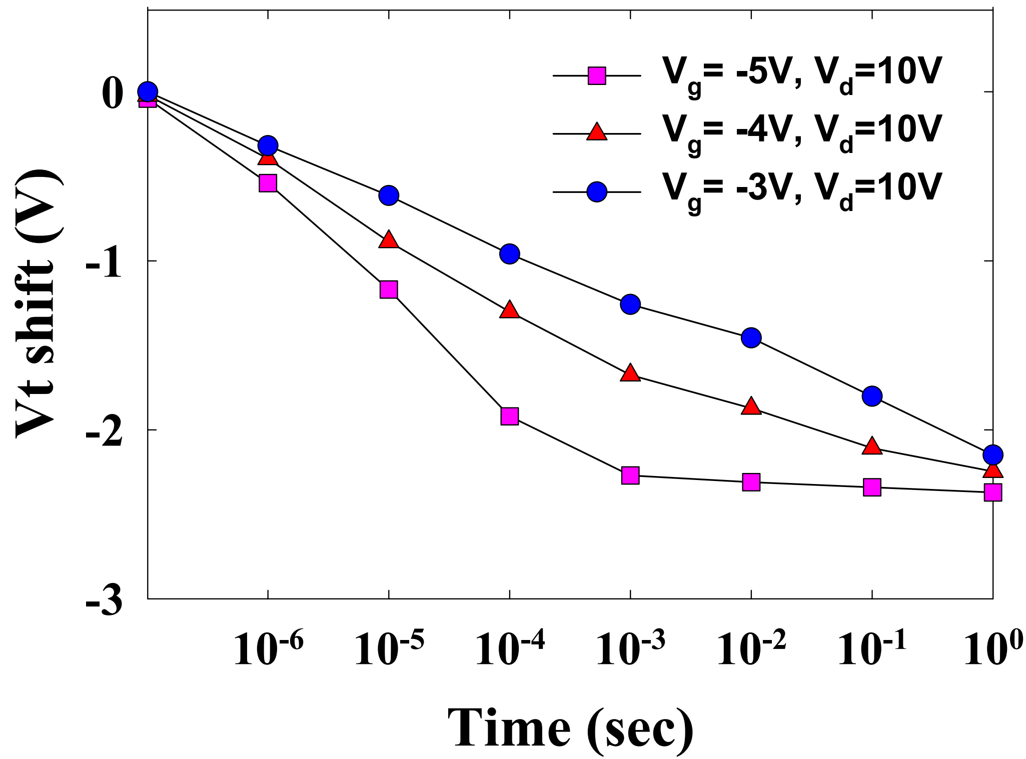
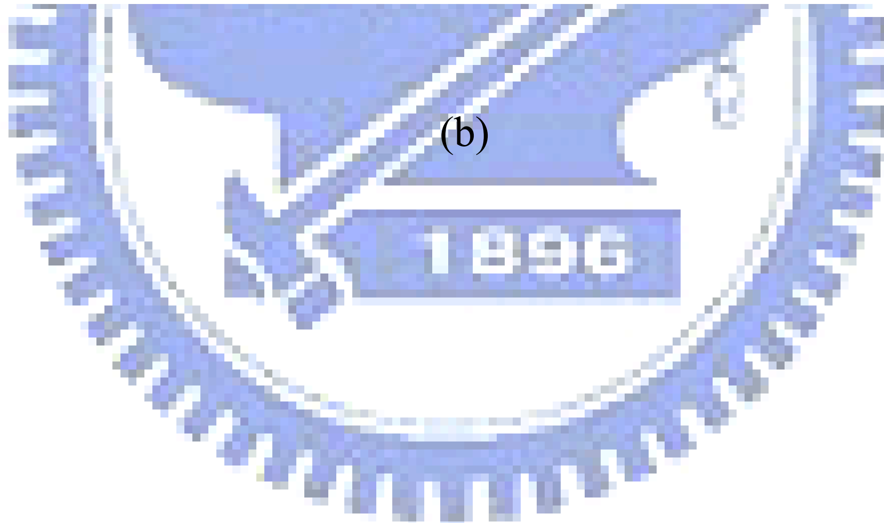


Fig. 2.6 (a) Program characteristics of HfO_2 nanocrystal memory devices with different programming conditions. A memory window of about 5V can be achieved with V_g=V_d=10V, and time=100μs programming operation. (b). Erase characteristics of HfO_2 nanocrystal memory devices with different erasing voltages.





(b)

Fig. 2.6 (a) Program characteristics of HfO_2 nanocrystal memory devices with different programming conditions. A memory window of about 5V can be achieved with V_g=V_d=10V, and time=100μs programming operation. (b). Erase characteristics of HfO_2 nanocrystal memory devices with different erasing voltages.

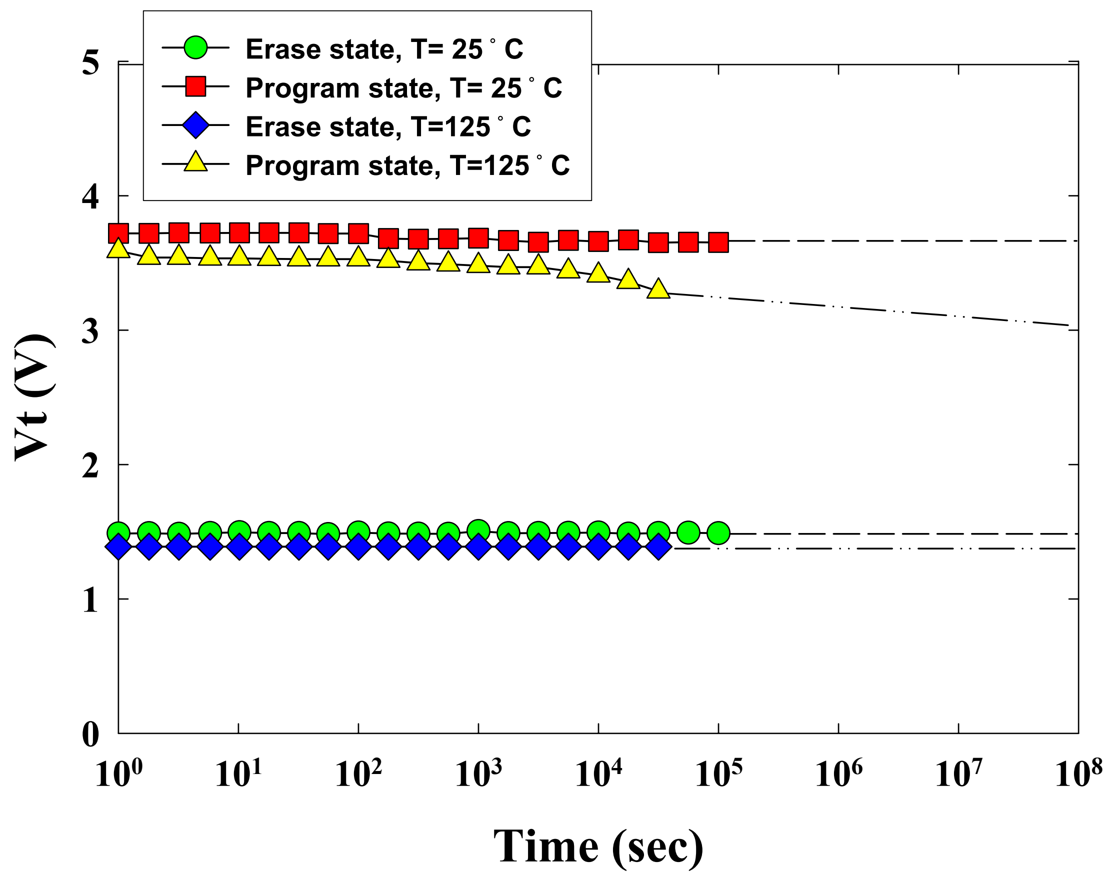


Fig. 2.7 Retention characteristics of HfO_2 nanocrystal memory devices at T=25°C and 125°C. Very low charge loss is seen even after 10^5 seconds.

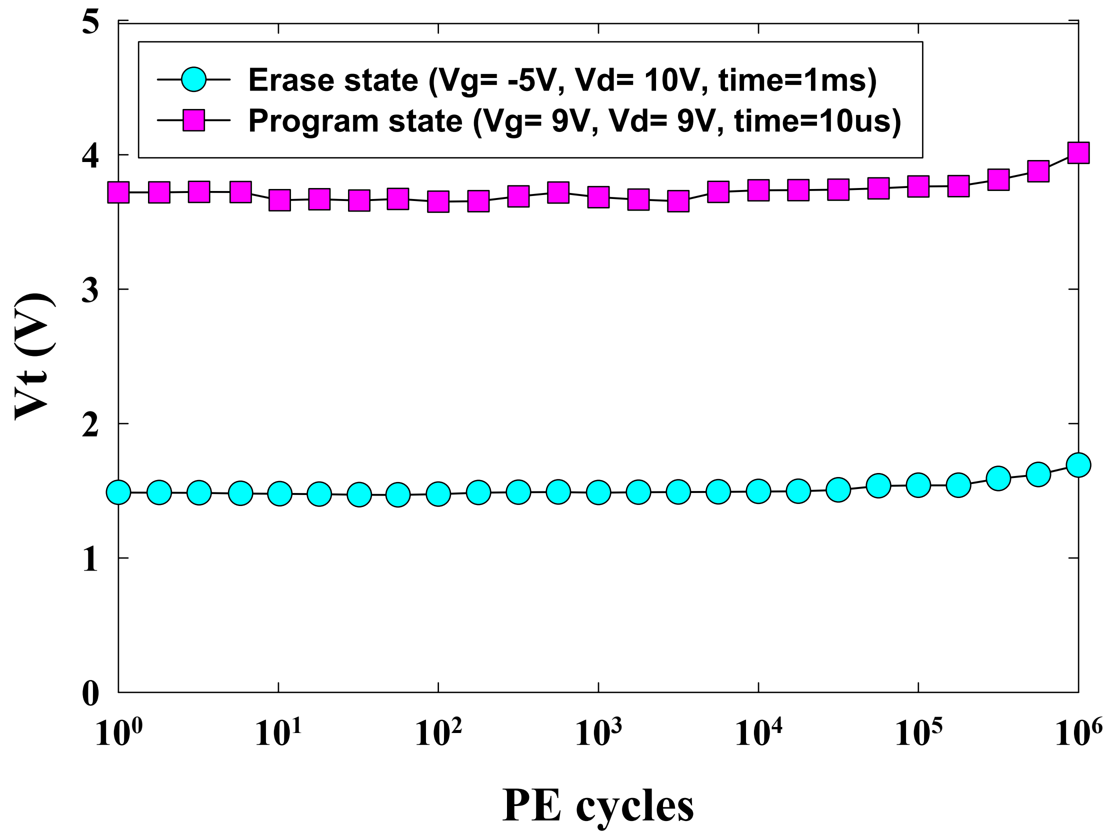


Fig. 2.8 Endurance characteristics of HfO_2 nanocrystal memory devices. Negligible degradation is found even after 10^6 P/E cycles.

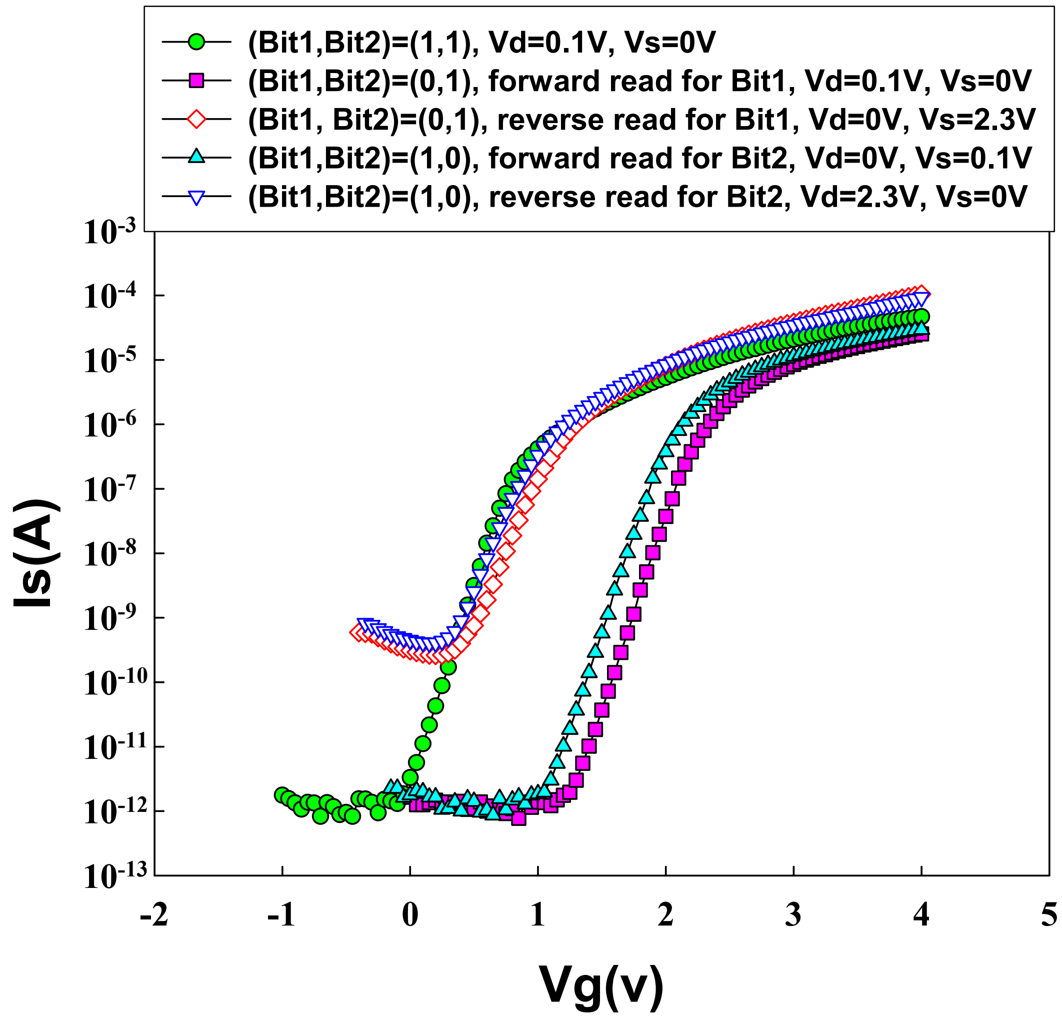


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Fig. 2.9 I_{ds}–V_{gs} Curves of the two-bit memory in a cell; forward read and reverse read for programmed bit1 and programmed bit2.

		Program	Erase	Read
Bit 1	V_g	9V	-5V	2.3V
	V_d	9V	10V	0V
	V_s	0V	0V	>1.6V
Bit 2	V_g	9V	-5V	2.3V
	V_d	0V	0V	>1.6V
	V_s	9V	10V	0V

Table 2.3 Operation principles and bias conditions utilized during the operation of the HfO_2 nanocrystal Flash memory cell.

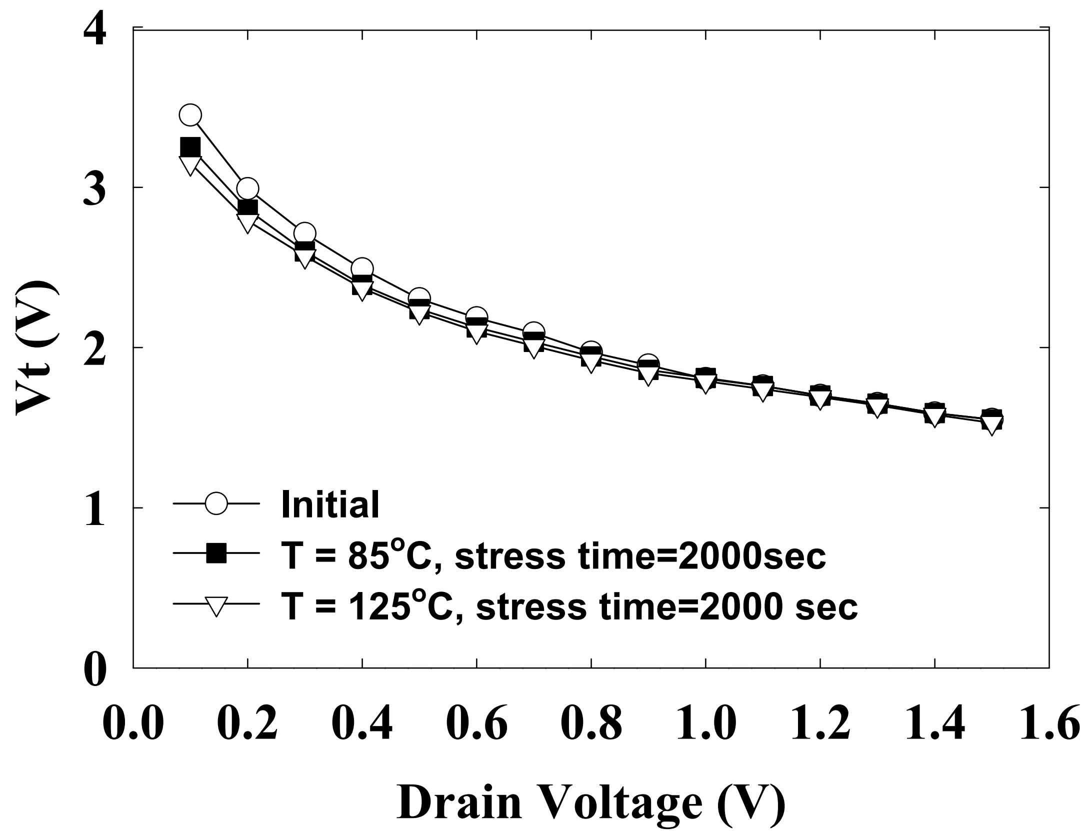

Fig. 2.10 Lateral charge migration characteristics of the HfO_2 nanocrystal Flash memory cells after 10k P/E cycling.

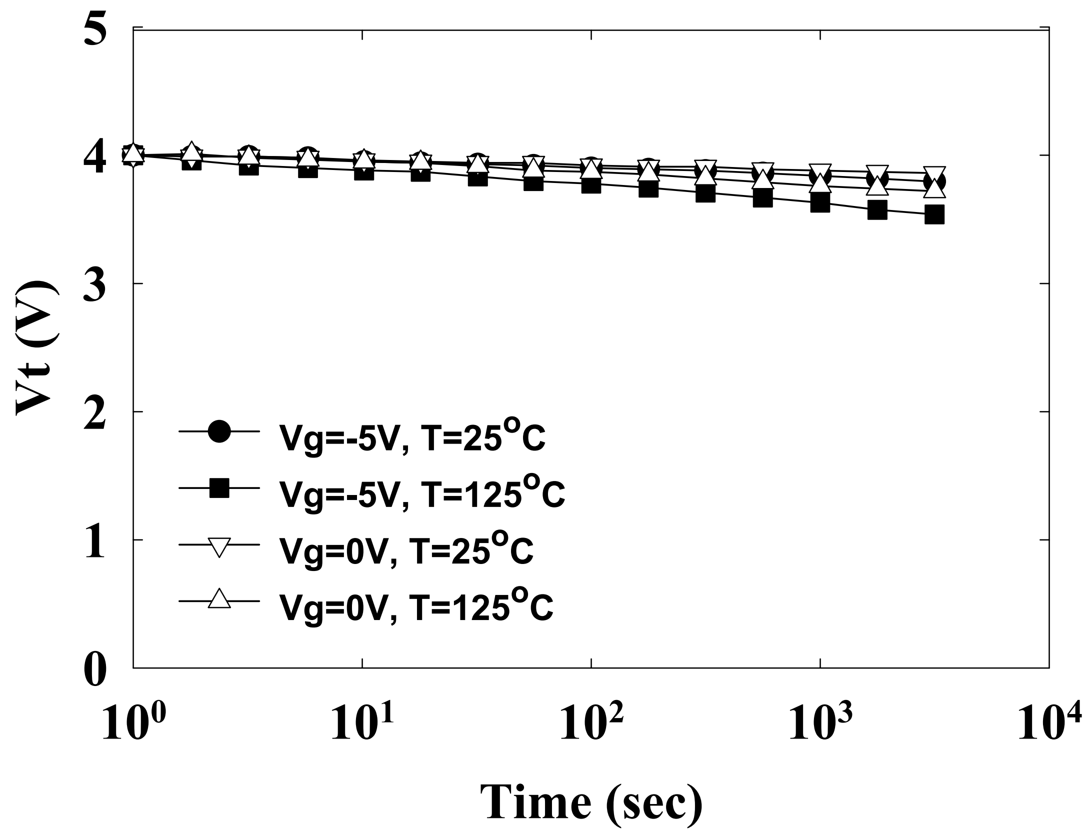

Fig. 2.11 Vertical charge migration characteristics of the HfO_2 nanocrystal Flash memory cells after 10k P/E cycling.

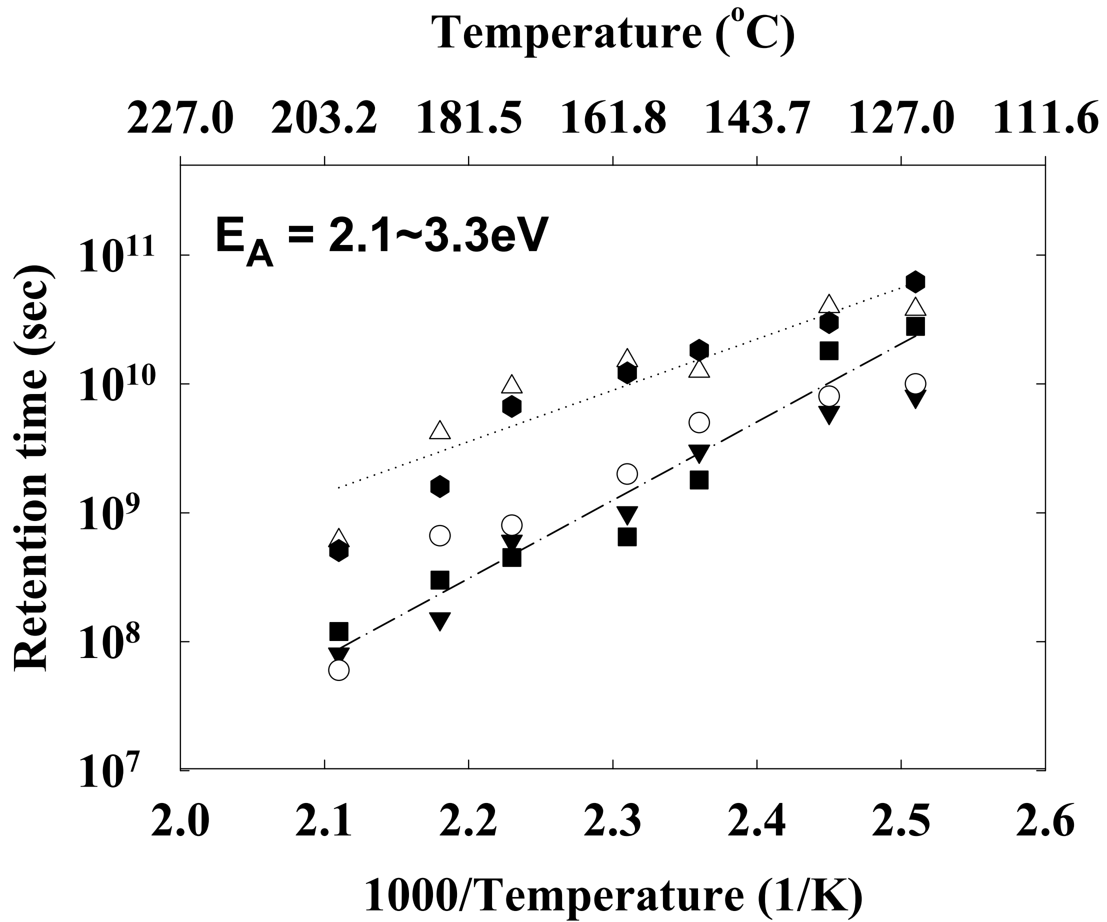

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Fig. 2.12 Activation energy characteristics of the HfO_2 nanocrystal Flash memory cells taken from five samples.

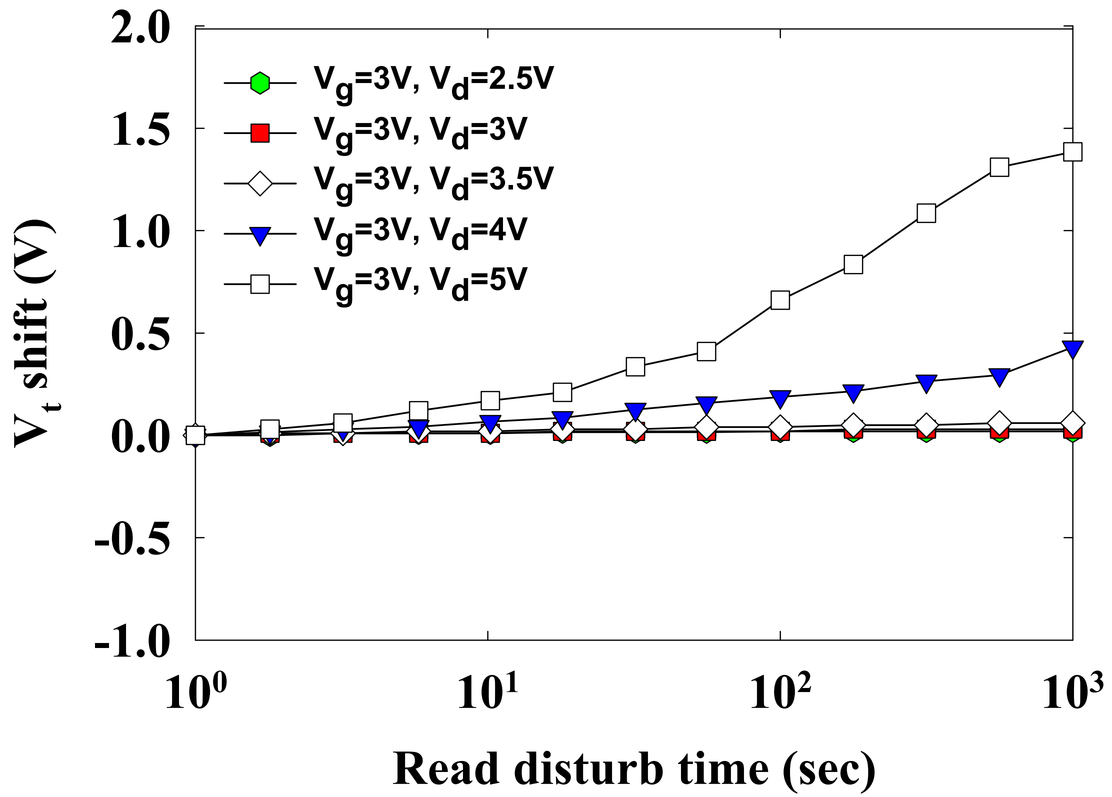

Fig. 2.13 Read disturbance characteristics of the HfO_2 nanocrystal memory devices. No significant V_t shift occurred for V_d < 4, even after 1000 s at 25 °C.

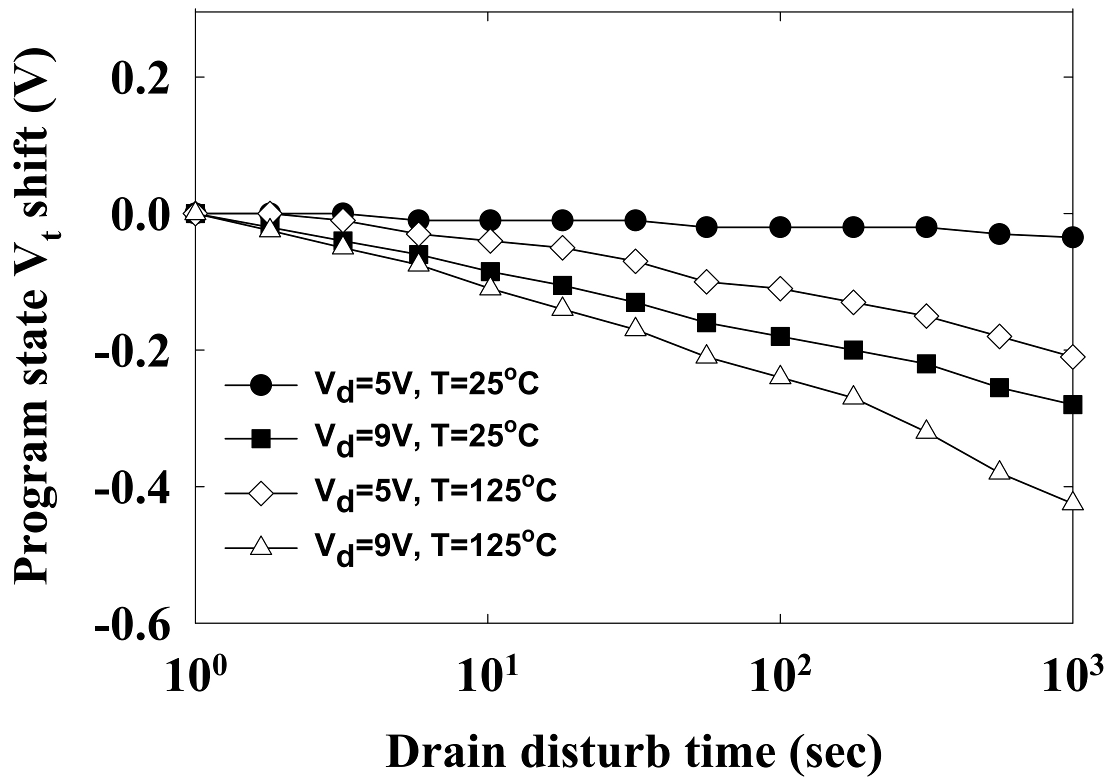

Fig. 2.14 Drain disturbance characteristics of the HfO_2 nanocrystal memory cells. After 1000 s at 25 °C, only a 0.3V drain disturb margin was observed.

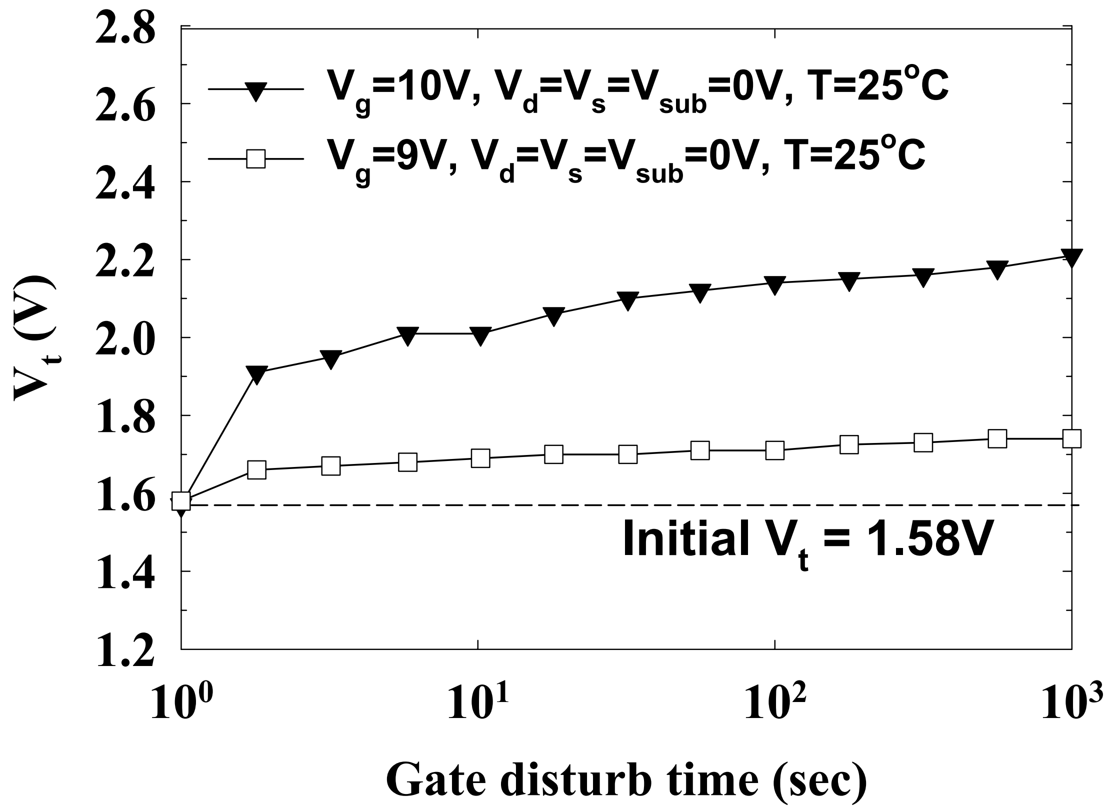

Fig. 2.15 Gate disturbance characteristics of the HfO_2 nanocrystal memory devices. A threshold voltage shift of only 0.22 V occurred after stressing at V_g = 9 V and V_s = V_d = V_{sub} = 0 V for 1000 s.

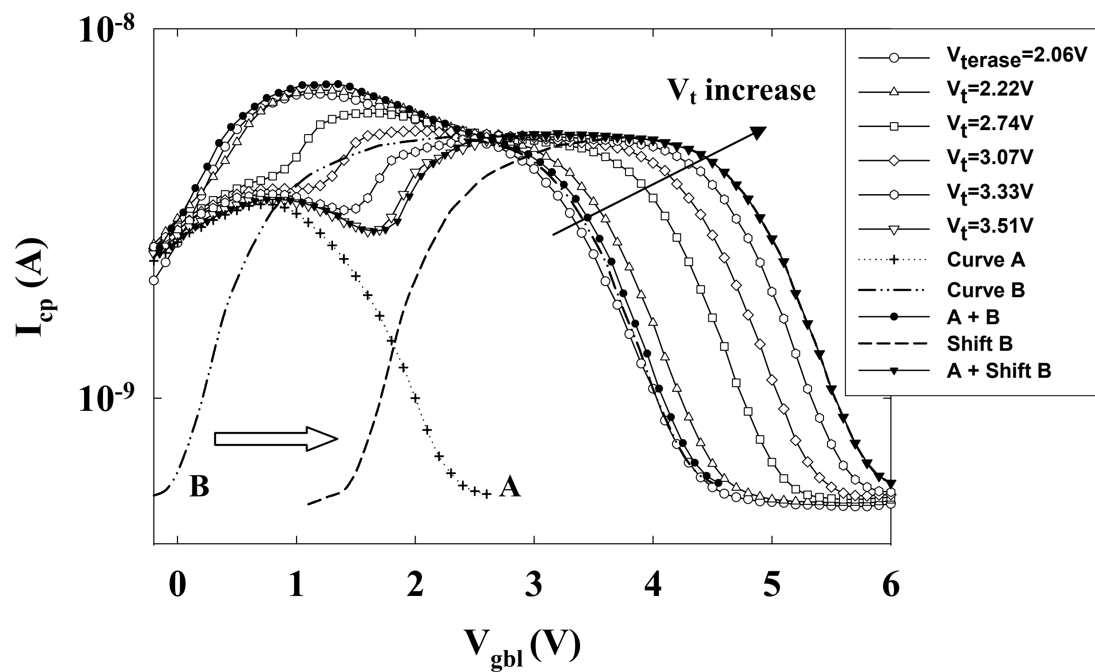

Fig. 2.16 Plots of I_{cp} vs V_{gbl} for the HfO_2 nanocrystal memory cell after F–N programming to different V_t levels.

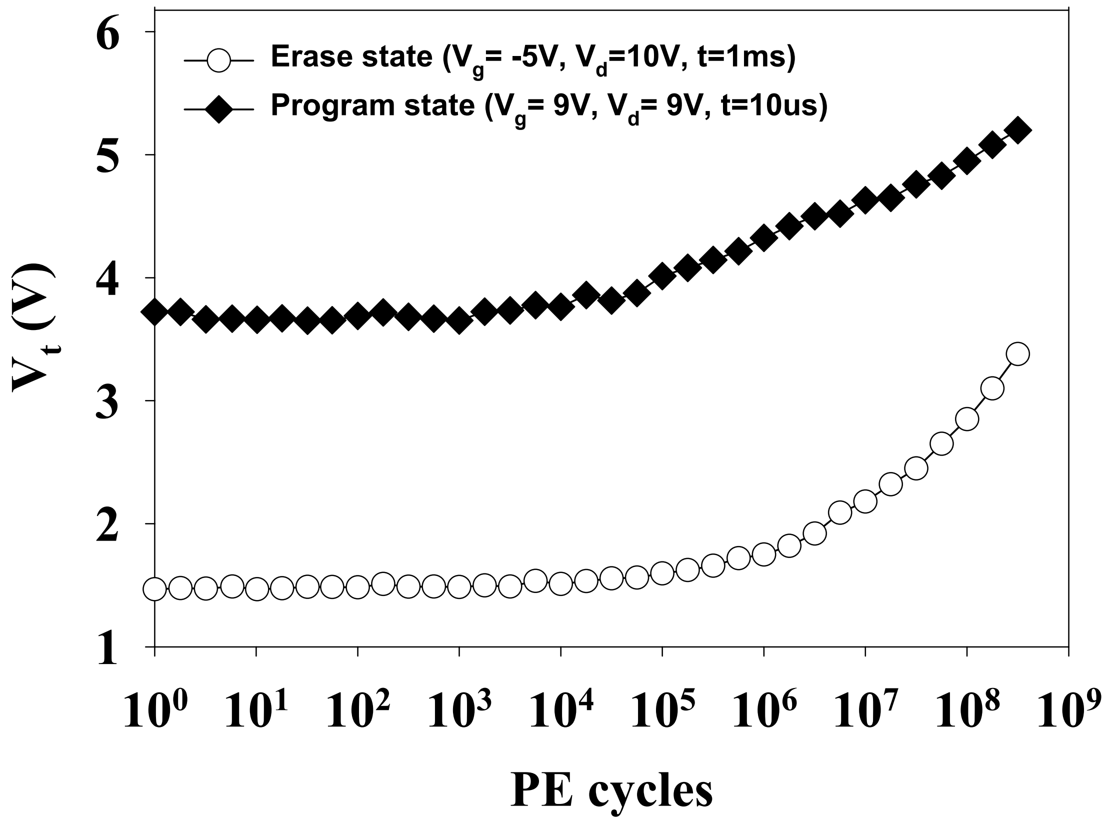

Fig. 2.17 Endurance characteristics of the HfO_2 nanocrystal memory after 10k P/E cycling.

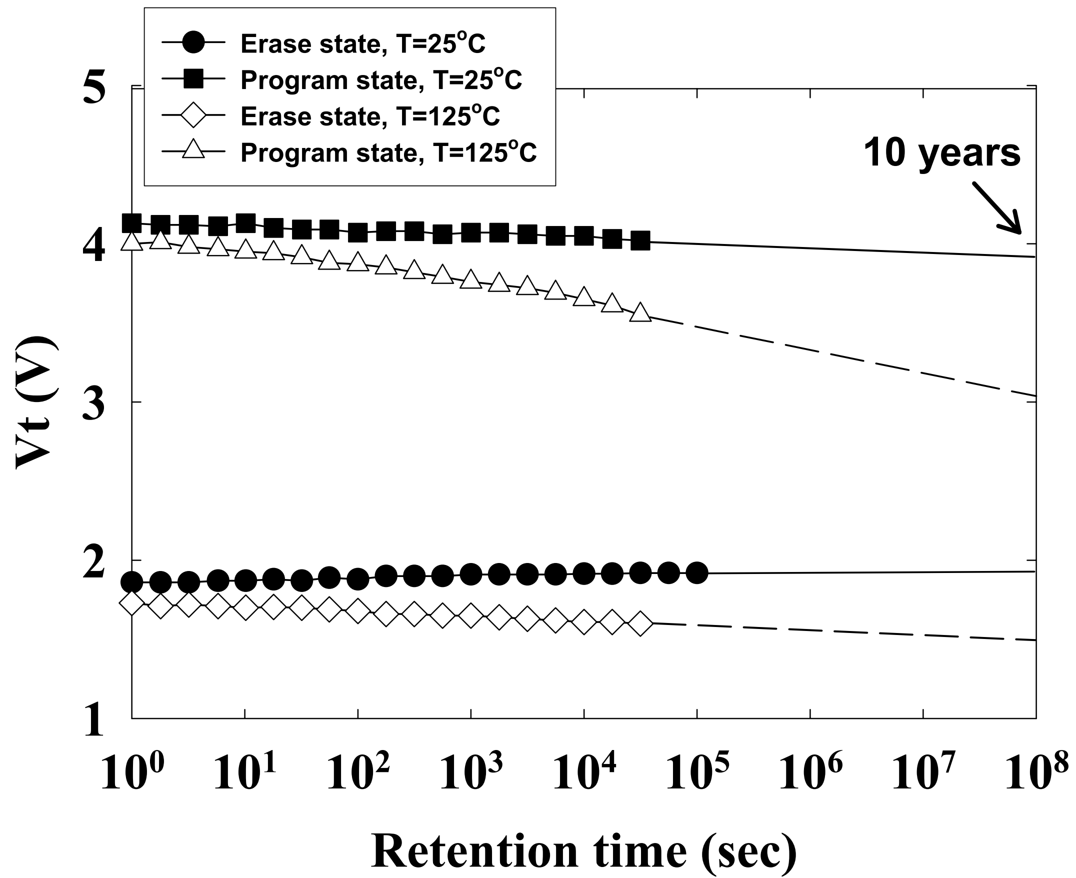

Fig. 2.18 Retention characteristics of the HfO_2 nanocrystal memory after 10k P/E cycling at 25 and 125 °C. No significant charge loss occurred at 25 °C; and only a very low charge loss occurred at 125 °C.

	Memory windows (volts)	20% charge loss at RT (sec.)	Write/ Erase speed (sec.)	Migration
This Work	1.2V ~ 5V	$>10^{8}$	P:$>10^{-6}$ E:$>10^{-4}$	No migration
HfO2 [8]	1.5V ~ 4V	$>10^{5}$	P:$>10^{-6}$ E:$>10^{-4}$	Lateral
Si dots [2]	0.5V ~ 2.2V	$>10^{8}$	P:$>10^{-6}$ E:$>10^{-1}$	N/A
Metal dots [5]	1V ~ 7V	$>10^{6}$	P:$>10^{-3}$ E:$>10^{-3}$	N/A
SONOS [8]	1.2V ~ 5.2V	$>10^{8}$	P:$>10^{-6}$ E:$>10^{-5}$	Vertical

Table 2.4 Memory characteristics of the device fabricated in this study and the comparison with reported data for various SONOS-type memory cells.

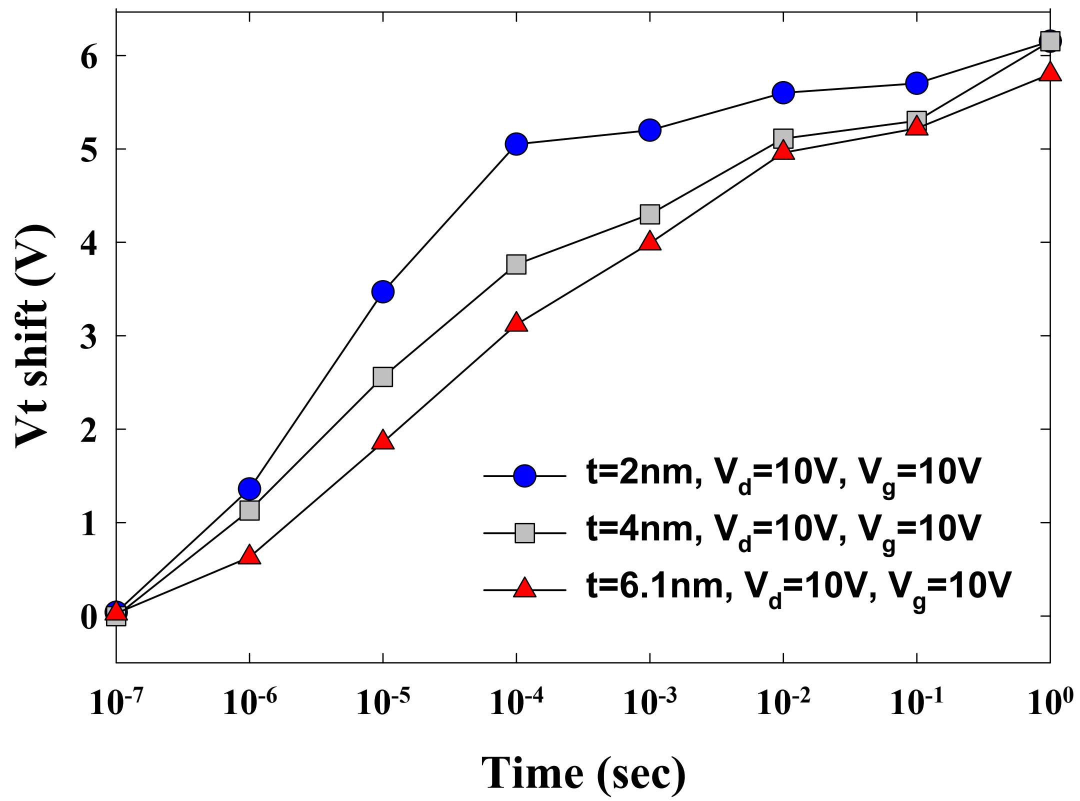

Fig. 2.19 Program characteristics of HfO_2 nanocrystal memory devices with different tunnel oxide thickness for different programming conditions

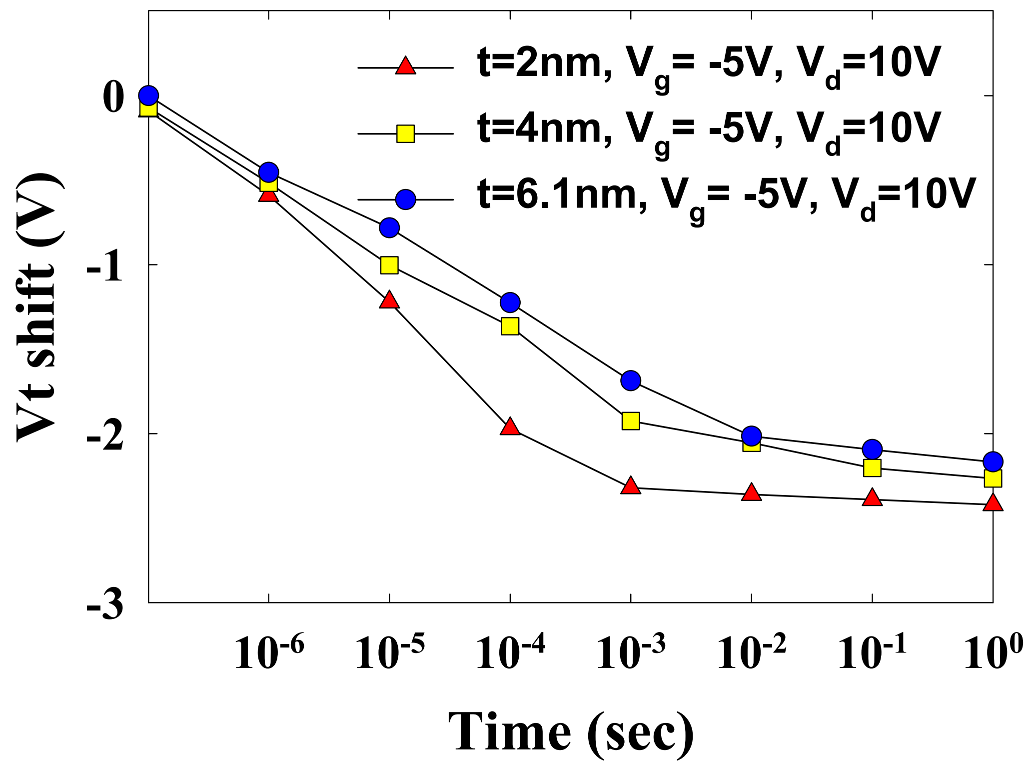

Fig. 2.20 Erase characteristics of HfO_2 nanocrystal memory devices with different tunnel oxide thickness for different programming conditions

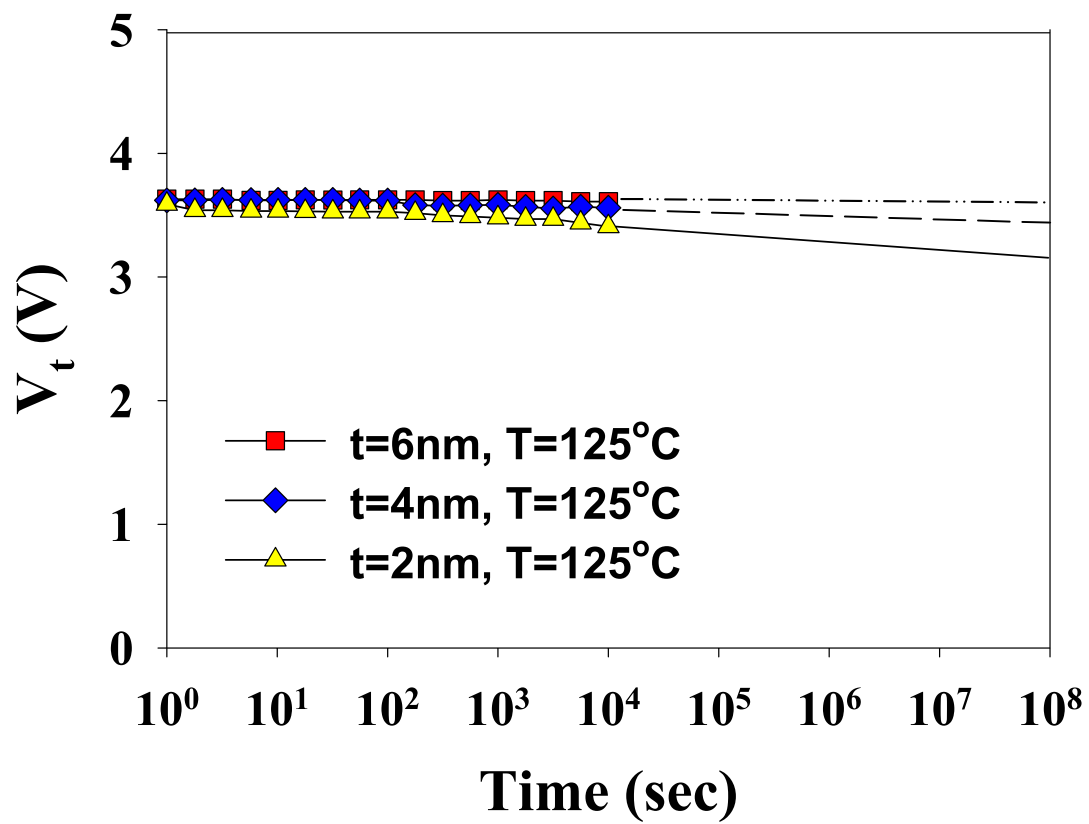

Fig. 2.21 Retention characteristics of HfO_2 nanocrystal memory devices at 125°C with different tunnel oxide thickness.

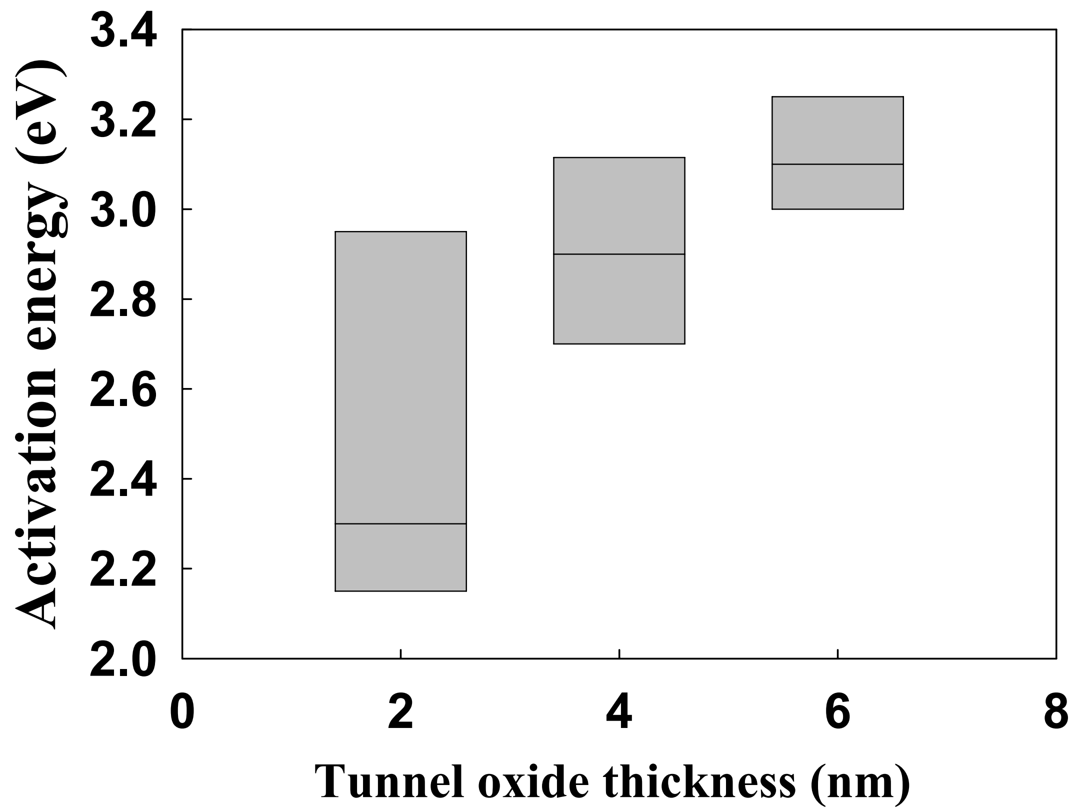

Fig. 2.22 The activation energy of the traps in the HfO_2 nanocrystals for the fresh device with different tunnel thickness

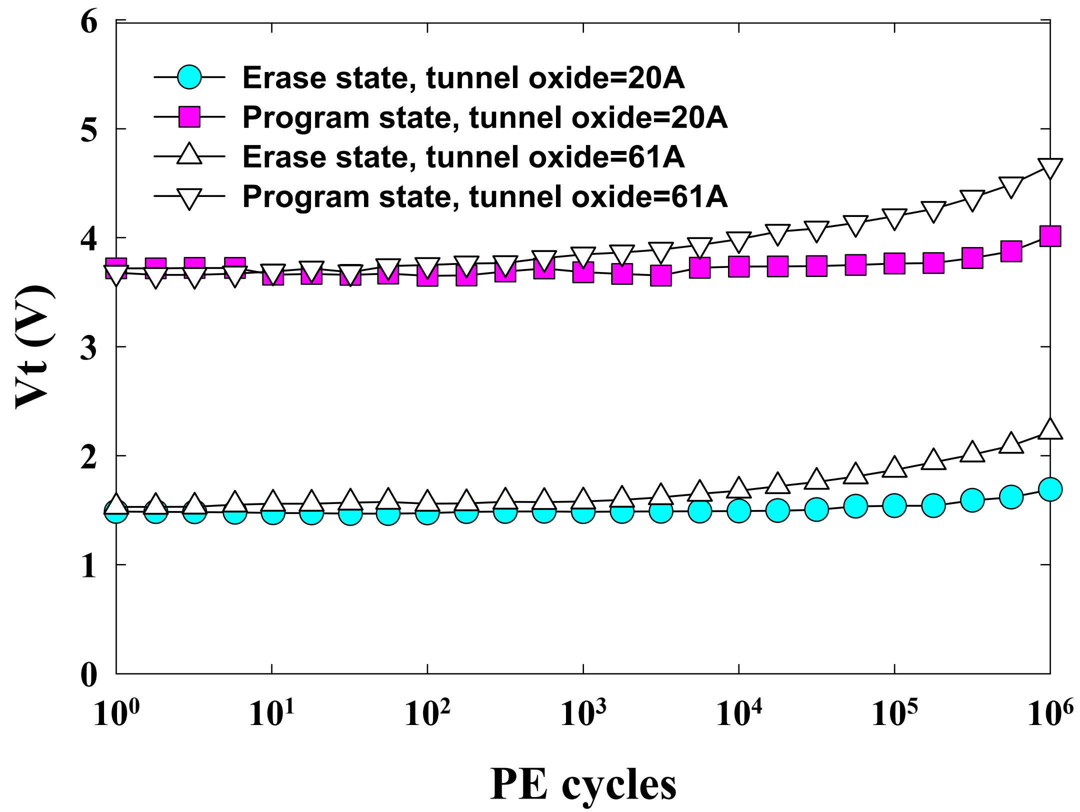

Fig. 2.23 Endurance characteristics of HfO_2 nanocrystal memory devices with different tunnel oxide thickness.

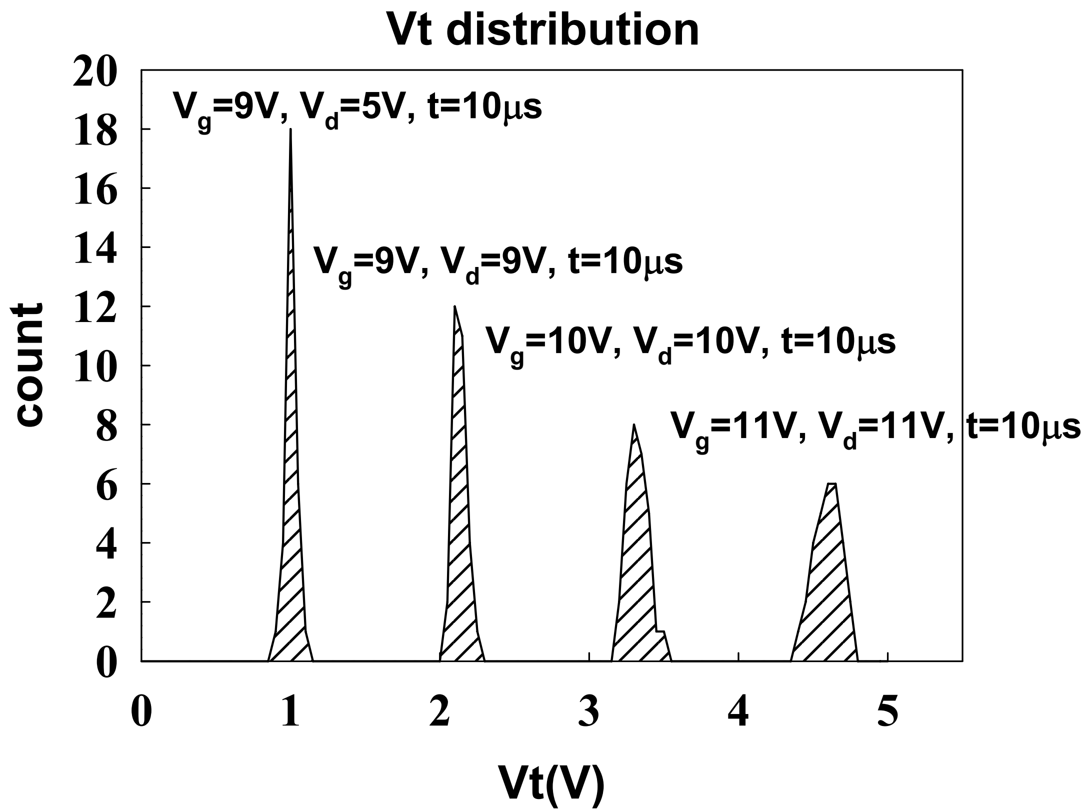

Fig. 2.24 Four-level threshold voltage (V_{th}) distribution of multilevel programming.

Chapter 3

Annealing Temperature Effect on the Performance of Nonvolatile HfO_2 SONOS-type Flash Memory

3.1 Introduction

SONOS-type (poly-Si-oxide-nitride-oxide-silicon) Flash memories have recently attracted much attention for the application in the next-generation nonvolatile memories [3.1]. Based on discrete storage nodes, the SONOS-type Flash memories have grand potency for achieving high program/erase speed, low programming voltage, low-power performance, large memory window, excellent retention, endurance, and disturbance characteristics [3.2-3.6]. Hafnium oxide (HfO_2) is considered to be a promising candidate for the charge trapping layer for the SONOS-type Flash memory instead of Si_3N_4 film [3.7]. The high-κ dielectric film, HfO_2, is expected to have better charge trapping characteristics than the conventional Si_3N_4 films for sufficient density of trap states and deep trap energy level to achieve longer retention time [3.8-3.9]. This feature makes HfO_2 be more helpful in scaling the tunnel oxide for enhancing the performance and more suitable for the development of the SONOS-type memory with multi-bit operation [3.10-3.11]. However, using HfO_2 film as the trapping layers has the issue of lateral migration of trapped electrons and then leads to degraded retention [3.12].

In this chapter, we investigated the performances of the HfO_2 SONOS-type Flash memories by changing post-deposition annealing temperatures for the HfO_2 trapping layer. Besides, we show the high-κ dielectric film such as HfO_2 can trap electron and

hole for the trapping characteristics.

3.2 Experimental

The fabrication process of the HfO_2 SONOS-like Flash memory is shown in Figure 3.1. A 2nm direct tunneling oxide was thermally grown on a (100)-oriented p-type Si substrate. A 5nm amorphous HfO_2 layer was subsequently deposited by electron beam evaporation method with pure Hafnium dioxide (HfO_2) (99.9% pure) targets. Next, the samples were subject to rapid thermal annealing (RTA) through N_2 gas at 600 °C and 900 °C for 1 min. A blocking oxide of about 8nm was then deposited by PECVD followed by poly-Si deposition and gate patterning to complete the gate stack formation of the HfO_2 SONOS-type Flash memory devices.

3.3 Results and Disscussion

3.3.1 Devices Operation

Figure 3.2 and figure 3.3 show the programming and erasing characteristics, respectively, with different pulse widths for the HfO_2 SONOS-type Flash memories with different post-HfO_2-deposition annealing temperatures. All devices described in this paper had dimensions of L/W = 1/2 µm. We used channel hot-electron injection for the programming with the bias condition at V_g-V_t=7V and V_d=6V and band-to-band hot-hole injection for erasing with the bias condition at V_g-V_t=-6V and V_d=8V [3.13]. Based on the discrete charge storage of HfO_2 tapping layer, the feasibility of two-bit operation can be achieved with proper bias scheme. We can employ forward and reverse reads to detect the information stored in the programmed bit1 and bit2, respectively. This means that we can program one bit and read the information using a reverse read scheme. We have added the table 1 to summarize the

bias conditions for two-bit operation. For the temperature effect, it was clearly observed that the programming speed and the memory window increase when the annealing temperature increases. In addition, with the annealing temperature increases, the erasing speed increases but slight overerasure can be observed [3.14]. We speculate this is due to the crystallization-induced trap generation. As well known, the HfO_2 trapping layers will crystallize after high temperature annealing. The defects along the grain boundaries are thought being able to act as the extra trapping sites and, therefore, larger memory window can be obtained [3.15]. From the results of X-ray Diffraction (XRD) analysis, we did see that the degree of crystallization becomes more significant upon increasing temperature (Fig. 3.4). Since the V_t are 2.7V, 2.2V, and 1.8V for the as-deposited, 600°C-annealed and 900°C-annealed devices, respectively, we then conclude that the generated crystallization-induced traps inside the HfO_2 trapping layer are hole-trap-like, which fact can explain the result shown in Fig. 3.3 that the more severe overerasure upon increasing annealing temperature has been observed. Owing to the nature of discrete charge storage sites in the high-κ gate dielectrics, we can easily achieve 2 bits storage in one single memory device by just reversing source and drain [3.16].

Figure 3.5 illustrates the retention characteristics for all HfO_2 SONOS-type Flash memories. The retention time of the memory with as-deposited HfO_2 trapping layer can be up to 10^8 seconds for 10% charge loss. However, it was significantly degraded as the annealing was employed and the situation became worse as the temperature increased. We have calculated the activation energy of the traps in the HfO_2 nanocrystals for the fresh device. Activation energy tracing is used widely to characterize the Arrhenius relation extracted from the temperature dependence of charge loss in a nonvolatile memory as a function of time. For a given charge–loss threshold criterion (in our case, 20%), the failure rates obtained at higher temperatures

(125–200 °C), and five numbers for every temperature, can then be extrapolated to the nominal operating condition. The extracted activation energies are 2.45, 1.78, 0.96 eV for the as-deposited, 600°C-annealed and 900°C-annealed samples, respectively [3.17]. Therefore, we thought that the post-deposition annealing will induce more traps with shallower energy level in the trapping layer, which give rise to larger memory window and poor charge retention.

The endurance performances after 10^6 P/E cycles are shown in figure 3.6. Again, the rate of memory window narrowing increases upon increasing annealing temperature. As we know, the narrowing is mainly coming from charge gain. Because of the use of ultra-thin tunnel oxide, there is only very minute amount of trapped charges generated during operation in the tunnel oxide [3.18]. Hence, we attribute this to the residual charges along the grain boundaries because these highly localized induced traps are more difficult to remove unless their positions are coincided to overlap with the hot-hole injection. Figure 3.7 shows the vertical charge migration characteristics with applying V_g-V_t=-12V at room temperature 25°C. Consistent with the former result, the vertical charge migration is exacerbated by increasing annealing temperature. With the annealing temperature increases, the more vertical charge loss was found. It can be explained by more leakage path in the grain boundary of crystallized HfO_2 in the high annealing temperature.

3.3.2 Disturbances

Figure 3.8 shows the read disturb induced erase-state threshold voltage instability in a localized HfO_2 SONOS-type Flash memory cell for three samples. To allow for two-bit operation, the applied bitline voltage in reverse-read scheme must be sufficiently large (>1.5V) for being able to “read-through” the trapped charge in the

neighboring bit. Relatively large read bitline voltage may cause unwanted electron injection and then result in a significant threshold voltage shift of the neighboring bit. For our measurement, the gate and drain biases were applied and the source was ground. The results clearly show that almost no read disturbance appear for the low voltage reading operation of V_g -V_t= 3V and V_d = 2.5V in our HfO_2 Flash memory.

Figure 3.9 shows the programming drain disturbance of our HfO_2 SONOS-type Flash memories. The same drain voltages (V_d = 8V) were applied in the programming drain disturbance measurements at room temperature (T = 25°C). Upon the increasing annealing temperature, the more drain disturbances were observed. The storage charge leakage path along the grain boundaries induce more drain disturbances for the annealed devices. After 1000 seconds at 25°C, we have sufficiently drain disturb margin (< 0.3V) for the three annealed samples.

Figure 3.10 shows the gate disturb characteristics in the erasing state. Gate disturbance may occur during programming for the cells sharing a common wordline while one of the celles is being programmed. We measured the gate disturbance with the condition at V_g-V_t=7V and V_d=V_s=V_{sub}=0V for the three annealed samples. With the annealing temperature increases, the more gate disturbances were observed. A large amount trap generates in the high temperature annealing that induces more gate disturbances for the annealed devices. Only 0.5V threshold voltage shift has been observed for the 900ºC annealed devices after 1000 seconds stressing. Such good gate disturb characteristic with such thin tunnel oxide can be explained by using serial capacitor voltage divider model with small voltage drop at the tunnel oxide. In summary, we have good read, drain and gate disturbances for the as-deposited, 600°C-annealed and 900°C-annealed samples.

3.3.3 Charge pumping characteristics

The charge pumping (CP) measurement was used to investigate the characteristics of our HfO_2 Flash memory. We used a trapezoidal gate pulse having a fixed pulse amplitude with a varying V_{gbl}. The substrate current (the so-called "charge pumping current," I_{cp}) as a function of V_{gbl} was measured. The gate pulse have a frequency of 1 MHz and a 50% duty cycle; the rising and falling times were both 2 ns. Fig. 2.11 shows plots of the program state charge pumping current I_{cp} versus V_{gbl} for our HfO_2 nanocrystal memory cell. Fowler–Nordheim tunneling was used to program the cell with V_t levels from 2.20 to 3.55 V. The program state I_{cp} curve shifted increasingly toward the right upon increasing the value of V_t as a result of an increase in the amount of injected charge in the HfO_2 trapping layer. So, we conclude that HfO_2 can behave as an charge trapping centers for our SONOS-type Flash memories.

3.4 Summary

In this chapter, we have investigated the effect of post-deposition annealing temperature on the performance of the resultant HfO_2 SONOS-type Flash memories. Higher temperature treatment can have large memory windows due to the crystallization-induced trap generation whereas lead to poorer retention and endurance performances. Moreover, we found that the HfO_2 trapping layer can trap both electrons and holes. No significant read, drain and gate disturbances were observed for three samples. HfO_2 SONOS-type Flash memory is considered to be a promising candidate for the Flash memory devices application.

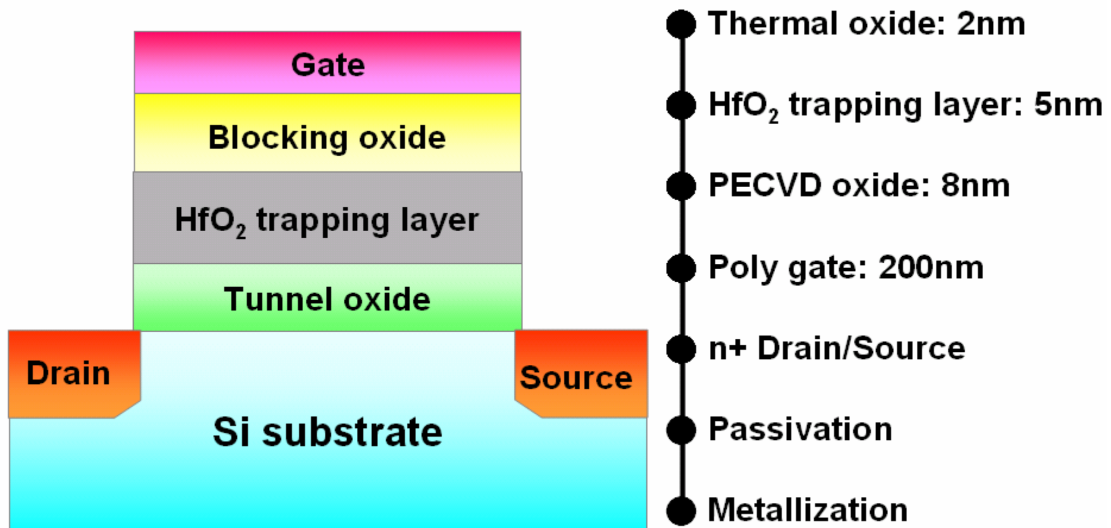

Fig. 3.1 Schematic cross section and process flow of the HfO_2 SONOS-type Flash memory device.

		Program	Erase	Read
Bit 1	V_g-V_t	7V	-6V	3V
	V_d	6V	8V	0V
	V_s	0V	0V	>2V
Bit 2	V_g-V_t	7V	-6V	3V
	V_d	0V	0V	>2V
	V_s	6V	8V	0V

Table 3.1 Operation principles and bias conditions utilized during the operation of the HfO_2 Flash memory cell.

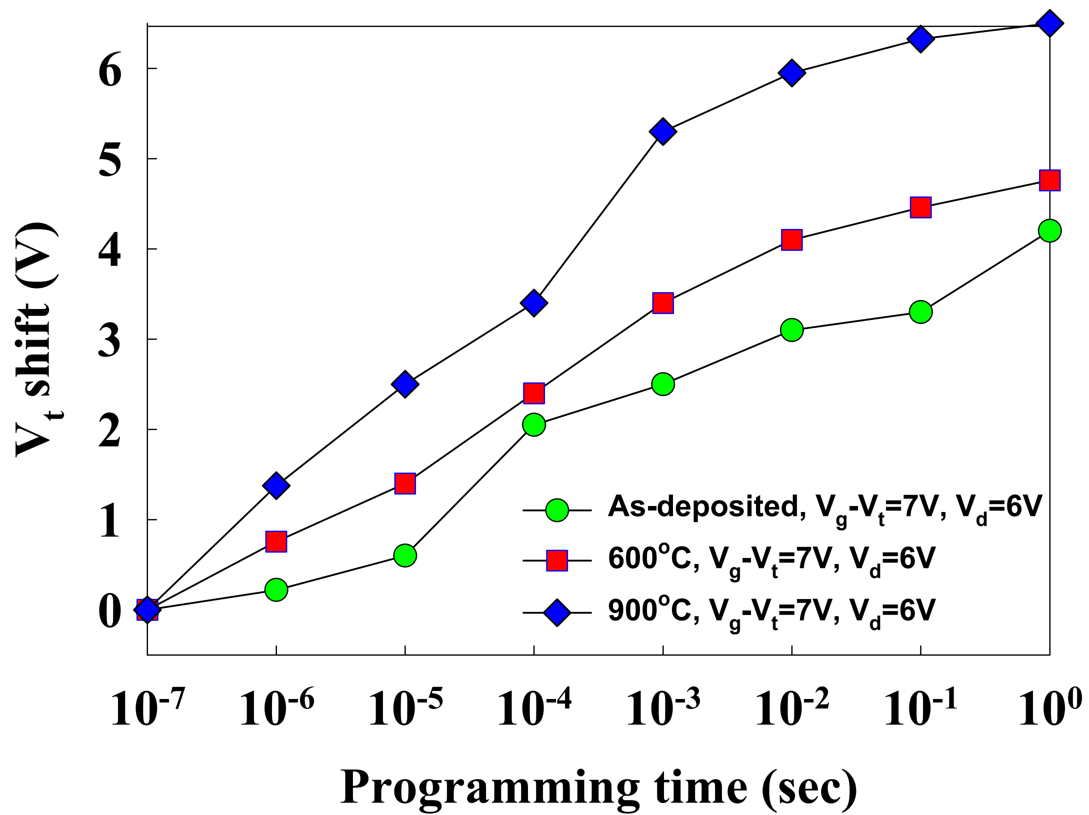

Fig. 3.2 Programming characteristics of the HfO_2 SONOS-type Flash memories. It was clearly observed that the programming speed and the memory window increase when the annealing temperature increases.

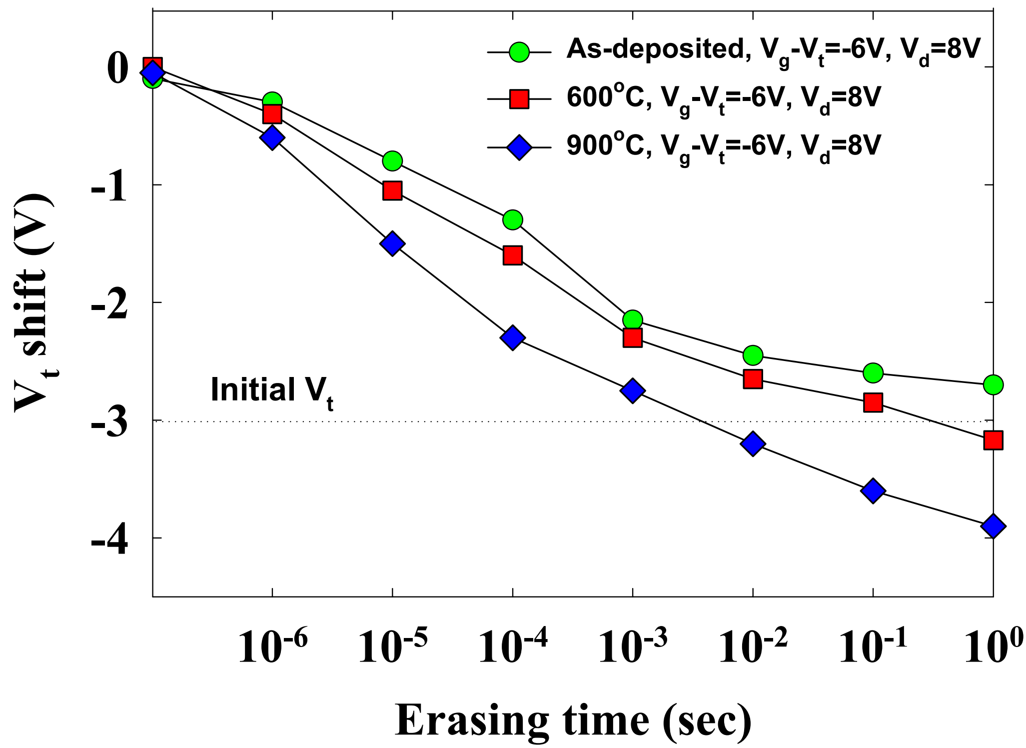

Fig. 3.3 Erasing characteristics of the HfO_2 SONOS-type Flash memories. With the annealing temperature increases, the erasing speed increase and shows little overerasure.

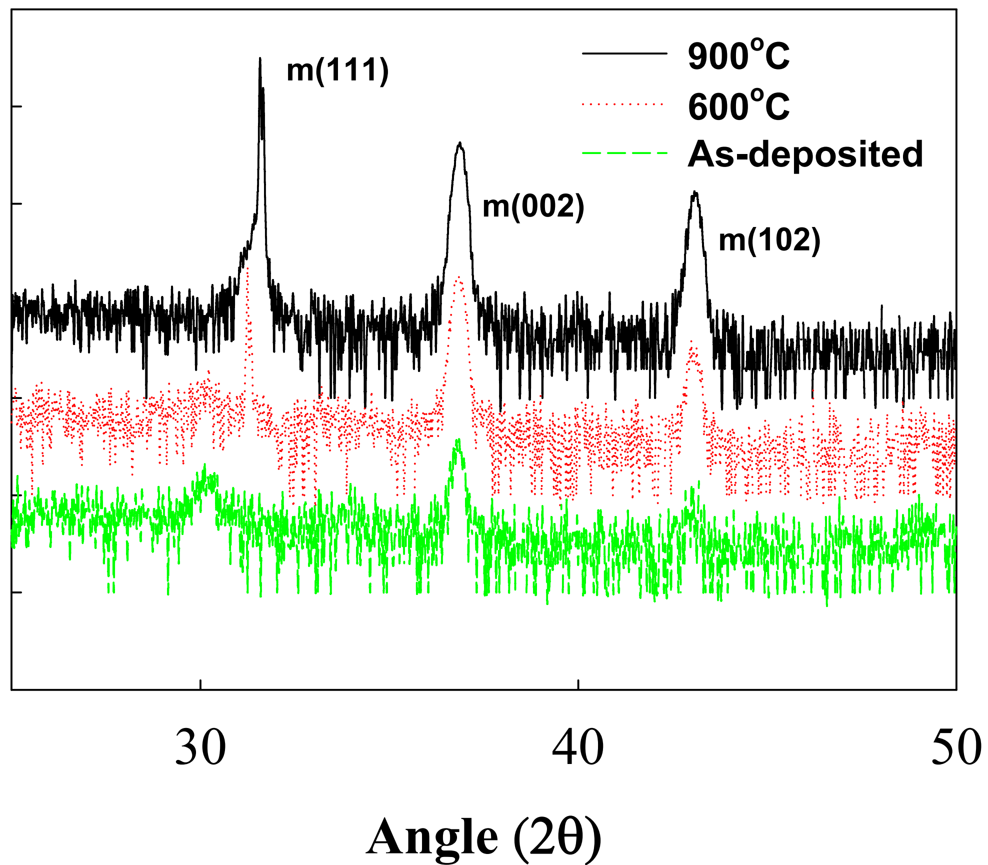

Fig. 3.4 X-ray Diffraction (XRD) analysis of the HfO_2 trapping layer with different temperature.

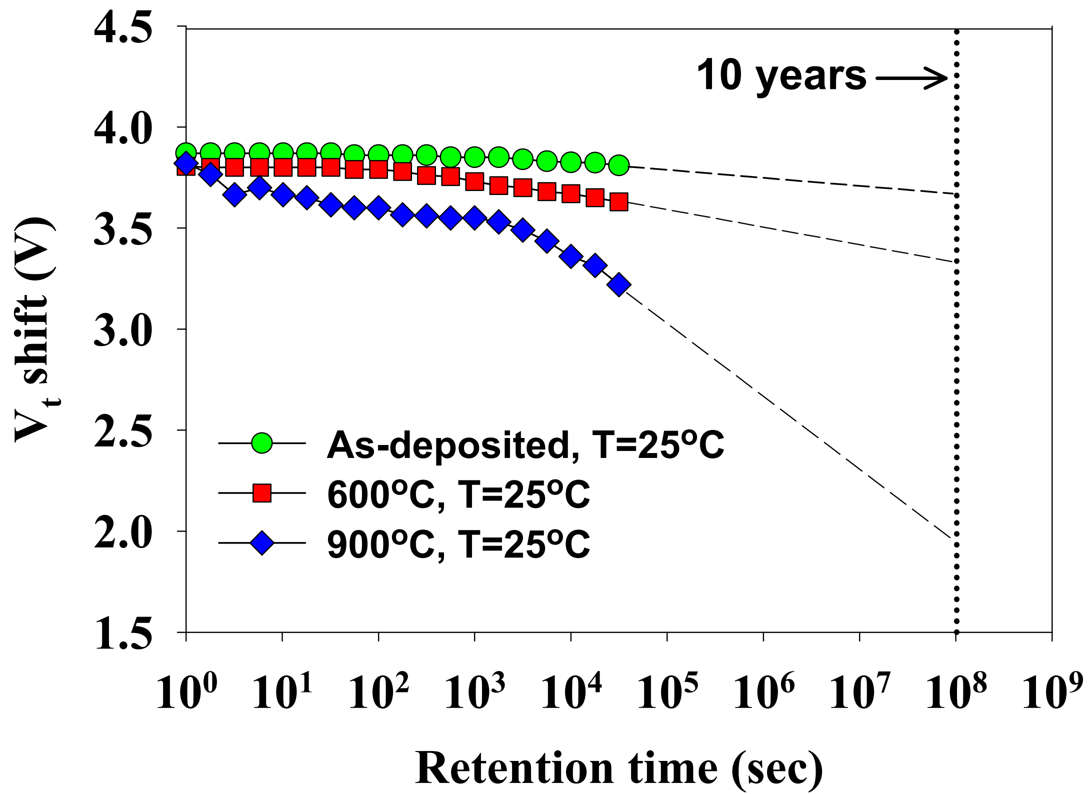

Fig. 3.5 Retention characteristics of the HfO_2 SONOS-type Flash memories at room temperature T=25°C. The 900°C-annealed device shows the worst retention performance.

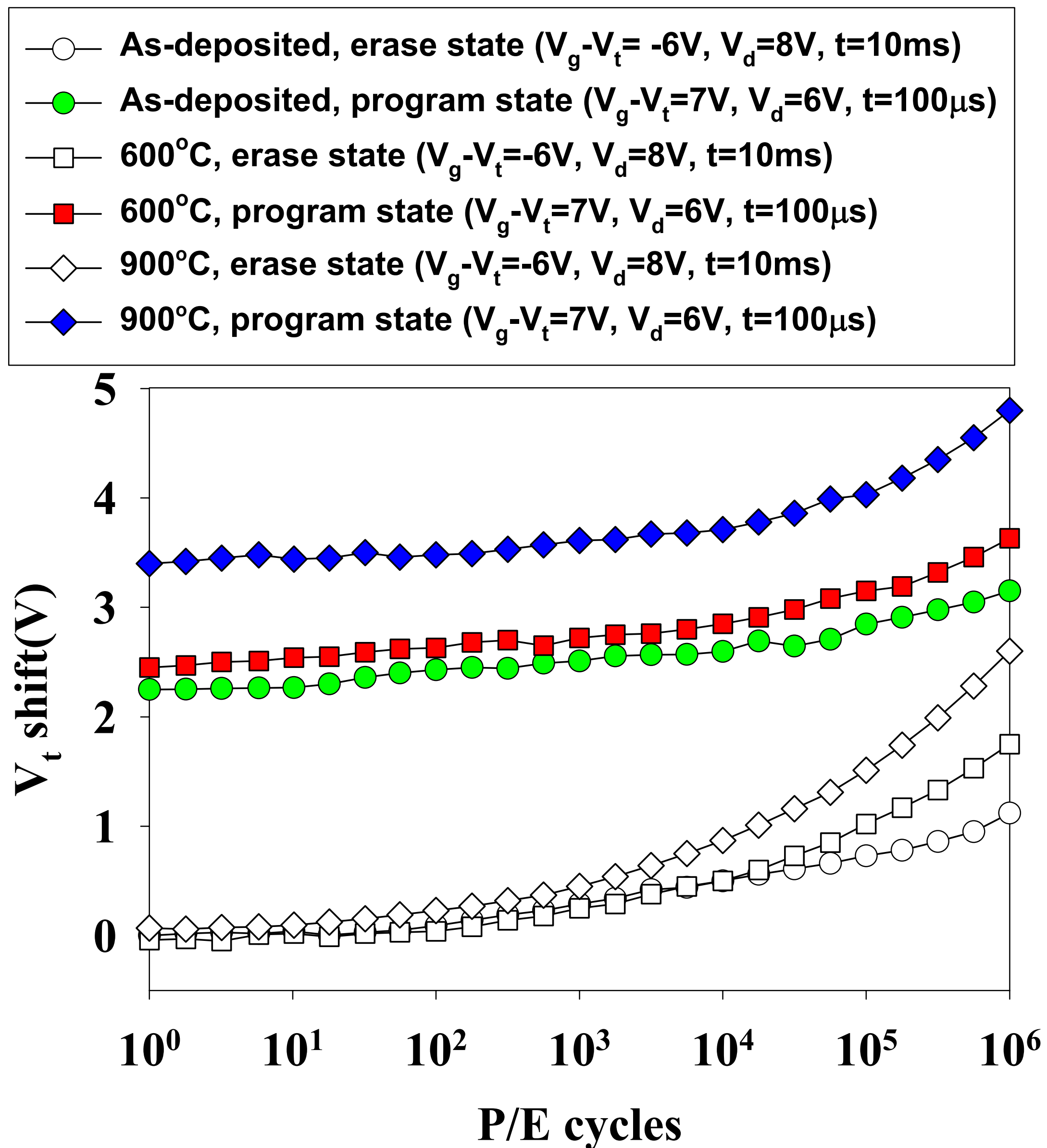

Fig. 3.6 Endurance characteristics of the HfO_2 SONOS-type Flash memories. The 900° C-annealed device shows larger memory window but worse endurance performance in the same condition.

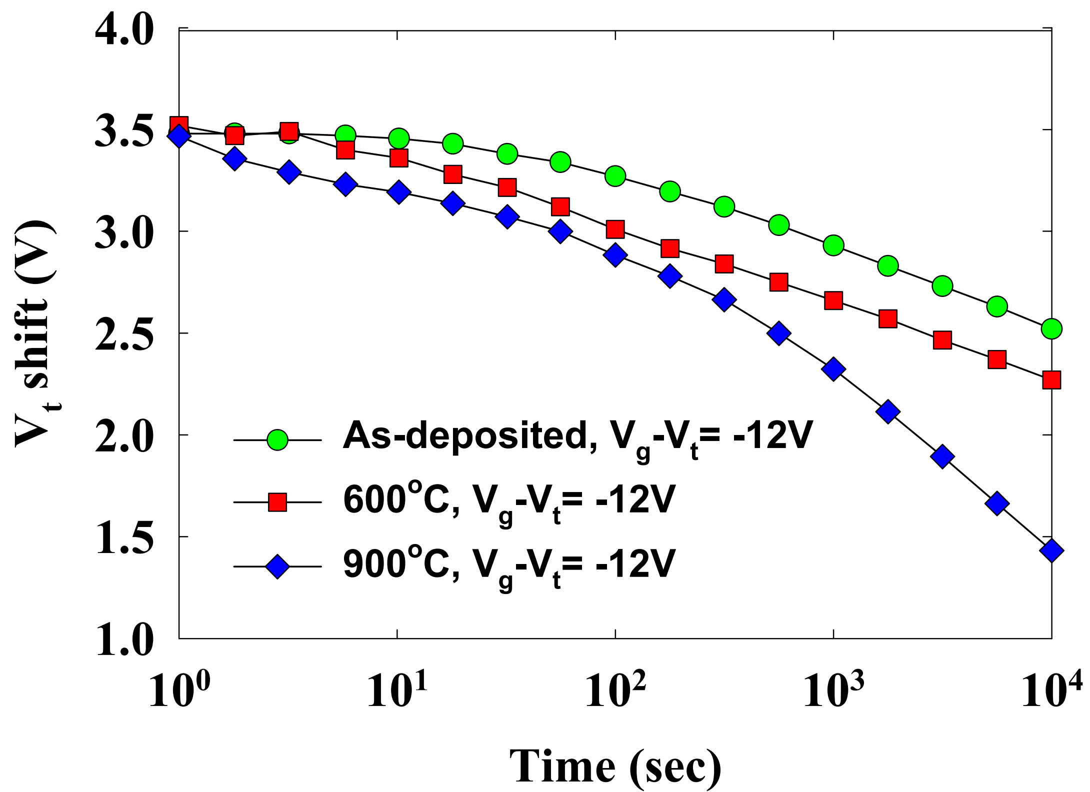

Fig. 3.7 Vertical migration characteristics of HfO_2 SONOS-type Flash memories. Consistent with the former result, the vertical charge migration is exacerbated by increasing annealing temperature.

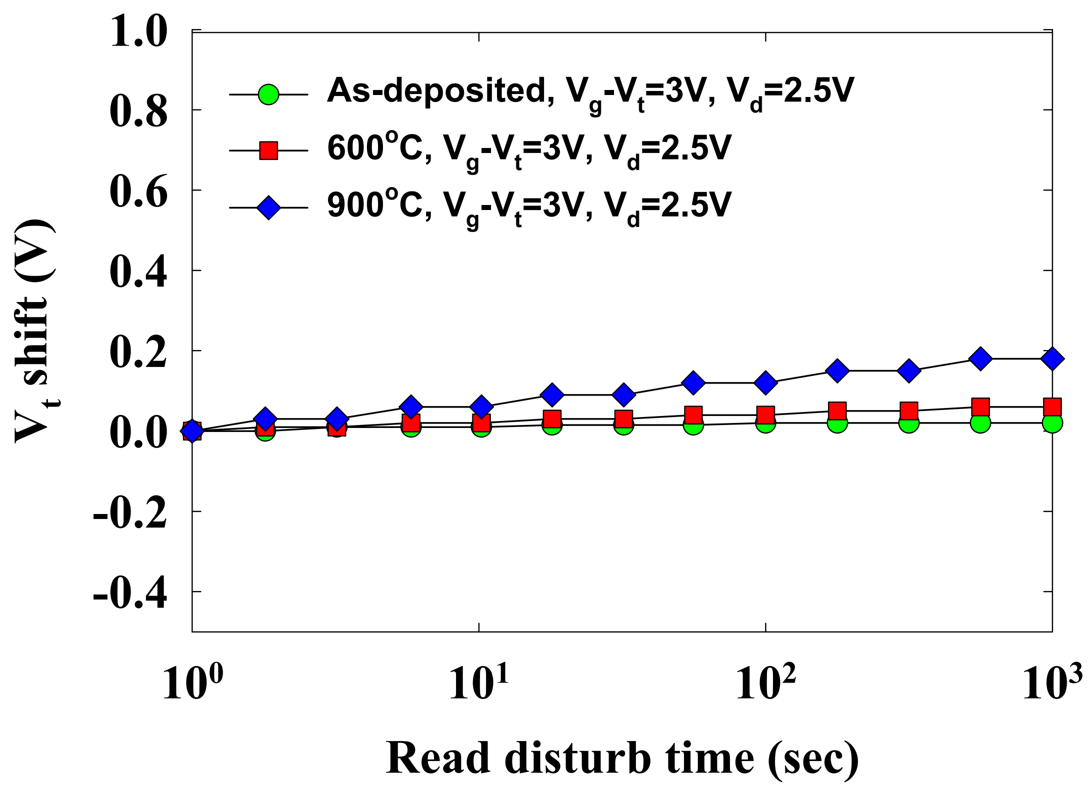

Fig. 3.8 Read disturbance characteristics of HfO_2 SONOS-type Flash memories. No significant V_t shift for all samples even after 1000 seconds at 25°C.

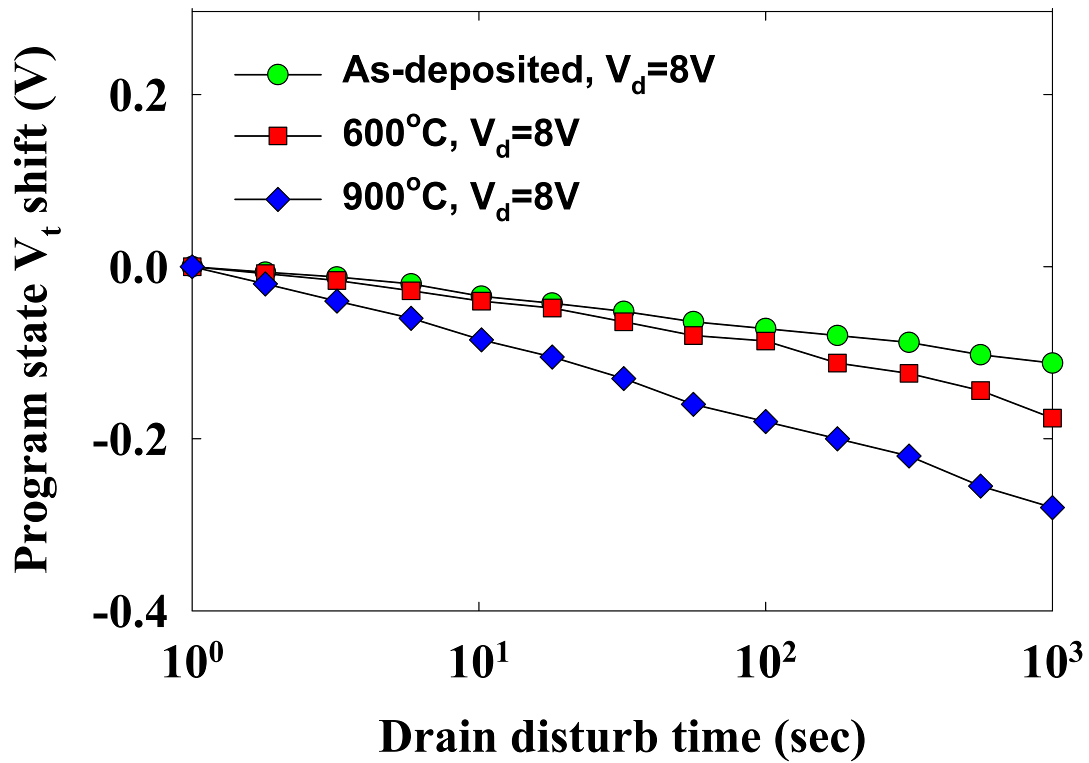

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Fig. 3.9 Drain disturbance characteristics of HfO_2 SONOS-type Flash memories. After 1000 seconds at 25°C, only 0.4V drain disturb margin is observed for the 900ºC annealed devices.

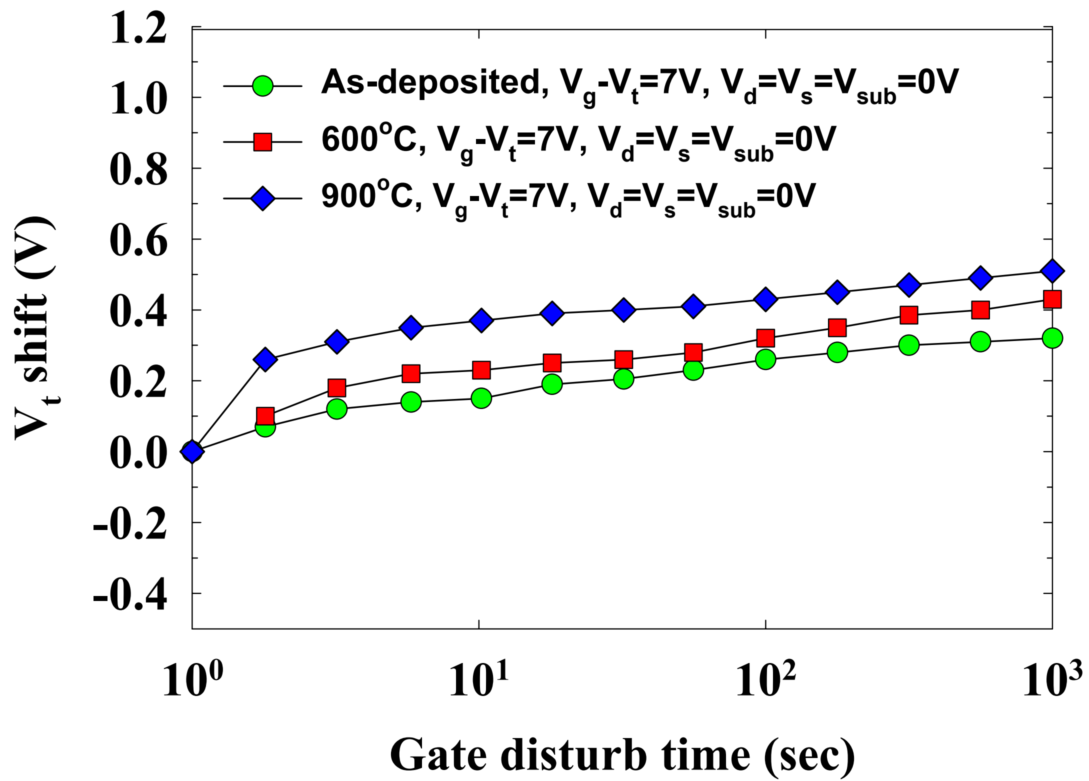

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Fig. 3.10 Gate disturbance characteristics of HfO_2 SONOS-type Flash memories. Only 0.5V threshold voltage shift has been observed for the 900ºC annealed devices after V_g-V_t=7V and V_s=V_d=V_{sub}=0V, 1000 seconds stressing.

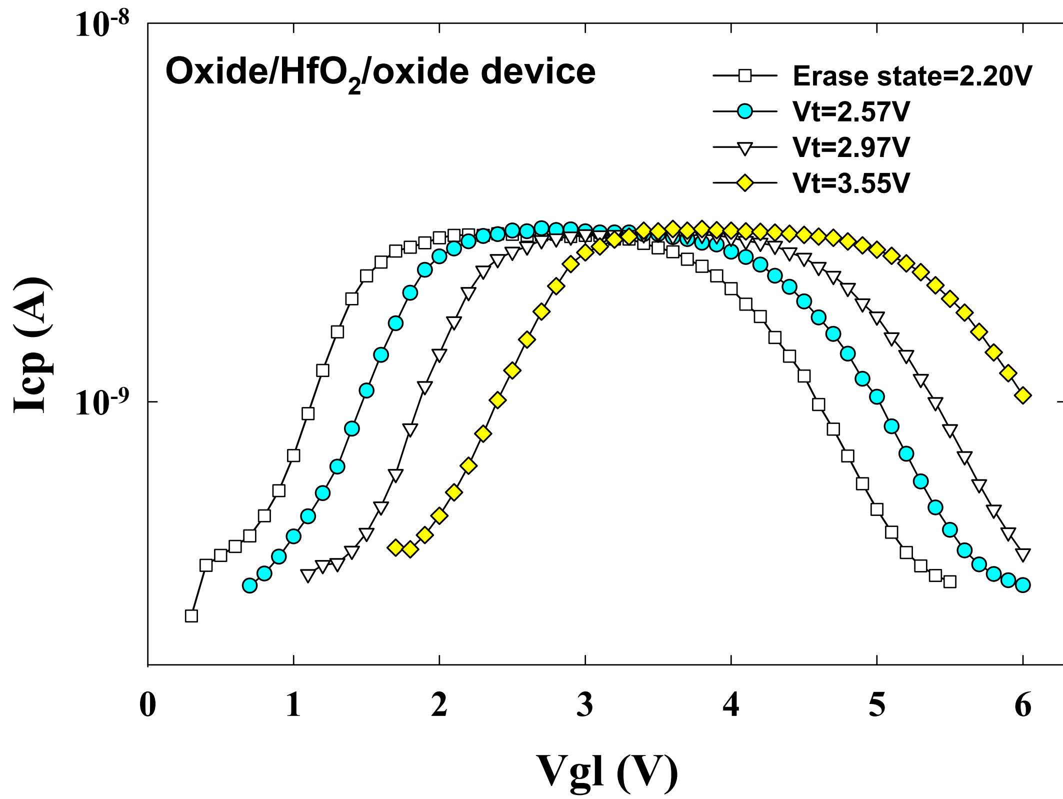


Fig. 3.11 Plots of I_{cp} vs V_{gbl} for the HfO_2 memory cell after F–N programming to different V_t levels.

Chapter 4

Low Temperature Polycrystalline Silicon Thin-Film Flash Memory with High-k Materials

4.1 Introduction

Polycrystalline silicon thin-film transistors (Poly-Si-TFT) have been widely used to integrate driver circuits for the application of AMLCD's [4.1]. With progressive manufacturing technologies, the complexity of circuit integration will continue to increase. Currently, the feasibility of integrating an entire system on top of the panel (SOP) is being actively pursued [4.2]. Since a system shall include the functionality of memory, efforts shall be paid in order to successfully integrate the memories, such as SRAM, EEPROM, and Flash memory, directly on the panel [4.3-4.6]. SONOS (poly-Si-oxide-nitride-oxide-silicon)-type nonvolatile memory based on discrete storage nodes possesses great potential for achieving large memory windows, high program/erase speed, low programming voltage, low-power performance, excellent retention and good disturb characteristics [4.7].

In this chapter, we used three kinds of high-k dielectrics, including HfO_2, Hf-silicate and Zr-silicate for the trapping layer of the poly-Si TFT memory. By employing low thermal cycle (600°C, 24hrs) for post high-κ deposition annealing and S/D activation, the proposed nonvolatile memory fabrication is fully compatible with the current mass-production TFT processing. This makes the realization of producing the embedded nonvolatile memories on the panel becomes feasible.

4.2 Experimental

The schematic diagram of the memory structure is illustrated in Fig. 4.1 First, 500-nm-thick thermal oxide was grown on the Si wafers by furnace system to substitute for the glass substrate and all the experimental devices in this study were fabricated on thermally-oxidized Si wafers. Then, a 100-nm-thick amorphous-silicon layer was deposited on thermally oxidized Si wafer by dissociation of SiH_4 gas in a low-pressure chemical vapor deposition (LPCVD) at 550°C. Subsequently, solid phase crystallization (SPC) was performed at 600°C for 24 hours in N_2 ambient for the phase transformation. Individual active regions were then patterned and defined. After a standard RCA cleaning, two kinds of tunneling oxide thickness were deposited, one is 90-nm-thick TEOS oxide, the other is 200-nm-thick TEOS oxide. The followed by the depositions of three different kinds of high-k dielectrics, including HfO_2, Hf-silicate and Zr-silicate thin films by co-sputtering method. A blocking oxide of about 33nm was then deposited by PECVD at 350°C. A 200-nm-thick poly-Si was deposited to serve as the gate electrode by LPCVD. Then, gate electrode was patterned and the regions of source, drain, and gate were doped by a self-aligned phosphorous ion implantation at the dosage and energy of 5×10^{15} ions/cm^{-2} and 40keV, respectively. After S/D formation, which was activated at 600°C for 24-hr, passivation, metallization and NH_3 plasma sintering were performed to complete the fabrication of the poly-Si TFT memories.

4.3 Results and Discussion

4.3.1 Material Analysis

Figure 4.2 shows the cross-sectional HRTEM images of the gate stacks of the poly-Si-TFT memories. For SONOS-type structure, the thicknesses of the tunnel

oxide and blocking oxide layer are 9nm, 33nm, respectively. The trapping layer thicknesses are 9.8nm, 20.1nm and 13.9nm for the memories with HfO_2, Hf silicate, and Zr silicate, respectively. In addition, from the diffraction patterns, it is found that HfO_2 and Hf silicate samples depict less degree of crystallization than Zr silicate after 600°C, 24hrs dopant activation. For the operation of our poly-Si-TFT memories, we employed channel hot-electron injection and band-to-band hot-hole injection for the programming and erasing, respectively. All devices described in this paper had dimensions of L/W = 1/1.5 μm. Fig. 4.3 demonstrates the feasibility of performing two-bit operation with our poly-Si-TFT memories through a reverse read scheme in a single cell [4.8]. From the I_{ds}–V_{gs} curves, it is clear to see that we can conduct forward and reverse reads to detect the information stored in the programmed Bit1 and Bit2, respectively. We programmed the Bit1 and Bit2 with the bias condition of $V_d = V_g =$ 12V with the programming time of 1ms, and erased the Bit1 and Bit2 with the bias condition of V_d = 10V and V_g = -10V with the erasing time of 10ms. The read operation was achieved using a reverse read scheme with V_d = 1V, V_g = 3.5V. Table 4.1 summarizes the bias conditions for two-bit operation.

4.3.2 Characteristics of three kinds of high-k TFT memories

We compared the characteristics of the three different kinds of high-k TFT memories with different trapping layers for the TFT memories. Program/erase characteristics of the poly-Si TFT memories with HfO_2, Hf-silicate and Zr-silicate trapping layers are shown in figure 4.4 We can see that the program time can be as short as 1ms for a window of 3V with the operation condition of V_g=V_d=12V, and the erase time is about 10ms with V_g=-10V and V_d=10V for the HfO_2 and Zr-silicate cases. While for the split with Hf-silicate, slightly poor performance arises from the

thicker trapping layer. Fig. 4.5 illustrate the retention times for the fresh memories at room temperatur. The memory with Zr-slicate trapping layer depicts the worst retention. However, its retention time can be up to 10^6 s for 20% charge loss at room temperature and 10^4 s for 30% charge loss at 85°C. Such a good retention is believed to be ascribed to the sufficiently deep trap energy level in the high-k dielectrics [4.8]. Besides, the quality of the tunnel oxide can play a strong role in charge retention. Thus, further improvement of the tunnel oxide can be conducted for obtaining better charge keeping capability. Meanwhile, the endurance characteristics after 10^5 P/E cycles for the memories with HfO_2 , Hf silicate and Zr-silicate trapping layers are shown in Fig. 4.6 The programming and erasing conditions are V_g=V_d=12V for 1ms and V_g=-10V, V_d=10V for 10ms for both samples, respectively. Despite the occurrence of significant memory window narrowing, a memory window of about 2V is sustained even after 10^5 P/E cycles. The origin of the narrowing over cycling, mainly coming from the increase of V_t in erased state, might be due to two factors: The first is the mismatch between the localized spatial distributions for injected electrons and holes by using channel hot-electron programming and band-to-band hot-hole erasing. The uncompensated electrons will then cause the V_t to increase gradually over P/E cycling. The other is the stress-induced electron traps generated in the tunnel oxide during cycling. Therefore, in pursuing superior performance in charge storage capability of these new TFT memories, nano-dots formation [4.9], if feasible, and higher quality tunnel oxide are highly recommended.

4.3.3 Comparison of different tunnel oxide thickness

Now, we compared characteristics of the different tunnel oxide thickness samples for hafnium silicate TFT memories. Figure 4.7 shows the programming and erasing

characteristics, respectively, with different pulse widths for the Hf silicate TFT Flash memories for comparing two different tunnel oxide thickness samples. We used channel hot-electron injection for the programming with the bias condition at V_g = 10V and V_d = 10V and band-to-band hot-hole injection for erasing with the bias condition at V_g = 10V and V_d = -10V. For the tunnel oxide thickness effect, it was clearly observed that the programming speed and the memory window increase when the tunnel oxide thickness decreases for the short pulse width. But for long pulse width, the hot carrier saturate and the programming state and erasing state almost have the same memory windows. Figure 4.8 illustrates the retention characteristics for comparing two different tunnel oxide thickness samples for the fresh memory at different temperature. The retention time of the TFT memory with Hf silicate trapping layer can be up to 10^8 seconds for 10% charge loss at room temperature. But the retention got worse as the temperature increased, 29% charge loss and 68% charge loss for the thick and thin tunnel oxide samples have obtained up to 10^8 seconds. We have calculated the activation energy of the traps in the Hf silicate for the fresh device. Activation energy tracing is used widely to characterize the Arrhenius relation extracted from the temperature dependence of charge loss in a nonvolatile memory as a function of time. For a given charge–loss threshold criterion (in our case, 20%), the failure rates can obtained then can be extrapolated to the nominal operating condition. The extracted activation energies are 1.04, 1.33 eV for the 9nm and 20nm samples, respectively [4.10]. Obviously, it is in the higher ranges at those values previously reported for conventional SONOS memories [4.11–4.13]. Therefore, we thought that the thick tunnel oxide sample can be conducted for obtaining better charge keeping capability. Fig. 4.9 illustrates the retention characteristics for comparing two different tunnel oxide thickness samples for the fresh memories both at room temperature (T = 25 °C) and above (T = 125 °C). The same results have been observed formed, the

retention got worse as the temperature increased, and 56% charge loss and 70% charge loss for the thick and thin tunnel oxide samples have obtained up to 10^8 seconds. Thick tunnel oxide sample have better charge keeping capability in the 10k P/E cycled devices.

The endurance performances after 10^5 P/E cycles for comparing two different tunnel oxide thickness samples are shown in figure 4.10. Again, the rate of memory window narrowing increases upon increasing P/E cycling and the thick samples have more memory window narrowing than the thin tunnel oxide samples. As we know, the narrowing is mainly coming from charge gain. Because of the use of thick tunnel oxide, there is only very large minute amount of trapped charges generated during operation in the tunnel oxide.

4.3.4 Disturbance characteristics

Disturbance characteristics are very important reliability characteristics of Flash memory, we showed the characteristics for taking the examples of the hafnium silicate samples. Figure 4.11 is the schematic circuitry of the NOR Flash memory array architectures, some failure phenomenon "disturbance" often takes place under operation when the electrical stress applied to those neighboring cells during programming a specific cell in the array for NOR Flash applications. During programming cell A, drain disturbance occurs in the cell B and same for those cells connected with the same bitline because the drain stress is applied to the same bitline (BL). On the other hand, gate disturbance occurs in the cell C and same for those cells connected with the same wordline because the gate stress is applied to the same wordline (WL). For the cell reading, the unwanted electron injection would happen while the wordline voltage and bitline voltage are under read operation. This

phenomenon would result in a significant threshold voltage shift of our selected reading cell. This is call read disturbance.

For almost all the popular Flash memory array architectures, erase is performed in blocks, and big chunk of devices are erased in one operation, so all the cells on the same bitline should be erased at the same time. In other words, drain disturb is a problem only during programming, when page or byte operations are employed. Moreover, since the bias condition for the disturbed bits is ground gate, with high voltage on the drain, the worst case is the unwanted erase of programmed bits. Figure 4.12 shows the programming drain disturbance of our Hf silicate TFT Flash memories. Two different drain voltages (V_d = 10V and 12 V, V_g=V_s=V_{sub}=0V) were applied at two different tunnel oxide thickness (t = 9nm and 20nm) samples in the fresh and cycled devices. We observed that a sufficient programming drain disturb margin exists (ΔV_t < 0.7 V) in our operation windows (ΔV_t < 3 V), even after programming at a value of V_d of 12V under 10k cycled devices after stressing for 1000 seconds. In particular, the Vt shift increased with the drain disturb time increased. This phenomenon is believed due to the presence of the localized traps along the grain boundaries in the channel, which can significantly affect the Vt shift through drain bias stressing [4.14-4.15]. The charge loss happened in the poly grain boundaries due to the band bending during drain bias stressing, the Vt should be increase that the channel electron charge can overcome the grain boundary sites to turn on the channel. The high voltage drain bias stressing (Vg=12V) have more Vt shift can demonstrate the grain boundaries issues.

For the gate disturbance, the word line for the memory cells in a row is common, when we want to program one of the cells with channel hot electron (such as V_g=10V, V_d=10V), the gate terminals in the other memory devices will also sustain this high voltage. Therefore, programming may lead to the so-called gate disturbance for the

operation. Figure 4.13 shows the gate disturb characteristics in the erasing state. We measured the gate disturbance with the condition at V_g =10V and V_d=V_s=V_{sub}=0V for two different tunnel oxide thickness (t = 9nm and 20nm) samples in the fresh and cycled devices.. Only 0.7V threshold voltage shift has been observed for the 10k cycled devices after 1000 seconds stressing. But opposite to the drain disturbance, the Vt shift decreased with the gate disturb time increased. The same phenomenon for the localized traps along the grain boundaries in the channel affect much for the Vt shift through drain bias stressing [4.14-4.15]. The charge gain happened in the poly grain boundaries of the channel during gate bias stressing, the Vt will be decreasing that the channel will turn on easily because electron charge fill the grain boundary sites. The thinner tunnel oxide sample (t=9nm) has more Vt shift during drain bias stressing (Vg=12V) also can demonstrate the grain boundaries issues. Therefore, to eliminate the traps along the grain boundaries in the channel is another key for achieving better performance.

Figure 4.14 shows the read disturb induced erase-state threshold voltage instability in a Hf silicate TFT Flash memory cell for 10k P/E cycled samples. To allow for two-bit operation, the applied bitline voltage in reverse-read scheme must be sufficiently large (>1V) for being able to "read-through" the trapped charge in the neighboring bit. Relatively large read bitline voltage may cause unwanted electron injection and then result in a significant threshold voltage shift of the neighboring bit. For the TFT memory, such low drain voltage (V_d=1V) can be used for the 2-bit operation because that the depletion region induced in the un-doped poly-Si body is considerably wide, which is able to mask the effect of the stored charge. For our measurement, the gate and drain biases were applied and the source was ground. The results clearly show that almost no read disturbance appear for the low voltage reading operation of V_g = 3V and V_d = 1V and 2V in our 10k P/E cycled TFT Flash

memory.

4.3.5 Channel dangling bonds

With investigating the long-term stability, we found that poly-Si-TFT's reliability characteristics, such as retention, drain and gate disturbance, are intimately related to the density of traps along the grain boundaries of the poly-Si films [4.16], [4.17]. Even though the charge retention capability could be significantly improved by reducing trap density with employing NH_3 plasma treatment [4.18], [4.19], the hydrogenated poly-Si-TFTs still depicted significant and rather unique threshold voltage deviation resulting from drain and gate disturbance. These specific drain and gate disturbance are believed to arise from the breaking of the weak Si-H bonds induced by the acting stresses and the filling of the un-passivated traps by the produced electrons. For comparison of our experiments, NH_3 plasma sintering was performed to complete the fabrication of the poly-Si-TFT memories, but some of comparison samples were not subjected to plasma treatment.

Figure 4.15 shows the retention behaviors of the poly-Si-TFT Flash memories with and without NH_3 plasma treatment. We could clearly see the memory device with NH_3 plasma treatment depicted a better room temperature retention performance than that without NH_3 plasma treatment. This result implies that the hydrogenation by NH_3 plasma treatment is closely related to the charge storage capability of the poy-Si-TFT Flash memories. The retention characteristic of a 10k P/E cycled hydrogenated memory device is also shown for comparison. The charge loss no doubt became worse and started only after few tenths of second due to the induced defects after cycling. This behavior feature was obviously different from that in the case without NH_3 treatment.

In order to clarify the mechanism responsible for this phenomenon, trap state densities (Q_T) of the samples were extracted. Fig. 4.16 exhibits the plots of the $\ln[I_D/(V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ curves at low V_{DS} and high V_{GS}. The Q_T values for the poly-Si-TFTs were estimated by Levison and Proano method [4.20], [4.21] from the slopes of these curves. The hydrogenated poly-Si-TFT exhibits a Q_T value of 1.51×10^{12} cm^{-2}, whereas the non-hydrogenated poly-Si-TFT has the value of 1.74×10^{12} cm^{-2}. To further study the hydrogenated passivation effect near the interface, the effective interface trap states densities (N_T) near the SiO_2/poly-Si interface were also calculated. From the subthreshold swing (S.S.), by neglecting the depletion capacitance, N_T can be expressed as [4.22]:

$$N_T = [(S.S./\ln 10)(q/kT)-1)](C_{ox}/q),$$

where the C_{ox} is the capacitance of the gate oxide. The N_T values of the non-hydrogenated and hydrogenated poly-Si-TFTs are 1.82×10^{12} cm^{-2} and 1.63×10^{12} cm^{-2}, respectively. After 10k P/E cycling, the extracted Q_T value is 2.42×10^{12} cm^{-2} and the N_T value is 2.68×10^{12} cm^{-2}. In Fig. 1, the evolution of Q_T value as a function of time for the sample without NH_3 treatment is also plotted. We found the tendency traced well with the charge loss behavior. In contrast, the Q_T value remains unchanged for the P/E cycled hydrogenated memory device (not shown). These results explain why two different charge loss trends were observed between the non-hydrogenated and the cycled hydrogenated one. In other words, we believe that the surprisingly steep charge loss in the case without NH_3 treatment is caused by the defects at the grain boundaries; while the smooth and early retention degradation of the 10k P/E cycled memory device arises from the combining effects of the generated traps in the bulk of the tunnel oxide and those traps produced near the interface during cycling.

Disturbance is a very important reliability concern for the Flash memories. It

often takes place during programming a specific cell in the NOR Flash memory, which operation leads to the unwanted electrical stress acting on those neighboring cells connected to the same bitline, i.e, drain disturbance, and to the same wordline, i.e., gate disturbance. Fig. 4.17 shows the drain disturb characteristics of the poly-Si-TFT Flash memories in the programmed state. Two different drain voltages were applied, i.e., V_d = 10V and 12V, with the other terminals grounded. For the hydrogenated samples, we observed that a drain disturb (ΔV_t~0.7 V) existed for the cycled memory device under a drain disturb of 12V for 1000 seconds. However, for the non-hydrogenated device the degradation was quite severe. This result is believed due to the presence of the localized traps along the grain boundaries in the channel, which can significantly affect the V_t shift through drain bias stressing [4.23-4.24]. Here, we can confirm our former speculation–the generated traps after cycling locate mostly near the Si/SiO_2 interface rather than at the grain boundaries deep inside the channel [4.25]–since the cycled hydrogenated device depicts higher Q_T value but less significant disturbance. Fig. 4.18 shows the gate disturb characteristics of both fresh hydrogenated and non-hydrogenated memory devices in the erased state with two different tunnel oxide thicknesses (t = 9nm and 20nm). The applied gate voltage was 12V with other terminals grounded. Even though the non-hydrogenated devices again exhibited poorer gate disturb results, the V_t shift decreased rather than increased as the stressing time increased, which is in strong contrast to the situation in the conventional SONOS-type memories [4.26]. Since no cycling had been done for the fresh devices, the decrease in V_t seems unlikely to be caused by the electron detrapping. Thus, we thought this phenomenon is ascribed to the filling of the traps at the grain boundaries by the induced electrons by the applied gate voltage. Moreover, the larger V_t shift in the thinner oxide case is due to the more induced electrons by the higher electric field. These results mean that the defects in the channel not only

significantly influence the data retention but also the drain and gate disturbance of the poly-Si-TFT Flash memories.

4.4 Summary

In this chapter, we have studied three kinds of high-k dielectrics, including HfO_2, Hf-silicate and Zr-silicate for the trapping layer of the poly-Si TFT memory devices with two different thickness tunnel oxides. By sticking with sufficiently low thermal-budget processing, we have successfully demonstrated the feasibility of fabricating nonvolatile poly-Si TFT memories with excellent characteristics in terms of large memory windows, good speed program/erase, long retention time and 2-bit operation. Moreover, the poly-Si grain boundary is the concerned issues about the disturbance characteristics. We demonstrated that the reliability characteristics of a poly-Si-TFT memory device in terms of retention, drain and gate disturbance are closely related to the defects along the grain boundaries in the channel. The NH_3 plasma treatment is one of the useful methods to improve the SiO_2/poly-Si interface and the channel quality because it can effectively eliminate the trap densities in both regions. These poly-Si TFT memories make the realization of producing the embedded nonvolatile memories for system on the panel.

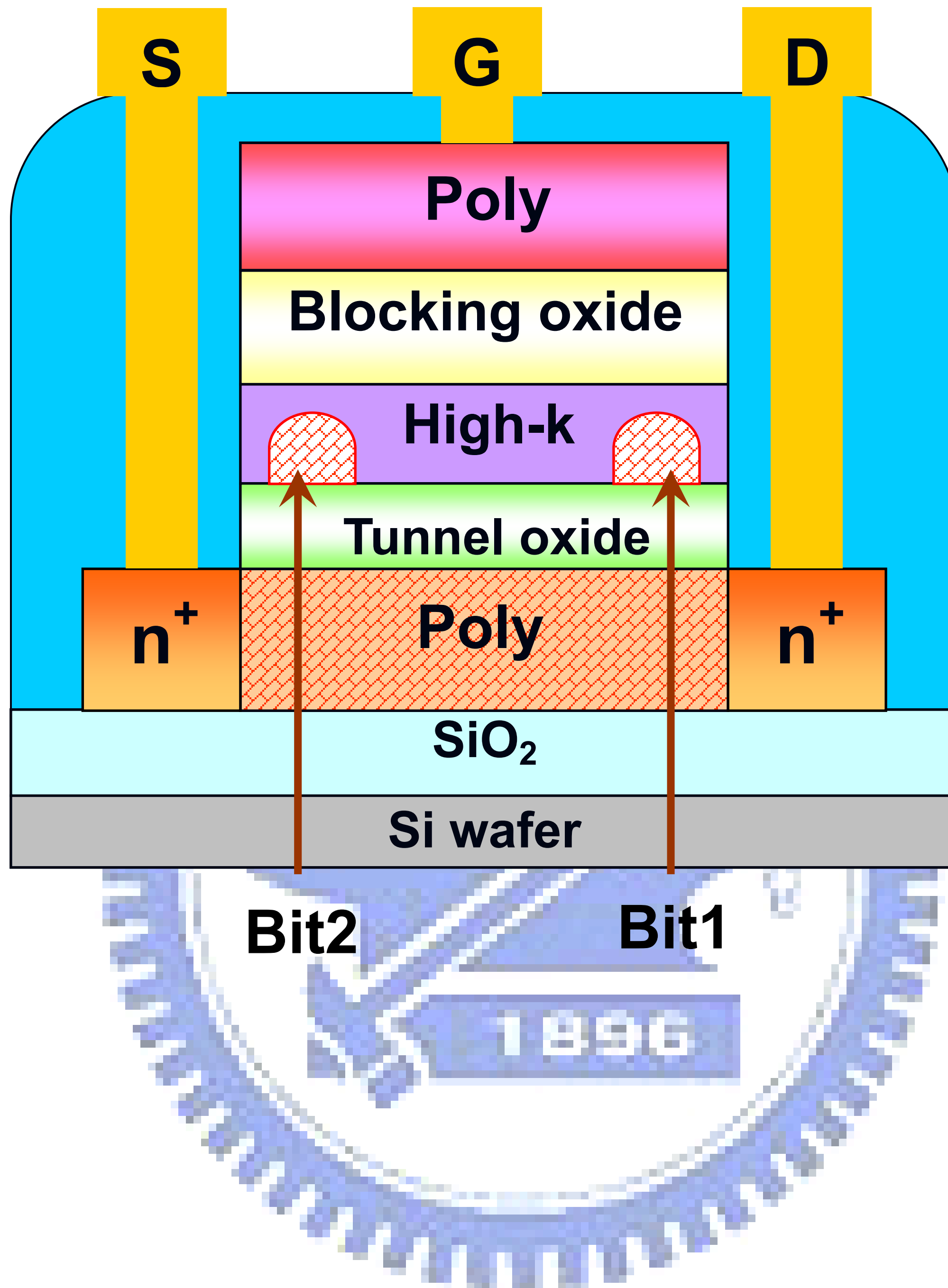


Fig. 4.1 Schematic cross section of the high-κ dielectric poly-Si-TFT nonvolatile memories.

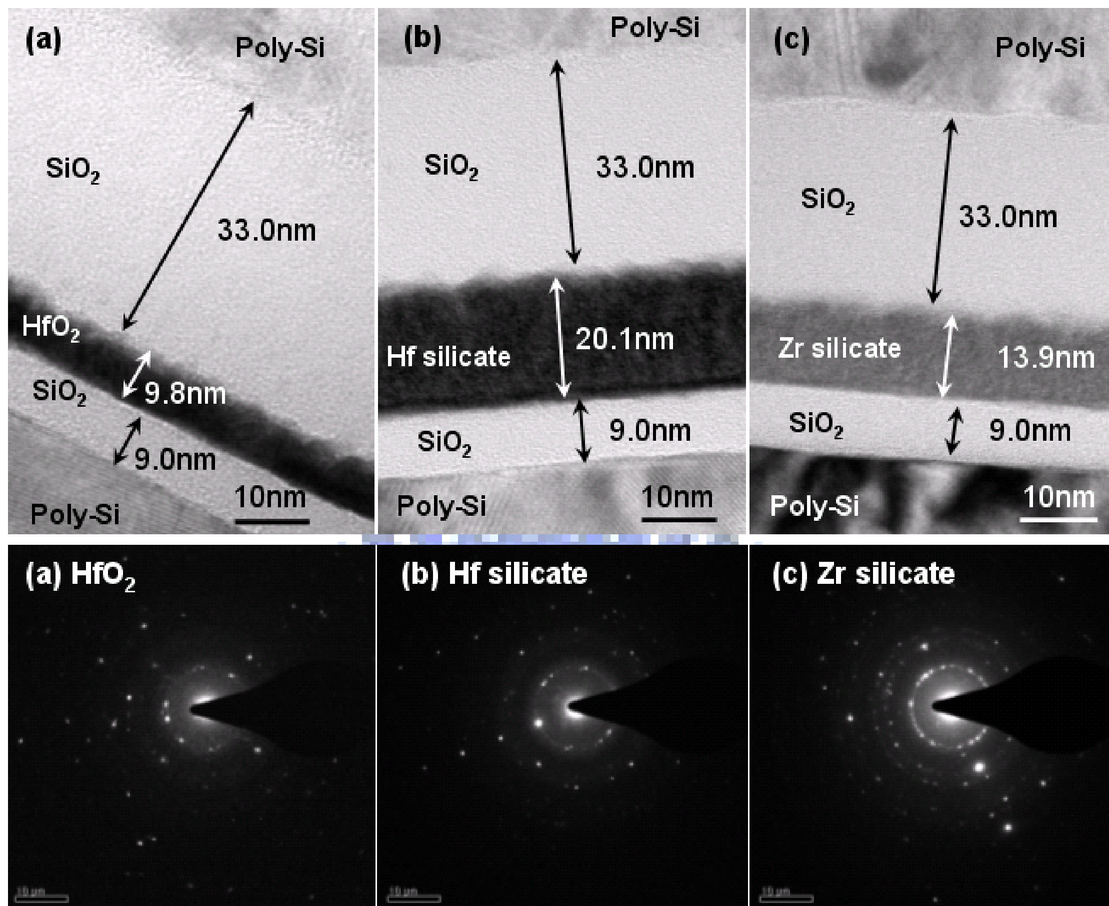


Fig. 4.2 Cross-sectional HRTEM images of the gate stacks for the poly-Si-TFT memories with HfO_2, Hf silicate and Zr silicate trapping layers. The inset show the diffraction patterns of them.

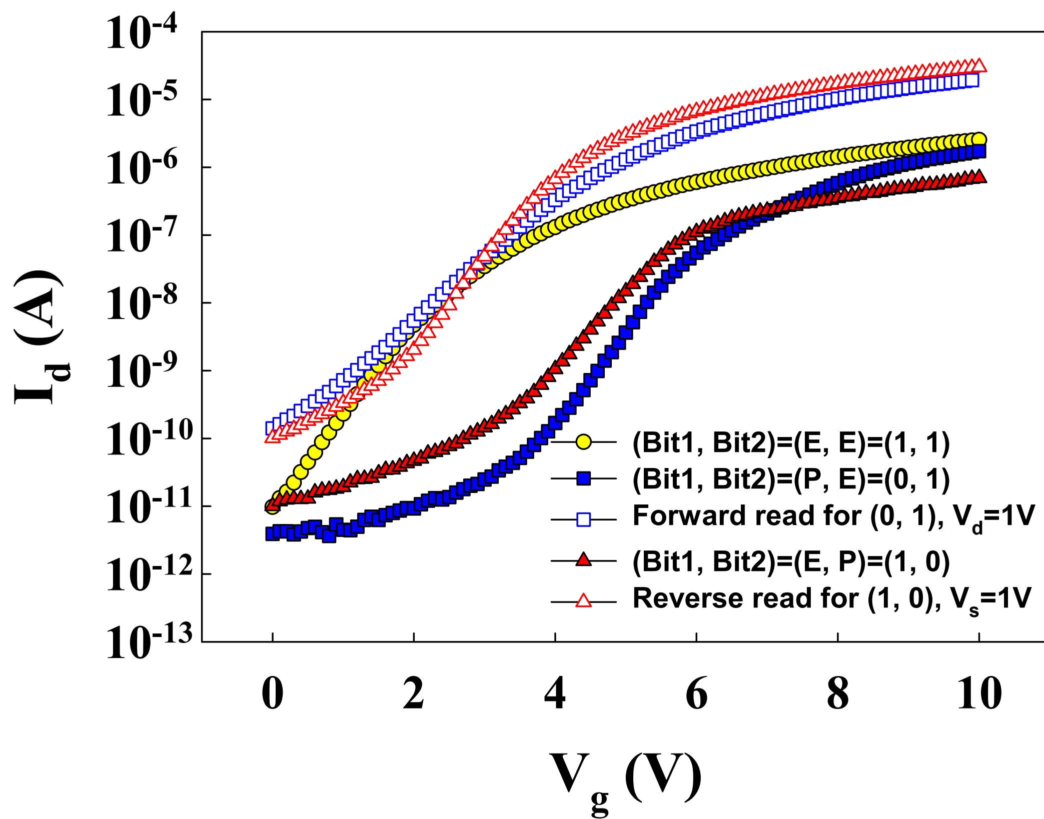


Fig. 4.3 Demonstration of 2 bits/cell operation. E: erased; P: programmed; Bit1: drain side; Bit2: source side.

		Program	Erase	Read
Bit 1	V_g	12V	-10V	3V
	V_d	12V	10V	0V
	V_s	0V	0V	1V
Bit 2	V_g	12V	-10V	3V
	V_d	0V	0V	1V
	V_s	12V	10V	0V

Table 4.1 Operation principles and bias conditions utilized during the operation of the poly-Si TFT Flash memory cell.

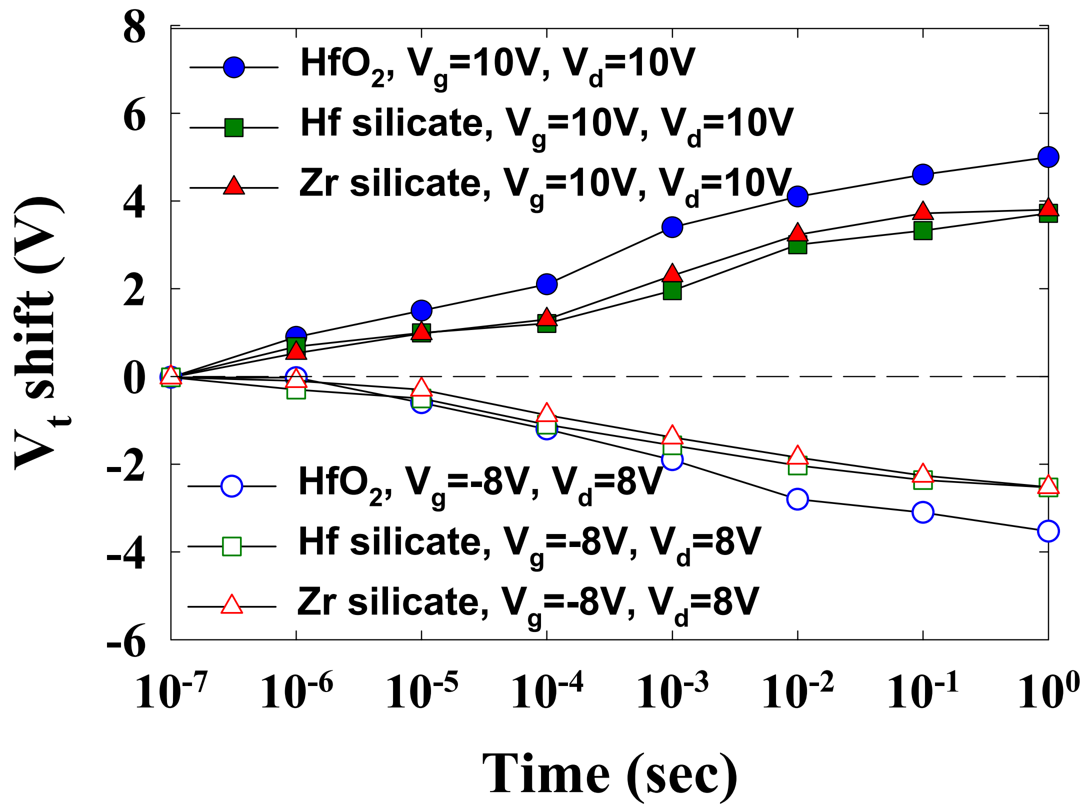


Fig. 4.4 Programming and erasing speed characteristics of poly-Si TFT memories with HfO_2, Hf silicate and Zr silicate trapping layers for different programming conditions. The programming time can be as short as 1ms if the window margin is set to 3V with V_g=V_d=12V. The erasing time is about 10 ms.

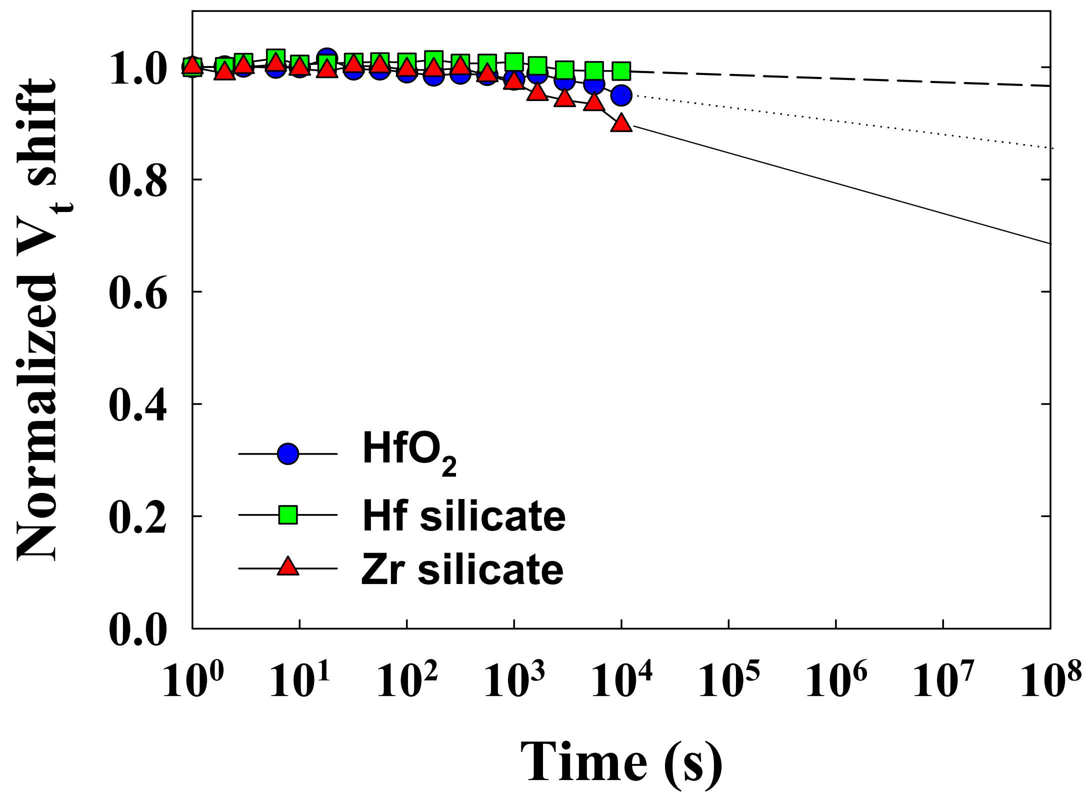


Fig. 4.5 Retention characteristics of the fabricated poly-Si-TFT memories at T=25°C. The retention time can be up to 10^6 s for 20% charge loss at room temperature.

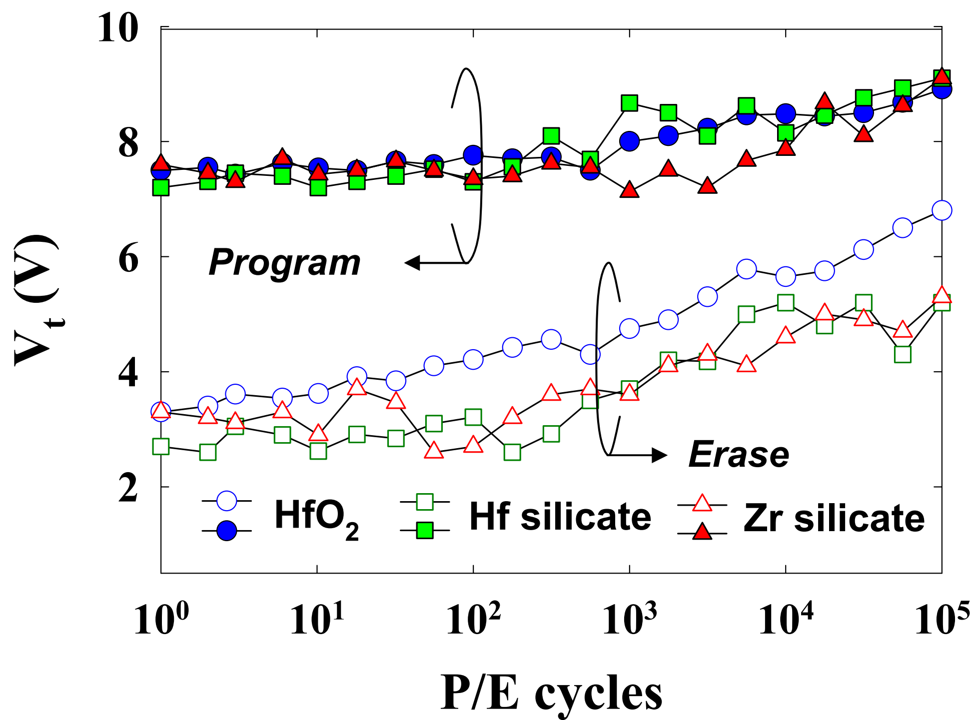


Fig. 4.6 Endurance characteristics of the poly-Si-TFT memories. Despite the occurrence of significant memory window narrowing, a memory window of about 2V is sustained even after 10^5 P/E cycles.

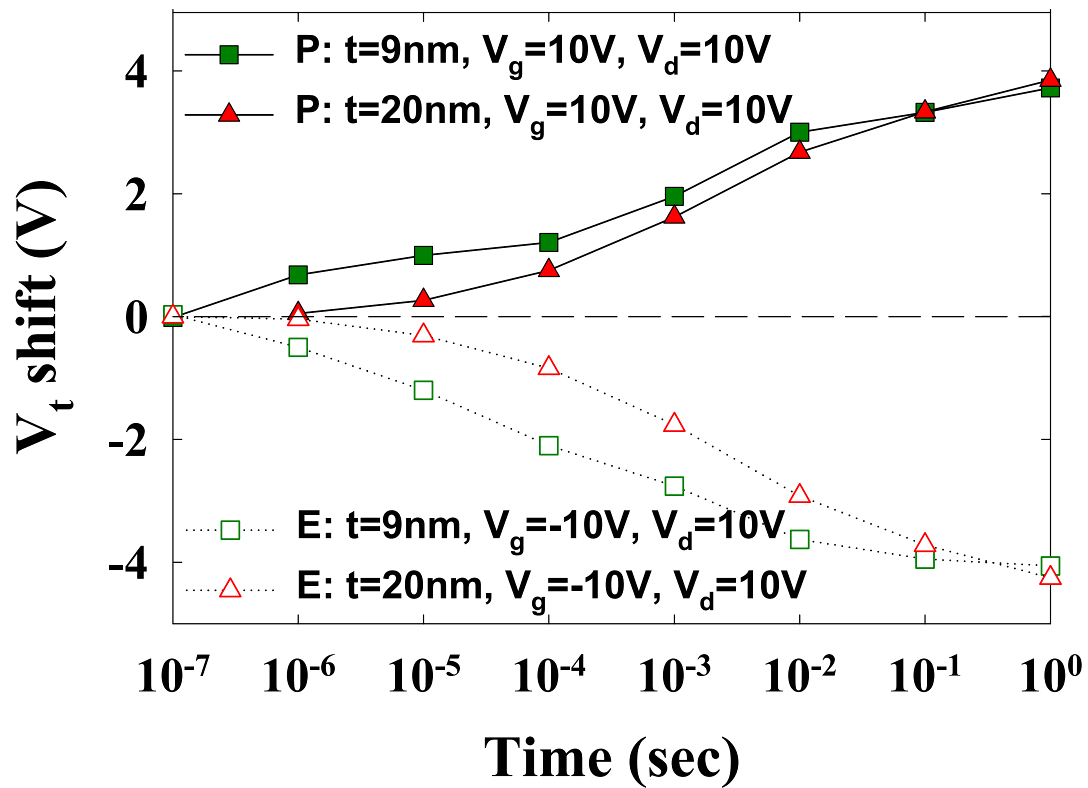


Fig. 4.7 Programming and erasing speed characteristics of poly-Si TFT memories with HfO_2, Hf silicate and Zr silicate trapping layers for different programming conditions. The programming time can be as short as 1ms if the window margin is set to 3V with V_g=V_d=12V. The erasing time is about 10 ms.

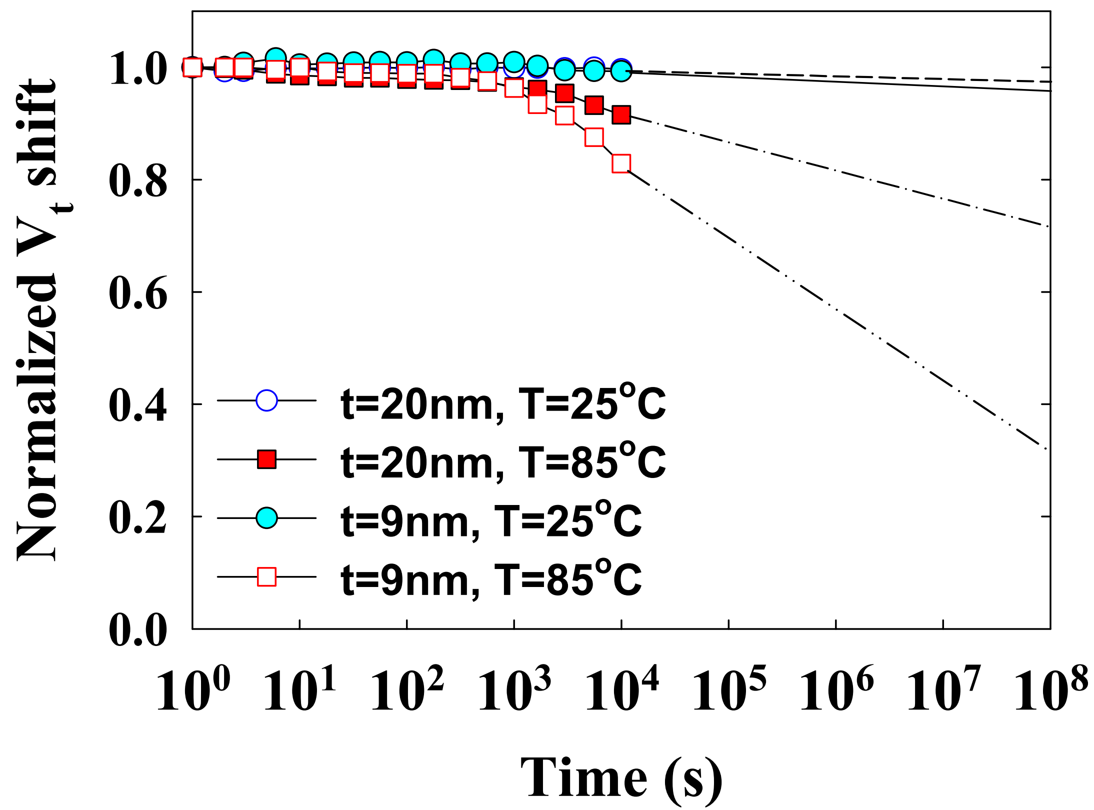


Fig. 4.8 Retention characteristics of the fabricated poly-Si-TFT memories with two different tunnel oxide thickness samples at T=25°C.

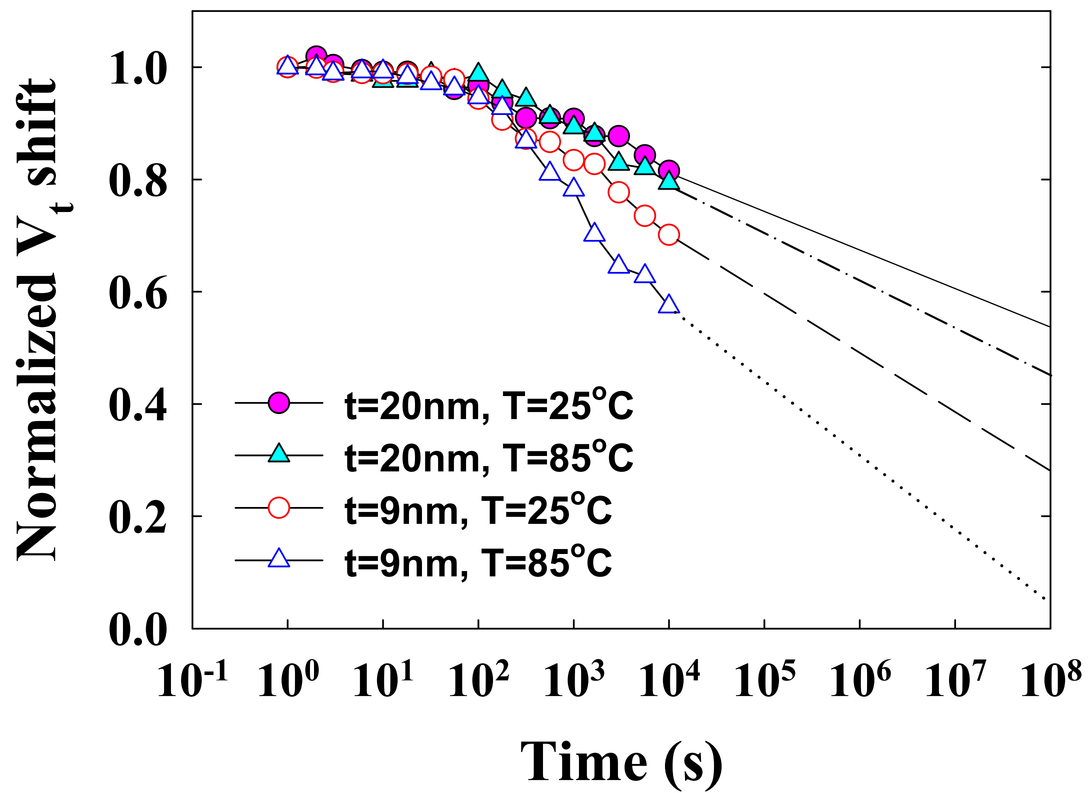


Fig. 4.9 Retention characteristics of the fabricated poly-Si-TFT memories with two different tunnel oxide thickness samples at T=85°C.

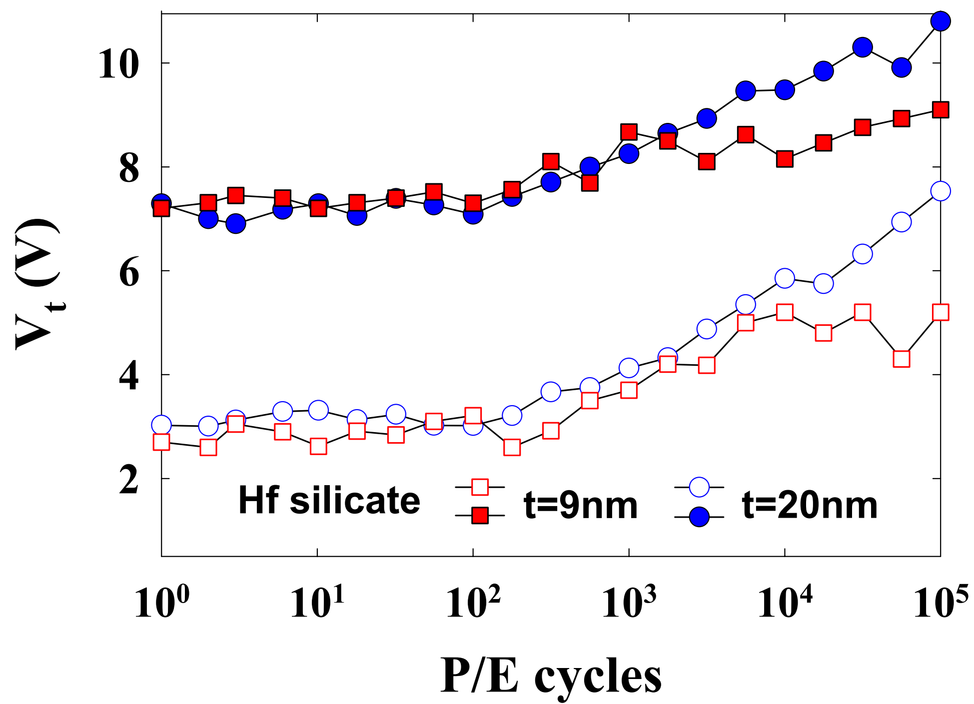


Fig. 4.10 Endurance characteristics of the poly-Si-TFT memories with two different tunnel oxide thickness samples.

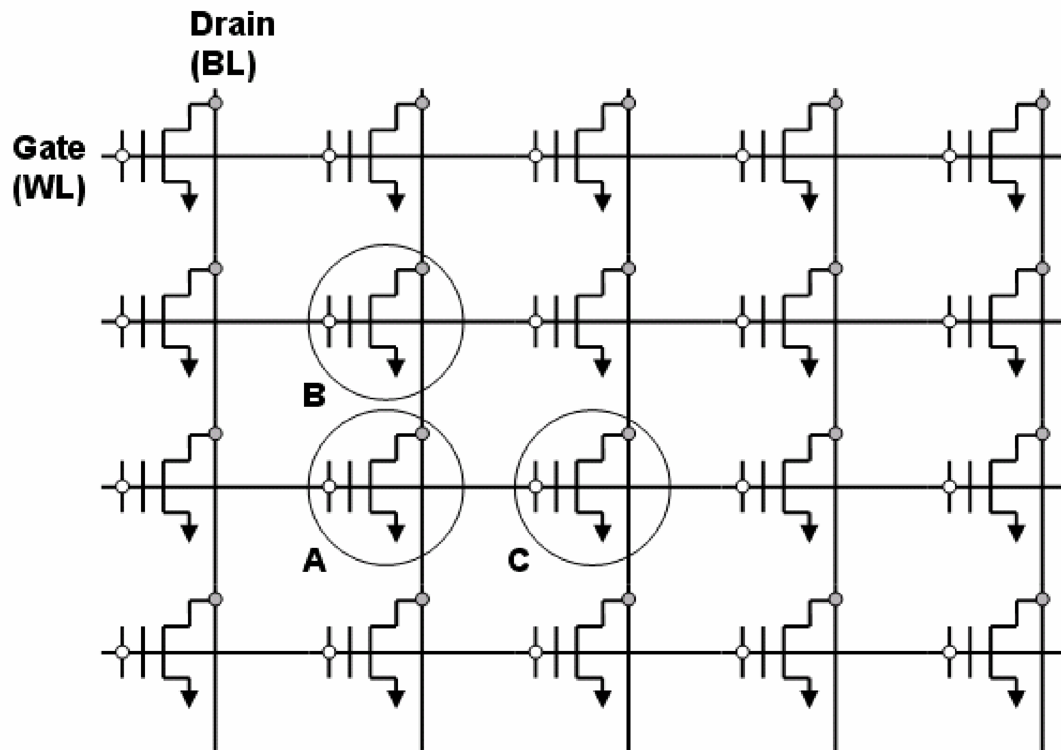


Fig. 4.11 The schematic illustration of disturb condition. Cell A is the programming cell. Cell B and Cell C are the drain disturbance and gate disturbance, respectively.

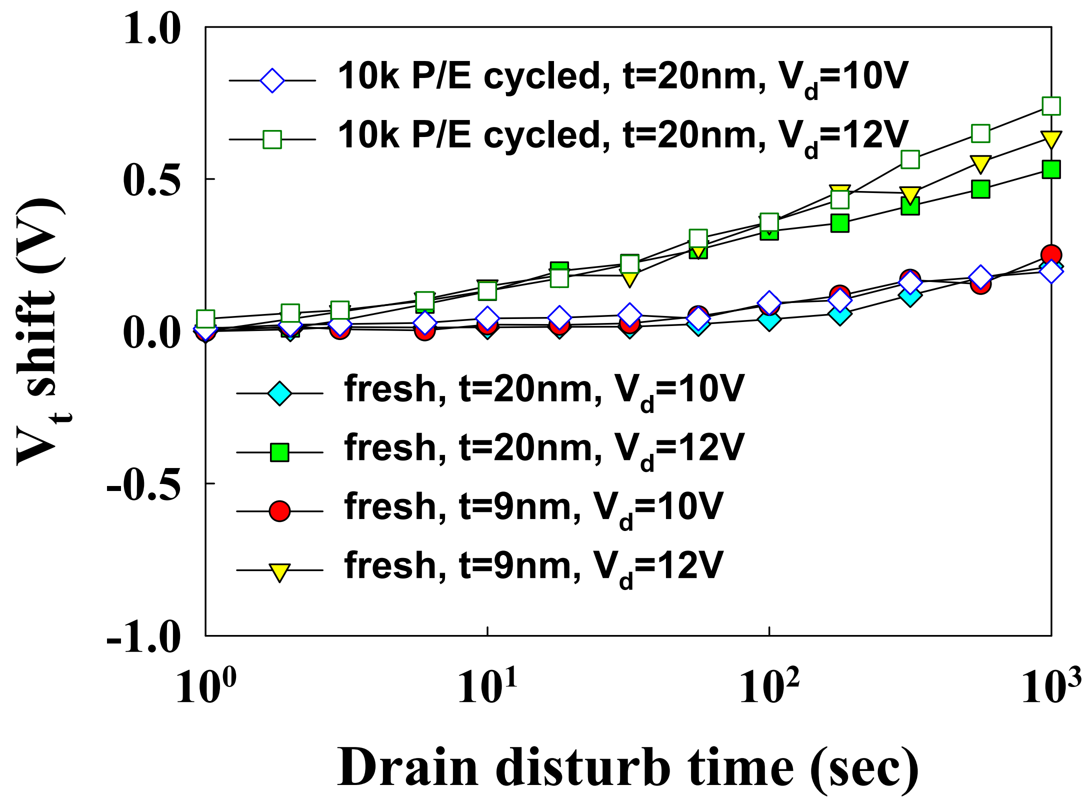


Fig. 4.12 Drain disturbance characteristics of the Hf silicate TFT memory devicess with two different tunnel oxide thickness samples. After 1000 s at 25 °C, small 0.7V drain disturb margin was observed.

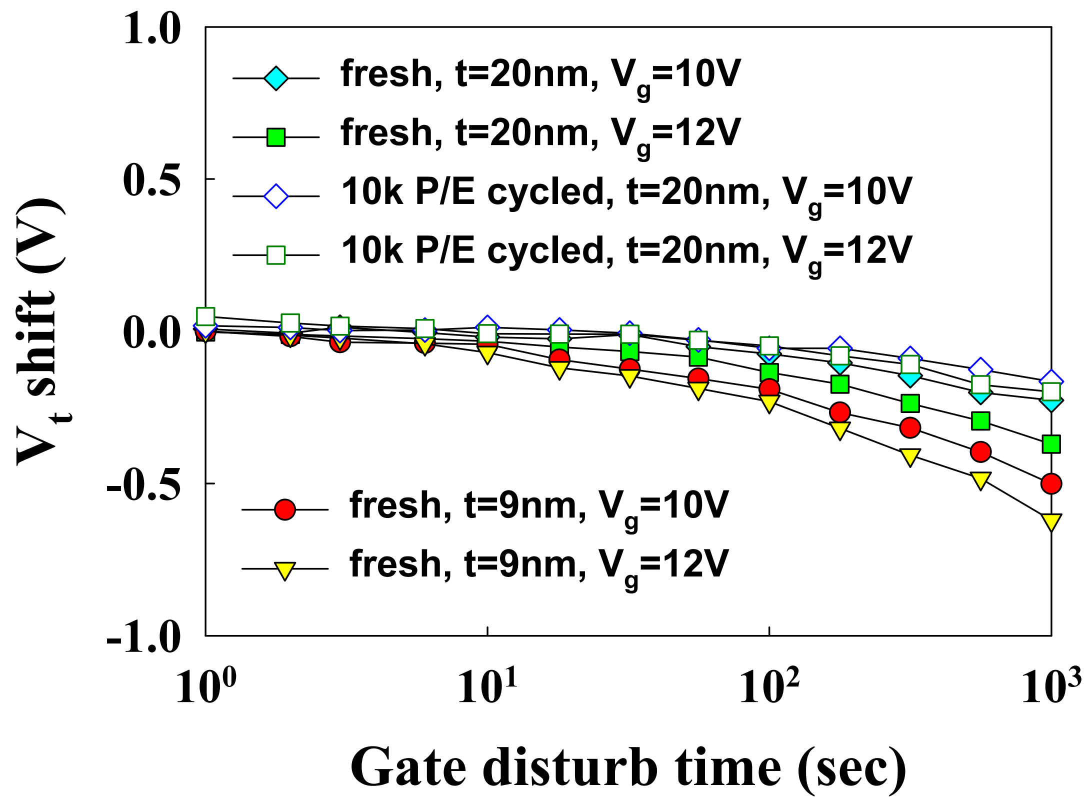


Fig. 4.13 Gate disturbance characteristics of the Hf silicate TFT memory devices with two different tunnel oxide thickness samples.

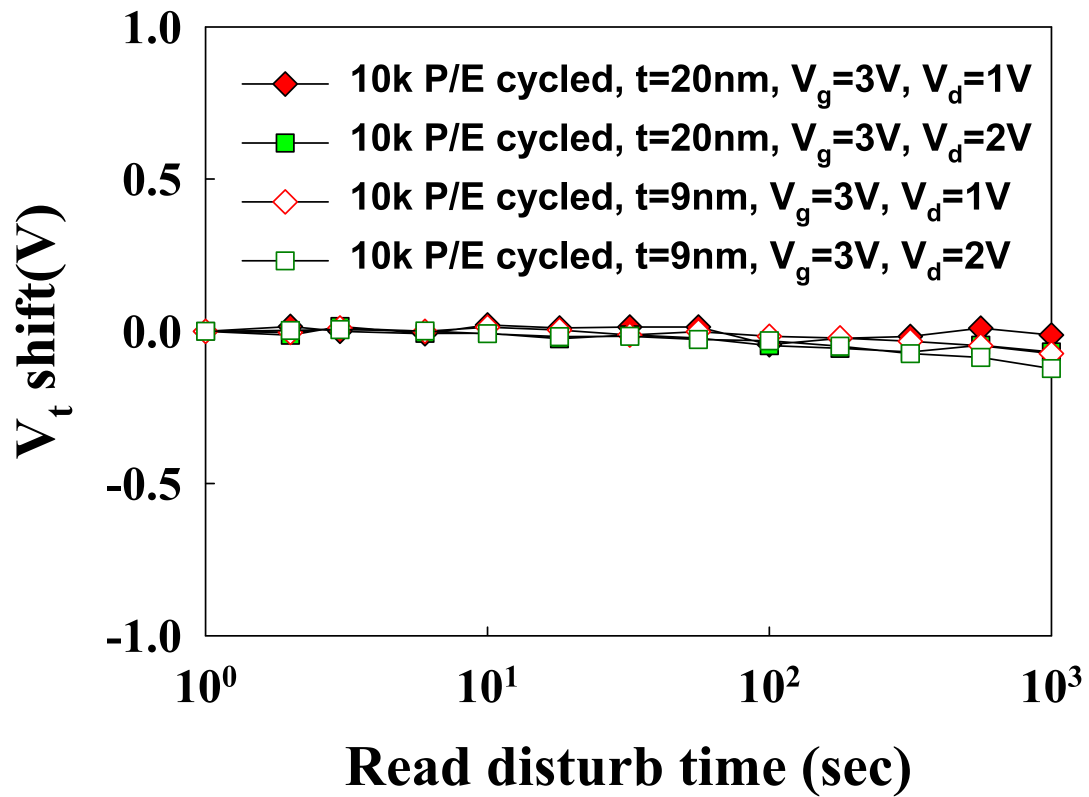


Fig. 4.14 Read disturbance characteristics of the Hf silicate TFT memory devices with two different tunnel oxide thickness samples. No significant V_t shift occurred for $V_d <$ 1, even after 1000 s at 25 °C.

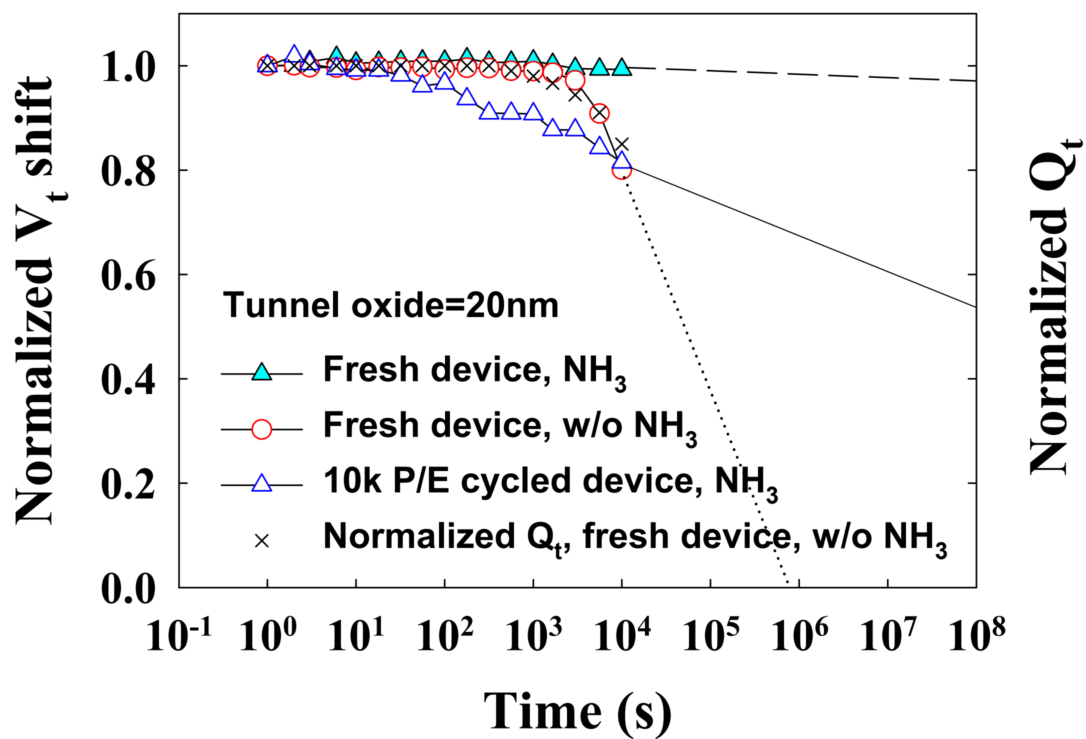


Fig. 4.15. Retention characteristics of the non-hydrogenated, fresh and 10k P/E cycled hydrogenated poly-Si-TFT memories at T=25°C.

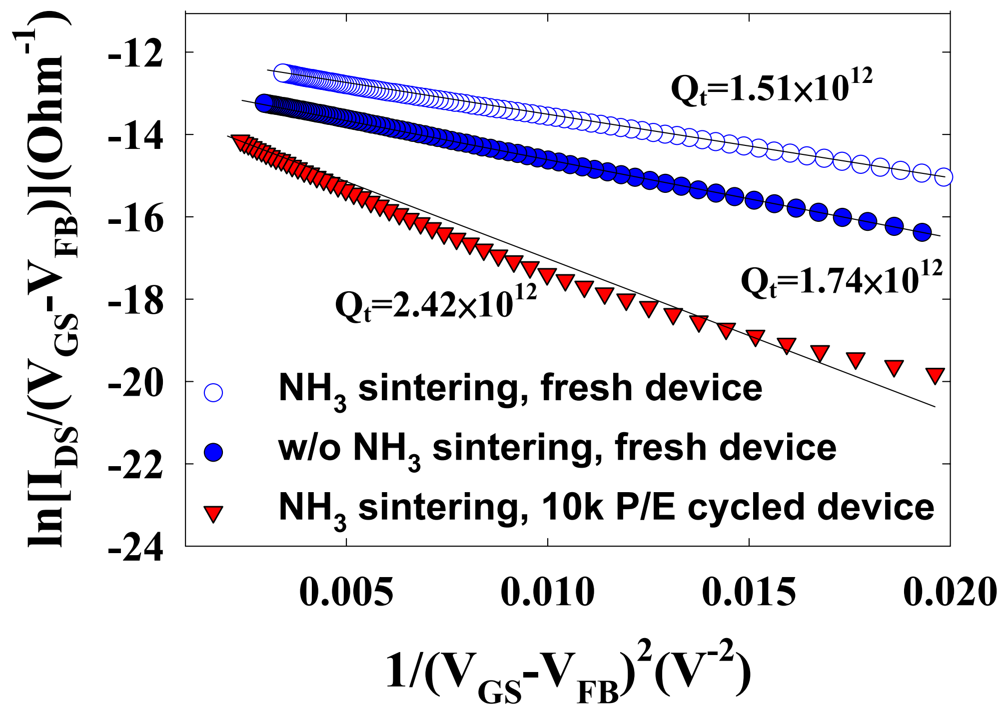


Fig. 4.16. In[I_D/(V_{GS}-V_{FB})] verus 1/(V_{GS}-V_{FB})^2 curves at V_{DS}=0.1V, and high V_{GS} for the three kinds of poly-Si-TFT memories.

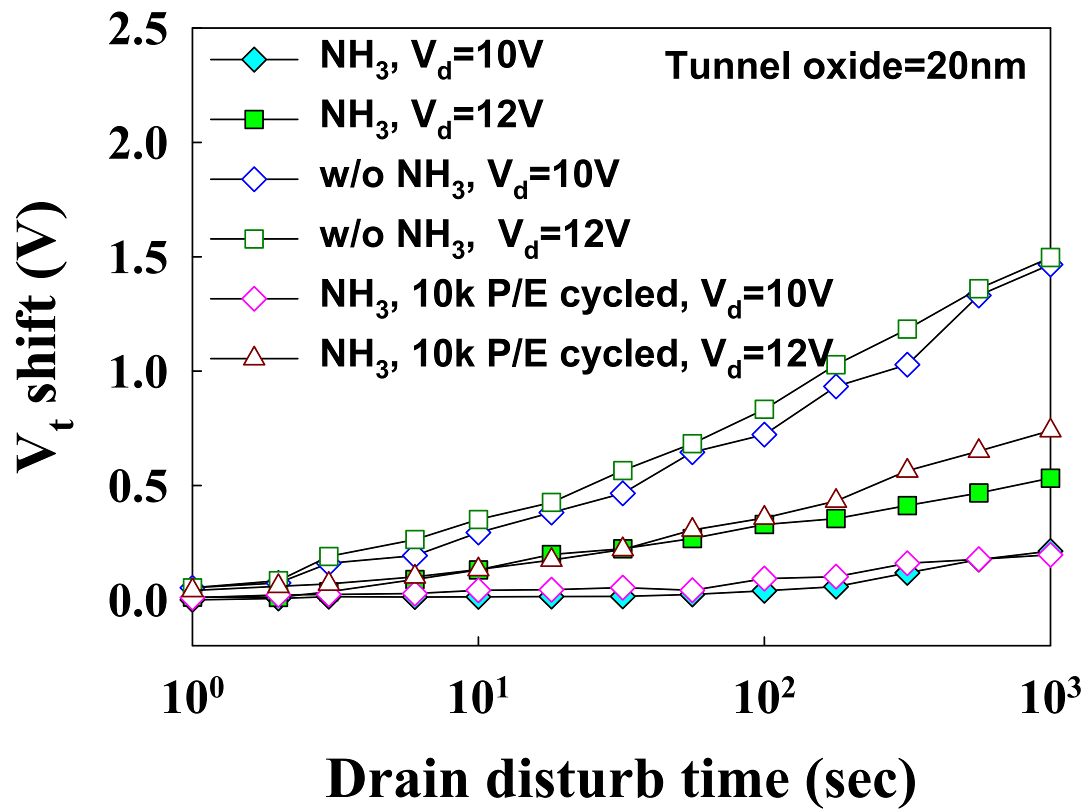


Fig. 4.17. Drain disturb characteristics of the non-hydrogenated, fresh and 10k P/E cycled hydrogenated poly-Si-TFT memories.

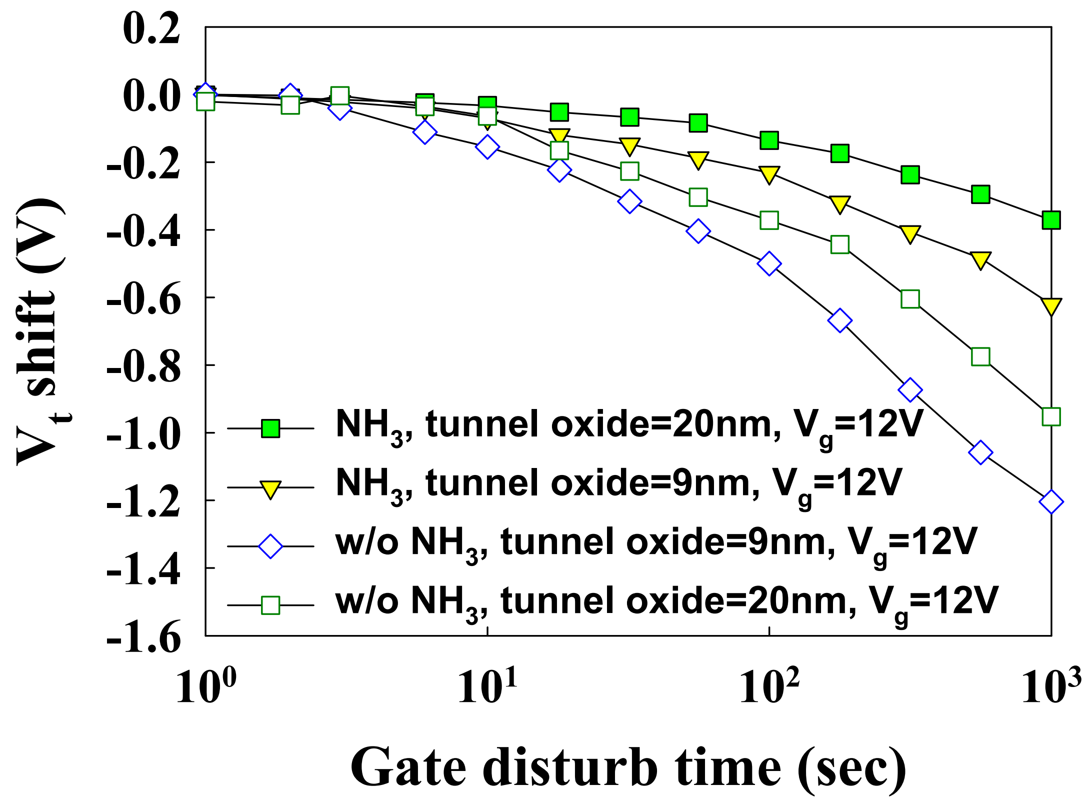


Fig. 4.18. Gate disturb characteristics of the non-hydrogenated, fresh and 10k P/E cycled hydrogenated poly-Si-TFT memories.

Chapter 5

Nano Scaled Tri-Gate HfO_2 Nanocrystal Flash Memory on SOI

5.1 Introduction

According to the International Technology Roadmap for Semiconductors (ITRS), there are critical limitations for aggressively scaling the conventional nonvolatile floating gate memories below sub-70nm node [5.1]. Therefore, the SONOS-type (poly-Si-oxide-nitride-oxide-silicon) structure memories including nitride memories and nanocrystal memories have recently attracted much attention for the application in the next-generation nonvolatile memories [5.2-5.11] because of their great potential for achieving high program/erase speed, low programming voltage and low power performance. However, many concerning issues are still presented for both types of memories. For conventional SONOS, erase saturation and vertical stored charge migration [5.8-5.9] are the major drawbacks; while for nanocrystal memories good enough charge keeping capability of the discrete storage nodes and the formation of nanocrystals with constant size, high density and uniform distribution are the extremely challenging issues [5.10]. In recent years, many papers have ever shown Al_2O_3 trapping layer as the potential candidate for replacing Si_3N_4 [5.11] and also demonstrated different kinds of nanocrystals to provide charge storage for the non-volatile memories, such as silicon (Si) nanocrystals, germanium (Ge) nanocrystals and metal nanocrystals [5.2-5.7].

In this chapter, we use the very local HfO_2 nanocrystals for the application of the nonvolatile Flash memories on the SOI. We have successfully achieved the 50nm

nanocrystal memories with good characteristics in terms of considerably large memory window, high speed program/erase, long retention time, and good endurance.

5.2 Experimental

The ultrashort HfO_2 nanocrystal Flash memory was fabricated by the following process steps for the structure on figure 5.1. After active region was patterned, a 2nm tunnel oxide was thermally grown at 1000 °C in a vertical furnace system. Next, a 10nm amorphous $HfSiO_x$ silicate layer was deposited by co-sputtering with pure silicon (99.9999% pure) and pure hafnium (99.9% pure) targets in an oxygen gas ambient. The co-sputtering process was performed with 7.6×10^{-3} Torr at room temperature and with precursors of O_2 (3 sccm) and Ar (24 sccm); in which both dc sputter powers were set at 150 W. A 8nm blocking oxide was then deposited through high-density-plasma chemical vapor deposition (HDPCVD). Next, a 100-nm *in-situ* n^+ phosphorus deoped a-Si gate layer was deposited by LPCVD. After gate patterning, the remaining oxide on source/drain regions was removed by diluted HF and then a 150-nm TEOS oxide sidewall spacer was formed by deposition and etching. A self-aligned implantation was used to perform the n^+ source/drain extension with As^+ to dose 1×10^{15} cm^{-2} and energy 20 keV, tilt 20°. Then, a self-aligned implantation was used to perform the n^+ source/drain with As^+ to dose 5×10^{15} cm^{-2} and energy 15 keV, tilt 7°. Dopants were activated by RTA at 950°C for 15s and the $HfSiO_x$ silicate film into the separated HfO_2 and SiO_2 phases. After contact and metallization have completed the processes.

5.3 Results and Discussion

5.3.1 Material Analysis of HfO_2 Nanocrystal memory

Figure 5.2(a) and Fig. 5.2(b) shows cross-section-view high-resolution transmission microscopy (HRTEM) image of the HfO_2 nanocrystals device. Clearly, the gate length is about 55nm and the nanocrystals were well separated in two dimensions within the SiO_2; in which the average distance is >5 nm. This isolation of the nanocrystals prevents the formation of effective conductive paths between adjacent nodes. The mechanism responsible for the formation of HfO_2 nanocrystal is through the phase separation of hafnium silicate into a crystallized structure [5.12]. For the Hf-silicate layer, the compositions within metastable extensions of the spinodal are unstable and HfO_2 nanocrystal will be formed and wrapped up by SiO_2 after cooling down from RTA processing. In addition, it is clear from the diffraction patterns that the as-deposited film was amorphous and that the sample subjected to RTA was polycrystalline. The HfO_2 nanocrystals have monoclinic crystalline structures.

5.3.2 Characteristics of Fresh Devices and 2-bit operation

Figure 5.3 shows the I_{ds}-V_{gs} curves of the HfO_2 nanocrystal memory devices with programming time of 10μs for different programming conditions. Channel hot-electron injection and band-to-band hot-hole injection were employed for programming and erasing, respectively. All cells described in this chapter have dimensions of L/W = 50/50 nm. A relatively large memory window of about 2.2V can be achieved at the V_g=11V, V_d=4V, T=1ms program operation. Program characteristics as a function of pulse width for different operation conditions are shown in Fig. 5.4(a). Both source and substrate terminals were biased at 0V. The “V_t shift” is defined as the threshold voltage change of a device between the written and the erased states. With V_d=4V, V_g=11V, relatively high speed (1ms) programming

performance can be achieved with a memory window of about 2.2V. Meanwhile, Fig. 5.5(b) displays the erase characteristics as a function of various operation voltages. Again, excellent erase speed of around 0.1 ms can be obtained.

The retention characteristics of the HfO_2 nanocrystal memory for the fresh devices at different temperature (T=25°C, 85°C, and 125°C) are illustrated in Fig. 5.5. The retention time can be up to 10^8 seconds for 17%, 30% and 71% charge loss at temperature 25°C, 85°C and 125°C. Much charge loss has been seen for the both samples. We ascribe these results that the the HfO_2 nanocrystals have good formation at the RTA at the temperature 950°C for 15sec. The endurance characteristics after 10^6 P/E cycles are also shown in Fig. 5.6. The programming and erasing conditions are V_g= 10V for 1ms and V_g=-10V for 1ms, respectively. Small memory window narrowing has been displayed. This trend indicates that the amount of operation-induced trapped electrons is very tiny. Certainly, this is intimately related to the use of ultra-thin tunnel oxide and very minute amount of residual charges in the HfO_2 nanocrystals after cycling. Fig. 5.7 demonstrates the feasibility of performing two-bit operation with our HfO_2 nanocrystal memories through a reverse read scheme in a single cell. From the I_{ds}–V_{gs} curves, it is clear that we could employ forward and reverse reads to detect the information stored in the programmed bit1 and bit2, respectively. The read operation was achieved using a reverse read scheme.

5.3.3 Different length and width characteristics

In the fabricated ultranarrow-channel memory, a larger threshold voltage shift has been observed than in the wide-channel memory for different length and width (Fig. 5.8(a)(b) and Fig. 5.9(a)(b)). From numerical calculations, it turns out that this is caused by bottleneck regions that dominate the conductance of the whole channel in

the ultranarrow-channel. In the wide channel, the current can flow through the wide and low-potential region. In the ultranarrow channel, on the contrary, the current path is completely blocked at the bottleneck region where one dot covers almost the entire channel bottleneck effect. Moreover, the average potential in the ultranarrow channel is higher than in the wide channel because of the effects of dots on the side surfaces. These effects are the origins of larger Vt shift in the ultranarrow devices.

5.3.4 Disturbance

Figure 5.10 demonstrates the read disturbance induced erase-state threshold voltage instability in a localized HfO_2 nanocrystal trapping storage Flash memory cell under several operation conditions. For two-bit operation, the applied bitline voltage in a reverse-read scheme must be sufficiently large (>1.5 V) to be able to "read through" the trapped charge in the neighboring bit. The read-disturb effect is the result of two factors: the word-line and the bit-line. The word-line voltage during read may enhance room temperature (RT) drift in the neighboring bit [5.13]. On the other hand, a relatively large read bit-line voltage may cause unwanted channel hot-electron injection and, subsequently, result in a significant threshold voltage shift of the neighboring bit. In our measurements, the gate and drain biases were applied and the source was grounded. The results demonstrate clearly that almost no read disturbance occurred in our HfO_2 nanocrystal Flash memory under low-voltage reading (V_g = 1.5 V; V_d = 1V~2.5 V). For a larger memory window, we found that no read disturbance can be observed after operation after 1000 s at 25 °C.

5.3.5 Few Electron Effect

Firstly, we studied the drain current versus gate voltage characteristic, I_dV_g of the

memory devices at room temperature. I_dV_g characteristics of the HfO_2 nanocrystal memories clearly show the occurrence of few electron effects. In particular, in Fig. 5.11, the continuous curve corresponds to the I_dV_g measurement, performed on a written device, when the gate bias is slowly swept down from 3 to -2 V. On this characteristic, abrupt peaks on the current are observed, corresponding to the subsequent discharging of few electrons from a HfO_2 nanocrystal. The dashed lines correspond to the same measurements performed with a fast voltage sweep on the same device after various writing conditions. In this case, no discharging event occurs during the measurement. Moreover, we can note that the continuous curve abruptly jumps from one dashed line to the other. Note that simultaneous injection/emission of electrons from different HfO_2-dots is improbable due to the fact that dots are largely spread in size in our devices. As reported in [5.14], the threshold voltage shift, △Vth induced by one electron trapped in the a HfO_2-dot can be estimated as

$$\Delta V_{\mathrm{th}} = \frac{q}{C_{\mathrm{fg}} + C_{\mathrm{cg}}\left(\frac{C_{\mathrm{fc}}+C_{\mathrm{fg}}}{C_{\mathrm{fc}}}\right)} \qquad (1)$$

where C_{fg} is the dot to gate capacitance, C_{cg} the channel to gate capacitance and the C_{fc} channel to dot capacitance. The following expressions for the capacitances are taken: $C_{fg}=\varepsilon_{OX}A_{dot}/t_2$; $C_{cg}=\varepsilon_{OX}(A-A_{dot})/(t_1+t_2)$; $C_{fc}=\varepsilon_{OX}A_{dot}/t_1$ where A_{dot} is the HfO_2-dot area, A is the total active area of the device (given by the top and the lateral sides of the SOI channel covered by the gate), t_1 and t_2 are the tunnel and control oxide thickness, respectively, and ε_{OX} is the oxide dielectric constant. After developments, (1) yields

$$\Delta V_{\mathrm{th}} = \frac{q \cdot t_2}{A \cdot \varepsilon_{\mathrm{ox}}} \qquad (2)$$

It should be stated that, in this capacitive approach, the threshold voltage shift is independent from the area of the HfO_2 dot, but only depends on the total gate area *A*

and on the number of charges trapped in the HfO_2-dot. Based on (2), the threshold voltage shift induced by only one electron trapped in one HfO_2-dot, named hereafter δVth, in a device with W=L=50nm, is about 15 mV. Note that this value is of the same order of magnitude of the average experimental threshold voltage shift, which can be extracted from Fig. 5.11. Fig. 5.12(a)(b) is the I_dV_g of the memory devices at low temperature (40°K). The I_dV_g characteristics of the HfO_2 nanocrystal memories clearly also show the occurrence of few electron effects. On this characteristic, abrupt peaks on the current are observed, corresponding to the subsequent discharging of few electrons from a HfO_2 nanocrystal. For the slowly swept, abrupt peaks are observed more clearly because more electron discharging, but they still have the same order of magnitude of almost 15mV.

5.4 Summary

In this chapter, we have proposed a novel simple, reproducible, reliable technique for preparation of 50nm high density HfO_2 nanocrystals using spinodal decomposition of hafnium silicate on SOI and achieved nanocrystal memories with characteristics in terms of large memory windows, high speed program/erase, retention time, and good endurance. Few Electron Phenomena at 40°K has been observed clearly. Discontinuities appear, that is corresponding to discharging of few electron from HfO_2 nanocrystals.

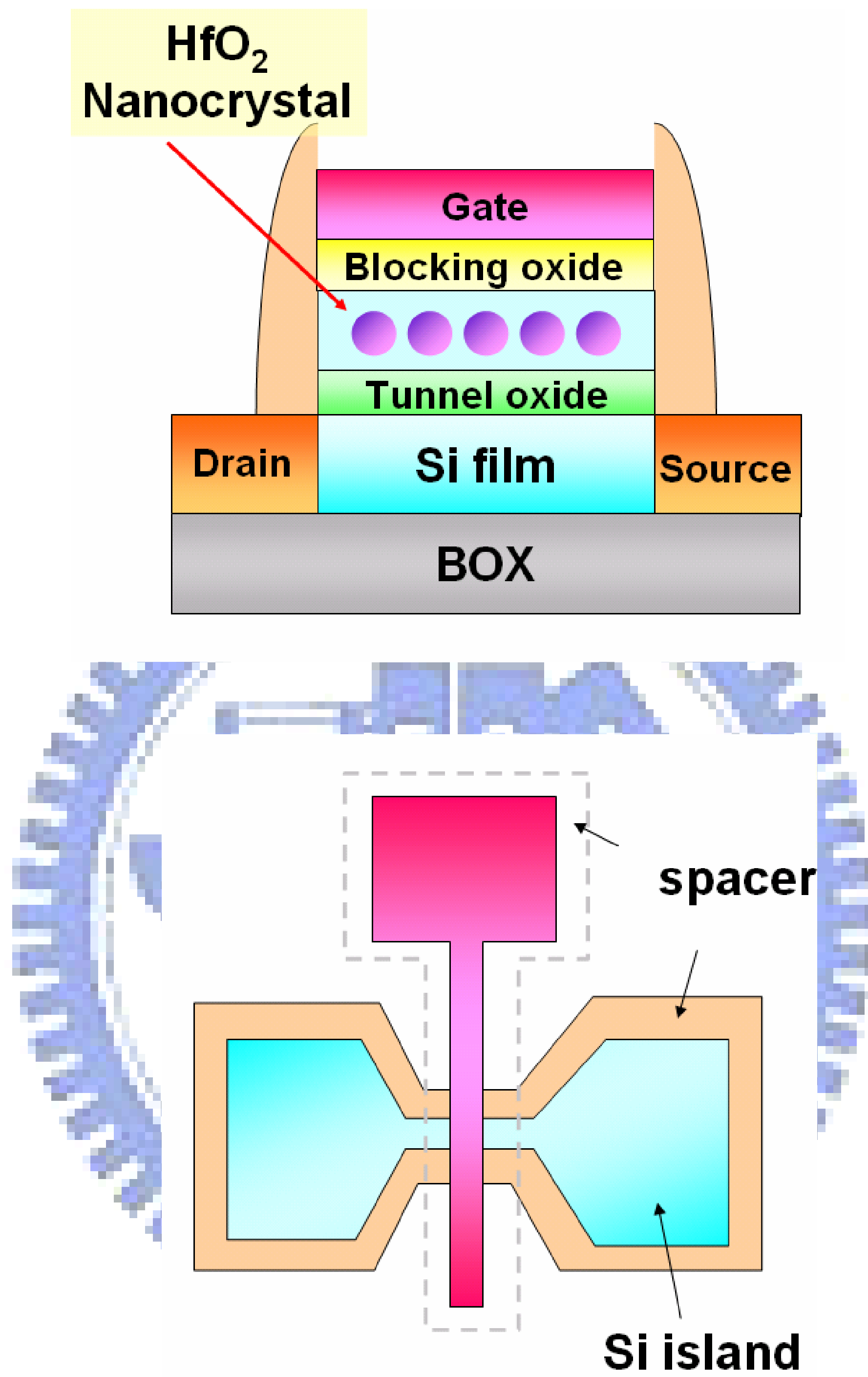
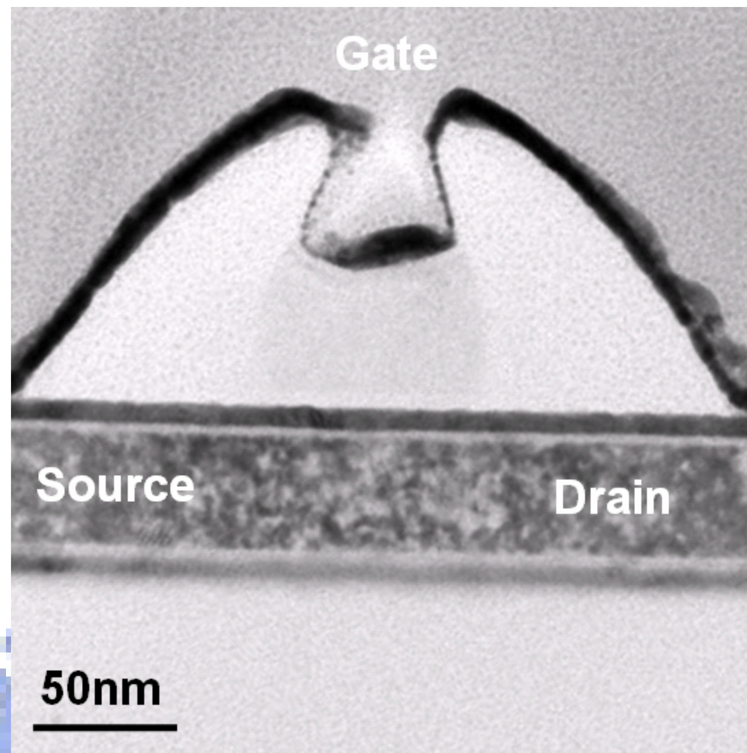


Fig. 5.1 HfO_2 nanocrystal Flash memory cell structure.



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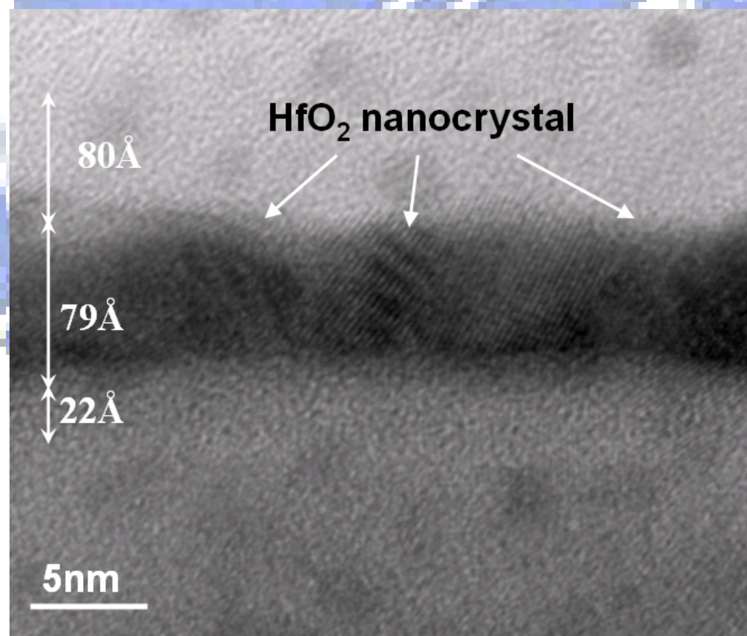

(b)

Fig. 5.2 (a) Planar-view HRTEM image of the 50nm HfO_2 nanocrystals devices. (b) Planar-view HRTEM image of the HfO_2 nanocrystals trapping layer.

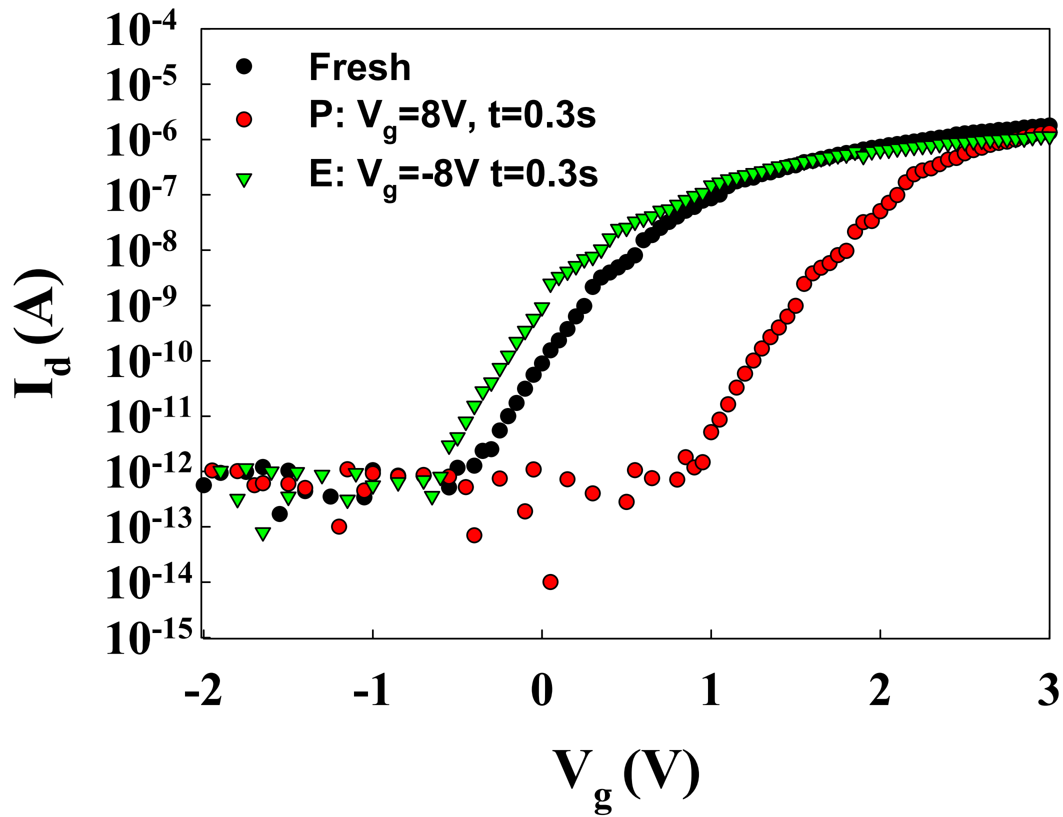

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Fig. 5.3 I_{ds}-V_{gs} curves of programmed memories with different programming conditions. The programming time is 10μs. A memory window of larger than 3V can be achieved with V_g= V_d=10V programming operation.

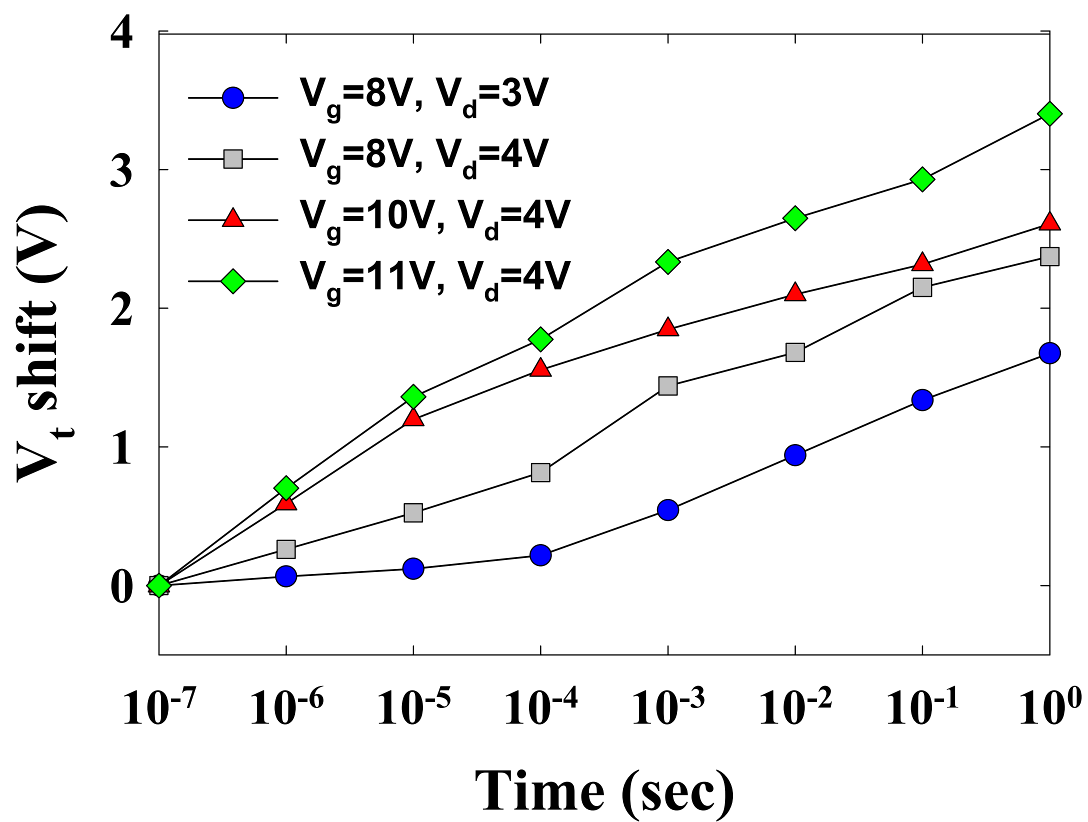


Fig. 5.4 (a) Program characteristics of HfO_2 nanocrystal memory devices with different programming conditions. (b). Erase characteristics of HfO_2 nanocrystal memory devices with different erasing voltages.

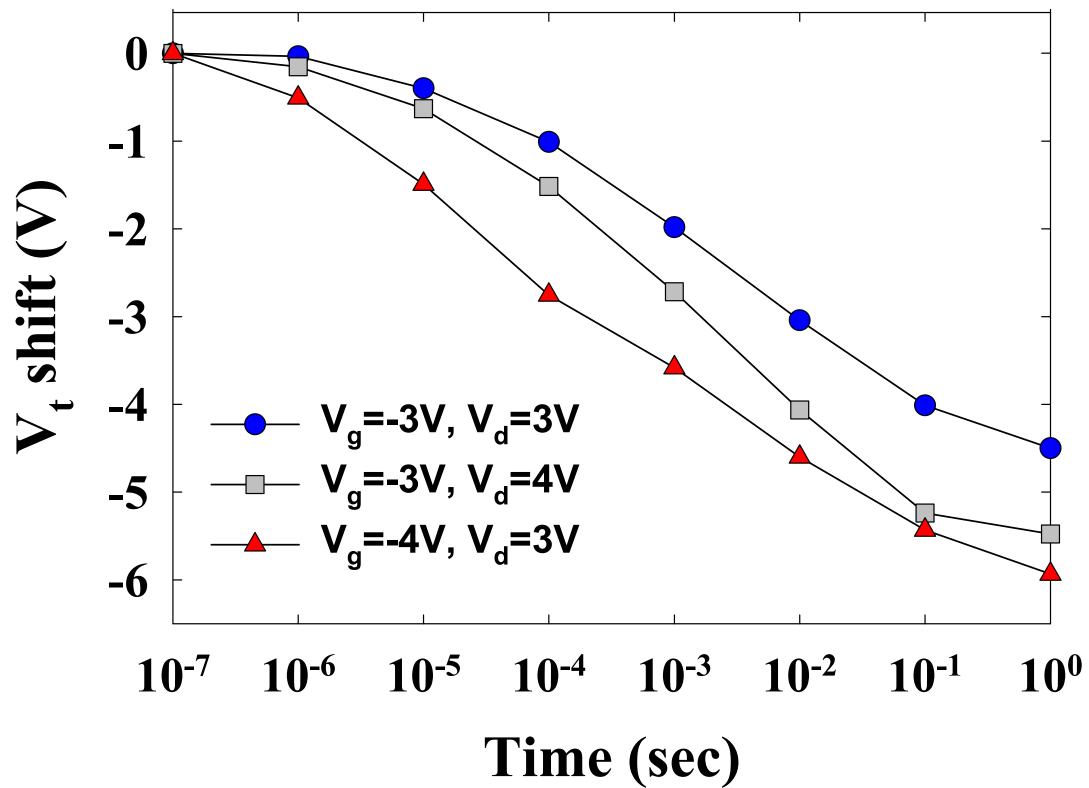


Fig. 5.4 (a) Program characteristics of HfO_2 nanocrystal memory devices with different programming conditions. (b). Erase characteristics of HfO_2 nanocrystal memory devices with different erasing voltages.

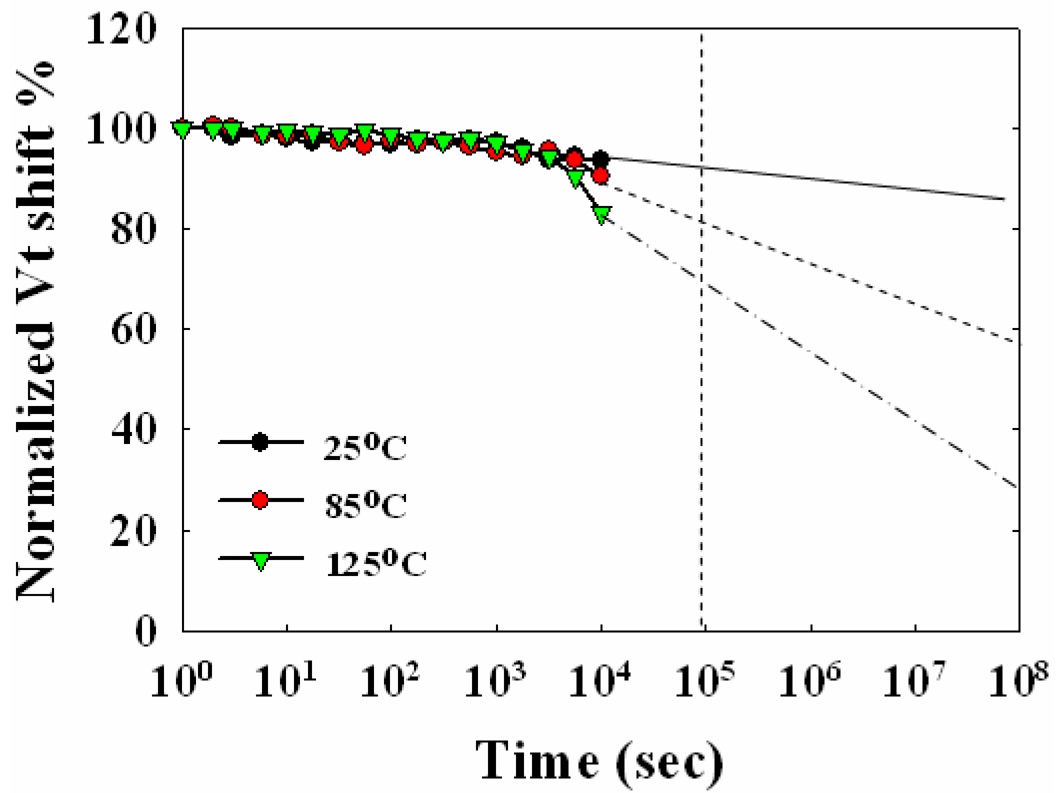


Fig. 5.5 Retention characteristics of HfO_2 nanocrystal memory devices at T=25°C.

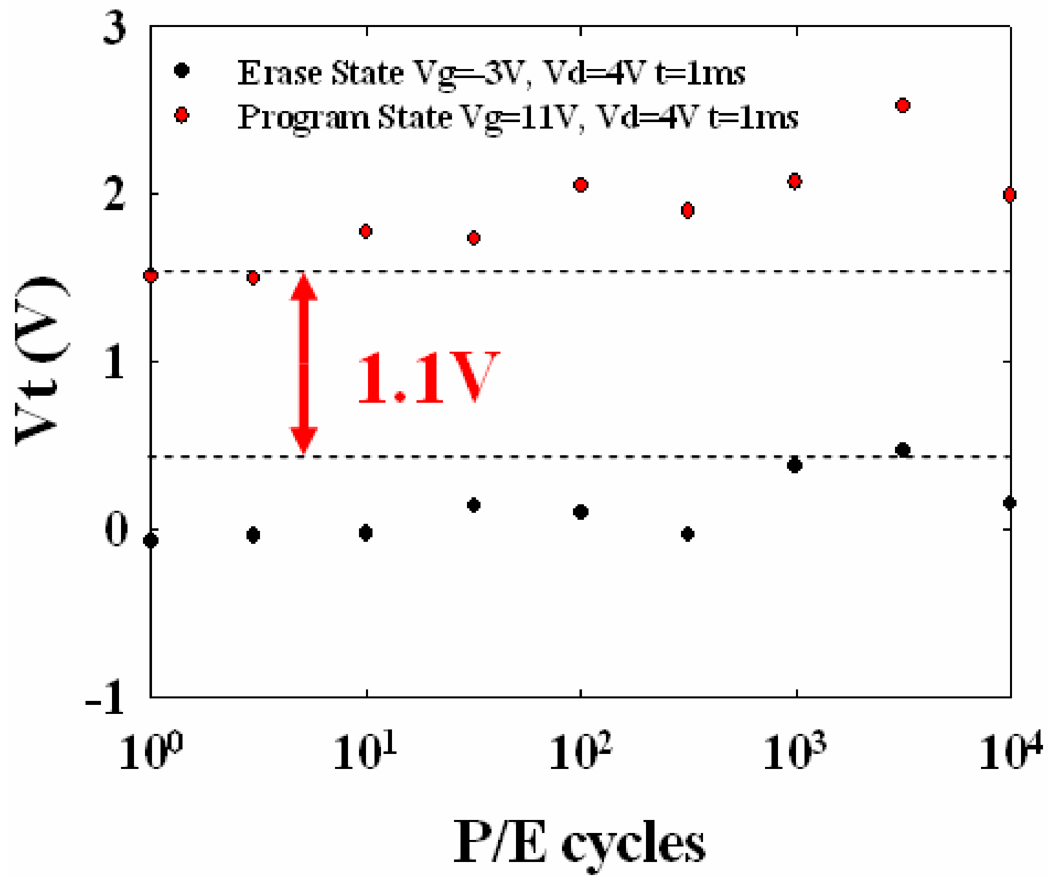


Fig. 5.6 Endurance characteristics of HfO_2 nanocrystal memory devices. Negligible degradation is found even after 10^5 P/E cycles.

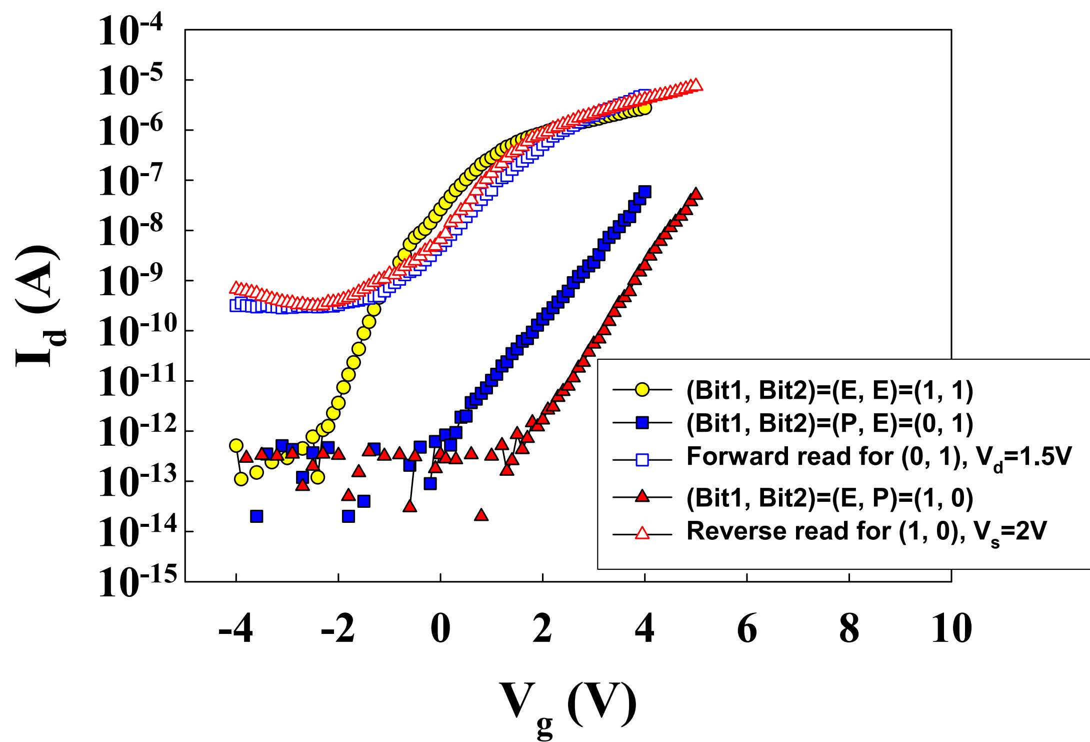
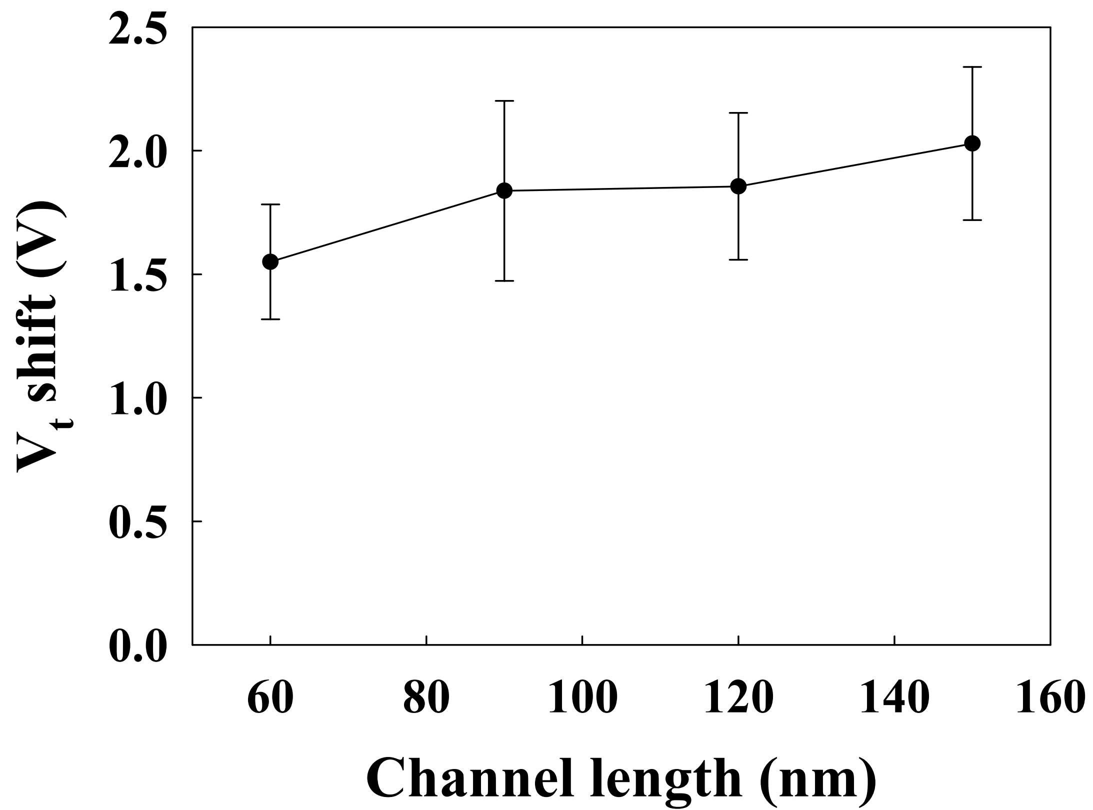


Fig. 5.7 I_{ds}–V_{gs} Curves of the two-bit memory in a cell; forward read and reverse read for programmed bit1 and programmed bit2.



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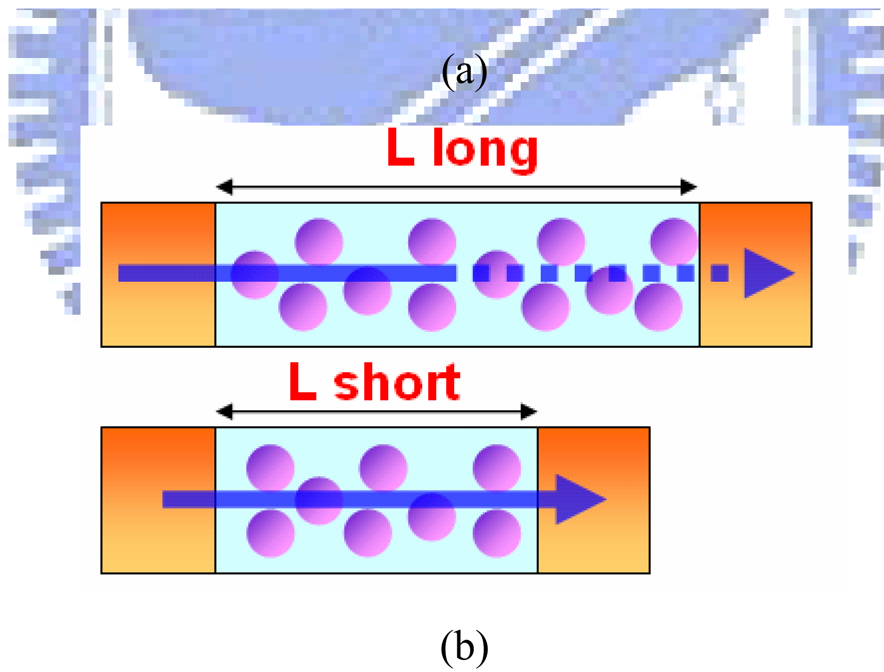

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Fig. 5.8 (a) Room-temperature hysteresis characteristics of the fabricated devices with various channel lengths. (b) The carrier mobiles with various channel lengths.

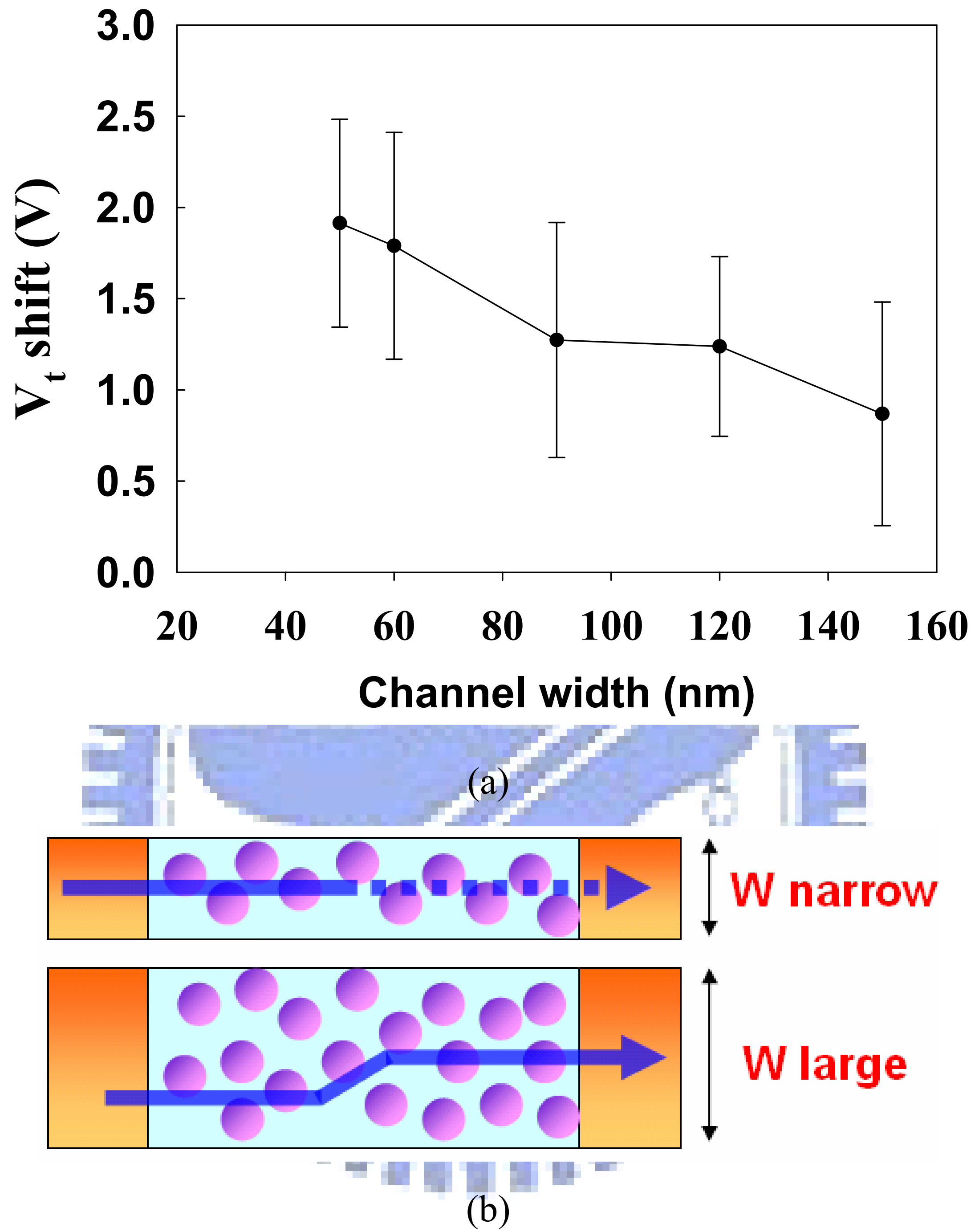


Fig. 5.9 (a) Room-temperature hysteresis characteristics of the fabricated devices with various channel widths. (b) The carrier mobiles with various channel widths.

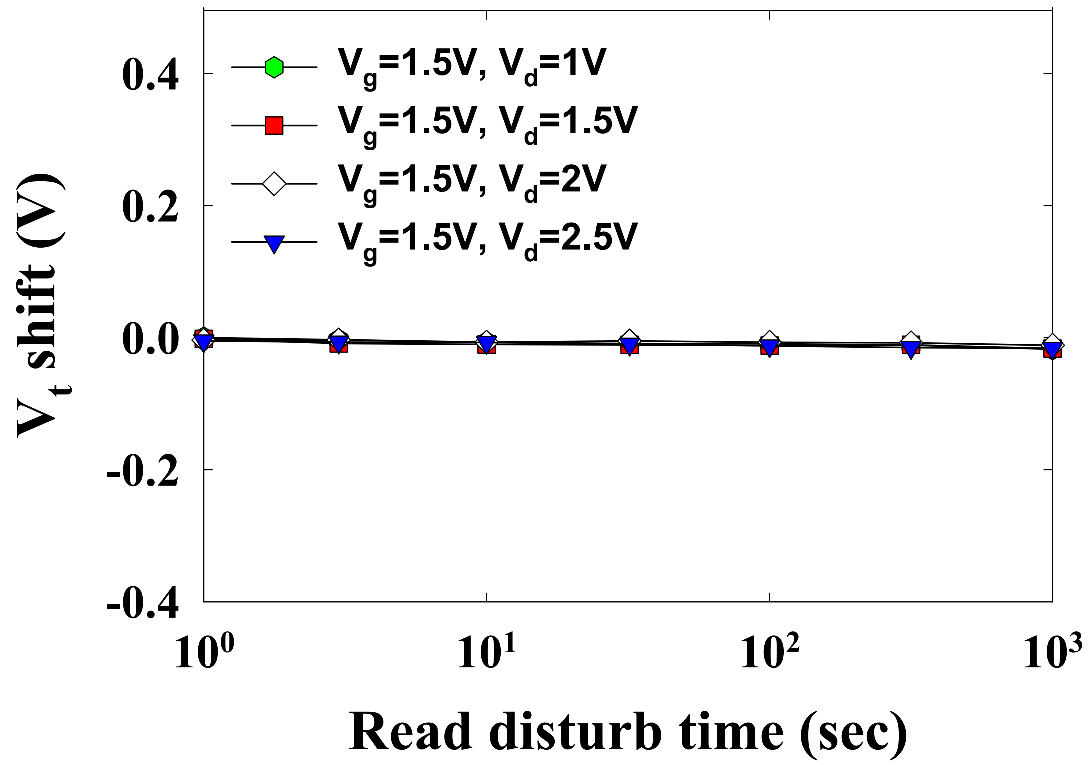


Fig. 5.10 Read disturbance characteristics of the HfO_2 nanocrystal memory devices.

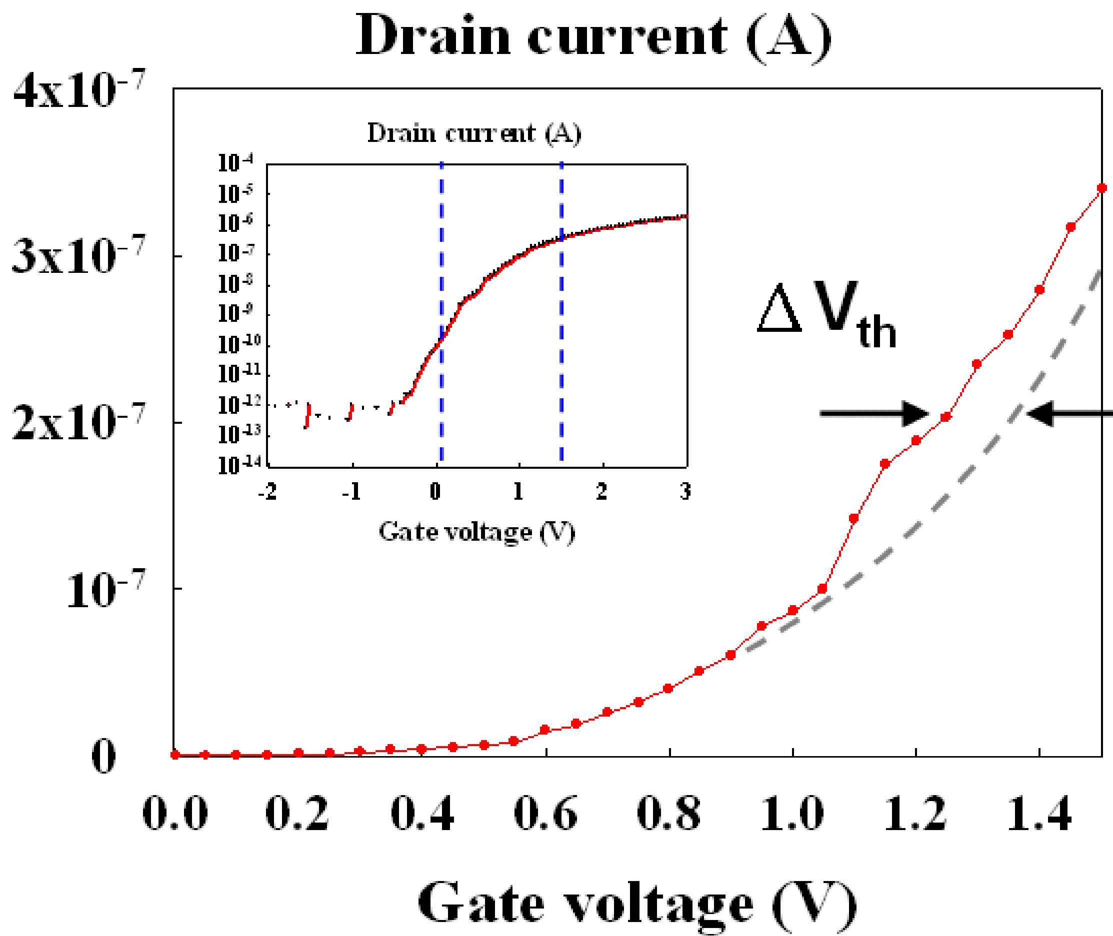
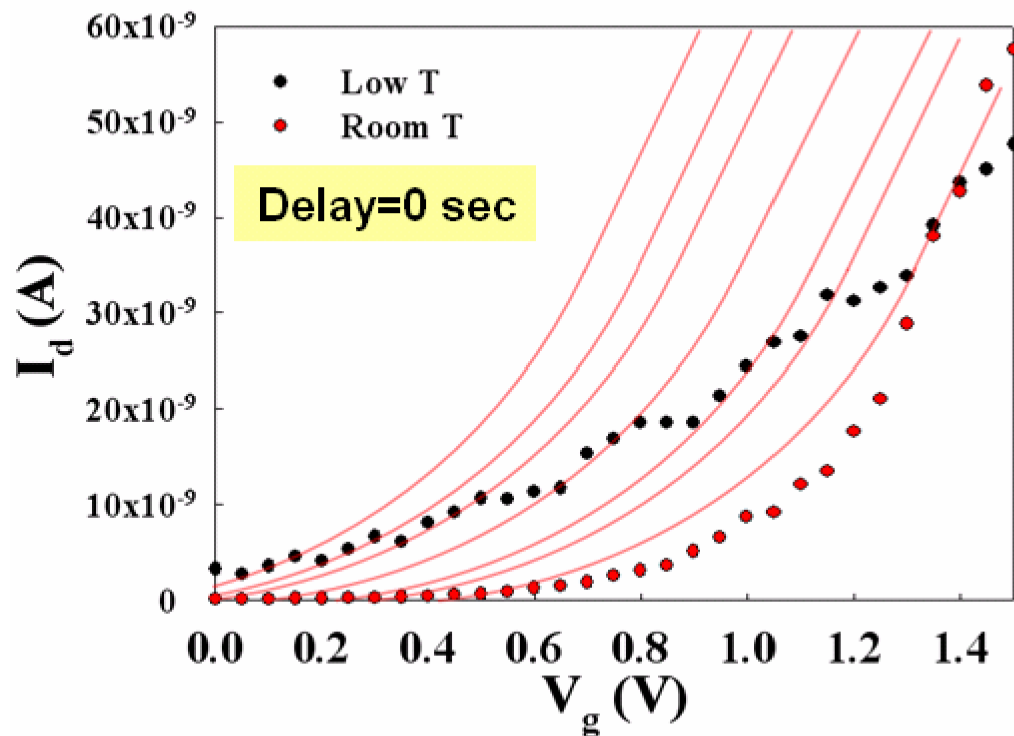
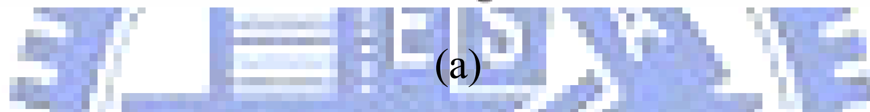
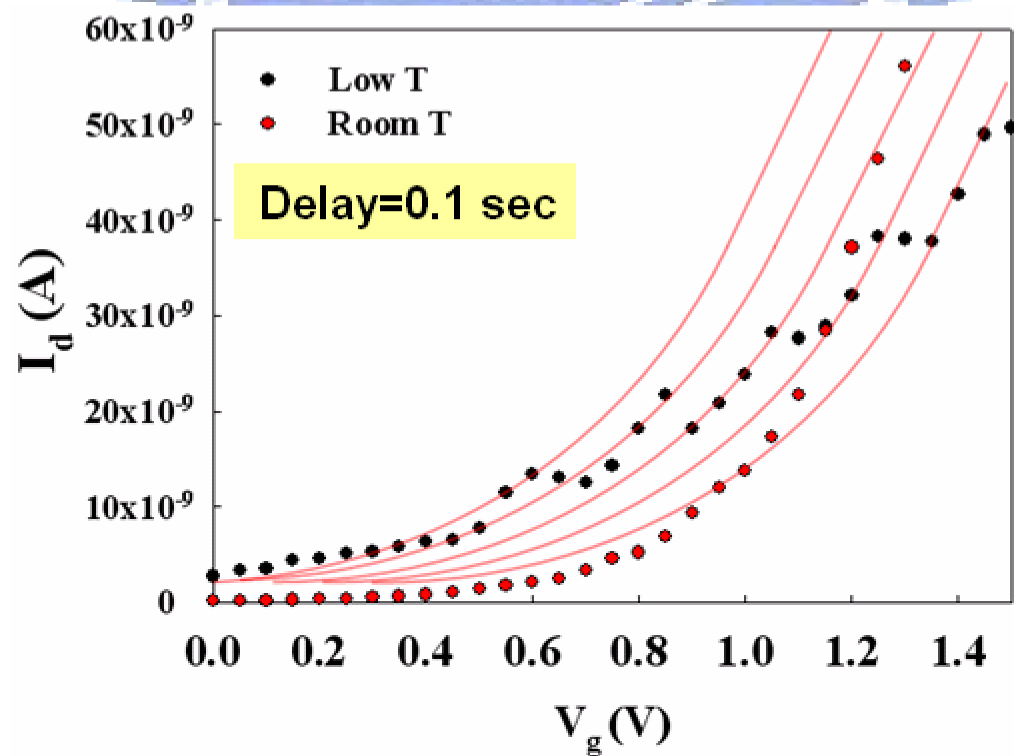


Fig. 5.11 Drain current versus gate voltage characteristic.





(a)



(b)

Fig. 5.12 Drain current versus gate voltage characteristic at low temperature (40°K) for different swept times. (a) delay=0 sec. (b) delay=0.1sec.

Chapter 6

2-Bit Lanthanum Oxide Trapping Layer Nonvolatile Flash Memory

6.1 Introduction

Silicon–oxide–nitride–oxide–silicon (SONOS) charge trapping-based nonvolatile memories have received a considerable amount of interest recently [6.1–6.3]. Obtaining nonvolatile, low-power, fast memories with short dimensions remains a key challenge in the electronics industry. According to the International Technology Roadmap for Semiconductors (ITRS) [6.4], the key issue for floating-gate nonvolatile semiconductor memories is the scaling of the tunneling oxide; the stress-induced leakage current (SILC), which can discharge the whole floating-gate memory with even one single defect, becomes a severe problem at very thin tunneling oxide thicknesses. This scaling issue remains a formidable challenge, especially for emerging system-on-chip (SOC) integrated circuit designs in which the programming voltage must be scaled for the nonvolatile memories to be compatible with low-voltage logic circuits. High-k dielectric materials, such as hafnium oxide (HfO_2) and lanthanum oxide (La_2O_3), are promising candidates to replace Si_3N_4 films as the charge trapping layer of SONOS-type Flash memories [6.5]. Such high-κ dielectric films are expected to exhibit better charge trapping characteristics than are displayed by conventional Si_3N_4 films; their sufficient densities of trap states and deep trap energy levels should result in longer retention times [6.6-6.7]. This feature suggests that HfO_2 will be more practical for further scaling of the tunnel oxide to enhance the performance and more suitable for the development of SONOS-type memories that

perform multi-bit operations [6.8-6.9]. Moreover, a greater voltage drop at the tunnel oxide can be obtained when using the high-k material as the trapping layer. Therefore, low-power, high-speed operation at short dimensions is achievable for high-k SONOS-type memories.

In this chapter, we prepared high-k SONOS-type memories incorporating lanthanum oxide (La_2O_3) as the trapping layer. These memories exhibit good characteristics: considerably large memory windows, high speed programming/erasing, good retention times, high endurance, and low disturbance.

6.2 Experimental

Figure 6.1 displays the structure and process flow for the preparation of the La_2O_3 high-k memories. The fabrication of the La_2O_3 memory devices involved the LOCOS isolation process on p-type, 5–10 Ω cm, (100) 150-mm silicon substrates. First, a 2-nm-thick tunnel oxide was grown thermally at 1000 °C in vertical furnace system. Next, a 4-nm-thick lanthanum oxide layer was deposited using the E-gun method with La_2O_3 targets. Subsequently, the samples were subjected to RTA treatment under an O_2 ambient at 900 °C for 1 min. A blocking oxide (ca. 7 nm) was deposited using high-density-plasma chemical vapor deposition (HDPCVD) followed by a N_2 densification process at 900 °C for 1 min. Poly-Si deposition, gate lithography, gate etching, source/drain (S/D) implanting, substrate and contact patterning, followed by the rest of the subsequent standard CMOS procedure, were then performed to complete the fabricating of the La_2O_3-containing high-k SONOS-type memory devices.

6.3 Results and Disscussion

6.3.1 Devices Operation

Figure 6.2 shows the cross-sectional high-resolution transmission microscopy (HRTEM) images of the gate stacks of the La_2O_3 Flash memory. For SONOS-type structure, the thicknesses of the tunnel oxide, La_2O_3 trapping layer, and blocking oxide layer are 2nm, 4nm, and 7nm, respectively. For the operation of our La_2O_3 SONOS-type memory, we employed channel hot-electron injection and band-to-band hot-hole injection for the programming and erasing, respectively. All devices described in this paper had dimensions of L/W = 2/1 μm. Figure 6.3 demonstrates the feasibility of performing two-bit operation with our La_2O_3 SONOS-type memory through a forward read and reverse read scheme in a single cell [6.10]. From the I_{ds}–V_{gs} curves, it is clear that we could employ forward and reverse reads to detect the information stored in the programmed bit1 and bit2, respectively. The read operation was achieved using a reverse read scheme. Table 6.1 summarizes the bias conditions for two-bit operation.

Program characteristics as a function of pulse width for different operation conditions are shown in fig. 6.4. Both source and substrate terminals were biased at 0V. The "V_t shift" is defined as the threshold voltage change of a device between the programmed and the erased states. With V_d=V_g=9V, relatively high speed (t=100μs) programming performance can be achieved with a memory window of about 2.2V. Meanwhile, Fig. 6.5 displays the erase characteristics as a function of various operation voltages. Again, excellent erase speed of a memory window around 10 ms can be obtained. More important, there is only a very small amount of over-erase observed. The reason is owing to the fact that we use the band-to-band hot-hole injection, the vertical electric field will decrease with decreasing amount of trapped electrons in the trapping layer during erasing and the hole injection into the trapping

layer will reduce significantly.

Figure 6.6 illustrates the retention characteristics observed at temperatures of 25, 85, and 125 °C. At room temperature, the charge loss of the memory incorporating the La_2O_3 trapping layer was below 19% after 10^8 s; this behavior is probably related intimately to the trap energy level in high-κ dielectrics [6.11]. The retention behavior deteriorated, however, as the temperature increased: we obtained 38 and 63% charge losses at 85 and 125 °C, respectively, after 10^8 s. We calculated the activation energy of the traps in the La_2O_3 layer of a fresh device. Activation energy tracing is used widely to characterize the Arrhenius relation extracted from the temperature dependence of charge loss in a nonvolatile memory as a function of time. For a given charge-loss threshold criterion (in our case, 20%), the failure rates obtained at higher temperatures (125–200 °C), with five measurements at each temperature, were then extrapolated to the nominal operating conditions. We obtained an extracted activation energy of 1.25 eV for the La_2O_3 trapping layer. Obviously, this value is higher than those reported previously for conventional SONOS memories [6.12–6.14].

Figure 6.7 displays the endurance characteristics after 10^5 P/E cycles (programming conditions: $V_g = V_d = 10$ V for 100 μs; erasing conditions: $V_g = -3$V, $V_d = 10$ V for 1 ms). A slight memory window narrowing occurred and individual threshold voltage shifts become visible in the program and erase states after 10^2 cycles. This finding suggests the formation of operation-induced trapped electrons. Certainly, this feature is related intimately to the use of the ultra-thin tunnel oxide and the minute amount of residual charge remaining in the La_2O_3 layer after cycling.

6.3.2 Disturbances

Figure 6.8 shows the programming drain disturbance of our La_2O_3 SONOS-type

memory. Three different drain voltages (V_d = 5, 7 and 9 V) were applied in the programming drain disturbance measurements at room temperatures. We observed that a sufficient programming drain disturb margin exists (ΔV_t < 1 V), even after programming at a value of V_d of 9V under room temperature and after stressing for 1000 s. Figure 6.9 shows the gate disturbance characteristics in the erasing state. Gate disturbance may occur during programming for the cells sharing a common word-line while one of the cells is being programmed. We observed a threshold voltage shift of only 0.9V under the following conditions: V_g = 10 V; V_s = V_d = V_{sub} = 0 V; stressed for 1000 s. Because of the small voltage drop at the tunnel oxide by using a serial capacitor voltage divider model, this memory can exhibit such good gate disturb characteristics with such a thin tunnel oxide.

Figure 6.10 demonstrates the read disturbance induced erase-state threshold voltage instability in a localized La_2O_3 trapping storage Flash memory cell under several operation conditions. For two-bit operation, the applied bitline voltage in a reverse-read scheme must be sufficiently large (>2 V) to be able to "read through" the trapped charge in the neighboring bit. The read-disturb effect is the result of two factors: the word-line and the bit-line. The word-line voltage during read may enhance room temperature (RT) drift in the neighboring bit [6.15]. On the other hand, a relatively large read bit-line voltage may cause unwanted channel hot-electron injection and, subsequently, result in a significant threshold voltage shift of the neighboring bit. In our measurements, the gate and drain biases were applied and the source was grounded. The results demonstrate clearly that almost no read disturbance occurred in our La_2O_3 Flash memory under low-voltage reading (V_g = 3 V; V_d = 2.5 V). For a larger memory window, we found that only a small read disturbance (ca. 0.3 V) can be observed after operation at V_d = 4 V after 1000 s at 25 °C.

6.4 Summary

In this chapter, we have investigated the memory effect on the performance of the La_2O_3 SONOS-type memories. It has good characteristics in terms of large memory windows, high speed program/erase, good retention time, excellent endurance, and 2-bit operation. Hence, La_2O_3 are the candidates used for the trapping layers for the SONOS-type memories.

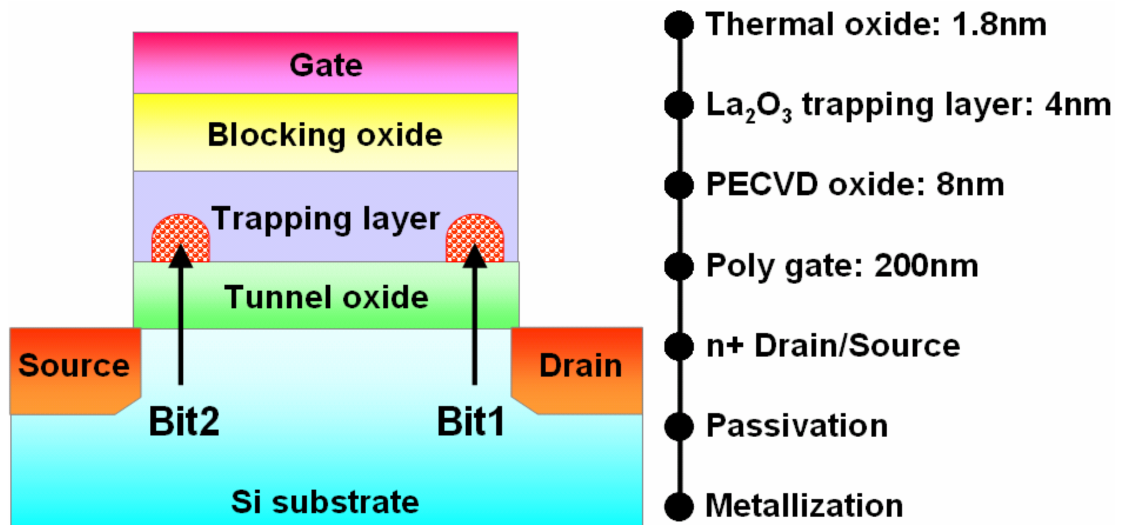


Fig. 6.1 Schematic representation of the La_2O_3 SONOS-type Flash memory cell structure and localized charge storage.

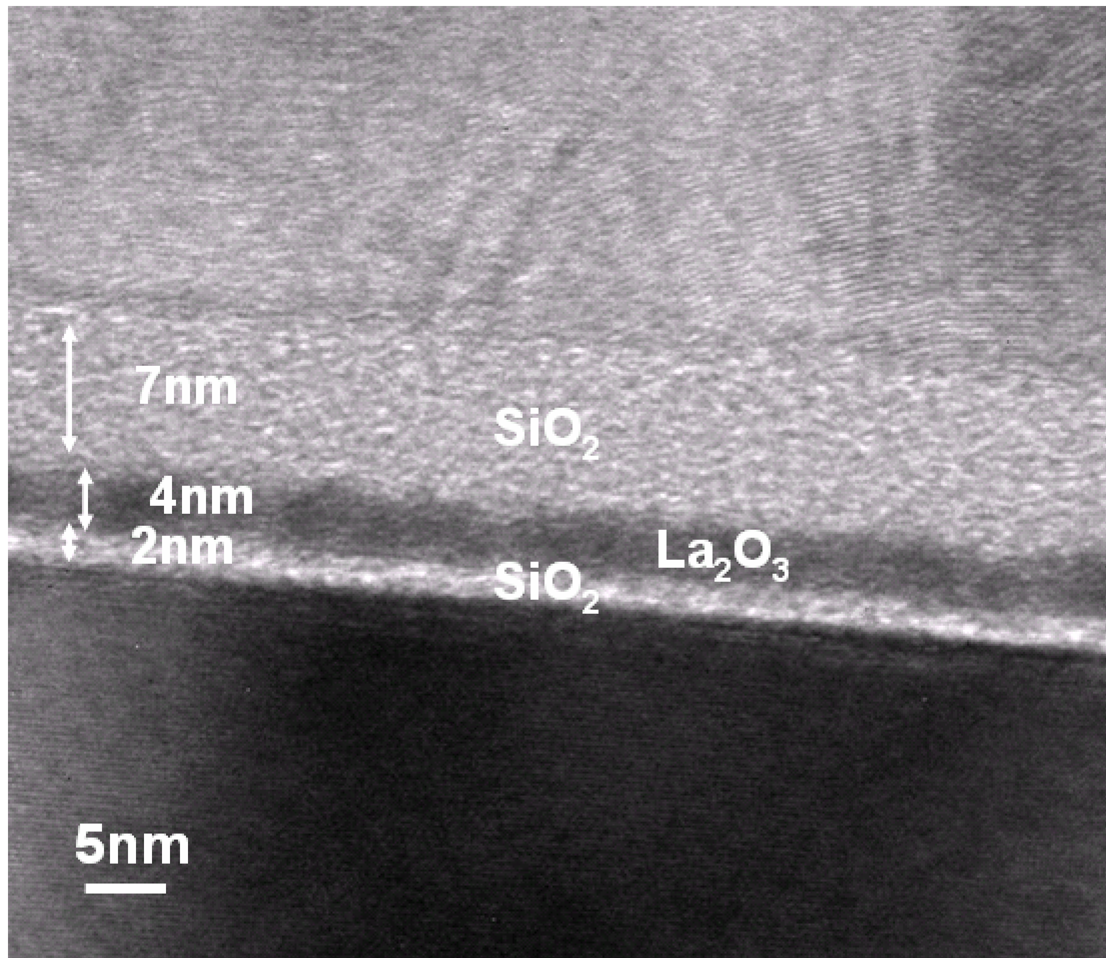


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Fig. 6.2 Planar-view HRTEM image of the La_2O_3 SONOS-type memory.

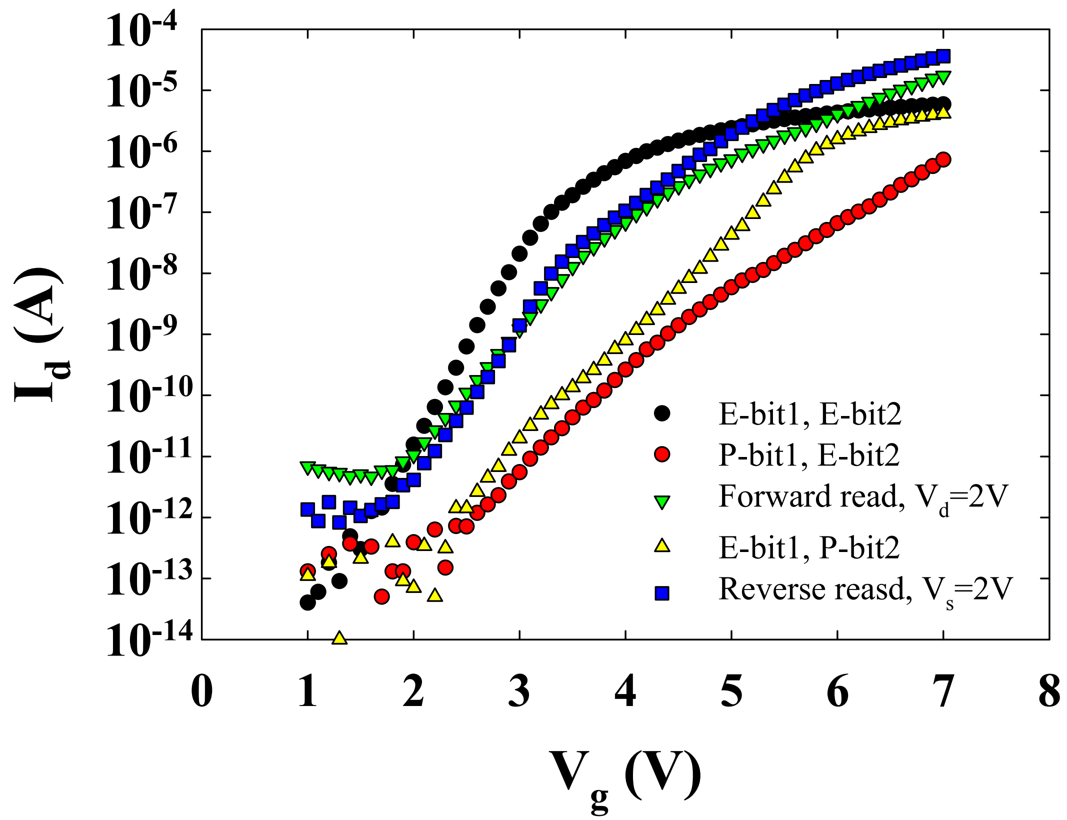

Fig. 6.3 I_{ds}–V_{gs} Curves of the two-bit memory in a cell; forward read and reverse read for programmed bit1 and programmed bit2.

		Program	Erase	Read
Bit 1	Vg	10V	-3V	4V
	Vd	10V	10V	0V
	Vs	0V	0V	>3V
Bit 2	Vg	10V	-3V	4V
	Vd	0V	0V	>3V
	Vs	10V	10V	0V

Table 6.1 Operation principles and bias conditions utilized during the operation of the La_2O_3 SONOS-type memory cell.

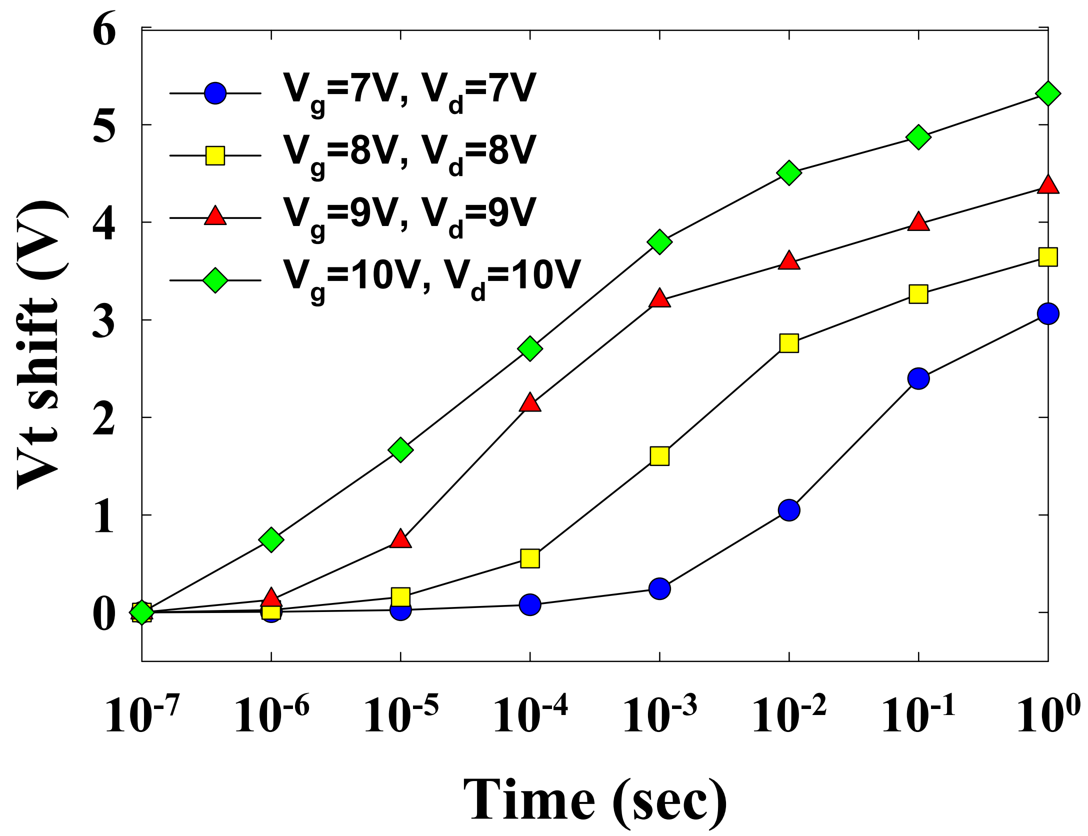

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Fig. 6.4 Program speed of the La_2O_3 SONOS-type memory

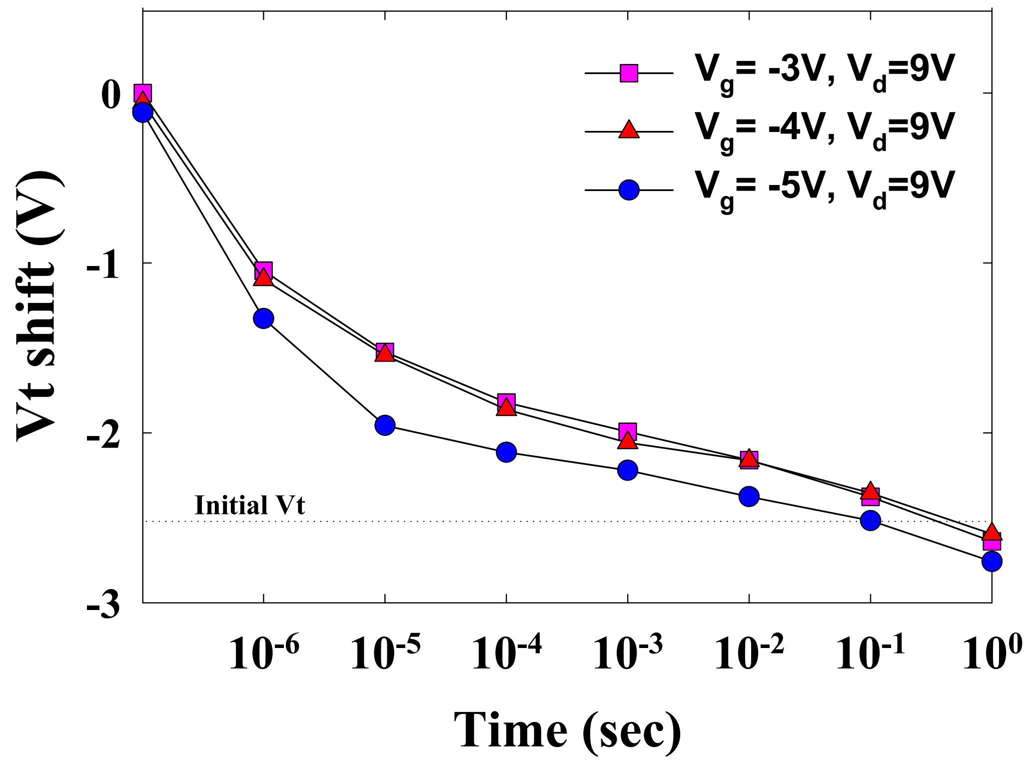

Fig. 6.5 Erase speed of the La_2O_3 SONOS-type memory.

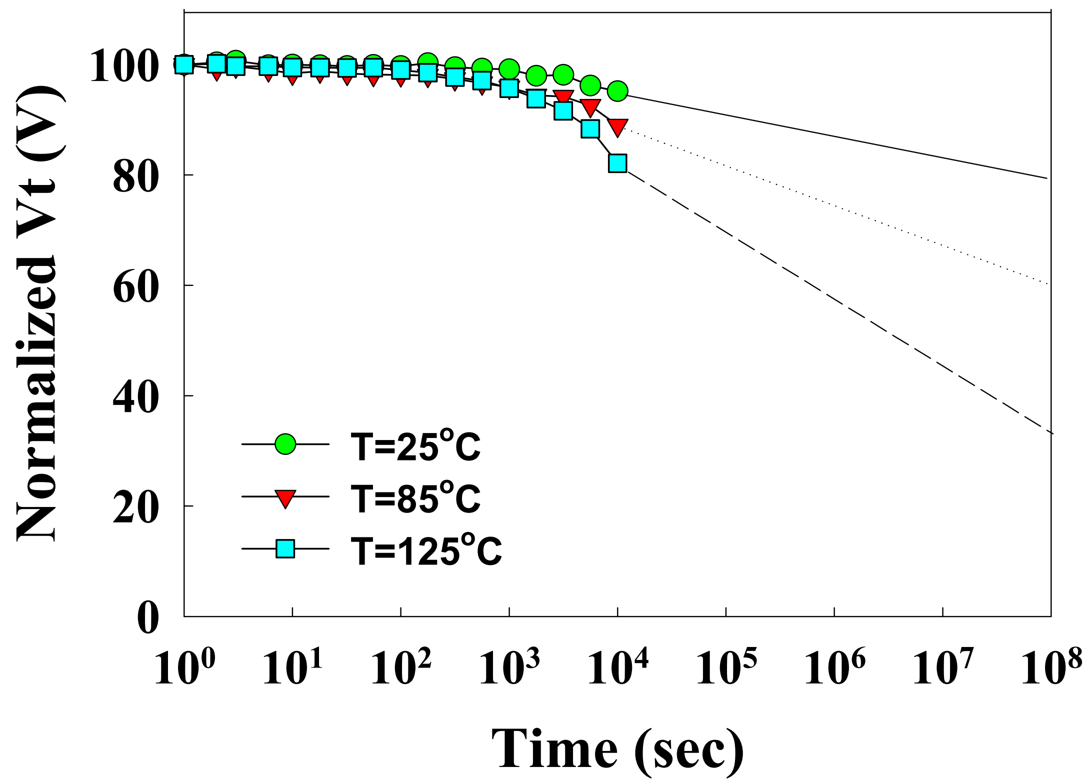

Fig. 6.6 Retention of. the La_2O_3 SONOS-type memory for three temperature (T=25°C, 85°C,and 125°C). 22% charge loss occurred at 25 °C; and 40% charge loss occurred at 125 °C up to 10^8 sec..

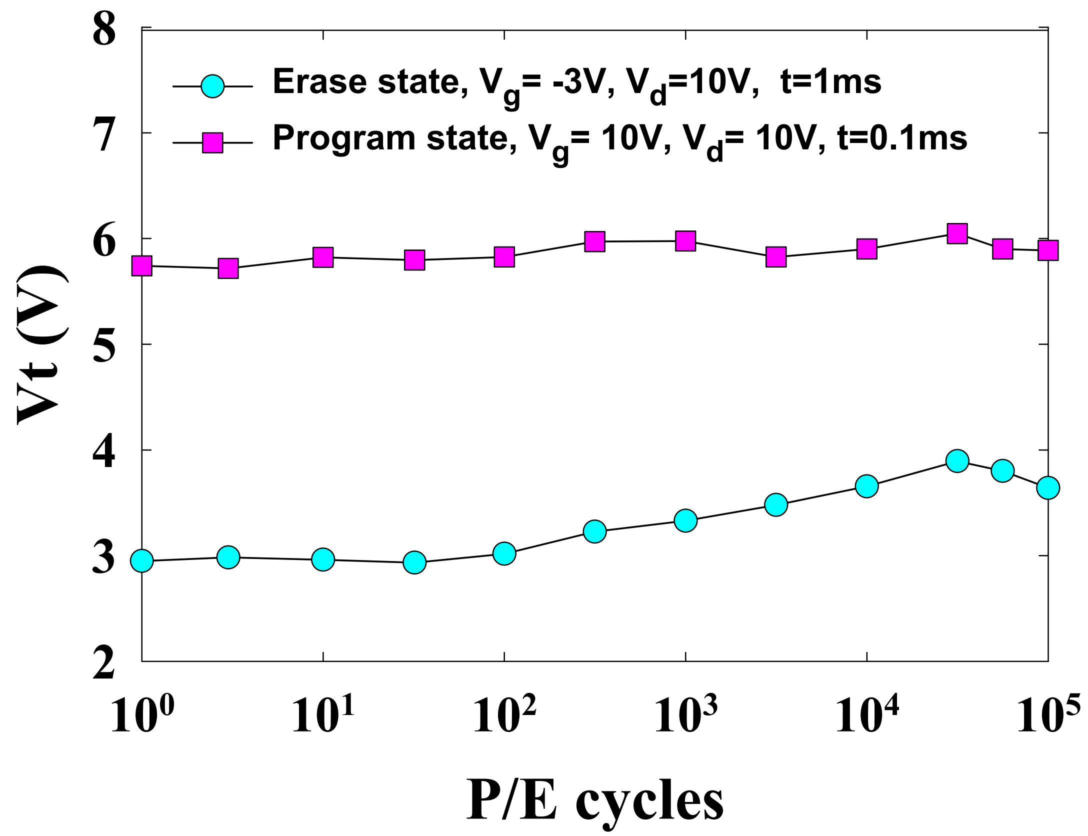

Fig. 6.7 Endurance characteristics of the La_2O_3 SONOS-type memory after 10k P/E cycling.

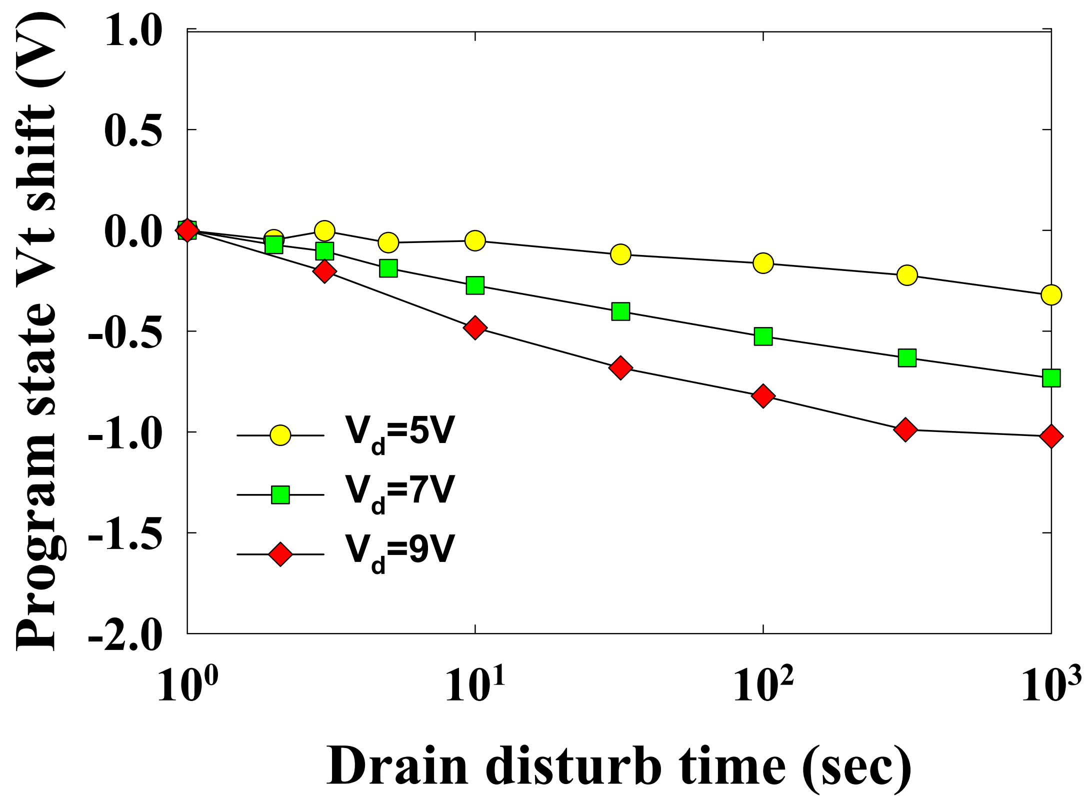

Fig. 6.8 Drain disturbance characteristics of the La_2O_3 SONOS-type memory. After 1000 s at 25 °C, only a 1V drain disturb margin was observed.

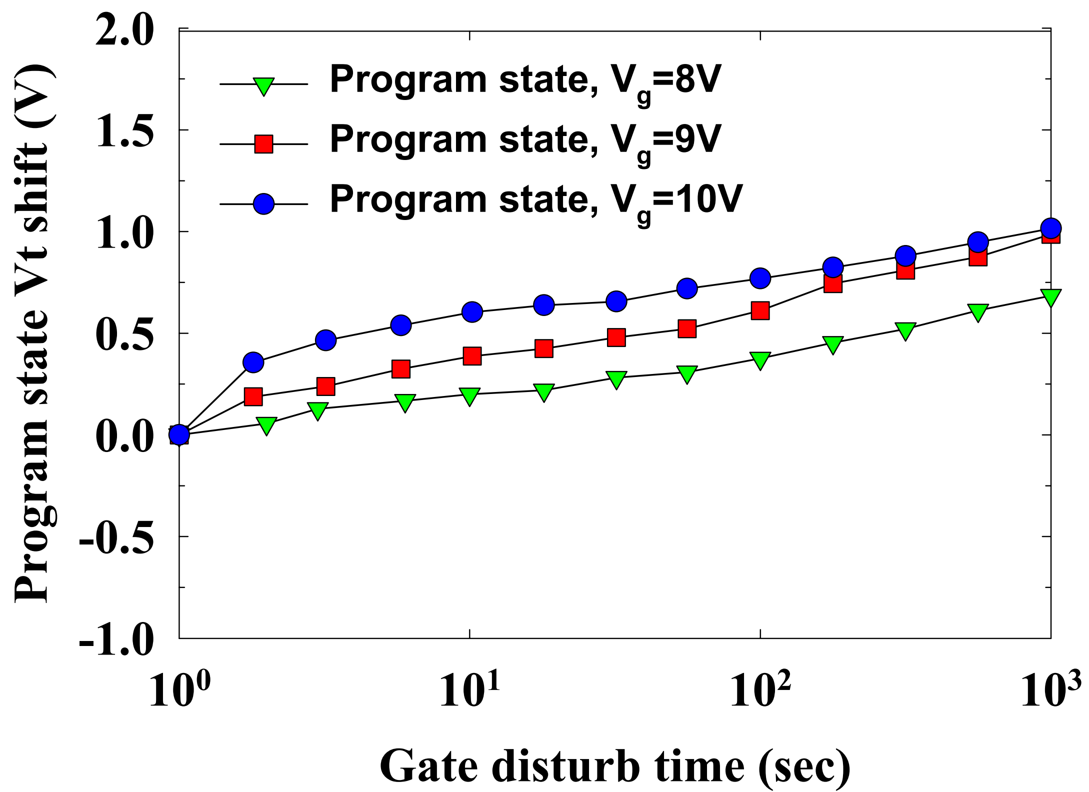

Fig. 6.9 Gate disturbance characteristics of the La_2O_3 SONOS-type memory. A threshold voltage shift of only 1 V occurred after stressing at V_g = 10 V and V_s = V_d = V_{sub} = 0 V for 1000 s.

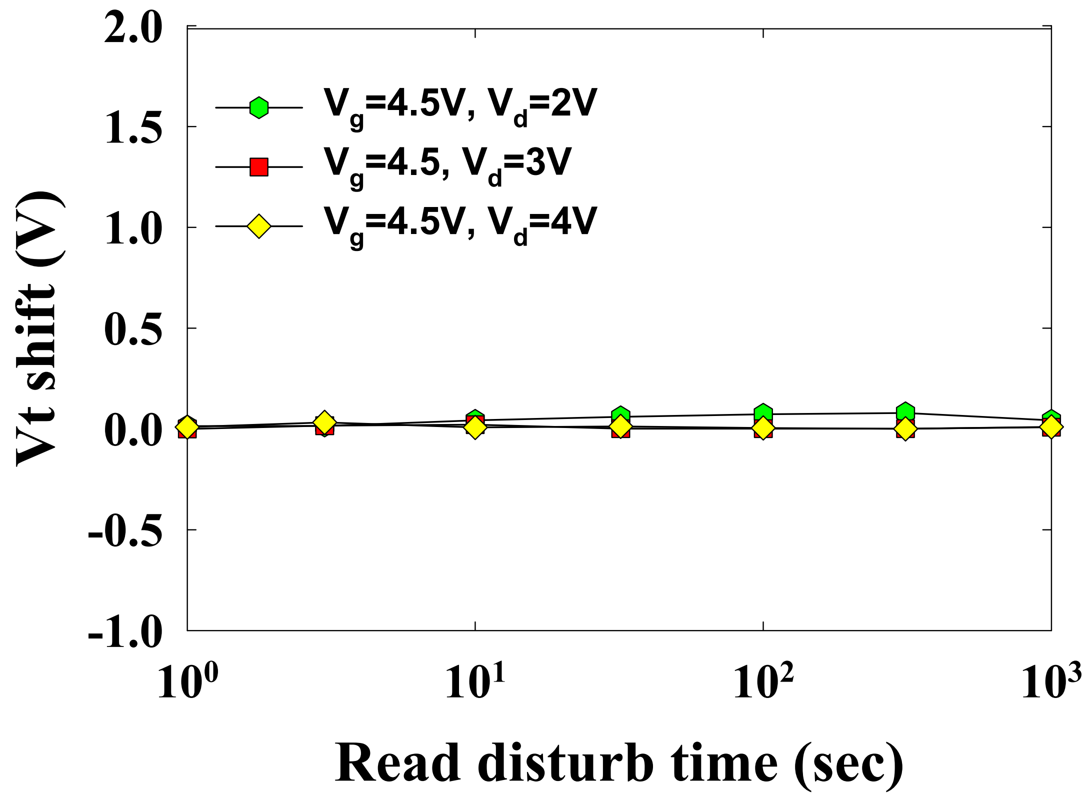

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Fig. 6.10 Read disturbance characteristics of the La_2O_3 SONOS-type memory devices. No significant V_t shift occurred for $V_d < 4$, even after 1000 s at 25 °C.

Chapter 7

Conclusions and Further Recommendations

7.1 Conclusions

In this thesis, for the chapter 2, we propose a novel, simple, reproducible, and reliable technique for the design of high-density HfO_2 nanocrystals through the spinodal decomposition of hafnium silicate. Our nanocrystal memory exhibits superior characteristics in terms of negligible lateral or vertical migration of stored charge and good disturbance characteristics. The cells after 10k P/E cycling also show a long retention time and excellent endurance. With these superior performance, we believe that HfO_2 nanocrystal Flash memory is quite suitable for the two-bit operation and that it has great potential for replacing the ONO stack in conventional SONOS-type Flash memory.

Then, in the chapter 3, we have investigated the effect of post-deposition annealing temperature on the performance of the resultant HfO_2 SONOS-type Flash memories. Higher temperature treatment can have large memory windows due to the crystallization-induced trap generation whereas lead to poorer retention and endurance performances. Moreover, we found that the HfO_2 trapping layer can trap both electrons and holes. No significant read, drain and gate disturbances were observed for three samples. HfO_2 SONOS-type Flash memory is considered to be a promising candidate for the Flash memory devices application.

In this chapter 4, we have studied three kinds of high-k dielectrics, including HfO_2, Hf-silicate and Zr-silicate for the trapping layer of the poly-Si TFT memory devices with two different thickness tunnel oxides. By sticking with sufficiently low

thermal-budget processing, we have successfully demonstrated the feasibility of fabricating nonvolatile poly-Si TFT memories with excellent characteristics in terms of large memory windows, good speed program/erase, long retention time and 2-bit operation. Moreover, the poly-Si grain boundary is the concerned issues about the disturbance characteristics. We demonstrated that the reliability characteristics of a poly-Si-TFT memory device in terms of retention, drain and gate disturbance are closely related to the defects along the grain boundaries in the channel. The NH_3 plasma treatment is one of the useful methods to improve the SiO_2/poly-Si interface and the channel quality because it can effectively eliminate the trap densities in both regions. These poly-Si TFT memories make the realization of producing the embedded nonvolatile memories for system on the panel.

In this chapter 5, we have proposed a novel simple, reproducible, reliable technique for preparation of 50nm nano-scaled tri-gate HfO_2 nanocrystals using spinodal decomposition of hafnium silicate on SOI and achieved nanocrystal memories with characteristics in terms of large memory windows, high speed program/erase, retention time, and good endurance. Few Electron Phenomena at 40°K has been observed clearly. Discontinuities appear, that is corresponding to discharging of few electron from HfO_2 nanocrystals.

In chapter 6, we have investigated the memory effect on the performance of the La_2O_3 SONOS-type memories. It has good characteristics in terms of large memory windows, high speed program/erase, good retention time, excellent endurance, and 2-bit operation. Hence, La_2O_3 are the candidates used for the trapping layers for the SONOS-type memories.

7.2 Further Recommendations

There are some interesting topics for further study. First, for the nanocrystal, we can use other high-k materials such ZrO2 nanocrystal. Moreover, we can change the SiO2 base to the Al2O3 base. Second, we can change other high-k dielectric trapping layer such as Pr2O3 and CeO2. Third, high-k PMOS Flash memory can realize. Final, we can use High-k dielectric tunnel oxide to obtain high speed operation.

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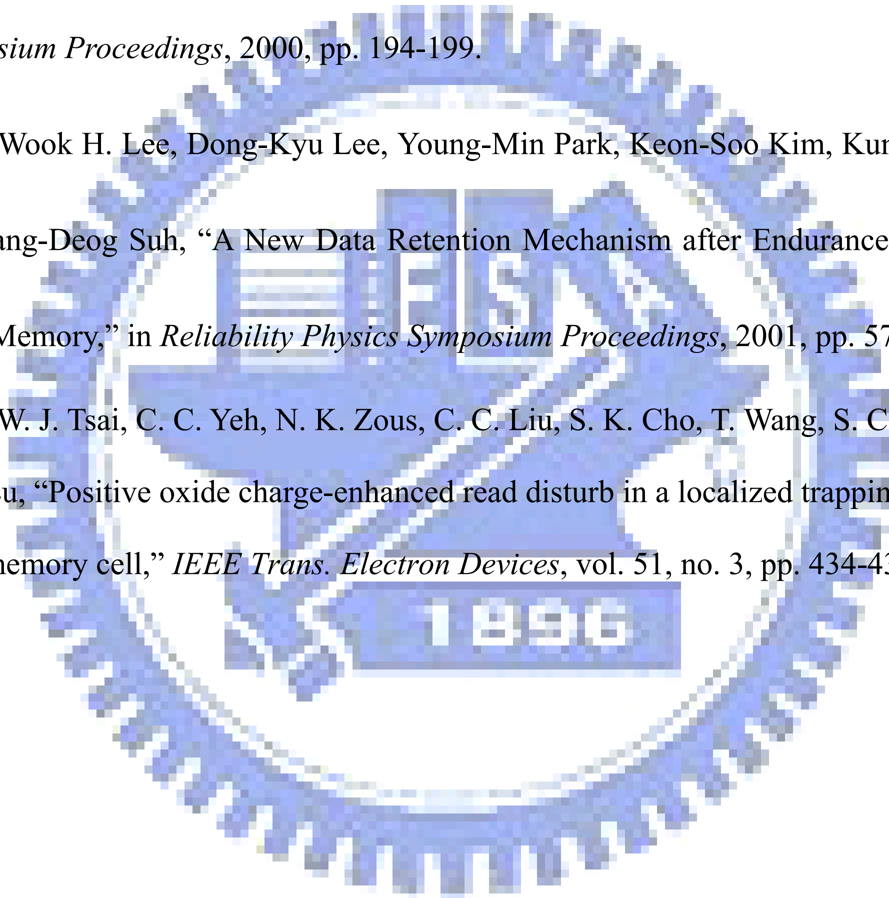

學經歷

姓名: 林育賢

性別: 男

出生: 民國 68 年 6 月 18 日

籍貫: 台灣省宜蘭縣

住址: 宜蘭縣擺厘路 15 巷 2 弄 6 號

學歷: 國立交通大學電子系 [86 年 9 月 - 90 年 6 月]

國立交通大學電子研究所碩士班 [90 年 9 月 - 91 年 7 月]

國立交通大學電子研究所博士班 [91 年 8 月 - 95 年 6 月]

博士論文題目:

新穎高介電常數材料與奈米微晶粒非揮發性記憶體之研究

Study on novel nonvolatile memory with high-k dielectric materials and nanocrystals

Publication Lists

1. International Journal:

[1] **Yu-Hsien Lin**, Chao-Hsin Chien, Ching-Tzung Lin, Chun-Yen Chang, and Tan-Fu Lei, "Novel Two-Bit HfO_2 Nanocrystal Nonvolatile Flash Memory**",** *IEEE Trans. Electron Devices*, vol. 49, pp. 782 – 789, Apr. 2006.

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[3] **Yu-Hsien Lin**, Chao-Hsin Chien, Tung-Hung Chou, Tien-Sheng Chao, and Tan-Fu Lei, "Low-Temperature Polycrystalline Silicon Thin-Film Flash Memory with Hafnium Silicate", submitted to *IEEE Trans. Electron Devices*.

2. International Letter:

[1] **Yu-Hsien Lin**, Chao-Hsin Chien, Ching-Tzung Lin, Chun-Yen Chang, and Tan-Fu Lei, **"**High Performance Nonvolatile HfO_2 Nanocrystal Memory**"**, *IEEE Electron Device Lett.*, vol. 26, no. 3, pp. 154-156, Mar. 2005.

[2] **Yu-Hsien Lin**, Chao-Hsin Chien, Tung-Hung Chou, Tien-Sheng Chao, and Tan-Fu Lei, "2-bit Poly-Si-TFT Nonvolatile Memory Using Hafnium Silicate Trapping Layer", submitted to *Applied Physics Letters*.

[3] **Yu-Hsien Lin**, Chao-Hsin Chien, Tung-Hung Chou, Tien-Sheng Chao, and Tan-Fu Lei, "Impact of channel dangling bonds on reliability characteristics of Flash memory on polycrystalline-silicon thin films", submitted to *Applied Physics Letters*.

3. International Conference:

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4. Local Conference:

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6. Patents

[1] “利用矽酸鉿奈米微粒備製之非揮發性快閃記憶體”, 中華民國專利已領證。

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