# 國立交通大學

## 電子工程學系 電子研究所

## 博士論文

# 新穎低溫複晶矽薄膜電晶體與前瞻非揮發性記憶體元件之製作與特性研究

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中華民國 九十六 年 三 月

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## 中文摘要

本論文首先提出以鈍化方式來提昇低溫複晶矽薄膜電晶體(Poly-Si TFTs)的特性以及元件的可靠度。本論文提出在非晶矽薄膜沈積後，以氟(F)離子佈植的方式，先預先植入非晶矽薄膜中，其佈植劑量為 $5\times10^{13}\mathrm{cm}^{-2}$。經過傳統的固態結晶技術（SPC）之後，再進行後續的元件製作。我們發現經過氟離子佈植過後的複晶矽薄膜電晶體其元件特性相較於傳統的固態結晶的薄膜電晶體，有比較低的起始電壓($V_{TH}$), 較低的次臨界導通特性(S.S), 以及較高的載子移動率($\mu_{FE}$)。此乃由於氟離子佈植會降低複晶矽薄膜中本身的缺陷(trap)，包括淺能階(tail state)以及深能階(deep state)的缺陷，進而提昇元件的特性。相較於傳統的氟離子佈植的鈍化方法，在做熱結晶前並沒有額外的氧化層沈積。經過固態熱結晶後，薄膜中的氟離子會聚積到複晶矽的表面，以及複晶矽與緩衝氧化層(buffer oxide)的介面，此乃氟離子會受熱而往氧化層聚積。複晶矽表面的原生氧化層(native oxide)同時也具有使氟離子聚積的驅動力。這不但可以將傳統以氟離子佈植來鈍化複晶矽薄膜電晶體的技術的製程步驟減少，以及減少元件製程的複雜度。更進一步地討論，當氟離子佈植劑量提高到 $5\times10^{15}\mathrm{cm}^{-2}$ 時，元件的特性卻造成劣化，此乃因為過多的佈植劑量將無法完全溶解在複晶矽薄膜中，形成額外的缺陷，卻降低了低溫複晶矽薄膜電晶體的特性。其經過氟離子佈植後而進行固態熱結晶的複晶矽晶粒尺寸也在此被討論，我們發現複晶矽晶粒大小並沒有隨著佈植劑量有改變。因此，其元件特性的提昇乃是由於氟離子的鈍化造成的結果。

同樣地，我們也發現以準分子雷射(excimer laser)進行雷射結晶的低溫複晶矽薄膜電晶體，也與傳統的固態結晶方法結晶的技術有相似的結果。由於雷射結晶是個快速的製程步驟，複晶矽薄膜以及緩衝氧化層也因快速的熱膨脹造成額外的缺陷密度。往複晶矽與緩衝氧化層介面聚積的氟離子將可以消除雷射結晶所造成額

外的缺陷密度。我們也發現過高的氟離子佈植劑量也會造成元件特性的劣化。此乃由於複晶矽薄膜本身對氟離子的固態溶解度的問題。同時，我們發現以氟離子佈植劑量為 $5\times10^{13}\text{cm}^{-2}$ 時，複晶矽晶粒比起傳統以及高劑量的複晶矽晶粒要來的大。因此，元件特性的提昇乃因為晶粒尺寸提昇以及氟離子鈍化的結果。

我們同時也對經氟離子佈植的低溫複晶矽薄膜電晶體元件做可靠度的探討。我們發現經過氟離子佈植過後的元件具有較高的直流(DC)偏壓下的電性可靠度，包括較低的起始電壓的漂移、次臨界特性漂移、以及導通電流漂移。此乃因為佈植的矽－氟(Si-F)鍵取代矽－矽(Si-Si)以及矽－氫(Si-H)，使得較強鍵結的矽－氟鍵可以抵抗電流的衝擊，造成可靠度的提昇。更進一步地討論，我們也發現氟離子佈植劑量為 $5\times10^{13}\text{cm}^{-2}$ 的時候，其載子移動率可以提昇到兩倍。而氟離子佈植應用在準分子雷射結晶的元件上，具有較為明顯的可靠度提昇。此乃因為以雷射結晶的元件具有較低的薄膜缺陷密度，使得後續的電流衝擊也不致破壞元件的可靠度。事實上，也發現矽－氟鍵的強鍵結可以抵抗由於準分子雷射結晶造成較高的載子移動率，造成較低的劣化程度。因此，氟離子佈植在結晶前的應用技術，更適用在以雷射結晶的方法。

以新結構方式來提高低溫複晶矽薄膜電晶體元件的可靠度，在此論文也提出來討論。我們提出以具氟摻雜的氧化矽（F-incorporated $SiO_x$,FSG）作為新穎的側壁子(spacer)材料。側壁子結構可以降低元件在汲極端的高電場，可以降低載子得到高的撞擊能量而造成斷鍵。具氟摻雜的氧化矽在複晶矽的表面產生保護的作用，相較於傳統以氧化矽為側壁子材料的低溫複晶矽薄膜電晶體具有壓抑的扭結效應(kink effect)，以及較明顯的可靠度提昇。

本論文同時也針對非揮發性記憶體元件做研究。我們提出兩種氮化矽鍺的堆疊結構氮化矽鍺(SiGeN)作為鍺奈米點(Ge nanocrystal)的自我析出層(self-assembling layer)，其一為以厚的氮化矽鍺作為自我析出層；其二為在氮化矽鍺沈積後，隨即成長非晶矽薄膜（a-Si）。經過高溫熱氧化後，鍺奈米點會自我析出在氮氧化矽(SiON)薄膜中。厚的氮化矽鍺薄膜堆疊結構以長時間的熱氧化來析出鍺奈米點，隨即形成較厚的氮氧化矽作為阻擋氧化層；而具非晶矽薄膜的堆疊結構以短時間的熱氧化來析出鍺奈米點，隨即再經由高溫水氣處理後，提昇阻擋氧化層自身的品質，可以抵抗儲存的電荷流失至閘極金屬。其明顯的記憶視窗(memory window)是來自於鍺奈米點的貢獻。

我們也針對傳統的氮氧化矽作為載子儲存層的堆疊結構，以及矽鍺薄膜作為鍺奈米點自我析出層的結構做比較。我們發現本論文所提出的鍺奈米點埋在氮氧化矽的結構，其得到的記憶體效應比傳統的氮氧化矽薄膜，以及鍺奈米點埋在氧化層中的堆疊結構還大。甚至其記憶體效應比兩者的疊加結果還要大，此乃因為鍺奈米點埋在氮氧化矽為主的載子儲存層中，會產生額外的儲存中心，進而增進記憶體效能。

# Fabrication and Characterization of Novel Low Temperature Polycrystalline Silicon Thin-Film Transistors and Advanced Nonvolatile Memory

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## Abstract

Passivation methods were proposed in low temperature polycrystalline silicon thin film transistors (Poly-Si TFTs) to improve the electrical performance and reliability. Fluorine ions with dosage of $5\times10^{13}\text{cm}^{-2}$ are pre-implanted into amorphous silicon (a-Si) before solid phase crystallization (SPC). The F-ion-implanted poly-Si TFTs have lower threshold voltage ($V_{TH}$), lower subthrshold swing ($S.S$), and higher field effect mobility ($\mu_{FE}$), due to the trap state reduction, including tail states and deep states. Compared to conventional F ions implantation, there is no extra pad oxide deposition before thermal crystallization. The F ions segregated to the surface of poly-Si and the interface between poly-Si and buffer oxide. The surface-oxidized a-Si layer drives the F ions to segregate the surface of active layer. This process steps and

difficulty are reduced by directly crystallization method. Furthermore, the electrical characteristics are degraded for implantation dosage is up to $5\times10^{15}$cm$^{-2}$, due to the extra trap state generation for F ions can not effectively dissolve into poly-Si. In addition, the grain sizes of the F-ions-implanted poly-Si are also discussed in this study. There is no obviously difference for various dosages of implantation. Hence, the improvement of electrical characteristics is resulted from the F ions passivation.

The F-ions-implanted poly-Si TFTs was also fabricated using excimer laser crystallization (ELC). Some interesting experimental results are observed in the F-ions-implanted poly-Si TFTs. Furthermore, the rapid thermal expansion between poly-Si and buffer oxide causes extra trap state due to the rapid ELC process step. The segregated F ions at the interface between poly-Si and buffer oxide can passivate the thermal generated trap states. The degraded electrical characteristics are found at higher implantation dosage. The grain size at implantation dosage of $5\times10^{13}$cm$^{-2}$ is obviously enlarged compared to conventional and higher implanted poly-Si. Hence, the performance improvement is resulted from grain size enhancement and passivation effect.

The electrical reliability for F-ions-implanted poly-Si TFTs is also investigated. The superior electrical reliability for DC stress are found for F-ions-implanted poly-Si TFTs, including $\Delta V_{TH}$, $\Delta S.S$, and $\Delta I_{ON}/I_{ON}$, due to strong Si-F bonds replace Si-Si and Si-H bonds. Furthermore, the $\mu_{FE}$ for F-ions-implanted poly-Si TFTs is twice to conventional poly-Si TFTs. In addition, the obviously electrical reliability improvement is found by using ELC method. It is considered that the lower trap state density in F-ions-implanted poly-Si for ELC method. In fact, strong Si-F bonds can resist the higher field effect mobility for poly-Si TFTs by ELC method. Hence, the pre-implanted technology is more suitable on the ELC method.

The novel structure on low temperature poly-Si TFTs is also discussed in this study. The F-incorporated $SiO_x$ (FSG) is proposed to serve as spacer material. The spacer reduces the high electrical field at drain side and the broken bonds for high impact energy. The FSG passivates the surface of poly-Si leads to suppressed kink effect and improved electrical reliability.

In addition, the nonvolatile memory device was also discussed in this study. We proposed novel material-SiGeN serving as Ge nanocrystals seft-assembling layer for two kinks of the stacked structures. One is thicker SiGeN layer, the other is the stacked structure for SiGeN layer plus a-Si layer. The Ge nanocrystals are nucleated in silicon-oxygen-nitride (SiON) layer after thermal oxidation. The long dry oxidation was performed for thicker SiGeN layer to nucleate Ge nanocrystals and form thicker SiON as blocking oxide. In addition, the steam treatment was performed for the stacked structure with SiGeN layer plus a-Si layer to improve the quality of blocking oxide to resist the stored charge leaking to gate pad. The obvious memory window is resulted from Ge nanocrystals.

The stacked structure for conventional SiON charge trapping layer and SiGe self-assembling layer to form Ge nanocrystals are also fabricated. The memory window for the stacked structure with Ge embedded in SiON layer is larger than SiON trapping layer and Ge embedded in $SiO_2$ layer. The memory window is even lager than the combination of SiON and Ge nanocrystals in $SiO_2$ layer. It is due to the extra charge trapping centers generation for Ge nanocrystal embedded in SiON layer.

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2007 年 3 月于新竹交大

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# Chapter 1

# Introduction

## 1.1 Overview of Poly-silicon Thin-Film Transistor Technology

In recent years, polycrystalline silicon thin film transistors (poly-Si TFTs) have been drawn much attention because of their widely applications on active matrix liquid crystal displays (AMLCDs) [1.1], and organic light-emitting displays (OLEDs) [1.2]. Except large area displays, poly-Si TFTs also have been applied into some memory devices such as dynamic random access memories (DRAMs) [1.3], static random access memories (SRAMs) [1.4], electrical programming read only memories (EPROM) [1.5], electrical erasable programming read only memories (EEPROMs) [1.6], linear image sensors [1.7], thermal printer heads [1.8], photo-detector amplifier [1.9], scanner [1.10], neutral networks [1.10]. Lately, some superior performances of poly-Si TFTs also have been reported by scaling down device dimension or utilizing novel crystallization technologies to enhance poly-Si film quality [1.11-1.12]. This provides the opportunity of using poly-Si TFTs into three-dimension (3-D) integrated circuit fabrication. Of course, the application in AMLCDs is the primary trend, leading to rapid developing of poly-Si TFT technology.

The major attraction of applying poly-Si TFTs in AMLCDs lies in the greatly improved carrier mobility in poly-Si film and the capability of integrating the pixel switching elements and the capability to integrate panel array and peripheral driving circuit on the same substrates [1.13-1.15]. In poly-Si film, carrier mobility larger than 15 cm$^2$/Vs can be easily achieved, that is enough to used as peripheral driving circuit including n- and p-channel devices. This enables the fabrication of peripheral circuit and TFT array on the same glass substrate, bring the era of system-on-glass (SOG) technology. The process complexity can be greatly simplified to lower the cost. In addition, the mobility of poly-Si TFTs is much better than that of amorphous ones, the dimension of the poly-Si TFTs can be made smaller compared to that of amorphous Si TFTs for high density, high resolution AMLCDs, and the aperture ratio in TFT array can be significantly improved by using poly-Si TFTs as pixel switching elements. This is because that the device channel width can be scaled down while meeting the same pixel driving requirements as in amorphous silicon thin film transistors (a-Si TFTs) AMLCDs.

For making high performance poly-Si TFTs, low-temperature technology is required for the realization of commercial flat-panel displays (FPD) on inexpensive glass substrate, since the maximum process temperature is limited to less than 600˚C [1.16]. There three major low-temperature a-Si crystallization methods to achieve high performance poly-Si thin film, solid phase crystallization (SPC), excimer laser crystallization (ELC), and metal-induced lateral crystallization (MILC). Typical fabrication of poly-Si TFTs include the deposition of amorphous silicon (a-Si) followed by long time furnace crystallization (> 20 h). Such a crystallization method is called solid phase crystallization (SPC). The *SPC* method has the advantage of good uniformity and smoother interface. However, the throughput is limited by the long crystallization time. In recent years, excimer laser crystallization (ELC) has been applied to crystallize the a-Si to poly-Si with lower temperature (substrate room temperature) compared to SPC. In addition, the ELC does not require a long time crystallization process, and a larger grain size compared to that with SPC method is possible with ELC method, which is ideally suited for applications of poly-Si TFTs. However, the roughness and uniformity of poly-Si films after ELC method is an important issue and it may degrade the electrical properties if ELC is not carefully controlled. In the last few years, several articles have been devoted to study of the growth mechanism of metal-induced-lateral-crystallization (MILC). Earlier observation of Ni induced crystallization of a-Si revealed that the onset temperature for crystallization of a-Si was significantly reduced in presence of $NiSi_2$ precipitates and crystallization occurred at around $500^0$C. The $NiSi_2$ precipitates acts as a good nucleus of Si, which has similar crystalline structure (the fluorite type, $CaF_2$) and a small lattice mismatch of 0.4% with Si. In the case of Ni induced crystallization, the growth of crystallites depends strongly on the migration of $NiSi_2$ precipitates, and the driving force for the migration of $NiSi_2$ precipitates is the reduction in free energy associated with the transformation of metastable a-Si to stable c-Si.

However, some problems still exist in applying poly-Si TFTs on large-area displays. In comparison with single-crystalline silicon, poly-Si is rich in grain boundary defects as well as intra-grain defects, and the electrical activity of the charge-trapping centers profoundly affects the electrical characteristics of poly-Si TFTs. Large amount of defects serving as trap states locate in the disordered grain boundary regions to degrade the ON current seriously [1.17]. Moreover, the relatively large leakage current is one of the most important issues of conventional poly-Si TFTs under OFF-state operation [1.18-1.19]. In most application, a low-cost substrate is essential and therefore a low temperature process (i.e., <650˚C) compatible with glass substrates is developed [1.20]. In summary, it is expected that the poly-Si TFTs will becomes more important in future technologies, especially when the 3-D circuit integration era is coming. More researches studying the related new technologies and the underlying mechanisms in poly-Si devices with shrinking dimensions are therefore worthy to be indulged in.

### 1.1.1 Defects in Poly-Si Film

Due to the granular structure of the poly-Si film, a lot of grain boundaries and intragranular defects exist in the film. The dangling bonds in grain boundaries will affect device characteristics seriously because they act as trapping centers to trap carriers. Carriers trapped by these low energy traps can no longer contribute to conduction, which results in the formation of local depletion region and potential barriers in these grain boundaries. Thus, the typical characteristics such as threshold voltage ($V_{TH}$), subthreshold swing (*S.S*), on current ($I_{ON}$), field effect mobility ($\mu_{FE}$) and transconductance (*Gm*) of TFTs are inferior to those of devices fabricated on single crystal silicon film. As for the leakage current, it is well known that the leakage current increase with the drain voltage and gate voltage. The dominant mechanism of the leakage current is field emission via grain boundary traps due to the high electric field near the drain junction [1.21-1.24].

To overcome this inherent disadvantage of poly-Si film, many researches have been focused on modifying or eliminating these grain boundary traps. Traps are associated with dangling bonds arising from lattice discontinuities between different oriented grains or at the Si/$SiO_2$ interface. The most useful method so far to remove traps is to passivate these dangling bonds, such as hydrogen plasma treatment has been utilized for the passivation [1.25-1.26], but it is difficult to control the hydrogen concentration in the TFT. The Si-H bonds may be broken under hot-carrier stress [1.27-1.28], leading to degradation of electrical characteristics after a long-term operation time. As the number of trapped carrier decreases, the potential barriers in grain boundaries decrease. And the leakage current decreases because of the fewer trap density near the drain region.

### 1.1.2 Motivation

To meet the requirement of higher circuit density and higher speed, it is necessary to improve the performance of the poly-Si TFTs. Although poly-Si TFTs have many superior advantages, the presence of a large number of grain boundaries in poly-Si TFTs contributes a large density of defects which cause the localized states in the energy gap and degrade performance. Hence, the reliability issue is one of the most constraints toward the applications. In the preview research, enlarging the grain size and passivating the defects at the grain boundary were widely used methods to reduce the trap states in the grain boundary. Generally, hydrogen plasma treatment has been utilized for the passivation, but it is difficult to control the hydrogen concentration in the TFTs. In recent years, fluorine ion implantation was applied to improve the electrical characteristics by eliminating the defects in the grain boundary [1.29-1.30]. It is found that the fluorine atoms piled up at the interface between the poly-Si and oxide to break the stress induced strained bonds to form stronger Si-F bonds, leading to local stress relaxation and thus decreasing the tail state density [1.31]. The fluorine atoms can also be the terminator of dangling bonding in poly-Si. Hence, the TFT with fluorine implantation has the superior electrical characteristics than conventional poly-Si TFTs. However, it needs additional oxide layer deposition and additional thermal annealing. The extra process steps will increase the difficulty for the fabrication of poly-Si TFTs. In this work, the electrical characteristics behaviors of poly-Si TFTs by various fluorine ion implantation dosages were investigated. In addition, there was no any pad oxide deposited firstly before thermal annealing. Hence, it also needed no additional thermal annealing step. Furthermore, it is known that one of the degradation is caused by the energetic electrons generated by impact ionization near the drain. By introducing the fluorinated silica glass (FSG) spacer technique, the stronger Si-F bonds passivate the interface of the drain which is the largest lateral electric field region location for light doped drain (LDD) structure. This method needs not additional process step and also can achieve the improvement of reliability. The electrical characteristics, including *I-V* measurement and DC bias stress reliability, were reported in this study. In addition, the material analysis such as secondary ion mass spectrometry (SIMS), and scanned electron microscope (SEM) were also discussed.

## 1.2 Overview of Nonvolatile Memory

In 1967, D. Kahng and S. M. Sze invented the floating-gate (FG) nonvolatile semiconductor memory (or flash memory) at Bell Labs [1.32]. To date, the flash memory device continues to be the most prevailing nonvolatile-memory implementation, and is widely used in both standalone and embedded memories. The invention of flash memory creates a huge industry of portable electronic devices such as cellular phones, digital cameras, digital voice recorders, MP3 walkman, personal data assistants to compact smart cards, USB flash personal disc etc.

Although a huge commercial success, conventional FG devices have their limitations. Two of the most prominent limitations are: (1) the limited potential for continued scaling of the device structure. This scaling limitation stems from the extreme requirements put on the tunnel oxide layer. The tunnel oxide must be thin enough to allow quick and efficient charge transport to and from FG. On the other hand, the tunnel oxide needs to provide superior isolation under retention, endurance, and disturbed conditions in order to maintain information integrity over periods of up to a decade. When the tunnel oxide is thinner for operation speed consideration, the retention characteristics may be degraded. And when the tunnel oxide is made thicker to take the isolation into account, the speed of the operation will be slower. Therefore, for mass production, there is a trade-off between speed and reliability for the optimal tunnel oxide thickness. (2) The quality and strength of tunnel oxide (or tunnel dielectric) after plenty of program/erase cycles. Once a leaky path has been created in tunnel oxide, all the charges stored in the floating gate will be lost. Therefore, two suggestions, poly-Si/oxide/nitride/oxide/Si (SONOS) [1.33-1.35] and nanocrystal nonvolatile memory devices [1.36-1.38], are proposed to overcome this oxide quality limit of the conventional FG structure. These technologies replace the floating gate structure with a great number of charge-storage nodes in the dielectric or in the nanocrystal. Unlike the floating gate, stored charges in isolated nodes cannot easily redistribute amongst themselves and the local leaky path will not cause the fatal loss of information for the nanocrystal nonvolatile memory device. This effectively prevents the leakage of all the stored charges out of the floating gate.

### 1.2.1 SONOS nonvolatile memory devices

poly-Si/oxide/nitride/oxide/silicon (SONOS) nonvolatile memory devices structure, the charge storage elements in SONOS memory are the charge traps distributed throughout the volume of the $Si_3N_4$ layer. A typical trap has a density of the order $10^{18}$-$10^{19}$ $cm^{-3}$ according to Yang et al [1.39] and stores both electrons and holes (positive charges) injected from the channel.

The nitride-based memory devices were extensively studied in the early 70s after the first metal-gate nitride device metal/nitride/oxide/silicon (MNOS) was reported in 1967 by Wegener et al [1.40]. Initial device structures in the early 1970s were p-channel metal-nitride-oxide-silicon (MNOS) structures with aluminum gate electrodes and thick (45nm) silicon nitride charge storage layers. Write/erase voltages were typically 25-30 V. In the late 1970s and early 1980s, scaling moved to n-channel silicon-nitride-oxide-silicon (SNOS) devices with write/erase voltages of 14-18 V. In the late 1980s and early 1990s, n- and p-channel SONOS devices emerged with write/erase voltages of 5-12 V. In the SONOS device, an oxide layer is introduced between the gate and the nitride region. Thus, it forms the $SiO_2/Si_3N_4/SiO_2$ (ONO) gate dielectric stack instead of capping the nitride layer with just a metal or semiconductor gate. The purpose of the top blocking oxide is to reduce the charge injection from the control gate into the nitride layer, limiting the memory window of both MNOS and SNOS devices.

During programming, the control gate is biased positively so that electrons from the channel can tunnel across the $SiO_2$ into the nitride layer. Some electrons will continue to move through the nitride layer then across the control oxide finally into the control gate. The remaining trapped charges in the nitride layer provide the electrostatic screening of the channel from the control gate. Therefore, there is a threshold voltage ($V_{TH}$) shift resulting from trapped charges in nitride and because of that SONOS can be used as a memory device just like conventional floating gate devices.

## 1.2.2 Nanocrystal nonvolatile memory devices

Nanocrystal nonvolatile memories are one particular implementation of storing charges by dielectric-surrounded nanodots, and were first introduced in the early 1990s by IBM researchers who proposed flash memory with a granular floating gate made from silicon nanocrystals [1.41], In a nanocrystal nonvolatile semiconductor memory (NVSM) device, charge is not stored on a continuous FG poly-Si layer, but instead on a layer of discrete, mutually isolated, crystalline nanocrystals or dots. Each dot will typically store only a handful of electrons; collectively the charges stored in these dots control the channel conductivity of the memory transistor.

As compared to conventional stacked gate NVSM devices, nanocrystal charge storage offers several advantages, the main one being the potential to use thinner tunnel oxide without sacrificing nonvolatility. This is a quite attractive proposition since reducing the tunnel oxide thickness is a key to lowering operating voltages and/or increasing operating speeds. This claim of improved scalability results not only from the distributed nature of the charge storage, which makes the storage more robust and fault-tolerant, but also from the beneficial effects of Coulomb blockade [1.42]. Quantum confinement effects (bandgap widening; energy quantization) can be exploited in sufficiently small nanocrystal geometries (sub-3 nm dot diameter) to further enhance the memory's performance.

Due to the less drain to FG coupling, nanocrystal memories suffer less from drain induced barrier lowering (DIBL). One way to exploit this advantage is to use a higher drain bias during the read operation, thus improving memory access time. Of particular importance is the low capacitive coupling between the external control gate and the nanocrystal charge storage layer. This does not only results in higher operating voltages, thus offsetting the benefits of the thinner tunnel oxide, but also removes an important design parameter (the coupling ratio) typically used to optimize the performance and reliability tradeoff.

Unlike volume distributed charge traps (ex: nitride in SONOS NVM), nanocrystals be deposited in a two-dimensional 2-D) layer at a fixed distance from the channel separated by a thin tunnel oxide. By limiting nanocrystals deposition to just one layer and adjusting the thickness of the top blocking dielectric, charge leakages to the control gate from the storage nodes can be effectively prevented.

### 1.2.3 Motivation

The Semiconductor Industry Association (SIA) International Technology Roadmap for Semiconductors (ITRS) indicates the difficult challenge, beyond the year 2005, for nonvolatile semiconductor memories is to achieve reliable, low-power, low-voltage performance [1.43]. For nonvolatile flash memories, two limitations encountered at the present time are: (1) the limited potential for continued scaling of the device structure. This scaling limitation stems from the extreme requirements put on the tunnel oxide layer. In order to get balance between program/erase speed and retention time, there is a trade-off between speed and reliability to get the optimal tunnel oxide thickness; (2) the quality and strength of tunnel oxide (or tunnel dielectric) after plenty of program/erase cycles. Once a leaky path has been created in tunnel oxide, all the charges stored in the floating gate will be lost. Therefore, two suggestions, the SONOS and the nanocrystal nonvolatile memory devices, are proposed to overcome this oxide quality limit of the conventional FG structure. These technologies replace the floating gate structure with a great number of charge-storage nodes in the dielectric or in the nanocrystal. Unlike the floating gate, the local leaky path will not cause the fatal loss of information for the nanocrystal nonvolatile memory device. This effectively prevents the leakage of all the stored charges out of the floating gate.

In this thesis, a combination of SONOS and nanocrystal nonvolatile memory devices is proposed. A SiGeN film is introduced to replace the nitride film in SONOS structure. After several different thermal processes, Ge in the SiGeN film will be segregated to form Ge nanodots embedded in the SiNx (or SiON) film. Because there are two charge-storage node sources, the nodes in Ge nanodots and in SiNx dielectric film, comparing to SONOS and Ge nanocystal NVMs, a larger memory window can be obtained. When a memory device has a larger memory window, it is easier to meet the requirement of retention of 10 years. And, hope to solve the two limitations mentioned above.

## 1.3 Thesis Organization

In this thesis, novel methods were proposed to improve the electrical characteristics of low temperature polycrystalline silicon thin film transistors (LTPS). In addition, the advanced nonvolatile memory devices were also fabricated and investigated for solving the problem of conventional nonvolatile memory. In chapter2, the transport properties and trap model of the poly-Si TFTs were introduced. Furthermore, the program/erase methods for memory device were also discussed. Also, the models of the reliability test were also investigated.

In chaprter3, fluorine ions implantation technology was applied for poly-Si TFTs fabrication. Before solid phase crystallization (*SPC*), fluorine ions were implanted to amorphous silicon (*a-Si*). The surface-oxidized a-Si is the driving force for fluorine ions segregating. The obvious fluorine concentration was observed at the surface of poly-Si and the interface between poly-Si and buffer oxide. The performance of fluorine-ions-implanted poly-Si TFTs was enhanced, due to the trap state density elimination.

In chapter4, the fluorine-ions-implanted poly-Si TFTs using excimer laser crystallization (*ELC*) method was also fabricated and investigated. The improvement of electrical characteristics of fluorine-ions-implanted poly-Si TFTs resulted from the pssivation of poly-Si. In addition, the segregated fluorine ions at the interface of poly-Si and buffer oxide reduces the mechanical stress resulted from the rapid crystallization.

In chaper5, the electrical characteristics and the electrical reliability of fluorine-ions-implanted poly-Si TFTs were investigated. The stronger Si-F bonds, replacing the Si-Si and Si-H bonds in the poly-Si, can resist the current impact. Hence, the reliability of fluorine-ions-implanted poly-Si TFTs is improved. The obvious enhancement of the reliability was found for using *ELC* method; due to the lower trap state density was obtained. Furthermore, the strong Si-F bonds is suitable to resist the higher current impact due to the poly-Si TFTs using *ELC* method.

In chapter6, fluorinated silica glass (FSG) was used for the application of spacer on poly-Si TFTs. The presence of FSG spacers can effectively reduce the lateral electrical field near the drain side of poly-Si TFT device, and strongly passivate Si dangling bonds at the grain boundaries. The significant enhancement in electrical performance suppresses serious kink effect, and improves electrical reliability of poly-Si TFTs effectively.

In chapter7, a large memory window is observed due to isolated Ge nanocrystals in the silicon-oxygen-nitride (SiON) gate stack layer. The Ge nanocrystals were nucleated after high temperature oxidized silicon-germanium-nitride (SiGeN) layer. Also, the manufacture technology using the sequent high-temperature oxidation of the amorphous silicon (a-Si) layer and directly oxidation of the SiGeN layer acting as the blocking oxide is proposed to enhance the performance of nonvolatile memory devices, respectively.

In chapter8, the formation of Ge nanocrystals embedded in SiON is proposed for charge storage elements in this work. Compared to the control samples of Ge nanocrystals /$SiO_2$ /Si structure and SiON/Si stack memory, the proposed Ge nanocrystals/SiON/Si memory obtained superior memory window, even larger than the summation of the typical both. It is considered that the extra interface trap states between Ge and SiON film was generated as Ge nanocrystals were embedded in SiON layer.

In chapter9, the Ge nanocrystal formation by oxidizing SiGeN with distributed charge storage elements is proposed in this work. The manufacture technology using the sequent high-temperature oxidation of a-Si layer acting as the blocking oxide. The longer duration of dry oxidation causes obvious Ge nanocrystals formation. Also, simple steam treatment improves the quality of blocking oxide and reduces the thermal budget of fabrication. Furthermore, overall oxidation by steam treatment causes initial Ge nanocrystal to become germanium oxide which is also a charge trapping center.

In chapter10, the Ge nanocrystal formation by oxidizing SiGeN with distributed charge storage elements is proposed in this work. The manufacture technology using the sequent high-temperature oxidation of SiGeN layer acting as the blocking oxide. Simple steam treatment improves the quality of blocking oxide. However, the Ge nanocrystals were formed far from the tunneling oxide which is obviously different from the long dry oxidation condition for quickly oxidation. In addition, the Ge nanocrystals were also oxidized after steam treatment.

Finally, conclusions and future work as well as recommendation for further research are given in chapter11 and chapter12, respectively.

# Chapter 2

# Poly-Si TFTs Conduction Mechanism and Nonvolatile Memory Basics Principles

## 2.1 Poly-Si TFTs Transportation Mechanisms

The device characteristics of poly-Si TFTs are strongly influenced by the grain structure in poly-Si film. Even though the inversion channel region is also induced by the gate voltage as in MOSFETs, the existence of grain structure in channel layer bring large differences in carrier transport phenomenon. A schematic MOSFET cross section, showing the axes of coordinates and the bias voltages at the four terminals, for the drain-current model is as shown in Figure 2-1. Many researches studying the electrical properties and the carrier transport in poly-Si TFTs have been reported. A simple grain boundary-trapping model has been described by many authors in details [2.1-2.3]. In this model, it is assumed that the poly-Si material is composed of a linear chain of identical crystallite having a grain size $L_g$ and the grain boundary trap density $N_t$ (cm$^{-3}$). The charge trapped at grain boundaries is compensated by oppositely charged depletion regions surrounding the grain boundaries. From Poisson's equation, the charge in the depletion regions causes curvature in the energy bands, leading to potential barriers that impede the movement of any remaining free carriers from one grain to another. When the dopant/carrier density $n$ (or $N_D$) (cm$^{-3}$) is small, the poly-Si grains will be fully depleted. The width of the grain boundary depletion region $x_d$ extends to be $L_g/2$ on each side of the boundary, and the voltage barrier height $V_B$ can be expressed as

**Fully depleted:**

$$V_B = \frac{qn}{2\varepsilon_S} x_d{}^2 = \frac{qnL_g{}^2}{8\varepsilon_S} \tag{2-1}$$

As the dopant/carrier concentration is increased, more carriers are trapped at the grain boundary. The curvature of the energy band and the height of potential barrier increase, making carrier transport form one grain to another more difficult. When the dopant/carrier density increases to exceed a critical value $N^* = N_t / L_g$, the poly-Si grains turn to be partially depleted and excess free carriers start to spear inside the grain region. The depletion width and the barrier height can be expressed as

**Partially depleted:**

$$x_d = \frac{N_t}{2n} \tag{2-2}$$

$$V_B = \frac{qn}{2\varepsilon_s}\left(\frac{N_t}{2n}\right)^2 = \frac{qN_t{}^2}{8\varepsilon_s n} \tag{2-3}$$

The depletion width and the barrier hight turn to decrease with increasing dopant/carrier density, leading to improved conductivity in carrier transport.

The carrier transport in fully depleted poly-Si film can be described by the thermionic emission over the barrier. Its' current density can be written as [2.4]

$$J = qnv_c \exp[-\frac{q}{kT}(V_B - V_a)] \tag{2-4}$$

where $n$ is the free-carrier density, $v_c$ is the collection velocity ($v_c = \sqrt{kT / 2\pi m^*}$), $V_B$ is the barrier height without applied bias, and $V_a$ is the applied average bias across the one grain boundary region. For small-applied biases, the applied voltage divided approximately uniformly between the two sides of a grain boundary. Therefore, the barrier in the forward-bias direction decreases by an amount of $V_a/2$. In the reserve-bias direction, the barrier increases by the same amount. The current density in these two directions then can be expressed as

$$J_F = qnv_c \cdot \exp[-\frac{q}{kT}(V_B - \frac{1}{2}V_a)] \tag{2-5}$$

$$J_R = qnv_c \cdot \exp[-\frac{q}{kT}(V_B + \frac{1}{2}V_a)] \tag{2-6}$$

Thus the net current density is then given by

$$J = 2qnv_c \exp(-\frac{qV_B}{kT})\sinh(\frac{qV_a}{2kT}) \tag{2-7}$$

At low applied voltages, the voltage drop across a grain boundary is small compared to the thermal voltage $kT/q$, thus Eq. (2-7) can be simplified as

$$J = 2qnv_c \exp(-\frac{qV_B}{kT})\frac{qV_a}{2kT} = \frac{q^2 nv_c V_a}{kT}[\exp(-\frac{qV_B}{kT})] \tag{2-8}$$

the average conductivity $\sigma = J / \xi = JL_g / V_a$ , and the effective mobility $\sigma = qn\mu_{eff}$ then the average conductivity can be obtained as

$$\sigma = \frac{q^2 nv_c L_g}{kT}\exp(-\frac{qV_B}{kT}) \tag{2-9}$$

$$\mu_{eff} = \frac{qv_c L_g}{kT}\exp(-\frac{qV_B}{kT}) \equiv \mu_0 \exp(-\frac{qV_B}{kT}) \tag{2-10}$$

where $\mu_0$ represents the carrier mobility inside grain regions. It is found that the conduction in poly-Si is an activated process with activation energy of approximately $qV_B$, which depends on the dopant/carrier concentration and the grain boundary trap density.

Applying gradual channel approximation to poly-Si TFTs, which assumes that the variation of the electric field in the y-direction (along the channel) is much less than the corresponding variation in the y-direction (perpendicular to the channel), as shown Figure 2-2. The carrier density $n$ per unit area ($cm^{-2}$) induced by the gate voltage can be expressed as

$$n = \frac{C_{ox}(V_G - V_{TH})}{qt_{ch}} \tag{2-11}$$

where

$t_{ch}$ is the thickness of the inversion layer,

$V_{TH}$ is the threshold voltage,

$C_{ox}$ is gate oxide capacitance per unit area.

$$I_D = J \cdot W \cdot t_{ch} \tag{2-12}$$

$$J = n \cdot q \cdot \mu_{eff} \cdot \xi \tag{2-13}$$

$$\xi = \frac{V_a}{L_g} = \frac{V_D}{N_g L_g} = \frac{V_D}{\frac{L}{L_g} L_g} = \frac{V_D}{L}; \quad N_g \text{ is the grain number} \tag{2-14}$$

Therefore, by replacing Eq. (2-11), (2-13) and (2-14) into Eq. (2-12), the drain current of poly-Si TFT then can be given by

$$I_D = C_{ox} \frac{W}{L} \left(V_G - V_{TH}\right) \cdot V_D \cdot \mu_o \exp(-\frac{qV_B}{kT}) \tag{2-15}$$

Obviously, this *I-V* characteristic is very similar to that linear region of MOSFETs, except that the mobility is modified.

### 2.1.1 Methods of Device Parameter Extraction

In this section, we will introduce the methods of typical parameters extraction such as threshold voltage ($V_{th}$), subthreshold slope (*S.S*), drain current $I_{ON}/I_{OFF}$ ratio**,** field-effect mobility ($\mu_{FE}$), and the trap density ($N_t$).

**Determination of the threshold voltage**

Many ways are used to determinate the $V_{th}$ which is the most important parameter of semiconductor devices. In poly-Si TFTs, the method to determinate the threshold voltage is constant drain current method. The gate voltage at a specific drain current $I_N$ value is taken as the threshold voltage. This technique is adopted in most studies of TFTs. Typically, the threshold current $I_N = I_D / (W / L)$ is specified 10 nA for $V_D = 0.1$V (saturation region) in this thesis.

**Determination of the subthreshold slope**

Subthreshold slope $SS_{\text{(V/dec.)}} = dV_G/d(\log I_D)$ is a typical parameter to describe the gate control toward channel. And in intrinsic polysilicon TFTs the parameter $SS$ is directly related with the total trap states density $N_T$ by the relationship

$$SS = \left(\frac{kT}{q}\right) \ln\, 10 \left(1 + \frac{q^2 t_{si} N_T}{C_{OX}}\right) \tag{2-16}$$

where

$kT$ is the thermal energy,

$t_{si}$ is the polysilicon layer thickness.

Thus, the decrease of $SS$ with stressing suggests a decrease in the total trap states density, which includes both bulk and interface traps. The $S.S$ should be independent of drain voltage and gate voltage. However, in reality, $S.S$ might increase with drain voltage due to short-channel effects such as charge sharing, avalanche multiplication, and punchthrough-like effect. The $S.S$ is also related to gate voltage due to undesirable factors such as serial resistance and interface state. In this experiment, the $S.S$ is defined as one-half of the gate voltage required to decrease the threshold current by two orders of magnitude (from $10^{-8}$A to $10^{-10}$A).

### Determination of $I_{ON}/I_{OFF}$ Current Ratio

Drain $I_{ON}/I_{OFF}$ current ratio is another important factor of TFTs. High $I_{ON}/I_{OFF}$ ratio represents not only large turn-on current but also small off current (leakage current). It affects gray levels (the bright to dark state number) of TFT AMLCD directly.

There are many methods to specify the on and off current. The practical one is to define the maximum current as on current and the minimum leakage current as off current while drain voltage is applied at 5V.

### Determination of the field-effect mobility

The field-effect mobility ($\mu_{FE}$) is determined from the transconductance ($g_m$) at low drain voltage ($V_d = 0.1$V, $V_G$-$V_{th} >> V_d$). The transfer I-V characteristics of poly-Si

TFT can be expressed as

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}[(V_G - V_{TH})V_D] \tag{2-17}$$

where

$W$ is channel width,

$L$ is channel length,

The transconductance is defined as

$$g_m = \frac{\partial I_D}{\partial V_G}\bigg|_{V_D = const.} = \frac{W C_{ox} \mu_{FE}}{L} V_D \tag{2-18}$$

Therefore, the field-effect mobility can be obtained by

$$\mu_{FE} = \frac{L}{C_{ox} W V_D} g_m \tag{2-19}$$

**Modification of effective field-effect mobility**

According Seto model, in uniform small grain poly-Si TFT, the effective field-effect mobility can be expressed [2.5]:

$$\mu_{eff} = \frac{q v_c L_g}{kT} \exp(-\frac{q V_B}{kT}) \equiv \mu_0 \exp(-\frac{q V_B}{kT})$$

However, in poly-Si films with enlarged grains, the uniform trap distribution model fails to give reliable results due to high nonuniformity of the polycrystalline material. According to Farmakis *et al*. model, the $\mu_{eff}$ depend on the number of grain boundaries present within the channel of the transistor [2.6]. Figure 2-3 represents the energy band structure of the polysilicon in the neighborhood of the grain boundaries of a n-channel polysilicon TFT along the channel in the linear region of operation (low drain voltage $V_D$). This energy band structure has two resistances $R_G$ and $R_{GB}$ equivalent to the grain region and the grain boundary respectively, both modulated by the gate voltage $V_G$. The grain region is considered to behave as in a bulk MOSFET. Therefore, considering an average number of $n$ *GB's* and $n$ entire grains within the channel, according to the standard MOSFET theory, the total channel resistance $R_{ch}$

will be

$$R_{ch} = \frac{L}{W\mu_{eff}Q_{invG}} = nR_{G} + NR_{GB} = \frac{nL_{G}}{W\mu_{G}Q_{invG}} + \frac{nL_{GB}}{W\mu_{GB}Q_{invGB}} \tag{2-20}$$

where

$\mu_{eff}$ effective electron mobility；

$\mu$ mobility；

$Q_{inv}$ charge in the inversion layer；

$L_G$ average intra-grain length;

$L_{GB}$ average grain boundary length

Throughout the text, the indices *G* and *GB* will be referred to the intra-grain and grain boundary region respectively. Assuming that the main conduction mechanism through the grain boundaries is the thermionic emission over the grain-boundary energy potential barrier $V_b$, the charge in the grain boundaries $Q_{GB}$ will be given by the relationship [2.6]：

$$Q_{invGB} = e^{-qV_b(V_G)/kT} Q_{invG} \tag{2-21}$$

When the potential barrier $V_b$ is high, $Q_{invGB} \ll Q_{invG}$ and according to Eq.(2-17) $\mu_{eff}$ is practically controlled by the grain boundary mobility being normally very low. When $V_b$ is lowered enough by increasing the gate potential $V_G$, $Q_{invGB}$=$Q_{invG}$ and $\mu_{eff} \approx \mu_{eff}$ .By taking into account that $L= nL_G + nL_{GB}$, from Eq. (2-17) and (2-18), it is obtained

$$\frac{L}{\mu_{eff}} = \frac{L\text{-}nL_{GB}}{\mu_{G}} + n\frac{L_{GB}}{\mu_{GB}e^{-qV_b/kT}} \tag{2-22}$$

The average grain-boundary number inside the channel is

$$n = \frac{L}{L_G} \tag{2-23}$$

$$\frac{L}{nL_{GB}} = \frac{L_G}{L_{GB}} \tag{2-24}$$

For polysilicon TFTs with gate length and width of the same order of the grain size , *n* takes small values. In this case, for typical values of $L_{GB}$ = 1-2 nm and L = 4-20 um, it is：

$$\frac{\mathrm{L}}{\mathrm{nLGB}} \rangle\rangle 1 \qquad (2\text{-}25)$$

Equation (2-19) is further simplified when Eq. (2-22) is taken into account：

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_G} + \frac{nL_{GB}}{L}\frac{1}{\mu_{GB}e^{-qV_b/kT}} \qquad (2\text{-}26)$$

So according to the polysilicon TFTs mobility model with separating grain and grain boundaries taking into account the average number of grain boundaries into the channel, in general the effective field-effect mobility ($\mu_{FE}$) is given by,

$$\mu_{FE} = \mu_G \frac{1}{1+(\mu_G/\mu_{GB})[(nL_{GB})/L]\exp(qV_b/kT)} \qquad (2\text{-}27)$$

where $n = L/L_G$ is the average grain-boundary number.

**Determination of the trap density**

In partially depleted condition, as described in Eq. (2-3), the grain boundary potential barrier height $V_B$ is related to the carrier concentrations inside the grain and the trapping states located at grain boundaries. Based on this consideration, the amount of trap state density $N_t$ can be extracted from the current-voltage characteristics of poly-Si TFTs. As proposed by Levinson *et al.* [2.7], the *I-V* characteristics including the trap density can be obtained by replacing Eq. (2-3) and (2-11) into Eq. (2-15):

$$I_D = \mu_0 C_{ox}\frac{W}{L}(V_G - V_{TH})V_D \exp\left(-\frac{q^3 N_t^{\,2} t_{ch}}{8kT\varepsilon_s C_{ox}(V_G - V_{TH})}\right) \qquad (2\text{-}28)$$

This equation had been further corrected by Proano *et al.* by considering the mobility under low gate bias [2.8]. It is found that the behavior of carrier mobility under low gate bias can be expressed more correctly by using the flat-band voltage $V_{FB}$ instead of the threshold voltage $V_{TH}$. Moreover, a better approximation for channel thickness $t_{ch}$ in an undoped material is given by defining the channel thickness as the thickness at which 80 percent of the total charge resides. Therefore, by solving the Poisson’s equation, the channel thickness is given by

$$t_{ch} = \frac{8kT\sqrt{\varepsilon_s \varepsilon_{ox}}}{qC_{ox}(V_G - V_{FB})} \qquad (2\text{-}29)$$

The drain current of poly-Si TFTs then should be expressed as

$$I_D = \mu_0 C_{ox} \frac{W}{L}(V_G - V_{FB})V_D \exp(-\frac{q^2 N_t^{\ 2} \sqrt{\varepsilon_{ox}/\varepsilon_s}}{C_{ox}^{\ 2}(V_G - V_{FB})^2}) \tag{2-30}$$

The effective trap state density then can be obtained from the slope of the curve $ln[I_D/(V_G\text{-}V_{FB})]$ versus $(V_G\text{-}V_{FB})^{-2}$.

### 2.1.2 Poly-Si TFTs Non-Ideal Effect

There are two major non-ideal effects will limit the TFTs application, including leakage current, and kink-effect. The mechanism of these three non-ideal effects is described briefly as bellow.

**Leakage current**

In AMLCD, TFTs play a switching device to turn $I_{ON}/I_{OFF}$ the current path for charging/discharging the liquid crystal capacitor. Thus, the leakage current should be low enough to remain a pixel gray level before it must be refreshed. The leakage current mechanism in poly-Si has been studied by Olasupe [2.9]. The leakage current resulted from carrier generation from the poly-Si grain boundary defects. There are three major leakage mechanisms, as shown in Figure 2-4. The dominant mechanism is a function of the prevailing drain bias. They pointed out carrier generation from grain boundary defects via thermionic emission and thermionic field emission to be prevalent at a low and medium drain biases, and carrier pure tunneling from poly-Si grain boundary defects to be the dominant mechanism at higher drain bias. In 1997, Angelis give a concise analytical equation for describing the leakage current [2.10].

$$I_L = I_{L0} e^{\beta\sqrt{E_m}} = qA_j W_D \sigma v_{th} N_t n_i e^{\beta_{PF}\sqrt{E_m}} e^{\beta_{TFE}\sqrt{E_m}} \tag{2-31}$$

$$E_m = \frac{|V_G - V_D - V_{fb}|}{t_{ox}(\varepsilon_{Si}/\varepsilon_{ox})} \tag{2-32}$$

Where $E_m$ is the peak electrical field, $A_j$ is the junction area, $W_D$ is the reversed-biased drain junction depletion width, $v_{th}$ is the carrier thermal velocity, and $\beta_{PF}$ and $\beta_{TFE}$ are the field-enhancement factors arising from Poole-Frenkel effect and thermal field emission. Thus, the most effective way to reduce the leakage current is decreasing the $E_m$.

**Kink effect** [2.11]

During devices operation, a high field near the drain could induce impact ionization there. Majority carriers, holes in the p-substrate for an n-channel poly-Si TFTs, generated by impact ionization will be stored in the substrate, since there is no substrate contact to drain away these charges. Therefore the substrate potential will be changed and will result in a reduction of the threshold voltage. This, in turn, may cause an increase or a kink in the current-voltage characteristics. The kink phenomenon is shown in Figure 2-5. This float-body or kink effect is especially dramatic for n-channel devices, because of the higher impact-ionization rate of electrons. The kink effect can be reduced in TFTs by lowering lateral field inside the channel.

## 2.2 Nonvolatile Memory Basics Principles

### 2.2.1 Programming/Erasing Mechanism

Most of operations on novel nonvolatile memories, such as nanocrystal and SONOS memories are base on the concept of Flash memory. If a datum has to be stored in a bit of the memory, there are different procedures. The threshold voltage shift of a Flash transistor can be written as [2.12, 2.13]:

$$\Delta V_T = -\frac{\overline{Q}}{C_{FC}} \tag{2-33}$$

where $\overline{Q}$ is the charge weighted with respect to its position in the gate oxide, and the capacitances between the floating gate (FG) and control gate. The threshold voltage of the memory cell can be altered by changing the amount of charge present between the gate and the channel, corresponding to the two states of the memory cell, i.e., the binary values ("1" and "0") of the stored bit. Figure 2-6 shows the threshold voltage shift between two states in a Flash memory. To a nonvolatile memory, it can be "written" into either state "1" or "0" by either "programming" or "erasing" methods, which are decided by the definition of memory cell itself. There are many solutions to achieve "programming" or "erasing". In general, hot carrier electron injection, tunneling and band to band tunneling, are three kinds of common operation mechanism employed in novel nonvolatile memories. The three mechanisms will lead difference characteristics for nonvolatile memories.

**Channel Hot-Electron Injection (*CHEI*)**

The physical mechanism of *CHEI* is relatively simple to understand qualitatively. An electron traveling from the source to the drain gains energy from the lateral electric field and loses energy to the lattice vibrations (acoustic and optical phonons). At low fields, this is a dynamic equilibrium condition, which holds until the field strength reaches approximately 100kV/cm [2.14]. For fields exceeding this value, electrons are no longer in equilibrium with the lattice, and their energy relative to the conduction band edge begins to increase. Electrons are "heated" by the high lateral electric field, and a small fraction of them have enough energy to surmount the barrier between oxide and silicon conduction band edges. Figure 2-7 shows schematic representation of *CHEI* MOSFET and the energy-distribution function with different fields. In the other hand, the effective mass of hole is heavier than one of electron. It is too hard to obtain enough energy to surmount oxide barrier. Therefore, hot-hole injection rarely is employed in nonvolatile memory operation. For an electron to overcome this potential barrier, three conditions must hold [2.15].

1) Its kinetic energy has to be higher than the potential barrier.

2) It must be directed toward the barrier.

3) The field in the oxide should be collecting it.

Nevertheless, a description of the injection conditions can be accomplished with two different approaches. The *CHEI* current is often explained and simulated following the “lucky electron” model [2.16]. This model is based on the probability of an electron’s being lucky enough to travel ballistically in the field ε for a distance several times the mean free path without scattering, eventually acquiring enough energy to cross the potential barrier if a collision pushes it toward the Si/SiO$_2$ interface. Consequently, the probability of injection is the lumped probability of the following events, which are depicted in Figure 2-8 [2.17].

1) The carrier has to be “lucky” enough to acquire enough energy from the lateral electric field to overcome the oxide barrier and to retain its energy after the collision that redirects the electron toward the interface ($P_{\Phi b}$).
2) The carrier follows a collision-free path from the redirection point to the interface ($P_{ED}$).
3) The carrier can surmount the repulsive oxide field at the injection point, due to the Schottky barrier lowering effect, without suffering an energy-robbing collision in the oxide ($P_{OC}$).

The current density of *CHEI* is expressed as

$$I_{inj} = A_d I_{ds} \left(\frac{\lambda E_m}{\varphi_b}\right)^2 e^{\left(-\varphi_b / E_m \lambda\right)} \tag{2-34}$$

Here $I_{ds}$ is the channel current and $A_d$ is a constant

**Tunneling Injection**

Tunneling mechanisms are demonstrated in quantum mechanics. Basically, tunneling injection must to have available states on the other side of the barrier for the carriers to tunnel into. If we assume elastic tunneling, this is a reasonable assumption due to the thin oxide thickness involved. Namely, no energy loss during tunneling processes. The tunneling probability, depending on electron barrier height ( $\varphi(x)$ ), tunnel dielectric thickness ( $d$ ), and effective mass ( $m_e$ ), is express as

$$T = \exp(-2\int_0^d \frac{\sqrt{\varphi(x)^* m_e}}{\hbar} dx) \tag{2-35}$$

Tunneling through the oxide can be attributed to different carrier-injection mechanisms. Which process applies depends on the oxide thickness and the applied gate field or voltage. Direct tunneling (*DT*), Fowler-Nordheim tunneling (*FN*), modified Fowler-Nordheim tunneling (*MFN*) and trap assistant tunneling (*TAT*) are the main programming mechanisms employed in memory as shown in Figure 2-9 [2.18-2.21].

**(a) Direct Tunneling**

For nanocrystal memories, the control-gate coupling ratio of nanocrystal memory devices is inherently small [2.22]. As a result, *FN* tunneling cannot serve as an efficient write/erase mechanism when a relatively thick tunnel oxide is used, because the strong electric field cannot be confined in one oxide layer. The direct tunneling is employed in nanocrystal memories instead. In the other hand, the direct tunneling is more sensitive to the barrier width than barrier height, two to four orders of magnitude reduction in leakage current can still be achieved if large work function metals, such as Au or Pt [2.23].

**(b) Fowler–Nordheim Tunneling**

The Fowler–Nordheim (*FN*) tunneling mechanism occurs when applying a strong electric field (in the range of 8–10MV/cm) across a thin oxide. In these conditions, the energy band diagram of the oxide region is very steep. Therefore, there is a high probability of electrons' passing through the energy barrier itself. Using a free-electron gas model for the metal and the *WKB* approximation for the tunneling probability [2.24], one obtains the following expression for current density [2.25]:

$$J = \frac{q^3 F^2}{16\pi^2 h^2 \Phi_B} \exp\left[ \frac{-4(2m_{OX}^*)^{1/2} \Phi_B^{3/2}}{3\hbar q F} \right] \tag{2-36}$$

Where $\Phi_B$ is the barrier height, $m_{OX}^*$ is the effective mass of the electron in the forbidden gap of the dielectric, *h* is the Planck's constant, *q* is the electronic charge, and *F* is the electric field through the oxide. However, the exponential dependence of tunnel current on the oxide-electric field causes some critical problems of process control because, for example, a very small variation of oxide thickness among the cells in a memory array produces a great difference in programming or erasing currents, thus spreading the threshold voltage distribution in both logical states.

**(c) Modified Fowler–Nordheim Tunneling**

Modified Fowler–Nordheim tunneling (*MFN*) is similar to the tradition *FN* tunneling mechanism, yet the carriers enter the nitride at a distance further from the tunnel oxide-nitride interface. *MFN* mechanism is frequently observed in SONOS memories. The SONOS memory is designed for low-voltage operation (<10V, depending on the Equivalent oxide thickness), a relatively weak electrical field couldn't inject charges by *DT* or *FN* mechanism.

**(d) Trap Assistant Tunneling**

The charge storage mediums with many traps may cause another tunneling mechanism. For example, the charges tunnel through a thin oxide and arrive to the traps of nitride layer at very low electrical field in SONOS systems. During trap assisted injection the traps are emptied with a smaller time constant then they are filled. The charge carriers are thus injected at the same distance into the nitride as for *MFN* injection. Because of the sufficient injection current, trap assistant tunneling may influence in retention [2.26].

### Band to Band Tunneling (*BTBT*)

Band to band tunneling application to nonvolatile memory was first proposed in 1989. I. C. Chen and et al. demonstrated a high injection efficiency (~1%) method to programming EPROM devices [2.27]. Band-to-band Tunneling (*BTBT*) process occurs in the deeply depleted doped surface region under the gate to drain / gate to source overlap region. In this condition, the band-to-band tunneling current density is expressed as

$$J_{b-b} = \frac{\sqrt{2m^*}\, q^3 \varepsilon V_{app}}{4\pi^3 \hbar^2 E_g^{\frac{1}{2}}} \exp[-\frac{4\sqrt{2m^*}\, E_g^{\frac{3}{2}}}{3q\varepsilon\hbar} \tag{2-37}$$

#### (a) Band to Band Hot Electron Tunneling Injection

When band-bending is higher than the energy gap of the semiconductor, the tunneling electron from the valence band to the conduction band becomes significant. The mechanism is at the condition for positive gate voltage and negative drain voltage. Hence, the hot holes are injected through the tunnel oxide and then recombine the stored electrons as shown in Figure 2-10.

#### (b) Band to Band Hot Hole Tunneling Injection

The injection is applied for p-type nonvolatile memory device. The mechanism is at the condition for negative gate voltage and positive drain voltage. Hence, the hot holes are injected through the tunnel oxide and then recombine the stored electrons as shown in Figure 2-11.

The electrons (n-type) / holes (p-type) are accelerated by a lateral electric field toward the channel region and some of the electrons with sufficient energy can surmount the potential barrier of $SiO_2$ [2.27-2.29]. Due to the small oxide field, the electron/hole influence through the oxide can easily reach hundreds of coulombs per square centimeter without failure, it means to the improvement reliability of memory cells.

**Hot hole Injection**

The hot hole injection can be used to erase the programmed nonvolatile memory device. The avalanche breakdown can be occurred at the condition for gate is grounded/negatively biased and grain is positively biased. Avalanche breakdown involves hot holes injection and requires relative high voltages on the drain side. The channel electrons accelerated by the lateral electrical field generate additional carriers (electron-hole pairs) by impact ionization. The gate current resulted from hot hole as gate bias is much lower than drain bias. The hot holes overcome the barrier of the tunnel oxide and inject into the charge trapping layer. The injected hot holes recombine with the stored electrons at the erase operation as shown in Figure 2-12.

**Channel Initiated Secondary Electron Injection (*CHISEI*)**

The main difference between *CHE* and *CHISEL* is that *CHISEL* is highly sensitive to the lateral electrical field and vertical electrical filed. The operation condition is at *CHI* condition plus negative body voltage ($V_B$). The procedure and the band diagram for the application of *CHISEL* are as shown in Figure 2-13 and Figure 2-14, respectively. The superior injection of *CHISEL* operation mode leads to more program efficiency. The improved program efficiency results from the substrate enhanced gate current component. Under optimized substrate condition, the substrate hot carriers and subsequent injection are expected for the application of low power and high speed.

## 2.2.2 Nonvolatile Memory Reliability

For a nonvolatile memory, the important to concern is distinguishing the state in cell. However, in many times operation and charges storage for a long term, the state is not obvious with charges loss. Endurance and retention experiments are performed to investigate Flash-cell reliability.

**Retention**

In any nonvolatile memory technology, it is essential to retain data for over ten years. This means the loss of charge stored in the storage medium must be as minimal as possible. For example, in modern Flash cells, FG capacitance is approximately 1 fF. A loss of only 1 fC can cause a 1V threshold voltage shift. If we consider the constraints on data retention in ten years, this means that a loss of less than five electrons per day can be tolerated [2.12].

Possible causes of charge loss are: 1) by tunneling or thermionic emission mechanisms; 2) defects in the tunnel oxide; and 3) detrapping of charge from insulating layers surrounding the storage medium.

First, several discharge mechanisms may be responsible for time and temperature dependent retention behavior of nonvolatile memory devices. Figure 2-15 shows a bandgap diagram of a SONOS device in the excess electron state, illustrating trap-to-band tunneling, trap-to-trap tunneling, and band-to-trap tunneling, thermal excitation and Poole-Frenkel emission retention loss mechanisms [2.21]. These mechanisms may be classified into two categories. The first category contains tunneling processes that are not temperature sensitive (trap-to-band tunneling, trap-to-trap tunneling and band-to-trap tunneling). The second category contains those mechanisms that are temperature dependent. Trapped electrons may redistribute vertically inside the nitride by Poole–Frenkel emission, which will give rise to a shift in the threshold voltage. Moreover, at elevated temperatures, trapped electrons can also be thermally excited out of the nitride traps and into the conduction band of the nitride (thermal excitation), and drift toward the tunnel oxide, followed by a subsequent tunneling to the silicon substrate.

Secondly, the generation of defects in the tunnel oxide can be divided into an extrinsic and an intrinsic one. The former is due to defects in the device structure; the latter to the physical mechanisms that are used to program and erase the cell.

Electrons can be trapped in the insulating layers surrounding the storage medium during wafer processing, as a result of the so-called plasma damage, or even during the UV exposure normally used to bring the cell in a well-defined state at the end of the process. The electrons can subsequently de-trap with time, especially at high temperature. The charge variation results in a variation of the storage medium potential and thus in cell decrease [2.30].

The retention capability of Flash memories has to be checked by using accelerated tests that usually adopt screening electric fields and hostile environments at high temperature.

**Endurance**

Endurance is the number of erase/write operations that the memory will complete and continue to operate as specified in the data sheet. Generally speaking, Flash products are specified for $10^6$ erase/program cycles. Nevertheless, the endurance requirement may be relaxed with the increase of memory density for the other using. In the higher density, a certain cell in a block has less possibility to be written and erased since the memory operation on the cell is repeated after using up the whole memory blocks. The endurance requirement is sufficient for the user to take 700 photos with a 1MB size every day for 10 years [2.31]. As the experiment was performed applying constant pulses, the variations of program and erase threshold voltage levels are described as “program/erase threshold voltage window closure” and give a measure of the tunnel oxide aging [2.30, 2.32].

In particular, the reduction of the programmed threshold with cycling is due to trap generation in the oxide and interface state generation at the drain side of the channel. The evolution of the erase threshold voltage reflects the dynamics of net fixed charge in the tunnel oxide as a function of the injected charge as shown in

Figure 2-16. The initial lowering of the erase is due to a pile-up of positive charge which enhances tunneling efficiency, while the long-term increase of the erase is due to a generation of negative traps.

Moreover, a high field stress on thin oxide is known to increase the current density at low electric field. The excess current component, which causes a significant deviation from the current–voltage curves from the theoretical F-N characteristics at low field, is known as stress-induced leakage current (*SILC*). *SILC* is clearly attributed by stress-induced oxide defects, which leads to a trap assisted tunneling as shown in Figure 2-17. The main parameters controlling *SILC* are the stress field, the amount of charge injected during the stress, and the oxide thickness. For fixed stress conditions, the leakage current increases strongly with decreasing oxide thickness [2.33-2.35].

## 2.2.3 Nanocrystal Memory

The nanocrystals are separated from each other within the gate oxide dielectric. Therefore, the tunnel oxide thickness in the nanocrystal memory device can be reduced. The faster programming and lower voltage operation can be allowed.

**(a) Quantum Confinement Effect**

The quantum dot, is quasi-zero-dimensional nanoscaled material, and is composed by small amount atoms. The quantum confinement energy dependence on nanocrystal size has been researched both experimentally and theoretically according to the tight-binding model [2.36]. The quantum confinement effect becomes significant when the nanocrystal size shrinks to the nanometer range, which causes the conduction band in the nanocrystal to shift to higher energy compared with bulk material [2.37]. The discontinue energy level will be expected to impact the nanoelectronics.

### (b) Coulomb Blockade Effect

The stored electron charge will raise the nanocrystal potential energy and reduce the electric field across the tunnel oxide, resulting in reduction of the tunneling current density during the write process. It is more dominant at low programming voltages (<3V). The Coulomb blockade effect can effectively inhibit the electron tunneling at low gate voltage and improve the flash memory array immunity to disturbance. Figure 2-18 exhibits the band diagram for before electron injected to nanocrystal and after one electron stored in nanocrysal, respectively. However, the reduced Coulomb blockade effect can be achieved by employing large size nanocrystals for large tunneling current and fast programming speed are considered. The Coulomb blockade effect has a serious effect on the retention time. Large tendency for electrons stored in nanocrystals will tunnel back into the channel if the potential energy is high in retention mode

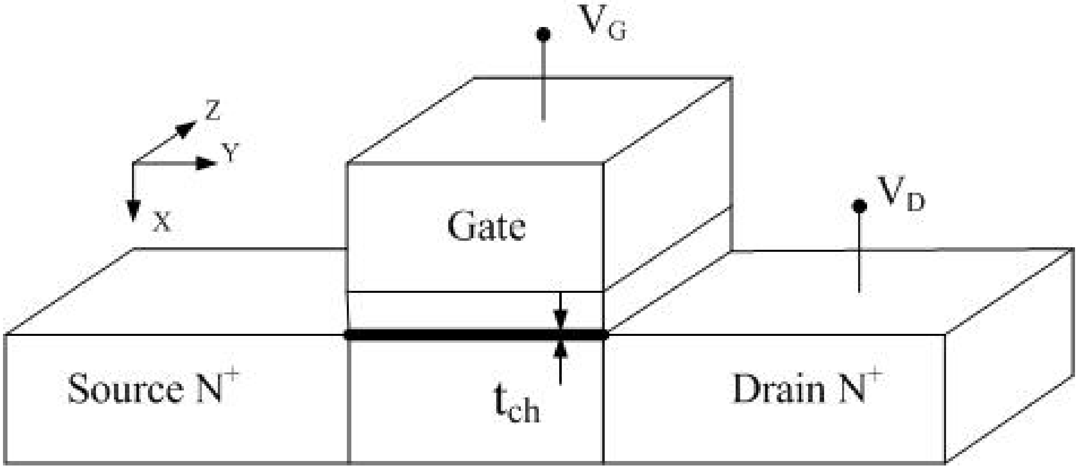


Figure 2-1 A schematic MOSFET cross section, showing the axes of coordinates and the bias voltages at the four terminals for the drain-current model

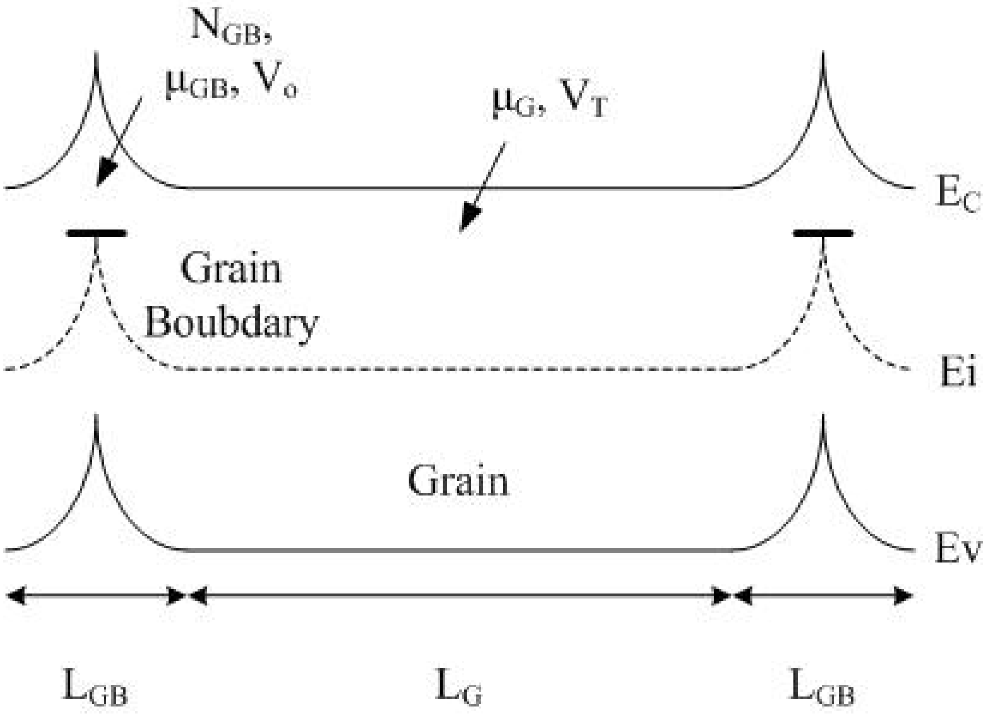


Figure 2-2 Energy band diagram in the lateral direction along the channel of n-channel polysilicon TFTs

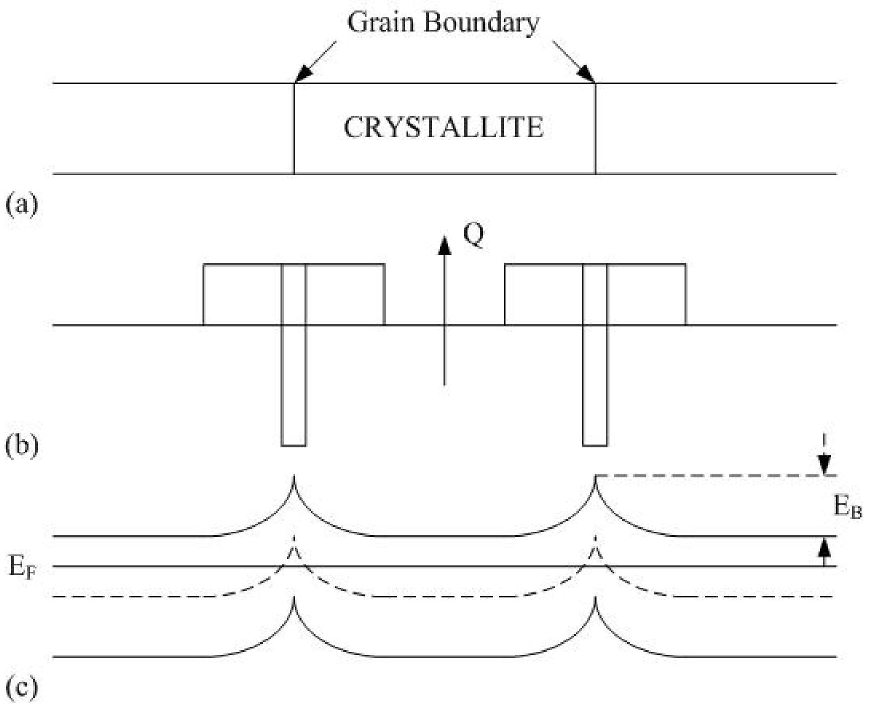


Figure 2-3 (a) Model for the crystal structure of polysilicon films. (b) The charge distribution within the crystallite and at the grain boundary. (c) The energy band structure of the polysilicon crystallites

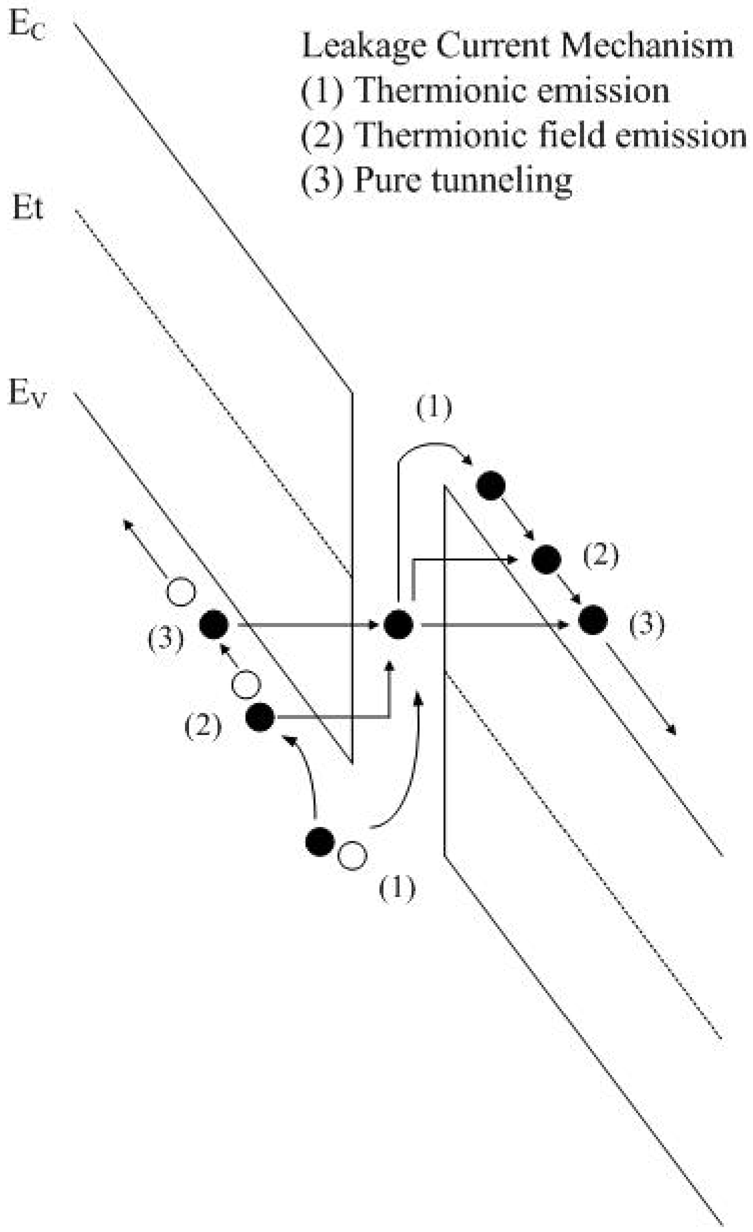


Figure 2-4 Three possible mechanisms of leakage current in poly-Si TFTs, including thermionic emission, thermionic field emission and pure tunneling

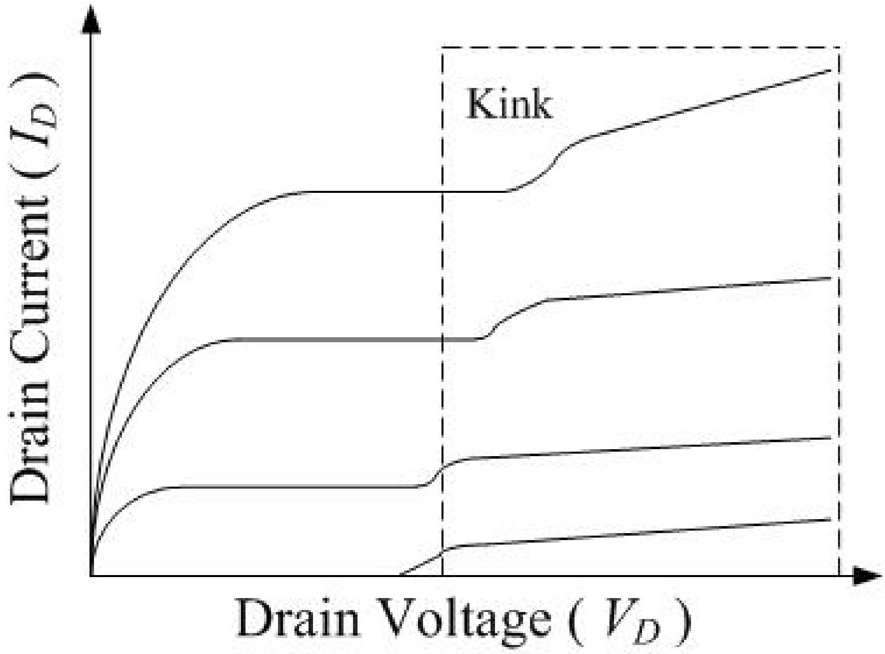


Figure 2-5 The kink effect in the output characteristics of an *n*-channel SOI MOSFET

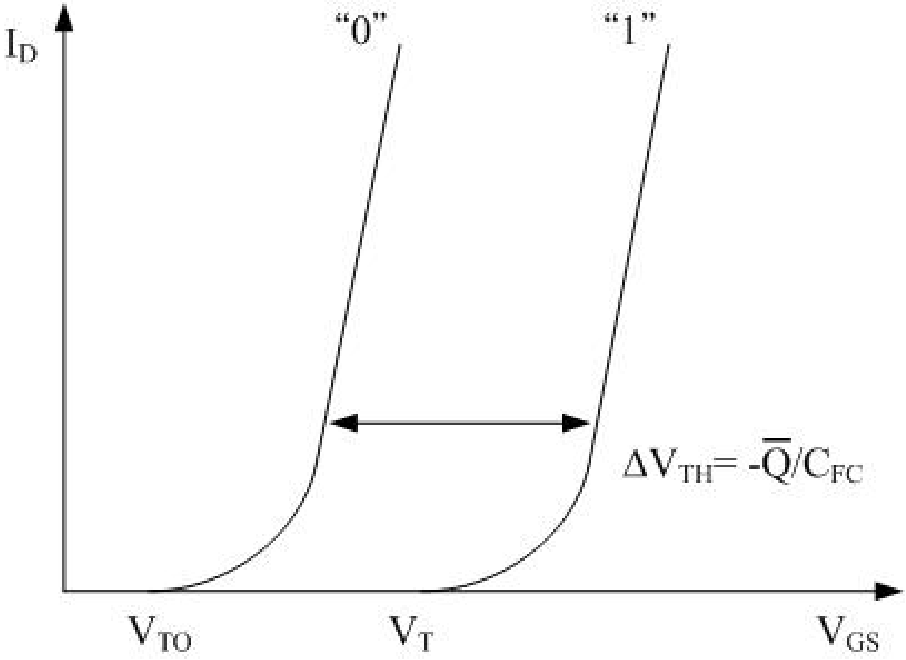


Figure 2-6 $I_D$–$V_{GS}$ curves of an FG device when there is no charge stored in the FG andwhen a negative charge $\overline{Q}$ is stored in the FG

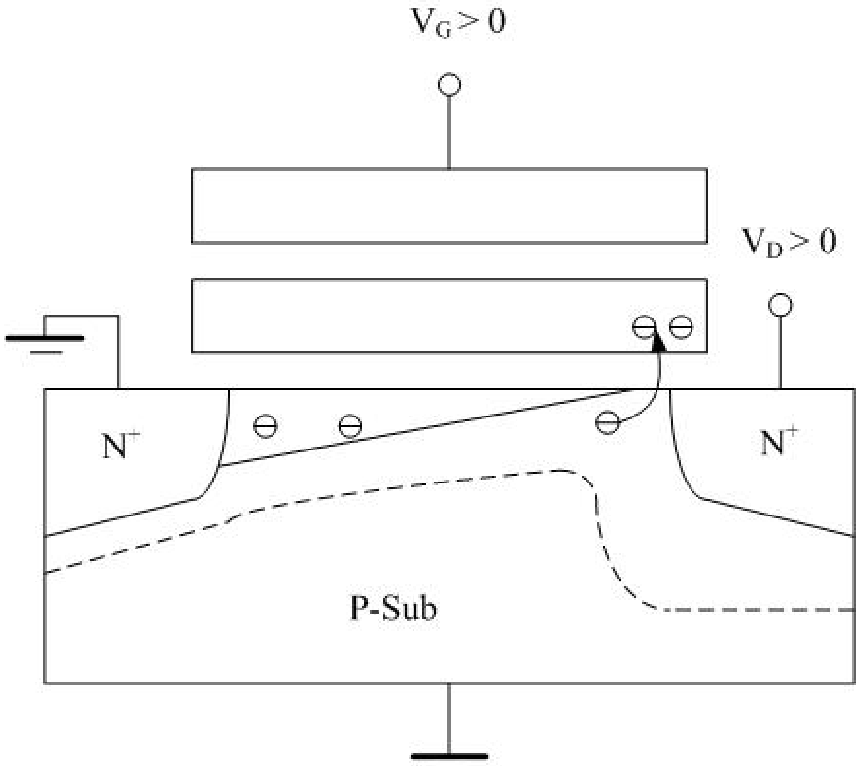


Figure 2-7 The procedure of channel hot electrons injection (*CHEI*)

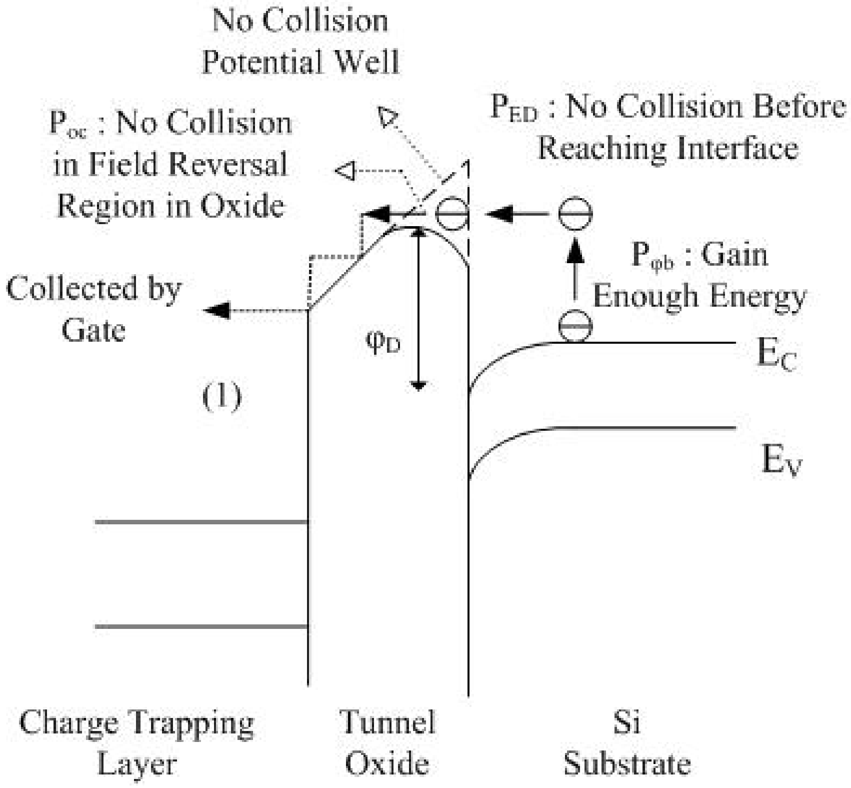


Figure 2-8 A schematic energy band diagram describing the three processes involved in electron injection

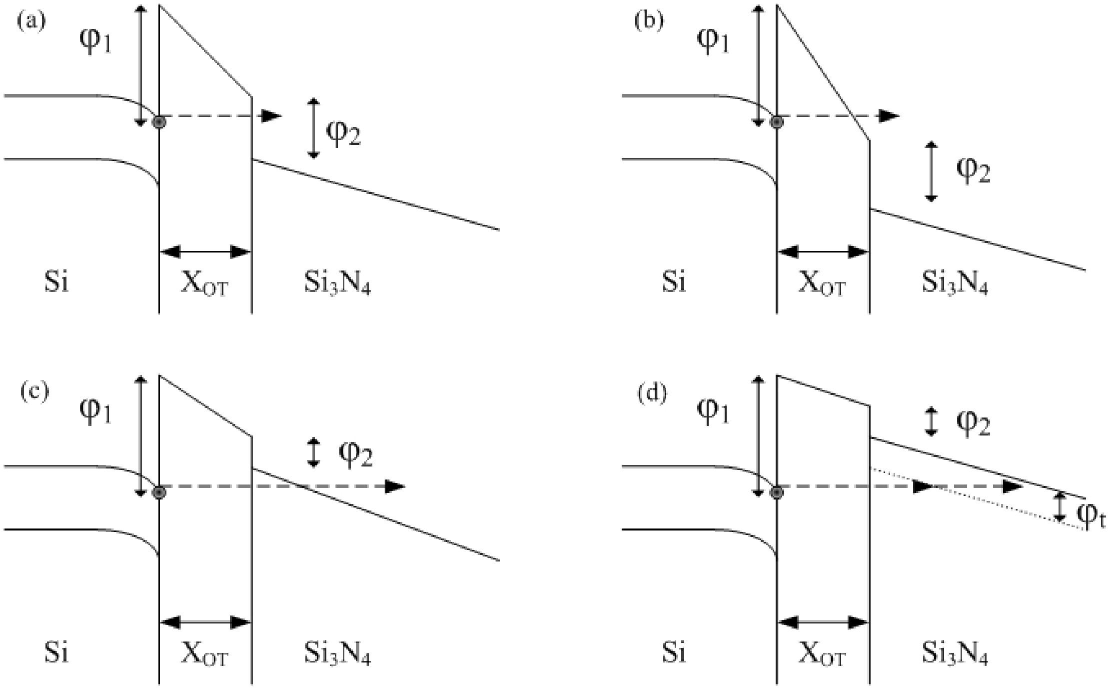


Figure 2-9 Fourth approaches to programming methods

(a)DT occur when $\frac{\phi_1}{X_{OT}} > |E_{OT}| > \frac{\phi_1 - \phi_2}{X_{OT}}$

(b)FN occur when $|E_{OT}| > \frac{\phi_1}{X_{OT}}$

(c)MFN occur when $\frac{\phi_1 - \phi_2}{X_{OT}} > |E_{OT}| > \frac{\phi_1 - \phi_2}{X_{OT} + \left( \varepsilon_{OX} / \varepsilon_N \right) X_N}$

(d)TAT occur when $\frac{\phi_3}{X_{OT}} > |E_{OT}| > \frac{\phi_3}{X_{OT} + \left( \varepsilon_{OX} / \varepsilon_N \right) X_N}$， $\phi_3 = \phi_1 - \phi_2 - \phi_t$

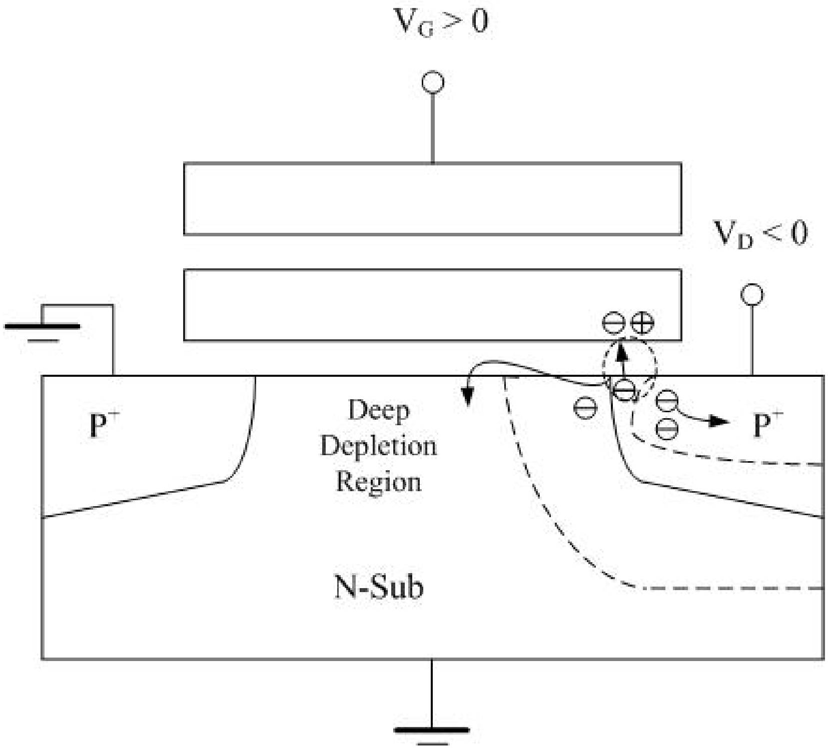


Figure 2-10 The procedure of band to band hot electron injection

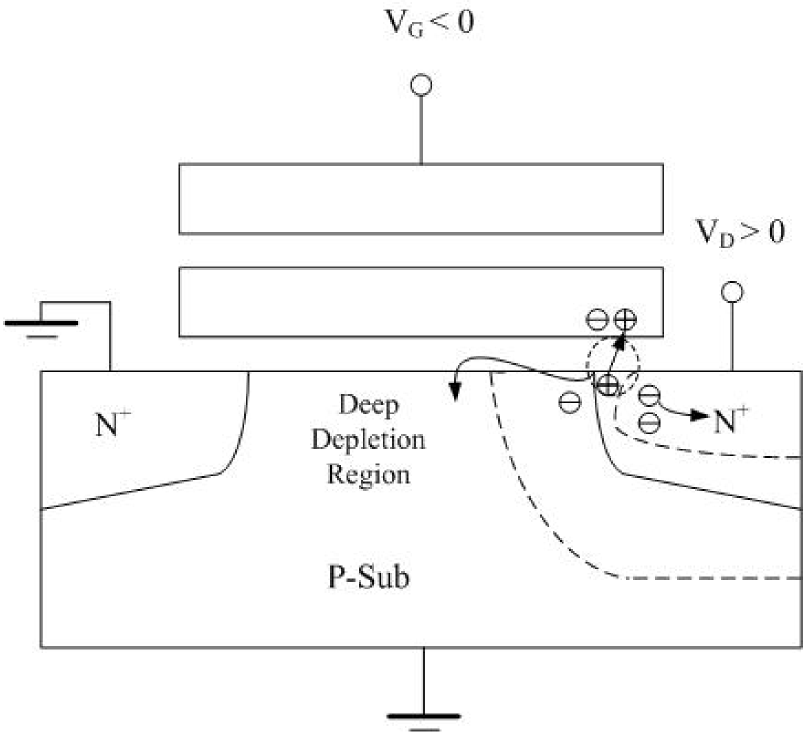


Figure 2-11 The procedure of band to band hot hole injection

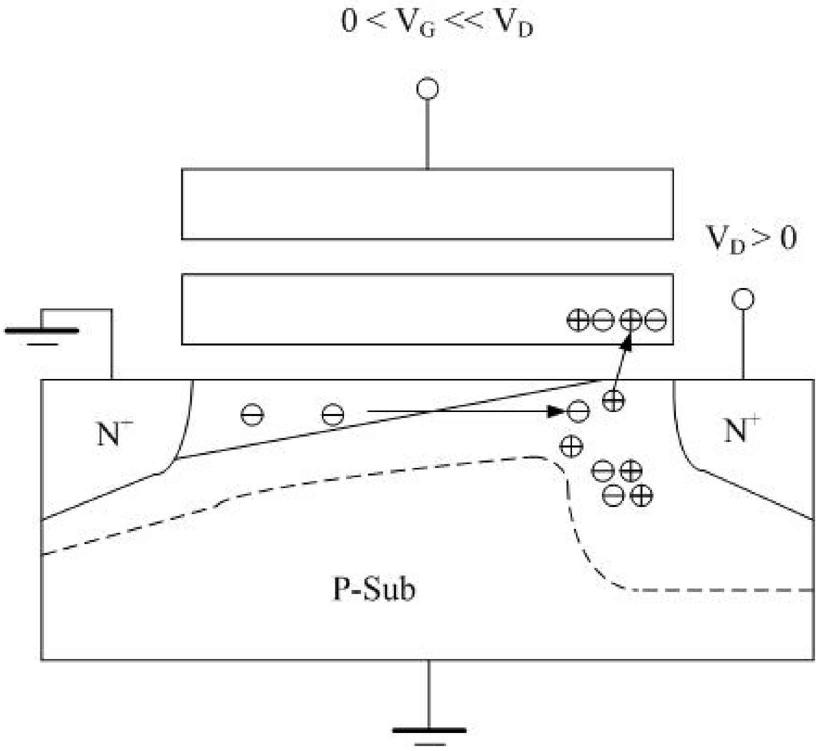


Figure 2-12 The procedure of hot hole injection

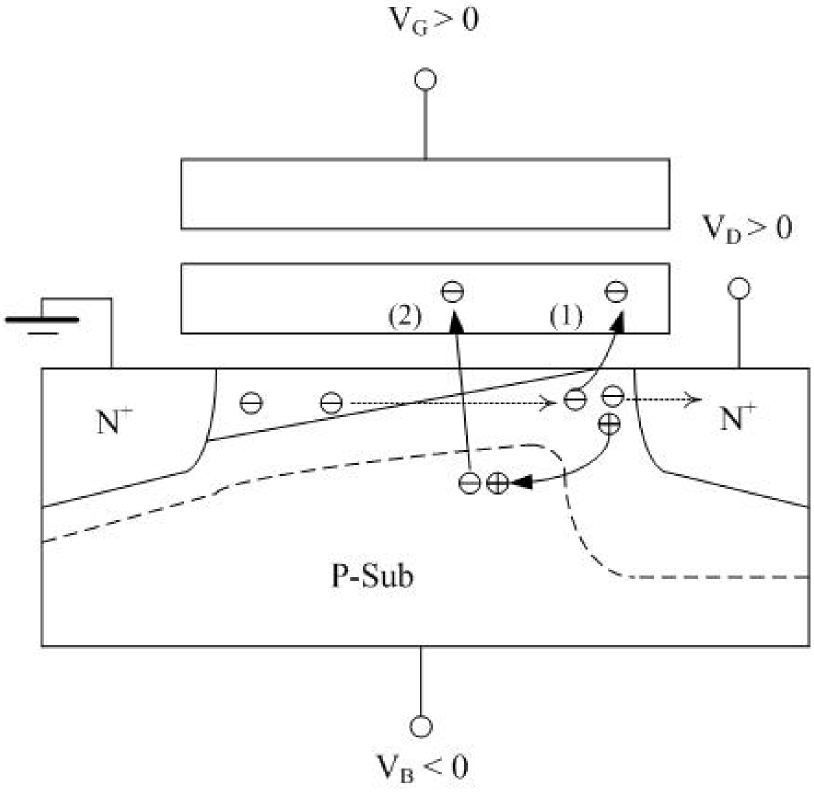


Figure 2-13 The procedure of channel initiated secondary electron injection (*CHISEL*)

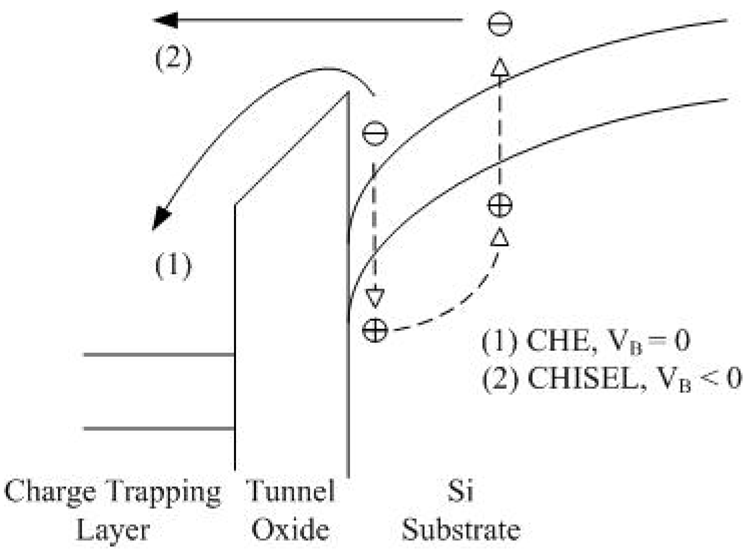


Figure 2-14 The band diagram of channel initiated secondary electron injection (*CHISEL*)

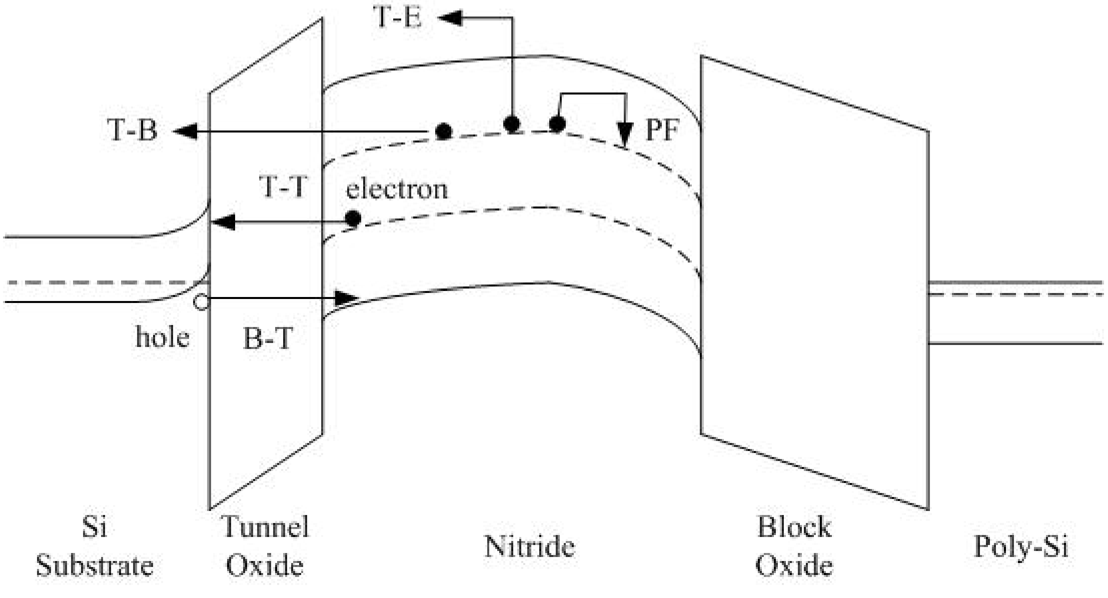


Figure 2-15 Bandgap diagram of a SONOS device in the excess electron state, showing retention loss mechanisms: trap-to-band tunneling (*T-B*), trap-to-trap tunneling (*T-T*), band-to-trap tunneling (*B-T*), thermal excitation (*TE*) and Poole–Frenkel emission (*PF*)

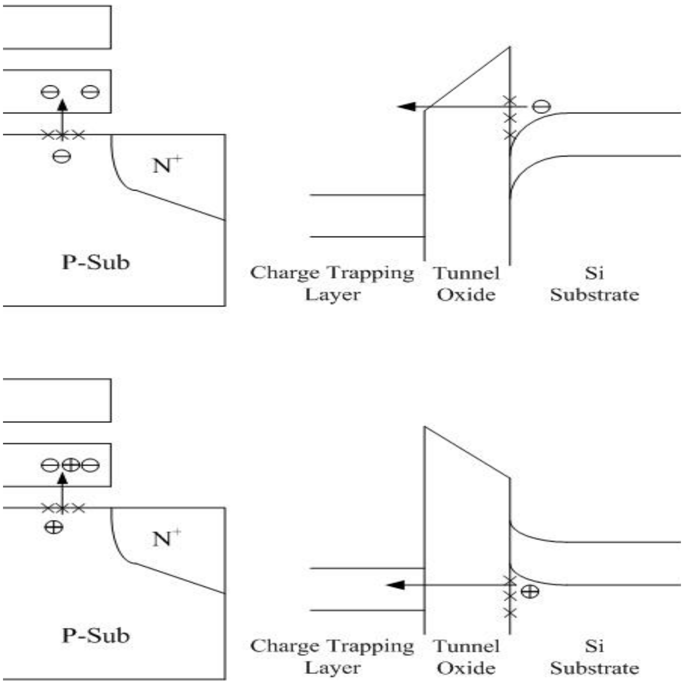


Figure 2-16 The procedure and band diagram for numerous program/erase circles

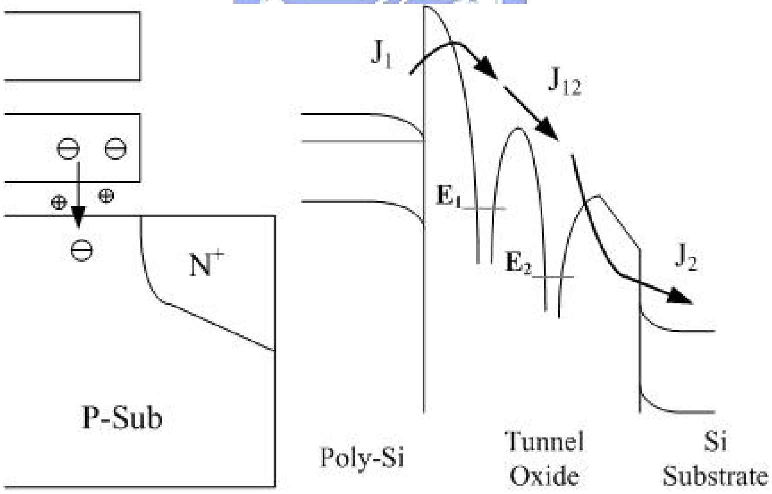
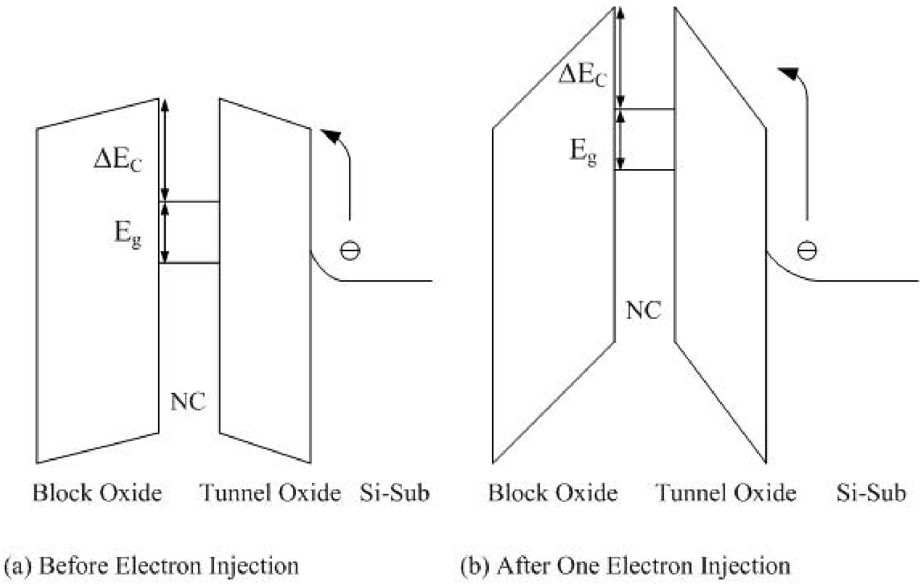


Figure 2-17 Anomalous stress induced leakage current (*SILC*) modeling. The leakage is caused by a cluster of positive charge generated in the oxide during erase



(a) Before Electron Injection (b) After One Electron Injection

Figure 2-18 The illustration of the band diagram for coulomb blockade effect (a) before electron injection, and (b) after one electron injection

# Chapter 3

# Enhancement of Fluorine-Ions-Implanted Poly-Si Thin Film Transistors using Solid Phase Crystallization

## 3.1 Introduction

In recent years the polycrystalline silicon thin film transistors (poly-Si TFTs) have been widely used in many applications, especially for active matrix liquid phase crystal displays (AMLCDs) [3.1-3.2]. The major attractions of the poly-Si TFTs in AMLCDs lie in the greatly improved carrier mobility. In addition, the capabilities of integrating the pixel switching elements, panel array, and peripheral driving circuit on the same substrates are also attractive [3.3-3.5]. The application of the poly-Si TFTs enables the fabrication of peripheral circuit and TFT array on the same glass substrate. The process complexity can be greatly simplified and the cost also can be reduced. The TFT array with high density, high resolution and high aperture ratio can be realized by using poly-Si TFTs as pixel switching elements. The channel width of poly-Si TFTs device can be scaled down while meeting the same pixel driving requirements as in a-Si TFT AMLCDs. For making high performance poly-Si TFTs, low-temperature technology is required for the realization of commercial flat-panel displays on inexpensive glass substrate, since the maximum process temperature is limited to less than 600℃. Solid phase crystallization (SPC) process is the widely used to recrystallize Si film due to its low cost and high uniformity in grain size. However, the SPC process requiring 24–48 hrs is a time consuming procedure, which obviously affects the throughput and thermal budget of fabrication processes. Besides, of the lower field effect mobility ($\mu_{FE}$) will limit the development for SPC poly-Si TFTs and, the poly-Si TFTs suffer from undesirable leakage current from trap states at the grain boundaries. Based on these issues of poly-Si TFTs, several processes have been applied to reduce the trap states and enhance the electrical characteristics [3.6-3.7]. The hydrogen plasma treatment is a widely used method to passivate the trap states to avoid the undesirable leakage current, but difficult to control the hydrogen concentration in the poly-Si film [3.8]. Recently, fluorine ion implantation has been applied to improve the electrical characteristics by eliminating the defects in the grain boundary [3.9-3.10]. The main purpose for fluorine ion implantation is to passivate the undesirable strain bonds at the interface between poly-Si and $SiO_2$. It was found that the fluorine piled up at the interface between the poly-Si and the oxide eliminating the strain bonds and can be the terminators of dangling bonding in poly-Si. In addition, the stronger Si-F bonds can replace weaker Si-H and Si-Si bonds and exhibit superior electrical reliability against DC stress, compared to standard poly-Si TFTs counterpart. However, previous issued reports need an additional oxide layer deposition and an additional thermal annealing. These extra steps will increase the difficulty for the fabrication of the poly-Si TFTs.

In this work the electrical behavior of SPC fluorine-ions-implanted poly-Si TFTs were investigated comprehensively. The amorphous silicon (a-Si) layer was deposited by using low pressure chemical vapor deposition (LPCVD) system. In addition, a simple re-crystallization process will be performed without the need of an initial pad oxide deposition, in contrast to the prior art.

## 3.2 Experimental

The 50-nm-thick undoped a-Si layer was deposited on oxide-coated silicon wafer by LPCVD system. Then, the fluorine ions were implanted into the a-Si layer without initial deposition of pad oxide layer. The ions implantation conditions were ion accelerating energy 11 KeV and the dosages $5\times10^{13}$, $5\times10^{14}$ and $5\times10^{15}cm^{-2}$, respectively. The re-crystallization process for the amorphous silicon (a-Si) film with and without fluorine ions implantation is performed by a thermal furnace at 600℃ for 24 hrs in $N_2$ ambient. After patterning the Si active regions, a 50-nm-thick tetraethylorthosilicate (TEOS) oxide layer and a 200-nm-thick poly-Si film were deposited by LPCVD system. The doping procedure of poly-Si gate electrode and source/drain was implemented simultaneously by the $P_{31}{}^{+}$ ions implantation with accelerating energy 17 KeV and the dosage $5\times10^{15}$ $cm^{-2}$. The dopant activation was realized by the the following deposition of a TEOS oxide passivation layer using LPCVD system at 700℃ for 3 hrs. The contact holes were patterned by buffer oxide etching (BOE) solution. The aluminum layer was deposited and then patterned as metal electrode pads. Finally, the devices were sintered in a thermal furnace at $350^0C$ for 30 min. The poly-Si TFTs device cross-section is shown in Figure 3-1.

## 3.3 Results and discussion

This work first investigates the electrical properties of fluorine ions implanted poly-Si TFTs. Figure 3-2 illustrates the transfer characteristics of poly-Si TFTs with fluorine ions implantation at an ion dosage of $5\times10^{13}$ $cm^{-2}$ and a typical poly-Si TFTs. Figure 2 summarizes major electrical parameters of the poly-Si TFT devices. The threshold voltage ($V_{TH}$) is given by the gate voltage that yields the drain current ($I_{DS}$) ($I_{DS} = 10\ nA \times W/L$). The electrical characteristics are improved with the fluorine implantation dosage $5\times10^{13}$ $cm^{-2}$, especially for the $\mu_{FE}$ and $V_{TH}$. The value of $\mu_{FE}$ for the fluorine implanted poly-Si TFTs is higher than 53.82 $cm^2$/v-s. The decrease of $V_{TH}$ benefits the proposed poly-Si TFTs application on electronics. Also, the on current of the fluorine incorporated poly-Si TFTs is significantly enhanced. The $I_D$-$V_D$ output characteristic is shown in Figure 3-3, exhibiting the greatly improved drain current of the fluorine-ions-implanted poly-Si TFTs at $V_G = 4, 7, 10$ volt, respectively. Figure 3-4 shows the activation energy ($E_A$) of drain current as a function of the gate voltage measured at $V_D$=5V for the standard and the fluorine-ions-implanted poly-Si TFTs. The $E_A$ was obtained by the measurement of $I_D$-$V_G$ characteristic at temperatures ranging from 20℃ to 150℃. The $E_A$ represents the carrier transportability which is related to the barrier height in the poly-Si channel [3.11]. The $E_A$ of off-state current is increased and the $E_A$ of on-state current is reduced for the fluorine-ion-implanted poly-Si TFTs, implying that fluorine implantation alters the trap state density. The fluorine ions effectively piled up at the poly-Si interface without pad oxide deposition, as demonstrated in Figure 3-5, the secondary ions mass spectroscope (SIMS) analysis. The ostensibly oxidized Si layer supplies fluorine ions a driving force to segregate at the surface during thermal processes. Hence, no extra thermal annealing steps were needed to segregate fluorine ions at the surface as compared with prior art. It has been reported that the deep trap states can be eliminated effectively by using fluorine ions implantation, leading to the reduced $V_{TH}$ in n-channel poly-Si TFTs [3.10]. In this work, a minimum of $V_{TH}$ is obtained with an optimal fluorine ion implantation dosage of $5\times10^{13}$ cm$^{-2}$.

To investigate the device reliability, the poly-Si TFTs were bias stressed at $V_D$=20V and $V_G$=20V for varied time durations of 100 sec, 200 sec, 600 sec, 1000 sec. More moderate threshold voltage variation ($\Delta V_{TH}$) was obtained in the fluorine-ions-implanted poly-Si TFTs than that in the standard poly-Si TFTs, as shown in Figure 3-6. Hot carrier multiplication near the drain side causes the degradation of $V_{TH}$, $I_{ON}$ and $S.S.$ It has been reported that the hot carrier stress induced degradation is attributed to the following two possible cases. One is the generation of gate oxide/poly-Si interface states, and the other is the formation of Si-Si or Si-H weak bonds in the poly-Si channel [3.12-3.13]. The fluorine ions terminate the Si dangling bonds and the stronger Si-F bonding possesses superior endurance against hot carrier stress, thereby exhibiting the enhanced reliability. Figures 3-7 and 3-8 separately show the $\Delta I_{ON}$ and $\Delta S.S$ of poly-Si TFTs after DC bias stress. Since the strong Si-F bonds prevent the generation of Si dangling bonds, the fluorine-ions-implanted poly-Si TFTs can suffer less degradation of $V_{TH}$, $I_{ON}$ and $S.S$ compared to the conventional poly-Si TFTs.

Electrical properties of the fluorine-ions-implanted poly-Si TFTs with heavy implantation dosages were also studied in this work. Figure 3-9 shows the electrical prosperities of poly-Si TFTs with various fluorine ions implantation dosages. Table 3-1 summarizes the key electrical parameters. It is found that the electrical characteristics of ploy-Si TFTs are degraded as the implantation dosage increases, especially for the case of $5\times10^{15}$ cm$^{-2}$. The $\mu_{FE}$, $V_{TH}$ and $S.S$ are all degraded for higher fluorine ions implantation dosage, as compared to the standard poly-Si TFTs. With the fluorine implantation dosages higher than Si solid solubility, the trap state density could be increased significantly as the implantation dosage increases. The segregated fluorine ions in the poly-Si channel will not passivate the trap states, but generate additional defects to degrade the electrical properties. In addition, the fluorine ions are prone to accumulate and form more fluorine clusters during the sequent fabrication process, even worsening the electrical characteristics [3.14, 3.15].

It is possibly thought that one of causes for the electrical improvement of the poly-Si TFTs might be from the enhancement in the recrystallized poly-Si grain size after ion implantation process. However, the possibility does not appear in this work. Scanning electron microscopy (SEM) image shown in Figure 3-10 apparently reveals a little difference in grain size between the poly-Si film with and without fluorine ions implantation. Therefore, it is reasonably believed electrical characteristics of the fluorine-ions-implanted poly-Si TFTs are less dependent on the poly-Si grain size. We conclude the incorporation of fluorine in poly-Si film plays a critical role in the electrical improvement of the fluorine-ions-implanted poly-Si TFTs.

## 3.4 Conclusions

In this work it has been found that electrical characteristics of the poly-Si TFTs are enhanced greatly with an optimum implantation dose of $5\times10^{13}$ $cm^{-2}$ by decreasing the trap state density. The significant improvements in field effect mobility and electrical reliability have been obtained, presumably due to the formation of stronger Si-F bonds instead of weak Si-Si and Si-H bonds in poly-Si layer. The F-incorporated poly-Si TFTs thereby can possess higher hot carrier endurance and improve the device reliability. With the fluorine implantation dosages higher than Si solid solubility, the trap state density could be increased significantly as the implantation dosage increases. The segregated fluorine ions in the poly-Si channel will not passivate the trap states, but generate additional defects to degrade the electrical properties. The proposed technology with fluorine ions implantation in poly-Si is practicable and compatible with the conventional poly-Si TFTs processes, potentially applicable for AMLCDs.

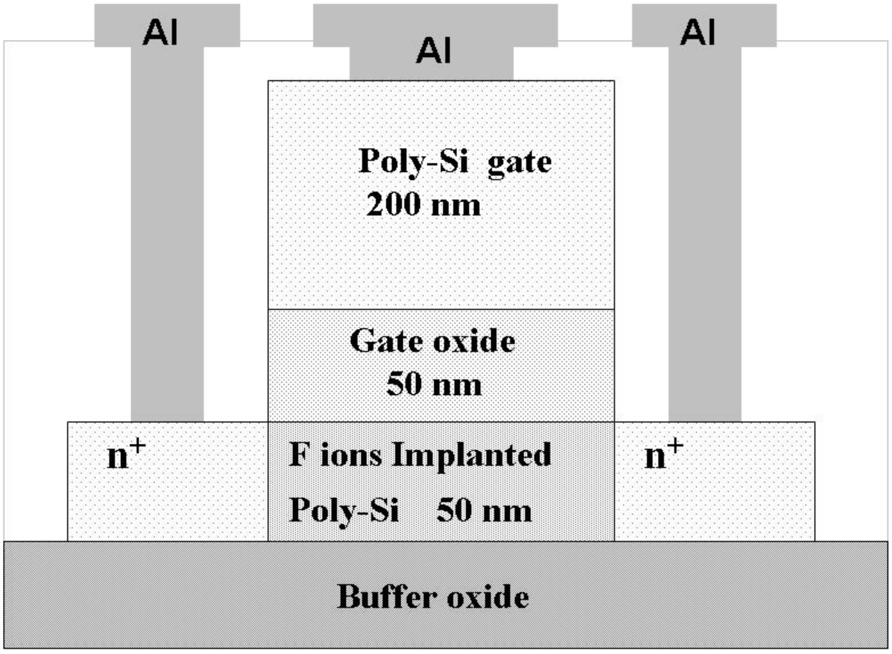
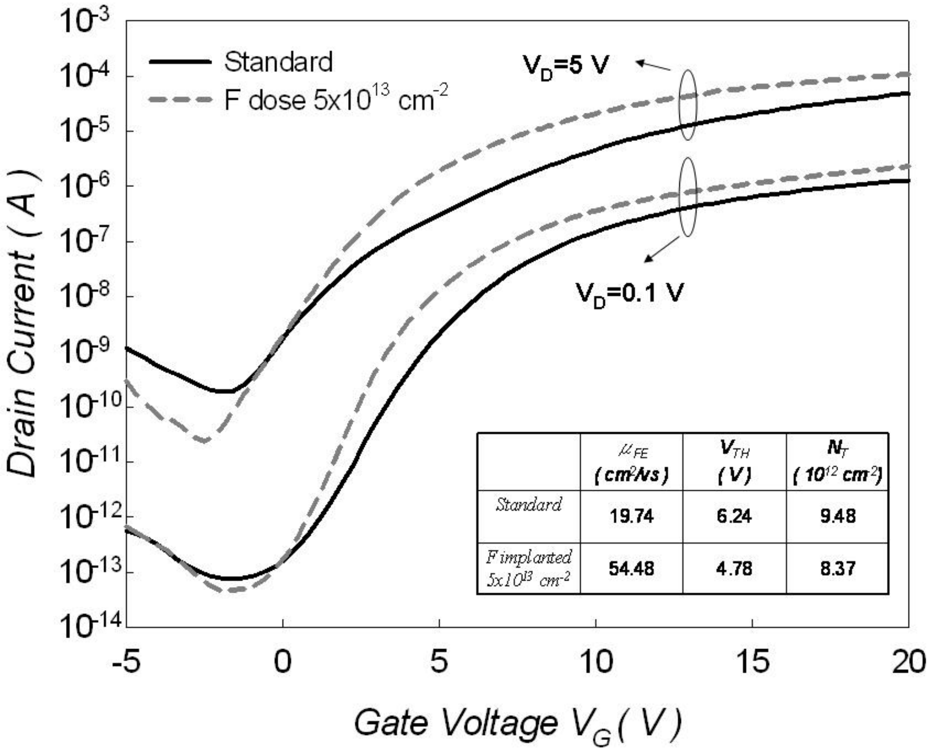


Figure 3-1 The cross-section of F-ions incorporated poly-Si TFTs structure



|  | $\mu_{FE}$ ( $cm^2/Vs$ ) | $V_{TH}$ ( V ) | $N_T$ ( $10^{12}$ $cm^{-2}$ ) |
|---|---|---|---|
| Standard | 19.74 | 6.24 | 9.48 |
| F implanted<br>$5x10^{13}$ $cm^{-2}$ | 54.48 | 4.78 | 8.37 |

Figure 3-2 Transfer characteristics ($I_D$-$V_G$) of the standard and the fluorine-implanted poly-Si TFTs with F ions implantation dosage of $5\times10^{13}$ $cm^{-2}$ (W/L=10um/10um)

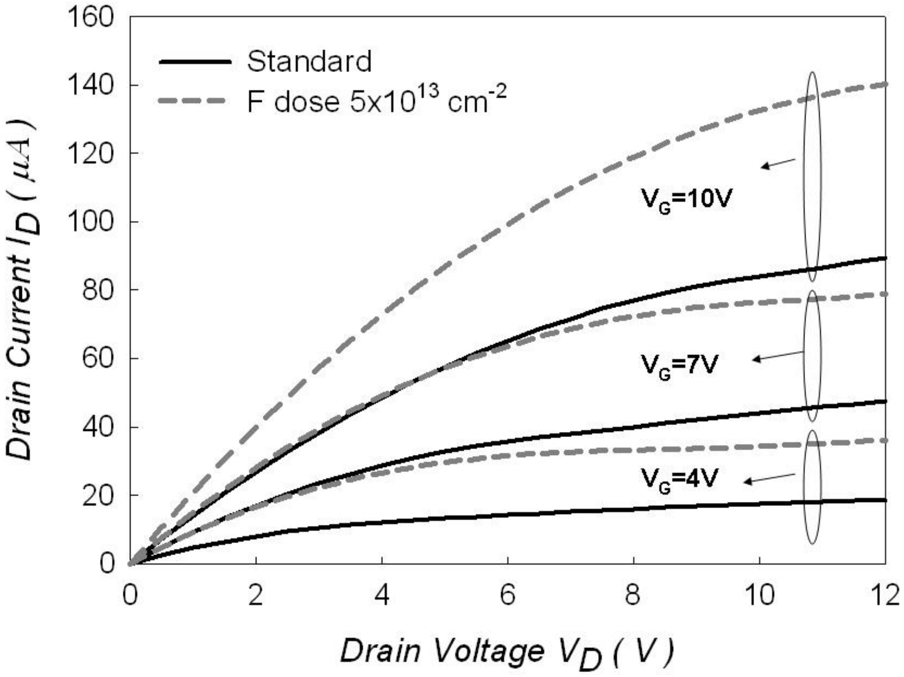


Figure 3-3 Output characteristics ($I_D$-$V_D$) of the standard and the fluorine-implanted poly-Si TFTs with F ions implantation dosage of 5×10$^{13}$ cm$^{-2}$ (W/L=10um/10um)

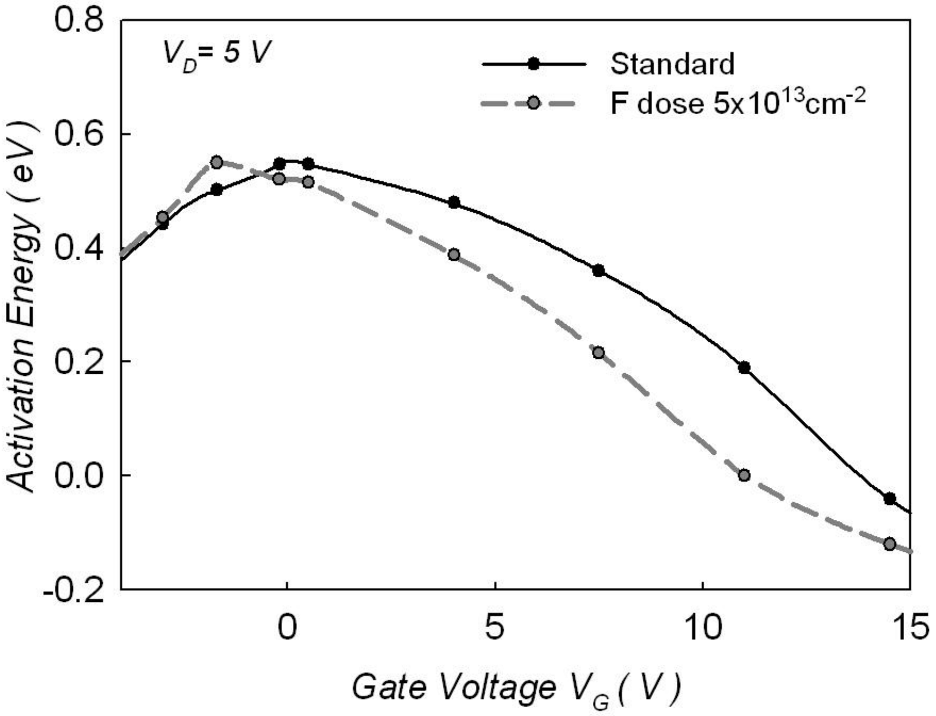


Figure 3-4 The activation energy ($E_A$) of the standard and the fluorine-implanted poly-Si TFTs with F ions implantation dosage of 5×10$^{13}$ cm$^{-2}$ at $V_D$=5 V

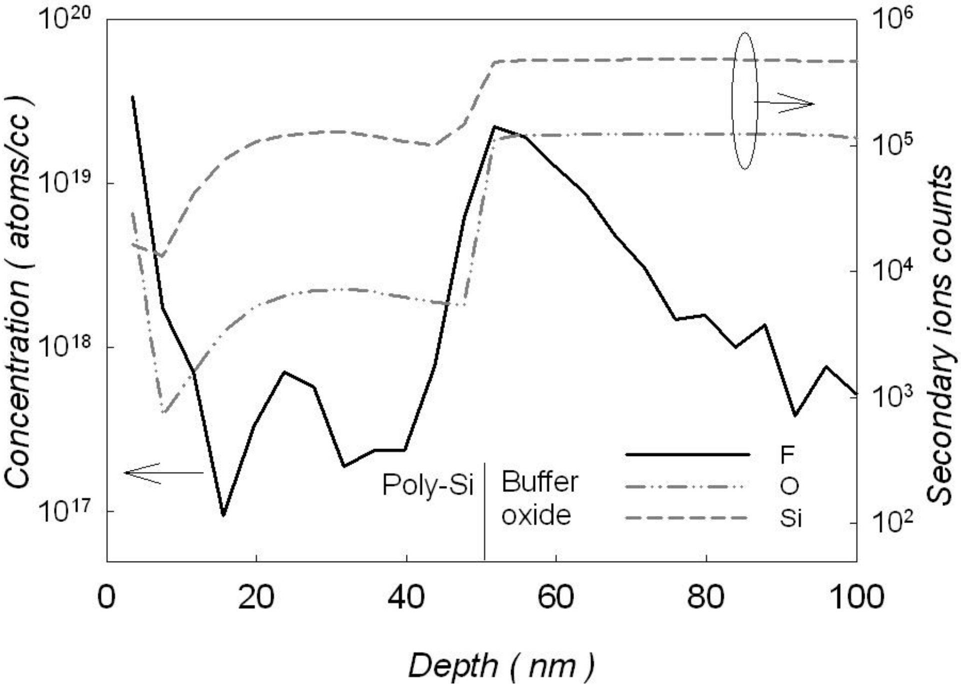


Figure 3-5 Secondary ions mass spectroscope (SIMS) analysis of fluorine-implanted a-Si film with dosage of $5\times10^{13}$ cm$^{-2}$ after solid phase recrystallization process

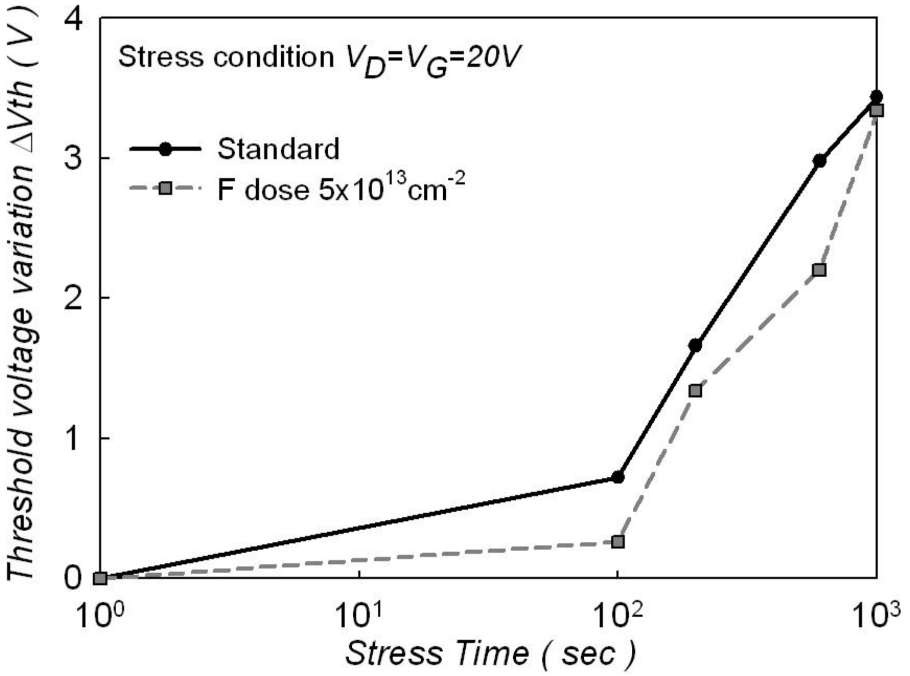


Figure 3-6 The threshold voltage variation ($\Delta V_{TH}$) versus stress duration for the standard and the fluorine-implanted poly-Si TFTs with F ions implantation dosage of $5\times10^{13}$ cm$^{-2}$

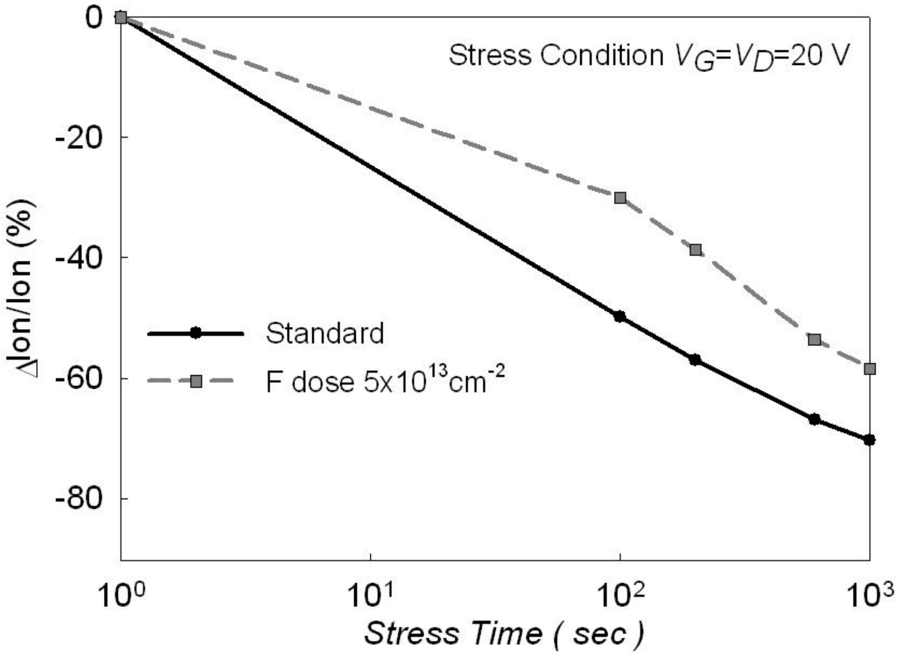


Figure 3-7 The on-current variation *($\Delta I_{ON}/I_{ON}$)* verse stress time for the standard and the fluorine-implanted poly-Si TFTs with implantation dosage of 5×10$^{13}$ cm$^{-2}$

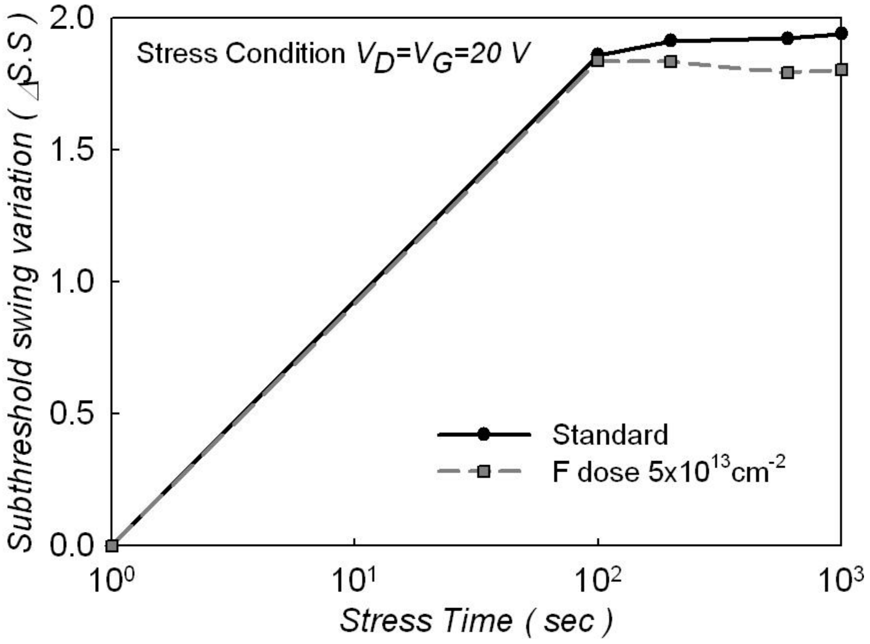


Figure 3-8 The subthreshold swing variation (*ΔS.S*) verse versus stress duration for the standard and the fluorine-implanted poly-Si TFTs with F ions implantation dosage of 5×10$^{13}$ cm$^{-2}$

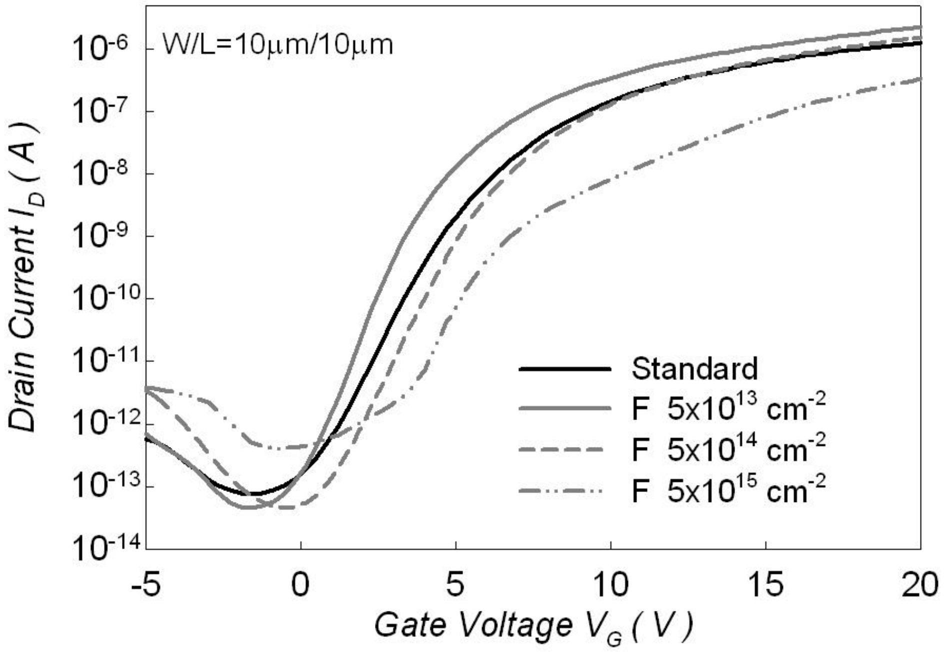


Figure 3-9 The transfer characteristics ($I_D$-$V_G$) of the standard and the fluorine-implanted poly-Si TFTs with various F ions implantation dosages

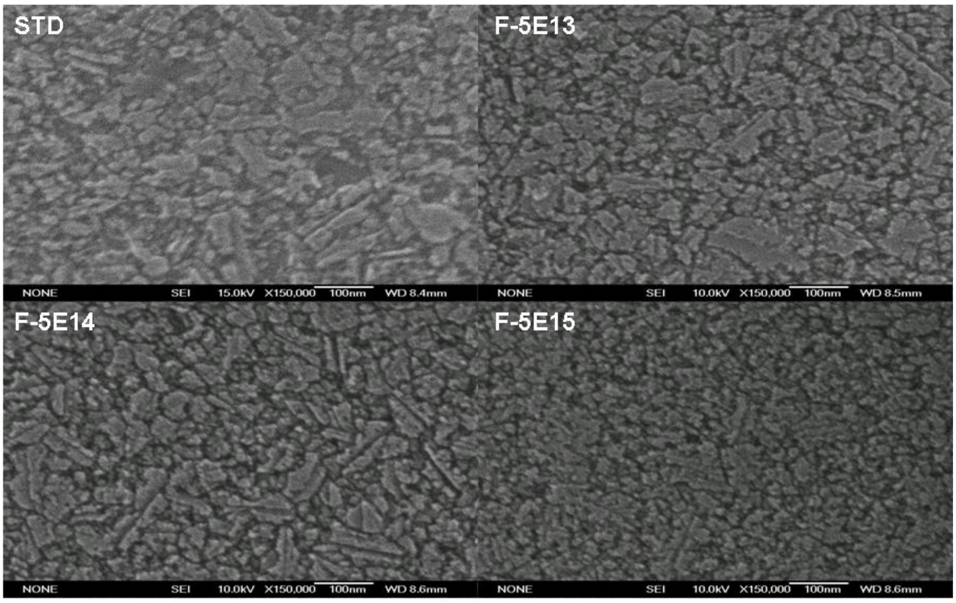
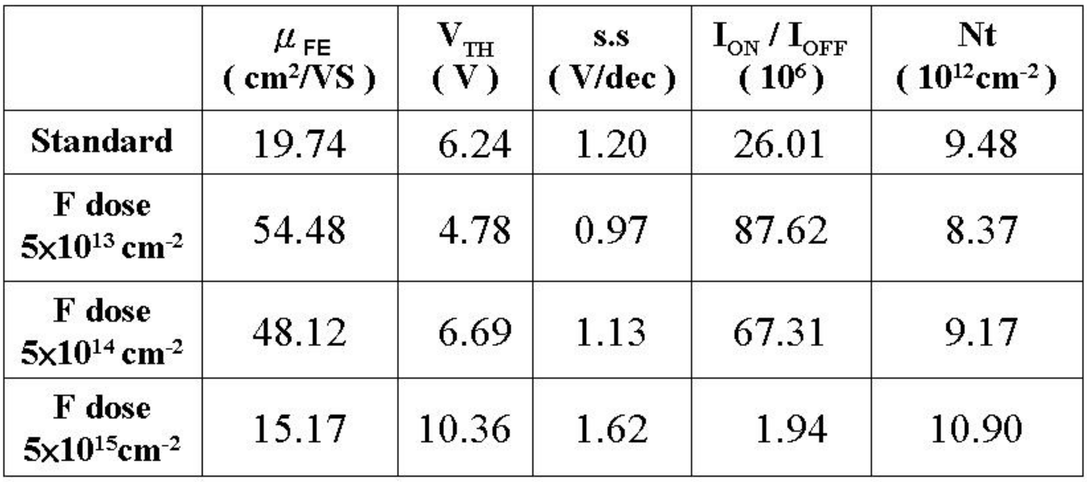


Figure 3-10 Scanning electron microscopy (SEM) images of the poly-Si film with and without fluorine ion implantation

Table 3.1 The critical electrical parameters for the standard and the F-ions-implanted poly-Si TFTs with various implantation dosages



|  | $\mu_{FE}$ ( $cm^2/VS$ ) | $V_{TH}$ ( V ) | s.s ( V/dec ) | $I_{ON}$ / $I_{OFF}$ ( $10^6$ ) | Nt ( $10^{12}cm^{-2}$ ) |
|---|---|---|---|---|---|
| **Standard** | 19.74 | 6.24 | 1.20 | 26.01 | 9.48 |
| **F dose $5x10^{13}$ $cm^{-2}$** | 54.48 | 4.78 | 0.97 | 87.62 | 8.37 |
| **F dose $5x10^{14}$ $cm^{-2}$** | 48.12 | 6.69 | 1.13 | 67.31 | 9.17 |
| **F dose $5x10^{15}cm^{-2}$** | 15.17 | 10.36 | 1.62 | 1.94 | 10.90 |

# Chapter 4

# Performance Enhancement of Excimer Laser Crystallized Poly-Si Thin Film Transistors with Fluorine Implantation Technology

## 4.1 Introduction

Low-temperature technology is required to realize commercial flat-panel displays on inexpensive glass substrate when manufacturing high performance poly-Si TFTs, since the maximum process temperature is restricted less than 600℃. However, poly-Si TFTs suffer from undesirable leakage current. Therefore, many methods have been proposed to resolve the detrimental effects of grain boundaries by enlarging the grain size or passivating the defects [4.1-4.3]. Experimental results indicate that excimer laser annealing can crystallize a-Si film to fabricate low temperature poly-Si TFTs with very few in-grain defects [4.1-4.2]. For the excimer laser crystallization (ELC) thermal annealing process, the difference of thermal expansion coefficient between the molten poly-Si film and buffer oxide causes serious mechanical stress. The mechanical stress is well known to cause numerous interface states and degrade the electrical properties of metal-oxide-semiconductors devices [4.3-4.4]. Moreover, the trap states present between the interface of poly-Si and buffer oxide were reported to degrade the electrical properties, such as on current ($I_{ON}$), subthreshold swings ($S.S$), and off current ($I_{OFF}$). It is believed that the reduction of trap states between poly-Si and buffer oxide improves the performance of poly-Si TFTs [4.5]. Based on this issue, trap state density elimination technology is also adopted to enhance the electrical properties. Hydrogen plasma treatment is a widely used method for passivating the trap states to avoid current leakage [4.6]. However, it is difficult to precisely control the concentration of hydrogen in the TFTs by the plasma treatment. F-ion implantation has recently been applied to improve the electrical characteristics of poly-Si films by eliminating defects at the grain boundaries [4.7-4.8]. The objective of F-ion implantation is to passivate undesirable strain bonds at the interface between poly-Si and $SiO_2$ and on the poly-Si surface. It has been found that the piling up of F at the interface between the poly-Si and the oxide can effectively reduce the strain bonds. However, the prior art required an extra oxide layer deposition and additional thermal annealing process. The extra process steps increase the difficulty in fabricating poly-Si TFTs. It is clearly indicated that the surface-oxidized a-Si also cause the F segregated to the poly-Si interface during thermal crystallization in our reported research [4.9-4.10]. Hence, the process difficulty can be decreasing. Since the segregation of fluorine at the poly-Si and buffer oxide interface eliminates the mechanical stress, the release of mechanical strain and the trap state passivation can be performed using the F-ion implantation. Additionally, strong Si-F bonds replace the weaker Si-H and Si-Si bonds, enhancing the electrical *DC* stress reliability, compared to standard poly-Si TFTs.

This work will investigate the behaviors of fluorine in the poly-Si film after thermal annealing and the electrical characteristics of F-ions-implanted poly-Si TFTs. The various doses of F ions were implanted into the a-Si layer which was deposited first by low pressure chemical vapor deposition (LPCVD) system. Then, the re-crystallization was performed by using excimer laser annealing system.

## 4.2 Experimental

The 50-nm-thick undoped a-Si layer was deposited on oxide-coated silicon wafer by LPCVD system. Then the F ions were implanted to the a-Si layer without any prior deposition of pad oxide. The ions implantation conditions were set at ion accelerating energy is 11 KeV and the doping dosages are $5\times10^{13}$, and $5\times10^{15}\text{cm}^{-2}$, respectively. The crystallization for the F-ions-implanted a-Si film and standard a-Si was realized by excimer laser annealing system. The re-crystallization was realized by a KrF excimer laser system at room temperature in vacuum ( $\sim10^{-3}$ Torr) with laser energy of 300 mJ/cm$^2$. After patterning and etching the active region, the 50-nm-thick $SiO_2$ layer deposited from tetraethylorthosilicate (TEOS) oxide layer and the 200-nm-thick poly-Si gate were deposited by LPCVD system. The $P_{31}^+$ ions served as the source/drain ion implantation after patterning and etching the poly-gate. The ion accelerating energy is at 17 KeV and the dosage is $5\times10^{15}\ \text{cm}^{-2}$. The activation was realized by the deposition of the TEOS passivation layer using LPCVD system at 700 ℃ for 3 hrs. The contact holes regions were patterned and then etched by buffer oxide etching (BOE) solution. The aluminum layers was deposited as the metal layers, and then patterned to form metal pads. Finally, the devices are sintered in the thermal furnace at 350℃ for 30 min. The device cross-section was shown in the insert of Figure 4-1. In this study, all devices investigated have channel length/width of 10um/10um.

## 4.3 Results and discussion

This study first examines the electrical characteristics of F-ions-implanted poly-Si TFTs. Figure 1 illustrates the transfer characteristics of poly-Si TFTs for F ion implantation dosage of $5\times10^{13}\text{cm}^{-2}$ and standard poly-Si TFTs without F ion implantation. Table 4-1 summarizes the major TFT device parameters. The threshold voltage ($V_{TH}$) is defined as the gate voltage yields the drain current ($I_{DS}$) ($I_{DS}= 10\ nA \times W/L$). The electrical characteristics are improved by F ion implantation at a dose of $5\times10^{13}\ \text{cm}^{-2}$, particularly for the $\mu_{FE}$ and $V_{TH}$. The $\mu_{FE}$ value for F-ions-implanted poly-Si TFTs was twice the magnitude of the standard one (56.65cm$^2$/volt-sec to 103.94cm$^2$/volt-sec). The decrease of $V_{TH}$ increased its potential for poly-Si TFTs application, and significantly improved the on-state performance of the F-ions-incorporated poly-Si TFTs. Moreover, the off-state current is also decreased. The improvement of electrical characteristics could be attributed to the reduction of trap states in the poly-Si TFTs. In order to confirm the effect of trap state, activation energy analysis was also executed in this study. Figure 4-2 shows the activation energy ($E_A$) of drain current as a function of the gate voltage measured at $V_D = 5$V for the standard and the F–ion-implanted poly-Si TFTs. The $E_A$ was determined by measuring the $I_D - V_G$ characteristic in the temperature range from 20℃ to 150℃ [4.11]. $E_A$ denotes the carrier transportability, which is related to the barrier height in the poly-Si channel. For the F-ion-implanted poly-Si TFTs, the value of $E_A$ extracted from on-state current is reduced, while $E_A$ extracted from the off-state current is increased, indicating that F-ion implantation effectively reduces the trap state density. Furthermore, by calculating the trap state density in the bandgap [4.12], the tail states and deep states are clearly eliminated through the way of F ions passivation, as shown in the insert of Fig. 4-2. The superior values of $S.S$, $V_{\mathrm{TH}}$ and $\mu_{FE}$ for the F-ions-implanted poly-Si TFTs confirm the decrease of trap state density at the interface between poly-Si and oxide. This result is consistent with the above electrical characteristics. The deep trap states can be effectively eliminated by using F ions implantation, leading to reduced $V_{TH}$ in n-ch poly-Si TFTs [4.2]. The fluorine effectively piled up at the poly-Si interface without the need of pad oxide deposition, as revealed in secondary ion mass spectrometer (SIMS) analysis in the insert of Figure 4-3. The native oxide of Si film provides F driving force to segregate at the surface during thermal annealing. Therefore, no additional thermal annealing step and manufacture processes were needed to accumulate the F ions. In addition, the high concentration of F ions between poly-Si and buffer oxide is also found. The mechanical stress resulted from ELC process can be thereby reduced by the incorporation of F ions. The stronger Si-F bonds are easily formed due to the high eletronegativity of F atoms. Fluorine piled up at the poly-Si/buffer oxide interface, which reduces the stress-induced strain bonds and form stronger Si-F bonds, leading to the decrease of off current. The accumulated F ions at the surface of poly-Si lower the trap states to achieve good performance of poly-Si TFTs. Hence, the improvement of ELC poly-Si TFTs is due to the release of mechanical stress at the poly-Si/buffer oxide interface and the passivation effect of fluorine at poly-Si surface.

To examine the device reliability, the poly-Si TFTs were bias-stressed at $V_D$ = 20V and $V_G$ = 20V for varied time durations of 100 sec, 200 sec, 600 sec and 1000 sec. Smaller threshold voltage variation was obtained in F-ion-implanted poly-Si TFTs compared to standard poly-Si TFTs, as demonstrated in Figure 4-4. Hot carrier multiplication near the drain side caused the degradation of $V_{TH}$. The F terminated the Si dangling bonds and formed the stronger Si-F bonding endurant to hot carrier degradation, leading to enhanced electrical reliability. Figures 4-5 and 4-6 illustrate the $\Delta I_{ON}$ and $\Delta S.S$, respectively, after DC bias stress. Impact ionization multiplication generated from hot carrier effect, near the drain side, degraded the $V_{TH}$, $I_{ON}$ and $S.S$, reportedly due to the generation of gate oxide/poly-Si interface states and/or the Si–Si and/or Si–H weak bonds in the poly-Si channel [4.13-4.14]. The strong Si–F bonds resulting from incorporating F into poly-Si TFTs prevent the bonds from breaking. Hence, F-ions-implanted poly-Si TFTs suffered less degradation of $V_{TH}$, $I_{ON}$ and $S.S$ than that of conventional poly-Si TFTs.

The electrical characteristics of poly-Si TFTs with heavily high dosage of F ion implantation were also considered in this investigation. The electrical characteristics were degraded as the implantation dosage increased ($5\times10^{15}$cm$^{-2}$). Figure 4-7 illustrates the electrical characteristics and the key parameters. The values of $\mu_{FE}$, $V_{TH}$ and $S.S$ for higher F-ions-implanted poly-Si TFTs were degraded as compared to the standard poly-Si TFTs. The trap state density increased as the implantation dosage increased. The segregated fluorine ions in the poly-Si channel will not passivate the trap states, but generate additional defects to degrade the electrical properties. In addition, the fluorine ions are prone to accumulate and form more fluorine clusters during the sequent fabrication process, even worsening the electrical characteristics [4.15-4.16]. Moreover, the fluorine elements were found to be highly volatile in high temperature in the process flow, possibly degrading the electrical characteristics [4.17]. In general, one of possible causes for the improved electrical characteristics of the poly-Si TFTs might be attributed to grain size enhancement. Figure 4-8 illustrates the scanning electron microscopy (SEM) analysis, demonstrating a slight difference in grain size between the standard and the F-ion-implanted poly-Si. Hence, in this work it is confirmed that the improvement in the electrical characteristics of F-ions-implanted poly-Si TFTs are not originated from the grain size enhancement. This study results have demonstrated that both the improvement and degradation of poly-Si TFTs could originate from the inclusion of F, dependent on the dosage of implanted fluorine. In this work, an optimization condition of F implantation dose is obtained with an ion dosage of $5\times10^{13}$ cm$^{-2}$.

## 4.4 Conclusions

The ELC poly-Si TFTs with F-ions-implantation treatment were fabricated and investigated in this study. Significant improvements in electrical performance and reliability have been obtained with fluorine dose of $5\times10^{13}$ cm$^{-2}$. The field effect mobility is increased from 56.65cm$^2$/volt-sec to 103.94cm$^2$/volt-sec and the threshold voltage is decreased from 3.07 V to 1.09 V. However, the performance will be degraded as the F ions dosage increased in poly-Si film. In our proposed method, the fluorine spontaneously segregates at the poly-Si interface without the procedure of an extra oxide layer deposition, reducing the process step as compared to the conventional fabrication of the F-ion implanted poly-Si TFTs. In addition, the proposed technology is compatible with the conventional poly-Si TFTs manufacture process.

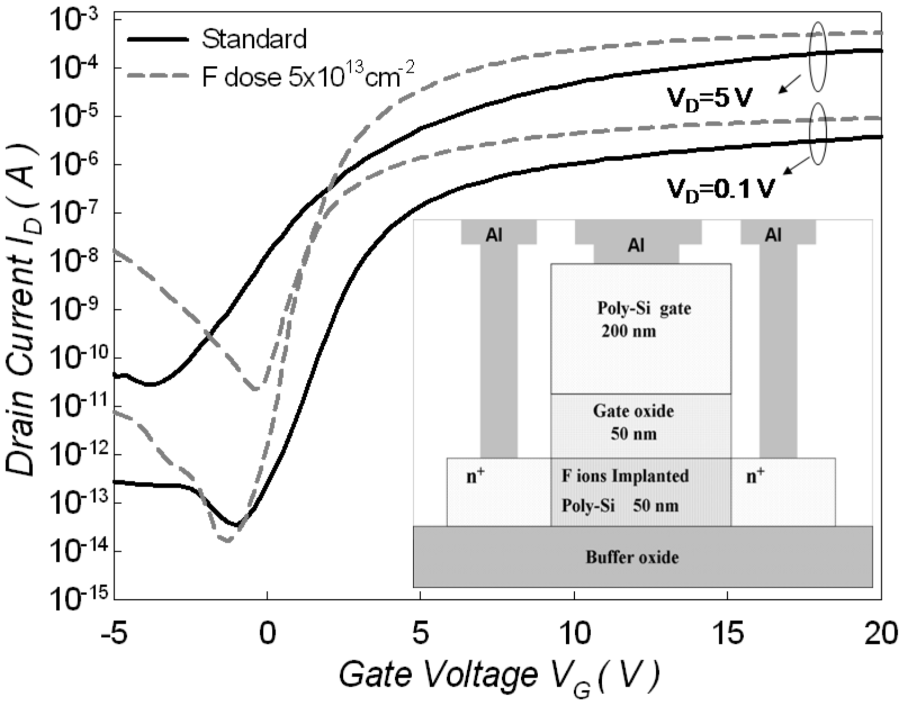


Figure 4-1 The transfer characteristics ($I_D$-$V_G$) of the poly-Si TFTs with F ions implantation dosage of 5×10$^{13}$ cm$^{-2}$, compared to the typically fabricated poly-Si TFTs (marked as Standard). (Insert is the schematic cross-section of the F-ions-implanted poly-Si TFTs structure)

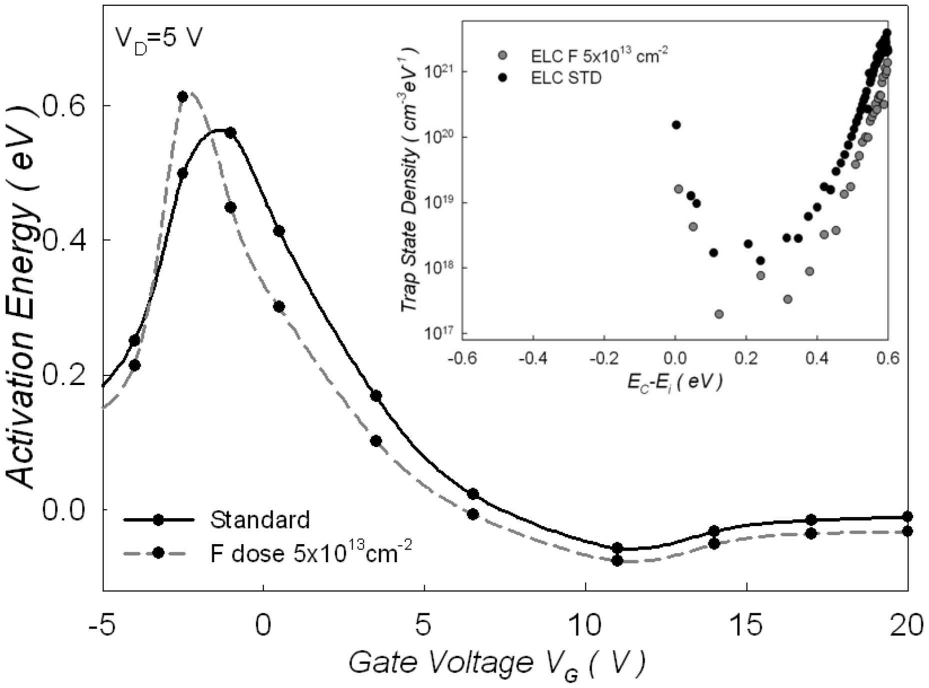


Figure 4-2 The activation energy ($E_A$) of the poly-Si TFTs with and without F ions implantation, as a function of gate voltage. (Drain voltage $V_D$ applied at 5 V). The insert shows the distribution of trap state density in the poly-Si bandgap

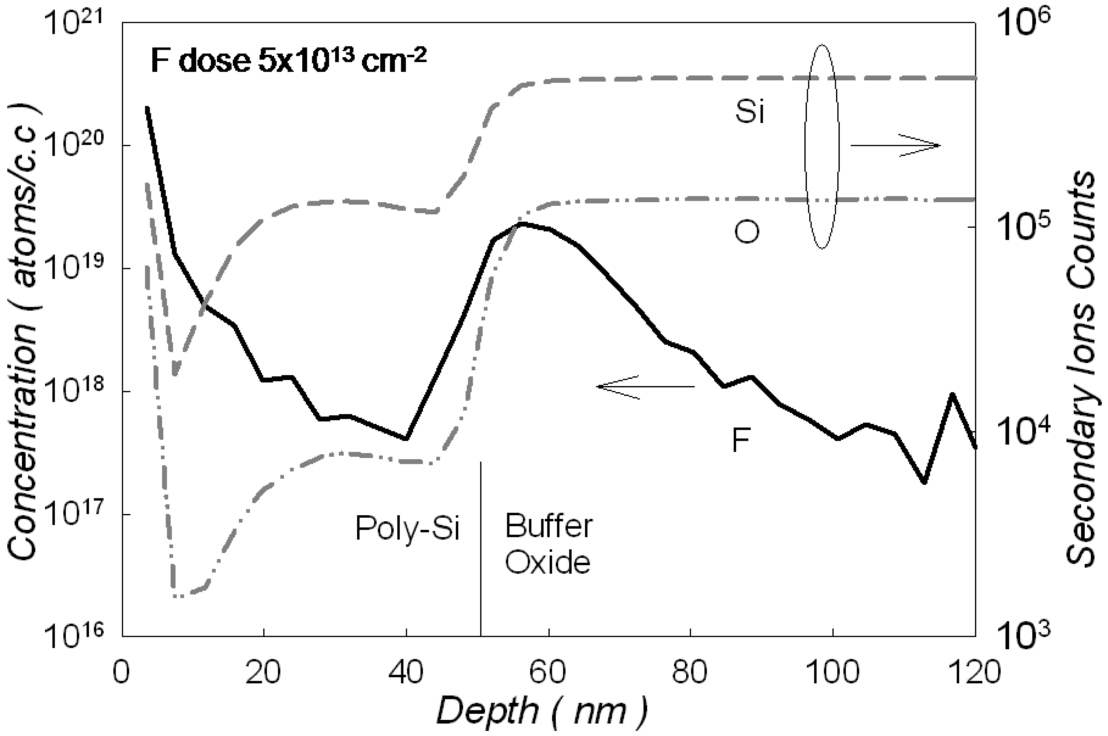


Figure 4-3 Secondary ion mass spectrometer (SIMS) analysis of fluorine in the F-implanted poly-Si film after excimer laser crystallization process

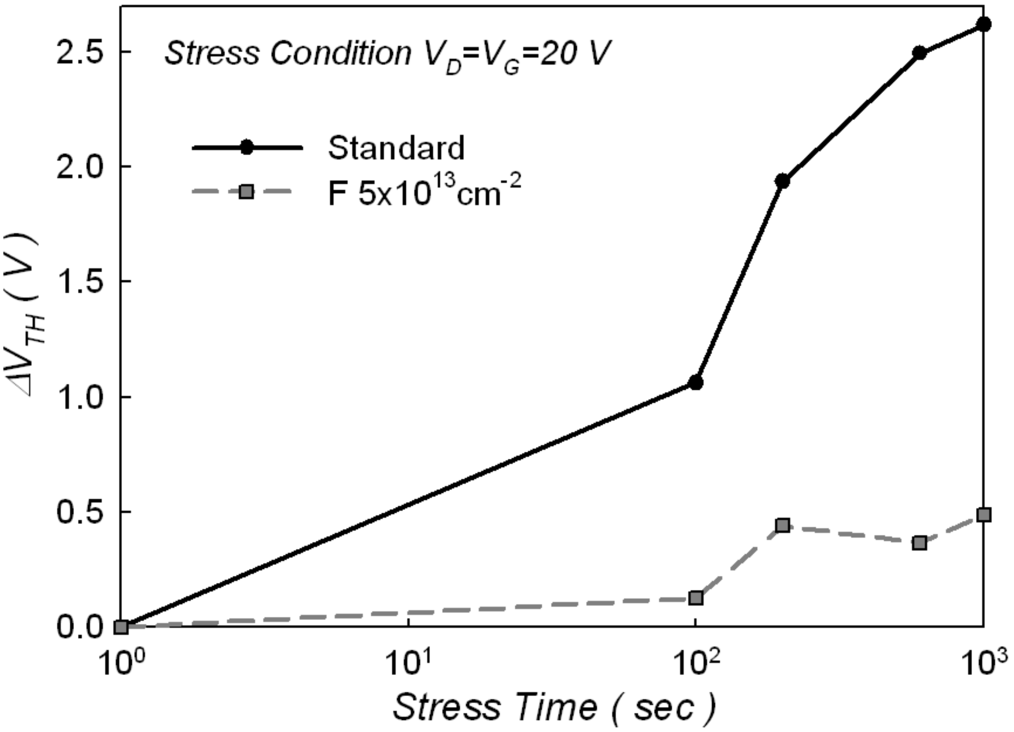


Figure 4-4 The threshold voltage variation ($\Delta V_{TH}$) as a function of stress time, for the standard poly-Si TFTs and F-implanted poly-Si TFTs with ion dosage of $5\times10^{13}$ cm$^{-2}$

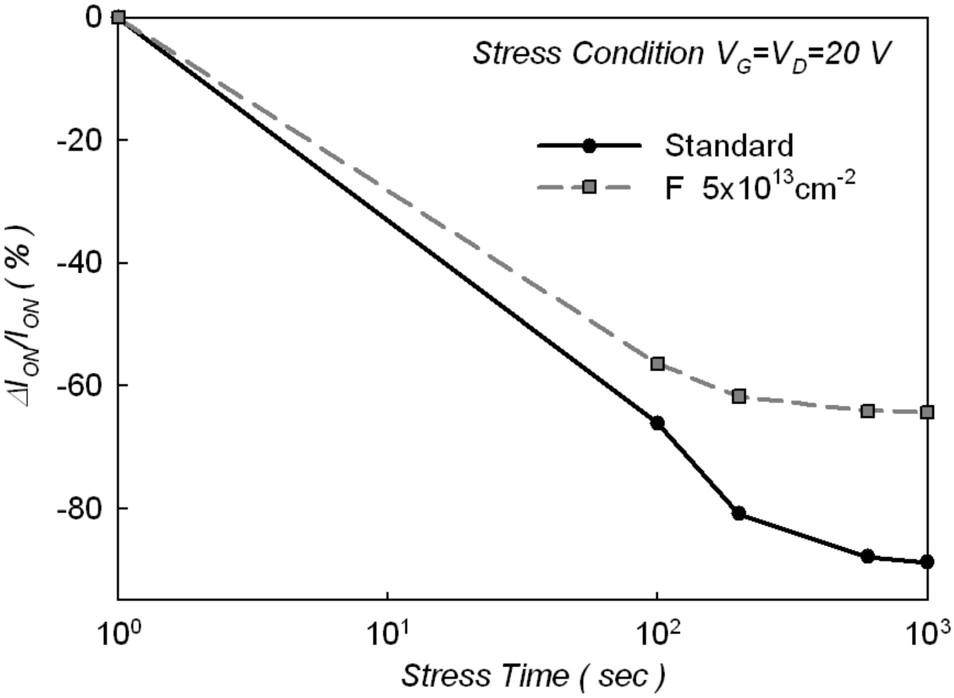


Figure 4-5 The on-current variation ($\Delta I_{ON}/I_{ON}$) as a function of stress time for the standard poly-Si TFTs and F- implanted poly-Si TFTs with ion dosage of $5\times10^{13}$ cm$^{-2}$

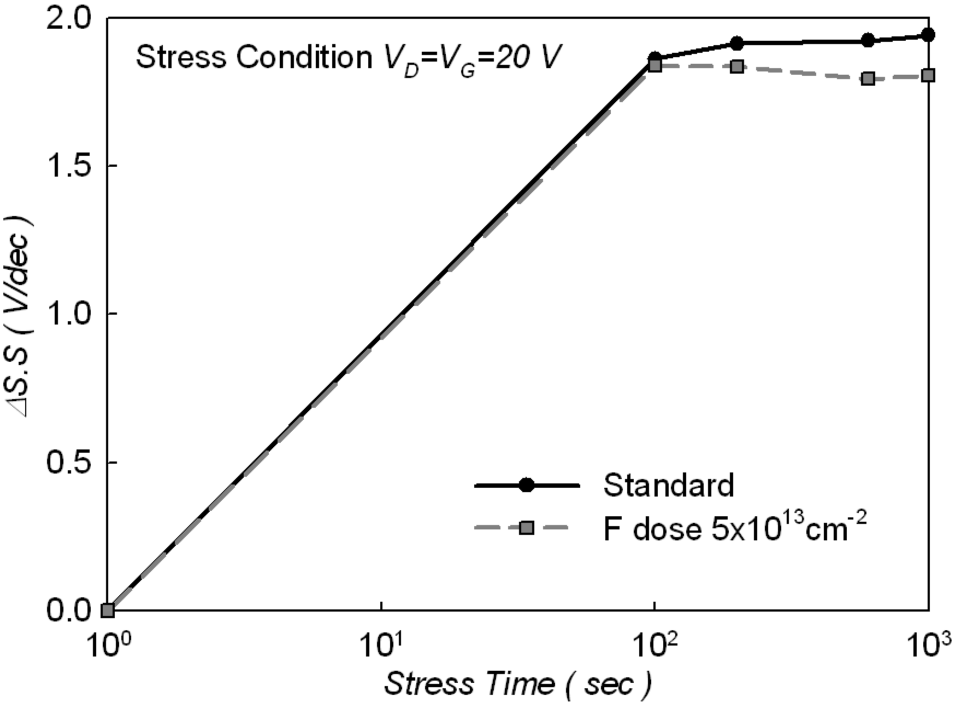
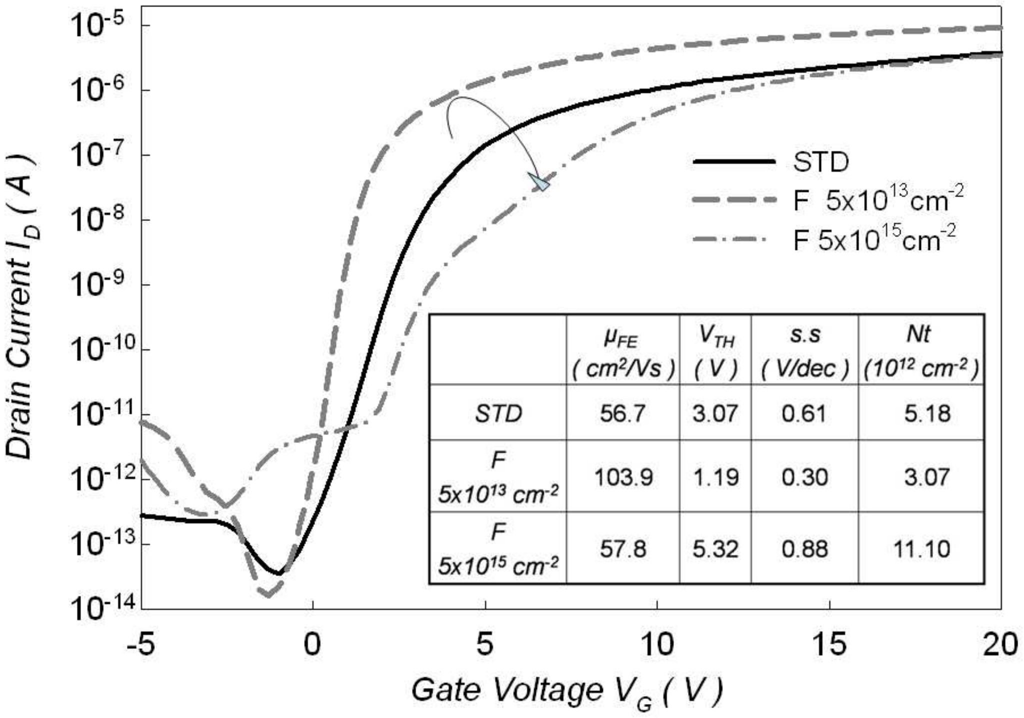


Figure 4-6 The subthreshold swing variation ($\Delta S.S$) as a function of stress time for the standard poly-Si TFTs and F-implanted poly-Si TFTs with ion dosage of $5\times10^{13}$ cm$^{-2}$



| | $\mu_{FE}$ ( $cm^2/Vs$ ) | $V_{TH}$ ( V ) | s.s ( V/dec ) | Nt ( $10^{12}$ $cm^{-2}$ ) |
|---|---|---|---|---|
| STD | 56.7 | 3.07 | 0.61 | 5.18 |
| F $5x10^{13}$ $cm^{-2}$ | 103.9 | 1.19 | 0.30 | 3.07 |
| F $5x10^{15}$ $cm^{-2}$ | 57.8 | 5.32 | 0.88 | 11.10 |

Figure 4-7 The transfer characteristics ($I_D$-$V_G$) for F-implanted poly-Si TFTs with various ion implantation dosages, compared to the standard poly-Si TFTs (Drain voltage $V_D$ applied at 0.1 V)

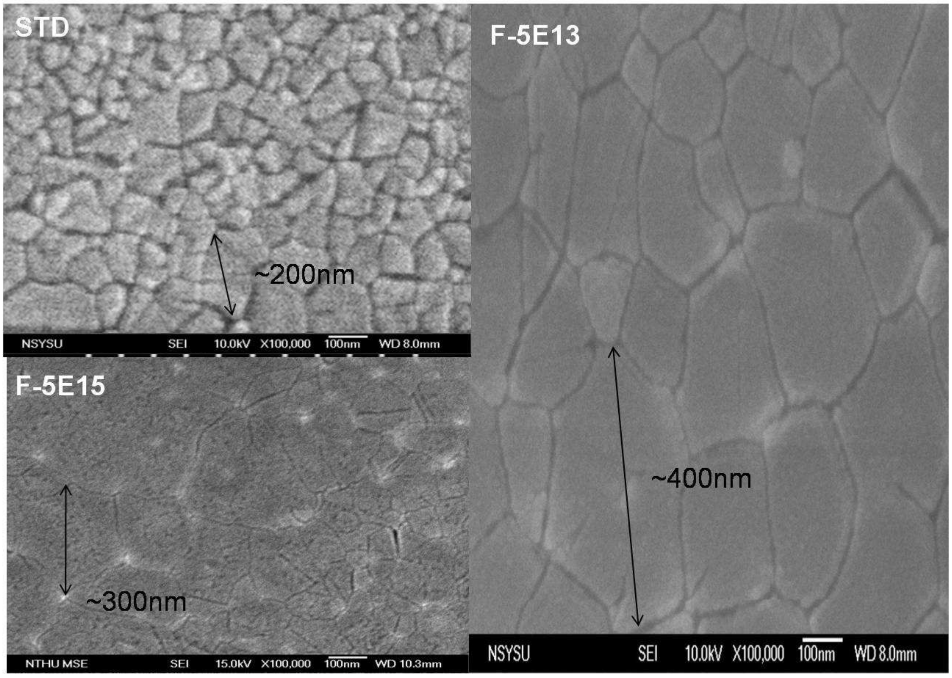


Figure 4-8 Scanning electron microscopy (SEM) images of the standard and the F-implanted poly-Si films

Table 4-1 The key electrical parameters of F-implanted poly-Si TFTs with ion dosage of $5\times10^{13}$ $cm^{-2}$ and $5\times10^{15}$ $cm^{-2}$, compared to the standard poly-Si TFTs

| | $\mu_{FE}$ ( $cm^2/vs$ ) | $V_{TH}$ ( V ) | s.s ( V/dec ) | Nt ( $10^{12}$ $cm^{-2}$ ) |
|---|---|---|---|---|
| STD | 56.65 | 3.07 | 0.61 | 5.18 |
| F <br> $5x10^{13}$ $cm^{-2}$ | 103.94 | 1.19 | 0.30 | 3.07 |
| F <br> $5x10^{15}$ $cm^{-2}$ | 57.83 | 5.32 | 0.88 | 11.10 |

# Chapter 5

# Improved Performance of F-Ions-Implanted Poly-Si Thin Film Transistors using Solid Phase Crystallization and Excimer Laser Crystallization

## 5.1 Introduction

The solid phase crystallization (SPC) and excimer laser crystallization (ELC) methods were widely used to re-crystallize amorphous silicon (a-Si) to poly-Si at low temperature fabrication process. The *SPC* process, requiring 24–48 hrs, is a time consuming procedure, which obviously affects the throughput and thermal budget of fabrication processes [5.1]. Furthermore, the resultant lower field effect mobility will limit the development for *SPC* polycrystalline silicon thin film transistors (poly-Si TFTs) for small grain size. The excimer laser system can create larger grain size and little intra grain defect than using conventional *SPC* method [5.2-5.3]. Furthermore, the laser annealing process is not a high temperature fabrication and a rapid process. Hence, the laser annealing system is generally applied in flat plant display application. However, the difference of thermal expansion coefficient for molten poly-Si and buffer oxide causes serious mechanical stress during the *ELC* process.

The off-state electrical characteristics of poly-Si TFTs are dominated by the trap state density of grain boundary. Based on this issue of poly-Si TFTs, the method for reducing trap state density is applied to enhance the electrical characteristics. The typically used passivation methods are hydrogen plasma treatment and ion implantation [5.4-5.6]. The hydrogen plasma treatment is widely used to passivate trap states at poly-Si grain boundaries to avoid the undesirable leakage current [5.9].

However, it is difficult to control hydrogen concentration precisely in the poly-Si TFTs [5.4]. Also, the Si-H bonds are not strong enough against the hot carrier impact, during high electrical bias operation. One of the promising strategies on the electrical improvement of the poly-Si TFTs was proposed using F ion implantation to eliminate the defects in the grain boundaries [5.5-5.6]. Several proposed F-implantation technologies are summarized as followed. In the initial study, the pad oxide deposition on a-Si layer before crystallization was implemented to cause F ions to pile up at the interfaces between the poly-Si and the oxide to eliminate the strain bonds. Also, F-implanted poly-Si TFTs without pad oxide deposition step were proposed to study in our previous work [5.7-5.8]. The oxidized a-Si film on surface during thermal crystallization provides the driving force for the implanted fluorine elements to segregate on the surfaces. The proposed modified F-implantation passivation technology reduces manufacture process steps, and exhibits high potential for the application on active matrix liquid crystal displays (AMLCDs). The undesirable strain bonds in the interface between poly-Si and $SiO_2$ are passivated by using F ions implantation. Furthermore, the segregated F ions at the interface between poly-Si and buffer oxide eliminated the strain bonds which are generated during rapid excimer laser annealing, leading to the superior electrical characteristics [5.9]. In addition, the strong Si-F bond replaced the weak Si-H and Si-Si bonds, resulting in the superior electrical DC stress reliability compared to standard poly-Si TFTs.

This work investigated the electrical characteristics of F-implanted poly-Si TFTs without the initial deposition of pad oxide before crystallization process. The poly-Si crystallizations were realized by using conventional solid phase crystallization and excimer laser crystallization, respectively. The behavior of F-implanted a-Si during the both the above crystallization steps were discussed. Also, the electrical reliability of poly-Si TFTs using both the crystallization methods were compared in this work.

## 5.2 Experimental

The 50-nm-thick undoped a-Si layer was deposited by decomposition of pure silane ($SiH_4$) on oxide-coated silicon wafer with using low pressure chemical vapor deposition (LPCVD) system at 550℃. Then the F ions were implanted to the a-Si layer without any pad oxide deposited first. The ion implantation conditions were set at an ion accelerating energy of 11 KeV and the doping dosages are $5\times10^{13}$ $cm^{-2}$. The crystallization for F-ions-implanted a-Si and standard a-Si was realized by heating in a furnace at 600℃ for 24 hrs in $N_2$ ambient and excimer laser annealing system, respectively. The *ELC* was realized by a KrF excimer laser system at room temperature in vacuum (~$10^{-3}$ Torr) with laser energy of 300 $mJ/cm^2$. After patterning and etching the active region, the 50-nm-thick tetraethylorthosilicate (TEOS) layer and the 200-nm-thick poly-Si gate were deposited by LPCVD system. The deposition temperature of TEOS oxide layer and poly-Si layer are 700℃ and 575℃, respectively. The $P_{31}^{+}$ ions are used for the source/drain ion implantation after patterning and etching the poly-gate. The ion accelerating energy is 17 KeV and the dosage is $5\times10^{15}$ $cm^{-2}$. The activation was realized by depositing of the TEOS passivation layer using LPCVD system at 700℃ for 3 hrs. The contact holes regions were patterned and etched by a buffer oxide etching (BOE) solution. Finally, the aluminum metallization was performed, followed by 350℃ sintering in the thermal furnace for 30 min. The device cross-section is shown in Figure 5-1(a).

## 5.3 Results and discussion

The behavior of F ions in poly-Si after thermal annealing was investigated in this work. Figure 5-1 (b) and 5-1(c) show the secondary ions mass spectroscope (SIMS) analysis of F ions after SPC and ELC, respectively. It is found that the F ions are piled up at the surface of poly-Si and the interface between poly-Si and buffer oxide. Without pad oxide deposited on a-Si layer, the F ions are segregated to the poly-Si surface during re-crystallization. Hence, it needs no extra thermal annealing step and no additional process steps for the F piling up. In addition, the electrical characteristics of F-ions-implanted poly-Si TFTs are investigated in this study. Figure 5-2 shows the transfer characteristics of poly-Si TFTs for F ions implantation dosages of $5\times10^{13}$ $\text{cm}^{-2}$ and standard poly-Si TFTs. It is clearly found that the electrical characteristics are improved with F-ions-incorporated poly-Si TFTs no matter using SPC method or ELC method. The major parameters including field effect mobility ($\mu_{FE}$), threshold voltage ($V_{TH}$), subthreshold swing (*S.S*), and trap state density (*Nt*) are summarized in the Table 5-1. It is considered that the reduction of trap state density improves the electrical characteristics for the two types of devices. The fluorine effectively passivates the dangling bond, leading to lower trap state density. The threshold voltage ($V_{TH}$) is defined as the gate voltage that yields the drain current ($I_{DS}$) ($I_{DS} = 10\ nA \times W/L$). The threshold voltage is greatly reduced by using F-ions implantation. The poly-Si TFTs with reduced $V_{TH}$ have even more potential for the application on AMLCDs. In addition, the $\mu_{FE}$ is greatly improved in this work. It is found that the $\mu_{FE}$ value for poly-Si using SPC method varies from 19.74$\text{cm}^2$/volt-sec to 54.48$\text{cm}^2$/volt-sec. Furthermore, the $\mu_{FE}$ value of F-ions-implanted poly-Si TFTs (*ELC* method) is approximately two times to those of standard (56.65$\text{cm}^2$/volt-sec to 103.94$\text{cm}^2$/volt-sec).

Fluorine piled up at the poly-Si/buffer-oxide interface, confirmed by SIMS analysis, and passivated the stress-induced strained bonds to form stronger Si-F bonds due to the high electronegativity of F atoms. The reduction of trap states between poly-Si and buffer oxide improves the performance of the poly-Si TFTs, such as $I_{ON}$,

$S.S$, and $I_{OFF}$ [5.9]. Hence, the superior electrical characteristics are attributed to the relaxation of mechanical stress and trap state elimination in poly-Si TFTs, especially for using *ELC* method.

The activation energy ($E_A$) calculation is useful to confirm the fact of trap state density elimination for F-ions-implanted poly-Si TFTs. Figure 5-3 (a) and (b) show the $E_A$ of drain current as a function of gate voltage measured at $V_D$=5V for standard and F-ions-implanted poly-Si TFTs. The activation energy was extracted by the measurement of $I_D$-$V_G$ characteristic in the temperature range from 20℃ to 150℃. From the equation $I_D = I_0 e^{\frac{-Ea}{KT}}$, using the linear fitting of the *ln* ($I_D$) versus the *1/KT* plot, in which *K* is the Boltzmann constant and *T* is the temperature. Then the activation energy can be extracted. The $E_A$ related with the barrier height in the poly-Si channel, expresses the carriers transportability [5.10]. For the F-ions-implanted poly-Si TFTs, the value of $E_A$ extracted from on-state current is reduced, while $E_A$ extracted from the off-state current is increased, indicating that F-ion implantation effectively reduces the trap state density. The $E_A$ of off-state current is increased and the $E_A$ of on-state current is reduced for the F-ions-implanted poly-Si TFTs, indicating that F implantation alters the trap state density. This result is consistent with the above discussion. Furthermore, by calculating the trap states density distribution in the bandgap [5.11], the trap state densities for *SPC* method and *ELC* method, are clear reduced with F ions incorporation are shown in Figure 5-4 (a) and (b), respectively. It is consistent with the result of activation energy as shown in Fig 5-3 (a) and (b). It is believed that the reduced trap states density causes the enhanced electrical characteristics. F-ions-incorporated poly-Si TFTs obtain reduced both the tail states and the deep states. The reduced deep states lead to decreased $V_{TH}$ in n-ch poly-Si TFTs [5.5]. The tail state reduction improves the electrical characteristics such as $S.S$

and $\mu_{FE}$ value, also compatible with our experimental results [5.5].

The study also considered the DC stress reliability for F-ions-implanted poly-Si TFTs. To investigate the device reliability, the poly-Si TFTs were bias stressed at $V_D$=20V and $V_G$=20V for time duration of 100 sec, 200 sec, 600 sec, 1000 sec. Figure 5-5 shows the $\Delta V_{TH}$ values by the *SPC* method and *ELC* method. F-ions-implanted poly-Si TFTs are found to yield more moderate $\Delta V_{TH}$ values than in standard poly-Si TFTs. Furthermore, hot carrier multiplication near the drain side degraded the $V_{TH}$, $I_{ON}$ and *S.S* values. The $I_{ON}$ and *S.S* also reflect the reliability of the proposed TFTs device. Figure 5-6 and 5-7 illustrate the $\Delta I_{ON}$ and *ΔS.S* after DC bias stress and demonstrate the F ions implantation significantly reduce hot-carrier-induced degradation, respectively. Degradation induced by hot carrier stress can be attributed to the generation of gate oxide/poly-Si interface states and/or the Si-Si and/or Si-H weak bonds in the poly-Si channel [5.12-5.13]. The Si dangling bonds are terminated by F ions, and the resulting strong Si-F bonding enhances the endurance to hot carrier impact, thus improving the overall electrical reliability.

The electrical characteristics of poly-Si TFTs using *ELC* method are superior to using *SPC* method for larger grain size and less intra grain defect. However, the hot carrier impact is found to degrade the electrical characteristics. Compared with both crystallization methods, the *ELC* method indeed clearly improves the electrical characteristics, such as the $\mu_{FE}$.. The resultant higher $\mu_{FE}$ causes more serious degradation on electrical properties. In contrast, with F ion implantation the improvement of DC bias stress reliability for *ELC* poly-Si TFTs is distinct. The lower trap state density for F-ions-implanted poly-Si TFTs (*ELC)*, as shown in Table 5-1, dominates the electrical improvement. The passivated Si dangling bonds (Si-F) can resist the hot carrier impact, although higher hot carrier energy can be obtained from

*ELC* poly-Si TFTs with superior $\mu_{FE}$. The *ELC* method clearly improved the electrical characteristics, but degraded the DC stress reliability due to the high carrier field effect mobility. However, the F ions implantation for *ELC* method is more useful to improve the ability to resist the electrical DC stress.

## 5.4 Conclusions

The electrical characteristics of the F-ions-implanted poly-Si TFTs have been investigated in this study. The fluorine ions segregated ($5\times10^{13}\text{cm}^{-2}$) at the poly-Si interfaces by *SPC* and *ELC* processes, which effectively reduces the trap state density to enhance the electrical characteristics. The improvement of threshold voltage for *SPC* and *ELC* with the incorporation of fluorine ions are from 6.24V to 4.78V and 3.07V to 1.19V, respectively. Also, the strong Si-F bonds instead of the Si-H and Si-Si bonds can prevent hot carrier impact near the drain side, and possess superior electrical reliability over typical poly-Si TFTs. These improvements in electrical characteristics indicate the proposed F ions implantation method is suitable for high performance poly-Si TFTs applications in the display fields.

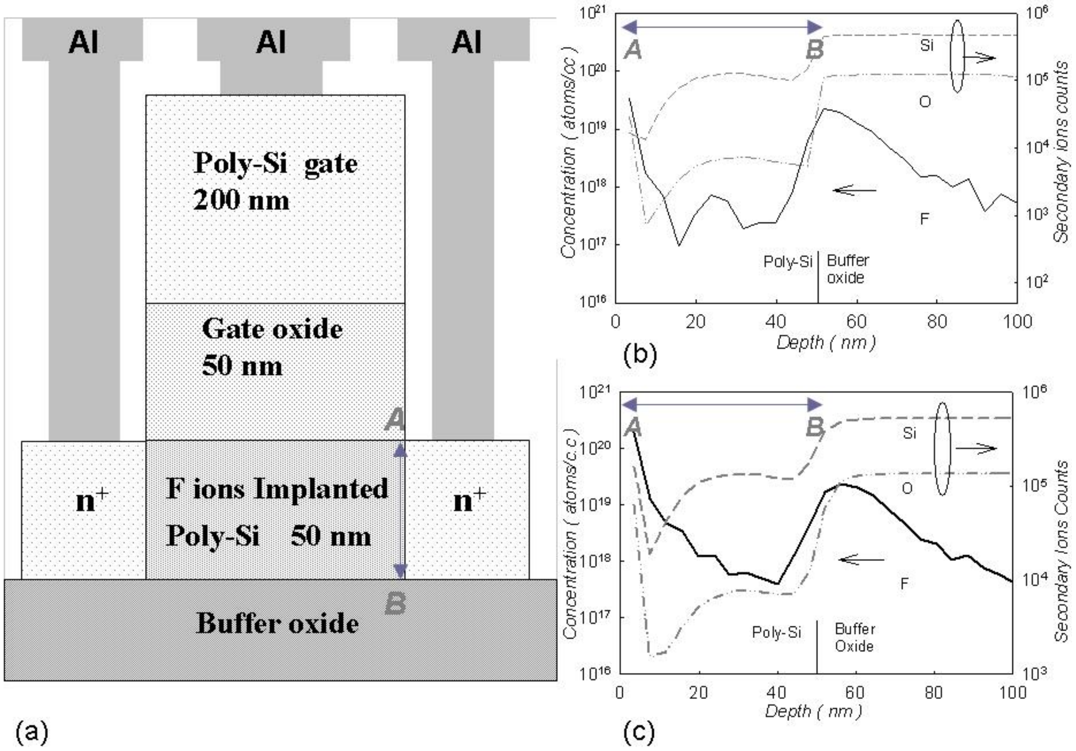


Figure 5-1(a) The cross-section of F-ions incorporated poly-Si TFTs, (b) The secondary ions mass spectroscope (SIMS) analysis of F ions in poly-Si channel after SPC, (c) The secondary ions mass spectroscope (SIMS) analysis of F ions in poly-Si channel after ELC

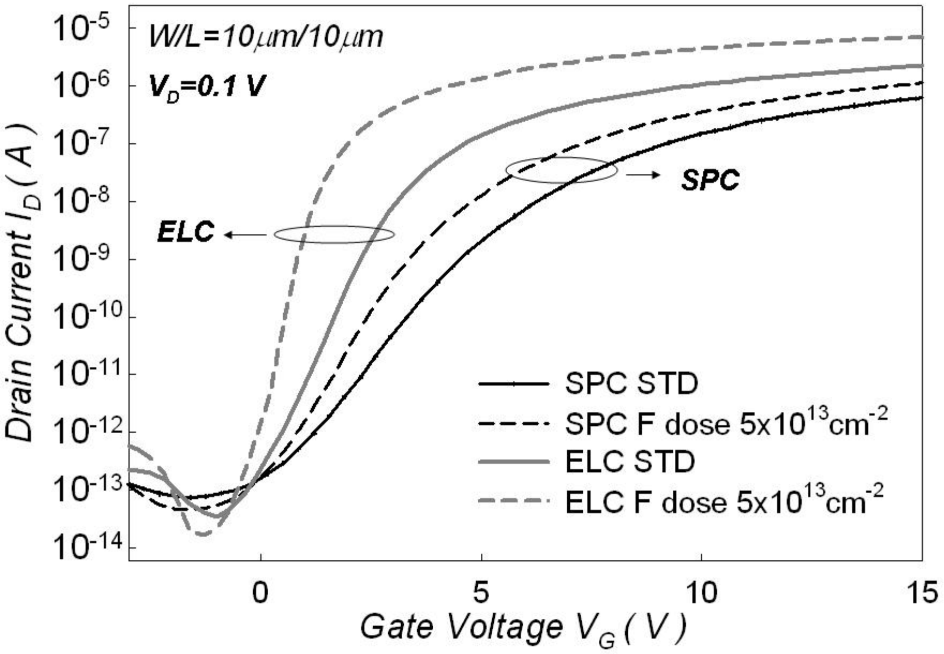


Figure 5-2 The transfer characteristics ($I_D$-$V_G$) of the poly-Si TFTs for F ions implantation dosage of $5\times10^{13}$ cm$^{-2}$ and standard

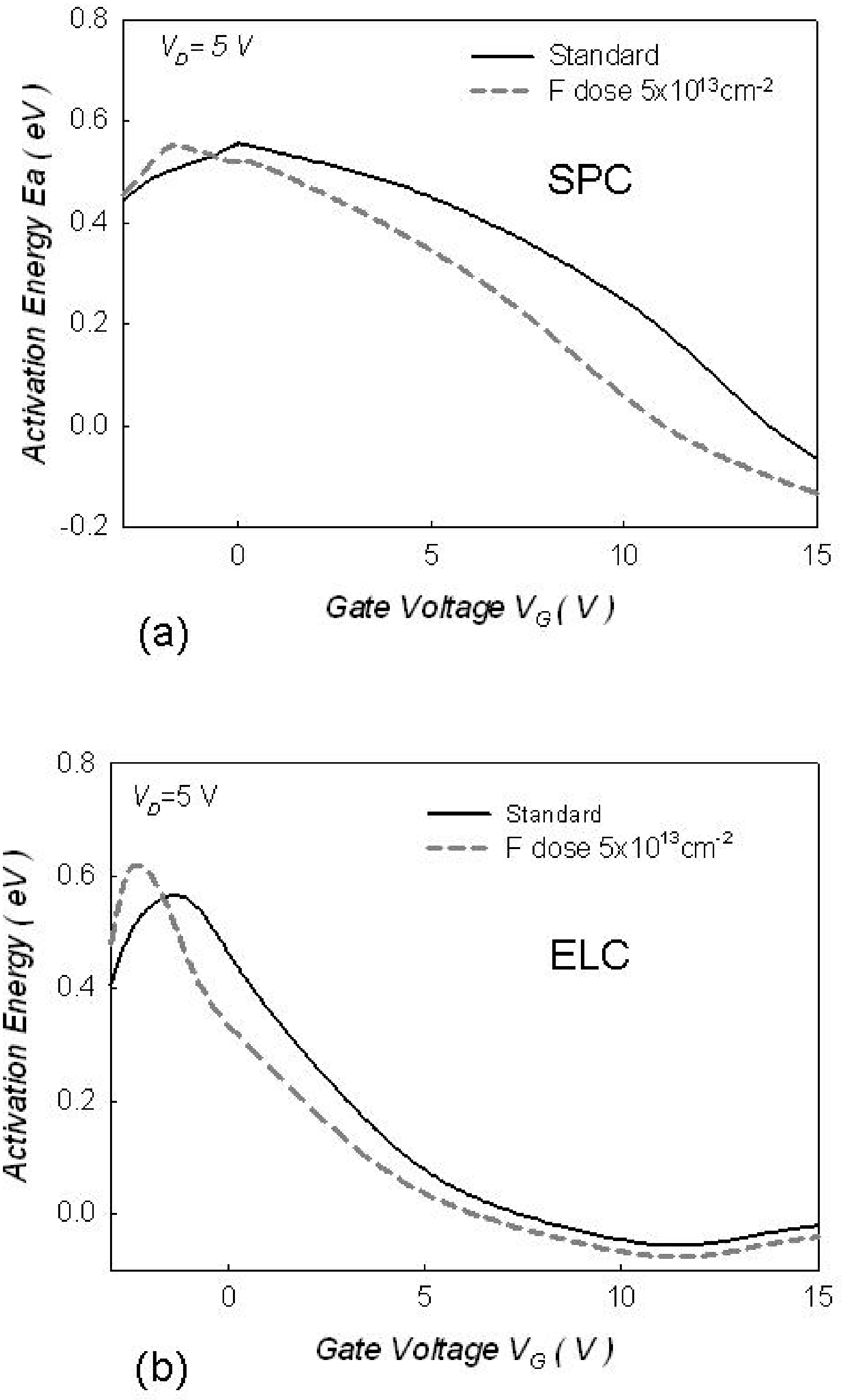


Figure 5-3 (a) The activation energy ($E_A$) of the poly-Si TFTs (SPC) for F ions implantation dosage of $5\times10^{13}$ cm$^{-2}$ and standard at $V_D$=5 V. (b)The activation energy ($E_A$) of the poly-Si TFTs (ELC) for F ions implantation dosage of $5\times10^{13}$ cm$^{-2}$ and standard at $V_D$=5 V

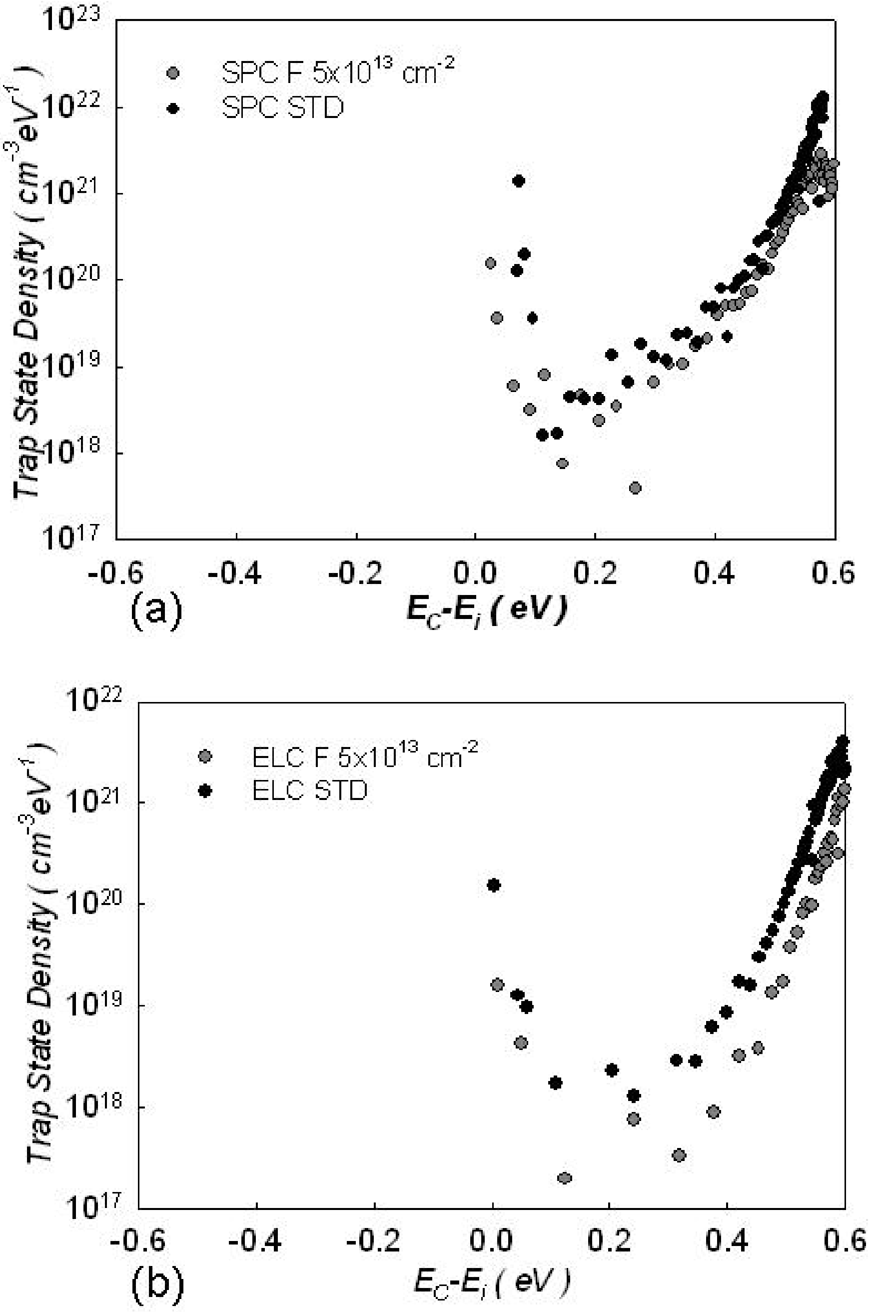


Figure 5-4 (a) The trap state distribution in the bandgap of the poly-Si TFTs (SPC) for F ions implantation dosage of 5×10$^{13}$ cm$^{-2}$. (b) The trap state distribution in the bandgap of the poly-Si TFTs (ELC) for F ions implantation dosage of 5×10$^{13}$ cm$^{-2}$

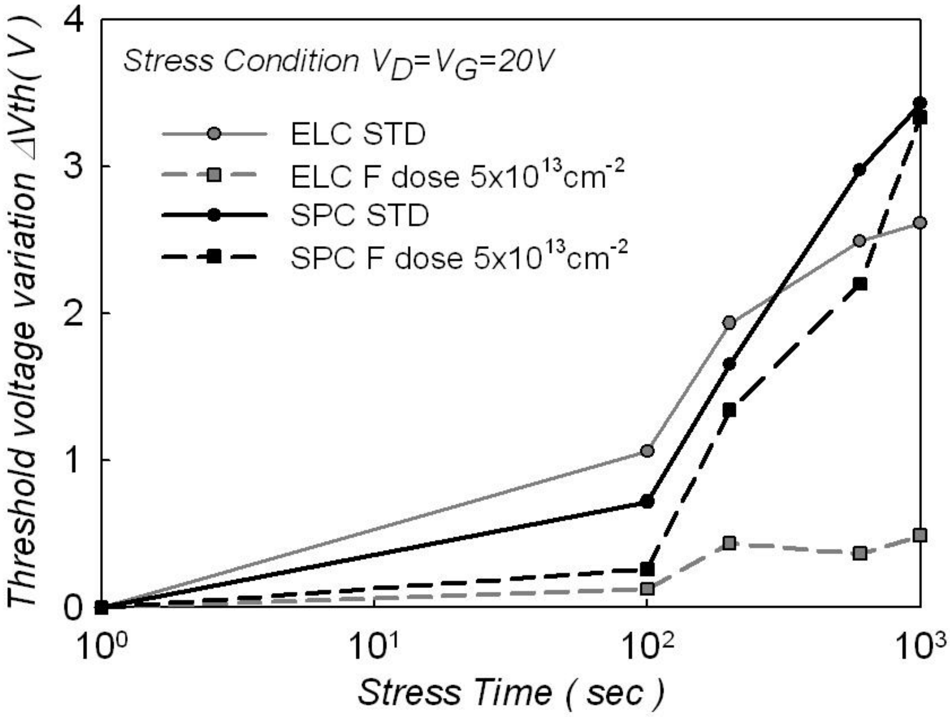


Figure 5-5 The threshold voltage variation ($\Delta V_{TH}$) verse stress time for standard poly-Si TFTs and F-ions-implanted poly-Si TFTs for dosage of $5\times10^{13}$ cm$^{-2}$

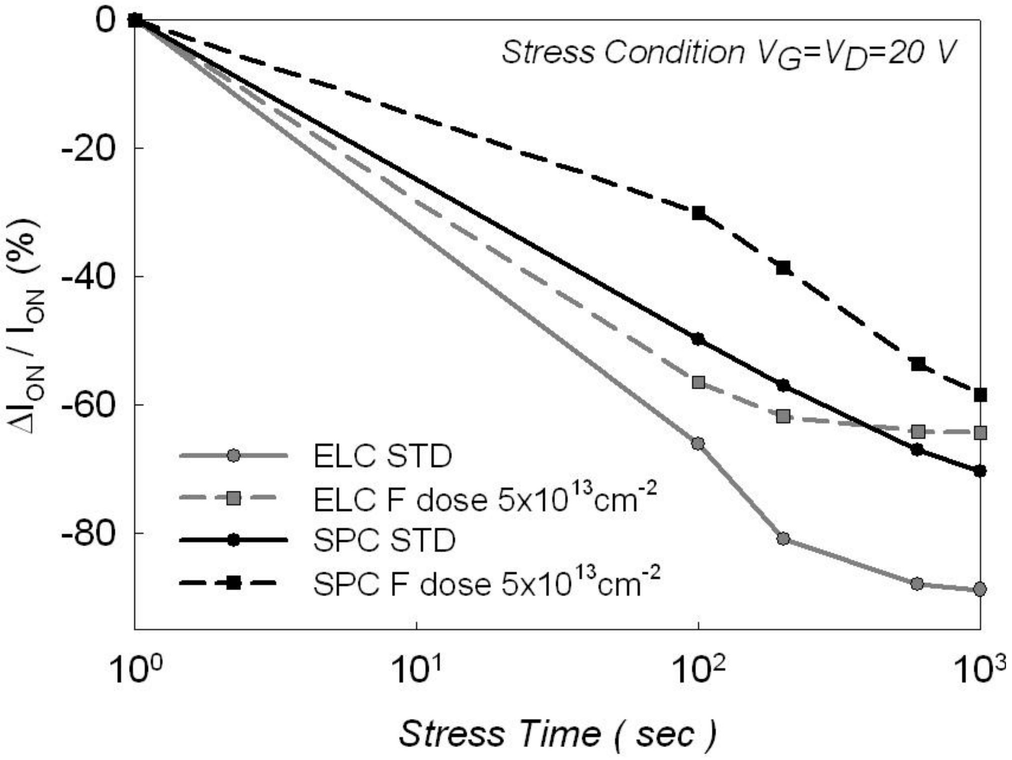


Figure 5-6 The on current variation ($\Delta I_{ON}/I_{ON}$) verse stress time for standard poly-Si TFTs and F-ions-implanted poly-Si TFTs for dosage of $5\times10^{13}$ cm$^{-2}$

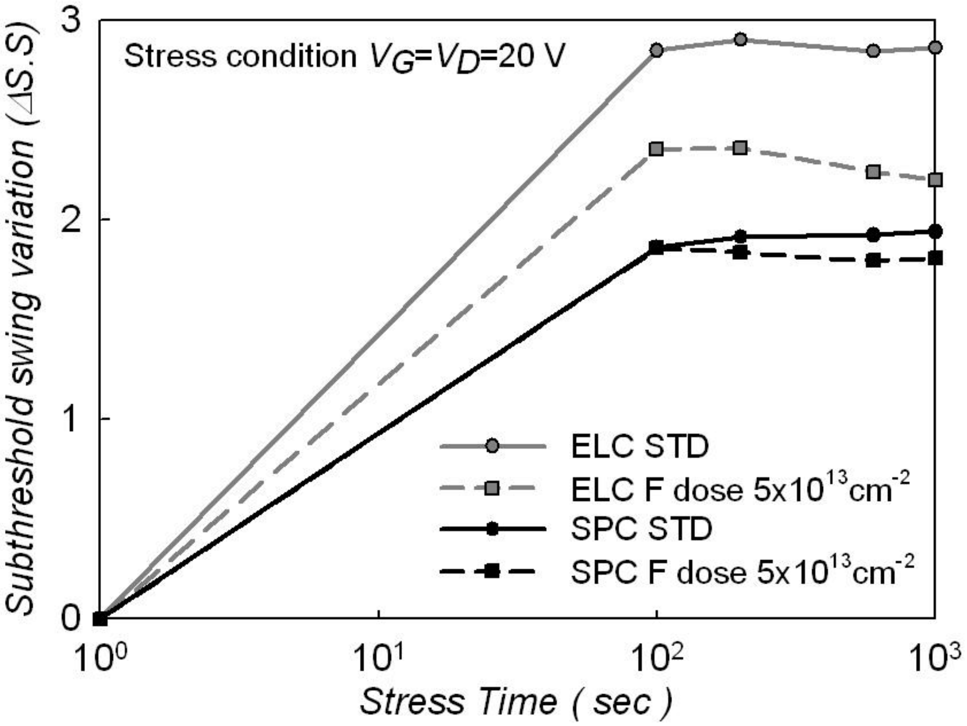


Figure 5-7 The subthreshold swing variation ($\Delta S.S$) verse stress time for standard poly-Si TFTs and F-ions-implanted poly-Si TFTs for dosage of 5×10$^{13}$ cm$^{-2}$

Table 5-1 The parameters of the poly-Si TFTs for F-ions-implanted and standard using SPC method and ELC method

| | | $\mu_{FE}$ ($cm^2/VS$) | $V_{TH}$ (V) | s.s (V/dec) | $I_{ON}/I_{OFF}$ ($10^6$) | $N_t$ ($10^{12}$ $cm^{-2}$) |
|---|---|---|---|---|---|---|
| **STD** | **SPC** | **19.74** | **6.24** | **1.20** | **11.10** | **9.48** |
| | **ELC** | **56.65** | **3.07** | **0.61** | **26.01** | **5.18** |
| **F** <br> **$5x10^{13}cm^{-2}$** | **SPC** | **54.48** | **4.78** | **0.97** | **56.38** | **8.37** |
| | **ELC** | **103.94** | **1.19** | **0.30** | **87.62** | **3.07** |

# Chapter 6

# Improvement of Reliability for Polycrystalline Thin Film Transistors Using Self-aligned Fluorinated Silica Glass (FSG) Spacers

## 6.1 Introduction

Polycrystalline silicon thin film transistors (poly-Si TFTs) are widely used in many applications, including in active matrix liquid phase crystalline displays (AMLCDs) [6.1-6.2]. The high field effect mobility and high on/off current ratio make poly-Si potentially applied for the system integration on panel (SOP) technology. However, the undesirable off-state leakage current makes it unsatisfied for switch device applications. In order to release this issue, lightly doped drain (LDD) structures were proposed to reduce the electrical field near the drain side of poly-Si TFTs. The typical LDD structures are used to form offset regions and oxide spacers to suppress the off current [6.3]. Thus kink effect originated from the hot carrier, due to the maximum lateral electrical field near the drain side, can be reduced further [6.4]. In this work the fluorinated silica glass (FSG) film, instead of typically used $SiO_2$, is proposed as the material of spacers for the first time. In previous studies, the FSG film has been applied in semiconductor manufacture technology, such as passivation layer and gate dielectric film [6.5-6.7]. For the back-end technology application, the incorporation of F ions into the $SiO_2$ can effectively reduce the dielectric constant, decreasing RC time delay in IC interconnection architecture. As the FSG is used as gate dielectric layer in IC technology, it not only improves the Si / $SiO_2$ interface hardness against the hot carrier impact [6.8-6.12], but also has superior breakdown voltage distributions [6.8]. Besides, fluorine can effectively passivate Si dangling bonds, and serves as the fixed charges [6.5]. As result of the F ions at the interface between the gate oxide and the channel, the characteristics of the TFT devices are improved significantly. These previous researches indicated the incorporation of a certain extent of fluorine certainly enhances device reliability of poly-Si TFTs. In this study, the proposed poly-TFTs devices with FSG spacers is thereby expected to exhibit superior electrical reliability than that of counterparts with typically used undoped $SiO_2$ spacers. Electrical performance and reliability of poly-Si TFTs with FSG spacers will be investigated comprehensively in this paper.

## 6.2 Experimental

The self-aligned poly-Si TFTs with FSG spacers were fabricated in this study. The device process flow is described as follows. After initial RCA cleaning procedure, the 500-nm-thick thermally grown $SiO_2$ were formed on Si wafer in the steam oxygen ambient at 1000℃. A 50-nm-thick thin undoped amorphous silicon (a-Si) film was deposited by using low pressure chemical vapor deposition (LPCVD) at 550℃. The amorphous silicon layer was then re-crystallized in a thermal furnace at 600℃ for 24hr under nitrogen ambient. After finishing pattern definition and plasma etching of the active region island, then a 50-nm-thick tetraethylorthosilicate (TEOS) gate oxide was deposited by the LPCVD system. It was followed that 200-nm-thick poly-Si film was deposited as gate electrode and patterned by plasma etching technology. After gate electrode formation, the implantation of phosphorous ions was performed at a dosage of $5x10^{13}$ $cm^{-2}$ and ion acceleration energy of 17 keV. The formation of spacers made of FSG films and TEOS films were implemented in parallel for comparison at a plasma-enhanced chemical vapor deposition (PECVD) system. The FSG films were deposited by adding $CF_4$ gas as fluorine source to TEOS / $O_2$ bases chemistry. In this work the flow rate of $CF_4$ is 600 sccm. After plasma etching back to define the sideward spacer, the source/drain regions were ion implanted by using phosphorous ions at a dosage of $5\times10^{15}cm^{-2}$, and an ion acceleration energy of 17keV. Both types of TFTs with FSG spacers and TEOS oxide spacers were subjected to a rapid thermal anneal (RTA) process at 820℃ for 20sec. The 550-nm-thick TEOS as a passivation layer was deposited by PECVD reactor. The contact holes were wet etched off by buffer oxide etching (BOE) solution. The aluminum layers used as gate and source/drain contact electrodes were deposited by a thermal evaporator and then patterned as the metal pad. Finally, the devices were thermally sintered at 350℃ for 30 min in nitrogen ambient. The device cross-section was shown in Figure 6-1.

## 6.3 Results and discussion

The characteristics for poly-Si TFTs with TEOS spacers and with FSG spacers are discussed as follows. Figure 6-2 shows the Fourier transform infrared (FTIR) spectra of undoped $SiO_2$ and FSG films between 400 $cm^{-1}$ and 2000 $cm^{-1}$. The FTIR spectra were measured from an unpatterned wafer with undoped $SiO_2$ and FSG layer respectively. The main peak of function group Si-F is around 930 $cm^{-1}$. The signal of Si-F bonds is clearly observed in the FSG film. The transfer characteristics of poly-Si TFTs with FSG spacers and TEOS spacers are compared separately as shown in Figure 6-3. It is found both types of poly-Si TFTs have nearly the same transfer characteristics. This indicates the introduction of FSG spacer in poly-Si TFTs device does not degrade electrical performance. Also, the output characteristics of poly-Si TFTs with FSG spacers and with TEOS spacers are shown in Figure 6-4. The threshold voltage ($V_{TH}$) was defined as the gate voltage that yield the drain current ($I_{DS}$) ($I_{DS}$= 10 nA × W/L). The drain current drastically increases with increasing drain voltage while device is operated in the saturation region, especially at high gate voltages. The kink effect in poly-Si TFTs is attributed to channel avalanche multiplication occurred in the high fields near drain side, associated with the floating body effect. The suppression of kink effect for the poly-Si TFTs with FSG spacers is more significant than the TEOS spacer poly-Si TFTs. The fluorine ions in the sideward spacer near drain side strongly passivate the Si dangling bonds to avoid the occurrence of hot carriers. To investigate the device reliability, the poly-Si TFTs were bias stressed at $V_D$=30V and $V_G$=15V for varied time duration, ranging from 100 sec, 200 sec, 600 sec, 1000 sec, 2000 sec, 6000 sec, and 10000 sec. Figure 6-5(a) and 5(b) exhibit that the variation of transfer characteristics ($I_D$-$V_G$) and transconductance ($G_m$) characteristics after DC bias stress for poly-Si TFTs with TEOS spacer and FSG spacer, respectively. Figure 6-6 shows the variation of threshold voltage ($V_{TH}$) for the poly-Si TFTs with FSG and the TEOS spacers after stressing process. Based on these experimental results, it is clearly shown that the $V_{TH}$ of poly-Si TFTs is increased with increasing stress duration, especially for the poly-Si TFTs with TEOS spacers. It is well known that the $V_{TH}$ is strongly dependent on the deep trap states which originate from the dangling bonds in the grain boundaries of the sideward channel [6.13]. Consequently, after stressing the poly-Si TFTs with undoped $SiO_2$ spacer, the density of the deep trap states and tail states are increased in the devices. Comparatively, in the proposed poly-Si TFTs structure with FSG spacers, fluorine ions from the FSG film will passivate Si dangling bonds, and Si-F bonds are more difficult to break under the bias stress. Hence, the TFTs with FSG spacers have less severe electrical degradation. With F-passivated drain side and LDD structure used in this work, the electrical characteristics and reliability of poly-Si TFTs devices can be improved effectively. In particular, the threshold voltage shift in the proposed poly-Si TFTs was reduced from 1.5V down to 0.3V after $10^4$ s stress at $V_D$ = 30V and $V_G$ = 15V, which was attributed to reduced hot carrier effect.

## 6.4 Conclusions

We have proposed and successfully demonstrated the novel poly-Si TFTs device with FSG film as the spacers to enhance the electrical characteristics due to fluorine passivation effect. The poly-Si TFTs with FSG spacers exhibits superior endurance against hot carrier effect, leading to improved electrical reliability and suppressed kink effect than the TFTs with TEOS $SiO_2$ spacer. In addition, the manufacture processes are compatible with the conventional TFTs process. This indicates our proposed poly-Si TFTs with FSG spacers is a promising technology for application in the TFT-LCDs.

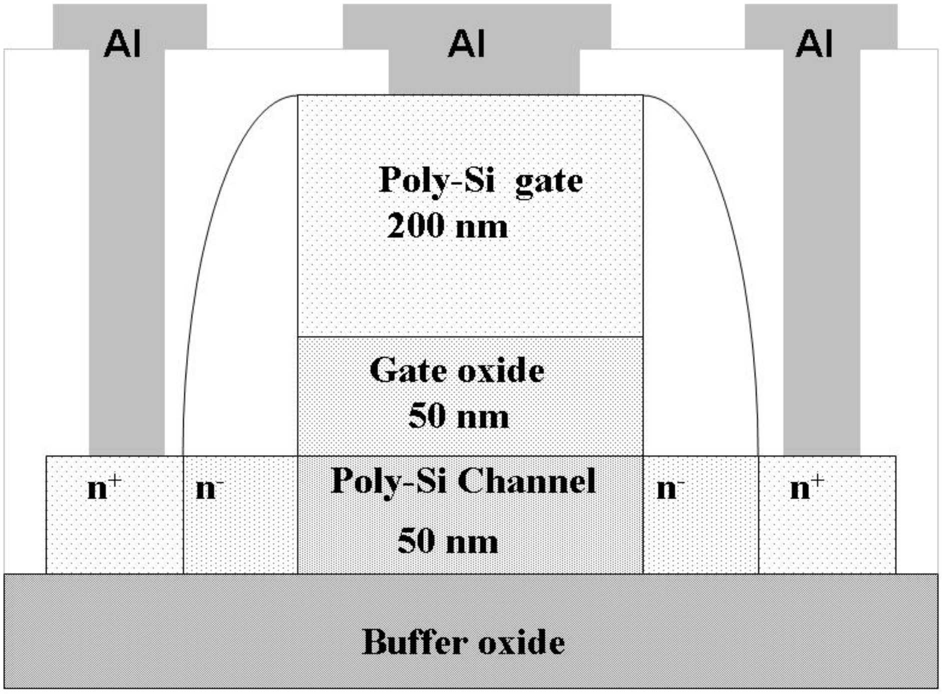


Figure 6-1 The device cross-section for the poly-Si TFTs with all layers

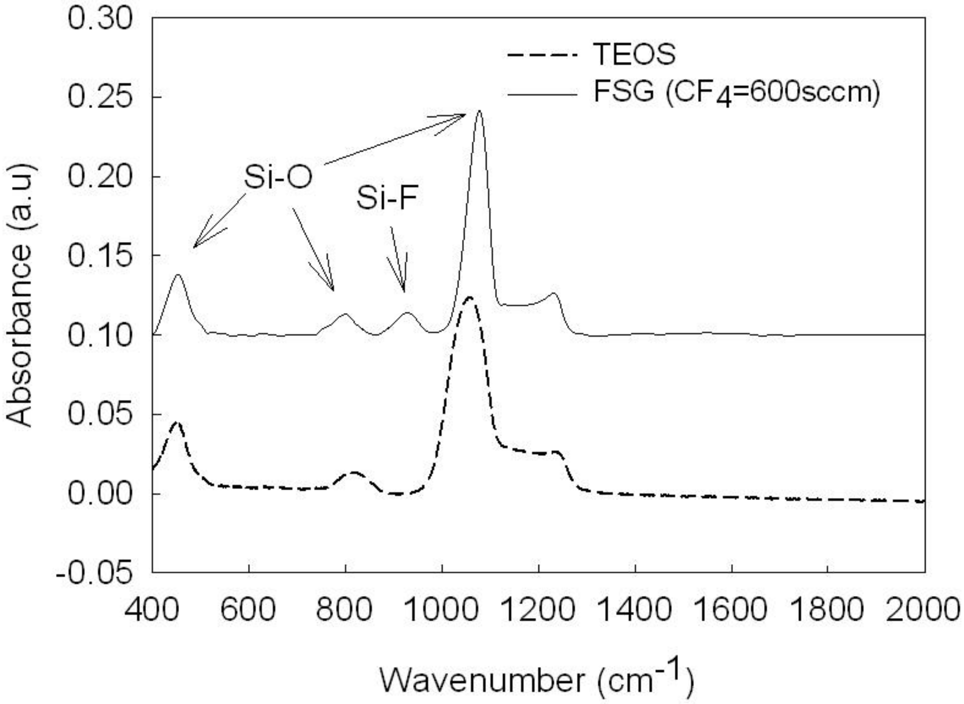


Figure 6-2 Fourier transform infrared (FTIR) spectra of FSG film and TEOS film between 2000 cm$^{-1}$ and 400 cm$^{-1}$

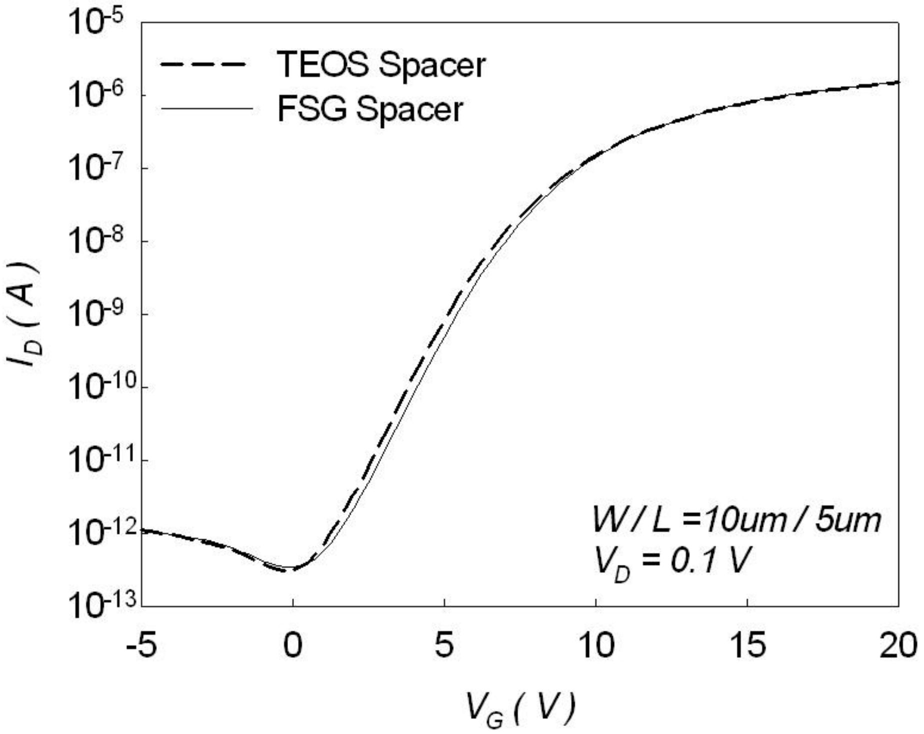


Figure 6-3 Comparison of transfer characteristics ($I_D$-$V_G$) for poly-Si TFTs with FSG spacer and TEOS spacer operated at $V_D$= 0.1 V (W/L =10um/5um)

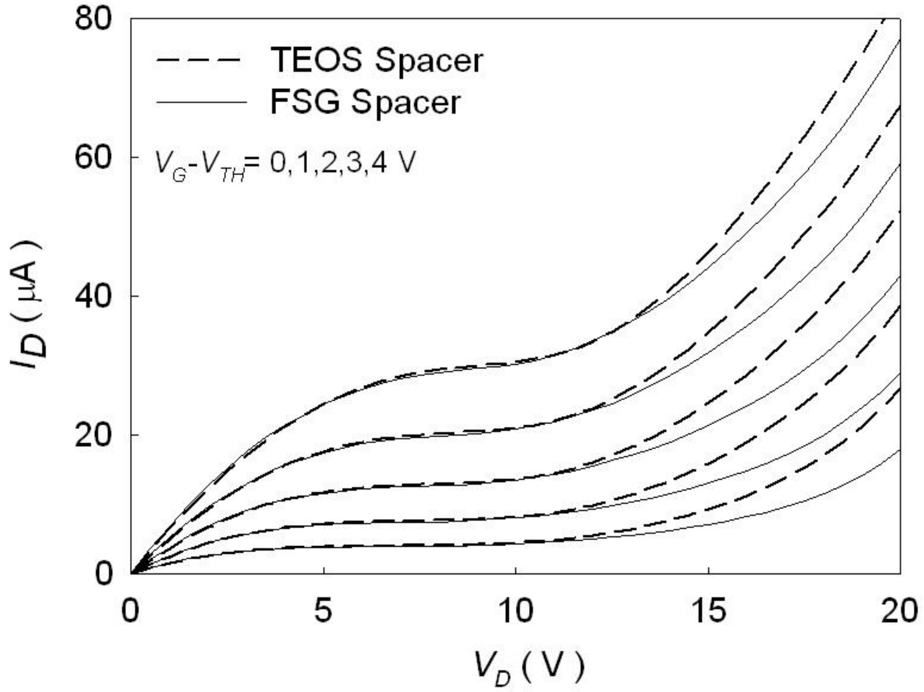


Figure 6-4 Comparison of output characteristics ($I_D$-$V_D$) for poly-Si TFTs with FSG spacer and TEOS spacer, W/L=10um/5um, $V_G$ - $V_{TH}$ = 0, 1, 2, 3, 4 V. The threshold voltages of poly-Si TFTs for FSG spacer and TEOS spacer are 7.61V and 7.29V, respectively

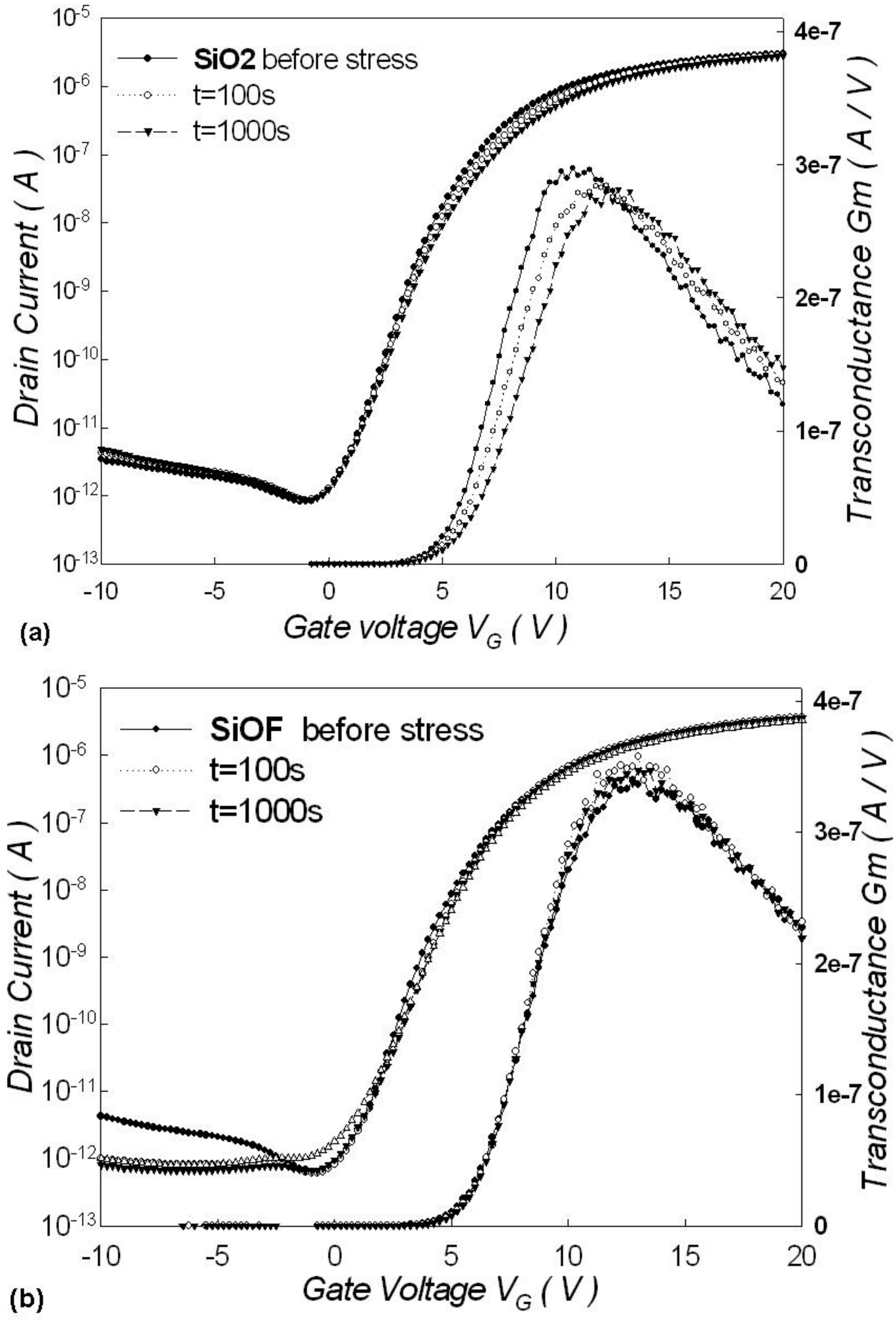


Figure 6-5 The variation of transfer characteristics ($I_D$-$V_G$) and transconductance ($G_m$) characteristics after DC bias stress for poly-Si TFTs with (a)TEOS oxide, and (b)FSG spacers, respectively

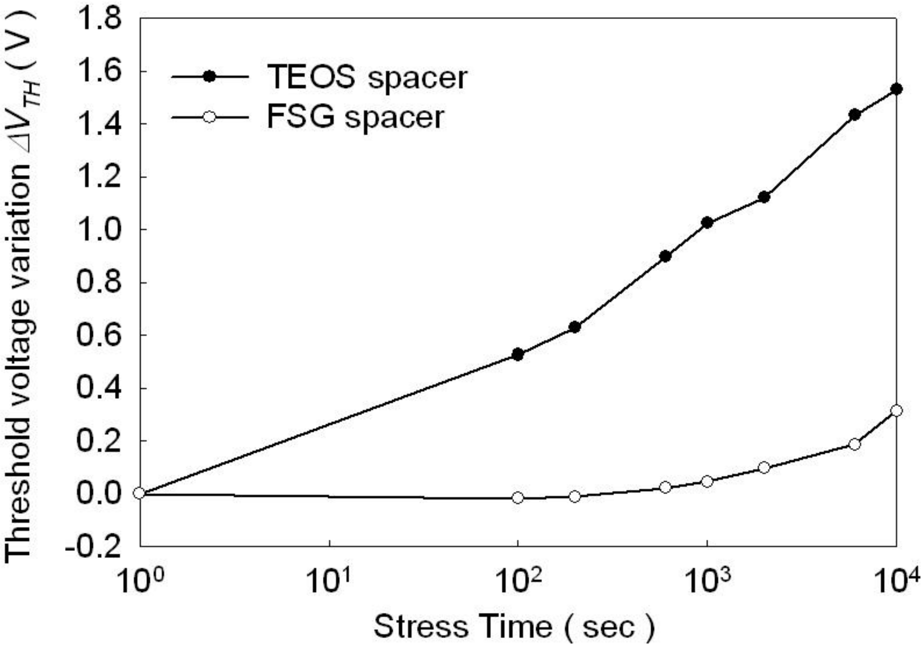


Figure 6-6 Comparison of threshold voltage variation ($\Delta V_{TH}$) characteristics for poly-Si TFTs with FSG spacer and TEOS spacer, operated at $V_D$=0.1V (W/L=10um/3um)

# Chapter 7

# Formation of Germanium Nanocrystals Embedded in Silicon-Oxygen-Nitride Layer

## 7.1 Introduction

In the past few years, the portable electronic devices have significantly impacted the market of consumer electronics. Because of the low working voltage and nonvolatility, the selection of storage media for most portable electronic devices is the Flash memory which almost bases on the structure of the continuous floating gate (FG) [7.1-7.2]. To date, the stacked-gate FG device structure continues to be the most prevailing nonvolatile-memory implementation, and is widely used in both independent and embedded memories. The invention of FG memory impacts more than the replacement of magnetic-core memory, and creates a moment of portable electronic systems. Despite a huge achievement in commercializing, conventional FG devices have some drawbacks [7.2]. The most prominent one is that once there is a charge leakage path (resulting from P/E-cycle degradation) in gate oxide, all the charges stored in the floating gate will leak away from this one single path because charges are stored in continuous energy level (conduction band) in FG. Nanocrystal memories have been presented in the mid-nineties as a possible alternative to conventional FG nonvolatile memory devices, by allowing further decrease in the tunnel oxide. In a nanocrystal nonvolatile memory device, charge is not stored on a continue FG poly-Si layer, but instead on a layer of discrete, mutually isolated, crystalline nanocrystals or dots. Also, the nanocrystal memory device can avoid the charge leakage and lower the power consumption when tunneling oxide is thinner [7.3-7.5]. The self-assembling of silicon or germanium nanocrystals embedded in $SiO_2$

layers has been widely studied, and strong memory effects in MOS devices were reported [7.3, 7.6-7.7]. Recently, different charge storage elements have been studied to achieve the robust distributed charge storage [7.8-7.13]. In this contribution, the germanium-incorporated silicon nitride (SiGeN) was investigated to be a self-assembling layer. The self-assembling layer of SiGeN, fabricated by the directly depositing using plasma enhanced chemical vapor deposition (PECVD) system. The following a-Si was also deposited in one chamber system by using PECVD. The sequent thermal oxidation was performed in thermal furnace at 900℃ to form blocking oxide layer and nucleate Ge nanocrystals for with and without a-Si layer capped SiGeN stacked structure. The structure with Ge embedded SiON layer exhibits obvious charge-trapping memory effects under electrical measurements. Also, material analysis techniques such as Raman spectroscopy and transmission electron microscopy (TEM) were utilized to observe the Ge nanocrystals nucleation in the oxidized SiGeN film.

## 7.2 Experimental

Figure 7-1 (a) and (b) exhibit the process flows in this work. First, a 5-nm-thick thermal oxide was grown as the tunnel oxide on p-type Si substrate by dry oxidation in an atmospheric pressure chemical vapor deposition (APCVD) furnace. Subsequently, a 20-nm amorphous silicon germanium nitride layer was deposited by plasma enhanced chemical vapor deposition (PECVD) on the tunnel oxide, followed by deposition of 20-nm amorphous silicon. In addition, the stacked structure with thicker SiGeN layer was also prepared on tunnel oxide without any a-Si layer deposition. The oxidation process was performed to fabricate the oxygen-incorporated $SiO_2$ or SiON served as blocking oxide, and the oxidation temperature was 900℃. Furthermore, the SiGeN layer is also oxidized to nucleate the Ge nanocrystals during the blocking oxide formation. Afterward, a steam densification at 900℃ was also performed for 180 sec to densify the blocking oxide. The deposition of the SiGeN film was kept at 200℃ in a low pressure of 0.6 mTorr with precursors of $SiH_4$ (20 sccm), $GeH_4$ (5 sccm), $NH_3$ (30 sccm) and $N_2$ (500 sccm) and plasma power of 20 W. The low pressure of 0.6 mTorr during deposition leads the mean free path of electrons to be increased and to improve the uniformity of the thin film. The deposition conditions of a-Si film, such as temperature and pressure, were the same as that of the SiGeN film deposition. Next, the high temperature thermal oxidation was performed in the thermal furnace in oxygen ambient. The sequent steam oxidation was performed to improve the quality of oxidized a-Si layer or oxidized SiGeN as the blocking oxide. Finally, the Al gate was patterned and sintered to form a metal-oxide-insulator-oxide-silicon (MOIOS) structure with the insulator combined the Ge nanocrystals.

## 7.3 Results and discussion

The Ge nanocrystals embedded SiON layer of a MOIOS memory device is utilized to capture the injected carriers from the channel, which causes a variation in the threshold voltage of the memory device. Figure 7-2 (a) and (b) show the capacitance-voltage (*C-V*) hysteresis and the current-voltage (*I-V*) characteristics of the MOIOS structure, respectively. The electrical *C-V* measurements were performed by bidirectional voltage sweeping. The sweeping conditions were split as follows, (I) operated from 10V to -10 V, and reversely, (II) from 3V to -3V and reversely. It is clearly shown in Fig. 7-2 (a) that the threshold-voltage shift (memory window, $\Delta V_{TH}$) of the MOIOS structure is prominent for 900℃ oxidation. In addition, Figure 8-3 (a) shows the capacitance-voltage (*C-V*) hysteresis of the MOIOS structure. The electrical *C-V* measurements were performed by bidirectional voltage sweeping. The sweeping condition was operated from (I) operated from 3V to -3 V, and reversely, (II) from 5V to -5V and reversely, (III) from 7V to -7V and reversely. It is clearly shown in Fig. 8-2 (a) that the threshold-voltage shift (memory window, $\Delta V_{TH}$) of the MOIOS structure is also prominent for 900℃ oxidation. When the device is programmed, the electrons directly tunnel from the Si substrate through the tunnel oxide, and are trapped in the forbidden gap of Ge nanocrystals in the SiON layer. For the erasion, the holes may tunnel from the valence band of the Si substrate and recombine with the electrons trapped in the Ge nanocrystals in SiON layer. The stacked structure with Ge nanocrsystals in the dielectric layer was used for the application of memory. The charge trap centers are believed to be resulted from the (a) interface states between the silicon substrate, (b) traps inside the dielectric layer, (c) nanocrystal confined state, and (d) interface states between nanocrystals and the surrounding dielectric [7-13]. The blocking oxide is utilized to prevent the carriers of gate electrode from injecting into the charge-trapping layer by Fowler-Nordheim (*F-N*) tunneling. The threshold-voltage shift after the 10-V programming operation is 4 V for the Ge nanocrystals embedded in SiON memory device with a-Si layer layer oxidized at 900℃. The 4 V of threshold voltage shift was obtained under 7 V program operation for thicker stacked SiGeN layer as shown in Figure 7-3(a). The large threshold voltage shift of memory device with oxidized a-Si film and oxidized SiGeN layer as blocking oxide layer is attributed to the presence of Ge nanocrystals in the SiON film. When electrons are captured in the Ge nanocrystals of the SiON film, a large threshold voltage shift is shown for a memory device. The leakage current in the MOIOS structure is as shown in Fig. 7-2(b) and 7-3(b). It is tolerate for MOIOS structure with Ge nanocrystals embedded SiON layer to avoid the storaged charge leaking to gate.

Raman spectra of the SiGeN stack film with and without a-Si deposition followed by an oxidation process are schematically shown in Figure 7-4(a) and 7-4(b), respectively. The crystalline phase for Ge is not found for as-deposited SiGeN layer using PECVD system. However, the Ge-Ge bonds are present in the SiGeN film after thermal oxidation. As result of the Si easily combine with oxygen first to form $SiO_2$ [7-14], the Ge will be nucleated after the thermal oxidation. The signal of Ge-Ge bonding is clearly found after the thermal oxidation, as shown in Fig. 7-4(a) and 7-4(b). The Ge nanocrystals in SiGeN layer are self-assembling after high temperature thermal oxidation. The nucleated Ge nanocrystals for are as shown in the Figure 7-5(a) and (b). Fig. 7-5(a) shows the Ge nanocrystals are nucleated at the surface of tunnel oxide for the SiGeN stacked structure with a-Si layer deposition. However, Fig.7-5(b) is the TEM analysis the thicker stacked SiGeN layer after thermal oxidation. Hence, the memory windows were formed after programmed for the oxidized proposed material SiGeN in this experiment. For the $SiO_2$ originated from oxidized a-Si film, there are dangling bonds or defects exist in the bulk and at the interface between SiGeN and $SiO_2$ layer. The electrons trapped near the channel will dominate the threshold voltage significantly than those far from the channel.

The reliability characteristics, such as the retention time and endurance, were also discussed in this study. The charge retention time in the MOIOS structure (oxidized a-Si as blocking oxide) is as shown in Figure 7-6(a). An obvious difference of memory window can be maintained after $10^4$ sec. However, the little degradation in low-$V_{TH}$ state can be attributed to the effect of hole trap states close to valence band of Ge nanocrystal [7-13, 7-15]. In addition, the endurance characteristics for program and erase are as shown in Figure 7-6(b). The obvious memory window can be kept after $10^6$ program/erase cycles. However, the threshold voltages for program and erase operation both shift to negative voltage, even if the memory window can be distinguished. It is considered that the positive oxide trapped charges causes the negative voltage shift. The program and erase curves in Fig. 7 shift to negative voltage at the same time because positive oxide trapped charges are created during the program/erase cycles in both tunnel oxide and the SiOx [7.16]. The positive trapped charges in SiON (partially oxidized as SiOx) will increase with the P/E cycles for the worse quality than tunnel oxide. Therefore, the threshold voltage in the Fig. 7-6(b) will shift to negative side. The obvious memory effect and good reliability can be obtained in the MOIOS structure with oxidized SiGeN as charge trapping layer.

In Figure 7-7(a), the threshold voltage shift for the MOIOS structure (oxidized SiGeN as blocking oxide) is measured with different periods of time at room temperature. It is found that the SiON stack with Ge nanocrystals retains a good retention property without a significant decline of the memory window, which is robust in the Flash nonvolatile memory technology. Figure 7-7(b) exhibits the endurance characteristics, after different write/erase cycles of the Ge nanocrystal embedded SiON layer memory device. The write and erase voltage is 3 and (-3) V, respectively. The memory windows are hardly the same until $10^6$ W/E cycles of operation performed. Even after $10^6$ cycles of pulse operation, it retains a large memory window of ~3.8 V without catastrophic decline as previous reports on nanocrystal memory devices [7.3-7.4]. This certainly demonstrates the rugged nature of the Ge nanocrystal memory device with the suitability for nonvolatile memory devices. The proposed Ge nanocrystals embedded in SiON stack layer with high-temperature oxidized a-Si layer and oxidized SiGeN layer, therefore, contributes both larger memory window and the additional blocking oxide deposition for the nonvolatile memory application promisingly.

## 7.4 Conclusions

In conclusion, the ease technology to form Ge nanocrystals embedded SiON stack film with both distributed storage elements and upside blocking oxide has been demonstrated for memory application. The memory windows after programming were resulted from the Ge nanocrystals embedded in SiON layer. The exhibition of memory windows after programming is resulted from the formation of Ge nanocrystals in SiON layer. The material of SiGeN severed as self-assembling layer was proposed and performed in this study.

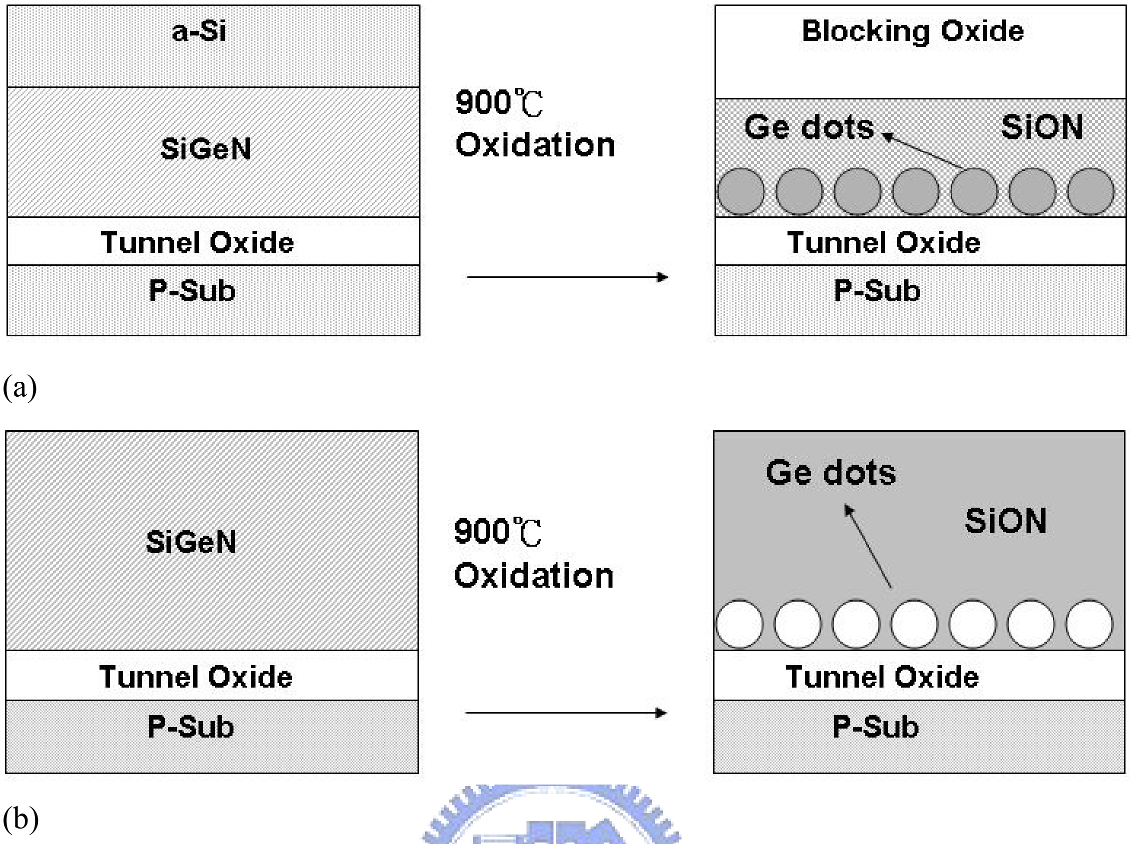


Figure 7-1 The process flow proposed in this work. (a) Oxidized a-Si layer as blocking oxide, (b) Directly oxidized SiGeN layer as locking oxide

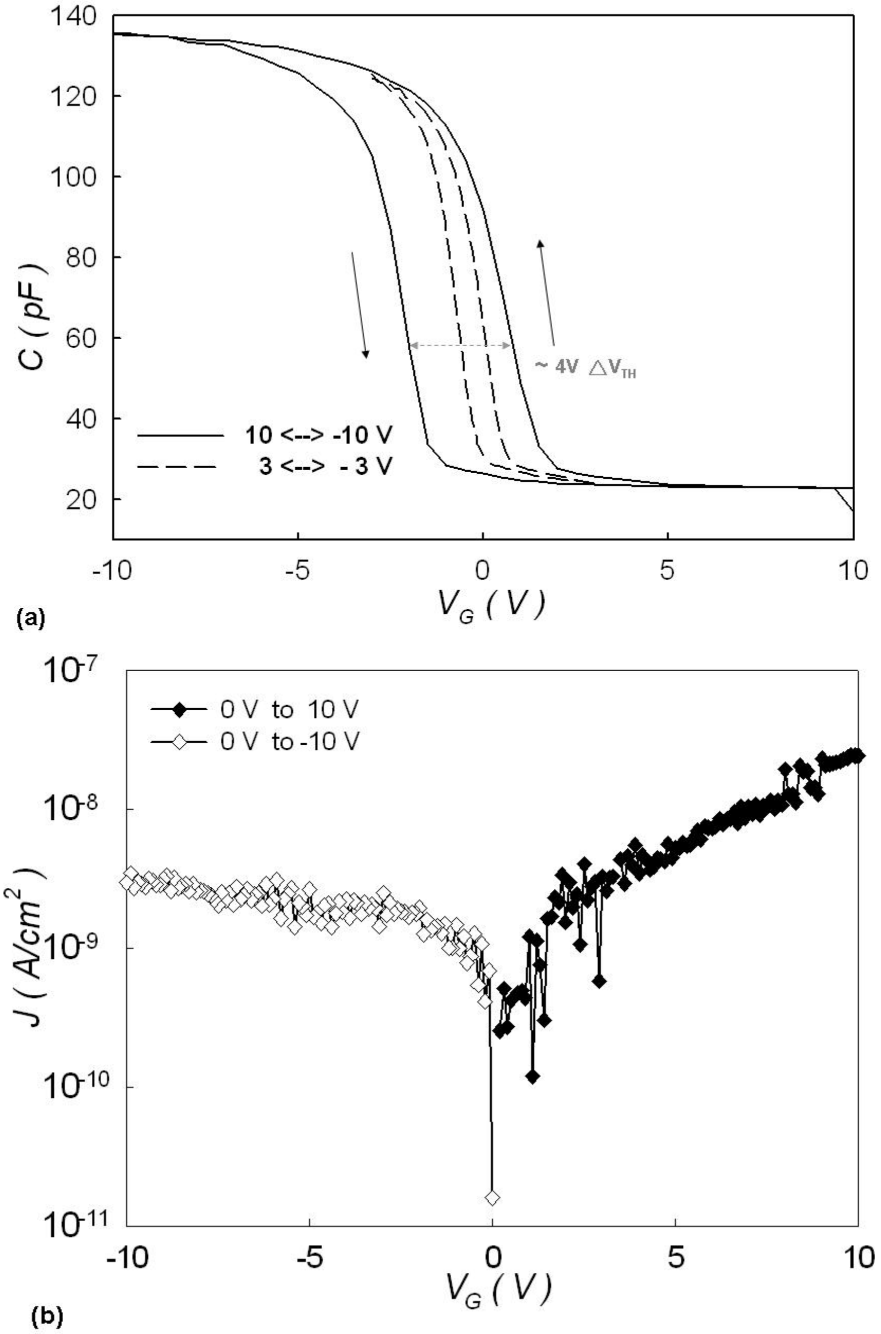


Figure 7-2 (a) The capacitance-voltage (*C-V*) hysteresis of the MOIOS structure. The electrical *C-V* measurements are performed by bidirectional voltage sweeping (1) from 10V~(-10) V and (-10)V~10V ;(2) from 3V~(-3)V and (-3)V~3V: (b)The current density measurement by voltage sweeping from (1) 0V ~ 10V and (2) 0V~ (-10)V

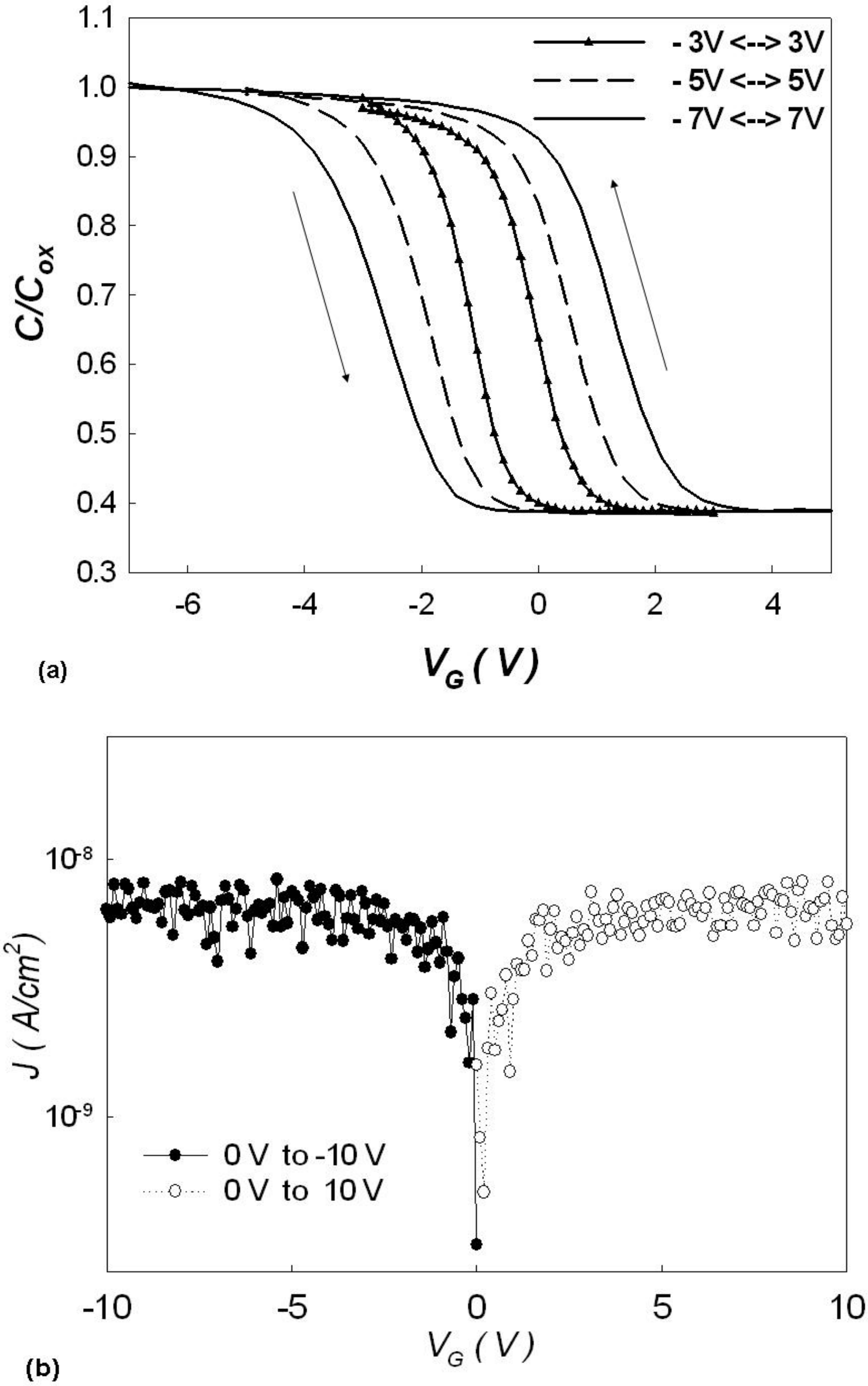


Figure 7-3 (a) The capacitance-voltage (*C-V*) hysteresis of the MOIOS structure. The electrical *C-V* measurements are performed by bidirectional voltage sweeping from(I) 3V~(-3)V and (-3)V~3V, (II) 5V~(-5)V and (-5)V~5V, (III) 7V~(-7)V and (-7)V~ 7V, (b)The current density measurement by voltage sweeping from (1) 0V~10V and (2) 0V~(-10)V

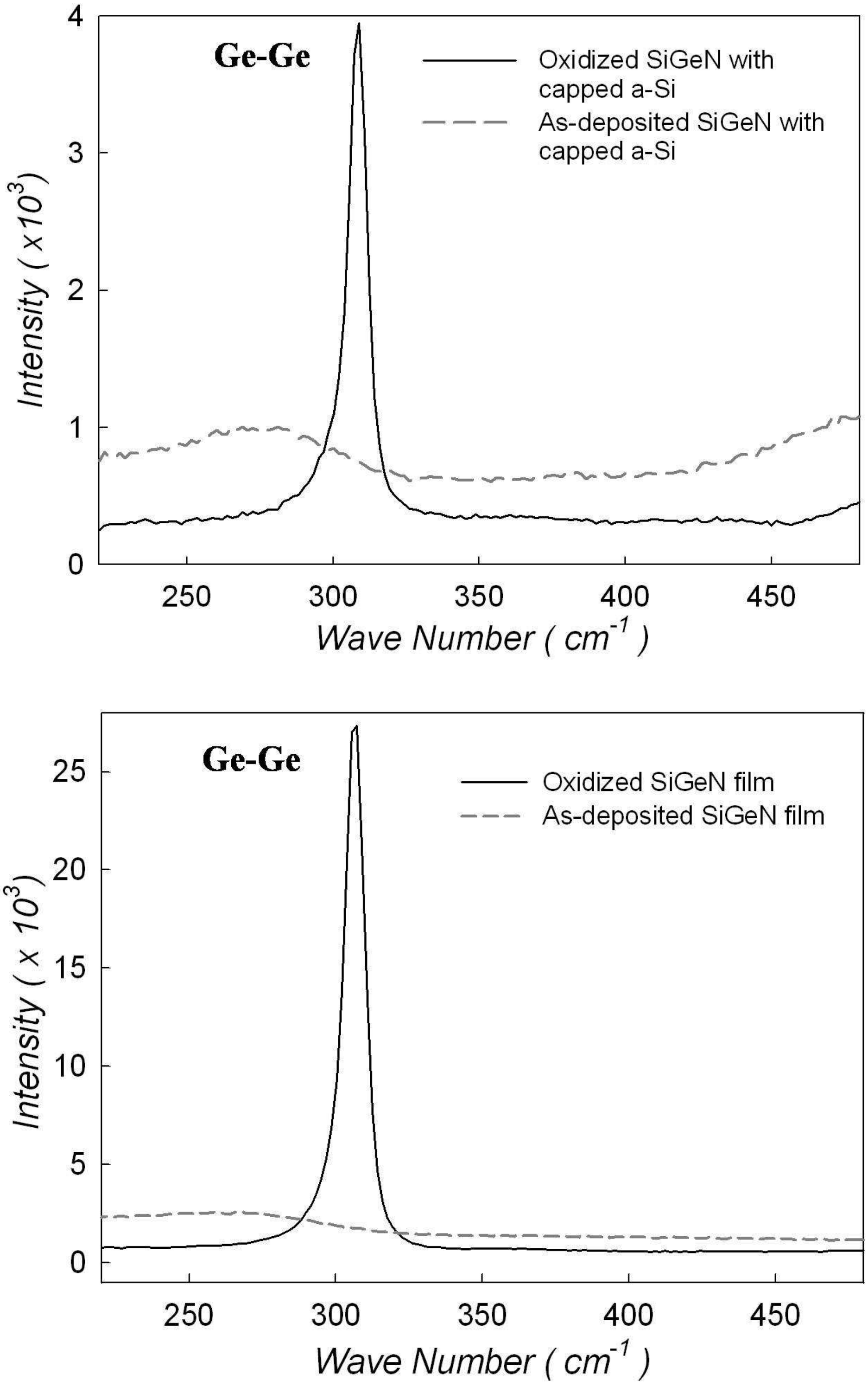


Figure 7-4 (a) Raman spectra of the SiGeN with a top capping a-Si layer, before and after thermal oxidation process; (b)Raman spectra of the SiGeN, before and after thermal oxidation process

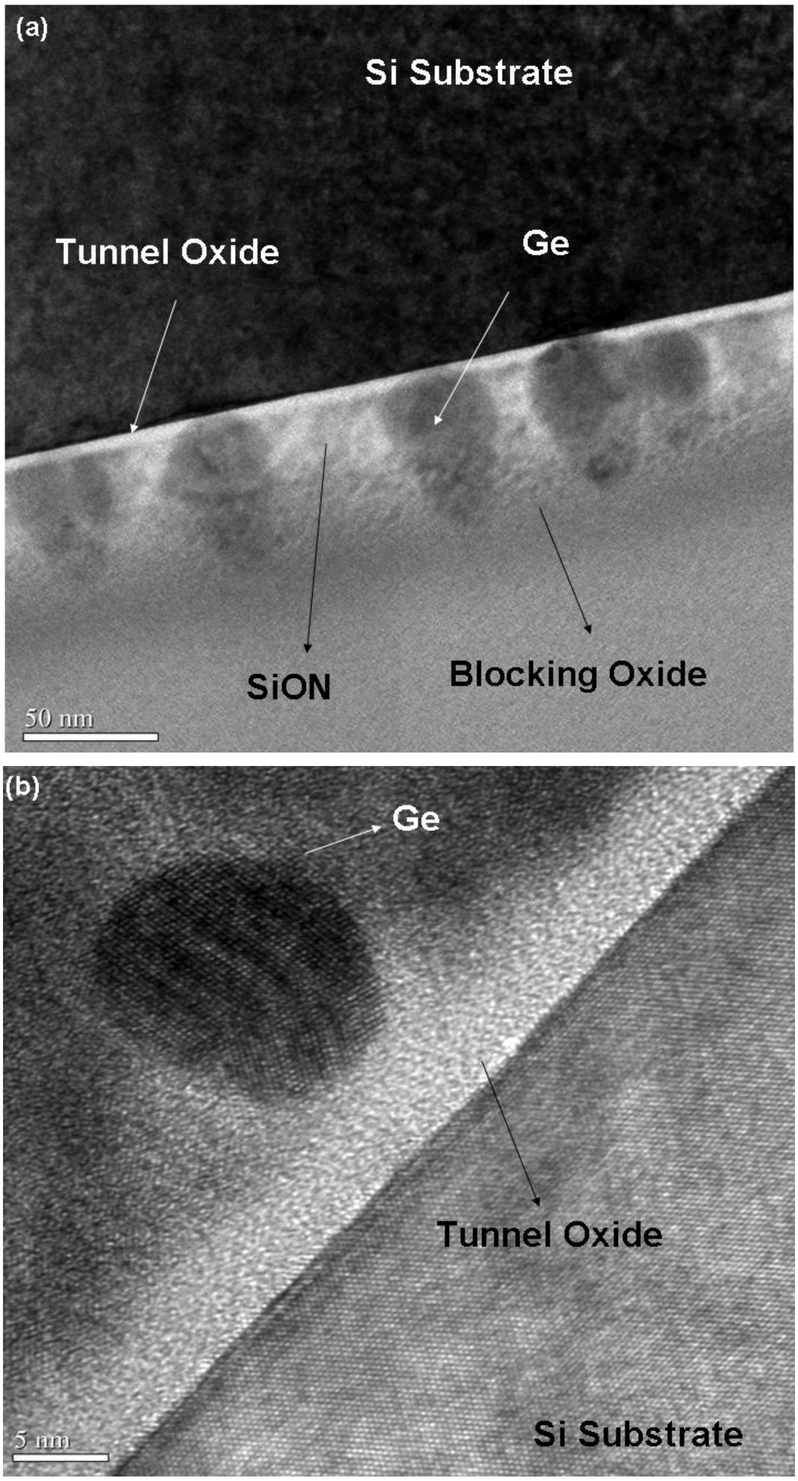


Figure 7-5 Transmission electron microscopy (TEM) analysis of thermal oxidized SiGeN layer (a)with oxidized a-Si layer as blocking oxide, (b)with directly oxidized SiGeN layer as blocking oxide.

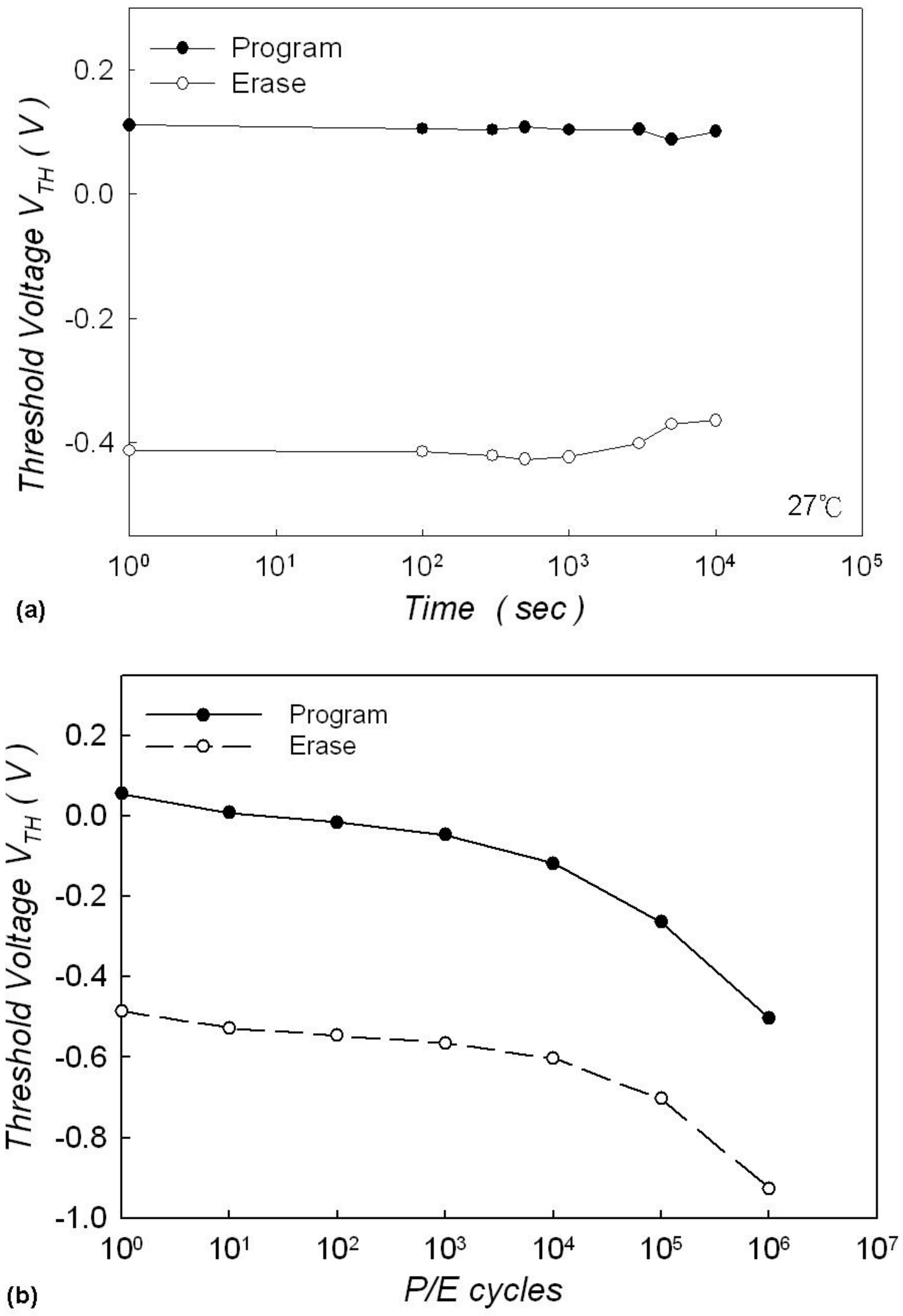


Figure 7-6(a) The threshold voltage shift ($\Delta V_{TH}$) versus different periods of time, (b)The endurance characteristics after different write/erase cycles of Ge nanocrystals nonvolatile memory with oxidized a-Si as blocking oxide

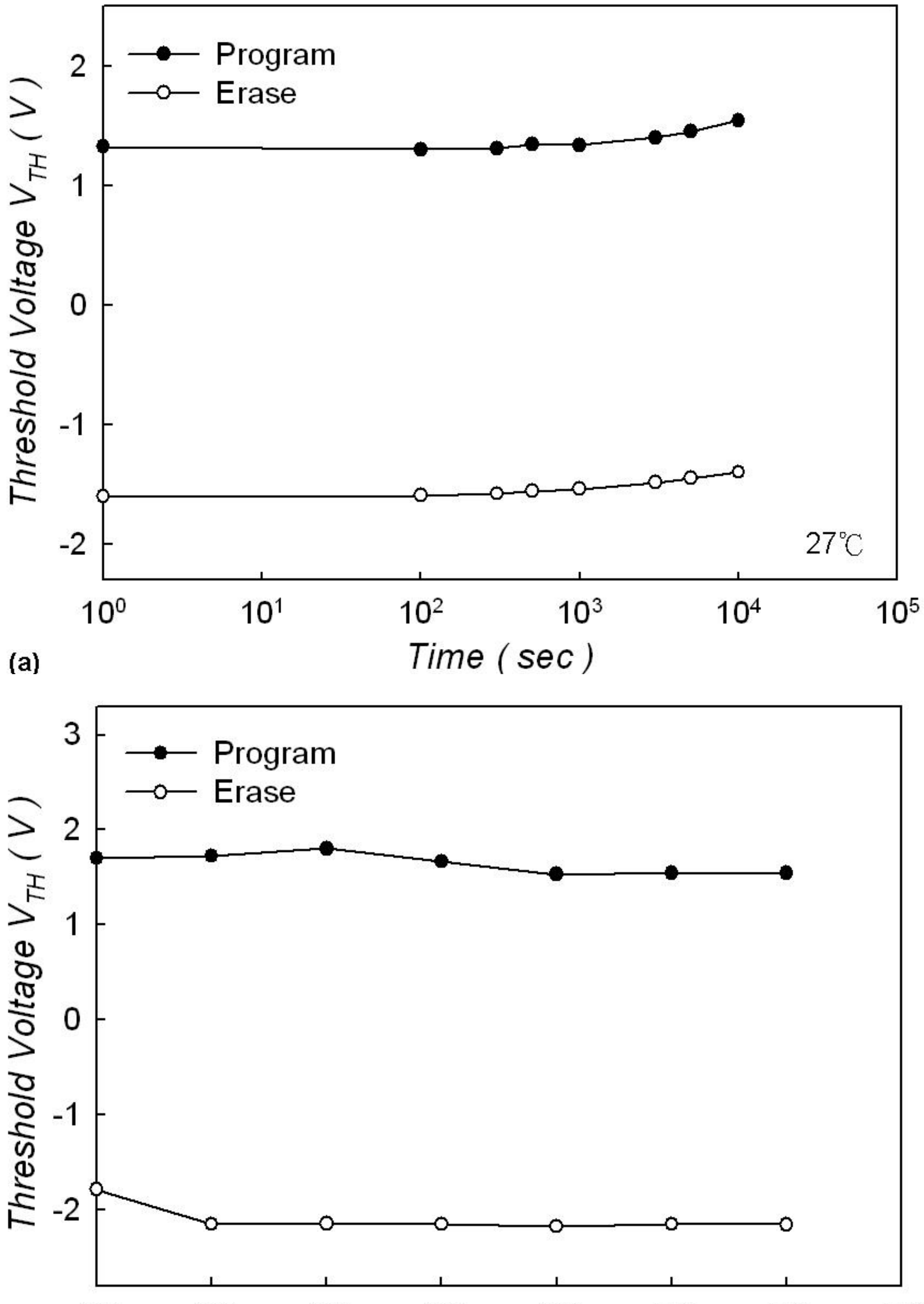


Figure 7-7(a) The retention characteristics and (b) The endurance characteristics of stacked structure with Ge embedded in SiON as charge trapping layer and oxidized SiGeN as blocking oxide

# Chapter 8

# Improved Memory Window for Ge Nanocrystals Embedded in SiON Layer

## 8.1 Introduction

In the past few years, the portable electronic devices have significantly impacted the market of consumer electronics. Because of the low working voltage and nonvolatility, the selection of storage media for most portable electronic devices is the Flash memory which almost bases on the structure of the continuous floating gate (FG) [8.1-8.2]. To date, the stacked-gate FG device structure continues to be the most prevailing nonvolatile-memory implementation, and is widely used in both independent and embedded memories. The invention of FG memory impacts more than the replacement of magnetic-core memory, and creates a moment of portable electronic systems. Despite a huge achievement in commercializing, conventional FG devices have some drawbacks [8.2]. Hence, the disserted stored center concept for charge trapping layer was proposed, such as poly-Si / oxide / nitride / oxide / Si (SONOS) and nanocrystals. In such proposed nonvolatile memory devices, charges are not stored in a continue FG poly-Si layer, but instead in a layer of discrete, mutually isolated. Also, the proposed nonvolatile device can avoid the charge leakage and lower the power consumption when tunneling oxide is thinner [8.3-8.5]. The self-assembling of silicon or germanium nanocrystals embedded in $SiO_2$ layers has been widely studied, and strong memory effects in MOS devices were reported [8.3, 8.6-8.7]. Recently, different charge storage elements have been studied to achieve the robust distributed charge storage [8.8-8.13]. Whereas research on nanocrystal memory has mainly focused on Si and Ge nanocrystals, it is also of interest for its smaller band gap, inducing a theoretically better faster writing/erasing times and reliability [8.14-8.15]. In this contribution, the SiGeN was investigated to be a self-assembling layer [8.16]. The self-assembling layer of SiGeN, fabricated by the directly depositing using plasma enhanced chemical vapor deposition (PECVD) system. The following amorphous silicon (a-Si) was also deposited in one chamber system by using PECVD. The structure with Ge embedded SiON layer exhibits obvious charge-trapping memory effects under electrical measurements.

## 8.2 Experimental

First, a 5-nm-thick thermal oxide was grown as the tunnel oxide on p-type Si substrate by dry oxidation in an atmospheric pressure chemical vapor deposition (APCVD) furnace. Subsequently, 20nm silicon nitride, silicon germanium and silicon-germanium-nitride thin film were prepared on tunnel oxide, respectively. The sequential a-Si layer was also deposited. The oxidation process was performed to fabricate the oxygen-incorporated $SiO_2$ served as blocking oxide, and the oxidation temperature was 900℃. Furthermore, the SiGe-based thin film layer is also oxidized to nucleate the Ge nanocrystals during the blocking oxide formation. Afterward, a steam densification at 900℃ was also performed for 180 sec to densify the blocking oxide. The deposition of the charge trapping film was kept at 200℃ in a low pressure of 0.6 mTorr. The low pressure of 0.6 mTorr during deposition leads the mean free path of electrons to be increased and to improve the uniformity of the thin film. Next, the high temperature thermal oxidation was performed in the thermal furnace in oxygen ambient. The sequent steam oxidation was performed to improve the quality of oxidized a-Si layer as the blocking oxide. Finally, the Al gate was patterned and sintered to form a metal-oxide-insulator-oxide-silicon (MOIOS) structure.

## 8.3 Results and discussion

The MOIOS memory device is utilized to capture the injected carriers from the channel, which causes a variation in the threshold voltage of the memory device. The blocking oxide is utilized to prevent the carriers of gate electrode from injecting into the charge-trapping layer by Fowler-Nordheim (*F-N*) tunneling. Figure 8-1 shows the capacitance-voltage (*C-V*) hysteresis of the MOIOS structure for SiON as charge trapping layer. The electrical *C-V* measurements were performed by bidirectional voltage sweeping. The sweeping conditions were split as follows, (I) operated from 7V to -7 V, and reversely, (II) from 5V to -5V and reversely. It is clearly shown in Fig. 1 that the threshold-voltage shift (memory window, $\Delta V_{TH}$) of the MOIOS structure is prominent for 900℃ oxidation. When the device is programmed, the electrons directly tunnel from the Si substrate through the tunnel oxide, and are trapped in the forbidden gap of silicon- nitride layer. For the erasion process, the holes may tunnel from the valence band of the Si substrate and recombine with the electrons trapped in the SiON layer. The memory window of 0.2 V is observed under an operation of 5V. However, the *C-V* hysteresis of the MOIOS structure for Ge nanocrystal is shown as Figure 8-2. The electrons (holes) directly tunnel from the Si substrate through the tunnel oxide, and are trapped (detrapped) in the forbidden gap of Ge nanocrystal. The lager memory window for Ge nanocrystal embedded in $SiO_2$ layer is obtained than the preview one. This is contributed from the trap state for nanocrystals surrounding the dielectric. Under an operation of 5V, a memory window of 0.4V is exhibited after a cycle of programming and erasing process.

The proposed MOIOS structure via a way of oxidizing SiGeN layer as charge trapping layer is also measured under the same operation conditions. The *C-V* electrical characteristic is shown in Figure 8-3. The threshold-voltage shift after the 5-V programming operation is 1-V for the Ge nanocrystals embedded in SiON memory device with a-Si layer layer oxidized at 900 ℃. The large threshold voltage shift of memory device with an oxidized a-Si film as blocking oxide layer is attributed to the presence of Ge nanocrystals in the SiON film. The memory windows under 5V operation for the three types of MOIOS structure are listed in Table.8-1. It is clearly that the memory window of Ge nanocrystals embedded in SiON memory structure is the largest than the above both. Even the memory window value is lager than the summation of that of SiON and Ge nanocrystal MOIOS structures. The Ge nanocrystal embedded in SiON layer exhibits the superior memory characteristics. It is considered that the extra interface trap states between Ge and SiON film was generated as Ge nanocrystals were embedded in SiON layer. The initial SiON trap state density plus the trap state density as Ge nanocrystal surrounding the dielectric causes more lager memory effect. Figure 8.4 exhibits the band diagrams for charge trapping center for (a) SiON layer, (b) Ge nanocrystal embedded in $SiO_2$ layer, and (c) Ge nanocrystal embedded in SiON layer, respectively. The proposed Ge nanocrystals embedded in SiON stack layer with high-temperature oxidized a-Si layer, therefore, contributes both larger memory window and the additional blocking oxide deposition for the nonvolatile memory application promisingly.

## 8.4 Conclusions

In conclusion, an ease nanocrystal memory technology has been demonstrated by oxidizing SiGeN film to form Ge distributed storage elements embedded in SiON layer. The memory window is obviously lager than the MOIOS structures with SiON layer alone or with Ge nanocrystals embedded in $SiO_2$ layer, and even larger than the summation of both. The exhibition of memory windows after programming is resulted from the formation of Ge nanocrystals embedded in SiON layer and extra interface trap states between Ge and SiON film. Therefore, the material of SiGeN severed as self-assembling layer is more potential for the application in the nanocrystal nonvolatile memory technology.

Table 8-1 The memory windows for three types of nonvolatile memory devices

| ***Nonvolatile Memory*** | ***$\Delta V_{TH}$ under 5V Operation*** |
|---|---|
| SiON | 0.2 |
| Ge Nanocrystal Embedded in $SiO_2$ | 0.4 |
| Ge Nanocrystal Embedded in SiON | 1 |

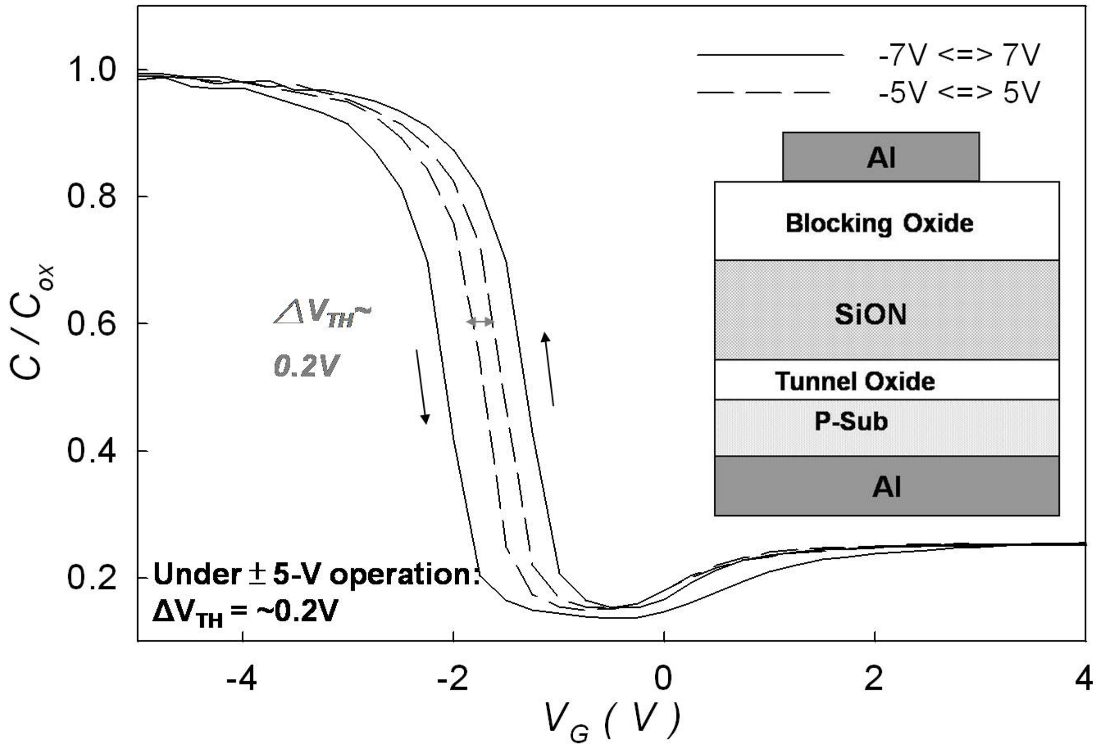


Figure 8-1 The capacitance-voltage (*C-V*) hysteresis of the MOIOS structure for SiON as charge trap center. The electrical *C-V* measurements are performed by bidirectional voltage sweeping from (1) from 7V~(-7)V and (-7)V~7V; (2) from 5V~(-5)V and (-5)V~5V. The insert is the stacked structure for charge trapping center for SiON layer

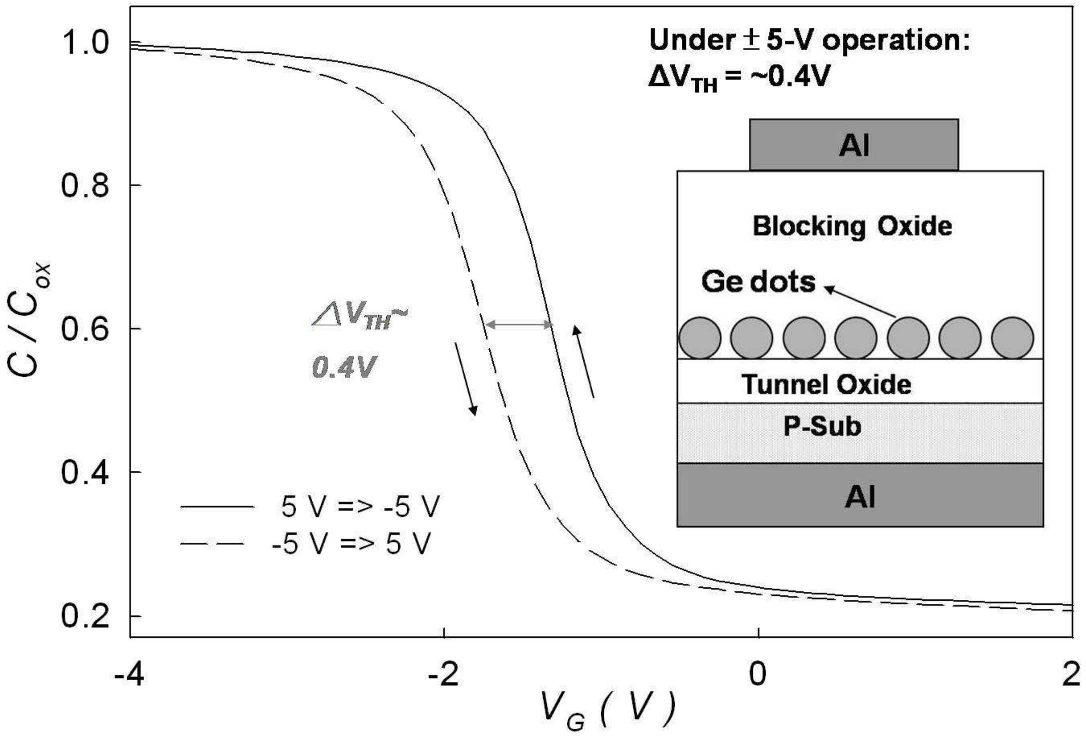


Figure 8-2 The capacitance-voltage (*C-V*) hysteresis of the MOIOS structure for Ge nanocrystal embedded in $SiO_2$ layer as charge trap center. The electrical *C-V* measurements are performed by bidirectional voltage sweeping from 5V~(-5)V and (-5)V~5V. The insert is the stacked structure for charge trapping center for Ge nanocrystal embedded in $SiO_2$ layer

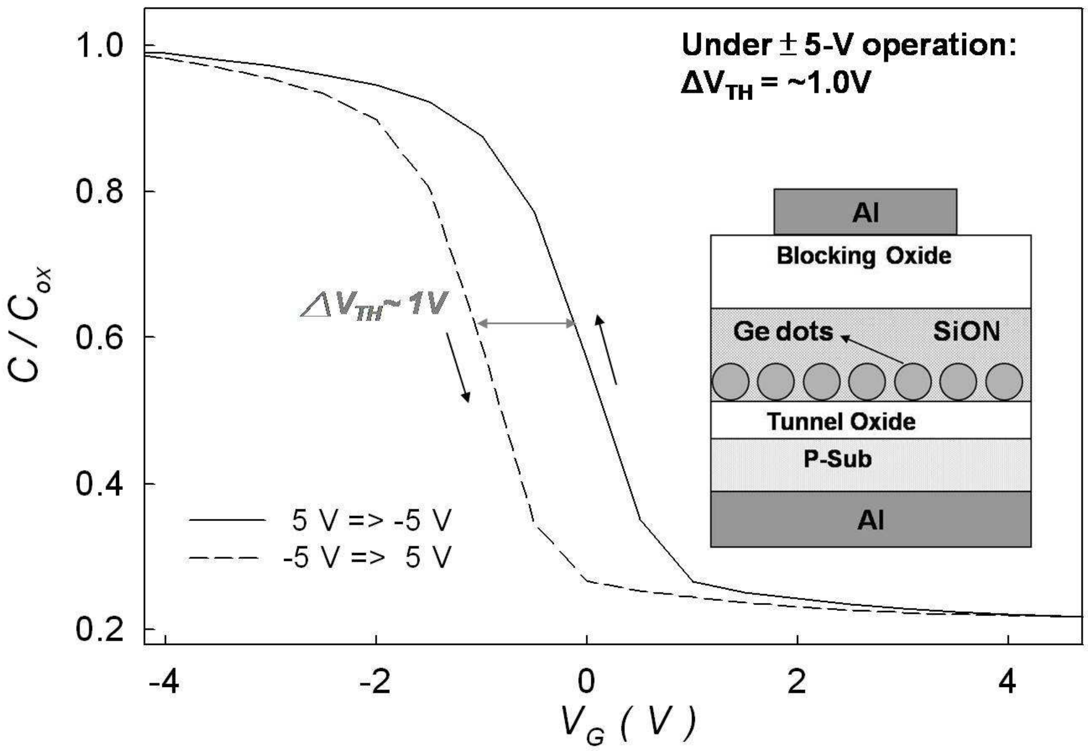


Figure 8-3 The capacitance-voltage (*C-V*) hysteresis of the MOIOS structure for Ge nanocrystal embedded in SiON layer as charge trap center. The electrical *C-V* measurements are performed by bidirectional voltage sweeping from 5V~(-5)V and (-5)V~5V. The insert is the stacked structure for charge trapping center for Ge nanocrystal embedded in SiON layer.

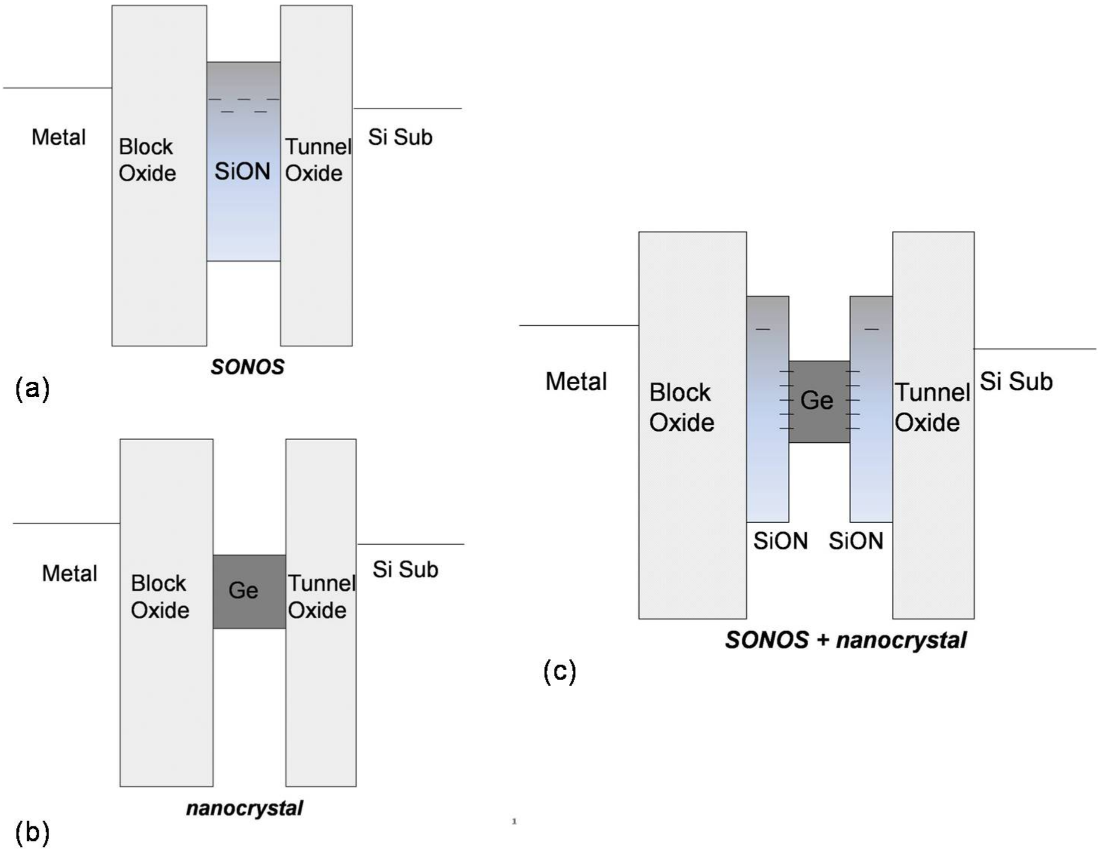


Figure 8-4 The band diagrams for charge trapping center for (a) SiON layer, (b) Ge nanocrystal embedded in $SiO_2$ layer, and (c) Ge nanocrystal embedded in SiON layer, respectively

# Chapter 9

# Application of Thermal Treatment for Germanium Nanocrystal Embedded in Silicon-Oxygen-Nitride Layer

## 9.1 Introduction

Nanocrystal semiconductor materials, such Si and Ge nanocrystals, have been attracted particular attention for the possibility to integrating nanocrystal into existing technology. In addition, Ge nanocrystals were also studied for its lower energy level to cause lower operation voltage and superior program/erase characteristics than Si nanocrystal [9.1-9.2]. Furthermore, the self-assembling technology for nucleating Ge nanocrystal by oxidizing SiGe layer has been a widely used technology [9.3-9.7]. Si is easily combining with oxygen to segregate Ge nanocrystal at the interface of tunnel oxide. In addition, Ge nanocrystals are embedded in silicon oxide layer to be serving as charge trapping center. In this contribution, the nitride-incorporated silicon germanium (SiGeN) was proposed to be a three novel distributed charge storage element in our previous study [9.8]. The Ge nanocrystals are formed after oxidizing SiGeN layer for sufficient oxidation. The SiGeN layer, fabricated by the directly depositing using plasma enhanced chemical vapor deposition (PECVD) system. After high temperature thermal oxidation, the Ge nanocrystals were nucleated in the oxidized SiGeN layer. The conditions for thermal oxidized a-Si layer serving as blocking oxide were also discussed in this study. In addition, steam treatment technology used as a method to improve the oxidation technology, is also discussed in this study. The material analysis such as Raman spectra, Auger electron spectroscopy

(AES) analysis, and transmission electron microscopy (TEM) analysis, were also utilized to determine the composition and the structure of oxidized SiGeN film.

## 9.2 Experimental

5-nm-thick thermal oxide was grown as the tunnel oxide on p-type Si substrate by dry oxidation in an atmospheric pressure chemical vapor deposition (APCVD) furnace. Subsequently, a 20-nm-thick amorphous silicon germanium nitride layer was deposited by plasma enhanced chemical vapor deposition (PECVD) on the tunnel oxide, followed by deposition of 20-nm-thick amorphous silicon. The oxidation process was performed to fabricate the oxygen-incorporated $SiO_2$ served as blocking oxide, and the oxidation temperature was 900℃. The thermal dry oxidation durations were 30 min, 45 min, and 60 min, respectively. Afterward, a steam densification at 900℃ was also performed for 180 sec to densify the blocking oxide for 30 min dry oxidation. The thermal treatment conditions were summarized in Table 9-1. The deposition of the SiGeN film was kept at 200℃ in a low pressure of 0.6 mTorr with precursors of $SiH_4$ (20 sccm), $GeH_4$ (5 sccm), $NH_3$ (30 sccm) and $N_2$ (500 sccm) and plasma power of 20 W. The low pressure of 0.6 mTorr during deposition leads the mean free path of electrons to be increased and to improve the uniformity of the thin film. Next, the conditions of high temperature SiGeN oxidation in Table 1 were performed in the thermal furnace. Finally, the Al gate was patterned and sintered to form a metal-oxide-insulator-oxide-silicon (MOIOS) structure with the charge trapping insulator of SiGeN.

## 9.3 Results and discussion

A thermal furnace process is introduced to form blocking oxide and segregate Ge atoms in this study. The electrical characteristics of Capacitance-Voltage (*C-V*) hysteresis are as shown in Figure 9-1(a), 9-1(b), 9-2, and 9-3, respectively. The gate injection phenomena are clearly found for low oxidation duration (30min and 45 min), as shown in Fig. 9-1(a) and (b). It is considered that the quality is not good enough to resist the current leakage to the gate pad. After longer oxidation duration, the blocking oxide is more denified than the above two. The substrate injection characteristics are found in Fig. 9-3. The memory window is about 1.5V under 5V operation. The insert in Fig. 9-2 is the transmission electron microscope (TEM) analysis of long oxidation duration (60min), exhibits the clearly Ge nanocrystal image at the interface of tunnel oxide. In addition, 30min dry oxidation plus 180sec steam treatment also cause obviously substrate injection characteristics. 2V memory window is obtained under 7V operation as shown in Fig. 9-3. Also, the image of Ge nanocrystals inserted in Fig. 9-3 is similar to long dry oxidation (60min). The memory effect is resulted form the contribution for combination of Ge nanocrystals and SiON charge trapping layer. When the device is programmed (positive voltage), the electrons directly tunnel from the Si substrate through the tunnel oxide, and are trapped in the Ge nanocrystals embedded in SiON layer. For the erasion operation (negative voltage), the holes may tunnel from the valence band of the Si substrate and recombine with the electrons trapped oxidized SiGeN layer. The blocking oxide is utilized to prevent the carriers of gate electrode from injecting into the charge-trapping layer by Fowler-Nordheim (*F-N*) tunneling.

During 900℃ dry oxidation process, Si in the SiGeN film more easily combines with oxygen to form silicon oxide. The Ge atoms will be segregated downward until they reach the tunnel oxide surface for the low solid solubility of Ge in silicon oxide [9.9-9.11]. In addition, the Ge nano-dots (or Ge nanocrystal) are nucleated near the tunnel oxide (or gate oxide). Therefore, the SiGeN film will be oxidized to form blocking oxide; meanwhile, the Ge in the SiGeN film will be segregated to form Ge nano-dots (or Ge nanocrystal) embedded by SiON dielectric near the tunnel oxide.

Furthermore, the current-voltage (*I-V*) characteristic for the above thermal treatment conditions are as shown in Figure 9-4. The leakage current of 30min dry oxidation plus 3min steam treatment is compatible with long duration dry oxidation (60min). It is considered that the higher quality of blocking oxide prevents the stored charge leaking to the gate. Hence, the substrate injection behavior is found for low leakage current as shown in Fig. 9-2 and Fig. 9-3. The steam treatment means let $H_2O$ into thermal furnace, the same as wet oxidation. Owing to its smaller size and lower activation energy than $O_2$ molecules, $H_2O$ molecules are more permeable through the blocking oxide and can efficiently passivate dangling bonds in the blocking oxide. The leakage current is decreasing as the duration of dry oxidation is increasing. The pure dry oxidation is not effectively for its big volume of oxygen atoms which is hard to diffuse to the inner layer. However, the long duration dry oxidation exhibits threshold voltage shift under bidirectional voltage sweep. The steam treatment reduces the thermal budget and improves the quality of blocking oxide. For the $SiO_2$ originated from oxidized a-Si film, there are dangling bonds or defects exist in the bulk and at the interface between SiGeN and $SiO_2$ layer. The electrons trapped near the channel will dominate the threshold voltage significantly than those far from the channel. The proposed SiGeN stack layer with high-temperature oxidized SiGeN layer, therefore, contributes both larger memory window and the additional blocking oxide deposition for the nonvolatile memory application promisingly.

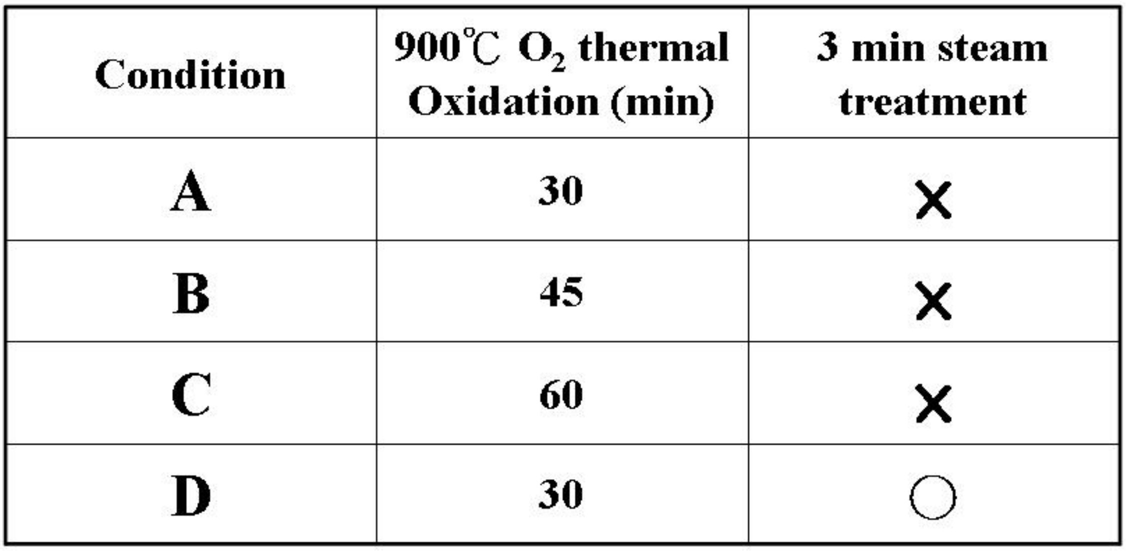
The Auger electron spectroscopy (AES) for as-deposited SiGeN thin film on 5nm-thick tunnel oxide is shown in Figure 9-5(a). The Si, Ge, and N signals and Si signal are uniformly distributed in as deposited SiGeN layer and a-Si layer, respectively. Figure 9-5(b) exhibits that the AES analysis of the MOIOS structure with oxidized SiGeN layer for dry oxidation 30min. It is indicated that the blocking oxide is formed for dry oxidation 30min. In addition, the Ge signal is also segregated after dry oxidation 30min. By increasing the dry oxidation duration, the Ge signal is more obviously observed in the AES analysis as shown in Figure 9-6(a). The Ge nanocrystals are clearly found at the interface of blocking oxide as shown in the TEM analysis of Figure 9-6(b). In addition, it is proven that steam treatment reducing the thermal budget of Ge nanocrystal formation form the above discussion. The AES analysis and TEM analysis for 30min dry oxidation plus 180 sec steam treatment are shown in Figure 9-7(a), and (b), respectively. The Ge nanocrystals are clearly formed at the interface of tunnel oxide. Compared the long duration dry oxidation process, steam treatment can also oxidize the dangling bonds in the blocking oxide from initial dry oxide. Hence, the thermal budget is reduced and the Ge nanocrystals are also nucleated in this condition.

The Raman analyses were also performed to confirm the crystalline phase of oxidized SiGeN layer in this study. Figure 9-8 exhibit that the Raman analysis for dry oxidation 30min and 45min, respectively. As the dry oxidation duration increasing, the Ge-Ge signal is increasing which indicates that the Ge nucleation is more completely. However, the Si-Ge signal is also accompanied with dry oxidation for this MOIOS structure. The upper a-Si layer on SiGeN layer is oxidized to $SiO_2$ layer. In addition, the a-Si is also combined with Ge atoms in SiGeN layer. Hence, the non-completed oxidation makes the Si-Ge signal in this analysis. By increasing the dry oxidation duration, the Si-Ge signal is reducing instead of improved Ge-Ge signal. This result is helpful to assist the issue. The role of steam treatment for crystalline phase in Raman analysis is also explored. Figure 9-9 exhibits steam treatment oxidizes the Si-Ge bonding and causes reduced Si-Ge signal for dry oxidation 30min. However, the Ge-Ge crystalline phase is also reduced. The long dry oxidation (60min) completely oxidizes the MOIOS structure, and the Si-Ge bonds are eliminated compared with the 30min and 45min dry oxidation. The addition of 180sec steam treatment reduces the initial Ge-Ge crystalline phase. The self-assembling Ge nanocrystal is also studied in the preview research in our research group [9.12]. By oxidizing Si atoms in SiGe thin film, the Ge nanocrystals are nucleated. But, over-oxidation make the charge trapping center form Ge nanocrystal to germanium oxide [9.13]. The similar result is also found in this study. As the duration of dry oxidation increasing (unto 60min), the Ge-Ge signal is increasing and even is without any Si-Ge signal as shown in Figure 9-10. In addition, the Ge-Ge signal is decreasing by addition of steam treatment. It is considered that the Ge nanocrystals are oxidized to germanium-oxide. The longer oxidation improve the quality of blocking oxide which will prevent the current leaky to gate. The steam treatment efficiently reduces the thermal budget to obtain the practicable blocking oxide. But, the addition of steam treatment also affects the phase of completely oxidized SiGeN layer.

## 9.4 Conclusions

In conclusion, the ease technology to form SiGeN stack film with both distributed storage elements and upside blocking oxide has been demonstrated successfully for memory application. The memory windows after programming were resulted from the germanium nanocrystal embedded in SiON layer. The completely dry oxidation causes Ge nanocrystal segregate to surface of tunnel oxide. The steam treatment is a method to improve the quality of blocking oxide which reducing the thermal budget. The short dry oxidation plus a simple steam treatment make the memory window and compatible with long duration dry oxidation, including leakage characteristics and memory effect. Steam treatment makes higher quality of blocking oxide formation, higher efficiency of oxidation, and even phase change for completely dry oxidized SiGeN layer. The new material of SiGeN severed as germanium nanocrystal seft-assembling layer was proposed and performed in this study. In addition, the oxidized SiGeN technology is an ease technology for the current nonvolatile memory device.

Table 9-1 The conditions of thermal oxidation for stacked SiGeN layer



| Condition | 900℃ $O_2$ thermal Oxidation (min) | 3 min steam treatment |
|---|---|---|
| A | 30 | × |
| B | 45 | × |
| C | 60 | × |
| D | 30 | ○ |

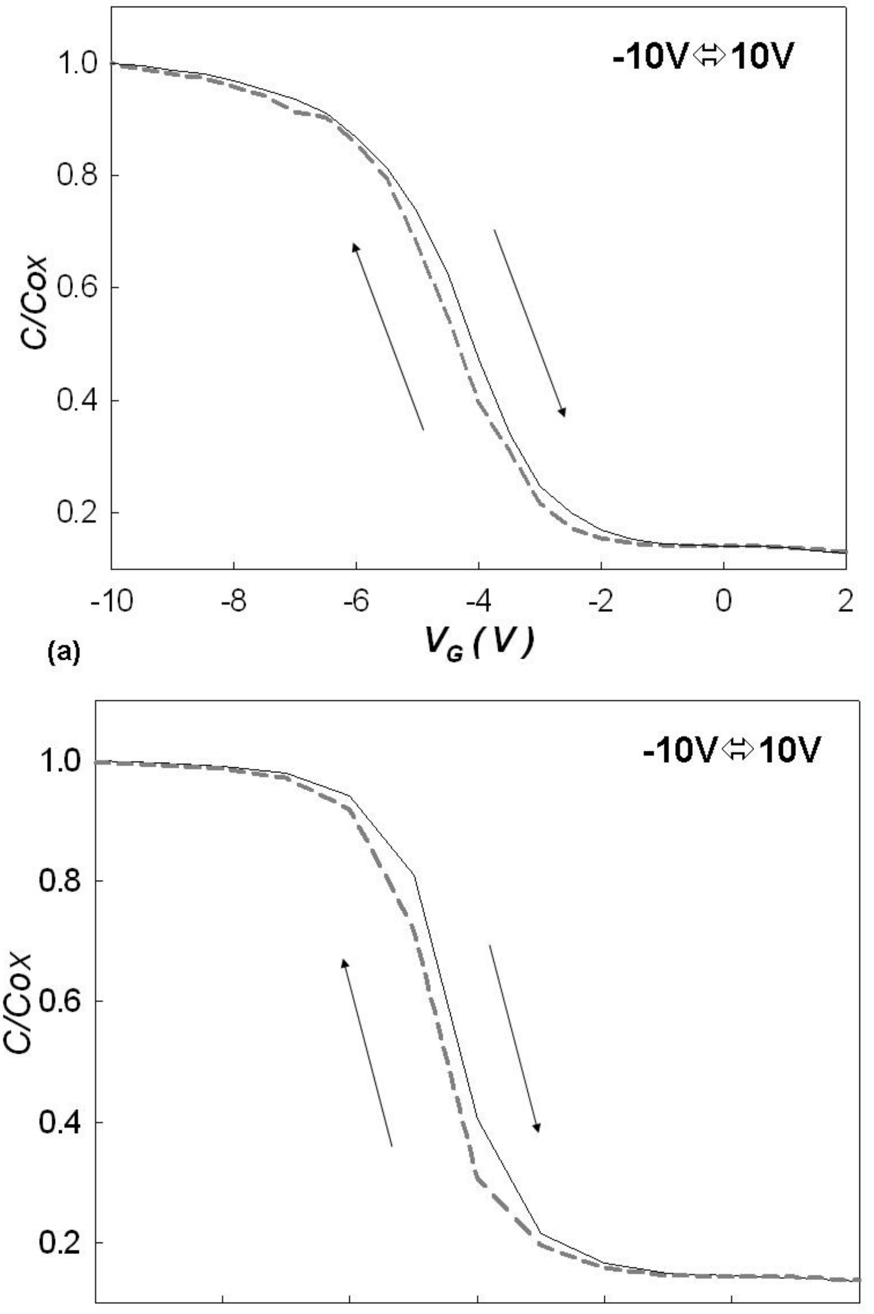


Figure 9-1 The capacitance-voltage (*C-V*) hysteresis of the MOIOS structure for (a) condition A (dry oxidation 30min), (b)condition B (dry oxidation 45min), respectively

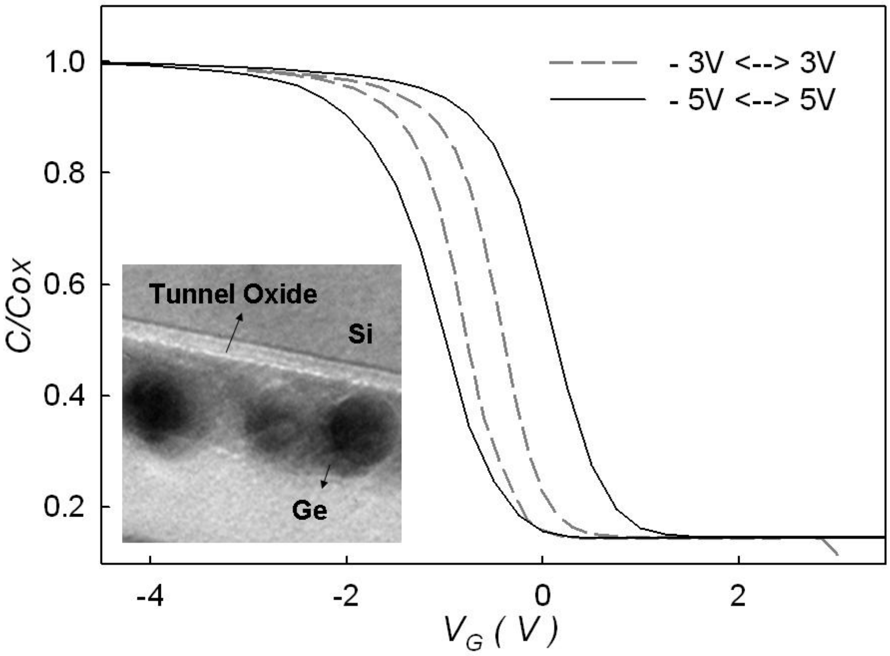


Figure 9-2 The capacitance-voltage (*C-V*) hysteresis of the MOIOS structure for condition C (dry oxidation 60min). The insert is the transmission electron microscopy (TEM) analysis

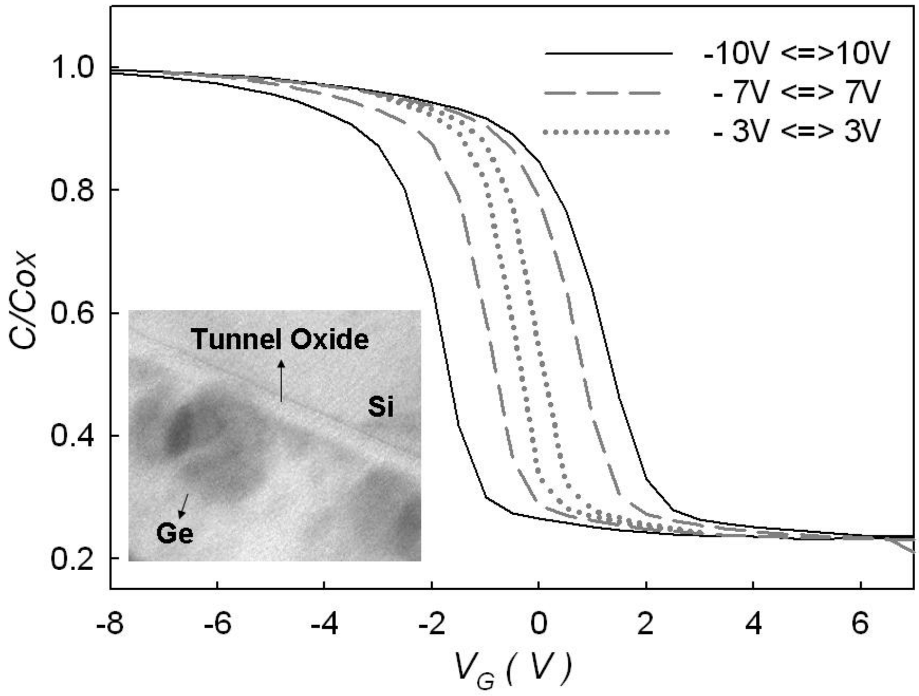


Figure 9-3 The capacitance-voltage (*C-V*) hysteresis of the MOIOS structure for condition D (dry oxidation 30min plus steam treatment 3min). The insert is the transmission electron microscopy (TEM) analysis

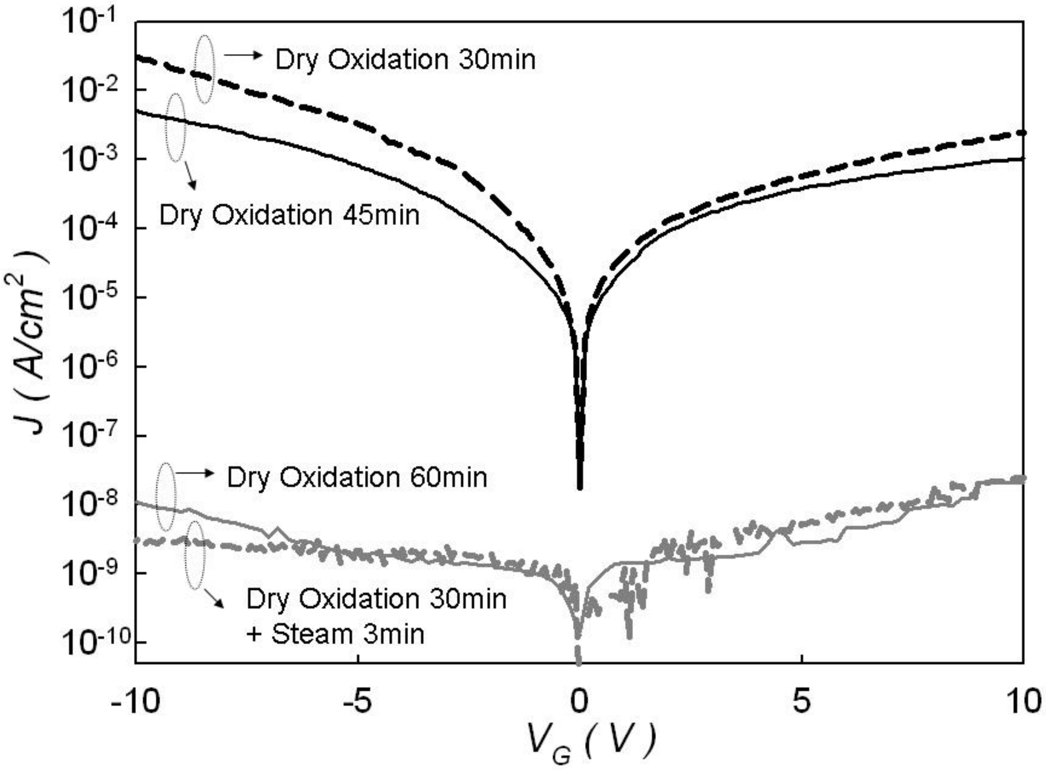


Figure 9-4 The current-voltage (*I-V*) hysteresis of the MOIOS structure for condition A, B, C and D, respectively

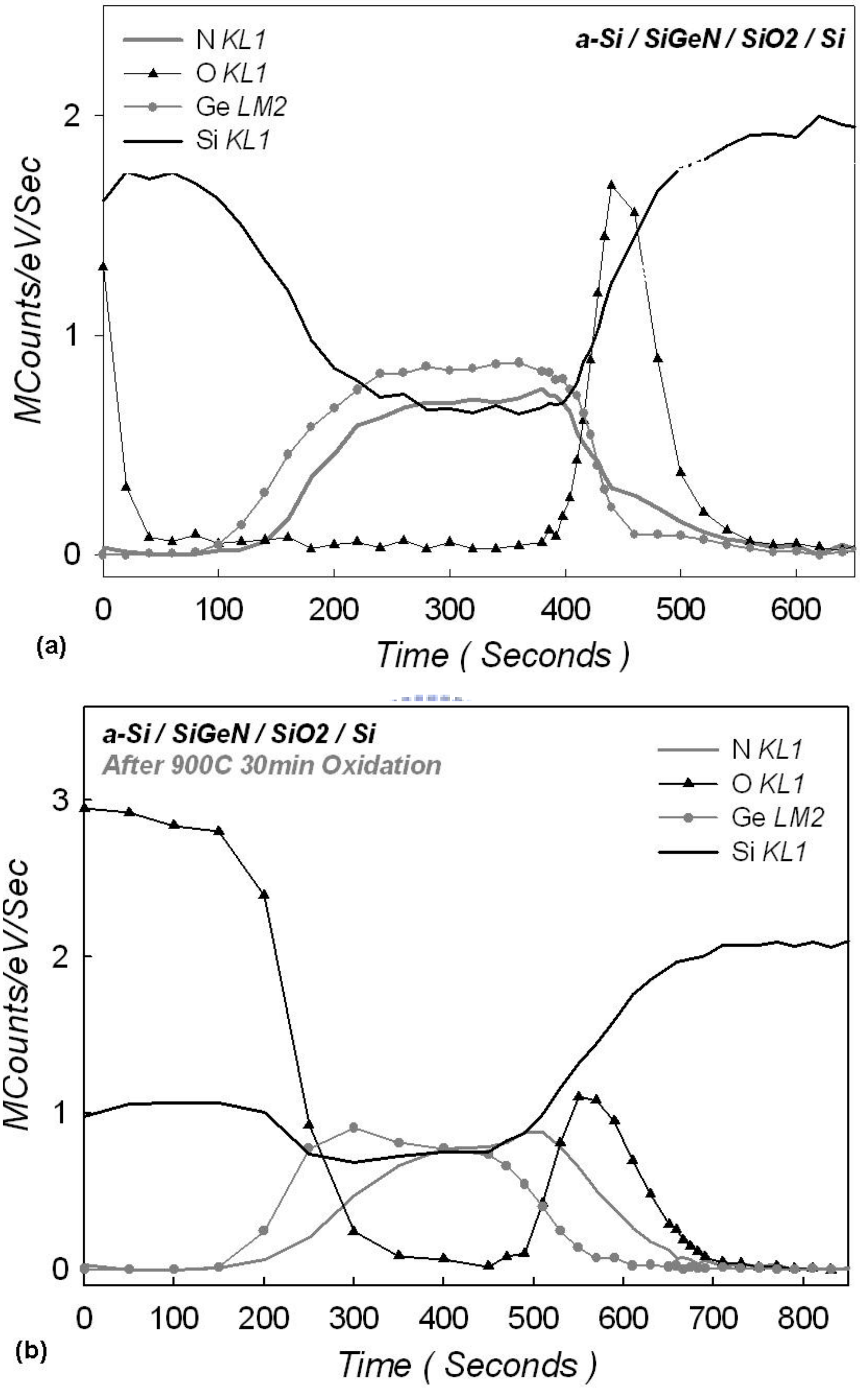


Figure 9-5 The Auger electron spectroscopy (AES) analysis of (a) stacked structure, (b)oxidized stacked structure for dry oxidation 30min

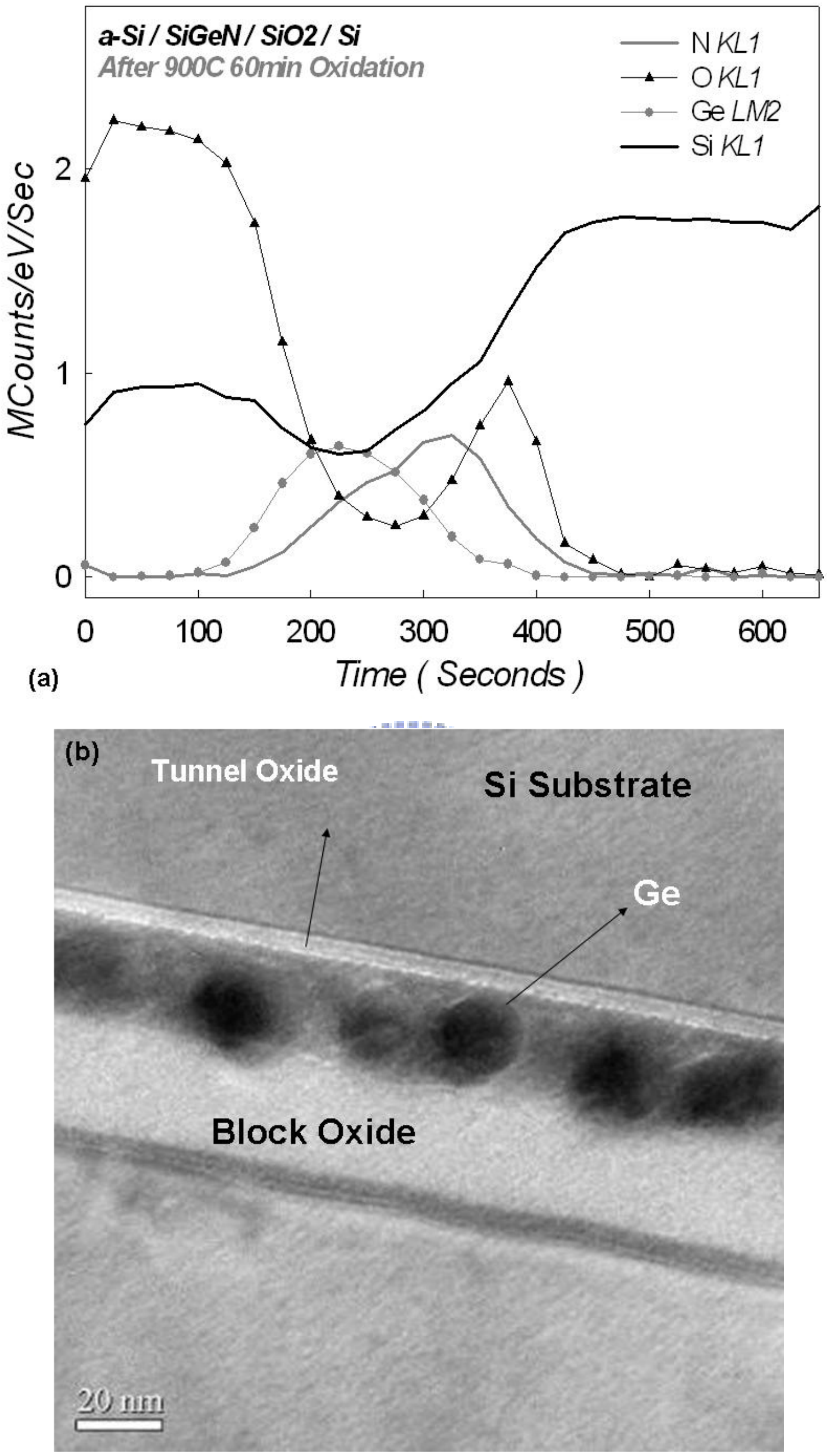


Figure 9-6 (a) The Auger electron spectroscopy (AES) analysis of stacked structure for 60min dry oxidation, (b) The transmission electron microscopy (TEM) analysis of stacked structure for 60min dry oxidation

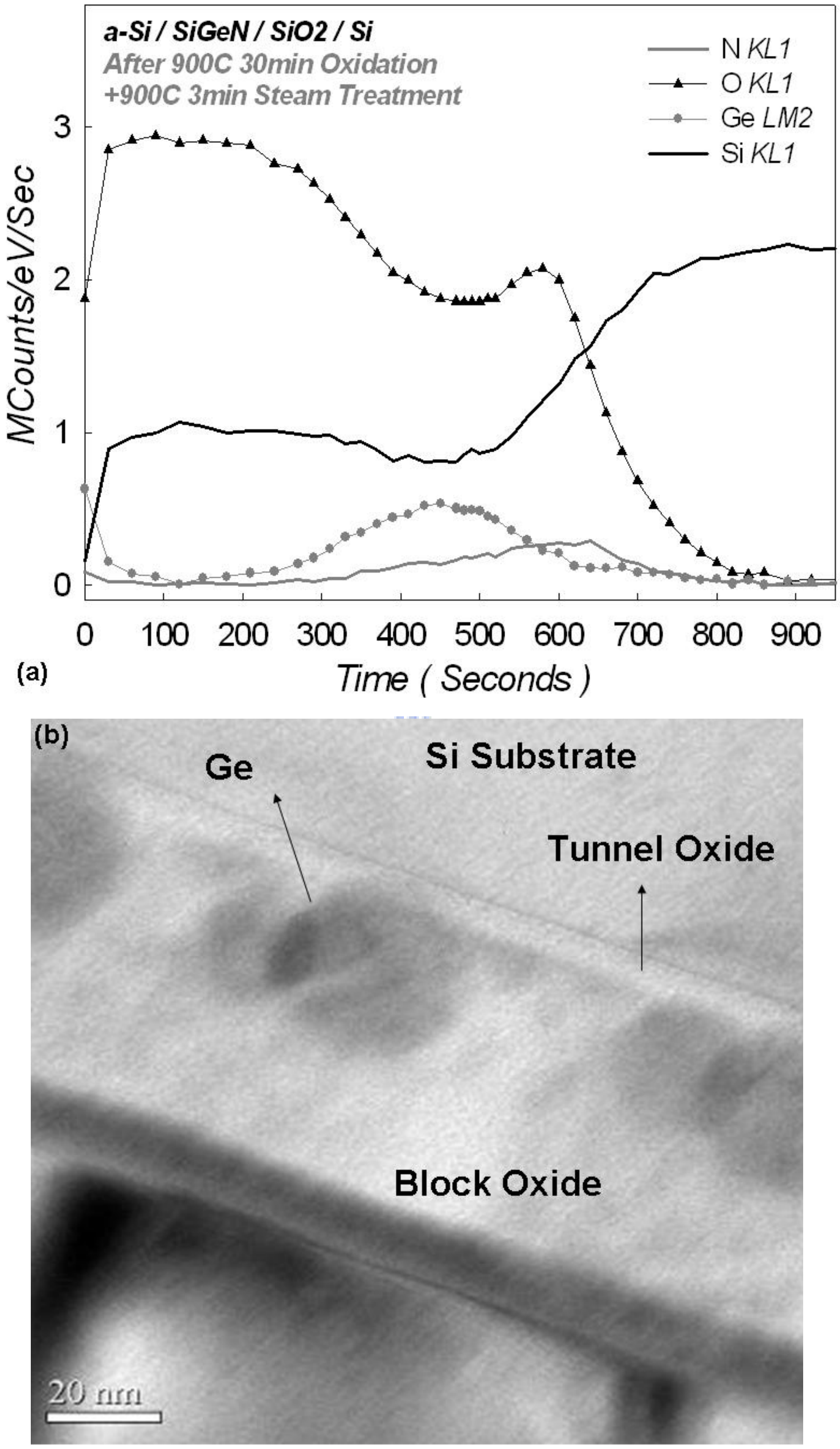


Figure 9-7(a) The Auger electron spectroscopy (AES) analysis of stacked structure for 30min dry oxidation plus 3min steam treatment, (b) The transmission electron microscopy (TEM) analysis of stacked structure for 30min dry oxidation plus 3min steam treatment

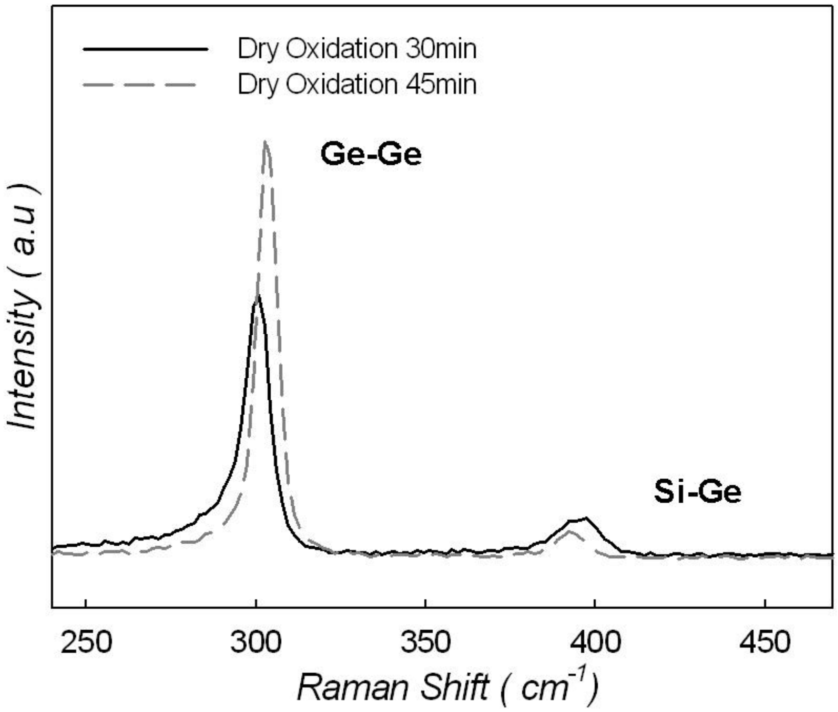


Figure 9-8 The comparison of the Raman spectra of stacked structure for dry oxidation 30min and 45min

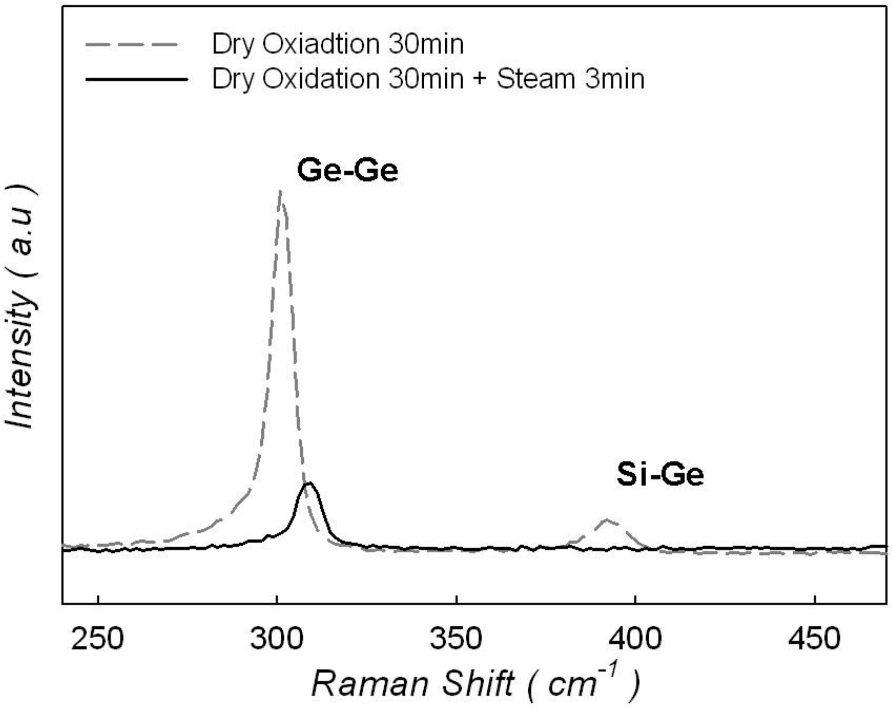


Figure 9-9 The comparison of the Raman spectra of oxidized SiGeN layer for 30min dry oxidation and 30min dry oxidation plus 3min steam treatment, respectively

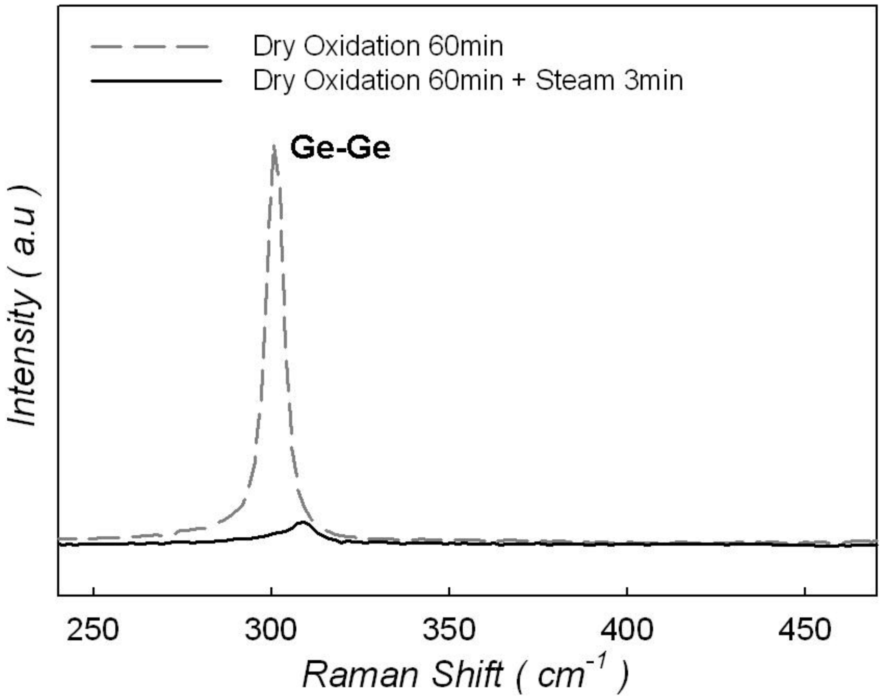


Figure 9-10 The comparison of the Raman spectra of oxidized SiGeN layer for 60min dry oxidation and 60min dry oxidation plus 3min steam treatment, respectively

# Chapter 10

# Application of Thermal Treatment for Silicon-Germanium-Nitride (SiGeN) Layer on Nonvolatile Memory

## 10.1 Introduction

In this contribution, the nitride-incorporated silicon germanium (SiGeN) was proposed to be a three novel distributed charge storage element in our review study [10.1]. The Ge nanocrystals are formed after oxidizing SiGeN layer. The SiGeN layer, fabricated by the directly depositing using plasma enhanced chemical vapor deposition (PECVD) system. After high temperature thermal oxidation, the Ge nanocrystals were nucleated in the oxidized SiGeN layer. The conditions for thermal oxidized SiGeN layer serving as blocking oxide were also discussed in this study. In addition, steam treatment technology used as a method to improve the oxidation technology, is also discussed in this study.

## 10.2 Experimental

First, a 5-nm-thick thermal oxide was grown as the tunnel oxide on p-type Si substrate by dry oxidation in an atmospheric pressure chemical vapor deposition (APCVD) furnace. Subsequently, a 20-nm amorphous silicon germanium nitride layer was deposited by plasma enhanced chemical vapor deposition (PECVD) on the tunnel oxide. The oxidation process was performed to fabricate the oxygen-incorporated $SiO_2$ served as blocking oxide, and the oxidation temperature was 900℃. The thermal dry oxidation durations were 30 min, 45 min, and 60 min, respectively. Afterward, a steam densification at 900 ℃ was also performed for 180 sec to densify the blocking oxide for 30 min dry oxidation. The thermal treatment conditions were summarized in Table 10-1. The deposition of the SiGeN film was kept at 200℃ in a low pressure of 0.6 mTorr with precursors of $SiH_4$ (20 sccm), $GeH_4$ (5 sccm), $NH_3$ (30 sccm) and $N_2$ (500 sccm) and plasma power of 20 W. The low pressure of 0.6 mTorr during deposition leads the mean free path of electrons to be increased and to improve the uniformity of the thin film. Next, the high temperature SiGeN oxidation was performed in the thermal furnace in oxygen ambient. The sequent steam oxidation was performed to improve the quality of oxidized SiGeN layer as the blocking oxide. Finally, the Al gate was patterned and sintered to form a metal-oxide-insulator-oxide-silicon (MOIOS) structure with the charge trapping insulator of SiGeN.

## 10.3 Results and discussion

A thermal furnace process is introduced to form blocking oxide (SiOx or SiON) and segregate Ge atoms in this study. During 900℃ dry oxidation process, Si in the SiGeN film more easily combine with $O_2$ than Ge to form SiOx. Because of the low solid solubility of Ge in silicon oxide, the Ge atoms will be segregated downward until they reach the tunnel oxide surface [10.2-10.4] and nucleate to form Ge nano-dots (or Ge nanocrystal) near the tunnel oxide (or gate oxide). Therefore, the SiGeN film will be oxidized to form SiOx film (as blocking oxide); meanwhile, the Ge in the SiGeN film will be segregated to form Ge nano-dots (or Ge nano-crystal) embedded by SiON dielectric near the tunnel oxide. The electrical characteristics of Capacitance-Voltage (*C-V*) hysteresis were as shown in Figure 10-1 (a), 10-1(b), 10-2(a), and 10-2(b), respectively. The gate injection phenomena are clearly found for low oxidation duration (30min and 45 min), as shown in Fig. 1(a) and (b). It is considered that the quality is not good enough to resist the current leakage to the gate pad. For the same oxidation rate, the a-Si with the same depth (20nm) is clearly becoming $SiO_2$ layer. After longer oxidation duration, the blocking oxide is more denified than the above two. The substrate injection characteristics are found in Fig. 10-2(a). The memory window is about 4V under 5V operation. In addition, 30min dry oxidation plus 180sec steam treatment also cause obviously substrate injection characteristics. 1V memory window is obtained under 10V operation. Furthermore, the current-voltage (*I-V*) characteristic for the above thermal treatment conditions are as shown in Figure 10-3. The leakage current of 30min dry oxidation plus 3min steam treatment is compatible with long duration dry oxidation (60min). The leakage current is decreasing as the duration of dry oxidation is increasing. The pure dry oxidation is not effectively for its big volume of oxygen atoms which is hard to diffuse to the inner layer. However, the long duration dry oxidation exhibits more obviously threshold voltage shift under bidirectional voltage sweep. When the device is programmed, the electrons directly tunnel from the Si substrate through the tunnel oxide, and are trapped in the Ge nanocrystals embedded in SiON layer. For the erasion operation, the holes may tunnel from the valence band of the Si substrate and recombine with the electrons trapped oxidized SiGeN layer. The blocking oxide is utilized to prevent the carriers of gate electrode from injecting into the charge-trapping layer by Fowler-Nordheim (*F-N*) tunneling.

For the $SiO_2$ originated from oxidized SiGeN film, there are dangling bonds or defects exist in the bulk and at the interface between SiGeN and $SiO_2$ layer. The electrons trapped near the channel will dominate the threshold voltage significantly than those far from the channel. The proposed SiGeN stack layer with high-temperature oxidized SiGeN layer, therefore, contributes both larger memory window and the additional blocking oxide deposition for the nonvolatile memory application promisingly.

The Auger electron spectroscopy (AES) for as-deposited SiGeN thin film on 5nm tunnel oxide is shown in Figure 10-4 (a). The Si, Ge, and N signals are uniformly distributed in as deposited SiGeN layer. The result is the same as the transmission electron microscope (TEM) analysis in Figure 10-4 (b), there is only a dielectric image on tunnel oxide without any crystallized image. Figure 10-5 (a) exhibits that the AES analysis of the MOIOS structure with oxidized SiGeN layer. The Ge signal is clearly segregated at the interface of tunnel oxide layer. In addition, Ge nanocrystals are embedded in SiON layer and the blocking oxide is also formed. The Ge nanocrystal image is also clearly found in Figure 10-5(b) which is also corresponding to the AES result ( Fig. 10-5(a) ). The memory effect is resulted form the contribution for combination of Ge nanocrystals and SiON charge trapping layer. The 30min dry oxidation plus 180sec steam treatment cause the SiGeN layer completely oxidized and the Ge atoms segregate to the blocking oxide as shown in Figure 10-6(a). There is no Ge signal segregated at the interface of blocking oxide. Figure 10-6(b) shows the TEM analysis for short oxidation duration plus simple steam treatment. The Ge nanocrystals are far from the tunnel oxide which is different form the long duration of dry oxidation. The schematic of the Ge nanocrystal formation is as shown in Figure 10-7. For the pure oxygen oxidation, the Ge is segregated to the surface of tunnel oxide in the hot environment. The final schematic of long duration oxidation is as shown in Fig. 10-7 (after 60min dry oxidation). However, the blocking oxide is also formed after 30 min dry oxidation. There is not enough thermal treatment to let Ge atom to be nucleated and to be pushed to the surface of tunnel oxide. The sequential steam treatment is a quickly thermal process. The un-completely oxidized bonds in the blocking oxide will be efficiently oxidized and. In addition, the Ge nanocrystals are instantaneously arising at the initial location. Hence, the formed Ge nanocrystals are far form the tunnel oxide. The thicker tunnel dielectric causes the lower program/erase efficiency as shown in Fig. 10-2(a) and (b).

Raman analysis was used to distinguish the phase transformation for oxidized SiGeN layer and as-deposited SiGeN layer. The 300cm$^{-1}$ signal in the Raman analysis represent that the Ge-Ge signals are formed by the Ge nanocrystal formation. The longer dry oxidation duration, the more obviously Ge-Ge signals are found as shown in Figure 10-8(a), and (b), respectively. It indicates that more oxidized Si will nucleate more Ge nanocrystal. The steam treatment also causes the crystalline phase change. The Ge-Ge signals are formed after thermal dry oxidation which indicates that the Ge nanocrystal is also formed during blocking oxide formation. This is corresponding to the Ge nanocrystal formation mechanism in Fig. 10-7. The addition of steam treatment decreases the initial Ge crystalline instead of increasing the germanium-oxide signal as shown in Figure 10-9. In the preview report for seft-assembling Ge nanocrystal, the excessively oxidation causes the germanium oxide formation [10.5]. The similar result is also found in this study. As the duration of dry oxidation increasing, the Ge-Ge signal is increasing. Steam treatment causes the decreasing of Ge-Ge signal instead of increasing of germanium oxide as shown in Figure 10-10.

## 10.4 Conclusions

In conclusion, the ease technology to form SiGeN stack film with both distributed storage elements and upside blocking oxide has been demonstrated successfully for memory application. The memory windows after programming were resulted from the germanium nanocrystal embedded in SiON layer. The completely dry oxidation causes Ge nanocrystal segregate to surface of tunnel oxide. The steam treatment is a method to improve the quality of blocking oxide which reducing the thermal budget. The short dry oxidation plus a simple steam treatment make the memory window, but the Ge nanocrystal formation far form the tunnel oxide which reduces the efficiency of memory. The new material of SiGeN severed as germanium nanocrystal seft-assembling layer was proposed and performed in this study. In addition, the thermal treatment makes different Ge nanocrystal formation mechanism.

Table 10-1 The conditions of thermal oxidation for stacked SiGeN layer

| **Condition** | **900℃ $O_2$ thermal Oxidation (min)** | **3 min steam treatment** |
|---|---|---|
| **A** | **30** | ✕ |
| **B** | **45** | ✕ |
| **C** | **60** | ✕ |
| **D** | **30** | ○ |

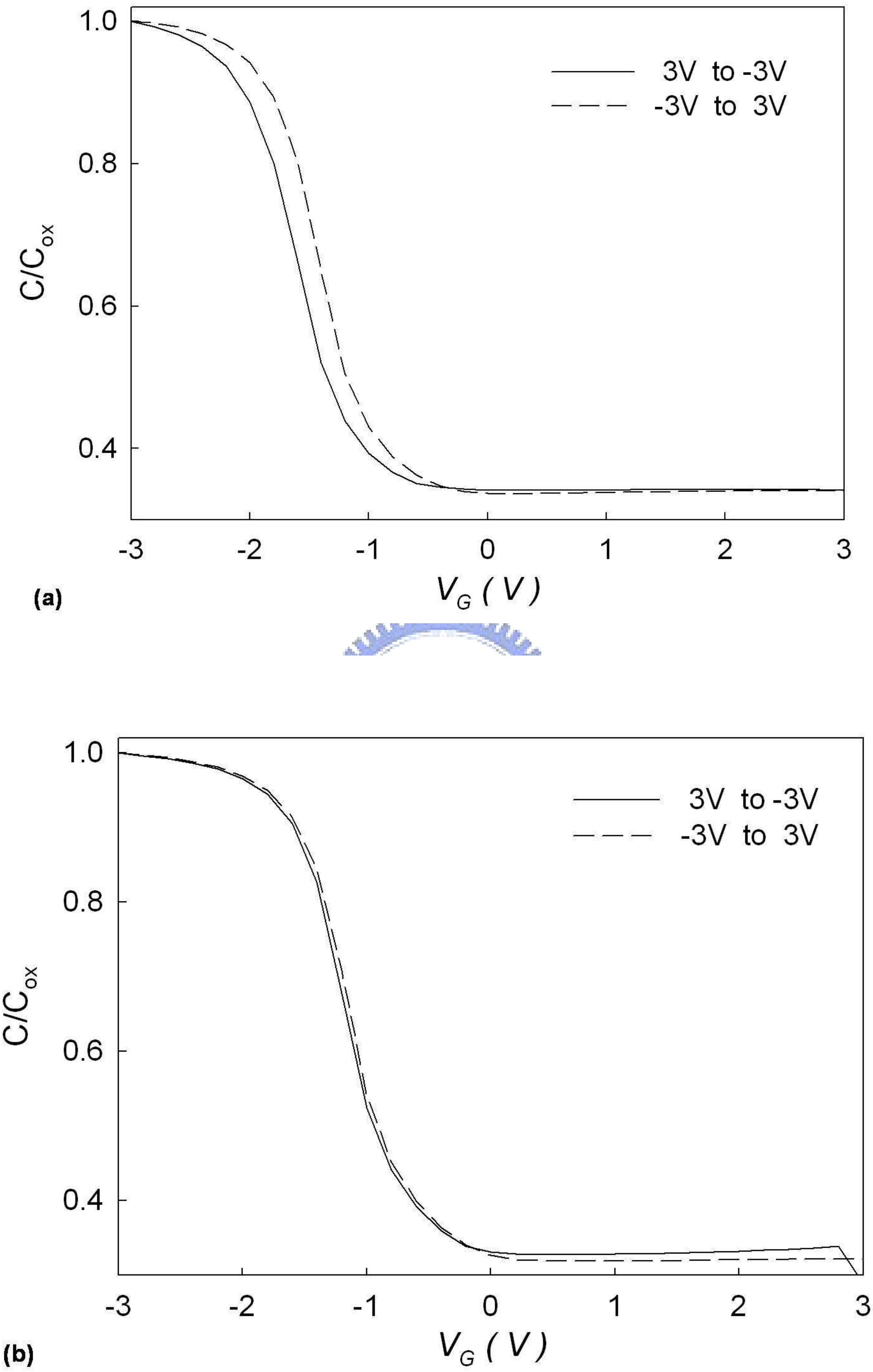


Figure 10-1 The capacitance-voltage (*C-V*) hysteresis of the MOIOS structure for (a) condition A (dry oxidation 30min), (b)condition B (dry oxidation 45min), respectively

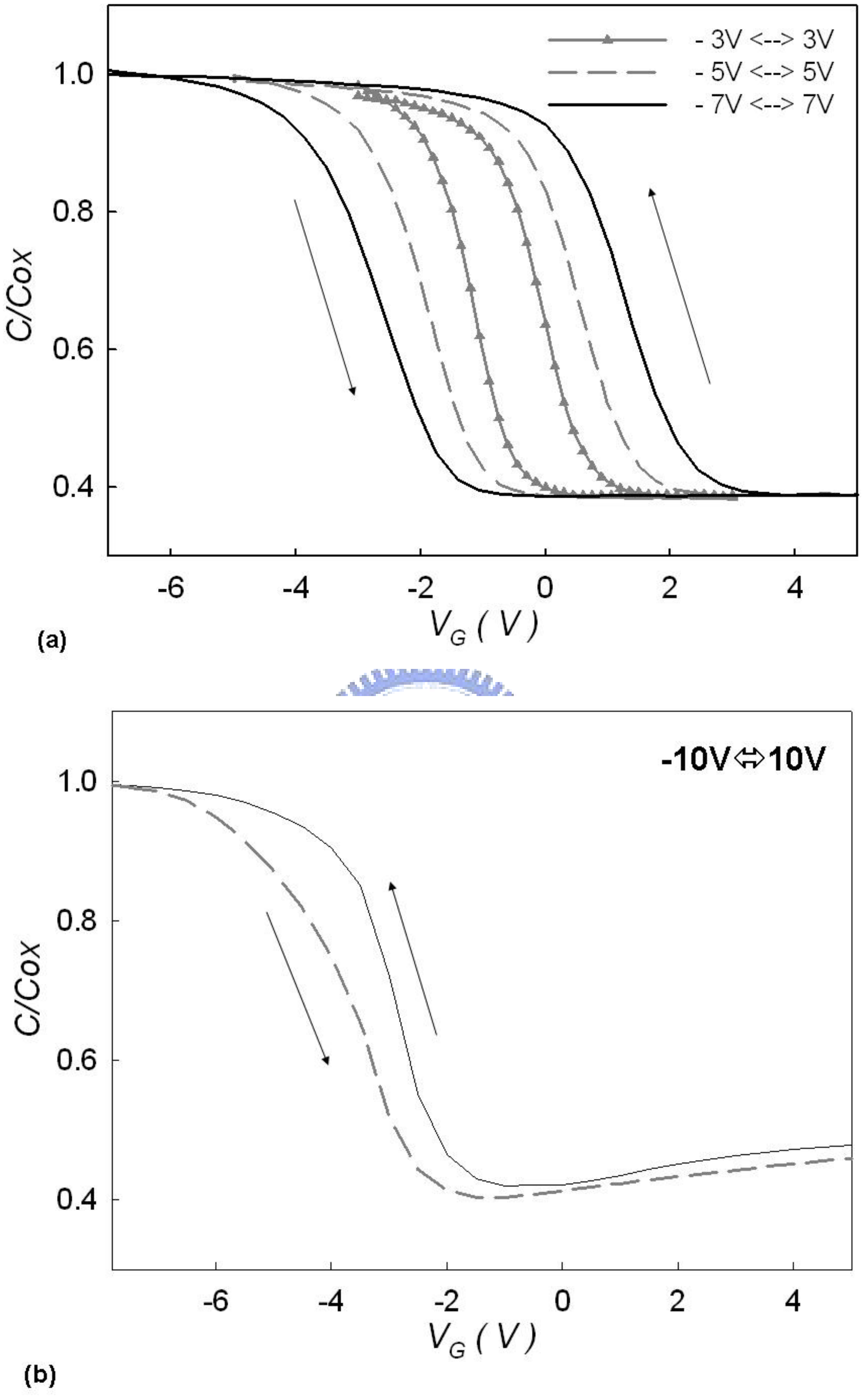


Figure 10-2 The capacitance-voltage (*C*-*V*) hysteresis of the MOIOS structure for (a) condition C (dry oxidation 60min) and condition D (dry oxidation 30min plus steam treatment 3min), respectively

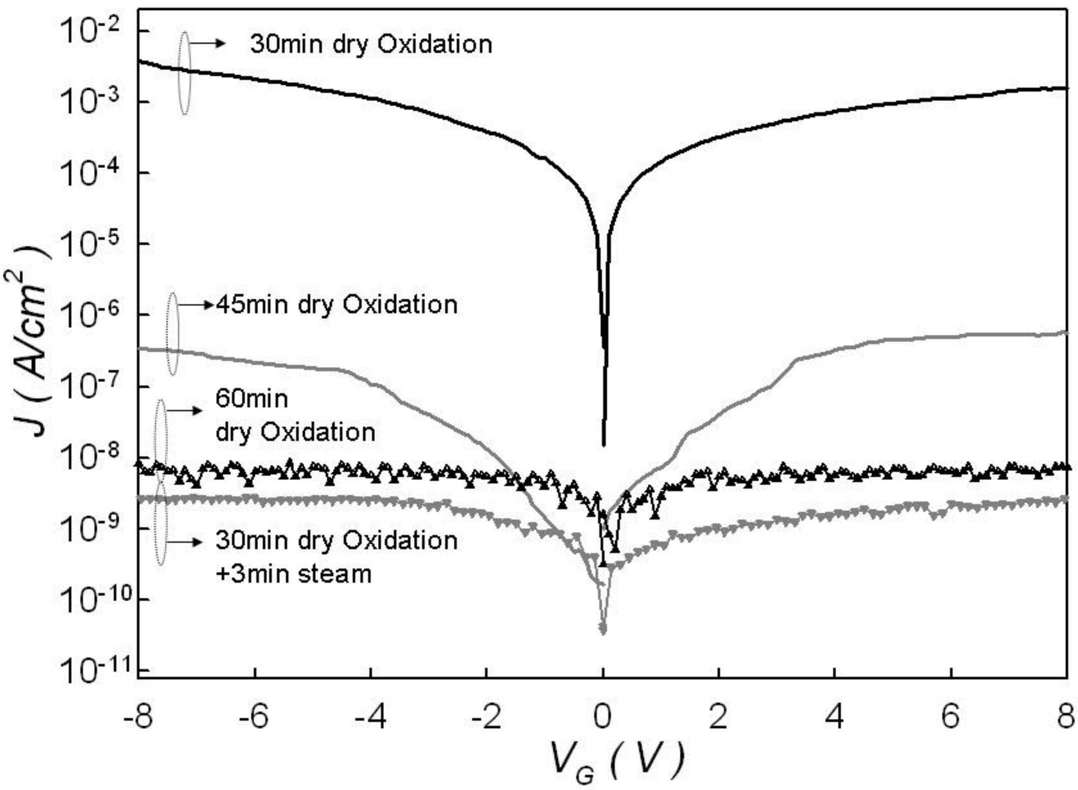


Figure 10-3 The current-voltage (*I*-*V*) hysteresis of the MOIOS structure for condition A, B, C and D, respectively

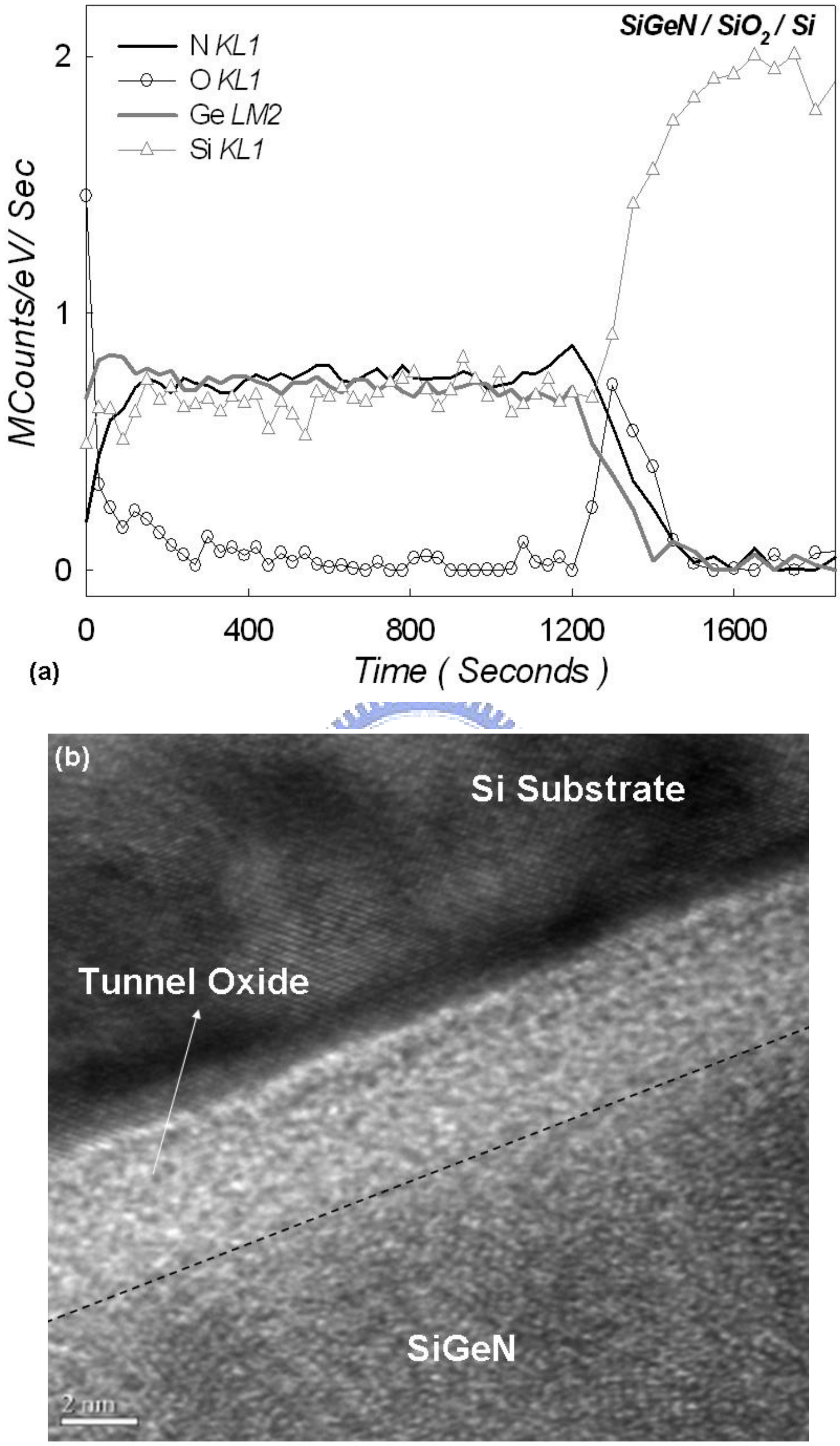


Figure 10-4 (a) The Auger electron spectroscopy (AES) analysis of stacked structure, (b) The TEM analysis of stacked structure

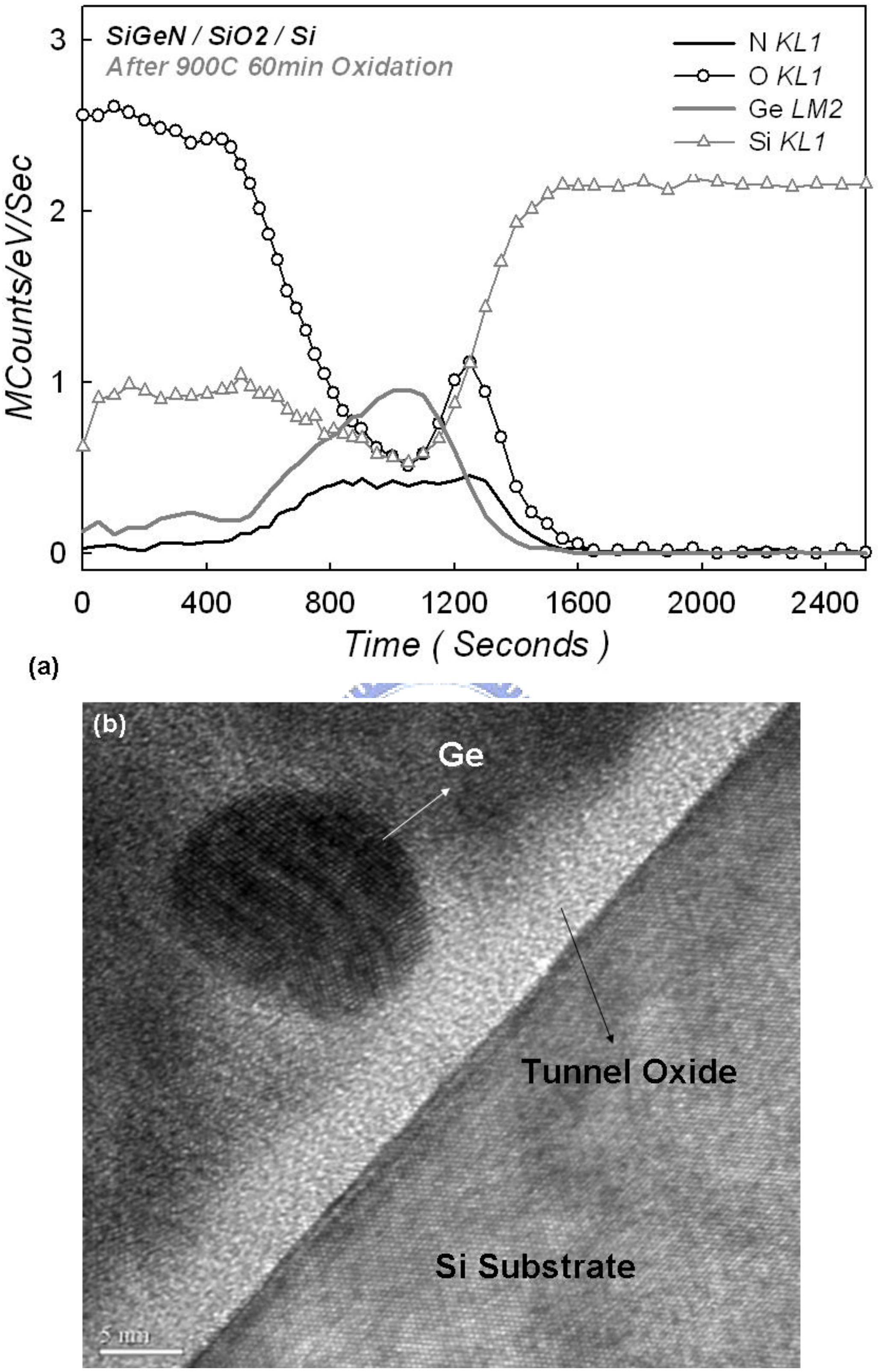


Figure 10-5 (a) The Auger electron spectroscopy (AES) analysis of stacked structure for 60min dry oxidation, (b) The TEM analysis of stacked structure for 60min dry oxidation

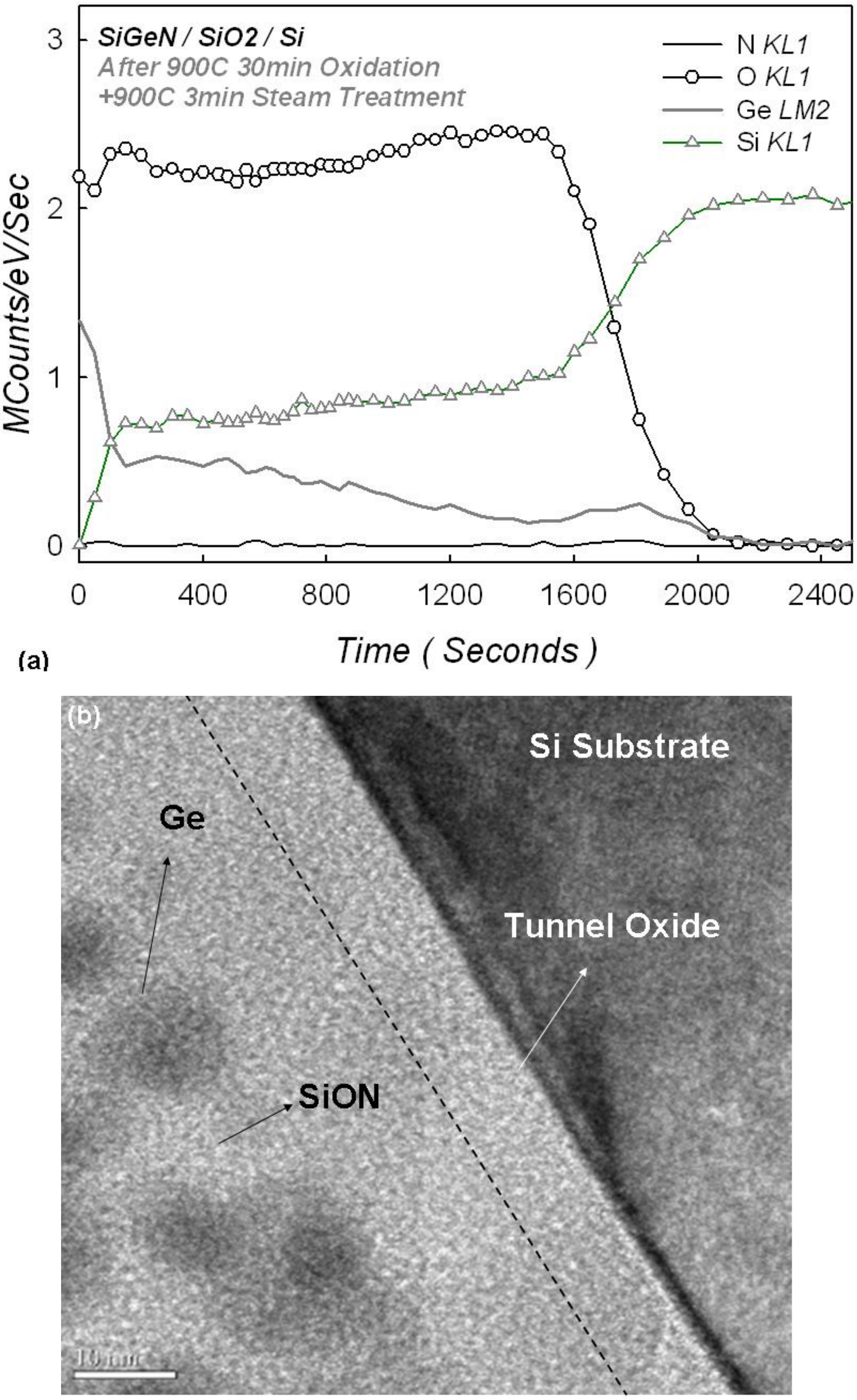


Figure 10-6 (a) The Auger electron spectroscopy (AES) analysis of stacked structure for 30min dry oxidation plus 3min steam treatment, (b) The TEM analysis of stacked structure for 30min dry oxidation plus 3min steam treatment

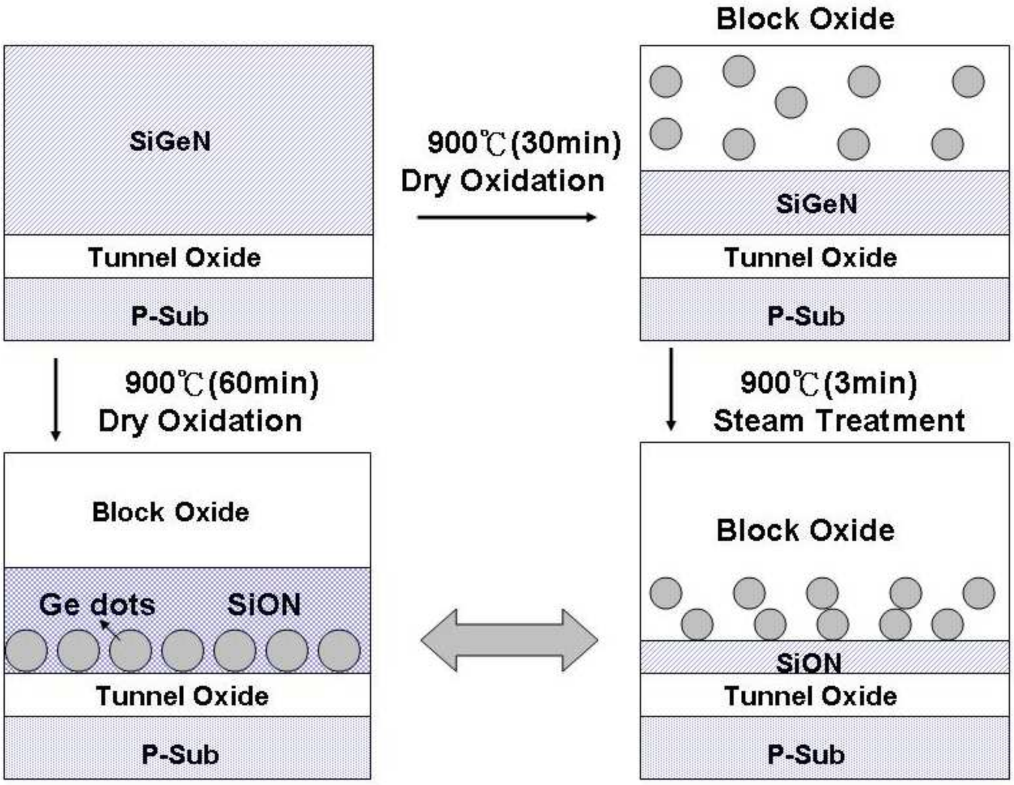


Figure 10-7 The process flow proposed in this work for 60min dry oxidation, and 30min dry oxidation plus 3min steam treatment

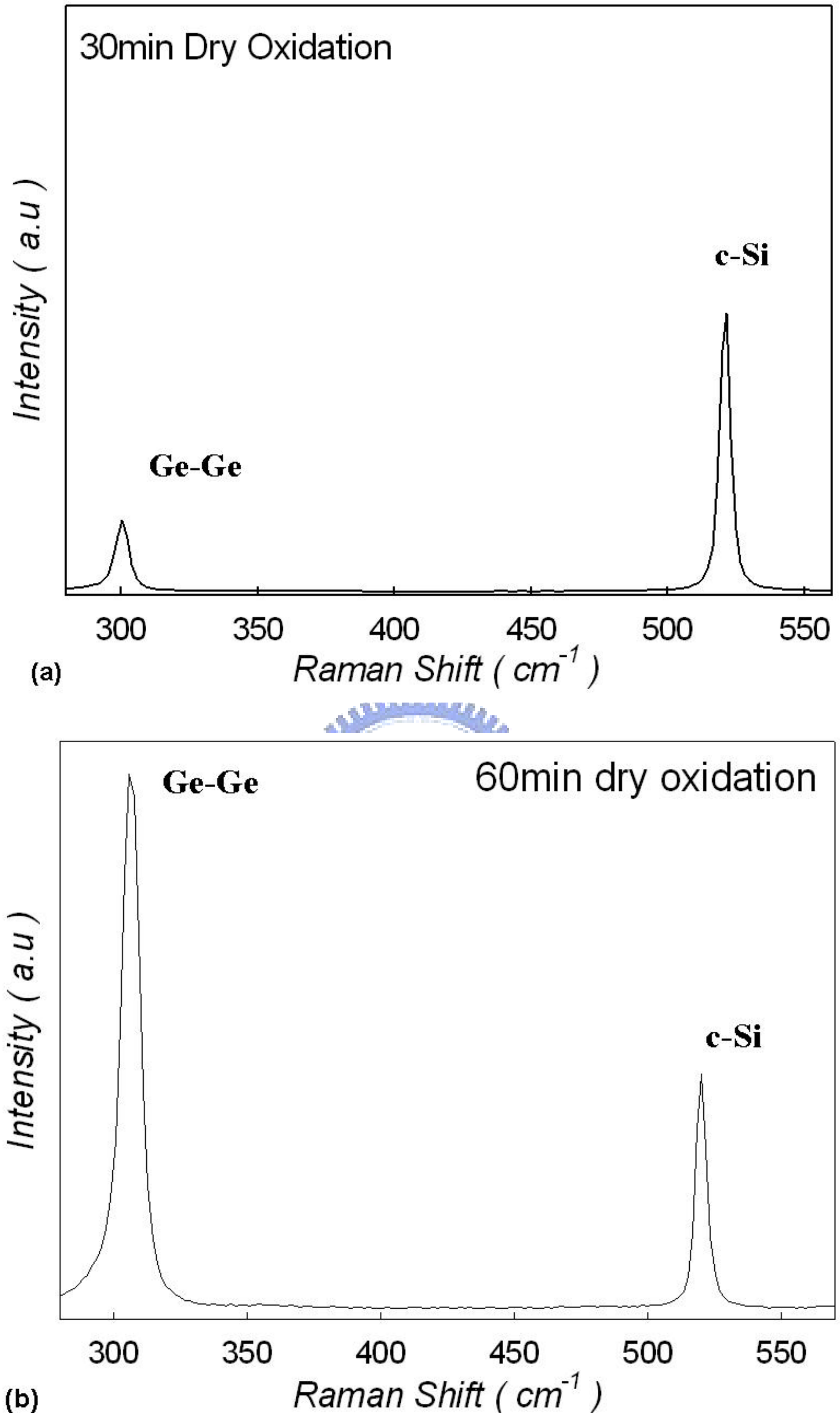


Figure 10-8 The Raman spectra of oxidized SiGeN layer for (a) 30min, and (b) 60min dry oxidation, respectively

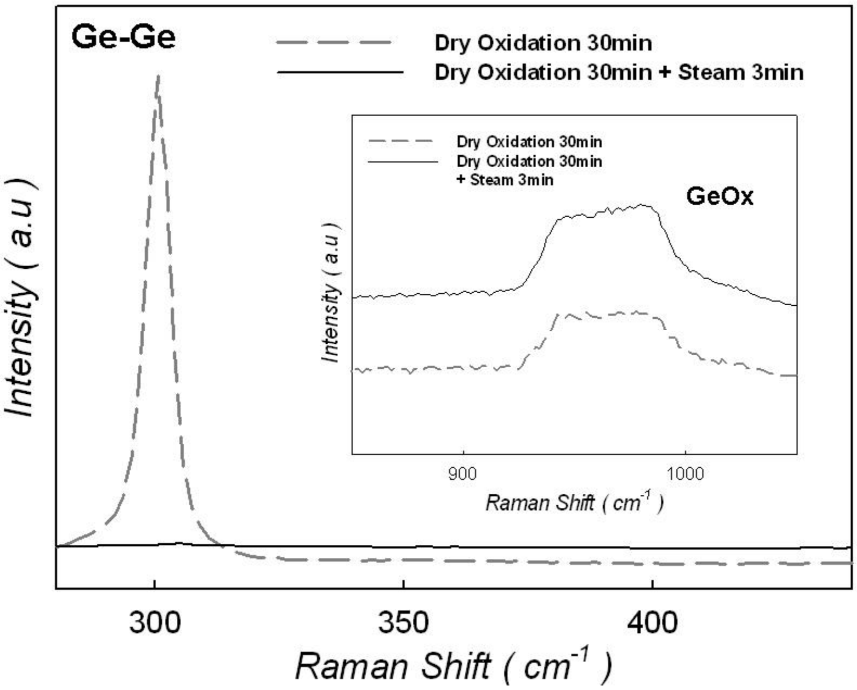


Figure 10-9 The Raman spectra of oxidized SiGeN layer for 30min dry oxidation, and 30min dry oxidation plus 3min steam treatment, respectively

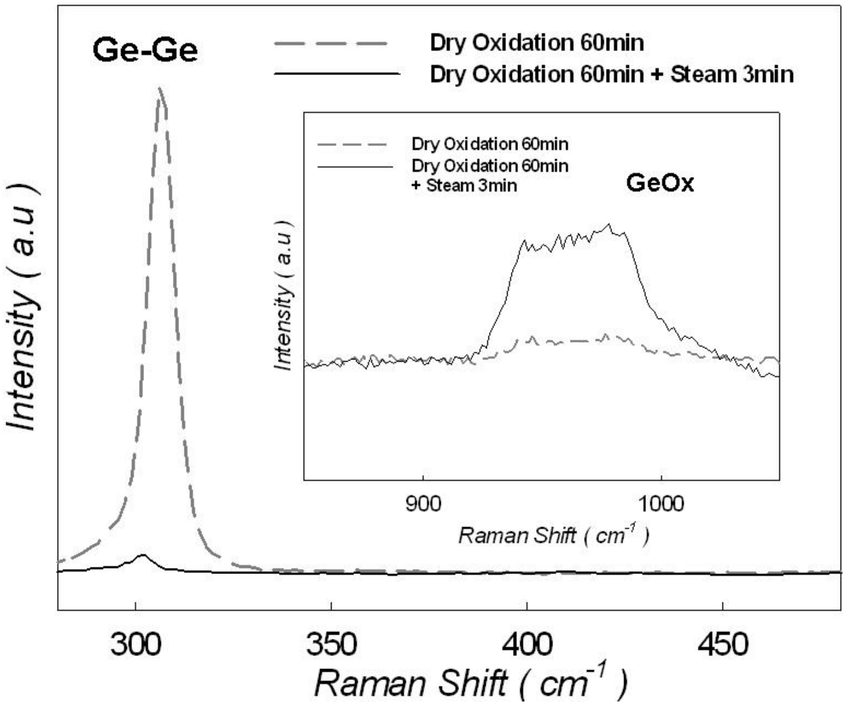


Figure 10-10 The Raman spectra of oxidized SiGeN layer for 60min dry oxidation, and 60min dry oxidation plus 3min steam treatment, respectively

# Chapter 11

# Conclusion Remarks

The electrical characteristics of the F-ions-implanted poly-Si TFTs have been investigated in this study. The fluorine ions segregated ($5\times10^{13}cm^{-2}$) at the poly-Si interfaces by SPC and ELC processes can effectively reduce the trap state density and enhance the device performances. The fluorine ions are spontaneously segregated at the poly-Si interface without an extra oxide layer deposition, thus reducing a process step as compared to the conventional fabrication of the F-ion implanted poly-Si TFTs. Significant improvements in field effect mobility and electrical reliability have been obtained, presumably due to the formation of stronger Si-F bonds instead of weak Si-Si and Si-H bonds in poly-Si layer. The F-incorporated poly-Si TFTs thereby can possess higher hot carrier endurance and improve the device reliability.

The reduction of threshold voltage for SPC and ELC with the incorporation of fluorine ions are 1.46V (from 6.24V to 4.78V) and 1.88V (from 3.07V to 1.19V), respectively. Also, the strong Si-F bonds can prevent hot carrier impact near the drain side, and possess superior electrical reliability over typical poly-Si TFTs. These improvements in electrical characteristics indicate the proposed F ions implantation method is suitable for high performance poly-Si TFT application in the display fields. However, when the fluorine implantation dosages are higher than Si solid solubility, the trap state density could be increased significantly with the implantation dosage increases. The segregated fluorine ions in the poly-Si channel will not passivate the trap states, but generate additional defects to degrade the electrical properties.

Furthermore, the novel poly-Si TFT device with fluorinated $SiO_2$ (FSG) film as the spacers was proposed to enhance the electrical characteristics due to fluorine passivation effect. The poly-Si TFT with FSG spacers exhibits superior endurance against hot carrier effect, leading to improved electrical reliability and suppressed kink effect than the TFT with TEOS $SiO_2$ spacer. In addition, the manufacturing processes are compatible with the conventional TFT process. This indicates our proposed poly-Si TFT with FSG spacers is a promising technology for application in the TFT-LCDs.

The technology to form Ge nanocrystals embedded in SiON stack film with both distributed storage elements and upside blocking oxide has also been demonstrated for memory application in this study. The memory windows after programming are resulted from the Ge nanocrystals embedded in SiON layer. The material of SiGeN as a self-assembling layer is proposed and studied.

Furthermore, the memory window for the stacked structure with Ge distributed storage elements embedded in SiON layer is obviously lager than the MOIOS structures with SiON layer alone or with Ge nanocrystals embedded in $SiO_2$ layer, and even larger than the summation of both. The exhibition of memory windows after programming is resulted from the formation of Ge nanocrystals embedded in SiON layer and extra interface trap states between Ge and SiON film. Therefore, the material of SiGeN as a self-assembling layer has more potential for the application in the nanocrystal nonvolatile memory technology.

The steam treatment is a method to improve the quality of blocking oxide which reducing the thermal budget. Steam treatment makes higher quality of blocking oxide formation, higher efficiency of oxidation. The short dry oxidation plus simple steam treatment makes the memory window compatible with long duration dry oxidation, due to lower leakage characteristics. The completely dry oxidation causes Ge nanocrystal to segregate to the surface of tunnel oxide. However, the memory window of oxidized SiGeN as blocking oxide by the condition of short dry oxidation plus a simple steam treatment is obviously lower, due to the Ge nanocrystal formation far from the tunnel oxide which reduces the efficiency of memory. Hence, the thermal treatment and the blocking oxide formation make different Ge nanocrystal formation mechanism.

# Chapter 12

# Future Work

In this thesis, we have already studied the passivation effect on the application of the poly-Si TFTs, including the fluorine ions implantation and fluorinated silica glass spacer. Furthermore, Ge nanocrystals self-assembling layer (Ge-doped silicon nitride) was also proposed to improve the ability of the charge storage. In fact, the fabrication of the poly-Si TFTs is time consuming. The process variation and uniformity issue are the main failed issues for the fabrication. Furthermore, the low temperature process is not acceptable in the use of the process machines. The successful electrical characteristics were finally obtained after numerous experimental conditions, including the implantation conditions, laser crystallization conditions, and low temperature thin film deposition conditions for three years. In addition, the study on the nonvolatile memory is also filled of difficulties. The fabrication of the proposed Ge nanocrystals self-assembling layer is finished in the self-assembly plasma enhanced chemical vapor deposition system. The recovery of the machine is such a boring event. In addition, this is even dangerous for the use of the poisonous gas. However, the finally results are interesting after hard fabrication. Although the experiment is executed only for three months, the recovery of the machine takes three years. It is firmly convinced that the correct attitude for the experiment is as important as the investment. The further study on the process of the laboratory is important, because we can know what we can do, how we can do. After finishing the academy degree, the detailed electrical characteristics and physical behavior are interesting for the further discuss. For example, the degraded performance for the fluorine-ions-implanted poly-Si TFTs operated at elevated temperature. The Ge contribution to the memory effect is also worth further studying.

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新穎低溫複晶矽薄膜電晶體與前瞻非揮發性記憶體元件之製作與特性研究

Fabrication and Characterization of Novel Low Temperature Polycrystalline Silicon Thin-Film Transistors and Advanced Nonvolatile Memory

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## 專利:

中華民國專利

1. 張鼎張、**涂峻豪**、劉柏村、張俊彥、戴亞翔,「多晶矽層與多晶矽薄膜電晶體的製造方法」,中華民國專利證書號:I 249856 ( 2006)
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美國專利

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