國立交通大學

電機學院IC設計產業研發碩士班

碩 士 論 文

新型紅外線偵測器陣列之互補式金氧半電流讀出積體電路設計與分析及影像應用

THE ANALYSIS AND DESIGN OF NEW CMOS CURRENT READOUT INTEGRATED CIRCUIT FOR INFRARED DETECTOR ARRAY AND IMAGE APPLICATIONS

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指導教授：吳重雨 教授

中華民國 九十六 年 一 月

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摘　要

當積分電容是由一整行共用時，我們必須減小積分端點的總寄生電容，對於減少積分時間與提昇電路操作速度。一個新的像素架構對於減小積分端點的寄生電容是這個論文中被提出，且這一個晶片是首次應用雙重三角取樣（Double Delta Sampling）電路在砷化銦鎵感測器陣列，此電路可用來減小固定樣式雜訊（fixed pattern noise），時脈回饋雜訊和通道電荷注入。有著新的像素架構和雙重三角取樣技術的的32 x 32讀出電路晶片是透過國家晶片系統設計中心委託台灣積體電路製造股份有限公司以0.35微米互補式金氧半導體的製程製造。晶片的面積是2500 μm x 2461 μm和操作在3.3 V電源供應時產生的18 mW功率消耗。整個 32 x 32 電流讀出電路已經被完整地設計、製造與量測完成。這個實驗性的晶片已經成功地證明了新提出的像素架構可以應用在共用積分電容的紅外線偵測器影像系統。

The ANALYSIS AND DESIGN OF NEW CMOS CURRENT READOUT INFRARED CIRCUIT FOR INFRARED DETECTOR ARRAY AND IMAGE APPLICATION

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Abstract

When the integration capacitor is shared by one column, we must decrease total parasitic capacitance of integration capacitor for decreasing integration time and increasing operational speed. A new pixel structure for decreasing total parasitic capacitor of integrated node is proposed in this thesis, and this chip is first application to double delta sampling (DDS) for InGaAs IR detector array. The double delta sampling (DDS) circuits are also used to suppress fixed pattern noise, clock feedthrough noise, and channel charge injection. An experimental chip of the proposed 32 x 32 ROIC with new pixel structure and double delta sampling technique has been fabricated by using 0.35 μm CMOS technology support by Taiwan Semiconductor Manufacturing Company via Chip Implementation Center. Chip size is 2500 μm x 2461 μm, and power dissipation is 18 mW under the power supply of 3.3V. The proposed 32 x 32 ROIC is completely design, fabrication and tested. It has been demonstrated that this chip can be applied in the design of infrared imaging systems with shared integration capacitor by one column.

誌　謝

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得之於人者太多，謹以此篇論文獻給所有關心我的人。

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CHAPTER 1
INTRODUCTION

1.1 Background

The discovery of infrared radiation occurred in 1800 when Sir William Herschel essentially repeated Newton's famous prism experiment and detector heat in the region just above the visible spectrum. The Planck radiation formula was derived in 1900 and quantitatively predicted the amount of energy radiated from a blackbody as a function of temperature and wavelength. During the 1950's and 1960's infrared sensors were used in anti-air missile seeker. At the same time, rapid advances were made in narrow bandgap semiconductors that would later prove to be useful in extending wavelength capabilities and improving sensitivity [1]. Infrared focal plane arrays have been developed for various applications including medical examination [1], astronomy [2], forward-looking infrared (FLIR) system, missile guidance, and night vision equipment.

The rapid advancement in CMOS VLSI with the progress in infrared focal-plane array (IR FPA) technologies like detector material, sensing structure, optics, coolers, readout electronics, image enhancement, and intelligent signal processing results in the revolution of IR image systems to a new generation with significant performance improvement. The application of various developed technologies on the design of IR FPAs has resulted in the advantages of simplified electrical interconnection, reduced signal number leads, higher performance reliability, and simplified package. Some commonly used structures of the three major classes of IR FPAs, namely, hybrid array, monolithic array, and pseudo-monolithic array. In the following, the hybrid array employed in this thesis will be described in detail.

Hybrid Array：

The most commonly used IR FPA structures in the hybrid array [3] are flip-chip and Z-plane technologies [4] as shown in Fig. 1(a) and 1(b), respectively. In Fig. 1(a) involves mating the detector array to a silicon multiplexer where the front side of the detector array is aligned with multiplexer and one contact for each detector is made using a previous deposited set of indium bumps fabricated on both the detector array and on the silicon multiplexer [5], [6] as shown in Fig. 2.

IR detector array chip and silicon readout chip are compounded by the indium bump grown on the aligned pixels of both chips. The detector array can be illuminated from either the front side (with the photons passing through the transparent silicon multiplexer) or backside (with the photons passing through the transparent detector array substrate). This is the mostly used structure in the hybrid array technology, and this method is also used in my work.

In the Z-plane technology shown in Fig. 1(b), the readout chips are stacked one on top of another and then the detector array is mounted to the third dimensional plate on the edge. In the Z-plane structure, one readout chip is used by one channel of detectors so that many electrical circuit techniques like complex input circuit, gain offset correction, analog-to-digital converter, filter, smart and neural function, as well as image signal processing stage can be implemented on the readout chip [7]. To achieve very small detector sizes however, the silicon IC chips must be thinned to very small dimensions. The image resolution is limited by the readout chip thickness. In the application of hybrid array technology, uniformity of indium bumps, chip alignment as well as thermal expansion effect and mechanical damage on the detectors should be considered during the hybridization process [8].

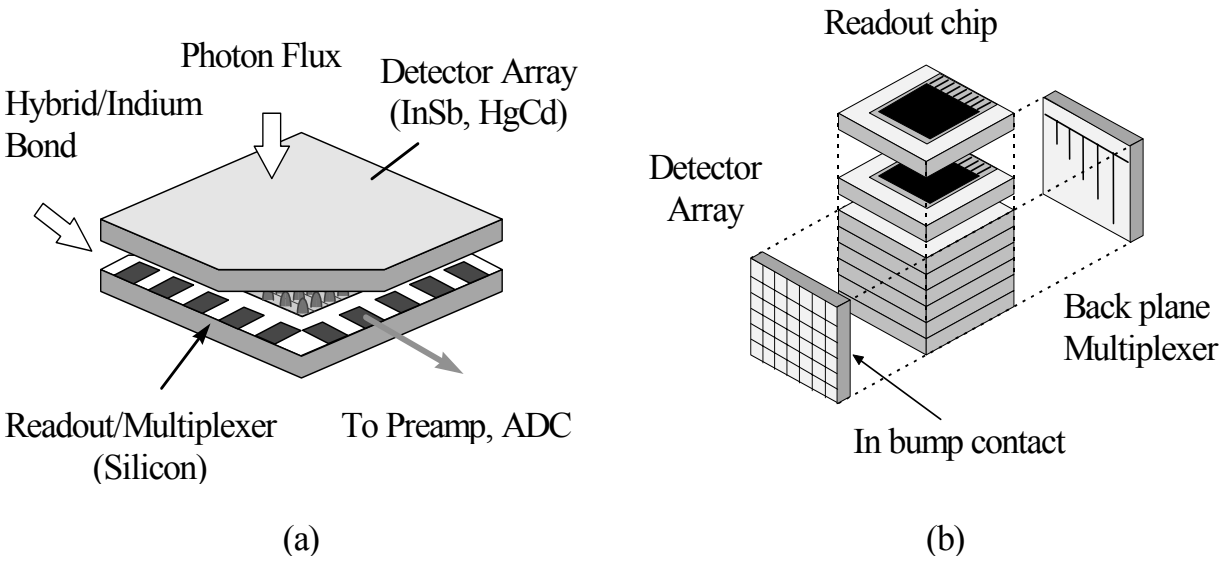


Fig. 1 The technologies of the hybrid array structures: (a) the flip-chip array technology; (b) the Z-plane technology.

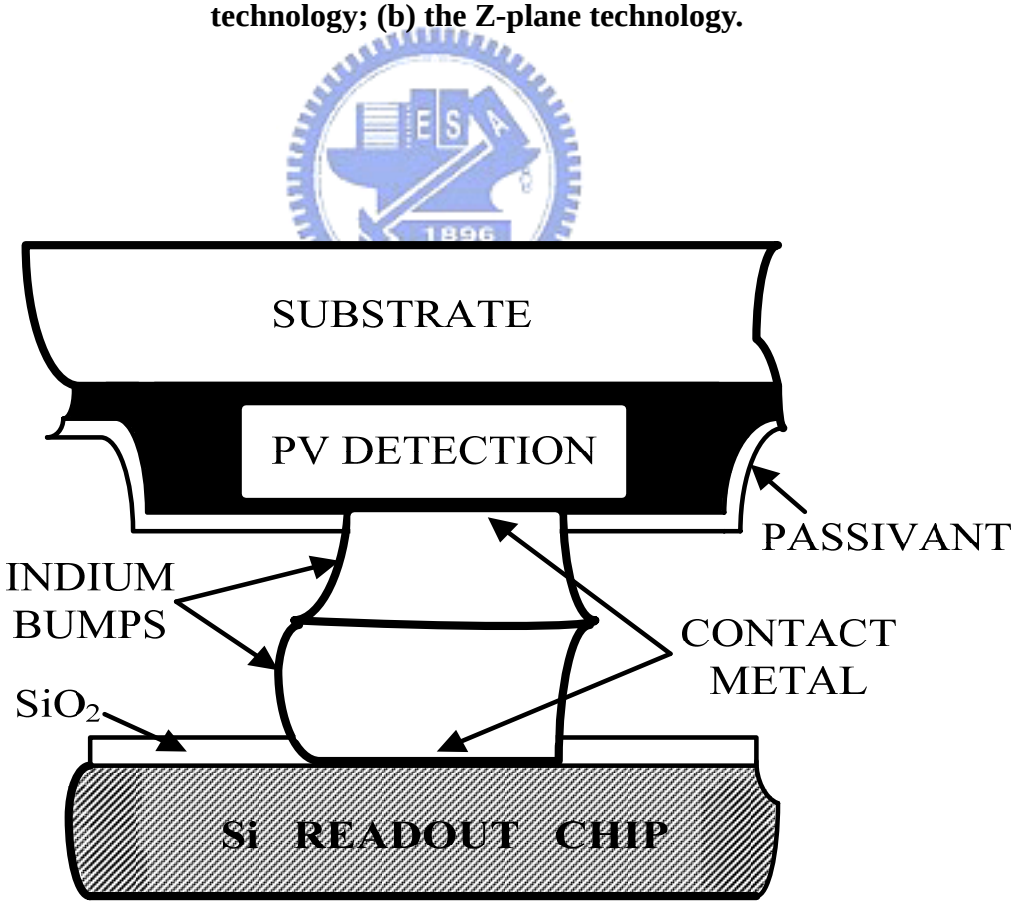


Fig. 2 Hybrid IR FPA interconnect techniques between a detector array and a silicon multiplexer. (Indium bump technique).

1.2 Review on CMOS readout technique for IR FPA

In the design of the infrared (IR) focal-plane array (FPA), high resolution has become a common requirement in many applications. To achieve the optimal overall performance of the IR FPAs, suitable trade-off among circuit performance, power dissipation, chip area, and image resolution should be made. A number of readout structures have been developed for different system application and concern. A high performance readout circuit should provide a stable and near zero detector bias to reduce the dark current and detector noise. It should have low input impedance to obtain high injection efficiency, large dynamic range, large charge capacity, high output swing, and low input referred noise. The integration capacitor is preferred to be placed outside of the pixel to increase its value without increasing the pixel size.

Earlier readout structures, including source-follower-per-detector (SFD) [9], direct-injection (DI) [10], and gate modulation input (GMI) [11] are simple occupy small area, but they cannot satisfy most of the high performance requirement. Later amplifier structures, such as buffered-direct-injection (BDI) [12], and capacitive feedback transimpedance amplifier (CTIA) [13], provide a better performance in term of injection efficiency and detector bias stability with the help of an in-pixel opamp, but their performance is limited with the quality of the opamp that should be implemented in a small pixel area.

A novel approach, buffered gate modulation input (BGMI) [14], provides in-pixel detector current amplification and background flux suppression and places the integration capacitance outside of the pixel, but it also requires in-pixel operational amplifier components for detector bias stabilization. Another approach, current mirroring integration (CMI)[15], [16], satisfies the high injection efficiency and almost-zero detector bias requirement. However, the CMI also requires the integration capacitor to be in the pixel, and therefore has large pixel area, low dynamic range, and low charge storage capacity. A recent novel

approach, switched current integration (SCI) [17], provides large charge storage capacity, stable detector bias, high injection efficiency, and very low input impedance. A number of readout structures have been developed for different system application and concern. In the following, some of commonly used CMOS readout techniques are described below.

1) Direct Injection（DI）[10]：

A simple readout circuit called direct injection (DI) is shown in Fig. 3(a), and the small signal ac equivalent circuit for the DI is shown in Fig. 3(b). The charge carries generated by the detector are directly injected into the input diffusion and potential well under the storage gate where it is accumulated. The direct injection approach has the advantage of simplicity (small area) and high injection efficiencies. The injection efficiency of direct injection can be expressed as

$$\eta(s)_{(DI)} = \frac{gm}{(C_{GS}+C_D)} \cdot \frac{1}{S+\frac{1+gmR_D}{R_D(C_{GS}+C_D)}} \tag{1.1}$$

At the low frequency can be expressed as

$$\eta_{LF\,(DI)} = \frac{gmR_D}{1+gmR_D} \tag{1.2}$$

where gm is the transconductance of MOSFET, C_D is the internal capacitance of detector, and R_D is the internal resistance of detector at the operating voltage. The 3-dB injection bandwidth for detector current can be expressed as

$$f_{BW} = \frac{1+gmR_D}{2\pi R_D(C_D+C_{GS})} \tag{1.3}$$

The origin of these dc offsets between different DI structures is attributed to the MOS threshold voltage. The dc offset variations (about ±250mv) are significant, and cause IR detector to become noisy.

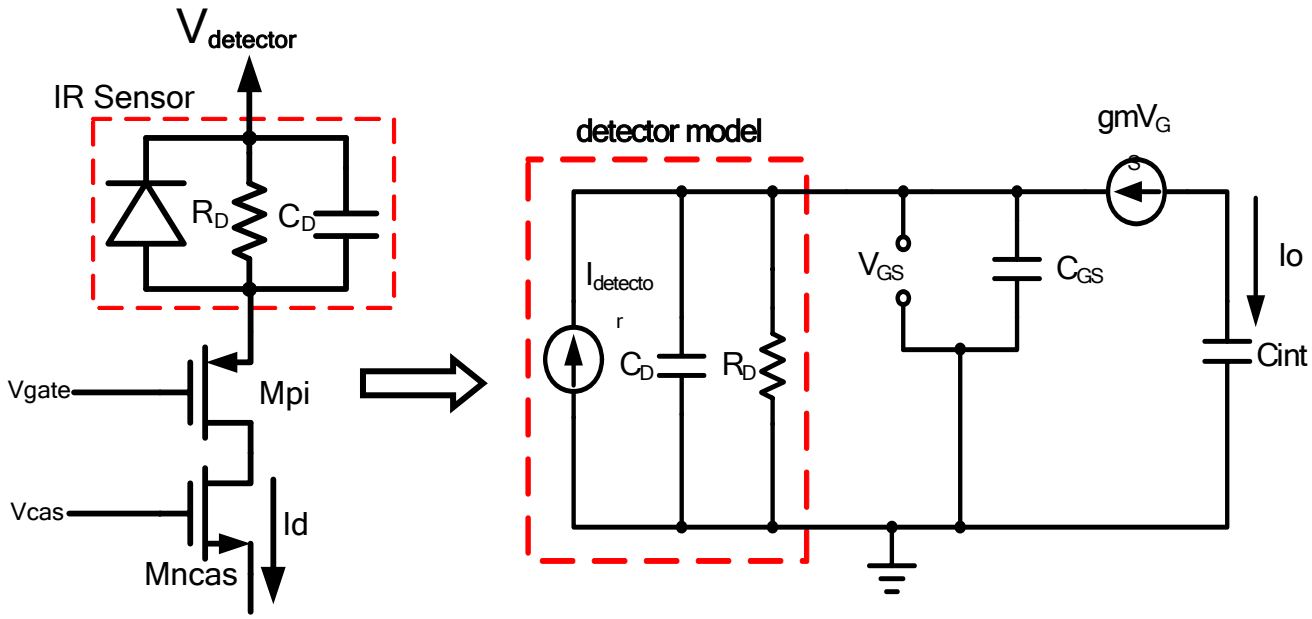


Fig. 3 (a) The direct injection (DI) readout circuit;(b) The small signal ac equivalent circuit for the DI structure.

2) Gated-Modulation-Input（GMI）[11]：

The conventional gate modulation input (GMI) structure is composed with the IR detector, a current mirror which mirrors and amplifies the photo excited current and a integration capacitance C_{int} as shown in Fig. 4. The detector absorbs the infrared flux and generates photo current. The photo excited current flows into M_{load} of the current mirror and amplified by M_{input}. The amplified current then flows into the integration capacitance and transferred it to output voltage. Similar to that in the DI circuit, the injection efficiency of the GMI is dependent on the ration of detector shunt resistance to input of M_{load}. The GMI leads to higher detection sensitivity, high injection efficiency and reduced input referred noise as compared to DI. Due to the simple structure, the pixel pitch can be very small to extend the array size larger. The current gain can be adjusted to suitable value according to the current level by the external adjustable V_{source}. The drawbacks of GMI are that the injection efficiency and linearity are affected by the threshold voltage variation and the noise of the adjustable V_{source}.

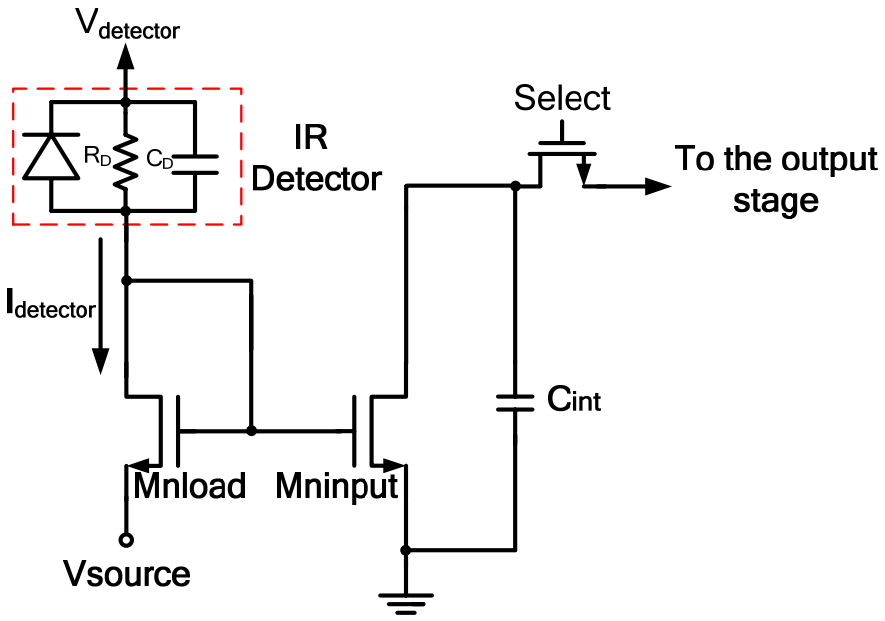


Fig. 4 The gate modulation input (GMI) readout circuit.

3) Buffered Direct Injection（BDI）[12]：

A complex readout circuit called the buffered direct injection (BDI) circuit is shown in Fig. 5 where the circuit structure is similar to the DI except that an additional inverted gain stage with the gain –A is connected between gate node of the common-gate input device and detector node. The BDI can be satisfactorily alleviated by an actively compensated injection structure. In this configuration, the transfer gate is no longer held at a constant potential, but varies in proportion to the photogenerated current of the detector.

Analysis of this circuit shows that it operates like the previously described direct injection circuit but with an effective gm, that is increased by a factor of (1 +A*)* where A is the gain of the amplifier. Another advantage of the buffered direct injection circuit is that the amplifier operating voltages can be controlled, allowing some flexibility in the level of reverse bias voltage applied to the detector. The buffered direct injection circuit achieves improved injection efficiency, better frequency response and lower noise.

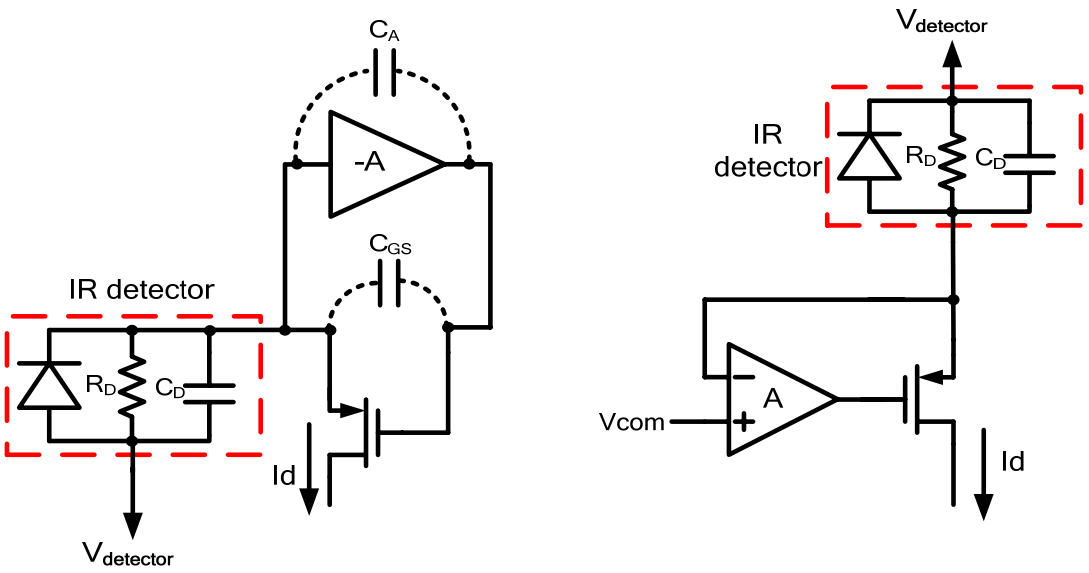


Fig. 5 (a) The buffered direct injection (BDI) readout circuit; (b) The equivalent circuit for the BDI structure.

The injection efficiency of direct injection can be expressed as

$$\eta(s)_{(BDI)} = \frac{(1+A)gm}{C_D + (1+A)(C_{GS}+C_A)} \cdot \frac{1}{S + \frac{1+(1+A)gmR_D}{R_D\left[C_D + (C_{GS}+C_A)(1+A)\right]}} \tag{1.4}$$

At the low frequency can be expressed as

$$\eta_{LF\,(BDI)} = \frac{(1+A)gmR_D}{1+(1+A)gmR_D} \tag{1.5}$$

where C_A is output-input capacitance of gain stage, gm is the transconductance of MOSFET, C_D is the internal capacitance of detector, and R_D is the internal resistance of detector at the operating voltage. The 3-dB injection bandwidth for detector current can be expressed as

$$f_{BW} = \frac{1+(1+A)gmR_D}{2\pi \bullet R_D\left[C_D + (C_{GS}+C_A)(1+A)\right]} \tag{1.6}$$

Clearly, the injection from the BDI structure is much less dependent on the input shunting capacitance and resistance than in conventional direct-injection case. Moreover,

circuit techniques exist which can minimize the output-input coupling capacitance C_A of the gain stage –A such that an increase injection bandwidth is obtained.

4) Capacitive transpedance amplifier（CTIA）[13]：

The schematic of the capacitive transimpedance amplifier (CTIA) is shown in Fig. 6. Where the integration capacitor Cint is placed on the feedback loop of the amplifier with a reset device M-Rst to discharge the integration capacitor and reset the amplifier output to the reference voltage Vcom. The detector bias is also controlled by Vcom through the virtual-short feature of the amplifier. Due to the Miller effect on the integration capacitor, its capacitance can be made extremely small. Unlike DI and BDI, the input impedance of the CTIA is independent of detector current. Thus a good detector bias control can be obtained in the CTIA as the BDI, and the CTIA can achieve very high sensitivity without the change of bias voltage. Although the CTIA can achieve high sensitivity and stable detector bias, the CTIA increase area and power consumption of the inverted gain stage. Usually, the inverted gain stage is implemented by a differential amplifier to provide low offset.

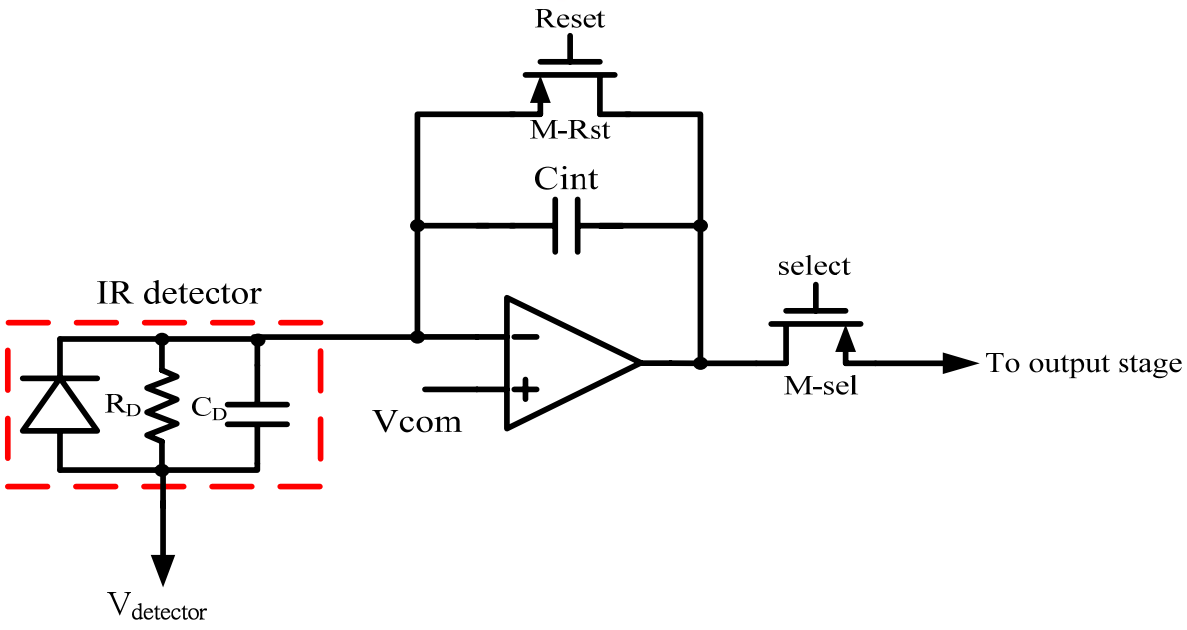


Fig. 6 The capacitive transimpedance amplifier (CTIA) readout circuit.

5) Buffered gate modulation input（BGMI）[14]： 320 × 256

The schematic of the buffered gate modulation input (BGMI) is shown in Fig. 7, and the BGMI structure is improved from GMI. The BGMI consists of a shared buffer as the input stage, unbalance current mirror Mn1 and Mn2, and row select switch M-sel. The shared-buffer technique provides a good bias control for the IR detector, whereas the unbalance current mirror has a large current gain due to the threshold voltage difference Mn1 and Mn2 caused by the intentional device channel length unbalance. Through the use of the threshold voltage, the strict requirement of low noise tunable dc source bias V_{source} in the GMI and the inevitable FPN due to the threshold voltage process dependent variation can be avoided. The current gain $A_{I,BGMI}$ and injection efficiency η_{SBDI} of the BGMI circuit can be expressed as

$$A_{I,BGMI} = \frac{\Delta I_i}{\Delta I_{out}} = \frac{g_{m,Mn2}}{g_{m,Mn1}} \eta_{SBDI} = \sqrt{\frac{K_{Mn2}}{K_{Mn1}}} \cdot \frac{\sqrt{I_{Mn2}}}{\sqrt{I_{Mn1}}} = \sqrt{\frac{K_{Mn2}}{K_{Mn1}}} \sqrt{K_{Mn2}} \left(\frac{1}{\sqrt{K_{Mn1}}} + \frac{\Delta V_T}{\sqrt{I_{Mn1}}} \right) \quad (1.7)$$

$$\eta_{SBDI} = \frac{(1+A) g_{m,Mn1} R_D}{1 + (1+A) g_{m,Mn1} R_D} \quad (1.8)$$

The threshold voltage difference ΔV_T is geometry dependent and thus is very stable. Unlike the GMI circuit, no strict source bias voltage control is required in the BGMI circuit. The current gain of BGMI circuit is immune to threshold non-uniformity and noise of the source bias voltage. It can also be adaptively controlled by different IR background input flux. This high front-stage current gain makes the downstream circuit and system noise contribution extremely low. It results in a low input referred noise. Moreover, BGMI circuit can operate with a larger integration capacitance compared to DI and BDI and still obtain low noise performance and high charge detection sensitivity.

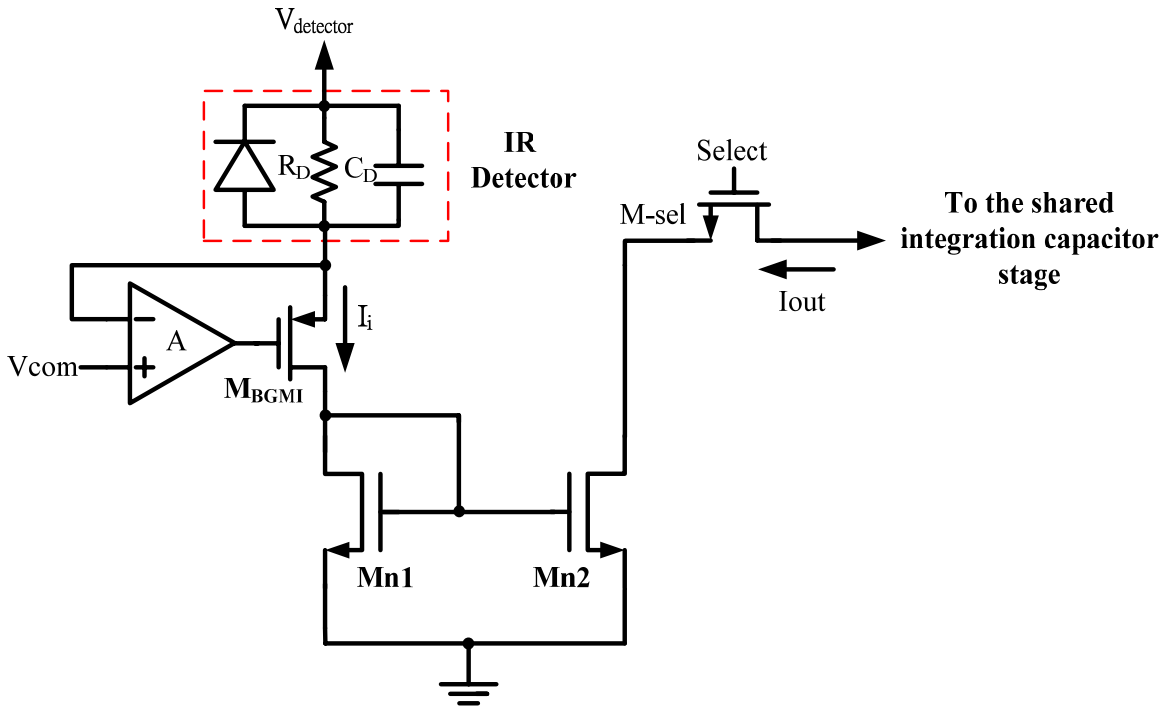


Fig. 7 The buffered gate modulation input (BGMI) readout circuit.

6) Current mirroring integration (CMI) [15], [16]：

The schematic of the current mirroring integration (CTIA) is shown in Fig. 6. The detector current is copied very linearly and accurately to an off-pixel integration capacitor by the help of a current feedback structure implemented with a high-swing NMOS current and a PMOS current mirror. The current feedback structure forces the drain currents of M_{P1} and M_{P2} to be similar, while the MN5 and MN6 pair copies the current to the outside of the cell when the pixel is selected by turning M-sel on. Since the integration capacitor can be placed outside of the pixels, its value can be selected as large as required for high charge storage capacity and high dynamic range.

The CMI structure provides a stable bias voltage, and it can be expressed as

$$V_{detector} = V_{DD} - V_{bias} + \left(\frac{K_P}{K_n} \cdot \Delta V_{tp} + \Delta V_{tn} \right) \tag{1.9}$$

The input impedance of the CMI can be expressed as

$$Rin = \frac{\left(\frac{gm_{P1}}{gm_{P2}} \cdot \frac{gm_{N4}}{gm_{N2}}\right) - 1}{gm_{P1}} \tag{1.10}$$

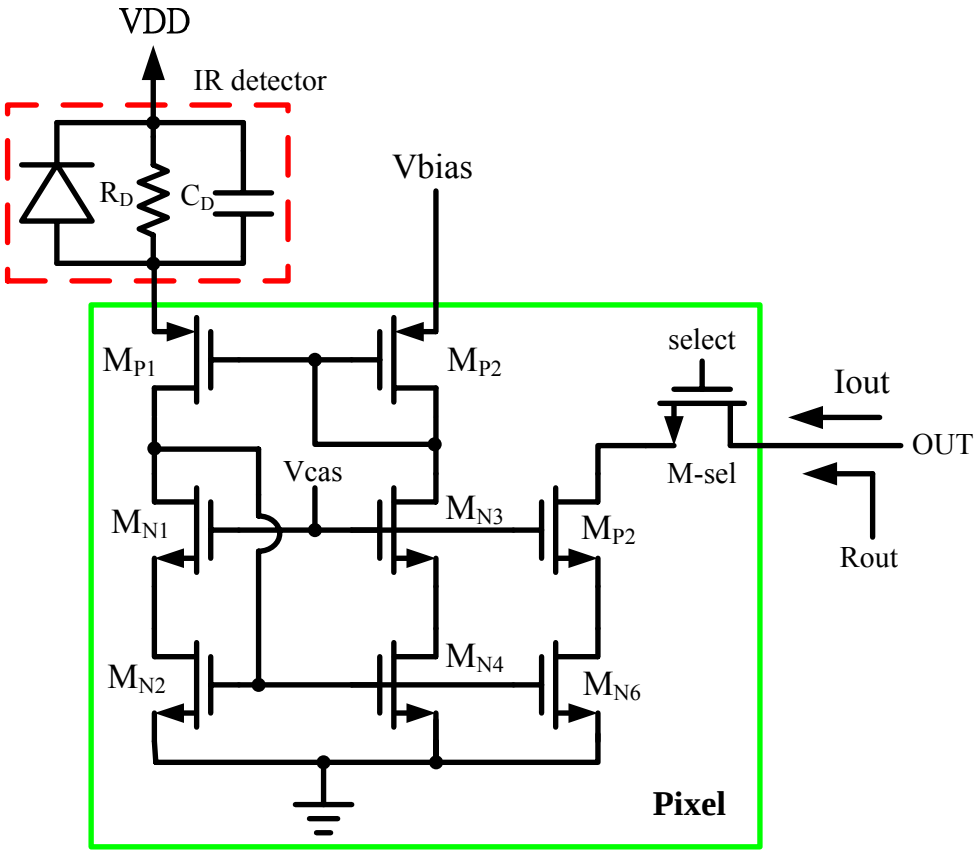


Fig. 8 Structure of the Current Mirroring Integration circuit.

The CMI technique provides high injection efficiency, very low input impedance, and stable detector bias while occupying small area.

1.3 Motivation

Infrared focal plane arrays have been developed for various applications, and the readout circuit is a very important interface in the infrared image system. Generally, infrared image system is very expensive, and has difficulties to obtainment because the high performance

readout circuit is commonly application to military. The readout circuit array is combined with the InGaAs IR detector array which developed by Chunghwa Telecom Lab to compose an IR image system. The detector array and the readout circuit array will be combined with the indium bond.

In this thesis, this chip is first application to double delta sampling (DDS) for InGaAs IR detector array, and we increase variable circuit to change sampling time at choice for all situations. The DDS circuit is composed of column sampling circuit and output correlated double sampling circuit, and it can reduce fixed pattern noise, clock feedthrough noise, and reset noise, and this technique can efficiently increase resolution and output swing. In my work, the CDS stage is shared by all column sampling circuits, and this method has no disadvantage on column CDS circuits. The disadvantages of column CDS circuits generally have some offset variation of output voltage. The output signal with offset variation of CDS circuits generates a column-wise fixed pattern noise. Because a column-wise FPN is much more conspicuous than a random fixed pattern noise, it is hard to eliminate. In this chip, output CDS circuit is shared; it does not generate a column-wise fixed pattern noise. Using the proposed input stage, the readout performance in the high-resolution large-format IR FPA can also be improved.

1.4 Thesis organization

In chapter 2, operational principles, architectures, circuit implementations, and simulation results of 32 x 32 and 320 x 256 IR FPA are described. In chapter 3, the circuit design and simulation of biochemical chip are presented. In chapter 4, measurement results of 32 x 32 readout chip and biochemical chip are presented. Finally, the conclusions and future works are given in chapter 5.

CHAPTER 2
ARCHITECTURE AND CIRCUIT DESIGN

2.1 Chip architecture

In the following, chip architectures of 32 x 32 IR FPA and 320 x 256 IR FPA are described below.

2.1.1 The chip architecture of 32 x 32 IR FPA

The block diagram of the proposed 32 x 32 IR FPA is shown in Fig. 9. The integration capacitor is put in the column sampling circuit to perform off-pixel integration. The row decoder and row counter on the left side of cell array are used to generate the control signals for row switches. The column decoder and the column counter on the top side of cell array are used to generate the control signals for the column reset operation, column switches, double delta sampling (DDS) circuit, and row counter. Each column of the cell array has a column readout circuit to lower the leakage current in the column bus and the column sampling circuits to reduce the fixed pattern noise.

The column readout circuit generates two analog output voltages. One is the signal proportional to the illuminative intensity of the 32 x 32 IR FPA whereas the other is the signal proportional to the reset voltage at the integration capacitor. The output CDS circuit is used to drive the external loads and perform the CDS operation. The image information is transformed as the photocurrent in the cell array by using the IR detector. The photocurrent is delivered to the column bus and converted into a voltage signal proportional to the illuminative intensity of image after the current integration outside the pixel. The photo-signal

and reset signal are used for the operation of the DDS.

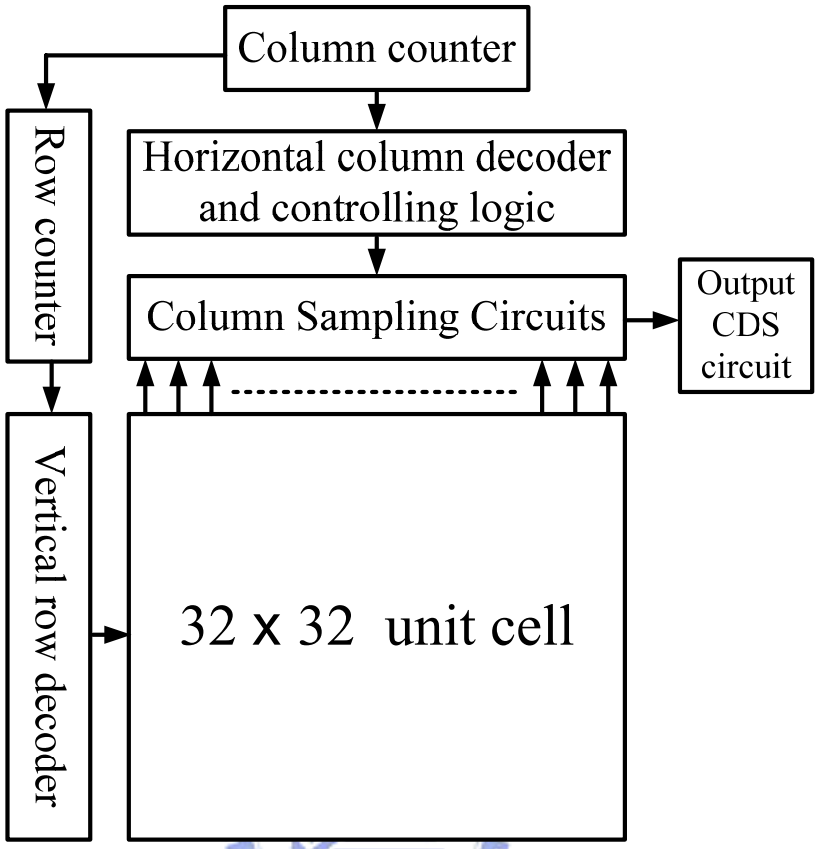


Fig. 9 The block diagram of 32 x 32 IR FPA.

2.1.2 The chip architecture of 320 x 256 IR FPA

The block diagram of 320 x 256 infrared focal plane arrays is shown in Fig. 10. There are three important parts of the analog circuits in this structure which are: the unit cell, column CDS stage and dynamic discharge output stage as the common output stage. There are four important parts of the digital circuits in the proposed structure which are: column counter, row counter, horizontal column decoder and vertical row decoder. Every unit cell will combine with the detector by an indium bond. The negative feedback amplifier is separated into two parts: half of the amplifier is shared by each row as the common left half and the other half is contained in every single pixel. By this arrangement the chip area and the power

dissipation will decrease. When the detector absorbs infrared flux, the photo-generate current flows into the current mirror in the unit cell. Then the mirrored and amplified current flows into the integration capacitance and transferred to voltage. The integrated signals from pixels in the same row are sampled to the CDS stages one row at one time controlled by the vertical row select logic. There are column CDS stage are shared by one column. The selected CDS signal is sampled to the common output stage column by column.

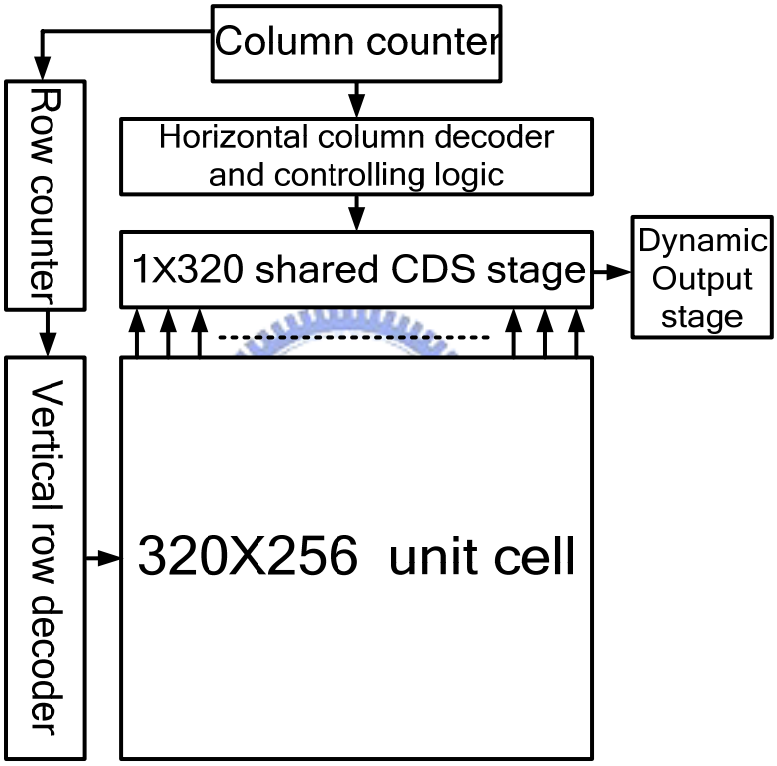


Fig. 10 The block diagram of 320 x 256 IR FPA.

2.2 Circuit implementation

In the following, circuit implementation of 32 x 32 IR FPA and 320 x 256 IR FPA are described below. The 32 x 32 IR FPA is using delta double sampling technique to reduce fixed pattern noise and reset noise. Similarly, the 320 x 256 IR FPA is using correlated double sampling (CDS) technique to reduce fixed pattern noise.

2.2.1 The circuit implementation of 32 x 32 IR FPA

The 32 x 32 IR FPA is composed of united cell stage and double delta double sampling (DDS) circuit. In the following, the united cell stage and delta double sampling circuit in this chip will be described in detail.

The united-cell input stage of 32 x 32 IR FPA：

The conventional united-cell stage of SCI readout structure and the proposed unit-cell stage are shown in Fig. 11 (a) and (b) respectively. When the integration capacitance is shared by one column, we must decrease total parasitic capacitance for decreasing integration time and increasing operational speed. For this reason, the Mrow is placed between MC2 and MC4 because this placing can decrease total parasitic capacitance of integration node to 43%. The readout speed can be increased by replacing integration cap by smaller one under constant integrated current (Io).

In the united-cell input stage of Fig. 11 (b), a single stage opa-amp and a cascode current mirror is used. As shown in Fig. 11, the single stage opa amp of input stage circuit formed by the MOS devices Mpu1, Mpu2, Mpu3, Mnu1, and Mnu2 in each pixel and the cascode current mirror circuit formed by the MOS devices MC1, MC2, MC3, and MC4 in each pixel. Due to the function of the differential amplifier, the detector bias at the anode of the IR detector can be stabilized to Vcom through the virtual ground and the input impedance of the input MOS device MG can be decreased to obtain high injection efficiency. The high injection efficiency, good detector bias stability, low noise, and good threshold uniformity can be achieved in the unit-cell input stage. The photo-current I_I signal flowing through MG of the input circuit is further mirrored to the next stage through the high-swing cascode current mirror MC1-MC4 as shown in Fig. 11 (b). The current mirror can improve the detection sensitivity and avoid the noise coupling effect to the input stage circuit. Moreover, as compared to the conventional cascode current mirror, the high-swing cascode current mirror

[18] increases output impedance and ratio accuracy while decreasing the required mirror output voltage to keep the output MOS devices in the saturation region.

The current ratio of Io to I_1 of the current mirror is determined by the dimension ratio of the MOS devices MC1 and MC2, which is very stable [19]. The current mode readout from united-cell to column readout circuit avoids the voltage swing in the highly capacitive column bus. The optimal gain of the current mirror can be determined for different input signal levels to achieve a maximum signal-to-noise ratio without integrating saturation on the capacitor. In the design, the current gain is 4. The amplified pixel current signal at the output of the current mirror is switched to the column sampling circuits through the MOS switch Mrow controlled by the row select clock *Row*.

The injection efficiency of the united-cell stage at the low frequency can be expressed as

$$\eta_{LF} = \frac{(1+A)\cdot gmR_D}{1+(1+A)\cdot gmR_D} \tag{2.1}$$

The input impedance of united-cell stage can be expressed as

$$Rin = \frac{1}{gm\times(1+A)} \tag{2.2}$$

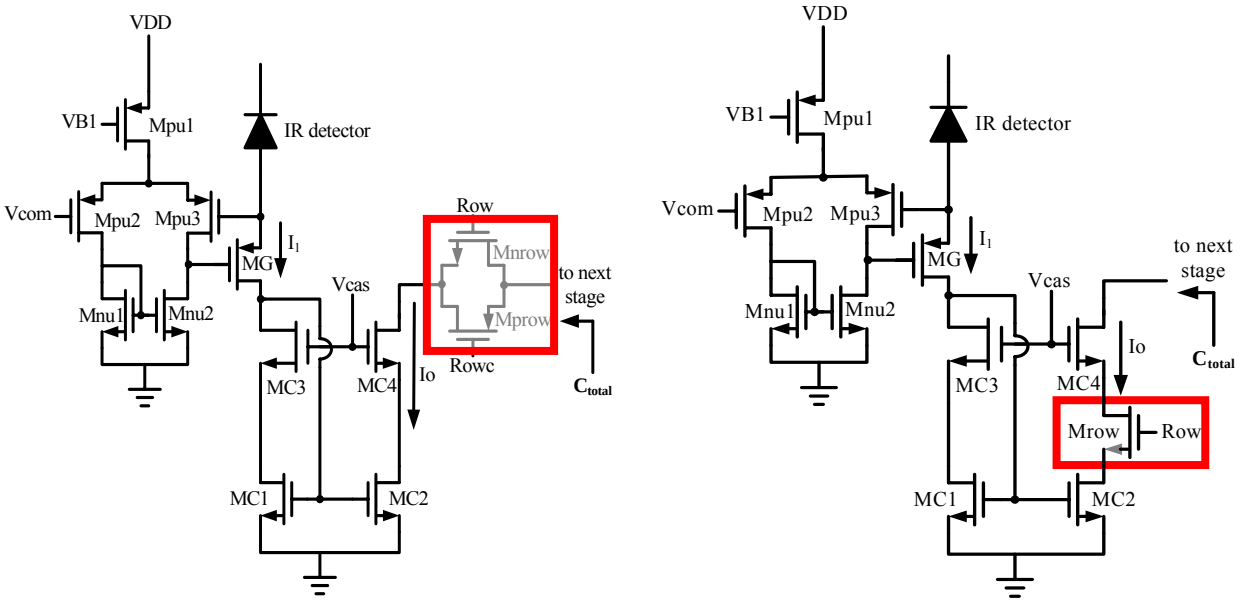


Fig. 11 The united-cell stage (a) conventional united-cell stage of SCI readout structure (b) proposed new united-cell stage.

To Calculate total integrated capacitor：Cox = 4.5 fF

Conventional united-cell stage

$$C_{total} \cong 32 \bullet (C_{SG(Mprow)} + C_{GD(Mnrow)})$$

$$= 32 \bullet \left[2 \bullet (\frac{1}{2} W \bullet L \bullet Cox + W \bullet Cox) \right]$$

$$= 32 \bullet \left[2 \bullet (\frac{1}{2} 2 \bullet 0.35 \bullet 4.5fF + 2 \bullet 4.5fF) \right]$$

$$= 667.8fF$$

New united-cell stage

$$C_{total} \cong 32 \bullet C_{GD(MC4)}$$

$$= 32 \bullet (W \bullet Cox)$$

$$= 32 \bullet (2 \bullet 4.5fF)$$

$$= 288fF$$

The total parasitic capacitance decreases to 43% through using new united-cell stage. The simulation results of reset signal and integrated signal of conventional united-cell stage of SCI structure and new united-cell stage under integrated time = 72.5 us and photocurrent = 2.5 nA are shown in Fig. 12 (a) and (b) respectively. In Fig. 12 (a), the integrated voltage is 1.08V. In Fig. 12 (b), the integrated voltage is 2.41V. It can demonstrate that the new united-cell stage have smaller total parasitic capacitance under the same integration time.

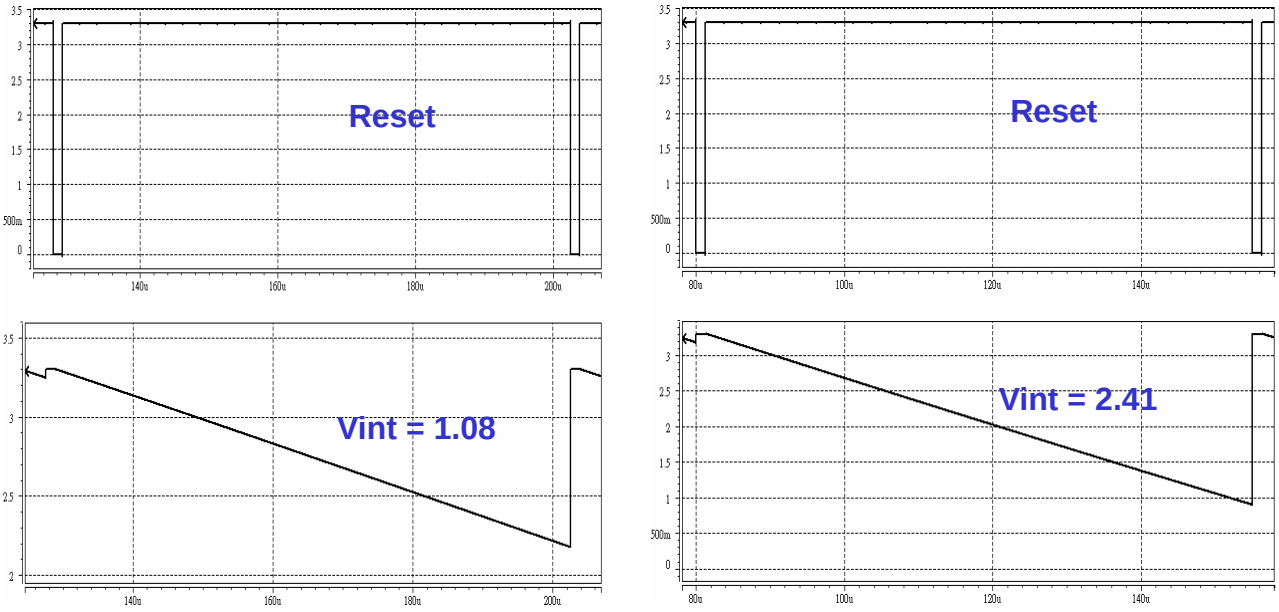


Fig. 12 The simulation results of the reset signal and integrated signal (a) conventional united-cell stage of SCI structure (b) new united-cell stage.

Double Delta Double Sampling (DDS) Operation circuit

Due to the process non-uniformities, the differences between the threshold voltages of transistors of analog buffer cause a column FPN. To compensate this column FPN, the readout chain contains a circuit named double delta sampling (DDS) [20], [21], [22]. The typical DDS circuit is shown in Fig. 13.

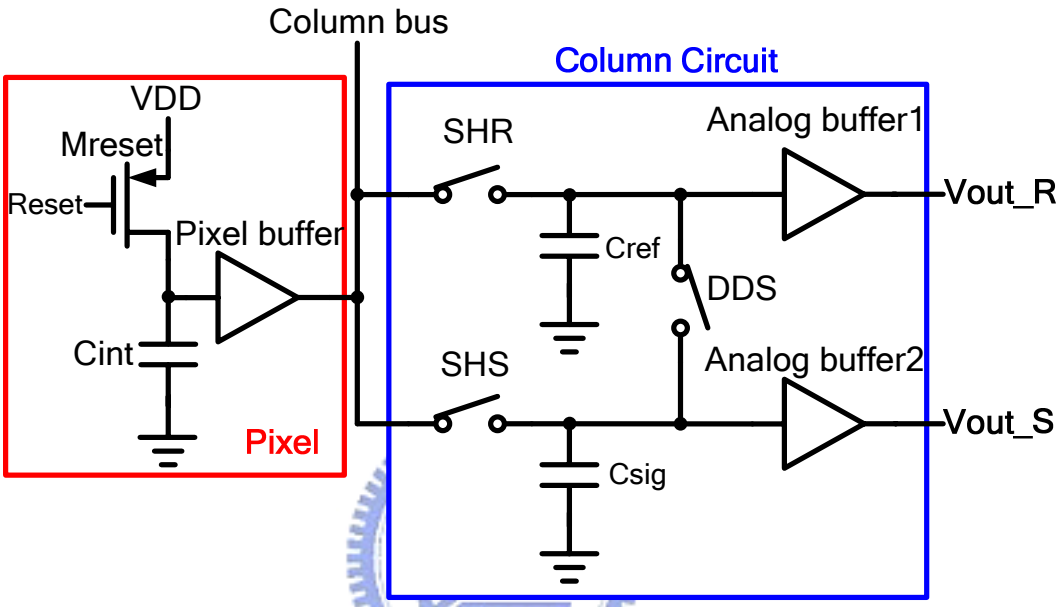


Fig. 13 Typical double delta sampling circuit.

The signal and reset levels are sampled to sample-and-hold capacitors Cref and Csig respectively. The difference between Vout_R and Vout_S is equal to Vref – Vsig + Δ1. Then, the DDS switch is activated and capacitors Cref and Csig are short-circuited. At this time, the difference between Vout_R and Vout_S is equal to Δ2 directly. By the subtracting this reference level from the previous reading, the offset due to threshold voltage variations is removed (Δ = Δ1 – Δ2). The timing of DDS process is shown in Fig. 14.

The output voltage ΔVo can be expressed

$$\Delta Vo(n+1) = [Vout\_R(n) - Vout\_S(n)] - [Vout\_R(n+1) - Vout\_S(n+1)] \quad (2.3)$$

$$= (Vref - Vsig) + (\Delta 1 - \Delta 2) \quad (2.4)$$

if $\Delta 1 = \Delta 2 \Rightarrow \Delta Vo(n+1) = Vref - Vsig$ (2.5)

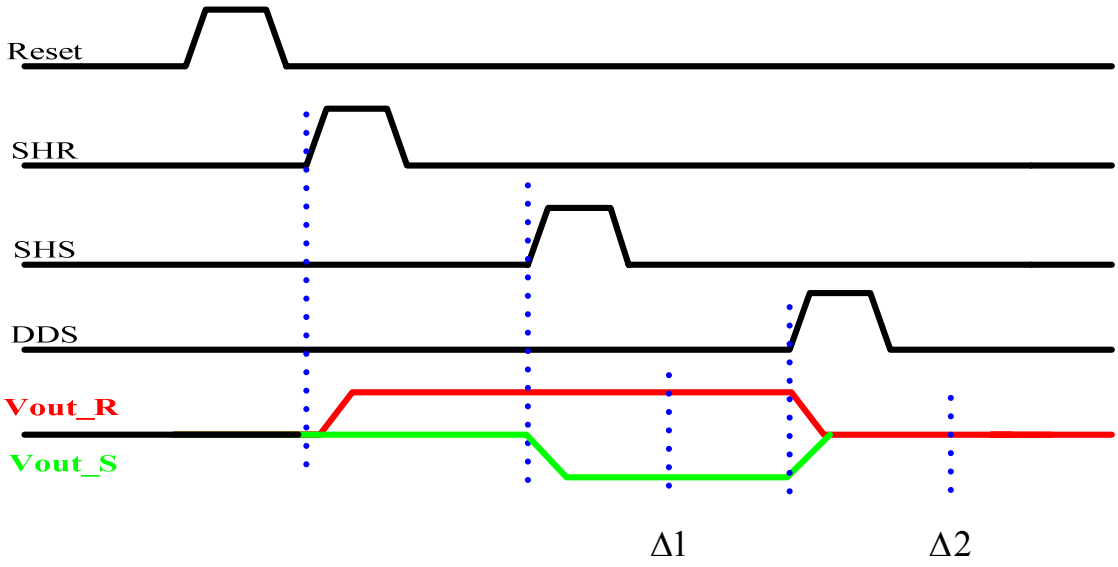


Fig. 14 The timing of typical double delta sampling circuit.

The DDS operation circuit in my work is shown in Fig. 15. The DDS is composed of column sampling circuit and output correlated double sampling circuit. The column sampling circuit is used in each column whereas the output CDS circuit is shared by all columns sampling circuit.

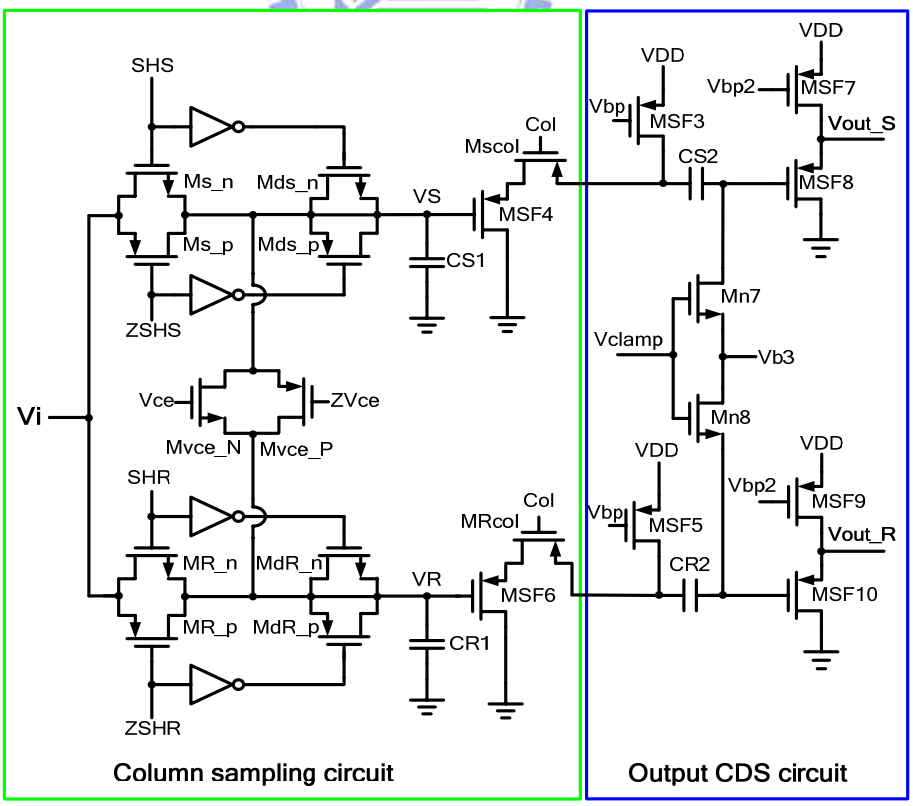


Fig. 15 The improved DDS circuit.

In the column sampling circuit as shown in Fig. 15, the devices of Ms_n, MR_n, Ms_p, and MR_p controlled by the signals of SHS, SHR, ZSHS, ZSHR, respectively, are sampling switches whereas Mvce_N and Mvce_P controlled by Vce and ZVce are the equalization switch. The signals generated by the integration of photocurrent and the reset signal transferred through the source follower are sampled by the devices of Ms_n, Ms_p, and MR_n, MR_p respectively. The double delta sampling circuit is used to remove offsets due to the column source follower, and hence reduces column-to-column fixed pattern noise.

Both the effects of clock feedthrough and channel charge injection resulted from the sampling operation of MS and MR in the original DDS circuit will degrade the performance of signal readout. In the improved DDS circuit of Fig. 15, the effect of signal-dependent channel charge injection caused by Ms_n, MR_n, Ms_p, and MR_p during the falling edges of SHS, ZSHS, SHR, and ZSHR is reduced by the dummy switch Mds_n, Mds_p, MdR_n, and MdR_p with their drain and source connected together. The dummy switch size of Mds_n, Mds_p, MdR_n, and MdR_p is designed to be about one half of the size of Ms_n, MR_n, Ms_p, and MR_p, respectively.

The signals after the sampling are held at the nodes of VS and VR until they are readout to the output CDS circuit when the column switches Mscol and MRcol are on. Since the column readout sampling is performed simultaneously in each column and the sampled column signals are readout to the output CDS circuit successively, the signal from the last column is held for the longest time that is almost equal to the integration time. The held signal voltages at the last column will be decreased by the leakage currents at the nodes of VS and VR. An extra capacitor of 250fF is added to the nodes of VS and VR to decrease the effect of leakage current. The extra capacitor of 250fF is determined by the leakage current I_{leak} =0.4p/um at the nodes of VS and VR, the gain G_{PGA}= 2 of the programmable gain amplifier (PGA), the total capacitances (C_{total}) at the nodes of VS and VR, and the integration time Tint.

The equation can be represented as

$$C_{total} \cdot V_{1LSB} = G_{PGA} \cdot (I_{leak} \cdot Tint) \tag{2.6}$$

The clamp signal in the output CDS circuit is then turned on to clamp the gate voltages of MSF8 and MSF10 to Vb3. Then, Mscol and MRcol are on to transfer the signal from the column sampling circuit to the output CDS circuit. Finally, Mn7, Mn8, Mvce_N, and Mvce_P are on, the voltage at both nodes of VS and VR of becomes $\frac{VS+VR}{2}$. If no loss in the stored charges of the capacitor, then the voltage change at the capacitors of CS2 and CR2 are transferred to the output node of the output source follower composed of MSF7 and MSF8 (MSF9 and MSF10) as shown in Fig. 15.

Thus we have

$$Vout\_S = \frac{\Delta V}{2} + Vb3 + V_{noise} + \frac{1}{2}(V_{SG(MSF4,Vce)} - V_{SG(MSF4,Vclamp)}) + V_{SG(MSF8)} \tag{2.7}$$

$$Vout\_R = -\frac{\Delta V}{2} + Vb3 + V_{noise} + \frac{1}{2}(V_{SG(MSF6,Vce)} - V_{SG(MSF6,Vclamp)}) + V_{SG(MSF10)} \tag{2.8}$$

$$Vout\_S - Vout\_R = \Delta V + \left[\left(V_{SG(MSF4,Vce)} - V_{SG(MSF4,Vclamp)}\right) + \left(V_{SG(MSF6,Vce)} - V_{SG(MSF6,Vclamp)}\right)\right] + \left(V_{SG(MSF10)} - V_{SG(MSF8)}\right) \tag{2.9}$$

where V_{noise} is the effect of clock feedthrough on the node of VS and VR of Fig. 15 when the MOSFET of Mvce_N and Mvce_P are on, the $V_{SG(MSF4,Vce)}$ and $V_{SG(MSF6,Vce)}$ are under the condition that the Vce is high. The $V_{SG(MSF4,Vclamp)}$ and $V_{SG(MSF6,Vclamp)}$ are under the condition that the Vclamp is high.

The variation of threshold voltage can be reduced by DDS circuit, but $V_{SG(MSF4,Vce)}$ and $V_{SG(MSF4,Vclamp)}$ can not cancel each other perfectly due to the body effect, so as $V_{SG(MSF6,Vce)}$ and $V_{SG(MSF6,Vclamp)}$. As may be seen from (2.7) and (2.8), the CDS operation is realized in the output CDS circuit. In the equation (2.9), the two output signals are sent out and subtracted each other by the subtraction circuit in the off-chip data acquisition (DAQ) card.

2.2.2 The circuit implementation of 320 x 256 IR FPA

The 320 x 256 IR FPA is composed of united cell stage, column CDS stage, and dynamic discharge output stage. In the following, the united cell stage, column CDS stage, and dynamic discharge output stage in this chip will be described in detail.

The united-cell input stage of 320 x 256 IR FPA：

In the input stage, a single stage opa-amp and a cascode current mirror is used. The Fig. 16 shows the unit cell combines with the common left half circuit. As shown in Fig. 16, the share-buffered direct-injection (SBDI) input circuit formed by the MOS devices Mpu1, Mpu2, and Mnul in each pixel and the common left half circuit formed by the MOS devices Mps1, Mps2, and Mns1 and shared by all the pixels in one column. In the shared common left half circuit, three common output bias lines Vb1, commonS, and commonG are connected to the SBDI input circuits of all the pixels in the same column. The total power dissipation of the unit-cell input stage can be kept small because the bias current of the SBDI input circuit in each pixel is low, and the chip area can be kept small.

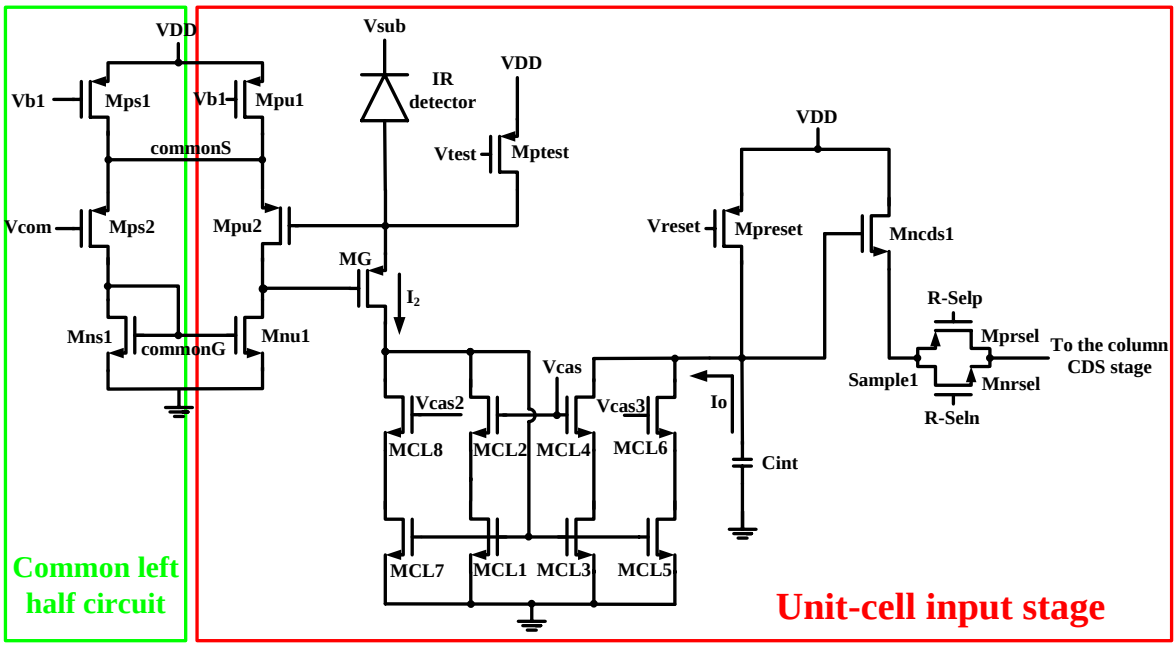


Fig. 16 The united-cell stage of 320 x 256 IR FPA.

The amplifier is connected as negative feedback type, and the detector bias at the anode of the IR detector can be stabilized to Vcom and adjusted by adjusting Vcom through the virtual ground. The input impedance of the input device MG can be decreased to obtain high injection efficiency. The photo-current I_2 signal flowing through MG of the input circuit is further mirrored to the next stage through the high-swing cascode current mirror with variable current gain (MCL1-MC8) as shown in Fig. 16.

In normal case (Vcas = Vcas2 = 0.8V, Vcas3 = 0V), the current gain is 6. If the readout circuit is operated in weak current (below 500p), the devices of MCL5 and MCL6 can increase the current gain from 6 to 60 through controlling bias Vcas2 and Vcas3 to turning on MCL5 MCL6 and turning off MCL7 MCL8 (Vcas = Vcas3 = 0.8V, Vcas2 = 0V). The amplified pixel current signal at the output of the current mirror is switched to the column sampling circuits through the MOS switch Mprsel and Mnrsel controlled by the row select clocks R-selp and R-seln respectively. The injection efficiency and input impedance are the same in equation (2.1) and (2.2). The integration capacitance is chosen small to increase the readout speed. The detailed device sizes of the unit cell are list in Table I.

Device	W/L (um/um)
Mpu1 Mps1	0.5/2.5 M=1
Mpu2 Mps2	0.5/0.7 M=1
Mnu1 Mus1	1/1.8 M=1
MG	1/1 M=1
MCL1 MCL2	0.5/0.4 M=1
MCL3 MCL4	3/0.4 M=3
MCL5 MCL6	3/0.4 M=7
MCL7 MCL8	0.5/0.4 M=2
Mpreset	0.5/0.4 M=1
Mncds1	2.5/0.35 M=6
Mnrsel	1/0.35 M=1
Mprsel	1.5/0.35 M=1
Cint	10fF

Table I The device parameters of the unit cell.

The column CDS stage of 320 x 256 IR FPA：

In the correlated double sample (CDS) stage, as shown in Fig. 17, the NMOS Mncds2 with the dc gate bias Vbn is the NMOS current source load of the source follower Mncds1 when the row switch is ON. The correlated double sampling (CDS) function is realized by the row switch Mnrsel and Mprsel, the clamp device Mnclp, and the AC coupling capacitor Ccds. The PMOS devices Mpcds1 and Mpcds2 form a P-type source follower, and the Mpcds1 of Nth column is turn on when Nth column is selected. By this arrangement the power dissipation can be reduced substantially.

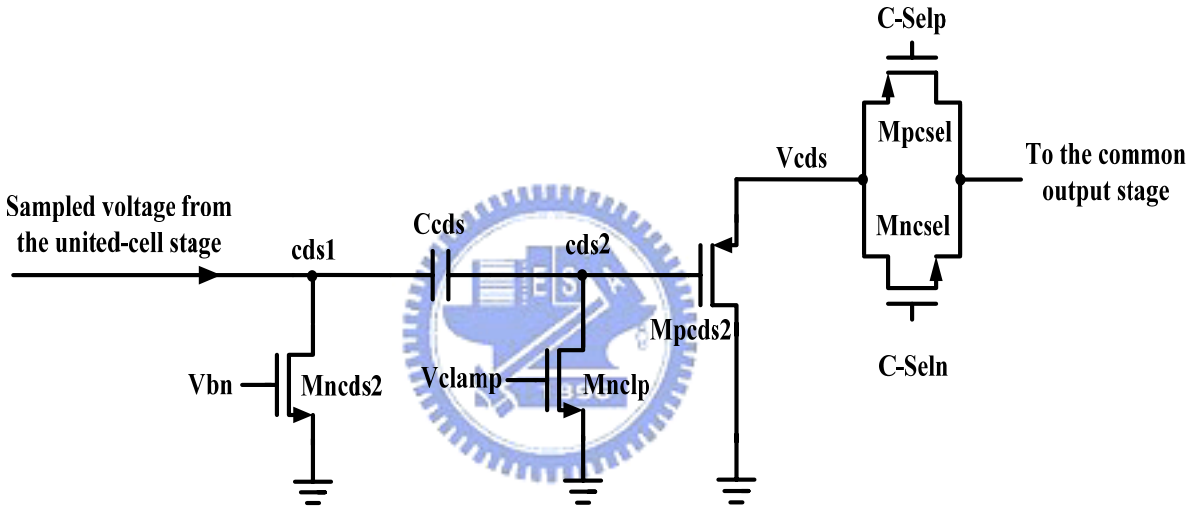


Fig. 17　The column CDS stage of 320 x 256 IR FPA.

The correlated double sampling (CDS) was introduced by White [24] as a signal processing technique for removal of switching transients and elimination of the Nyquist (reset) noise, both of which are associated with charge sensing circuits. An additional advantage is the attenuation of the 1/f noise and KTC noise components in the charge sensing circuits due to the zero in the CDS noise transfer function at the origin (w = 0). The effect of the CDS circuit on the reset noise and Johnson-Nyquist (white) noise in the associated circuitry has been adequately described [24]. The purpose of this correspondence is to present an analysis of the effect of the CDS circuit on the 1/f noise component generated in the preceding

circuitry. The reset noise on this node having a mean square value is given by kT/Co**.** Following reset and prior to charge transfer the clamp switch is closed briefly which causes the amplified reset noise to be stored on Ccds. Following charge transfer the sample switch is closed, resulting in an output voltage proportional to the difference in input levels at clamp and sample times. Assuming that all time constants associated with the switches are negligible compared to the sampling interval, the reset noise is fully correlated between clamp and sample and is therefore eliminated. In addition, Ccds is subject to reset noise from the clamp and sample switches and must be sufficiently large to avoid introducing additional noise components [25].

The CDS function of the column CDS stage is described below. At time T_1, the row switch is on and the clamping clock Vclamp is high and the clamp device Mnclp is on. The first sampled voltage signal is charged on the coupling capacitor Ccds and the voltages of Vcds1 and Vcds2 at time T_1 can be expressed

$$Vcds1(T_1) = VDD - V_{\text{int}} - V_{GSN(T_1)} \tag{2.10}$$

$$Vcds2(T_1) = 0 \tag{2.11}$$

where V_{int} is the integrated voltage signal on the capacitor and $V_{GSN(T_1)}$ is the voltage drop of the N-type source follower composed of the devices Mncds1 and Mncds2 at the time T_1.

At time T_2, the clamp device Mnclp is turned off before the internal integration capacitor is reset. Then the integrated node is reset to VDD and the second sampled voltage Vcds1 (T_2) becomes

$$Vcds1(T_2) = VDD - V_{GSN(T_2)} \tag{2.12}$$

where $V_{GSN(T_2)}$ is the voltage drop of the N-type source follower composed of the devices M_{ncds1} and M_{ncds2} at the time T_2.

Since the charges on the coupling capacitor Ccds is the same at T_1 and T_2. From equation

(2.10), (2.11) and (2.12), we have

$$Ccds[Vcds1(T_1) - Vcds2(T_1)] = Ccds[Vcds1(T_2) - Vcds2(T_2)] \quad (2.13)$$

Thus, the output signal *Vcds2* (T_2) after the CDS is

$$Vcds2(T_2) = V_{\text{int}} - (V_{GSN(T_2)} - V_{GSN(T_1)}) \quad (2.14)$$

The net voltage Vcds2 (T_2) is sent to P-type source follower of next stage, and the CDS function is realized. Each column CDS stage is shared by 256 unit cells, by applying CDS function the threshold variation between all the Mncds1 in every unit cell to improve the linearity.

The dynamic output stage of 320 x 256 IR FPA：

The dynamic discharge output stage is shown in Fig. 18. In the output buffer M_{nout1} and M_{nout2}, the Mpcds1 is shared by all the column, the dynamic discharge device Mndyn is used to save the static power dissipation and maintain the proper readout speed. The NMOS Mdyn is controlled by Vclamp. During the readout period, Vclamp is low, and M_{ndyn} is turned off to save the power dissipation. If the Mndyn is turned on by Vclamp, the output signal is pulled down, and finally readout speed can be increased.

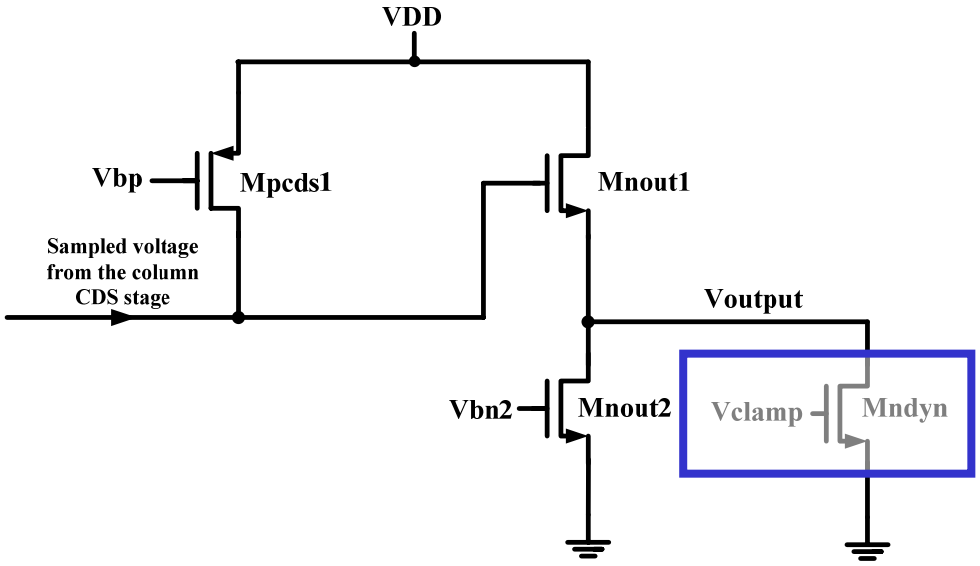


Fig. 18 The dynamic output stage of 320 x 256 IR FPA.

2.3 Chip operational principle

In the following, the chip operations of 32 x 32 and 320 x 256 IR FPA are described.

2.3.1 The chip operation of 32 x 32 IR FPA

The detailed circuit involving united-cell input stage, column sampling circuit, and output CDS circuit is shown in Fig. 19. The column sampling circuit is shared by one column, and the output CDS circuit is shared by all column sampling circuits.

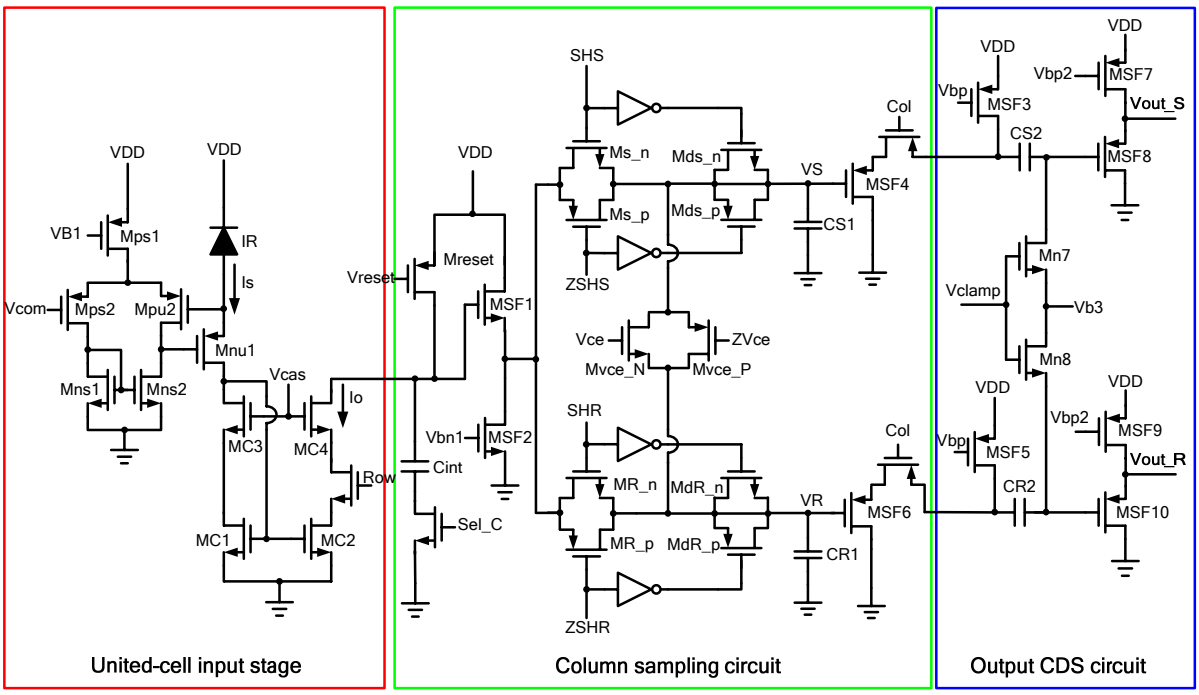


Fig. 19 The detailed circuit involving united-cell stage, column sampling circuit, and output CDS circuit.

The image information is transformed as the photocurrent in the cell array by using the IR detector. The photocurrent is delivered to the column bus and converted into a voltage signal proportional to the intensity of image after the current integration outside the pixel. The

photo-signal and reset signal are used for the operation of the double delta sampling (DDS). The two signals generated in the output CDS circuit are delivered to the programmable gain amplifier (PGA), A/D converter, and display system outside the chip to generate the raw image.

The major operational timing diagram is shown in Fig. 20. Firstly, the row select signal Row1 is high and the Reset control signal is low to reset the voltage at the integrating capacitor to 3.3V. After the reset operation, the photocurrents of all pixels in the Row1 are integrated at the gate of MSF1 of Fig. 19 during the integration time. Then the control signal of SHS and ZSHS are on to sample the photo-signal in the output of the first source follower MSF1/MSF2 to the node VS. After that, the Reset control signal is on again and then the control signal of SHR and ZSHR are on to sample the reset signal in the output of the first source follower to the node VR when the Reset control signal is off. This reset signal must be sampled after the Mreset is off because the effect of clock feedthrough on VS and VR from the Reset control signal is the same. Those noises can be reduced by the CDS operation. The duration of reset time is kept long enough to eliminate the amount of residual charges due to incomplete reset.

The integration time Tint and frame rate are expressed as

$$\text{Tint} = \text{N} \cdot \text{T}_{\text{DT}} = 2 \cdot N \cdot \frac{1}{f_{\text{clock}}} \tag{2.15}$$

$$\text{Frame rate} = \frac{1}{M \cdot N \cdot T_{DT}} = \frac{f_{clock}}{2 \cdot M \cdot N} \tag{2.16}$$

where M, N, T_{DT}, and f_{clock} are row number of imager, column number of imager, output data rate, and system clock, respectively.

This chip involving controlling logic which can switch signals SHS and ZSHS that are inputted from internal or external of the chip is used for adjusting integration time. The purpose of adjusting integration time is that when this chip is used in space, it would have wider adjusting range and wide application.

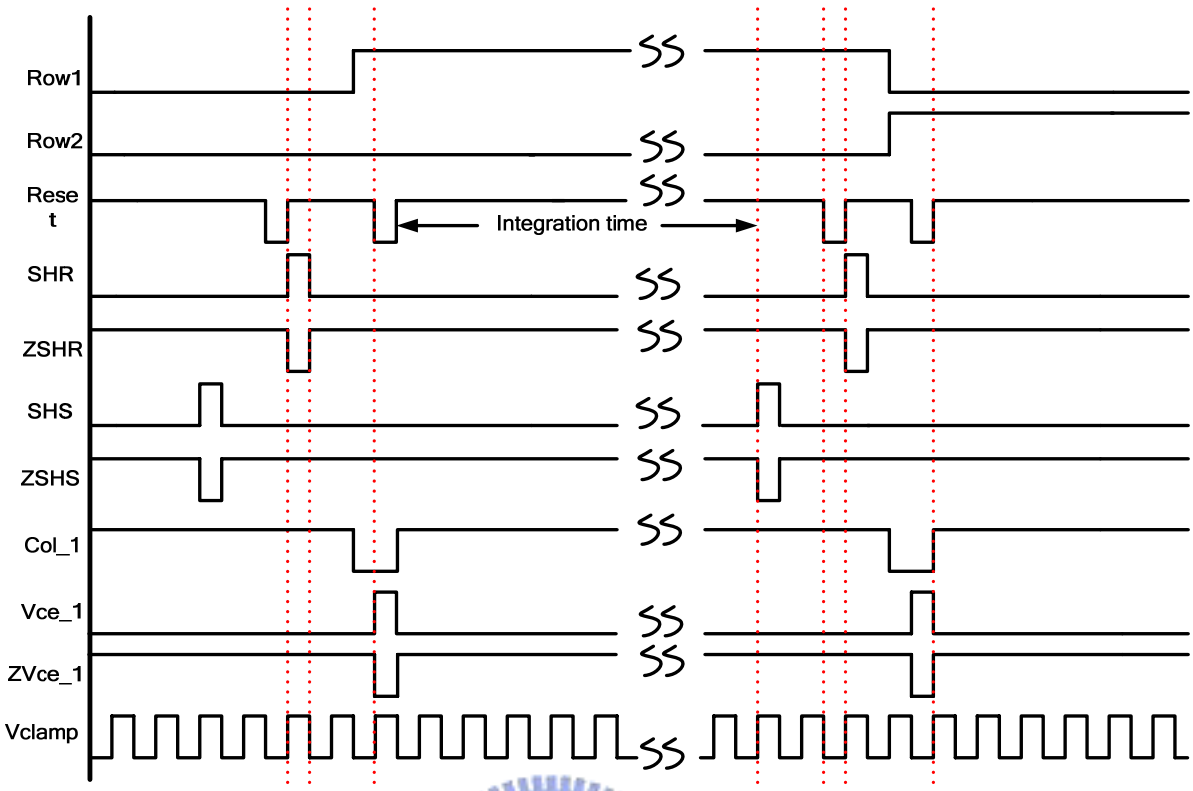


Fig. 20 The timing major diagram of the 32 x 32 IR FPA.

2.3.2 The chip operation of 320 x 256 IR FPA

The detailed circuit involving common left half circuit, united-cell input stage, column CDS stage, and Dynamic output stage is shown in Fig. 21. The major operational timing diagram is shown in Fig. 22. The clock timing waveforms of the start of frame, row select clock, and column select clock and clamping control Vclamp are shown in Fig. 22 where the clock signal has a high level of 3.3V and a low level of 0V. The readout operation is described below. When the start of frame signal is on, the first row is selected and the first column select column 1 is on, the integration voltages of the unit cell input stages of the first row are switched to the CDS stages. The integration time = 6.4us is based on 64 by 64 IR FPA, and it is controlled by the reset signal.

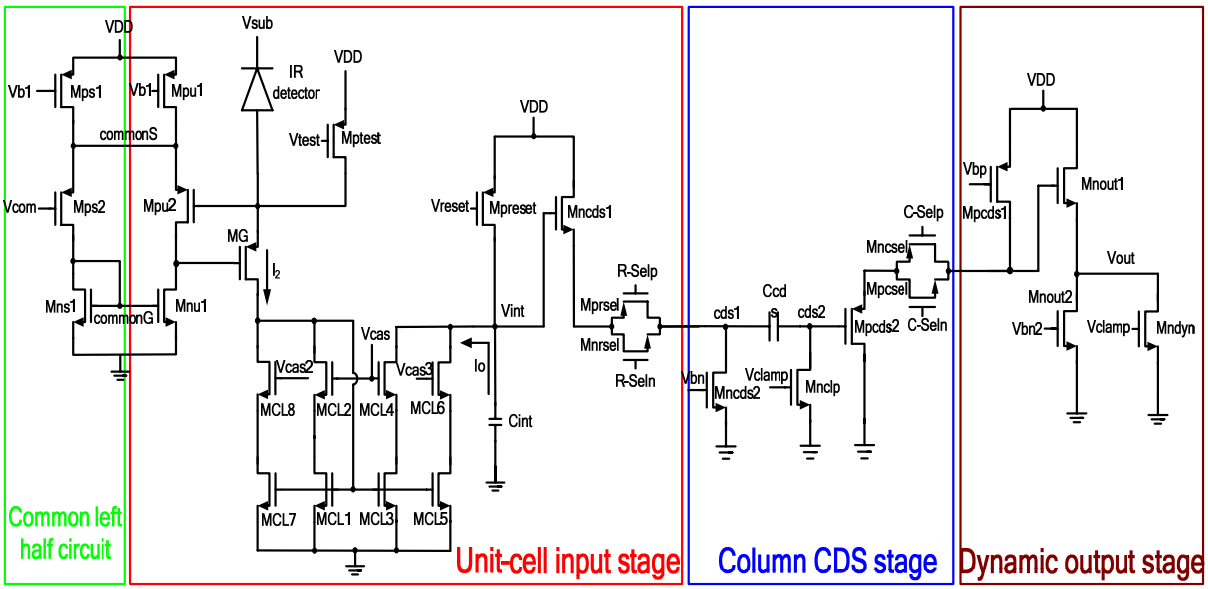


Fig. 21 The detailed circuit of 320 X 256 readout chip.

After an integration time T_{int} controlled by the column reset signal, the first column select signal column 1 is high again and the voltage signal of the first column in the first row is sampled to the output stage. The integration capacitor is reset immediately after it is sampled. Then the second pixel of the first row is read out serially. After all pixels in the first row have been readout, the second row select Row 2 is high and then the second row is switched to the integration capacitor. When the Row 256 is selected, the row select signal is invited to form the end-of-frame signal which indicates the first frame has been readout. Then the second frame is readout.

The integration time Tint and frame rate are expressed as

$$\text{Frame rate} = = \frac{f_{clock}}{4 \cdot M \cdot N} \tag{2.17}$$

where M, N, and f_{clock} are row number of imager, column number of imager, and the system clock, respectively.

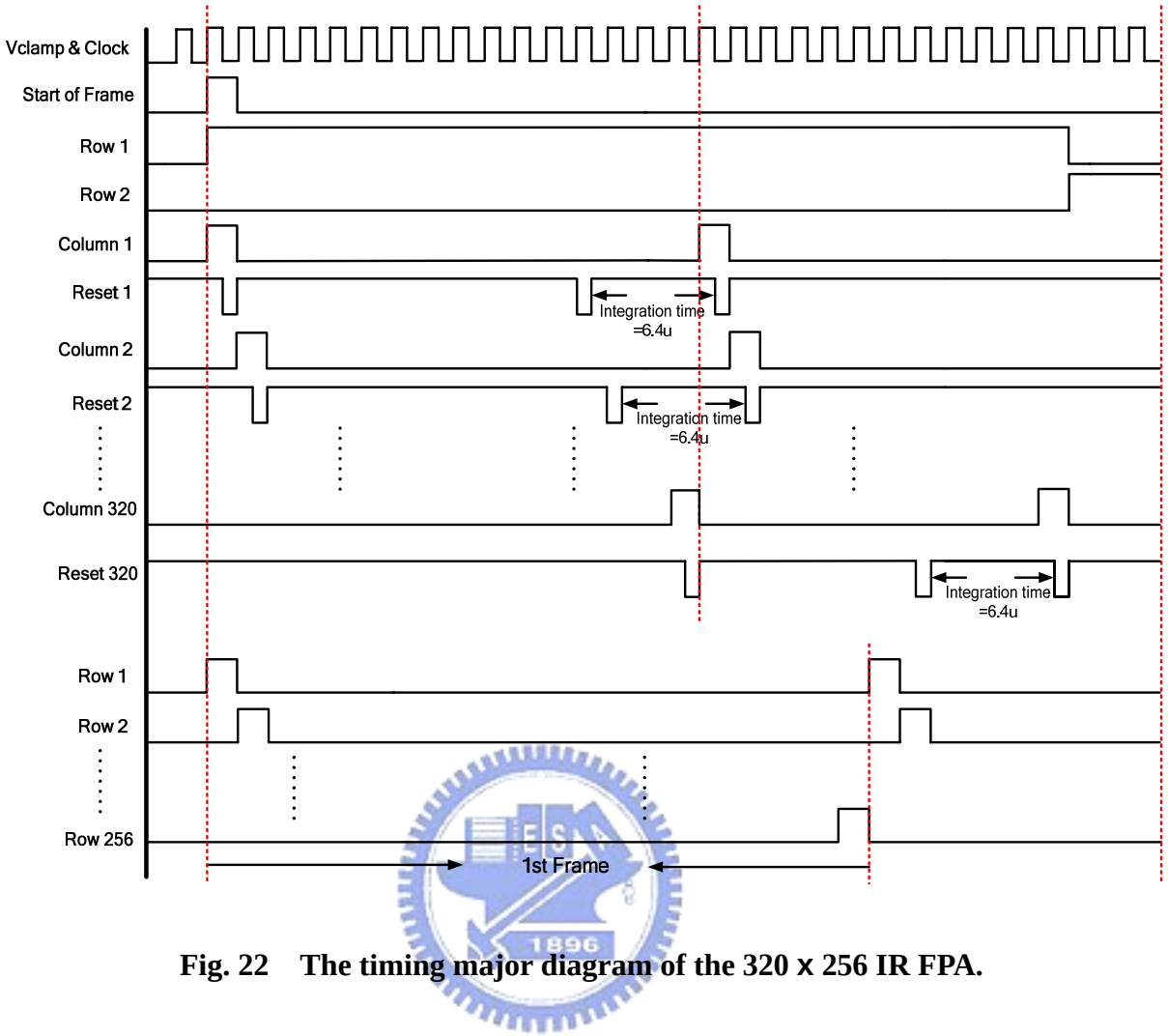


Fig. 22 The timing major diagram of the 320 x 256 IR FPA.

2.4 Simulation results

In this thesis, the 32 x 32 and 320 x 256 readout circuit array will be combined with the InGaAs IR detector array which developed by Chunghwa Telecom Lab to compose a complete IR image system. The property of the detector array is illustrated below. Fig. 23 shows the responsitivity of InGaAs detector, and the standard version with high efficiency is 900nm to 1700nm wavelength range. This detector is applied in the near-infrared (NIR) regime, and the uncooled operation is one of its remarkable features. In Fig. 24, it is shown that when the detector is biased at -3V, -1V, and 0V, the photo excited current is very stable and the detector shunt resistance is very large. The dark current measurement of InGaAs

detector array is shown in Fig. 25, and it shows that dark current of InGaAs detector approximates 11.5pA ~ 14.6pA under bias 0V ~ -1V. This dark current is higher than 0.5pA expected by Chunghwa Telecom laboratory. It can demonstrate that they underestimate the dark current of InGaAs detector. The chip photo of the detector is shown in Fig. 26.

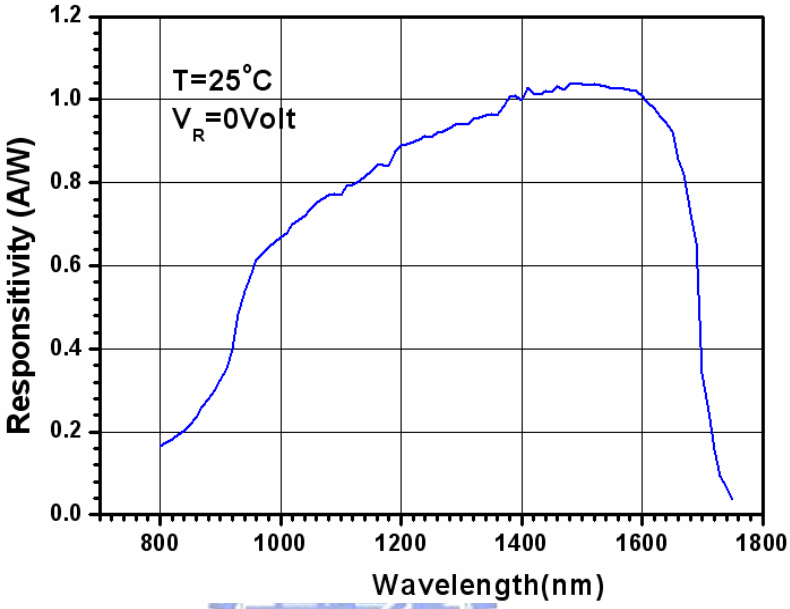


Fig. 23 The responsitivity of the InGaAs detector developed by Chunghwa Telecom laboratory.

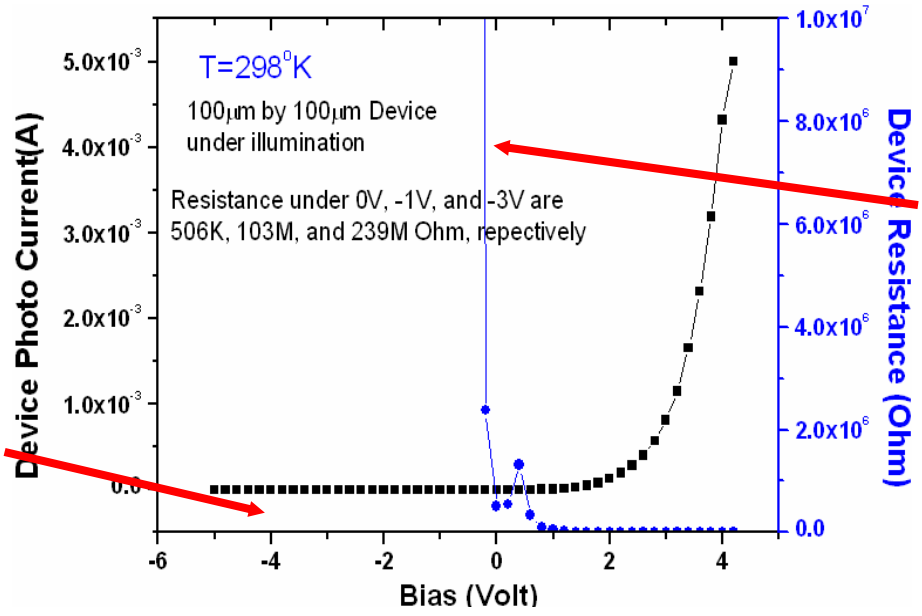


Fig. 24 The characteristic of the InGaAs detector array developed by Chunghwa Telecom laboratory.

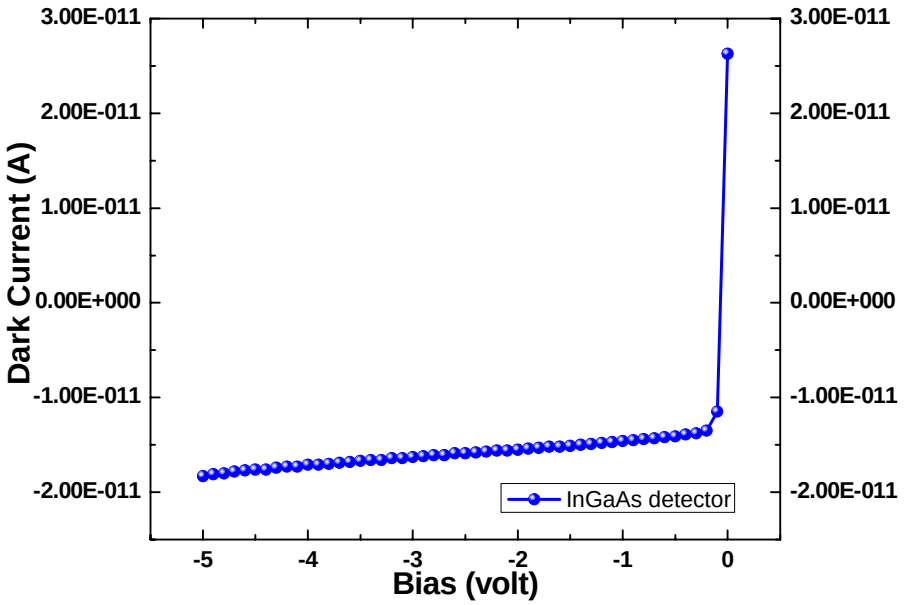


Fig. 25 Measurement of dark current of InGaAs detector array developed by Chunghwa Telecom laboratory.

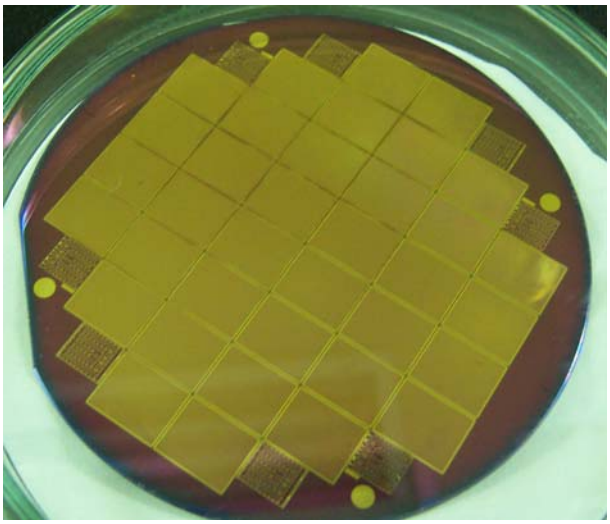


Fig. 26 The chip photo of the InGaAs detector developed by Chunghwa Telecom laboratory.

In the following, the simulation results and layout description of 32 x 32 and 320 x 256 readout circuits are described.

2.4.1 Simulation results of 32 x 32 IR FPA

The simulation results of the voltage difference between Vout_S and Vout_R of the output CDS circuit with input photocurrent 5pA to 105pA and 100pA to 5000pA are shown in

Fig. 27 and Fig. 29, respectively. In Fig. 27, the integration time is 73 us, the integration capacitor is 320 fF, and the input current signals are 5pA, 15pA, 25pA, 35pA, 45pA, 55pA, 65pA, 75pA, 85pA, 95pA, and 105pA. In Fig. 29, the input current signals are 100pA, 450nA, 800pA, 1150pA, 1500pA, 1850pA, 2200pA, 2550pA, 2900pA, 3250pA, 3600pA, 3950pA, 4300pA, 4650pA, and 5000pA. The normal integration capacitance (320 fF) is total parasitic capacitor at integration node (Vint). An extra capacitor of 320 fF with a MOS switch conveniently lay along vertical direction and in parallel with the 320 fF normal integration capacitor. The integration time is variable through off-chip controlled signal. The optional capacitor is used to prevent saturation when the incident light is strong and the integration time is long such as the application of still imager in the environment of strong light. The equalization of both photo-signal path and reset signal path controlled by Vce is performed after the readout of the held voltage. The equalized voltage at the two nodes of A and B is then readout to the output CDS circuit. In the output CDS circuit, the NMOS devices Mn7 and Mn8 controlled by the signal Vclamp is to clamp the voltage at the gate of MSF8 and MSF10 in the output source follower MSF7 and MSF8 (MSF9 and MSF10) to Vb3. The capacitor of 1.5 pF is used to perform the operation of correlated double sampling (CDS).

In this work, the device parameters of 0.35 um 2P4M N-well CMOS technology is used for SPICE simulation. In order to observe the process variation affects the linearity, the linearity of different corners is shown in Fig. 28 and Fig. 30. As may be seen from these figures, the linearity of the readout circuit is greater than 99% and the output swing is equal to 1.26 V. The series output voltage difference Vout_S and Vout_R of 32 cells is shown in Fig. 31, and it is verified full chip functional correctness for input photo current from 40pA to 5000pA with 160pA step. The cell array mask of 32 x 32 IR FPA is design by Chunghwa Telecom Lab using OrCAD tool, and it is shown in Fig. 32. An experimental 32 x 32 readout chip has been designed and fabricated to combine with the InGaAs IR detector array. The summary of specification of the 32 x 32 readout chip is listed in Table II.

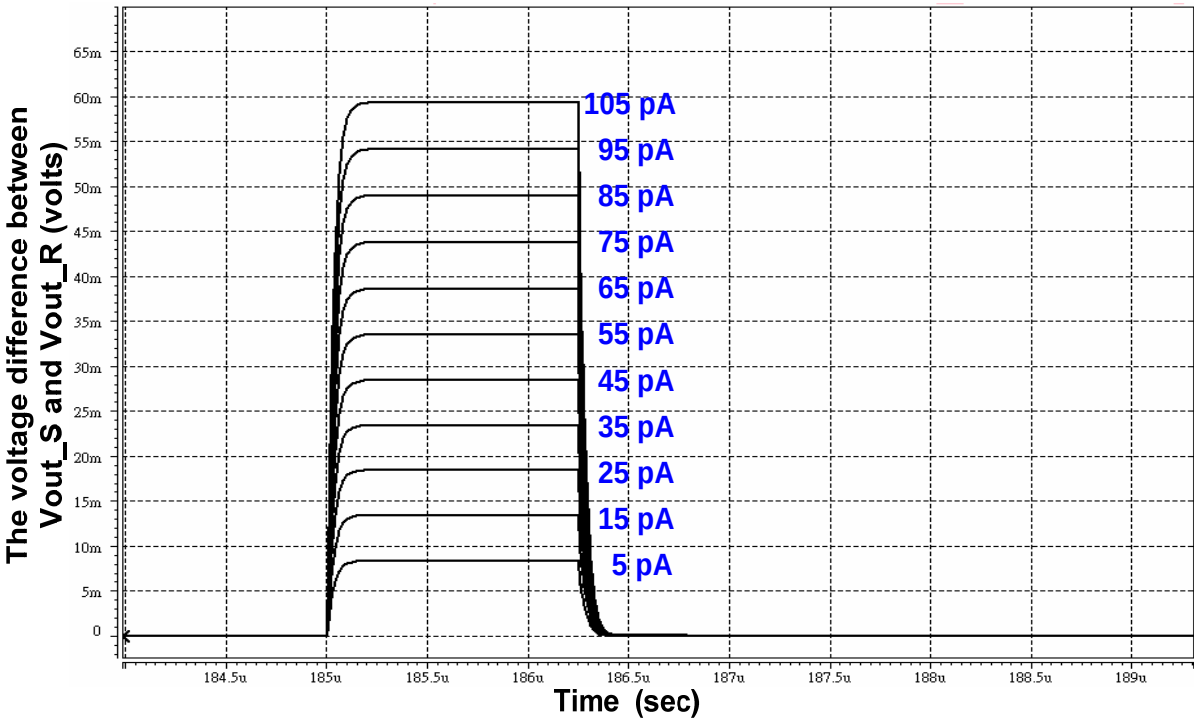


Fig. 27 The voltage difference between Vout_S and Vout_R of Fig. 19 for the input photocurrent from 5p to 105p with 10pA step.

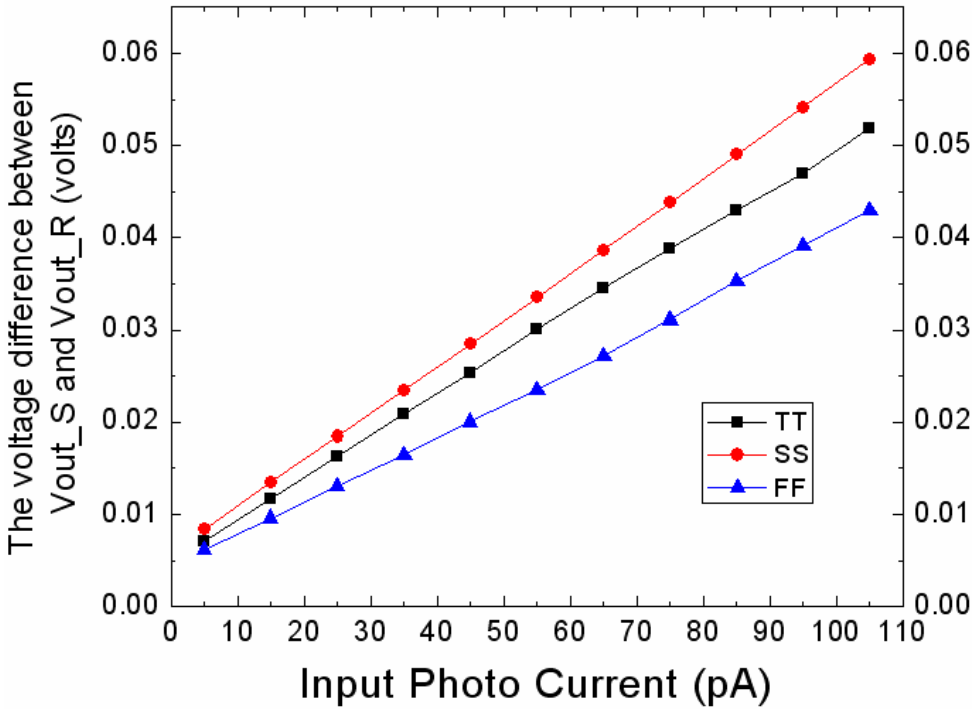


Fig. 28 The linearity of the voltage difference between Vout_S and Vout_R for input photocurrent 5pA to 105pA with 10pA step.

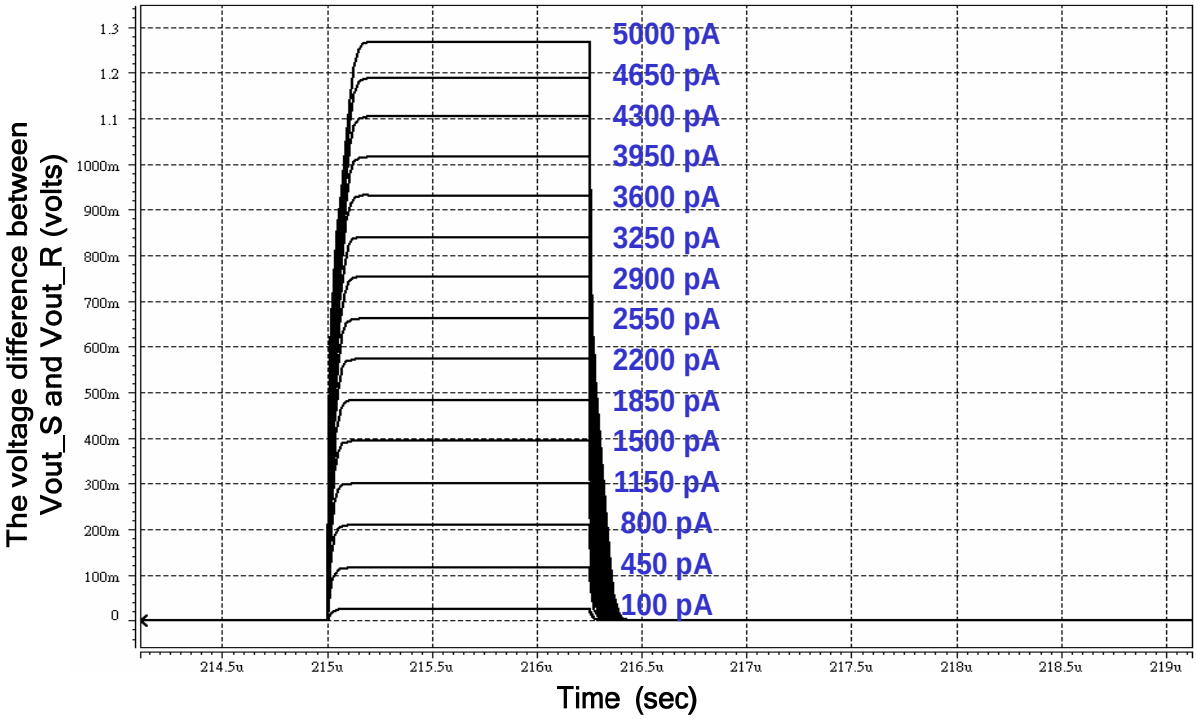


Fig. 29 The voltage difference between Vout_S and Vout_R of Fig. 19 for the input photocurrent from 100p to 5000p with 350pA step.

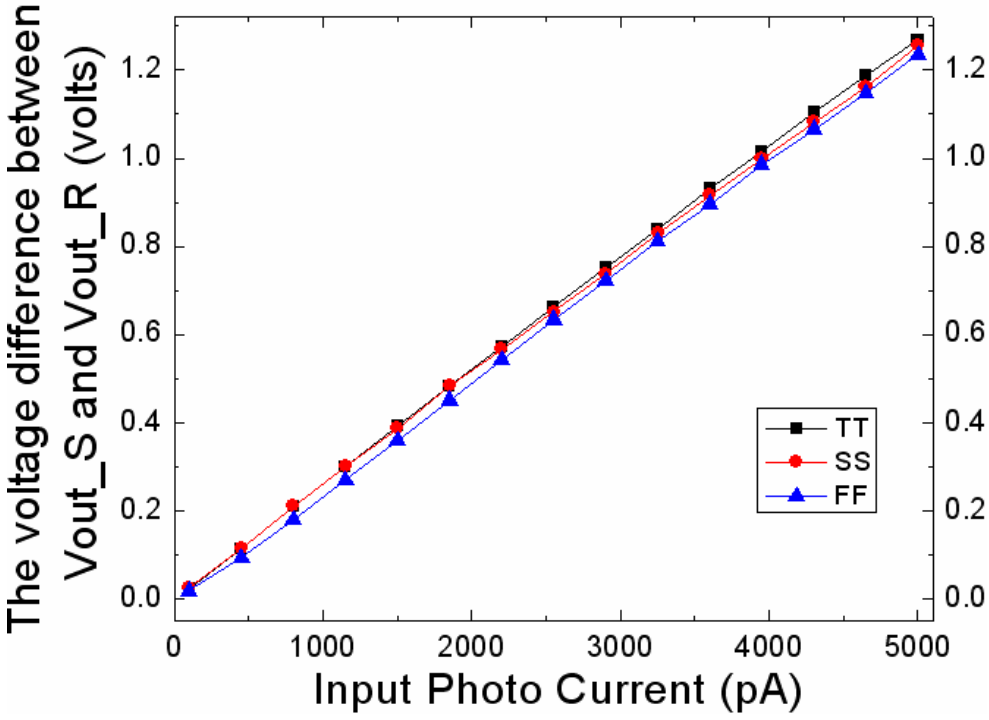


Fig. 30 The linearity of the voltage difference between Vout_S and Vout_R for input photocurrent 100pA to 5000pA with 350pA step.

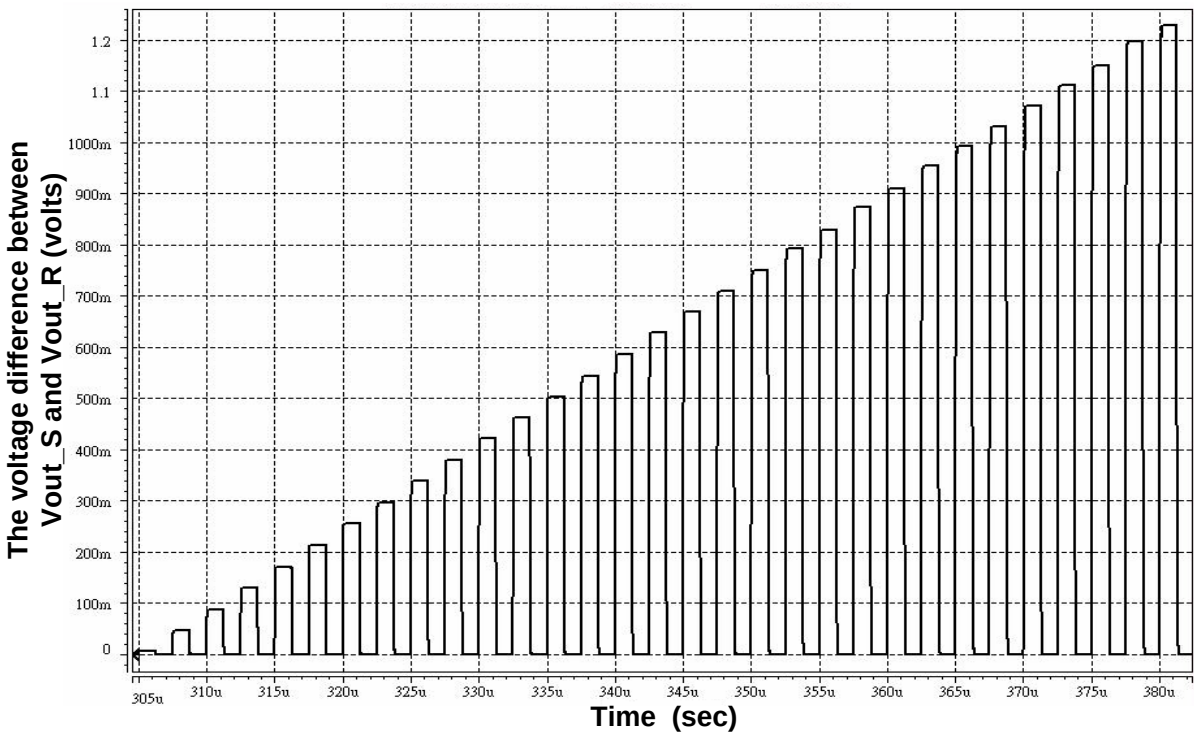


Fig. 31 The series output voltage difference between Vout_S and Vout_R of 32 cells for input photocurrent 40pA to 5000pA with 160pA step.

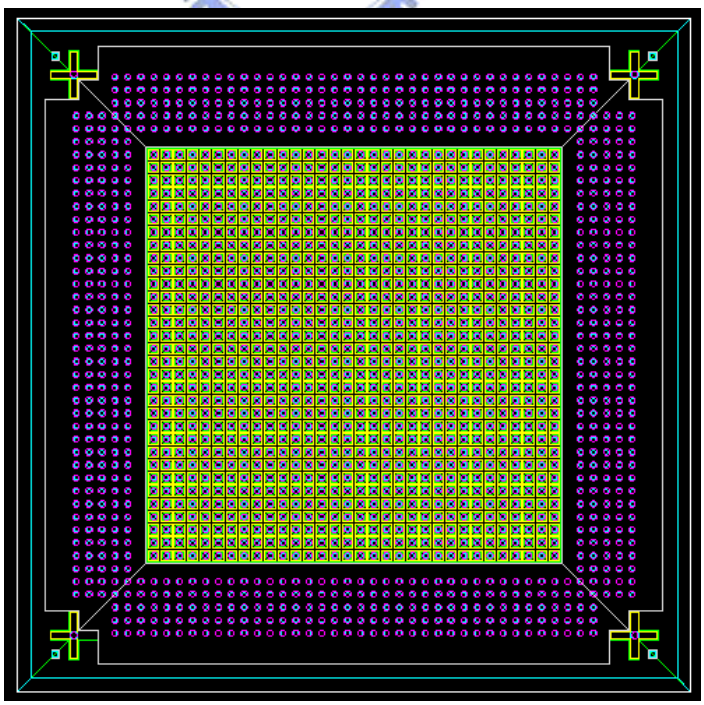


Fig. 32 The cell array masks of 32 x 32 IR FPA.

Table II The summary of specification of the 32 x 32 readout chip.

Technology	TSMC 0.35 um 2P4M CMOS
Array Size	32 x 32
Pixel Pitch	30 um x 30 um
Integration Capacitance	320 fF + 320 fF
Integration Time	72.5 us
Operational Current Range	5pA ～ 5nA
Output Swing	1.26 V
Maximum Charge Capacity	9.2×10^{6} e^{-}
Transimpedance	5.04×10^{8} ohms
Chip Area	2500um X 2461 um
Power	16.8 mW
Linearity	99 %
Nonlinearity	< 1.8% (for 10% ~90% full swing)
Maximum Readout Speed	0.8 M Hz
Maximum Frame Rate	714 frame/sec

2.4.2 Simulation results of 320 x 256 IR FPA

The simulation results of output voltage Vout in the dynamic output stage for input photocurrent 0pA to 500pA and 100pA to 5000pA in Fig. 18 are shown in Fig. 33 and Fig. 35, respectively. In Fig. 33, the integration time is 73 us, the integration capacitor is 10fF, and the input current signals are 0pA, 50pA, 100pA, 150pA, 200pA, 250pA, 300pA, 350pA, 400pA, 450pA, and 5000pA. In Fig. 29, the input current signals are 0pA, 500pA, 1000pA, 1500pA, 2000pA, 2500pA, 3000pA, 3500pA, 4000pA, 4500pA, and 5000pA. The linearity of different corners is shown in Fig. 34 and Fig. 36. The linearity of the readout circuit is greater than 99%, and the maximum output swing is equal to 1.5 V. When Vclamp is high during T_{pixel}, Vout is clamped to 0.3V. When Vreset is low during T_{pixel}, the integration node Vint is reset to 3.3V. These two operations realize both clamping and dynamic discharging functions. The readout speed is defined as the reciprocal of the pixel processing time ($1/T_{pixel}$), and the simulation readout speed can reach 10MHz. The total chip size is 11500 μm x 8650 μm, and will combined with the InGaAs detector array which developed by Chunghwa Telecom Lab to complete the entire IR image system. The series output voltage (Vout) of 32 cells is shown in Fig. 37, and it is verified full chip functional correctness for input photo current from 40pA to 5000pA with 160pA step.

The summary of specification of the 320 x 256 readout chip is listed in Table III.

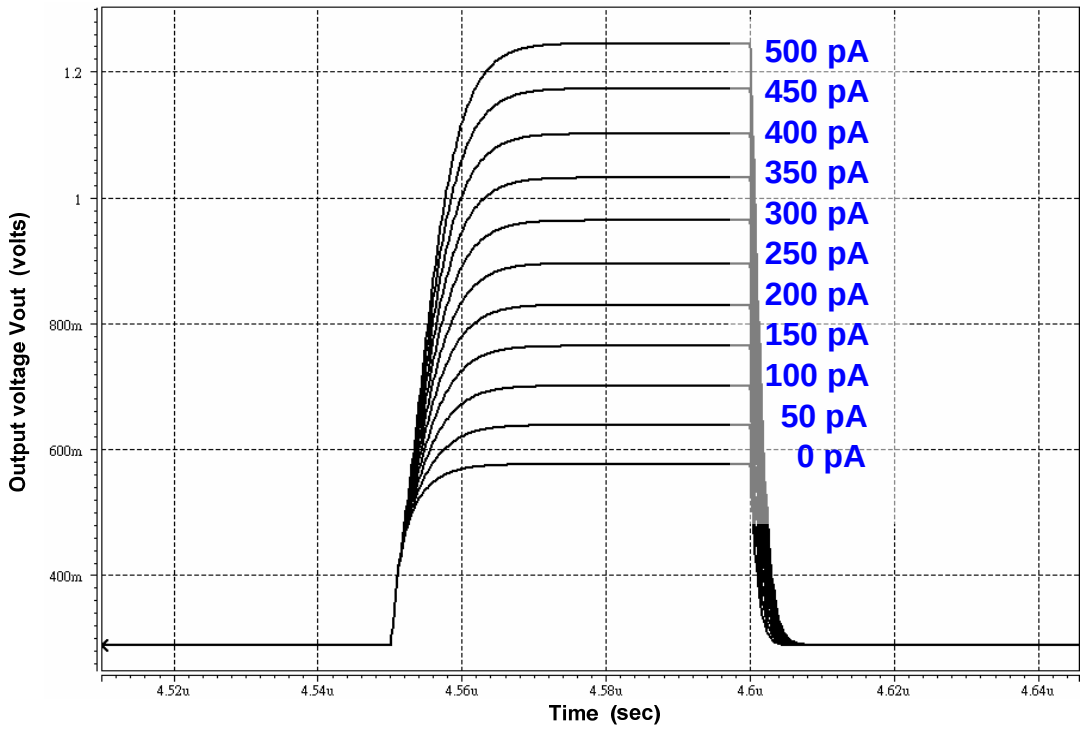


Fig. 33 The simulated waveforms of output voltage Vout in the dynamic output stage for the input photocurrent from 0pA to 500pA with 50pA step.

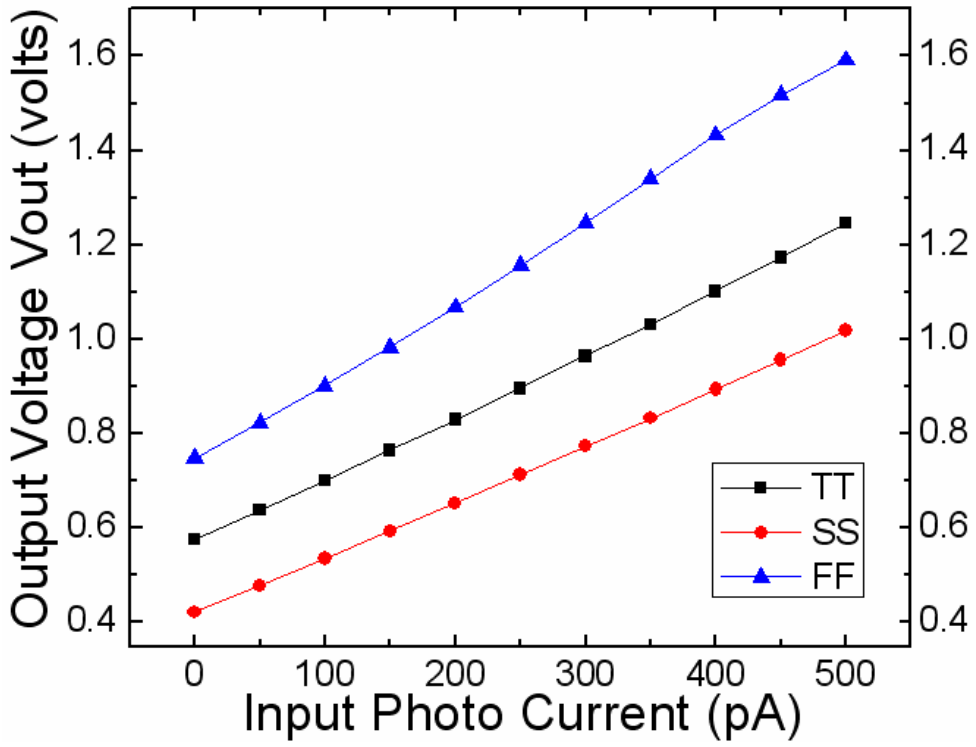


Fig. 34 The linearity of output voltage Vout in the dynamic output stage for the input photocurrent from 0pA to 500pA with 50pA step.

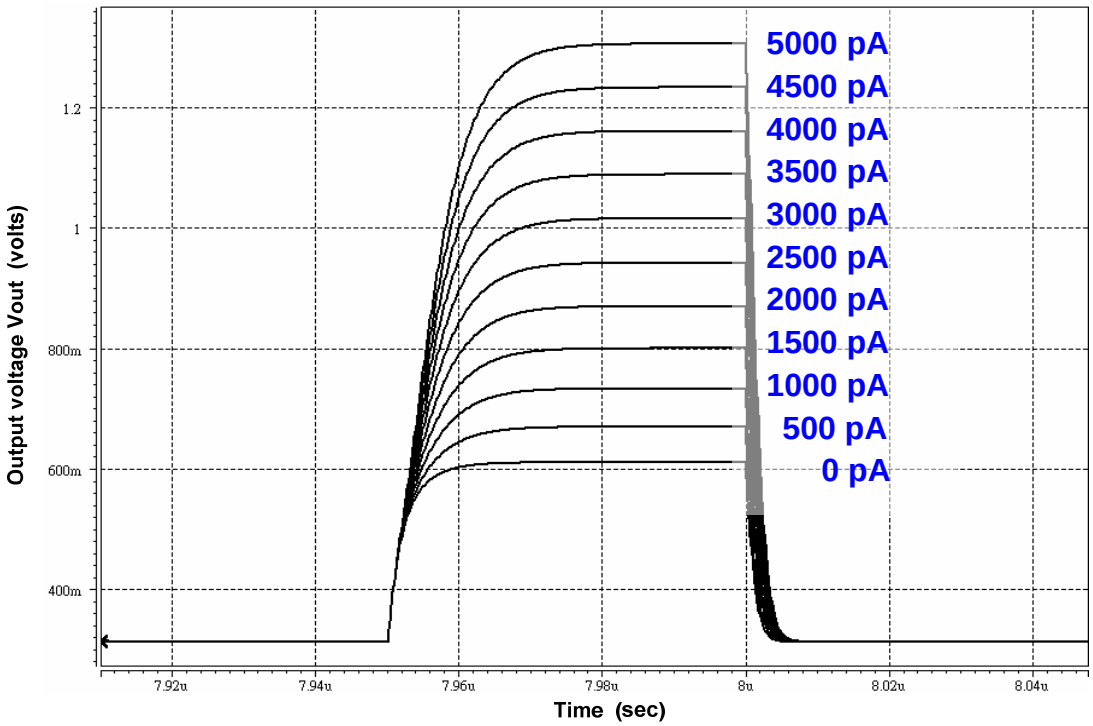


Fig. 35 The simulated waveforms of output voltage Vout in the dynamic output stage for the input photocurrent from 0p to 5000pA with 500pA step.

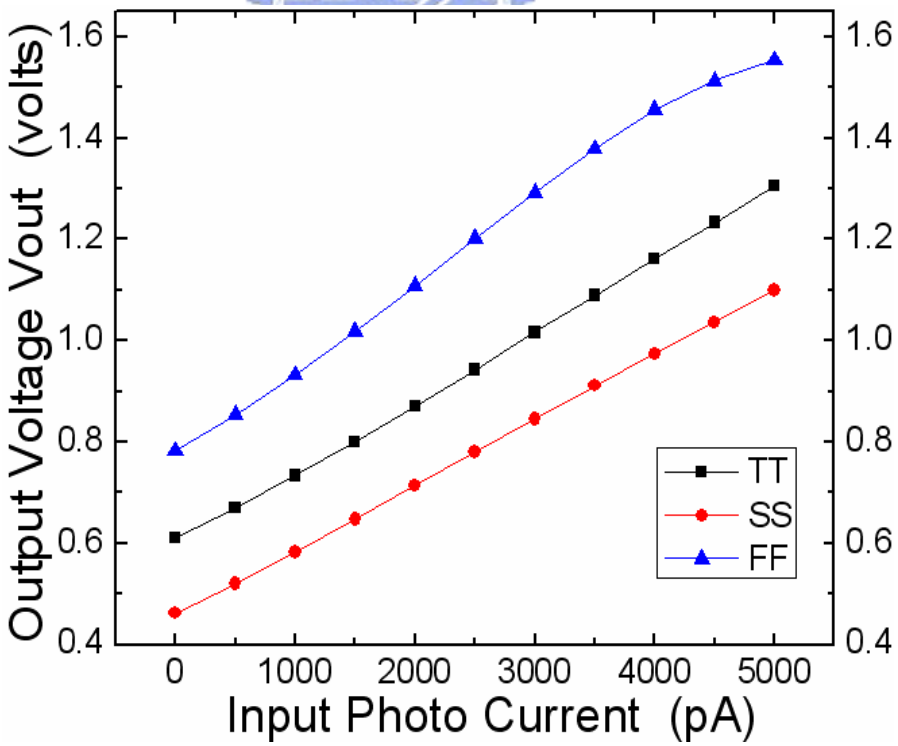


Fig. 36 The linearity of output voltage Vout in the dynamic output stage for the input photocurrent from 0pA to 5000pA with 500pA step.

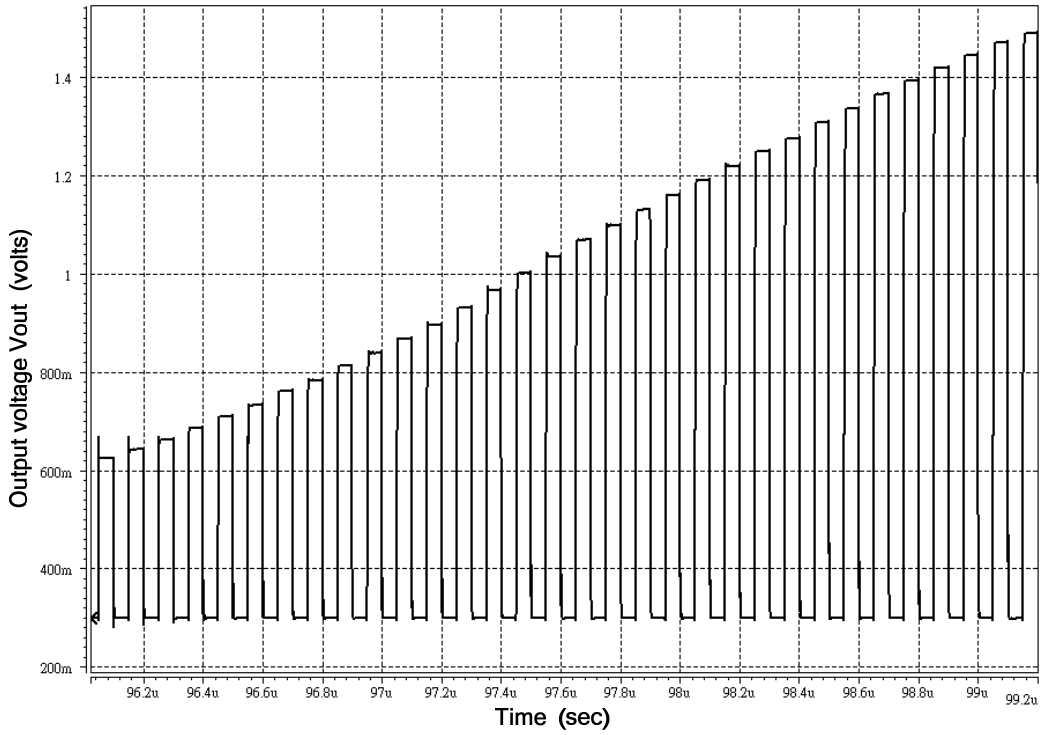


Fig. 37 The series output voltage (Vout) of 32 cells for input photocurrent 40pA to 5000pA with 160pA step.

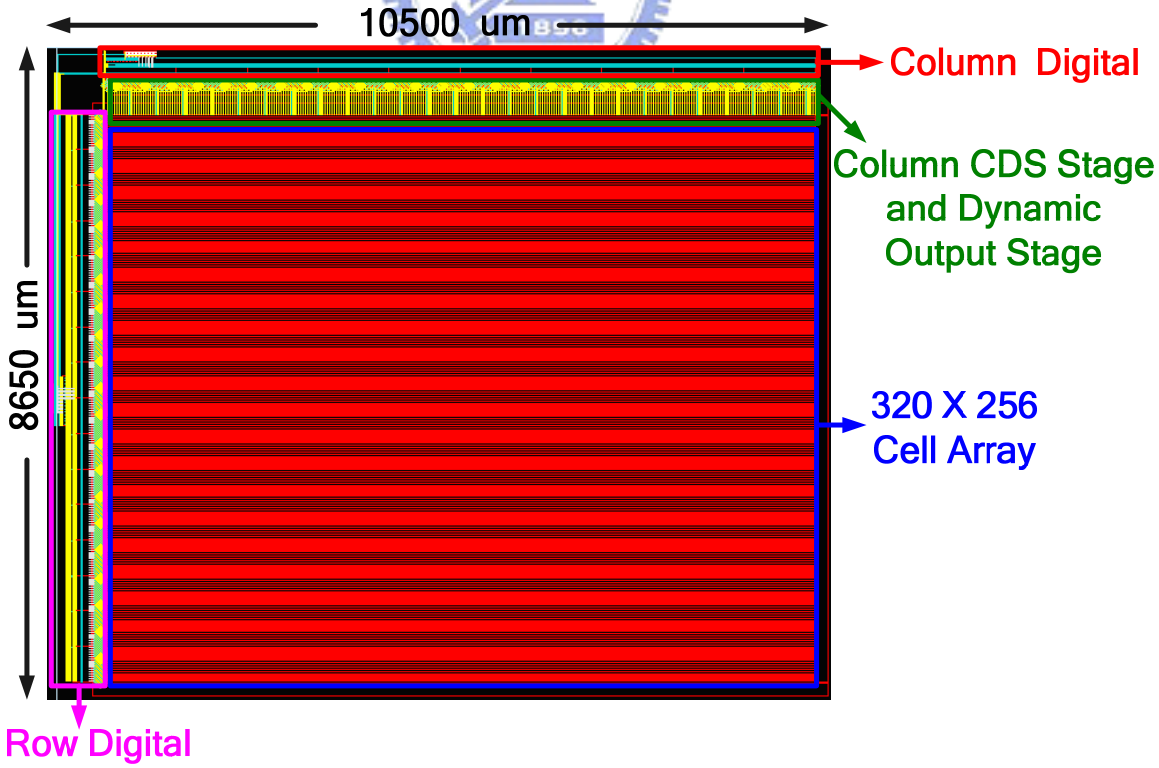


Fig. 38 The layout of 320 x 256 readout chip.

Table III The summary of specification of the 320 x 256 readout chip.

Technology	TSMC 0.35 um 2P4M CMOS
Array Size	320 x 256
Pixel Pitch	30 um x 30 um
Integration Capacitance	10 fF
Integration Time	6.4 us
Current Range	5pA ～ 5nA
Output Swing	0.9 V
Maximum Charge Capacity	1.125×10^{5} e^{-}
Transimpedance	1.8×10^{8} ohms
Chip Area	10500um × 8650 um
Power	103.7 mW
Linearity	99 %
Nonlinearity	< 5% (for 10% ~ 90% full swing)
Maximum Readout Speed	10 M Hz
Frame Rate	61 frame/sec

CHAPTER 3
CMOS READOUT CIRCUIT APPLICATION TO BIOCHEMISTRY

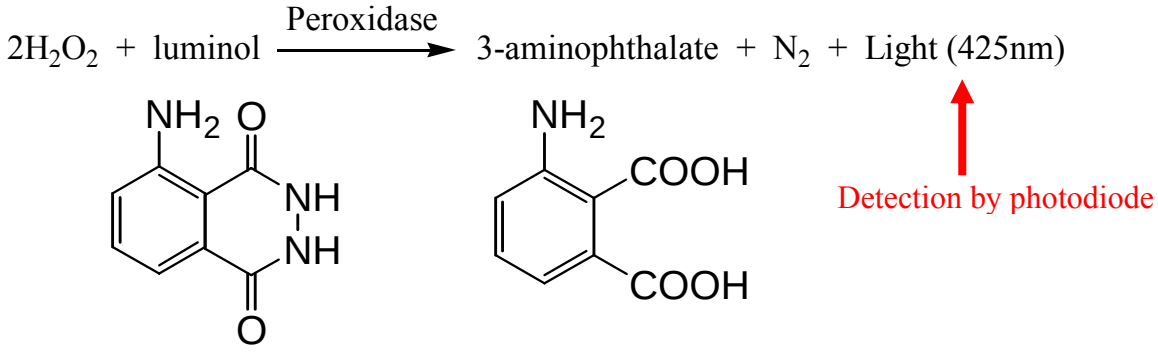
3.1 Background

Rapid advancement in modern biology has produced opportunities and needs in clinical diagnostics and many other biorelated measurements. To develop a high-throughput instrument with small size, low cost, ease of use, and high accuracy is becoming more and more important. Development of a suitable sensor for a variety of biochemical reactions is the key for this progress [26]. The small size of semiconductor sensors not only contributes to their potentially low cost, but also allows them to be integrated with microelectronic circuit, creating the so called integrated sensors, further enhancing their performance [27].

The photo-multiplier tube (PMT) is the most common light sensor used in these spectrophotometers. PMT is an effective and sensitive light sensor, wherein one photon can induce approximately electrons in the photomultiplier tube. However, the need for high voltage (about 500 to 1000 V), the size, and the price of the PMT limit its application in a variety other fields such as personalized diagnosis kits.

The complementary metal oxide semiconductor (CMOS) process is the most commonly used procedure in semiconductor industry. A photodiode is basically a p-n junction operated under reverse bias. Free electron-hole pairs will be generated in photodiode when photodiode is illuminated by the photon, which contains energy higher than the band gap of photodiode [28]. CMOS photodiodes act as semiconductor light sensor with the advantages of low price, small size, and low power consumption as compares to that of PMT. These features make CMOS photodiodes easy to be a personalized healthy care instrument.

We demonstrated a reaction that can be used as the platform light emitting reaction to permit enzymatic activity to be observed



which shows the light emitting reaction catalyzed by horseradish peroxidase (HRP). Since many enzymes produce (Table IV), the HRP-luminol-system should be a good platform reaction to couple and detect many other enzymatic reactions by luminescence. In a CMOS photodiode system, the chemiluminescence generated from the biochemical reaction produces current flow that corresponds to the rate of enzymatic-catalyzed reaction.

Table IV Important biochemicals that can be determined by HRP-luminol-H_2O_2 system.

Target	H_2O_2 producing reactions
Glucose	$Glucose + O_2 + 2H_2O \xrightarrow{Glucose\ Oxidase} Gluconic\ acid + 2H_2O_2$
Uric acid	$Uric\ acid + O_2 + 2H_2O \xrightarrow{Uricase} allantoin + CO_2 + 2H_2O_2$
Cholesterol	$Cholesterol + O_2 \xrightarrow{Cholesterol\ oxidase} cholesten\text{-}3\text{-}one + H_2O_2$
Lactate	$L\text{-}Lactate + O_2 \xrightarrow{Lactate\ oxidase} pyruvate + H_2O_2$
Phospholipid	$Phospholipids + H_2O \xrightarrow{Phospholipase} Fatty\ acids + Choline$ $Choline + H_2O + 2O_2 \xrightarrow{Choline\ oxidase} betaine + 2H_2O_2$
Triglycerides Lipase	$Triglycerides + 3H_2O \xrightarrow{Lipase} Fatty\ acids + glycerol$ $Glycerol + O_2 \xrightarrow{Glycerol\ oxidase} glyceraldehyde + H_2O_2$

3.2 Circuit implementation

A novel of luminescent measurement chip is designed in 0.35um technology. As shown in Fig. 39, the chip is composed of 128 by 128 photodiodes and a current readout circuit. The concentration of H_2O_2 is proportional to liberated luminescence. The chemiluminescence signal is absorbed by photodiode, and the photodiode generates the signal current.

The signal current injects into readout circuit, and it is converted to the voltage. The signal current (I_{signal}) injects into readout circuit and this current flowing through MG is mirrored to integration capacitance (Cint) through the high-swing cascode current mirror M5-M8. The discharge voltage of integration capacitance is proportional to signal current, and the discharge voltage is transferred to Vout through CDS circuit. In other words, the current readout circuit can convert different signal current to linearity output voltage (Vout).

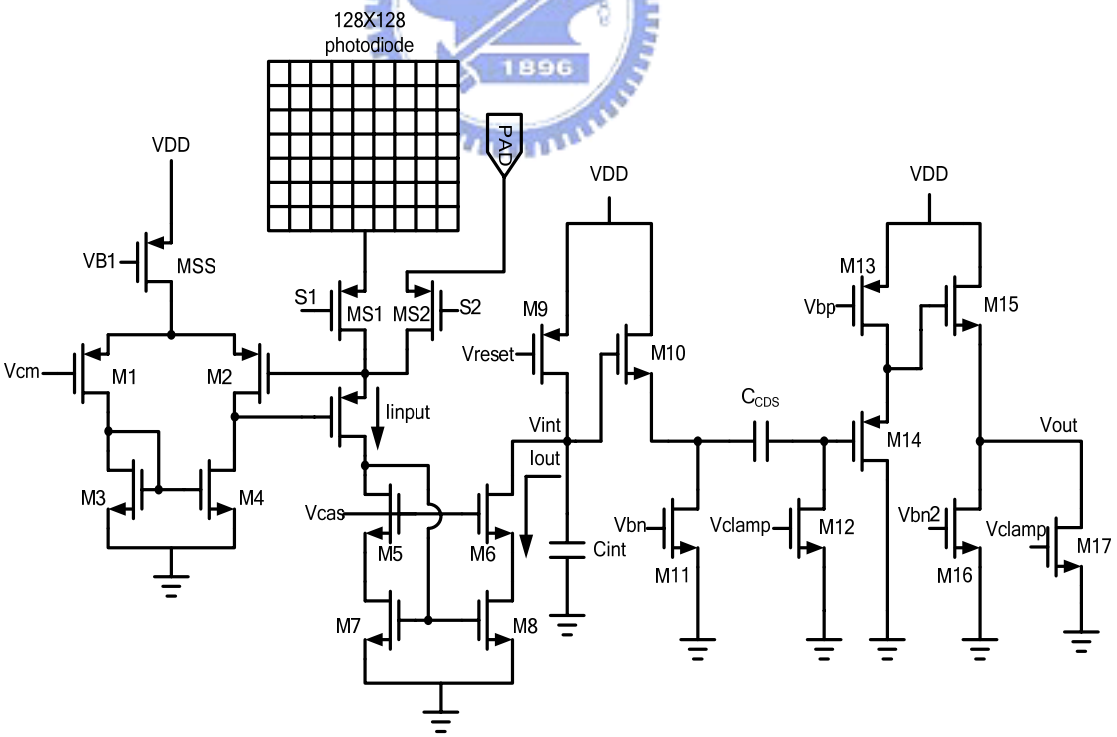


Fig. 39 The readout circuit for detection chemiluminescence.

3.3 Simulation results

The simulation results of output voltage Vout for input photocurrent 10pA to 250pA and 1nA to 111nA in Fig. 39 are shown in Fig. 40 and Fig. 42, respectively, where the integration capacitor is 500fF, the integration time is controlled by external clock. The linearity of different corners is shown in Fig. 41 and Fig. 43, and the linearity of the readout circuit is greater than 99%.

As shown in Fig. 40 and Fig. 42, the Vout is clamped to 0.05V and integration capacitance is integrated by Iout when Vclamp and Vreset are high. The integration node Vint is reset to 3.3V and the integrated voltage is transferred to output node (Vout), when Vclamp and Vreset are low. These two operations realize both clamping and dynamic discharging functions. The readout speed is defined as the clock frequency. This chip size is designed and fabricated in 0.35um n-well CMOS technology, and total chip area is 2700 μm x 1740 μm.

The summary of operational specification of the readout chip is listed in Table V.

Table V The summary of operational specification of the readout chip.

Input current	System clock	Integration time	Integration Cap	Linearity	Average Power
10 pA～250 pA	125 HZ	4 ms	500 f F	99 %	1.0715 mW
1 nA～111 nA	62.5 KHZ	8 us	500 f F	99 %	1.1842 mW

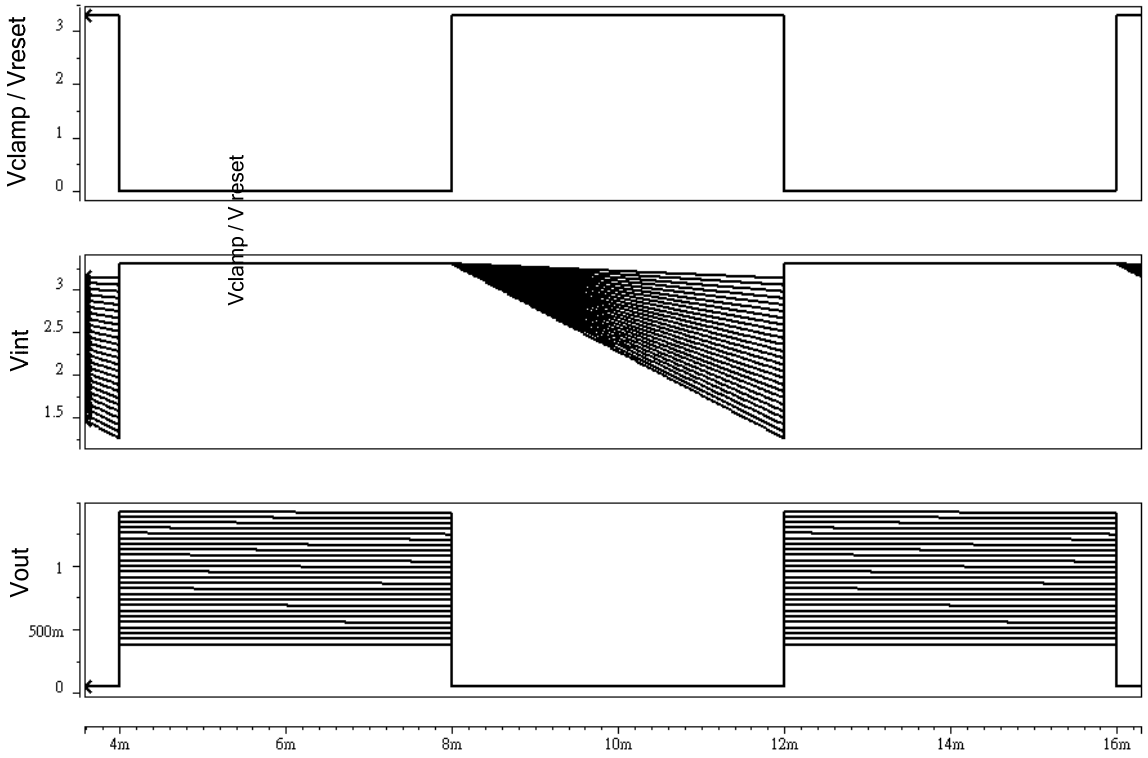


Fig. 40 The simulated waveforms of output voltage Vout for the input photocurrent from 10pA to 250pA with 10pA step.

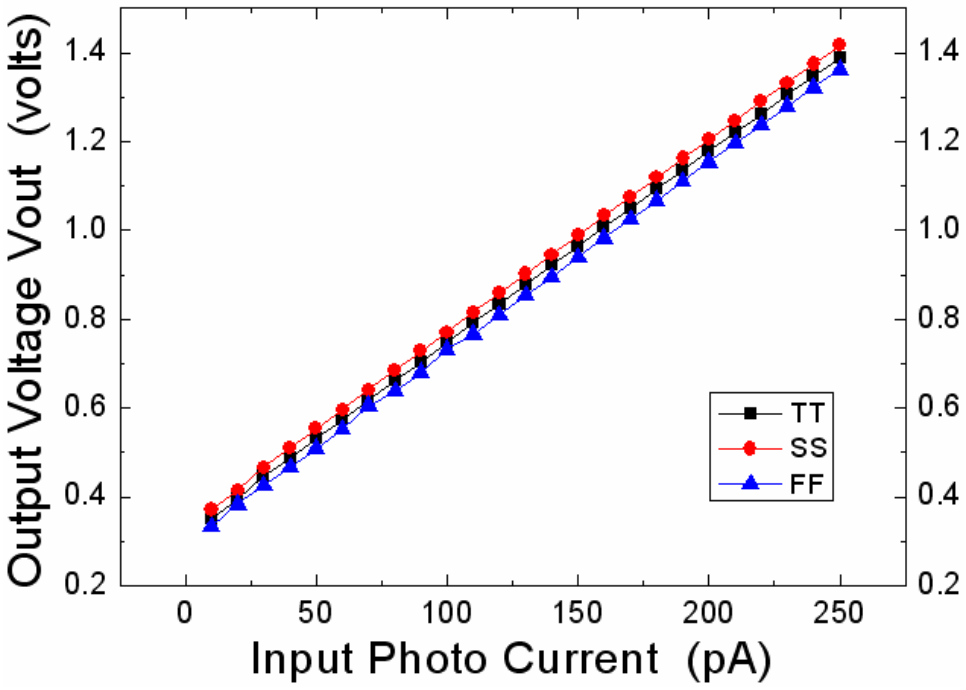


Fig. 41 The linearity of output voltage Vout for the input photocurrent from 10pA to 250pA with 10pA step.

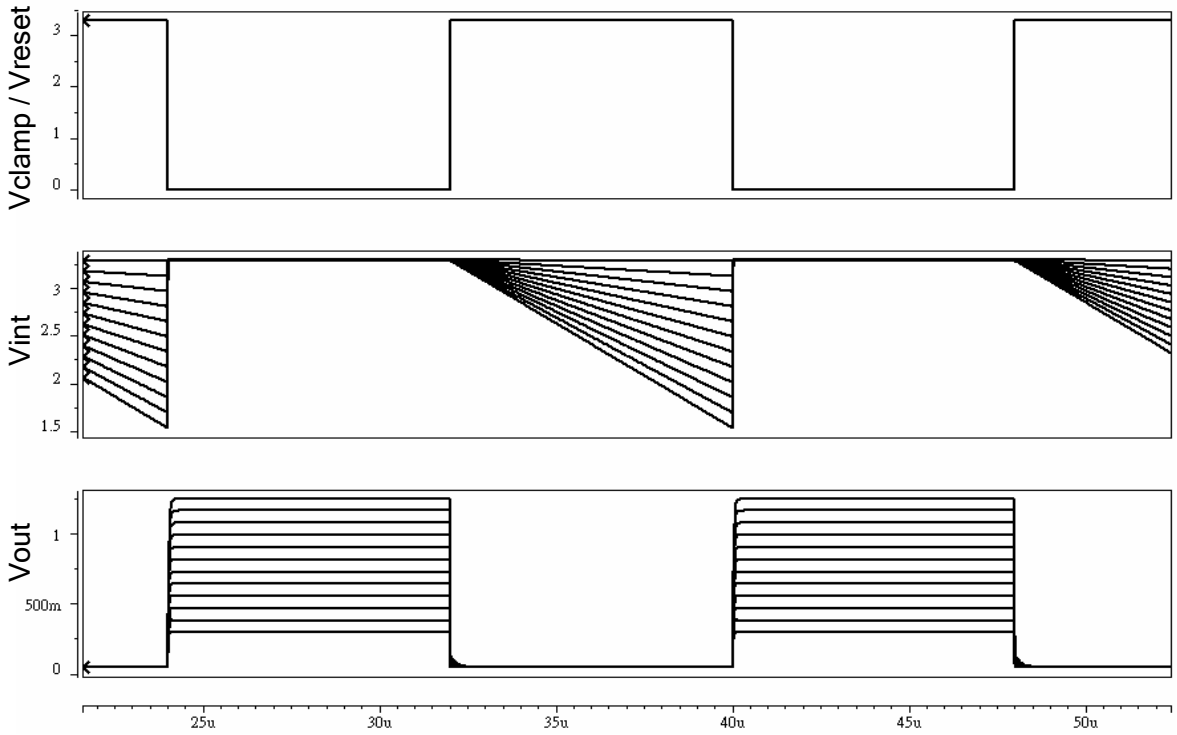


Fig. 42 The simulated waveforms of output voltage Vout for the input photocurrent from 1nA to 111nA with 10nA step.

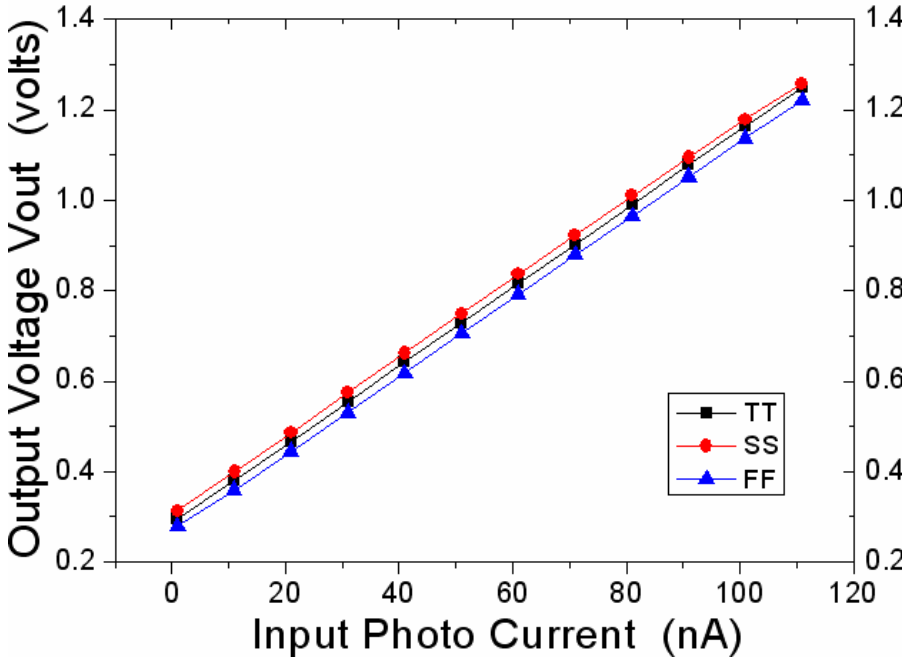


Fig. 43 The linearity of output voltage Vout for the input photocurrent from 1nA to 111nA with 10nA step.

CHAPTER 4
THE EXPERIMENTAL RESULTS

4.1 Measurement of 32 x 32 IR FPA

The die photograph of the 32 x 32 readout chip for InGaAs detector array is shown in Fig. 44. The Fig. 44 includes the 32 x 32 cell array, row digital, column digital and controlling logic. The environment setup for measuring digital function is shown in Fig. 45. The power is 3.3 volts supplied from the Agilent E3620. The clock is generated by Agilent 81110A pulse-/pattern generator. Output waveform is shown on the oscilloscope TDS 3054. The measured waveforms (Row31, Row32, Start_frame, and End_frame) of digital component are shown in Fig. 46 (a)-(d). It can demonstrate that the digital block is verified to operate appropriately.

The environment setup for measuring analog function is shown in Fig. 47. The output waveforms (Vout) is recorded by the DAQ system, the grayscale image is converted by the Labview tools. The trigger signal of DAQ system is Start_frame of digital output of 32 x 32 ROIC. The measured output waveforms (Vout = Vout_S – Vout_R) of single pixel and grayscale image with the input current signals 0nA, 1nA, 2nA, 3nA, 4nA, and 5nA are shown in Fig. 48(a) – (l). The brightness of grayscale image is proportional to output voltage (Vout). The measured output voltage (Vout) versus input current is shown in Fig. 49. In the following, the measured results of the 32 x 32 ROIC combined with InGaAs IR detector array will be discussed.

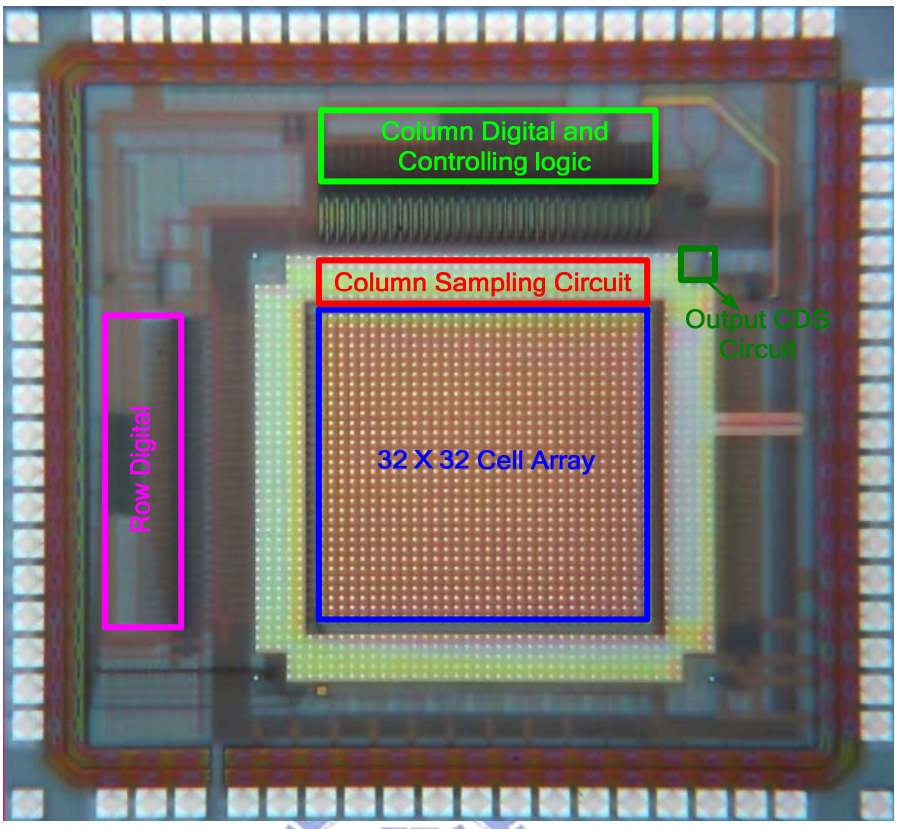


Fig. 44 Die photograph of the 32 x 32 readout chip for InGaAs detector array.

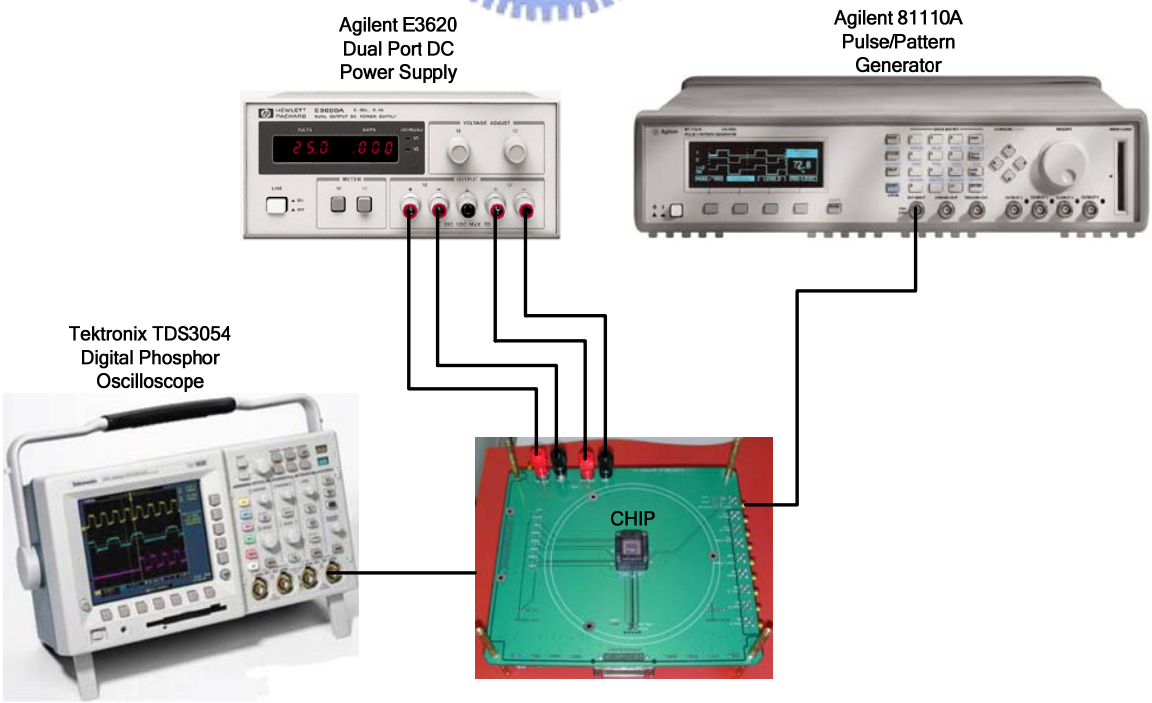


Fig. 45 The environment setup for measuring digital function.

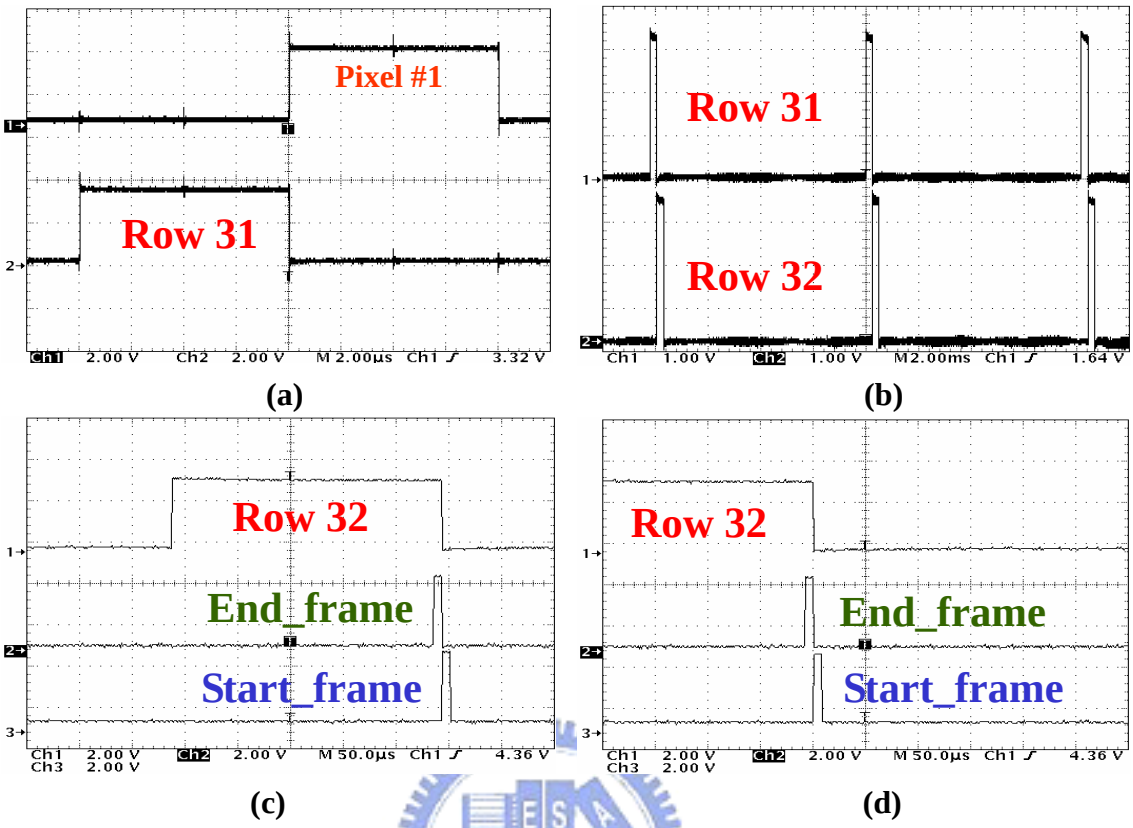


Fig. 46 The measured waveform of digital component.

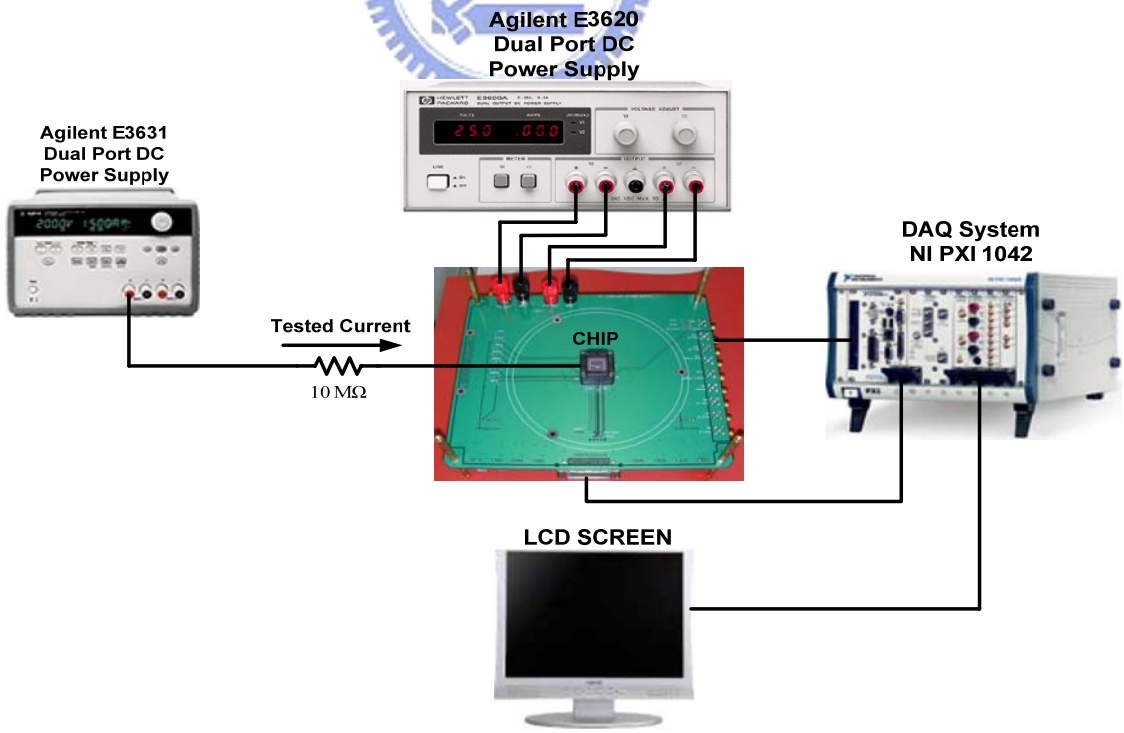
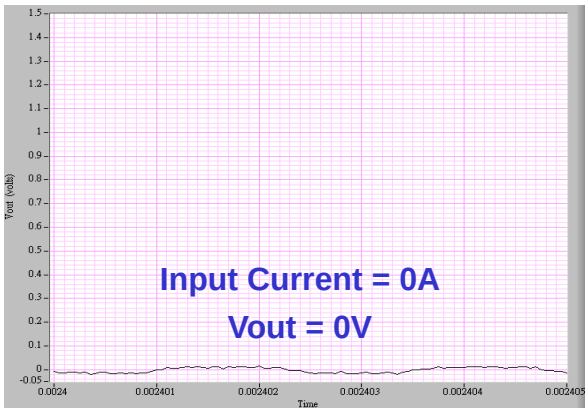
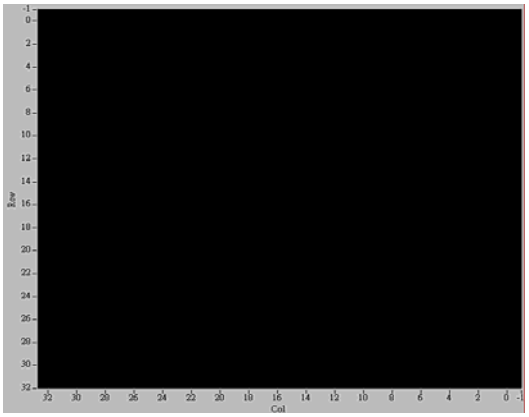


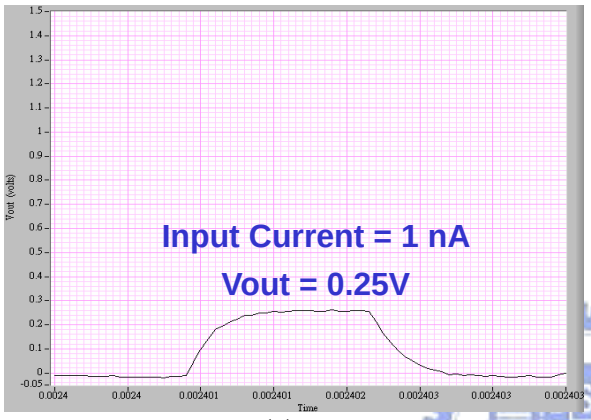
Fig. 47 The environment setup for measuring analog function.


Input Current = 0A
Vout = 0V
Vout (volts)
Time

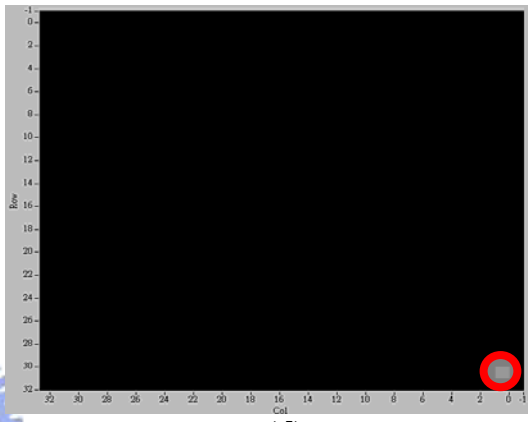
(a)


Row
Col

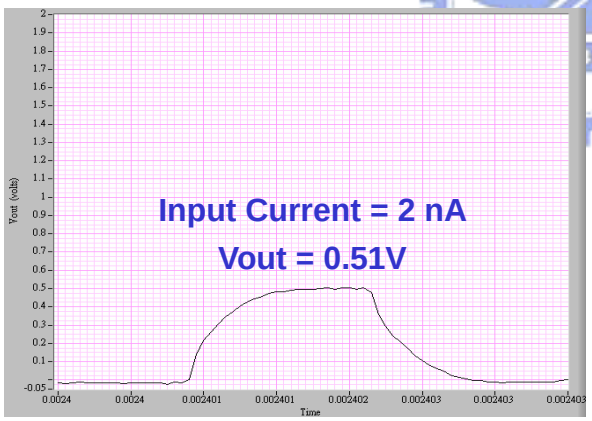
(b)


Input Current = 1 nA
Vout = 0.25V
Vout (volts)
Time

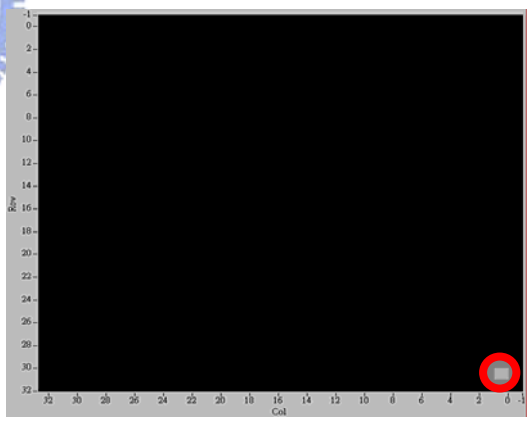
(c)


Row
Col

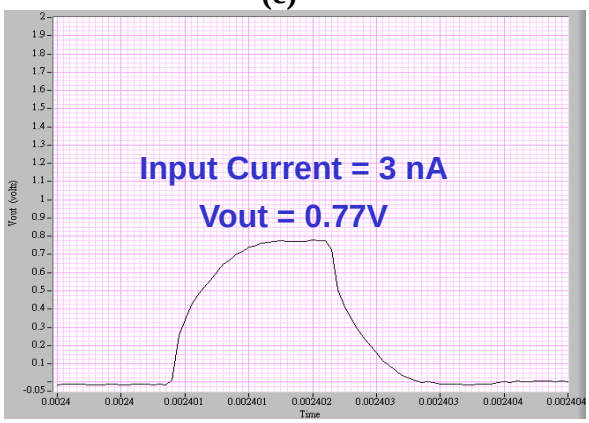
(d)


Input Current = 2 nA
Vout = 0.51V
Vout (volts)
Time

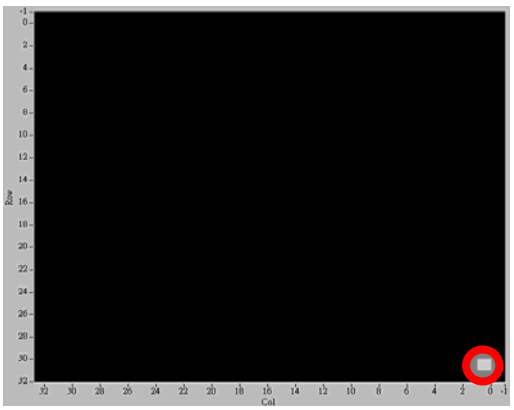
(e)


Row
Col

(f)


Input Current = 3 nA
Vout = 0.77V
Vout (volts)
Time

(g)


Row
Col

(h)

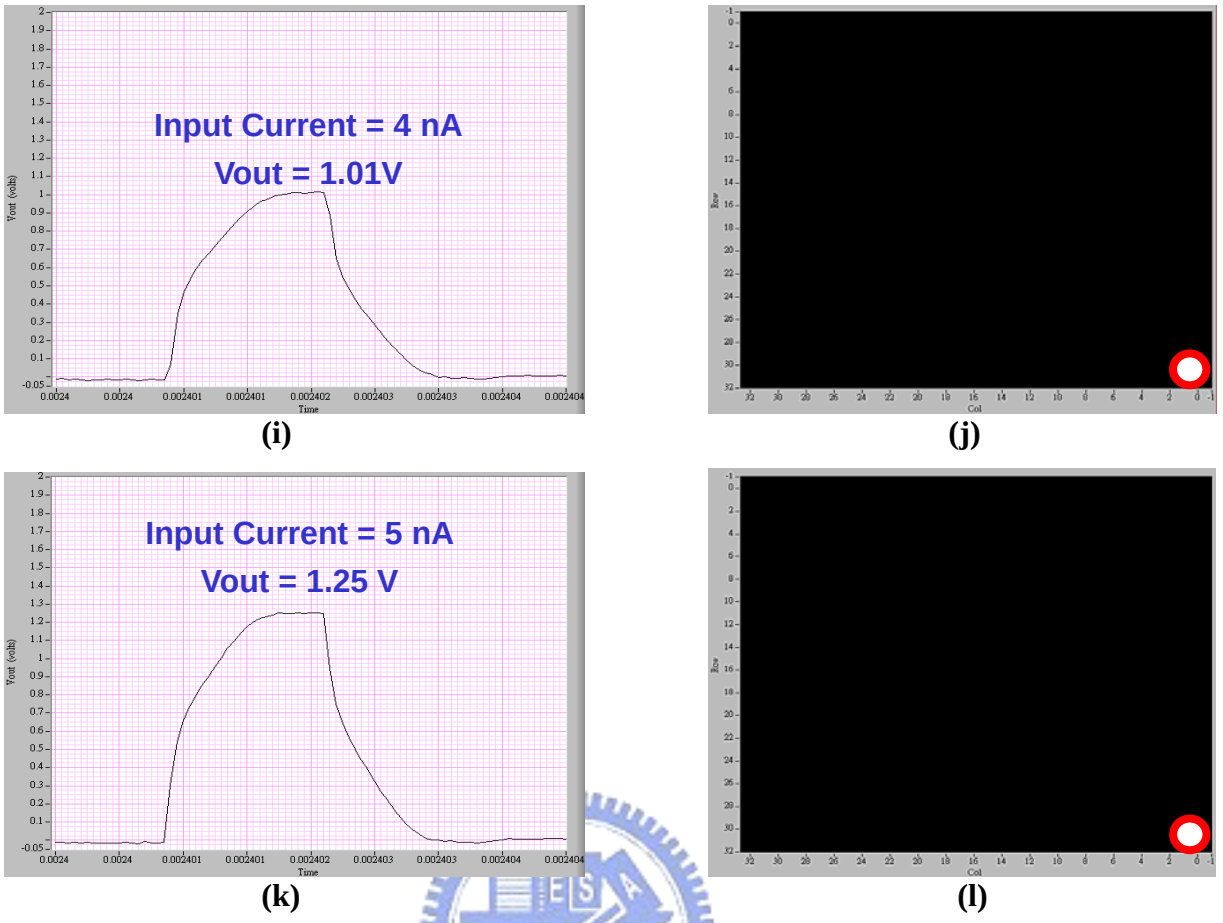


Fig. 48 The measured output waveforms (Vout = Vout_S – Vout_R) of single pixel and equivalent image under different current.

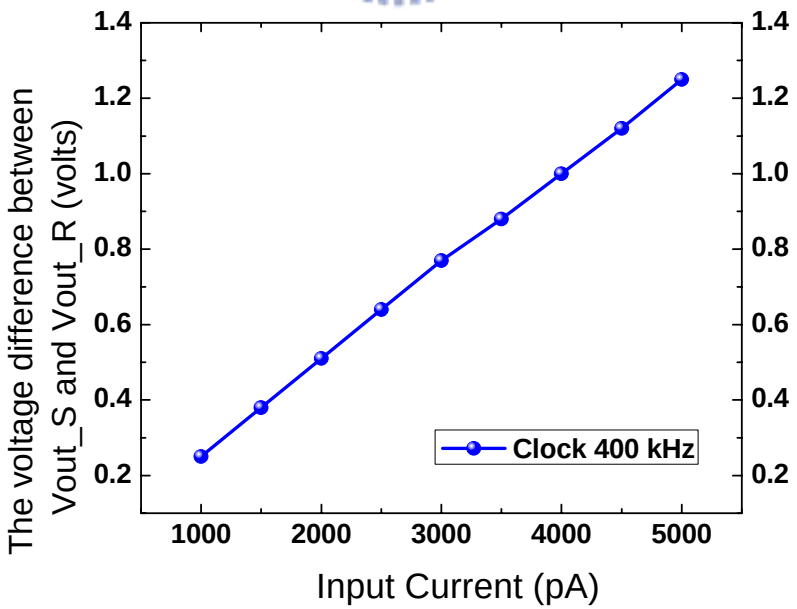
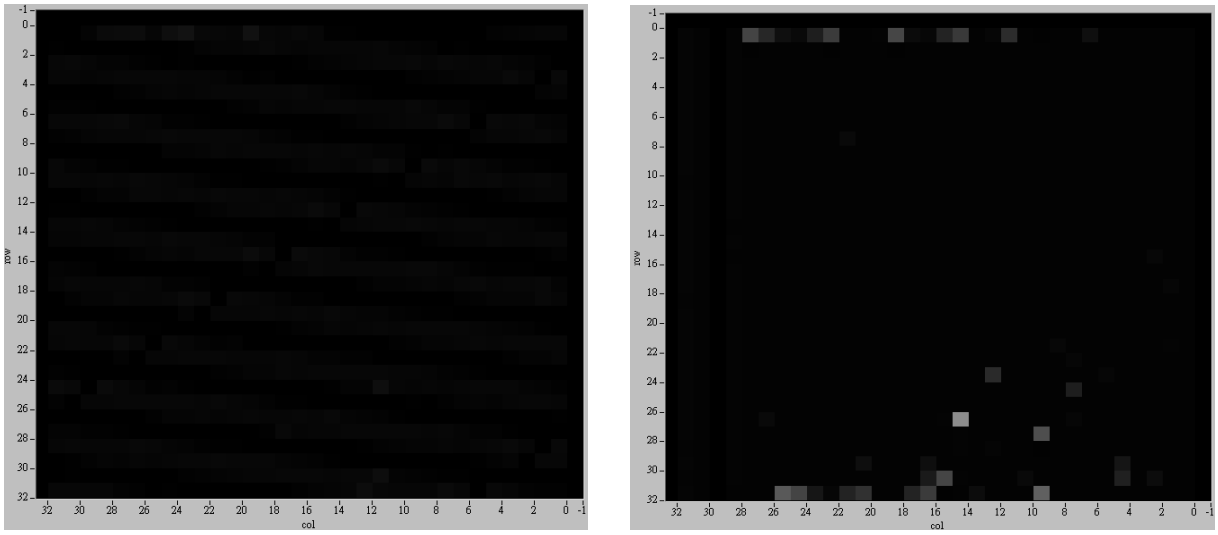


Fig. 49 The linearity of the voltage difference between Vout_R and Vout_S for input photocurrent 1000pA to 5000pA with 500pA step.

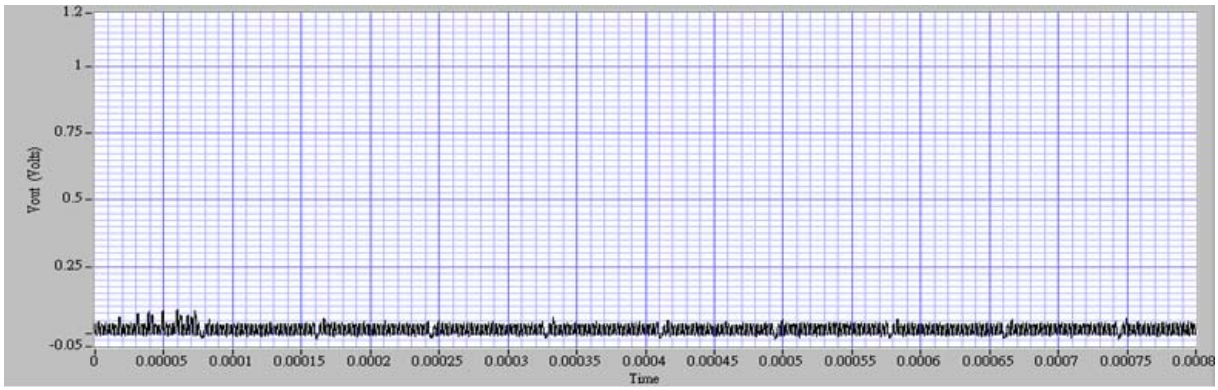
The 32 x 32 ROIC combined with InGaAs detector array has been measured under two conditions: one is illuminated under fluorescent lamp and unilluminated condition. DAQ system recorded the measured data and the data are converted to equivalent image shown in Fig. 50 (a), (b), Fig. 52 (a), (b), and Fig. 54 (a), (b) from different chip with various clock rates. The measured output voltage of CHIP_J and CHIP_F are Fig. 51 (a), (b), Fig. 53 (a), (b), Fig. 55 (a), and (b). For CHIP_J and CHIP_F, the output waveform can be observed in tens of pixels under the exposure to fluorescent lamp while the rest are pixels without response: the phenomena explain that optimization of bonding condition is not achieved.

The environment setup of measuring output voltage of pixel of 32 x 32 ROIC combined with InGaAs detector array is shown in Fig. 56. The photonetics tunable external cavity laser via single fiber illuminated this chip. DAQ system recorded the measured data and supplied system clock (400 KHz). Measured output voltage (Vout) of pixel #1 (pixel #2) of 32 x 32 readout chip combined with InGaAs detector array via laser light with wavelength 1550 nm is shown in Fig. 57 (a), (d), (g), (j), (m), and (p) with different laser power. In Fig. 57 (a) – (r), the laser power are 0 uW, 0.574 uW, 1.761 uW, 3.128 uW, 4.1573 uW, and 5.812 uW. DAQ system recorded the measured data and the data are converted to grayscale image shown in Fig. 57 (b), (e), (h), (k), (n), (q) from different laser power. The partial grayscale image of the whole array is shown Fig. 57(c), (f), (i), (l), (o), and (r). The measured output voltage of pixel #1 (Vout) versus different laser power from 0 uW ~ 7.452 uW is shown in Fig. 58. The measured output voltage of pixel #2 (Vout) versus different laser power from 0 uW ~ 5.812 uW is shown in Fig. 59. The linearity performances of pixel #1 and pixel #2 are 97.3 % and 97.2 % respectively. The summary of measured results of the 32 x 32 ROIC is listed in Table VI.

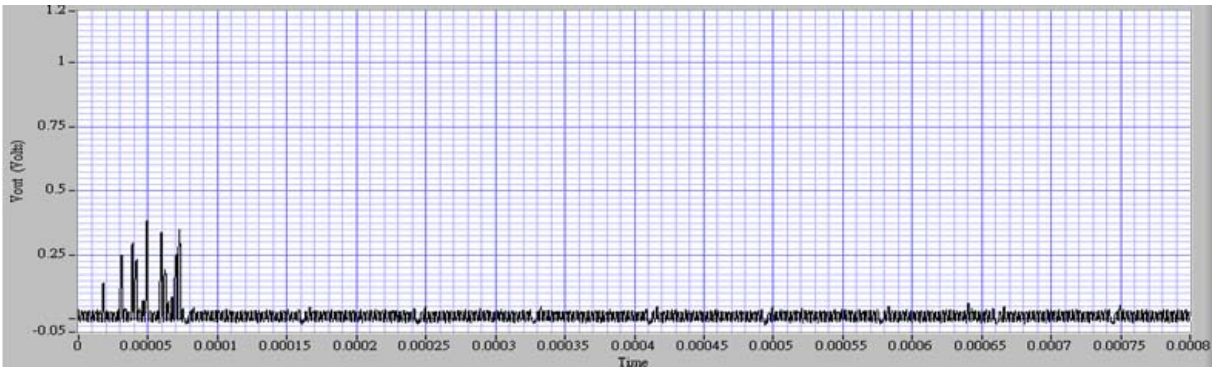


(a) unilluminated condition **(b) Fluorescent lamp**

Fig. 50 The CHIP_J (clock rate=400 KHz) combined with InGaAs detector array has been measured under two conditions: (a) unilluminated condition (b) fluorescent lamp.

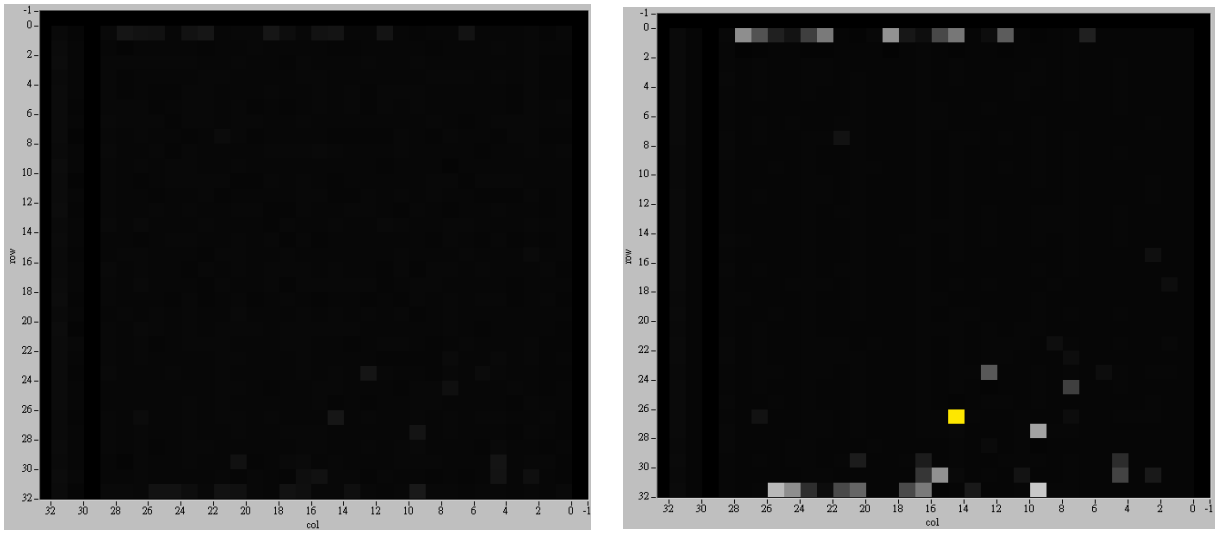


(a) unilluminated condition



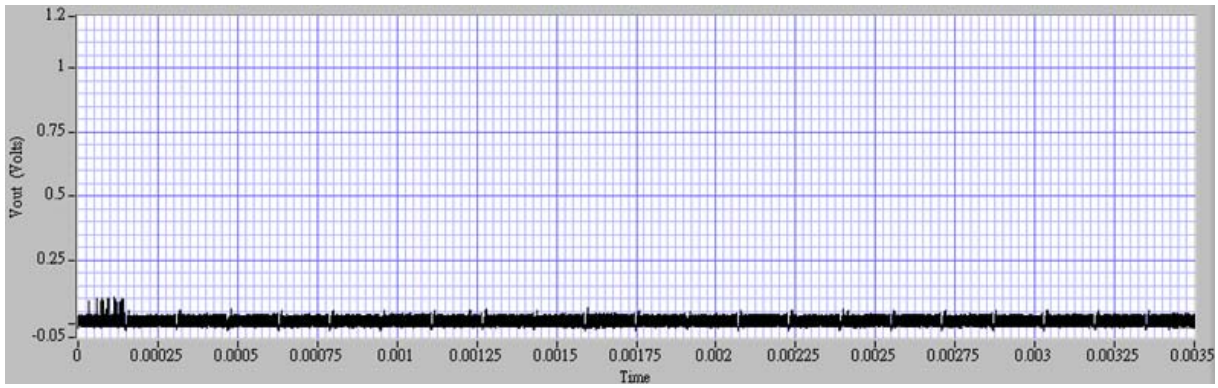
(b) Fluorescent lamp

Fig. 51 The measured output voltage (Vout) of chip_J with clock rate of 400 KHz has been measured under two conditions: (a) unilluminated condition (b) fluorescent lamp.

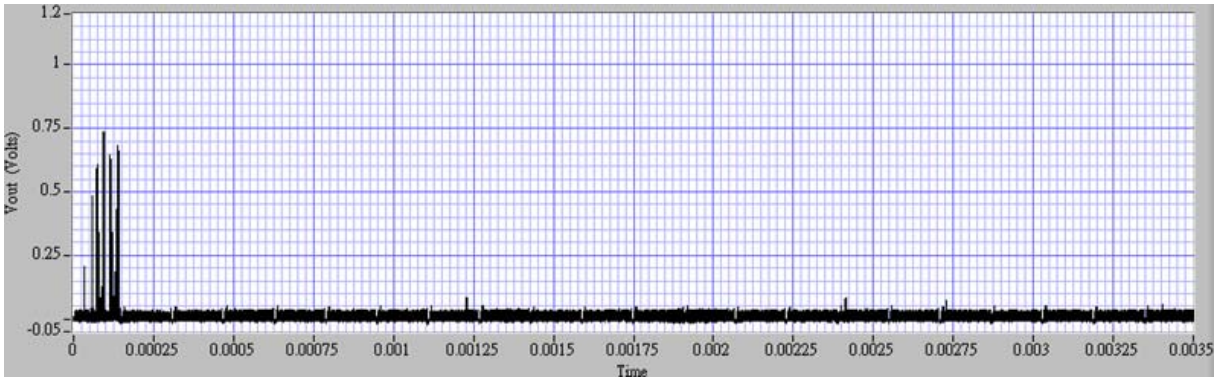


(a) unilluminated condition **(b) Fluorescent lamp**

Fig. 52 The CHIP_J (clock rate=200 KHz) combined with InGaAs detector array has been measured under two conditions: (a) unilluminated condition (b) Fluorescent lamp.

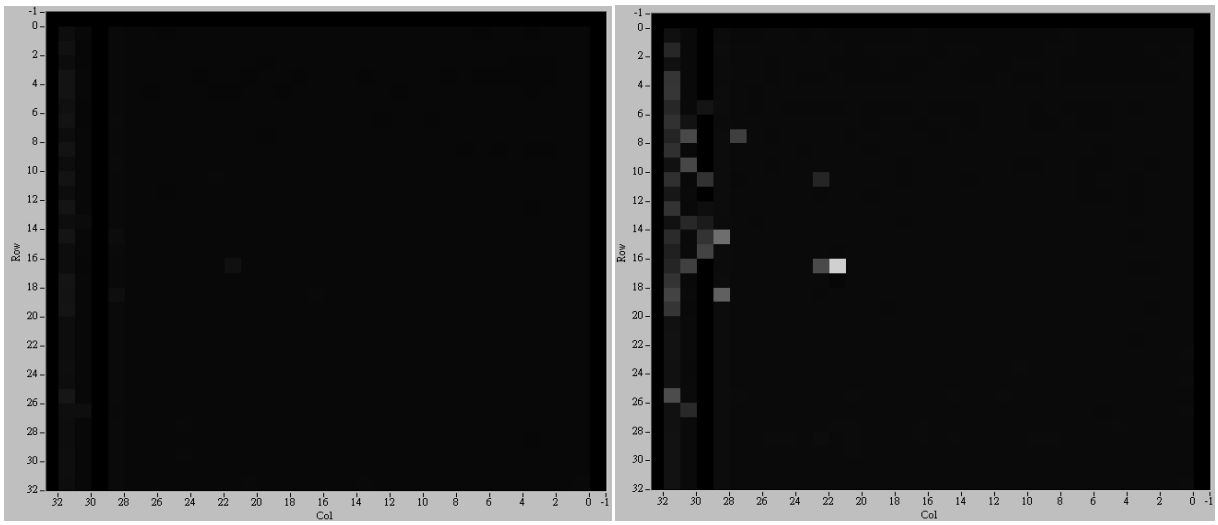


(a) unilluminated condition



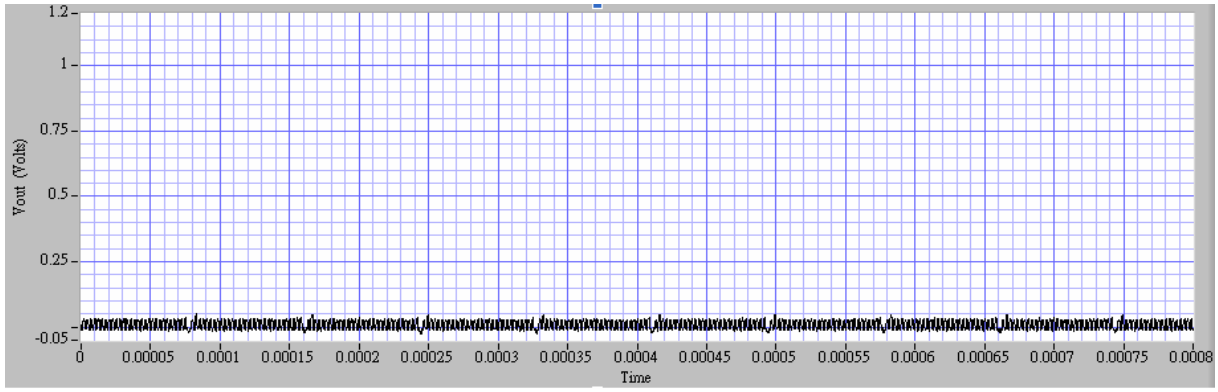
(b) fluorescent lamp

Fig. 53 The measured output voltage (Vout) of chip_J with clock rate of 200 KHz has been measured under two conditions: (a) unilluminated condition (b) fluorescent lamp.

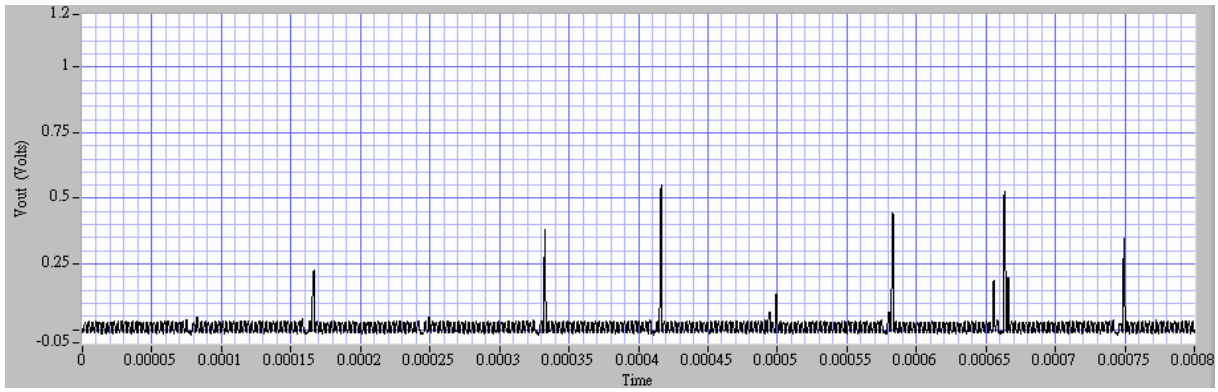


(a) unilluminated condition **(b) Fluorescent lamp**

Fig. 54 The CHIP_F (clock rate=400 KHz) combined with InGaAs detector array has been measured under two conditions: (a) unilluminated condition (b) fluorescent lamp.

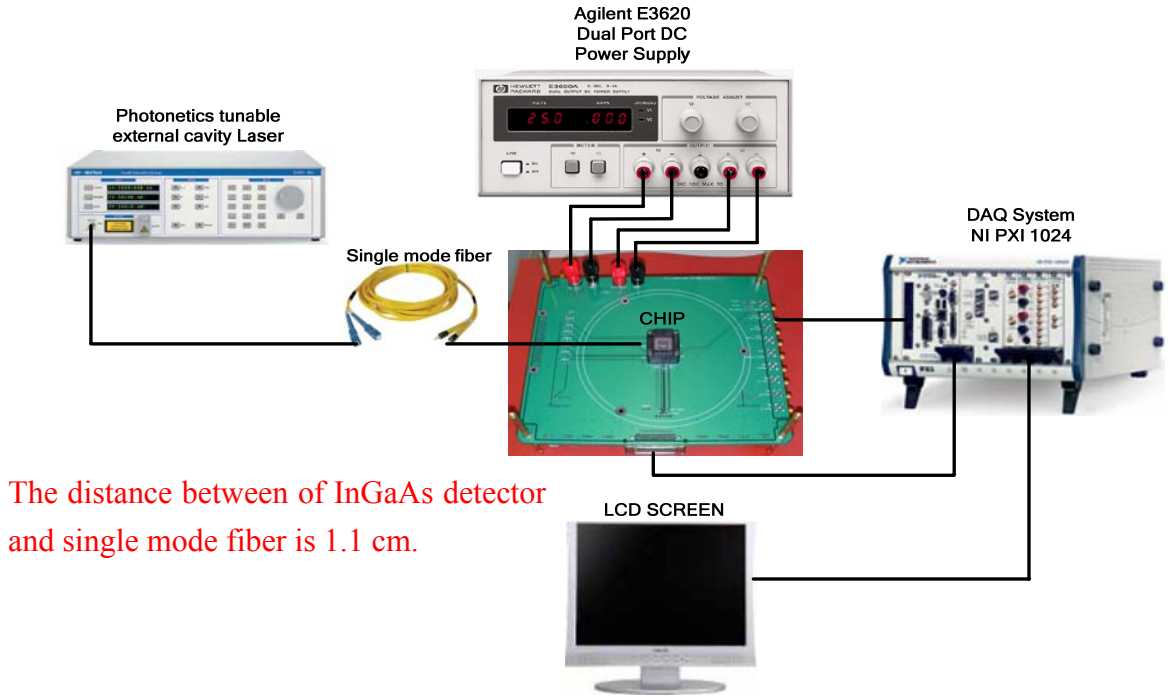


(a) unilluminated condition



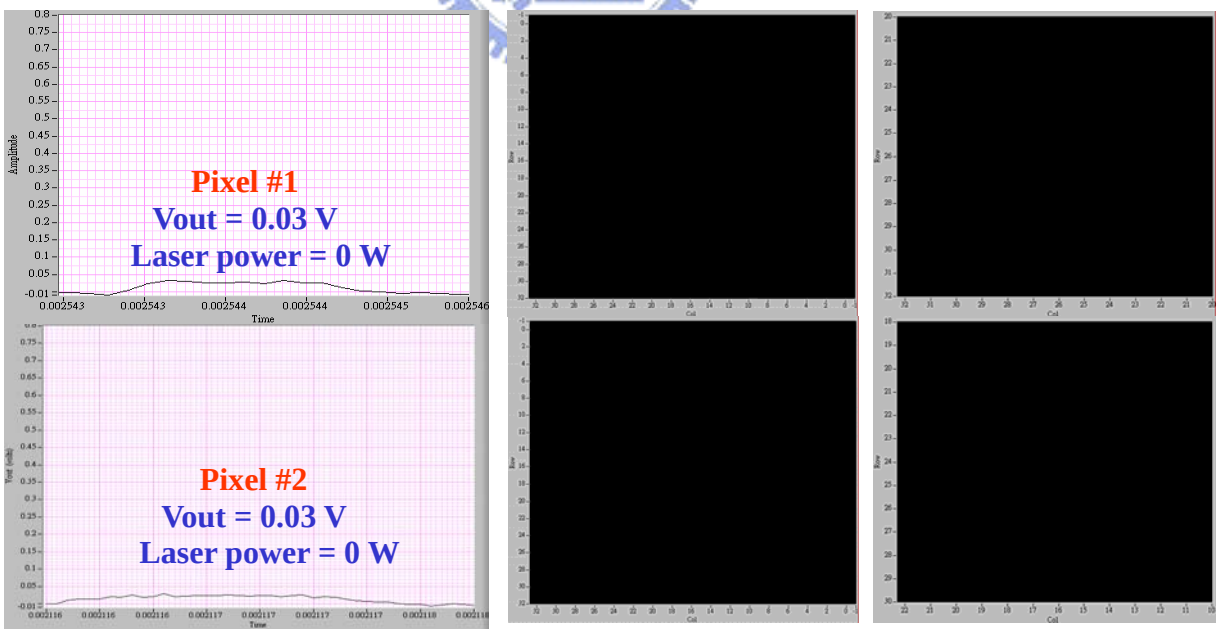
(b) fluorescent lamp

Fig. 55 The measured output voltage (Vout) of chip_F with clock rate of 400 KHz has been measured under two conditions: (a) unilluminated condition (b) fluorescent lamp.

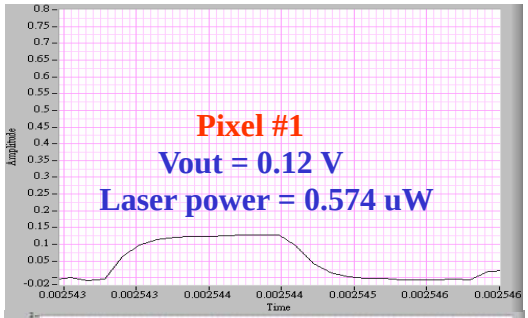


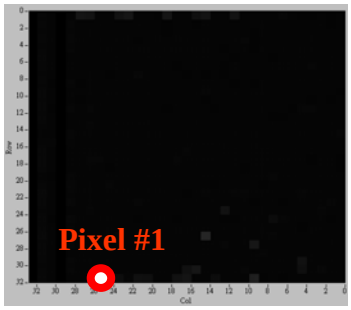
The distance between of InGaAs detector and single mode fiber is 1.1 cm.

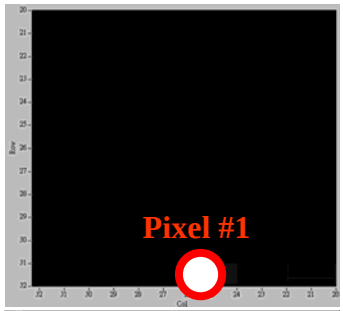
Fig. 56 The environment setup of measuring laser light.

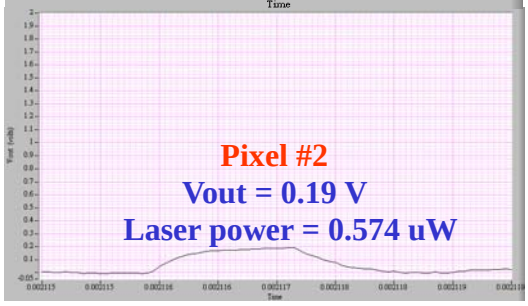


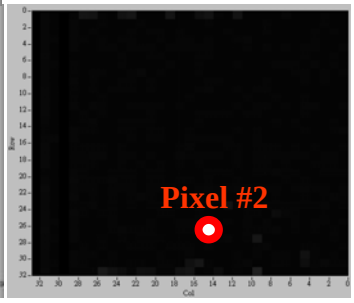
(a) (b) (c)

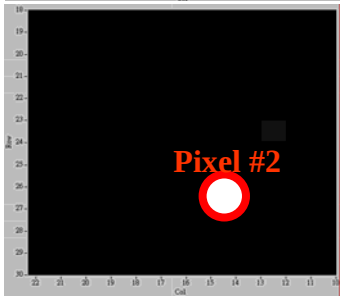

Pixel #1
Vout = 0.12 V
Laser power = 0.574 uW


Pixel #1

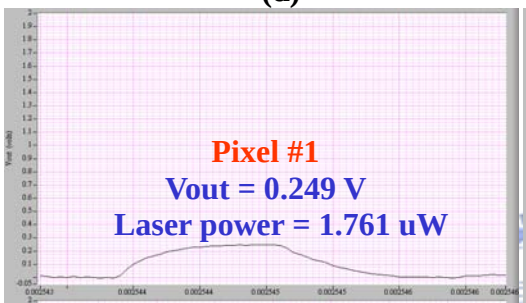

Pixel #1

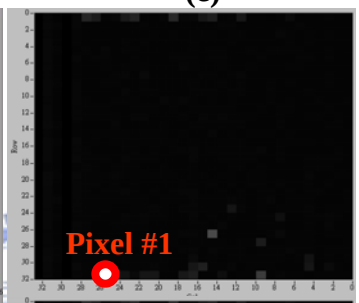

Pixel #2
Vout = 0.19 V
Laser power = 0.574 uW

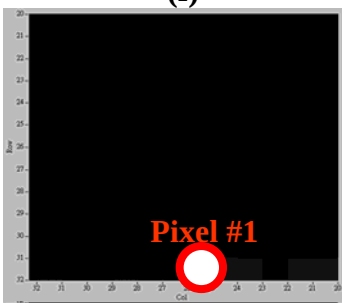

Pixel #2

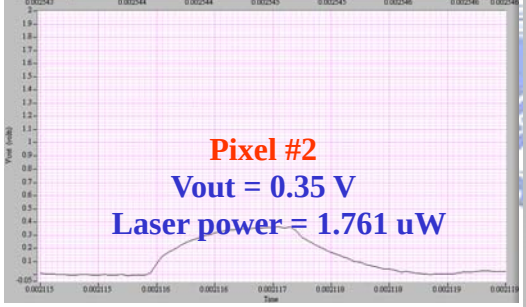

Pixel #2

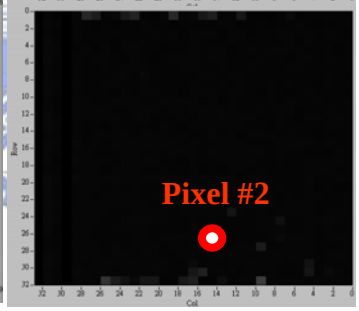
(d) (e) (f)

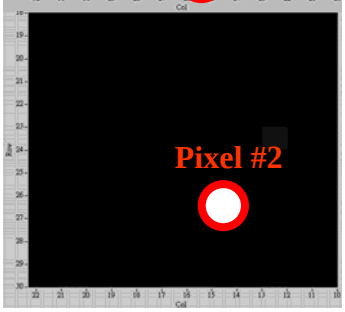

Pixel #1
Vout = 0.249 V
Laser power = 1.761 uW


Pixel #1

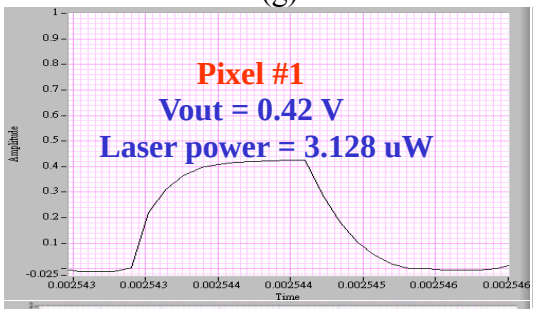

Pixel #1

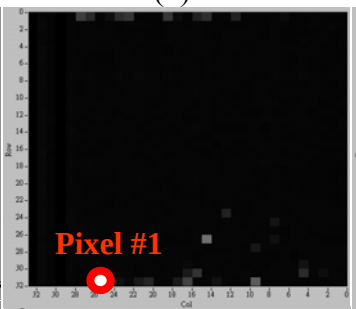

Pixel #2
Vout = 0.35 V
Laser power = 1.761 uW

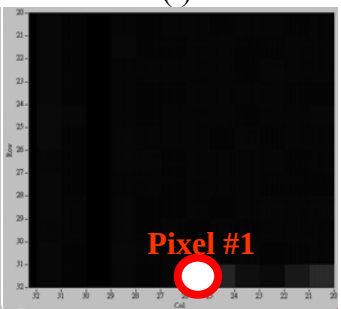

Pixel #2

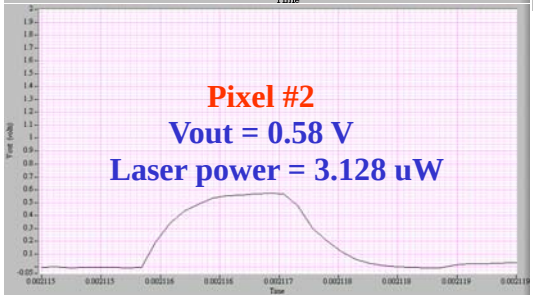

Pixel #2

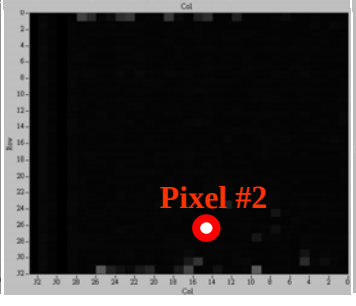
(g) (h) (i)

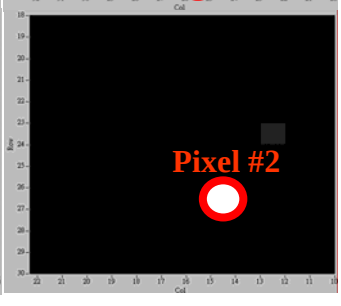

Pixel #1
Vout = 0.42 V
Laser power = 3.128 uW


Pixel #1


Pixel #1


Pixel #2
Vout = 0.58 V
Laser power = 3.128 uW


Pixel #2


Pixel #2

(j) (k) (l)

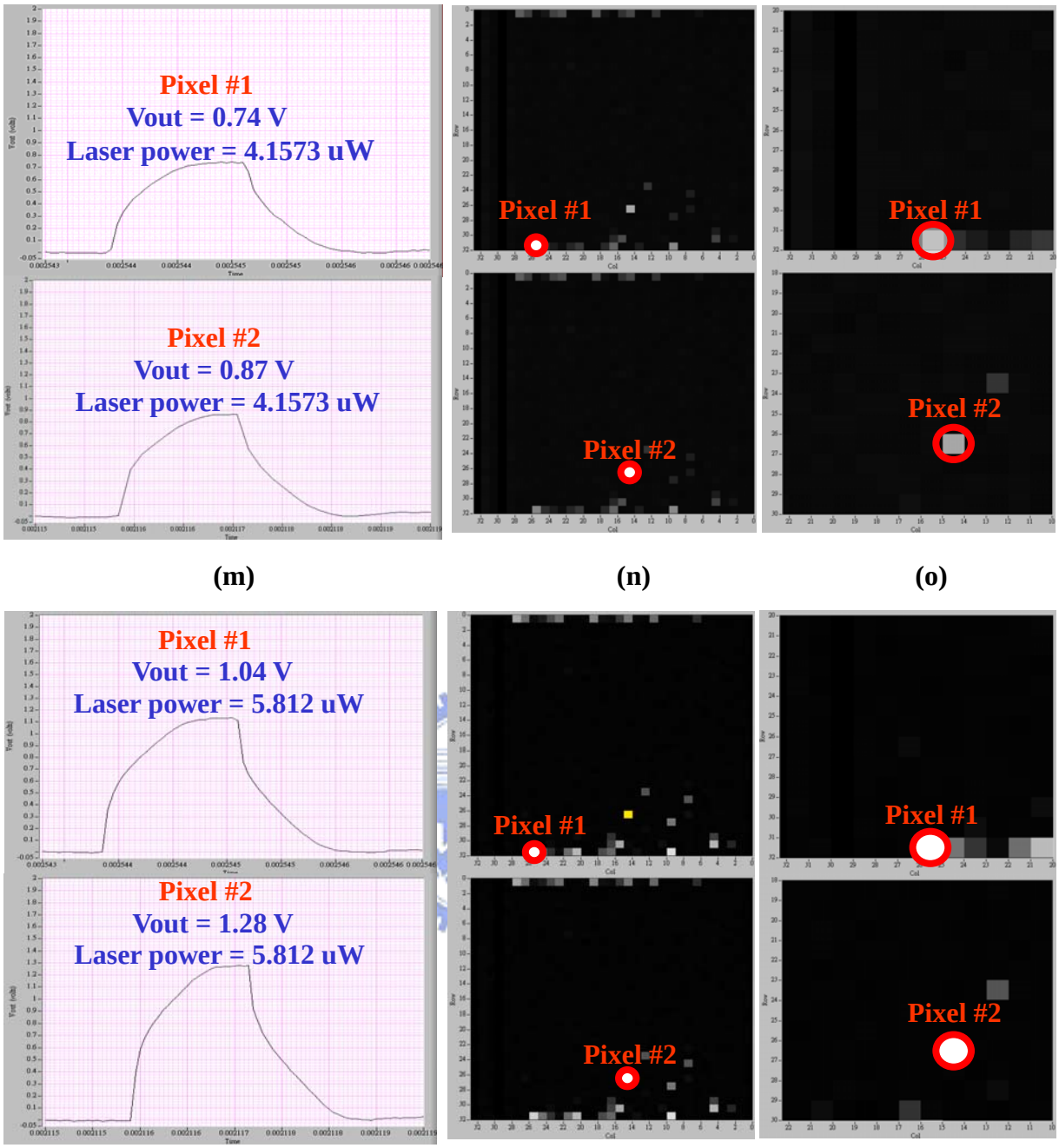


Fig. 57 The measured output voltage (Vout) of single pixel of 32 x 32 ROIC combined with InGaAs detector array via laser light with wavelength 1550 nm.

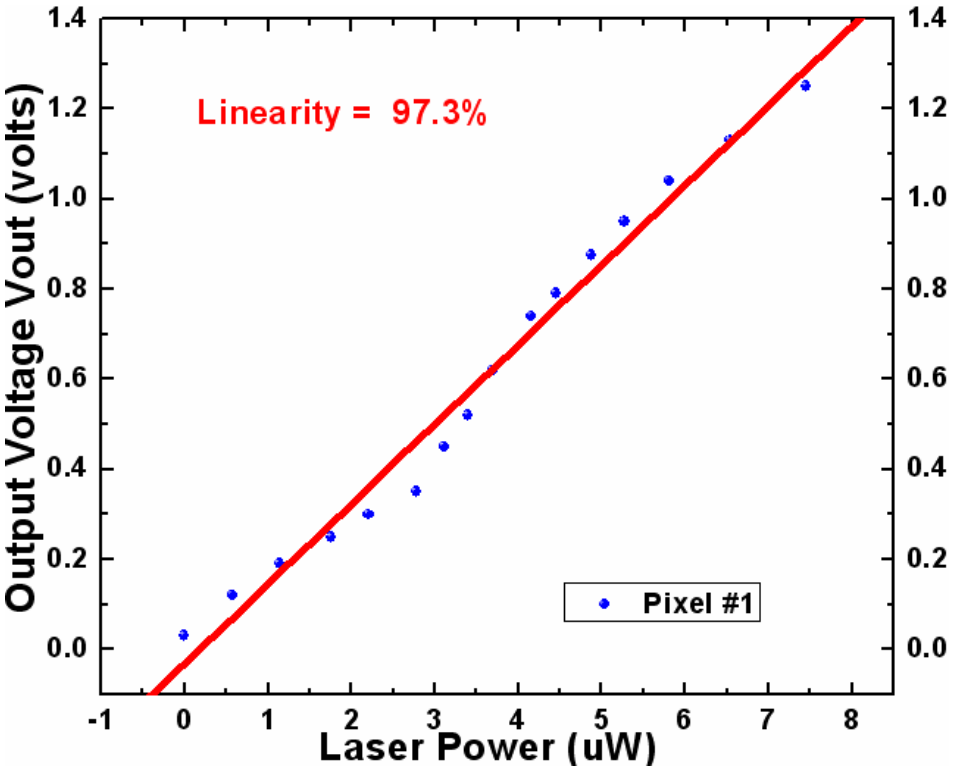


Fig. 58 The measured output voltage (Vout) of pixel #1 versus different laser power from 0 uW ～ 7.452 uW.

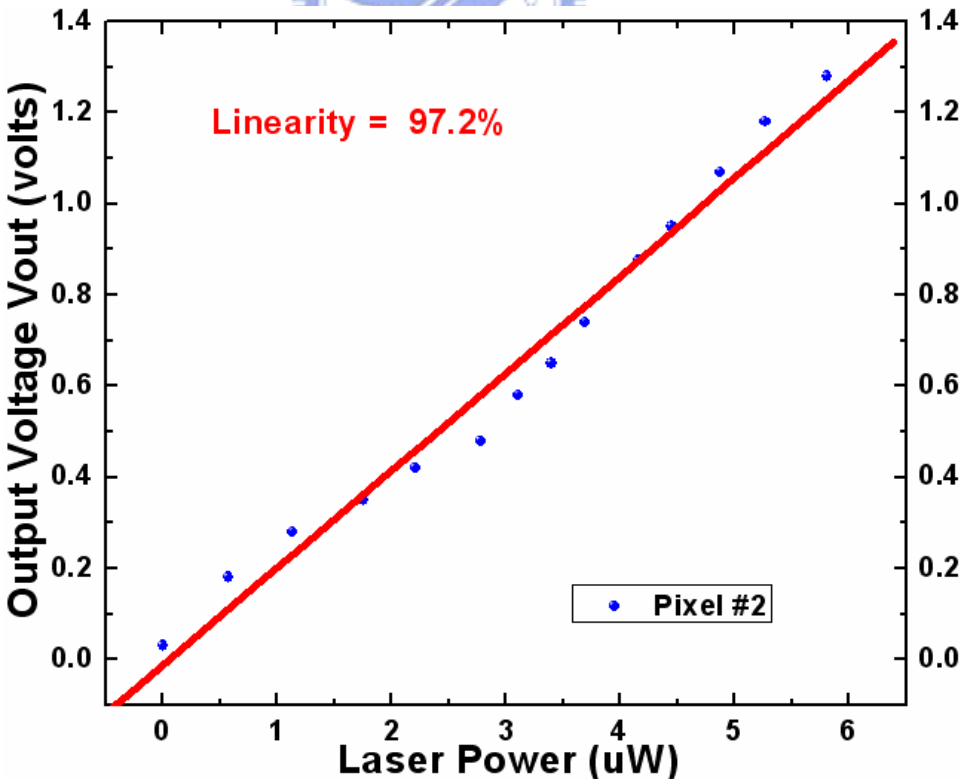


Fig. 59 The measured output voltage (Vout) of pixel #2 versus different laser power from 0 uW ～ 5.812 uW.

The measured laser power of Photonetics tunable cavity laser at around 3 uW and 5uW are shown in Fig. 60 (a) and (b) respectively. Fig. 60 (a) and (b) are measured fifty times by power meter. It can demonstrate that the laser power of Photonetics tunable cavity laser is unstable. The nonlinearity phenomenon of output voltage (Vout) under the illumination of Photonetics tunable cavity laser is caused by the unstable laser power. When laser power is unstable, the output voltage (Vout) is also changeful. The DAQ system recorded the output voltage (Vout) under the laser light, but this laser power is nonequal to the laser power by power meter because Photonetics tunable laser is unstable. The measured laser power by power meter is also nonequal to the laser power absorbed by InGaAs IR detector. The linearity performance is limited by unstable laser power. The instrument keep laser power as stable as possible, and the linearity performance can be increased.

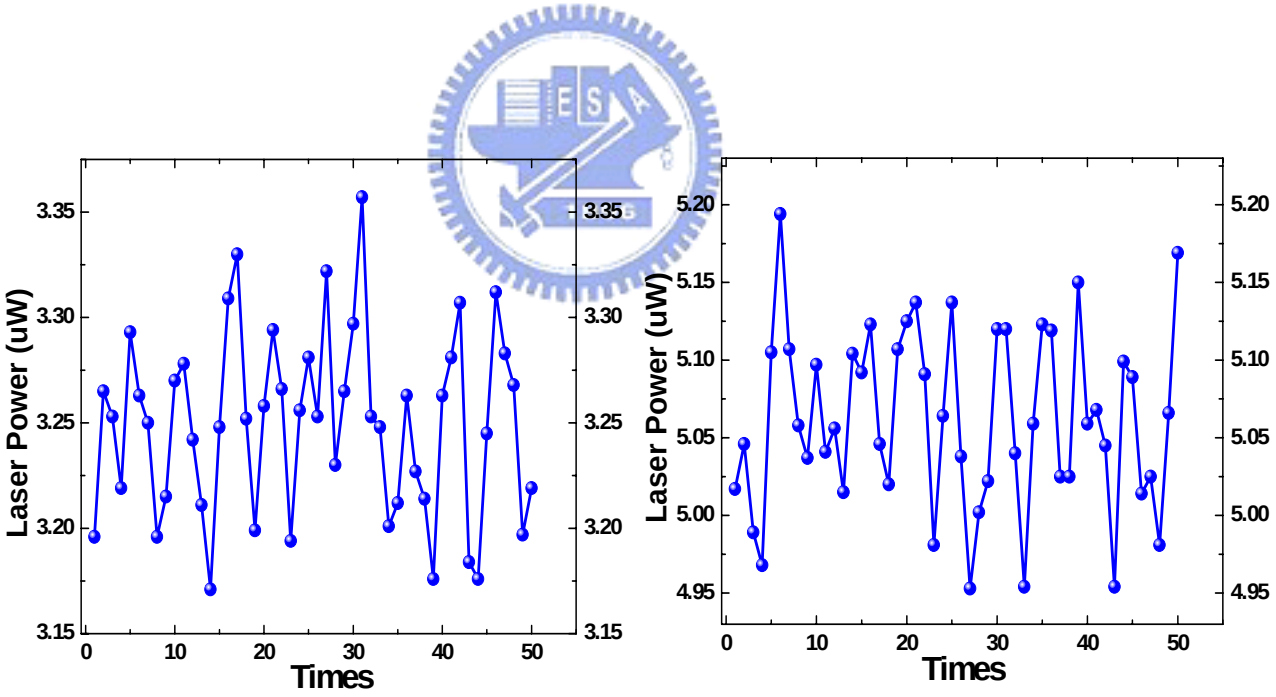


Fig. 60 The measured laser power of Photonetics tunable cavity laser. (a) around 3 uW by power meter, max = 3.322 uW, min = 3.176 uW, error = 4.6 %. (b) around 5 uW by power meter, max = 5.196 uW, min = 4.951 uW, error = 4.86 %.

Table VI The summary of measured results of the 32 x 32 ROIC.

	Simulation	Measurement
Array Size	**32 X 32**	**32 X 32**
Pixel Pitch	**30 um x 30 um**	**30 um x 30 um**
Integration Capacitance	**320 fF + 320 fF**	**————————**
Integration Time	**72.5 us**	**72.5 us**
Dark current	**< 0.5 pA**	**11.5 pA ~ 14.6 pA (bias 0V ~ -1V)**
Output Swing	**1.26 V**	**1.25 V**
Transimpedance	**5.04×10^{8} ohms**	**5×10^{8} ohms**
Power Dissipation	**16.8 mW**	**18 mW**
Optical Dynamic range	**80 dB**	**44.4 dB**
Photo-sensitivity	**1.12 uV/e^- (320 fF) 0.56 uV/e^- (640 fF)**	**1.1 uV/e^- (320 fF) 0.55 uV/e^- (640 fF)**
Linearity	**99 %**	**97 %**
Maximum Readout Speed	**0.8 M Hz**	**0.8 M Hz**
Maximum Frame Rate	**714 frame/sec**	**714 frame/sec**

4.2 Measurement of biochemical chip

This chip size is designed and fabricated in 0.35um n-well CMOS technology, and total chip area is 2700 μm x 1740 μm. The die photograph of the readout chip is shown as Fig. 61, and it is packaged to 40 pins SB40. In Fig. 61, it includes 128 x 128 photodiodes, readout circuit, and TSMC standard pads which include ESD device, pre-driver and post-driver are used.

The environment setup of functional measurement is shown in Fig. 62. The power is 3.3 volts supplied from the Agilent E3620. The clock is generated by Agilent 81110A pulse-/pattern generator. Because this chip will be used in different chemical actions, the integration time is variable through adjusting clock frequency. Output waveform is shown in the oscilloscope TDS 3054. The stable incident-light is generated by Oriel constant current power supply and illuminator.

The measured output voltage (Vout) waveforms of biochemical chip with clock frequency 125 kHz for illuminated intensity 0W, 60W, 120W, and 180W are shown in Fig. 63. The measured output voltage (Vout) versus illuminated intensity is shown in Fig. 64 where the illuminated intensity is from 0W to 220W. In Fig. 64, the linearity performance is 98.3%. The measured output voltage (Vout) waveforms of biochemical chip with clock frequency 10 kHz for illuminated intensity 0W, 15W, 30W, and 45W are shown in Fig. 65. The measured output voltage (Vout) versus illuminated intensity is shown in Fig. 66 where the illuminated intensity is from 0W to 60W. In Fig. 66, the linearity performance is 99.3%. The linearity performance will be increased if the integration time is increased by adjusting clock frequency.

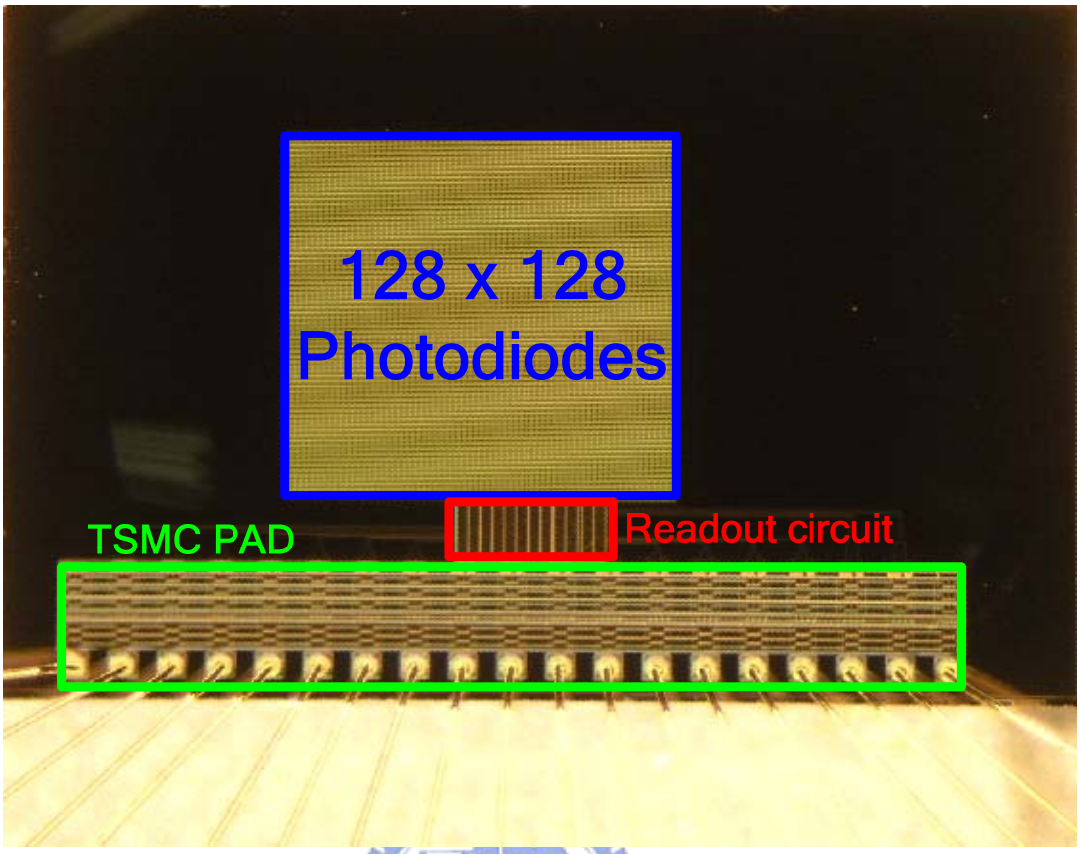


Fig. 61 Die photograph of the readout chip for detection chemiluminescence.

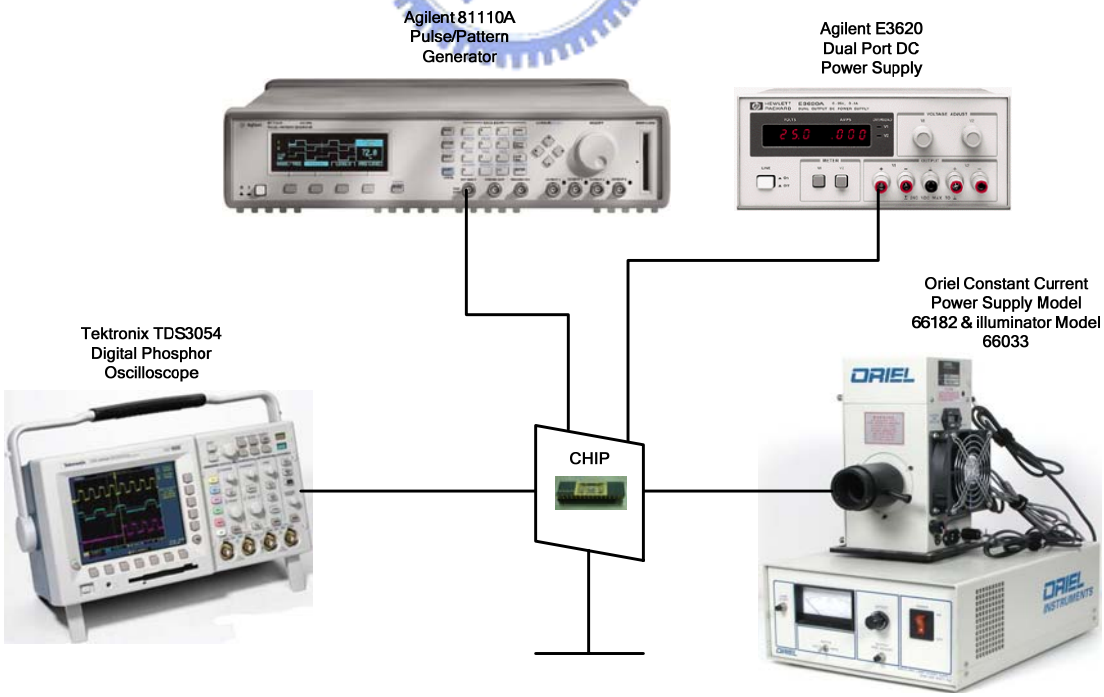
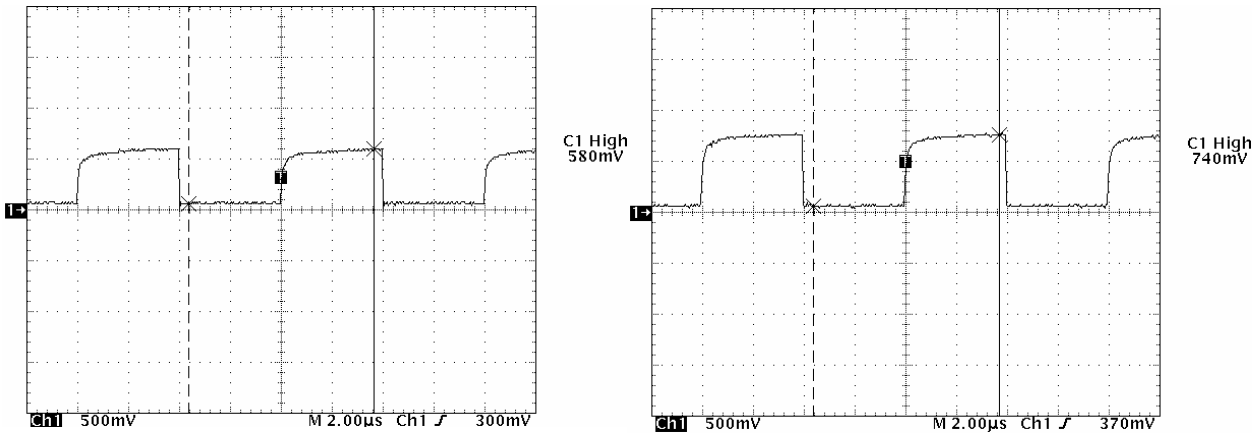
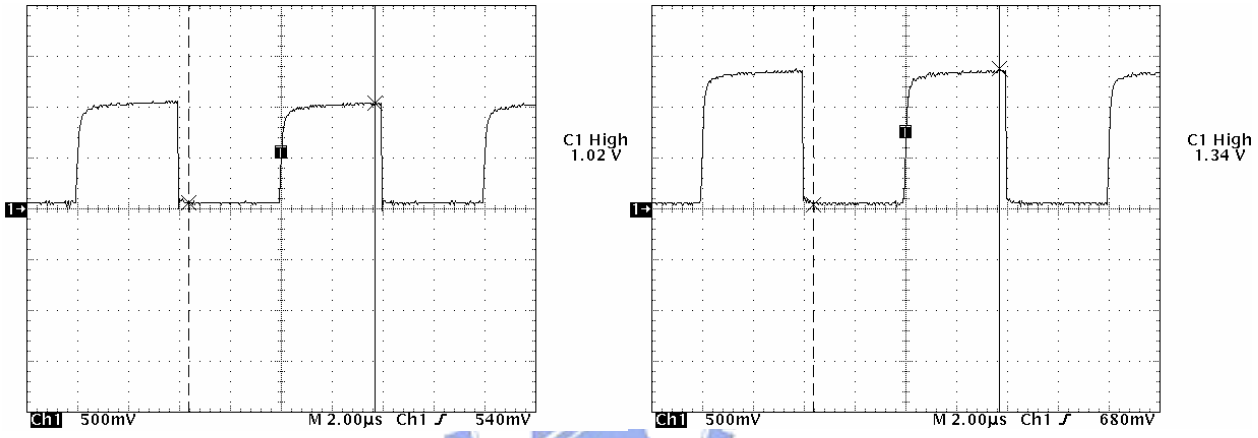


Fig. 62 The environment setup of measurement.



(a) Vout =0.58V, illuminated intensity =0W (b) Vout = 0.74V, illuminated intensity =60W



(c) Vout =1.02V, illuminated intensity =120W (d) Vout =1.34V, illuminated intensity =180W

Fig. 63 The measured Vout waveforms of biochemical chip with clock=125 KHZ.

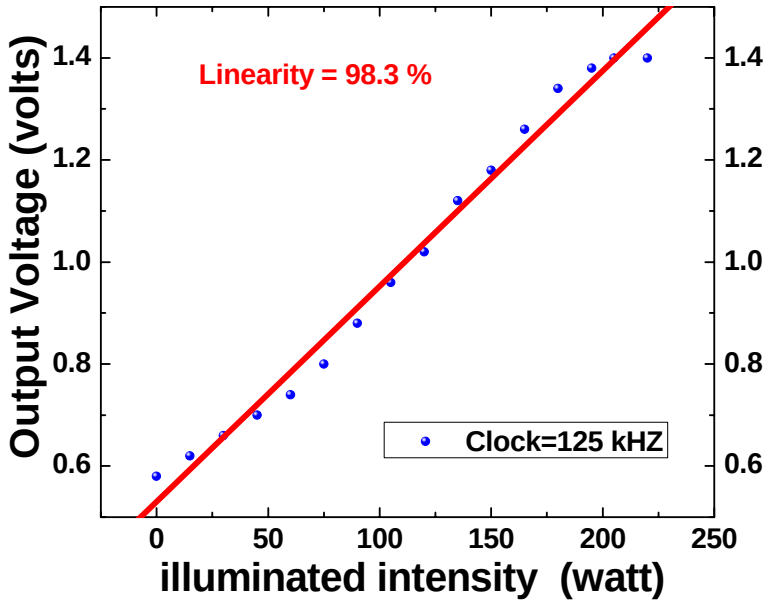
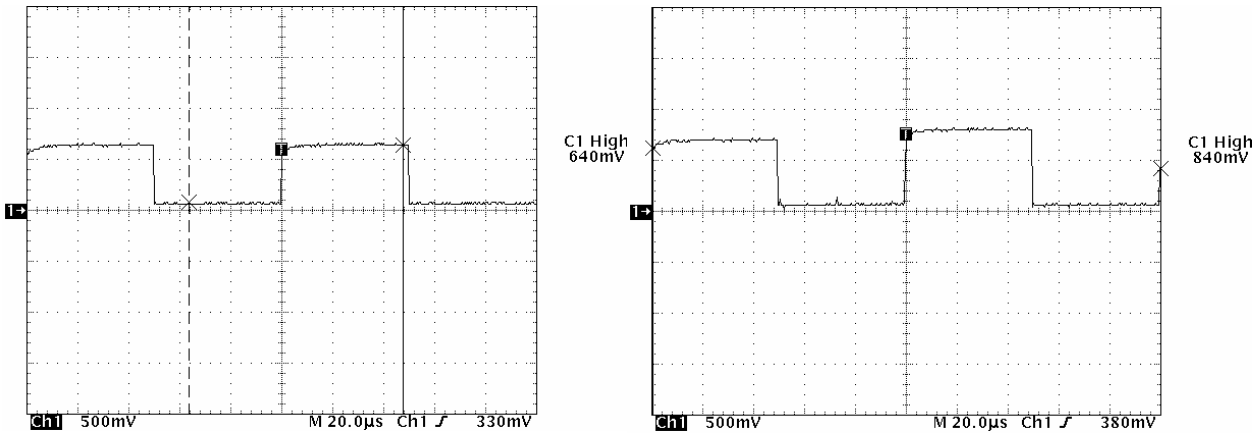
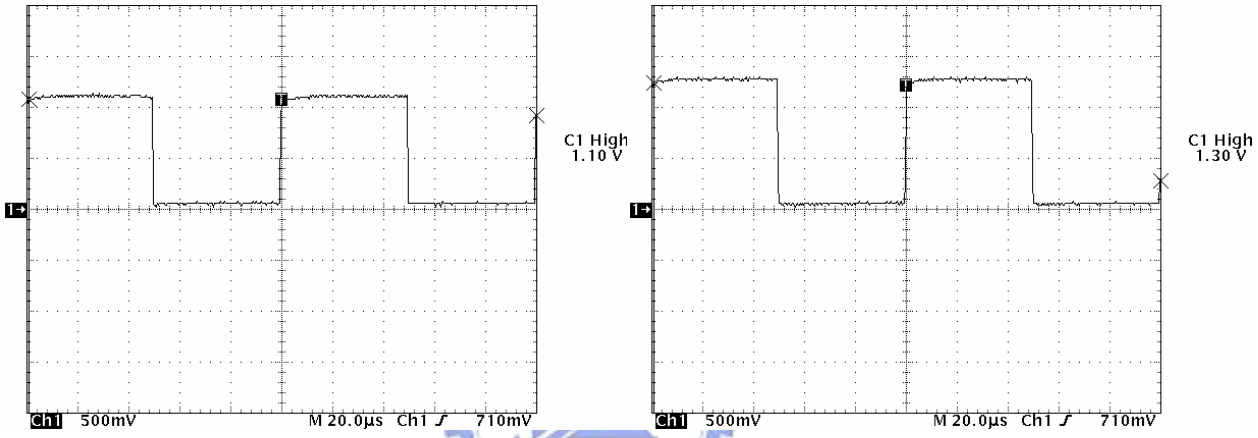


Fig. 64 The measured linearity of biochemical chip with clock = 125 KHZ.



(a) Vout =0.64V, illuminated intensity =0W (b) Vout = 0.84V, illuminated intensity =15W



(c) Vout =1.1V, illuminated intensity =30W (d) Vout =1.3V, illuminated intensity =45W

Fig. 65 The measured Vout waveforms of biochemical chip with clock=10 KHZ.

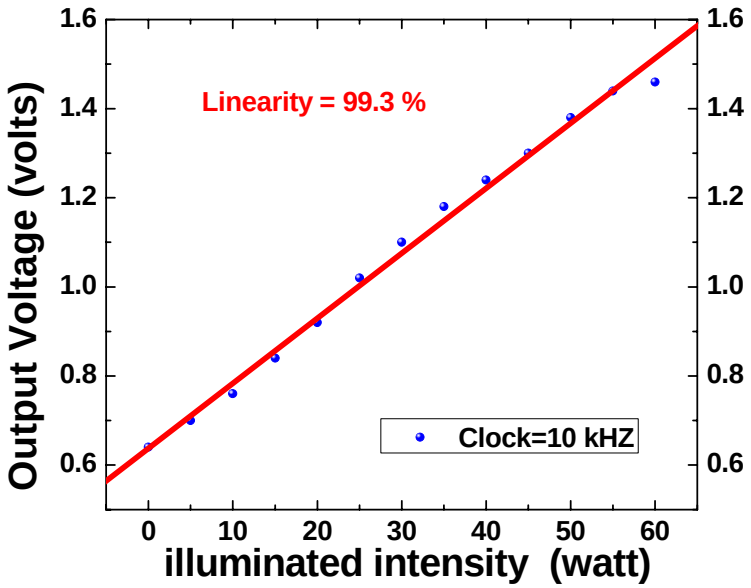


Fig. 66 The measured linearity of biochemical chip with clock = 10 KHZ.

The environment setup of measuring chemical reaction is shown in Fig. 67. The clock is generated by Agilent 8110A pulse-/pattern generator. The power is 3.3 volts supplied from the Agilent E3620. The multimeter Agilent 34401 measures the analog output data, and all measured data is stored on PC though GBIP interface. The chemical reactant is injected to a plastics vessel placed on a sheet glass, and the background luminance is generated by LED. We use phenol/4-aminoantypyrine/H2O2 chromogenic system to couple with cholesterol oxidase catalyzed reaction in order to get the enzyme kinetic analysis of cholesterol standard curve. The chemical reactions equation is shown in equation (4.1) and (4.2).

$$\text{Cholesterol} + O_2 \xrightarrow{\text{Cholesterol oxidase}} \text{Cholest-4-en-3-One} + H_2O_2 \qquad (4.1)$$

$$2\,H_2O_2 + \text{4-AAP} + \text{Phenol} \xrightarrow{\text{Peroxidase}} \text{Quinoneimine} + H_2O \qquad (4.2)$$

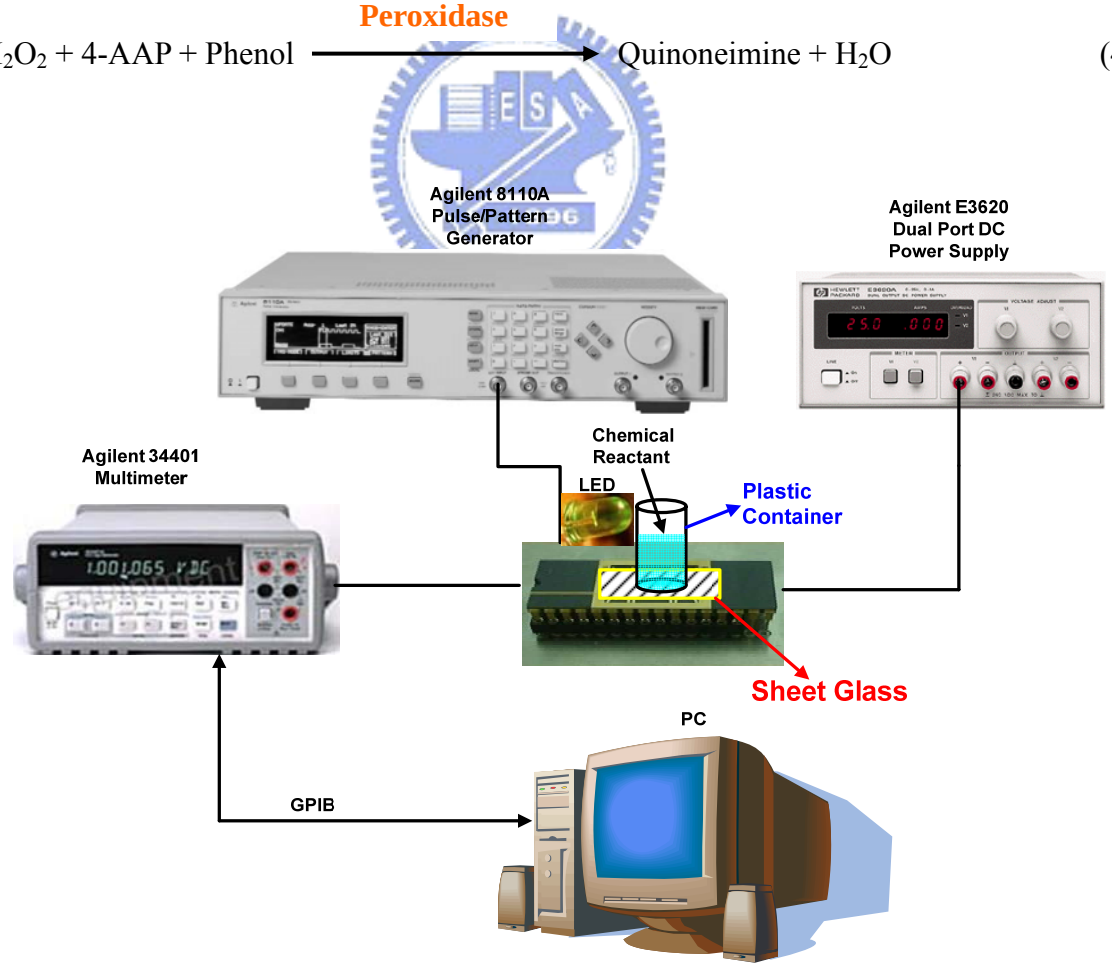
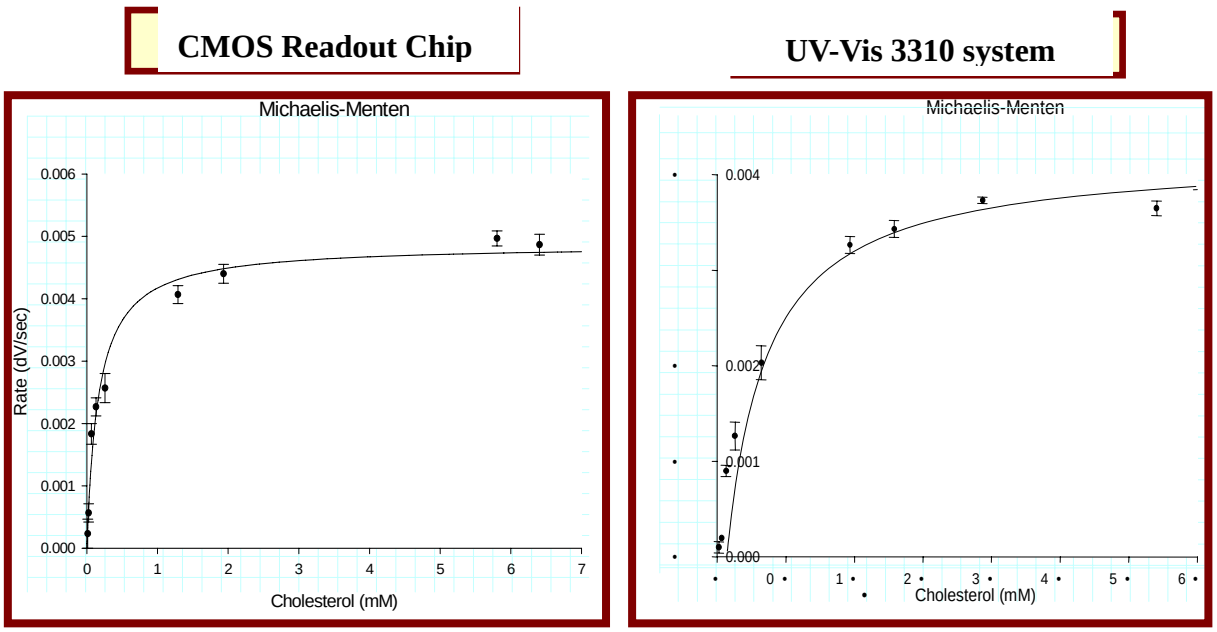


Fig. 67 The environment setup for measuring chemical reactions.

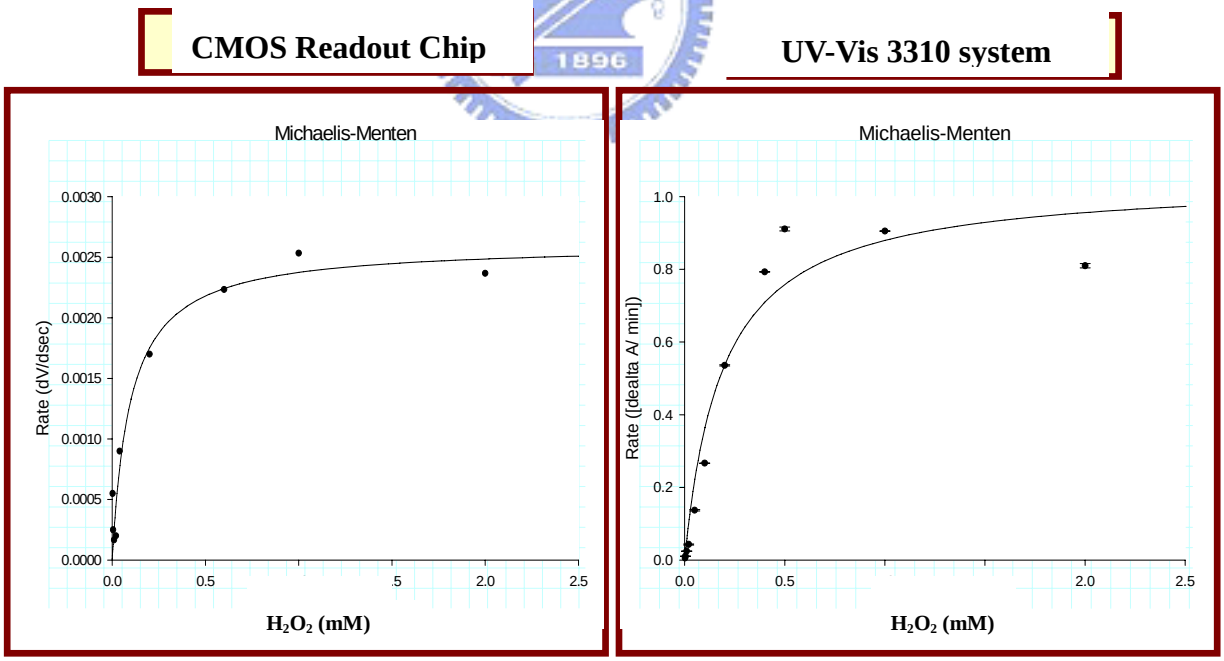
In terms of adding the cholesterol into the solution with Cholesterol oxidase and other reagents required, cholesterol will react with the oxidase to produce hydrogen peroxide. The reaction used in this practical involves hydrogen peroxide (H_2O_2) rapidly reacting with phenol and 4-aminoantipyrine in the presence of horseradish peroxidase to produce a quinoneimine chromogen which is intensely coloured with a maximum absorbance at 510 nm. Combined with the photodiode detection system, the chromogen quinoimine has an absorbance maximum and it is appeared in 510nm. Due to the light contributed to the photodiode will be absorbed by the chromogen, and the absorbance is proportional to the concentration of the product, quinoneimine, we can get the reagent concentration since we know the product concentration. And that would be a chemical quantification method for determine the cholesterol concentration.

In Fig. 68 (a) and (b), the cholesterol standard curve is measured by CMOS readout chip system and traditional UV-vis spectrophotometer (UV-3300) respectively. All the curve and Km value are obtained with Michaelis-Menten equation in enzyme kinetics analysis of Sigma Plot 2001. Enzyme kinetic analysis of cholesterol oxidase observed with our improved semiconductor sensing chip is shown in Fig. 68. The measured output voltage can be figure out the original concentration, it illustrated that this CMOS detection system have reversibility. The sensitivity of this chip can be varied through adjusting clock frequency. It has been demonstrated that the CMOS readout chip is useful to quantify human blood cholesterol assay. In Fig. 69 (a) and (b), the H_2O_2 concentration with CHOD = 0.02U, HRP = 0.016U is detected by CMOS readout chip and UV-Vis-3300 respectively. In this work, the recognizable range of H_2O_2 could be found from 0.01 mM to 0.5 mM, and the optical signal returns to stability after 0.5 mM. It has been demonstrated that the combination of CMOS photodiode, CMOS readout circuit and other commercially available electronic devices are useful to quantify biological enzyme assay.



(a) **(b)**

Fig. 68 The Coupled enzyme reaction kinetics using incubation method detected by (a) CMOS chip and (b) UV 3300 system.



(a) **(b)**

Fig. 69 The H_2O_2 concentration with CHOD = 0.02U, HRP = 0.016U detected by (a) CMOS readout chip and (b) UV-Vis-3300.

CHAPTER 5
CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

An experimental chip of 32 x 32 readout chip is designed, fabricated, and measured. When the integration capacitance is shared by one column, we must decrease total parasitic capacitance for decreasing integration time and increasing operational speed. For this reason, the Mrow is placed between MC2 and MC4 because this placing can decrease total parasitic capacitance of integration node to 43%. The integration capacitance can be selected for 320 fF or 650 fF. The optional integration capacitor is used to prevent saturation when the incident light is strong. In this thesis, 32 x 32 readout chip is first application to double delta sampling (DDS) for InGaAs IR detector array, and it increase variable circuit to turn sampling time at choice for all situations. The double delta sampling circuits are also used to suppress fixed pattern noise, clock feedthrough noise, and channel charge injection. The circuit has been fabricated with TSMC 0.35 μm double-poly-quadruple-metal CMOS process. The chip area is 2500 x 2460 μm^2 and includes 1024 pixels. The area of a single pixel is 30 x 30 μm^2. The linearity from post simulation can achieve more than 99%, and the power is 18mW. The smaller optical dynamic range is caused by underestimating the value of dark current of InGaAs detector. Nonlinearity phenomenon of output voltage (Vout) under the illumination of Photonetics tunable cavity laser is caused by the unstable laser power.

An experimental chip of 320 x 256 readout chip is designed and simulated. It contains a high swing cascade current mirror to increases the output range, and the current gain 6 and 60 are selectable for weak and strong photo-current. There is an integration capacitance in every pixel to increase the readout speed. The output stage is composed by correlated double

sampling (CDS) stage and dynamic discharge output stage. The chip area is 10500 x 8650 μm^2 and includes 81920 pixels. The area of a single pixel is 30 x 30 μm^2. The linearity from simulation can achieve more than 99%, and the power is 103.7 mW.

An experimental chip of biochemical chip is designed, fabricated, and measured. The purpose is replaced UV-vis spectrophotometer (UV-3300) by this biochemical chip. We can believe that the variation of colorimetric signal could be detected by the biochemical chip and establish the linear detection curve. This chip is with great potential to have the same sensitivity as the commercial self-integrated photodiode system. In the future, we still need to establish the realizable calibration curve and enhance the sensitivity to make it more sensitive and very useful in clinical applications.

5.2 Future work

In 32 x 32 IR FPA, the bonding condition is one of challenge problems to be solved. This integrated chip is feasible to capture the grayscale image in the future. The 320 x 256 readout chip will be fabricated and measured. In biochemical chip, we still need to establish the realizable calibration curve and enhance the sensitivity to make it more sensitive and very useful in clinical applications.

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THE ANALYSIS AND DESIGN OF NEW CMOS CURRENT READOUT INTEGRATED CIRCUIT FOR INFRARED DETECTOR ARRAY AND IMAGE APPLICATIONS