用低壓元件實現之混合電壓共容石英振盪電路設計

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摘要

隨著互補式金氧半（CMOS）製程技術進步至奈米尺寸（Nanometer-Scale），為了要在一個較低的供應電壓（1xVDD）下能提供更快的操作速度，閘極氧化層的厚度也必須跟著下降，然而在電路板上的電壓準位為了能相容於較早期的微電子系統介面規格，有可能還維持在較高的電壓準位（2xVDD 或是更高），所以針對此種混合電壓共容應用的輸入輸出介面電路設計上，則要考量閘極氧化層可靠度（Gate-Oxide Reliability）、熱載子衰退效應（Hot-Carrier Degradation）以及漏電流（Leakage Current）等的問題。

在本篇論文中，提出了三種混合電壓介面電路，第一個電路是使用閘極電壓追隨電路（Gate-Tracking Circuit）以及動態 N 型井偏壓電路（Dynamic N-Well Bias Circuit）實現之混合電壓輸入輸出緩衝器（Mixed-Voltage I/O Buffer），目的是為了改善之前的混合電壓輸入輸出介面電路的一些問題，第二個電路是新提出的混合電壓石英振盪電路一，第三個電路是新提出的混合電壓石英振盪電路二，上述所提之三個電路皆以低壓元件實現之，且成功克服在混合電壓介面下的閘極氧化層可靠度問題。上述所提之三個混合電壓介面電路皆已在 1.2 伏 0.13 微米互補式金氧半製程裡實現，用以操作在 1.2/2.5 伏的混合電壓介面下；並且針對第二及第三個新提出的混合電壓石英振盪電路，又另外實現在 1 伏 90 奈米互補式金氧半製程中，用以操作在 1/1.8 伏的混合電壓介面。

Circuit Design of Crystal Oscillator in Mixed-Voltage-Tolerant I/O Interfaces with Low-Voltage Devices

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ABSTRACT

In the nanometer-scale CMOS technology, the gate-oxide thickness has been scaled down to support a higher operating speed under a lower power supply (1xVDD). However, the board-level voltage levels could be still in a higher voltage levels (2xVDD, or even more) for compatible to some earlier interface specifications in a microelectronics system. The I/O interface circuits have been designed with considerations on the gate-oxide reliability, leakage current and hot-carrier degradation in such mixed-voltage applications.

In this thesis, three kinds of mixed-voltage interface circuits are presented, The first is the mixed-voltage I/O buffer with gate-tracking circuit and dynamic n-well bias circuit for improving some drawbacks of the prior ones, the second is the new proposed mixed-voltage crystal oscillator circuit Ⅰ and the third is the new proposed mixed-voltage crystal oscillator circuit II. All of these three circuits have been realized with low-voltage CMOS devices to prevent the gate-oxide reliability issue

and designed in a 130-nm 1.2-V CMOS process to serve 1.2/2.5-V mixed-voltage interface applications. Moreover, the new proposed mixed-voltage crystal oscillator circuit I and II have been also redesigned and realized in a 90-nm 1-V CMOS process to serve 1/1.8-V mixed-voltage interface applications.

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TABLE CAPTIONS

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Chapter 1
Introduction

1.1 MOTIVATION

In CMOS technology, the device dimension of transistor has been scaled toward the nanometer region and the power supply voltage of chips in the nanoscale CMOS process technology has been also decreased to around 1V. Table 1.1 summarizes the key features of the semiconductor scaling trend, which are predicted by the Semiconductor Industry (SIA) [1]. Obviously, the shrunk device dimension makes the chip area smaller to save fabrication cost. The lower power supply voltage (VDD) results in lower power consumption. Therefore, chip design quickly migrates to the lower voltage level with the advancement of the nanoscale CMOS technology.

However, some peripheral components or other ICs in a microelectronic system are still operated at the higher voltage levels for compatible to some earlier interface specifications. In other words, the interface circuits between two chips have to deal with the I/O signals in different voltage levels [2]-[4], as shown in the Fig. 1.1. For example, 1.2/2.5-V interfacing is required for ICs realized in processes with a nominal power supply voltage of 1.2-V. As CMOS processes technology continues scaling down, it is essential to deal with the interfacial components with different power supplies.

To be compatible to the earlier defined standards or interface protocols of CMOS ICs in a microelectronics system, the chips fabricated in the advanced CMOS processes will face to the interface of input signals with voltage levels higher than their normal

supply voltage (VDD). Such mixed-voltage I/O interfaces must be designed to overcome several problems, such as gate-oxide reliability [5], hot-carrier degradation [6], and the undesired circuit leakage current paths [7], [8].

A complete I/O library includes the digital and analog I/O cells, power/ground cells and crystal oscillator cells. In receiving mode, the digital I/O cells receive external signals to internal circuit. And sometimes, we use crystal oscillator cells to receive an external clock signal instead of combining a crystal. So the two kinds of cells need to face the problems of mixed-voltage application.

1.2 RELIABILITY ISSUES

In modern CMOS technology, the CMOS processes are optimized to get the maximum performance of transistors used in digital circuit for certain lifetime. The nominal lifetime is typically 5-10 years with continuous operation under specified worst-case operating conditions. That means the circuits or transistors are supposed to be operated correctly without function error or leakage issue at least for 5-10 years at nominal power supply voltage level. However, overstress on the circuit shortens the lifetime, because of the higher electric filed strength in the device.

Reliability of transistors determines the lifetime duration of an electrical product. To meet the specified lifetime, the reliability of transistors in the circuit needs to be considered and concerned. There are three kinds of electric fields appearing to affect the reliability of a MOS transistor: the vertical and lateral electric fields in a transistor and electric fields across junctions. The three reliability-determining mechanisms corresponding to these fields are denoted as oxide breakdown [5], hot-carrier degradation [6], and junction breakdown [9], respectively.

The power supply voltage (VDD) for a CMOS technology is a trade-off of the speed performance, the power consumption, and the reliability issue. For speed performance, the higher supply voltage makes the device having the larger drain current to charge and to discharge the capacitive load. The gate-oxide breakdown over time and hot-carrier stress set the maximum supply voltage. And the oxide breakdown issue is the most important challenge for mixed-voltage interface applications.

1.2.1 Oxide Breakdown

The thinner gate oxide is required in the advanced processes due to the higher current density of the device. If the device dimensions are scaled down with the operation voltage kept the same, the device suffers from the short-channel effect. However, the larger electric field is across the gate oxide if the thickness of the gate oxide is scaled down with the operation voltage kept the same. The large electric field on the gate oxide may cause the gate-oxide breakdown.

The oxide voltage somewhere between the source and drain region is between the source-gate voltage (V_{sg}) and the drain-gate voltage (V_{dg}), if the MOS transistor is "on". It is because that voltage at each point in the channel is between the source and drain voltage. If the transistor is switched "off", an applied bulk-gate voltage (V_{bg}) is subdivided over a depletion layer in the silicon and over the gate oxide; most of the voltage drop will fall across the depletion layer. That means the V_{gb} of a MOS transistor could be higher than the nominal voltage of the process.

1.2.2 Hot-Carrier Degradation

Fig. 1.2 is a cross-section view of a typical enhancement-mode n-channel MOS

(NMOS) transistor where the source terminal is connected to ground. Heavily doped n-type source and drain regions are fabricated in a p-type substrate. A thin layer of silicon dioxide is grown over the substrate material and a conductive gate material covers the oxide between source and drain. In operation, the gate-source voltage (V_{gs}) modifies the conductance of the region under the gate, allowing the gate voltage to control the current following between source and drain. In the Fig. 1.2, the positive voltages, V_G and V_D, are applied to the gate and drain, respectively. An inversion layer is produced as the V_G is equal to or larger than the V_{th} of NMOS device. When the value of V_D is increased, the induced conducting channel narrows at the drain end. The induced electron charge at the drain end approaches zero as V_D approaches (V_G - V_{th}). That is, the channel is no longer connected to the drain when $V_D > V_G - V_{th}$, which is known as pinch-off. At this time, the electric field starts rise dramatically at the pinch-off point of the NMOS device. In the high electric field, carriers are accelerated to high velocities, reaching a maximum kinetic energy (hot) near the device drain. If the carrier energy is high enough, impact ionization can occur, creating electron-hole pair. The generated electrons called secondary electrons tend to be swept to the drain and generated holes called secondary holes swept into the substrate in the NMOS device.

Some of the electrons generated in the space charge region are attracted to the oxide due to the electric field induced by the positive gate voltage, V_G. These generated electrons have energies far greater than the thermal-equilibrium value and are called hot electrons (or hot carriers). If the electrons have energies on the order of 1.5 eV, they may be able to tunnel into the oxide. In some cases the generated holes and electrons can attain enough energy to surmount the Si–SiO_2 barrier and become trapped in the gate oxide. The charge trapping in interface states causes a shift in threshold voltage, additional surface scattering, and reduced mobility. The hot

electron charging effects are continuous processes, so the device degrades over a period of time. There are several techniques used to reduce maximum electric field in process and device structures, such as the lightly doped drain (LDD) structure [10]-[13]. However, the LDD structure increases the series drain resistance, which degrades the speed performance. Thus, the power supply voltage (VDD) maximizes the speed for a fixed reliability level.

1.2.3 Junction Breakdown

The third reliability-threatening mechanism is junction breakdown. For modern CMOS processes, this junction breakdown occurs at voltage of at least a number of times the nominal supply voltage and is therefore not a real concern for circuits that should operate at voltage level up to 2.5 times the nominal supply voltage. However, for reverse voltage somewhat higher than the nominal supply voltage, the junction goes into weak avalanche. With this effect, the reverse diode current, i.e., the leakage current, increases with increasing reverse bias levels.

1.3 ORGANIZATION

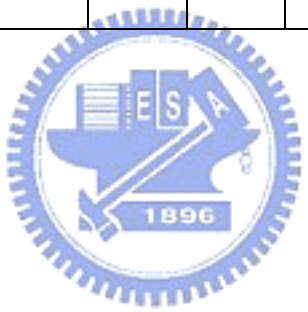
This thesis is organized into seven chapters and this introduction is the first one. Chapter 2 introduces design issues for mixed-voltage I/O interface and prior solutions. Chapter 3 describes the design of mixed-voltage I/O interface using floating n-well and gate-tracking circuit. Chapter 4 presents the conventional crystal oscillator circuit and a new idea of mixed-voltage crystal oscillator circuit I with an extra control signal. In chapter 5, a new mixed-voltage crystal oscillator circuit II without an extra control signal is proposed. In chapter 6, the experimental results are shown. Finally, chapter 7 summarizes this work and discusses the further works.

Table 1.1

Key Features of the Semiconductor Scaling Trend

(High-Performance Logic Technology) [1]

	2006	2007	2008	2009	2010	2011	2012
Gate Length, L (nm)	28	25	22	20	18	16	14
Oxide Thickness, t_{ox} (Å)	11	11	9	7.5	6.5	5	5
Power Supply Voltage, VDD (V)	1.1	1.1	1	1	1	1	0.9
Threshold Voltage, V_t (mV)	168	165	160	159	151	146	148
NMOS Drain Current (μA/μm)	1130	1200	1570	1810	2050	2490	2300



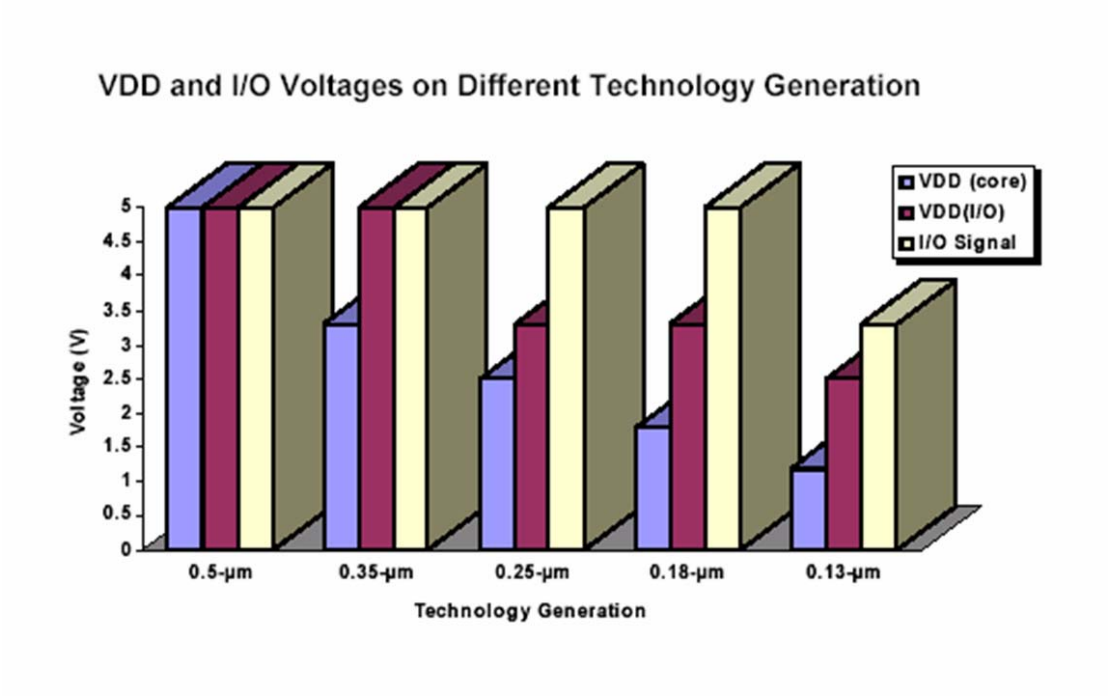


Fig. 1.1 Power supply voltage and I/O voltage on different technology generation.

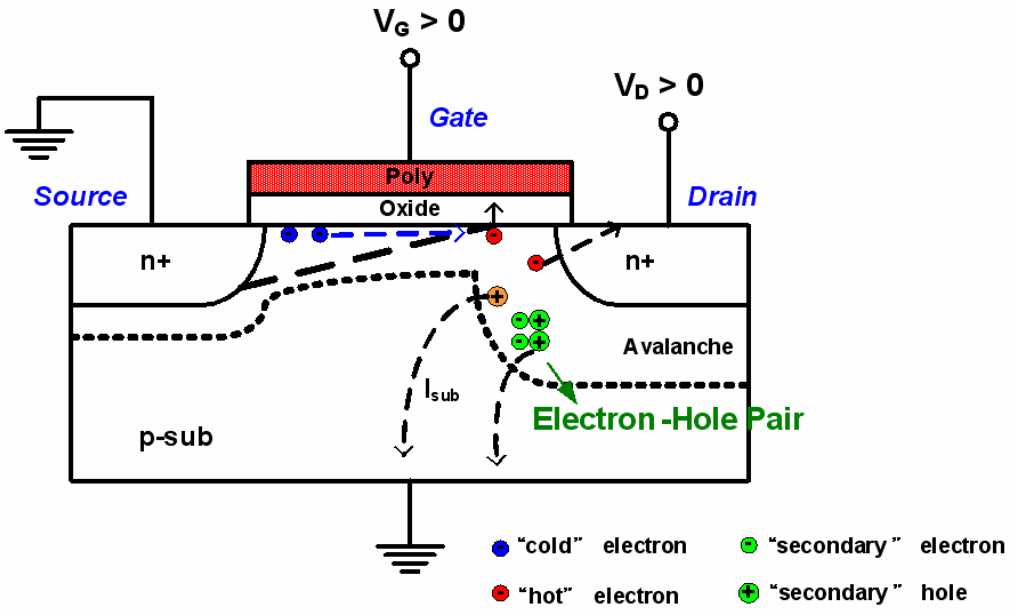


Fig. 1.2 The diagram of hot-carrier effect.

Chapter 2

Prior Designs of Mixed-Voltage I/O Buffer

In this chapter, the conventional I/O buffer and the issues in mixed-voltage I/O interface are introduced first, and then the prior solution concept is presented. Finally, a mixed-voltage I/O buffer with blocking NMOS and dynamic gate-controlled circuit reported in [14] is introduced before the proposed reliable mixed-voltage I/O buffers in the thesis. The mixed-voltage I/O buffer with blocking NMOS and dynamic gate-controlled circuit is designed to be tolerant of 2xVDD.

2.1 CONVENTIONAL I/O BUFFER

Fig. 2.1 shows the block diagram of a bidirectional input/output (I/O) buffer. As the output enable signal OE is high (VDD), the mixed-voltage I/O buffer is operating in transmit mode to transmit output signal from Dout to I/O PAD. On the other hand, the mixed-voltage I/O is operating in receive mode to receive input signals from I/O PAD to Din (internal circuit) if the OE is low (0V). In dual-oxide (thin-oxide and thick oxide) CMOS process, the core circuits usually use thin-oxide devices with low power supply voltage to reduce power consumption and silicon area while the interface circuits use thick-oxide to tolerant higher voltages and prevent reliability problems in traditional mixed-voltage I/O buffers.

2.2 ISSUES IN MIXED-VOLTAGE I/O INTERFACE

The conventional tri-state I/O buffer with 1.2-V gate-oxide devices in a 0.13-μm CMOS process is shown in Fig. 2.2, where the power supply voltage (VDD) is 1.2 V. However, the input signal at the I/O pad in the mixed-voltage I/O interface may rise up to 2.5 V in the tri-state input (receive) mode. In the receive mode, the gate voltages of the pull-up PMOS device and the pull-down NMOS device in the I/O buffer are traditionally controlled at 1.2 V and 0 V to turn off the pull-up PMOS device and the pull-down NMOS device by the pre-driver circuit, respectively. When the input signal at the I/O pad raises up to 2.5 V in the tri-state input mode, the parasitic drain-to-well pn-junction diode in the pull-up PMOS device will be forward biased. Therefore, an undesired leakage current path flows from the I/O pad to the power supply voltage (VDD) through the parasitic pn-junction diode. Besides, because the gate voltage of the pull-up PMOS device is 1.2 V and the input signal at I/O pad is 2.5 V, the pull-up PMOS device will be turned on in such tri-state input mode to conduct another undesired leakage current path from the I/O pad to the power supply voltage (VDD). Such undesired leakage currents cause not only more power consumption in the electronic system but also malfunction in the whole electronic system.

Moreover, because the gate-drain voltage (Vgd) of the pull-down NMOS device and the gate-source voltage (Vgs) of the input buffer in Fig. 2.2 with 2.5-V input signal are higher than their voltage levels in the normal operation, such high voltage across the thin gate oxide of the pull-down NMOS device and the input buffer results in the gate-oxide overstress reliability issue [5], [15]. In addition, the pull-down NMOS device and the input buffer with a 2.5-V input signal may suffer serious hot-carrier degradation if their drain-source voltages are too high [13].

2.3 PRIOR MIXED-VOLTAGE SOLUTIONS

The design concept is shown in Fig. 2.3. To solve the problem of gate-oxide reliability, a CMOS technology with a dual-oxide option [16], [17] is used. Because the thick gate-oxide can avoid the instances of gate-oxide breakdown, transistors that may suffer excessive gate-oxide stress should be replaced with thick oxide devices, and other transistors remain unchanged. To solve the problem of undesired leakage paths by the pull-up PMOS and the parasitic drain-to-well pn-junction diode, a gate-tracking circuit and a higher external voltage (VDDH) are used.

In Fig. 2.3, the mixed-voltage I/O buffer transmits GND-to-VDD (low voltage level) output signals and receives GND-to-VDDH (high voltage level) input signals. The pre-driver circuit generates control signals to output transistors MN and MP. In the mixed-voltage I/O buffer, the output transistors, gate-tracking circuits, and input circuit, INV, are thick-oxide devices to overcome reliability problems. The pre-driver circuit uses thin-oxide devices since the input data come from internal core circuit with low voltage level. In order to avoid leakage current path from the I/O PAD to the power supply (VDD) through the parasitic drain-to-well pn-junction diode in the pull-up PMOS device, MP, a higher external voltage (VDDH) is used to bias the N-well of the MP. In addition, a gate-tracking circuit is required to avoid the leakage current path induced by the incorrect conduction of the MP. Such mixed-voltage interface applications with dual-oxide devices can successfully overcome the gate-oxide reliability and hot-carrier degradation problem.

Although the mixed-voltage I/O buffer with dual-oxide devices and an external N-well bias voltage can successfully solve these problems, there are some drawbacks in these mixed-voltage I/O buffers. Fist of all, an extra pad and another power supply (VDDH) are required for the external bias voltage, which results in the increase of

silicon area and cost. Second, the driving capacity is decreased due to higher threshold voltage of thick-oxide device when the gates of output transistors are controlled by pre-driver circuit with thin-oxide devices. Thirdly, the threshold voltage of the pull-up PMOS device (MP) is also increased since the N-well of the pull-up PMOS device (MP) is connected to a higher voltage (VDDH), which results in body effect. Because the driving capacity is decreased, the larger device dimension is required for the pull-up PMOS device to achieve the desired driving specifications. As a result, the silicon area in such I/O buffers is increased. Moreover, the manufacturing time of thick-oxide device is even three times large than that of thin-oxide device. For these reasons, the mixed-voltage I/O buffer with dual-oxide devices and an external n-well bias is unsuitable for the low-cost commercial ICs. Considering these limitations, several mixed-voltage I/O buffers with only thin-oxide devices have been reported in [18]-[21], [24]-[26].

Fig. 2.4 re-draws the mixed-voltage I/O buffer with stacked pull-up PMOS devices reported in [24]. Signal OE is the output-enable control signal. In the transmit mode, transistor MN1 is turned on and transistor MP2 is turned off, so that this I/O buffer drives the I/O pad according to the output signal Dout. In the tri-state input mode, transistor MN1 is turned off and transistor MP2 is turned on by the control signal OE at logic zero. If the input signal at the I/O pad is 5 V, the gate voltage of transistor MP1 and the floating n-well are pulled up to 5 V through transistor MP2 and the parasitic drain-to-well pn-junction diode in transistor MP0 to prevent the undesired leakage current paths from I/O pad to power supply voltage (VDD), respectively. Although this I/O buffer is simple, transistors MN0, MN1, and MP2 have the gate-oxide reliability problem in the tri-state input mode when the input signal has a 5-V voltage level. Besides, because the stacked PMOS devices with the floating n-well is applied to this I/O buffer, the PMOS devices in stacked

configuration occupy more silicon area.

Fig. 2.5 re-draws another mixed-voltage I/O buffer with stacked pull-up PMOS devices and stacked pull-down NMOS devices [25]. This I/O buffer uses transistors MP2, MN3, and MN4 as the gate-tracking circuit and transistors MP0, MP3, and MP4 as the dynamic n-well bias circuit. In the tri-state input mode with the control signal OE at GND, transistor MN4 is turned off and transistor MP2 is turned on. If the input signal at the I/O pad is 5 V, the gate voltage of transistor MP3 is biased at 5 V through transistors MP0 and MP2 to avoid the undesired leakage current path due to the incorrect conduction of transistor MP3. The floating n-well is biased at ~5 V through the parasitic drain-to-well pn-junction diode of transistor MP0. In the transmit mode with the OE control signal at VDD, transistor MN4 is turned on so that transistor MP3 is turned on, and transistor MP2 is kept off. Hence, this I/O buffer drives the I/O pad according to the output signal Dout. When the signal at the I/O pad is 0 V, the floating n-well is biased at 2.5 V through transistor MP4. When the input signal at the I/O pad is 2.5 V, the floating n-well is biased at ~2.5 V through the parasitic source-to-well pn-junction diodes of transistors MP3 and MP4. However, transistor MP2 has the gate-oxide reliability problem when the input signal at the I/O pad is 5 V in the tri-state mode. Besides, because the I/O buffer uses two PMOS devices, MP0 and MP3, in stacked configuration to drive the I/O pad, the stacked devices occupy more silicon area.

The mixed-voltage I/O buffer with a depletion PMOS device is re-drawn in Fig. 2.6 [18]. The depletion PMOS device MP2 in the I/O buffer is used as the gate-tracking circuit. In the tri-state mode, if the input signal at I/O pad is 5 V, the gate voltage of transistor MP0 is biased at 5 V through the depletion PMOS device MP2 to avoid the undesired leakage current path through the transistor MP0. This I/O buffer uses an extra pad that is connected to 5-V power supply (VDDH) to avoid the

undesired leakage current path through the parasitic drain-to-well pn-junction diode. However, using the depletion device increases mask layer and process modification. Thus, the fabrication cost of such I/O buffer design will be increased. In addition, using the extra n-well bias (VDDH) not only degrades the driving capacity of output device MP0 due to the body effect, but also increases the system cost.

Fig. 2.7 re-draws the mixed-voltage I/O buffer realized with only thin-oxide devices reported in [26]. In Fig. 2.7, the gate-tracking circuit and the dynamic n-well bias circuit are formed by transistors MP1, MP2, MP3, MP4, MN2, MN3, MN4, and MN5. In the transmit mode with signal OE at logic "1", transistor MN4 is turned on to keep transistors MP3 and MP4 on. Thus, this I/O buffer drives the I/O pad according to signal Dout. Besides, because transistor MP3 is turned on, the floating n-well is biased at 2.5 V by transistor MP3 in the transmit mode. In the tri-state input mode with signal OE at logic "0", transistor MN4 is kept off. If the input signal at the I/O pad is 5 V, the gate voltages of transistors MP0 and MP4 are biased at 5 V through transistor MP1 and MP2 to avoid the undesired leakage paths through the transistors MP0 and MP4. Besides, the floating n-well is also biased at ~5 V to avoid the undesired leakage path through the parasitic drain-to-well pn-junction diode of transistor MP0 when the voltage at the I/O pad is 5 V in tri-state input mode. When the input signal at the I/O pad is 0 V in the tri-state input mode, transistor MN3 is turned on to keep transistor MP3 on. So, the floating n-well is biased at 2.5 V.

Another mixed-voltage I/O buffer realized with only thin-oxide devices is re-drawn in Fig. 2.8 [19]. The gate-tracking circuit in Fig. 2.8 is composed of transistors MN3, MN4, MP2, MP3, and MP4. The dynamic n-well bias circuit in Fig. 2.8 is formed by transistors MN5, MP5, MP6, and MP7. Besides, the body terminals of all PMOS transistors in the gate-tracking circuit and the dynamic n-well bias circuit are connected to the floating n-well. Such I/O circuit shown in Fig. 2.8 can overcome

the gate-oxide reliability problem and avoid the undesired leakage paths. However, there are too many devices used to realize the desired functions of the gate-tracking circuit and the dynamic n-well bias circuit. More devices used in the mixed-voltage I/O cause more complex metal routing connection in the I/O cells.

2.4 A MIXED-VOLTAGE I/O BUFFER WITH BLOCKING NMOS AND DYNAMIC GATE-CONTROLLED CIRCUIT

The block diagram of mixed-voltage I/O buffer with a blocking NMOS and a dynamic gate-controlled circuit proposed in [14] is depicted in Fig. 2.9. Here, VDDH has a high voltage of 2xVDD, which can be generated by the on-chip charge pump circuit [22] or other high-voltage generators. Transistor MN1 is used to protect the conventional I/O buffer from the high-voltage overstress. The operations of the dynamic gate-controlled circuit in the proposed I/O buffer with blocking NMOS are listed in Table 2.1. When the I/O buffer is in the receive mode, the gate terminal (node 2) of MN1 is biased at VDD by the dynamic gate-controlled circuit, whereas the pull-up device MP0 and pull-down device MN0 are both turned off by the pre-driver. At this moment, if an input signal of logic '0' (0V) is received from the I/O PAD, node 1 is discharged to 0 V through the transistor MN1, and this input signal can be successfully transferred to the node Din. When a logic '1' (VDDH) signal is received at the I/O pad, the gate terminal of transistor MN1 is still biased at VDD, so the voltage on node 1 is pulled to "VDD−V_{th}". A feedback device MP1 is added to restore the voltage level on node 1 to VDD, which avoids the undesired static dc current through the inverter INV1. In this design, MN1, MP1, and inverter INV1 can convert the VDDH input signal to VDD signal successfully. Therefore, MN1 can protect the I/O buffer without suffering high-voltage overstress in both steady states of transmit

mode and receive mode.

Fig. 2.10 depicts the dynamic gate-controlled circuit of the I/O buffer in Fig 2.9, where MP2 and MP3 are designed with the cross-coupled structure. If the gate voltage of MP2 (or MP3) is pulled down, this transistor is turned on and pulls up the gate voltage of the other transistor to VDDH (2xVDD) to turn it off. For example, if the voltage on node 5 is lower than "VDDH−$|V_{tp}|$" and the voltage on node 6 is VDDH, MN2 is turned on to keep the node 5 at VDD. Capacitors C1 and C2 are used to couple the signals from nodes 3 and 4 to nodes 5 and 6, respectively. The voltages across these capacitors are always VDD, because the voltage levels on the top plate and bottom plate of capacitors C1 and C2 are either VDD and 0V or 2xVDD and VDD. With these capacitors, when node 3 converts the voltage level from VDD to 0V, the voltage on node 5 is pulled down to VDD and then the voltage level on node 6 is pulled up to 2xVDD by transistor MP3. On the contrary, when the voltage level on node 4 is converted from VDD to 0V, the voltage on node 6 is pulled down to VDD, and that on node 5 is pulled up to 2xVDD by MP2. Initially, the voltages on nodes 3, 4, 5, and 6 could be unknown. If the voltages on nodes 5 and 6 are 2xVDD and VDD, and the voltages on nodes 3 and 4 are 0V and VDD, the voltages across capacitors C1 and C2 are 2xVDD and 0V, respectively, instead of both VDD. In order to overcome this problem, diode strings DS1 and DS2 are added. The turn-on voltages of the diode strings are designed to a little higher than VDD by using multiple diodes in stacked configuration. In order to prevent the leakage current path to the grounded p-type substrate, the diode-connected MOSFET or poly diode [23] is suggested. With these diode strings, if the voltage on node 3 is at 0V and that on node 4 is at VDD initially, the voltage on node 5 is clamped at the turn-on voltage (~VDD) of DS1. Therefore, MP3 is turned on to pull up the voltage on node 6 to 2xVDD. Thus, the voltages across capacitors C1 and C2 are both VDD.

In this mixed-voltage I/O buffer, the bulk of the blocking NMOS MN1 can be coupled to 0V (GND) without any gate-oxide reliability problem, even if the gate voltage of MN1 may be as high as VDDH (2xVDD). The reason is that this blocking NMOS MN1 is always turned on and the voltage across the gate oxide of MN1 is from the gate to the conducting channel, but not from the gate to its bulk. The gate oxides of all NMOS devices in the dynamic gate-controlled circuit are also safe because these NMOS devices are turned on when their gates are pulled up to VDDH.

Table 2.1

Operations of the dynamic gate-controlled circuit in the mixed-voltage I/O buffer with blocking NMOS [14].

Mode	Transmitted Signals (Dout)	Gate Voltage of MP0 (PU)	Gate Voltage of MN1 (Node 2)
Receive Mode	X	VDD	VDD
Transmit Mode	Low (0 V)	VDD	VDD
Transmit Mode	High (VDD)	0 V	VDDH (2xVDD)

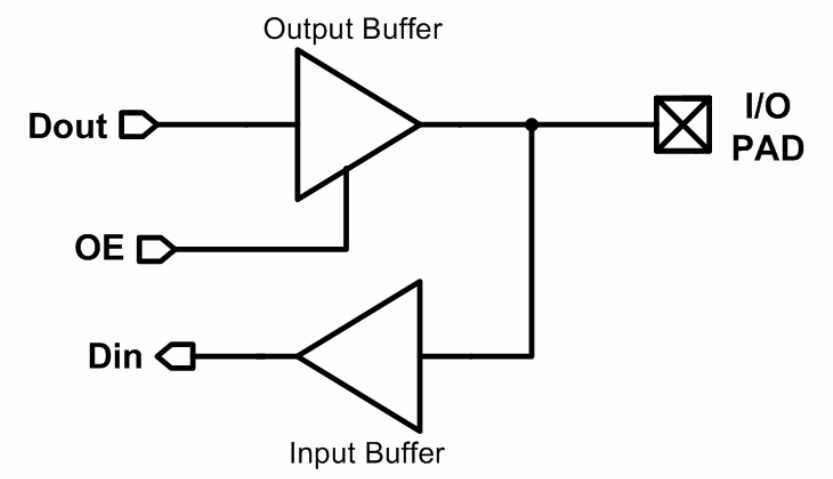


Fig. 2.1 Block diagram of bidirectional I/O buffer.

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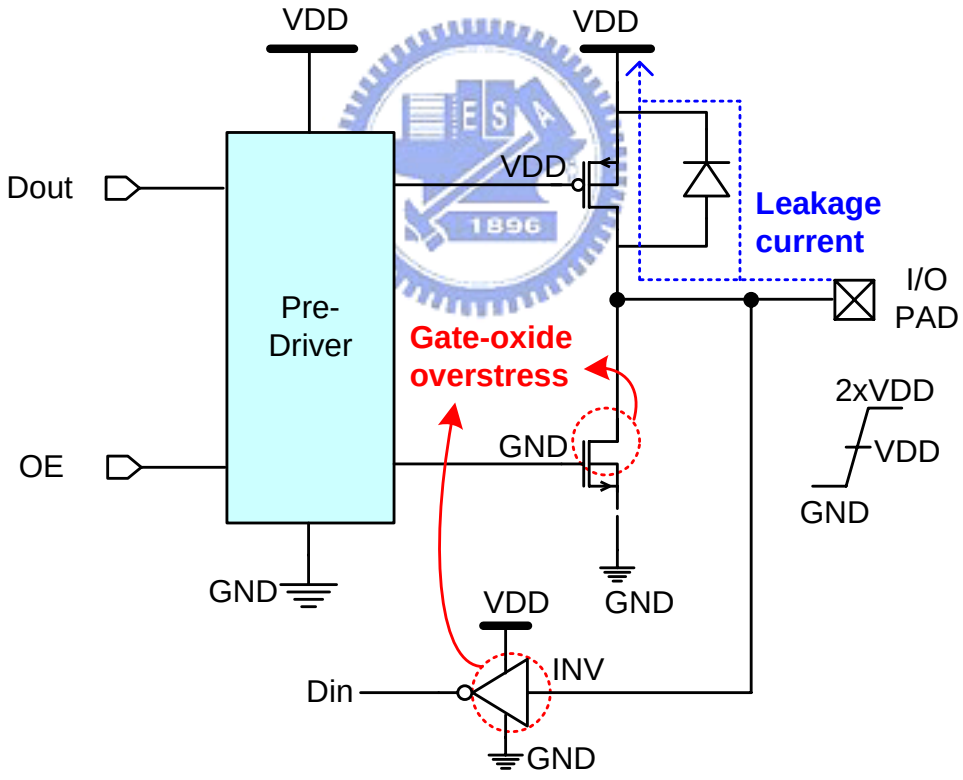


Fig. 2.2 Conventional tri-state I/O buffer will suffer the circuit leakage and gate-oxide reliability issues in the mixed-voltage I/O interface.

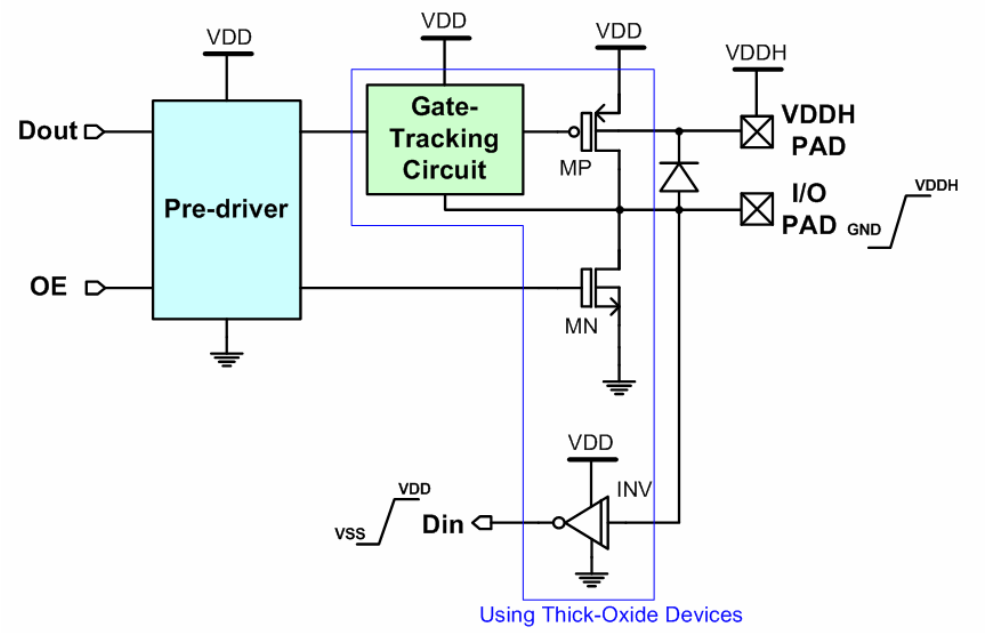


Fig. 2.3 Block diagram of a mixed-voltage I/O buffer with dual-oxide devices and an external n-well bias voltage.

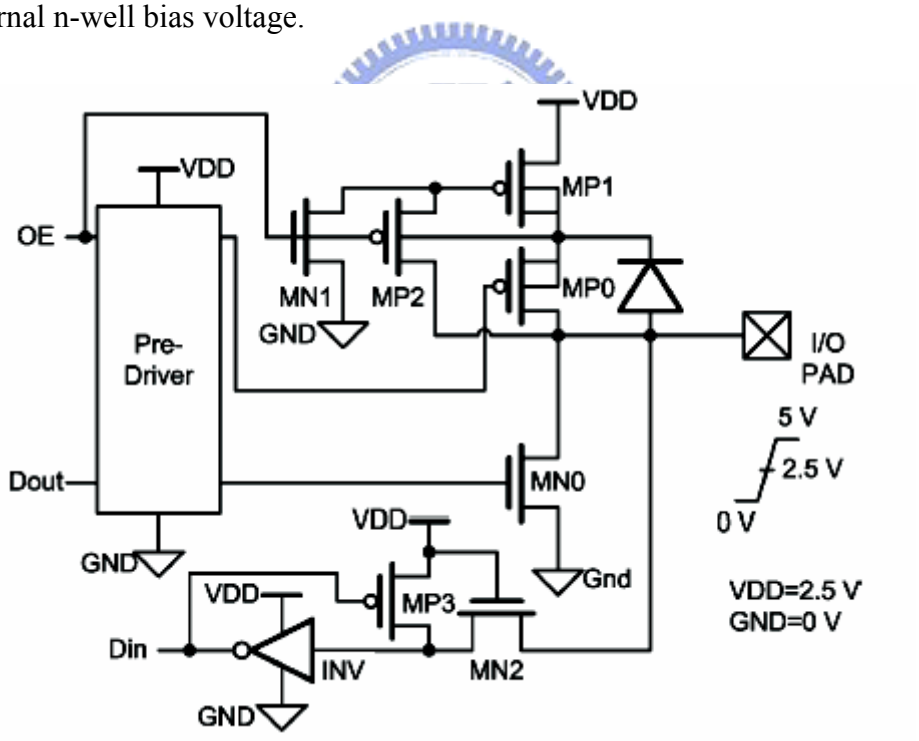


Fig. 2.4. Mixed-voltage I/O buffer with stacked pull-up PMOS devices [24].

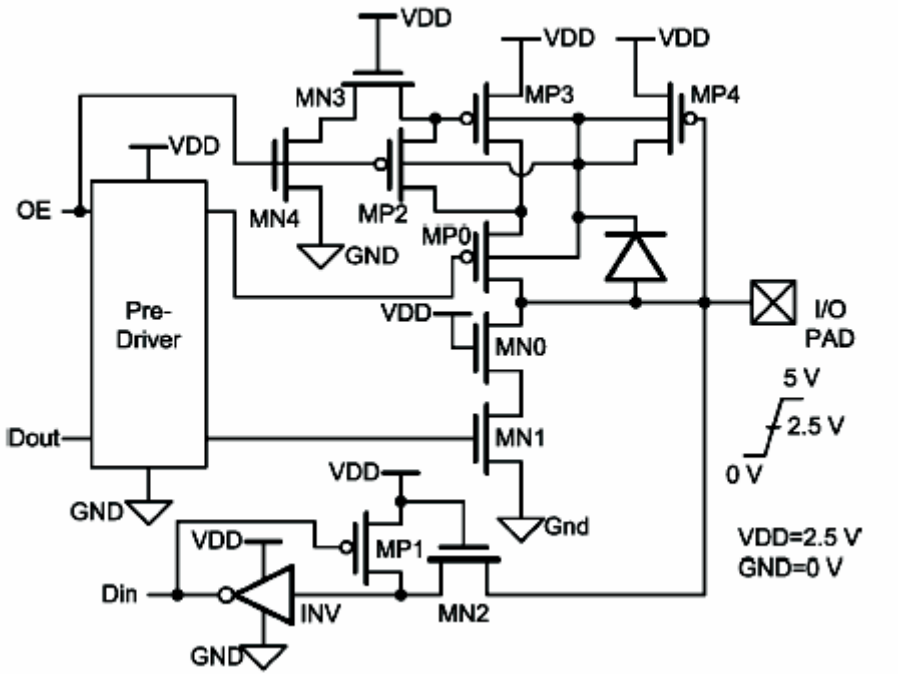


Fig. 2.5. Mixed-voltage I/O buffer with stacked pull-up PMOS devices and stacked pull-down NMOS devices [25].

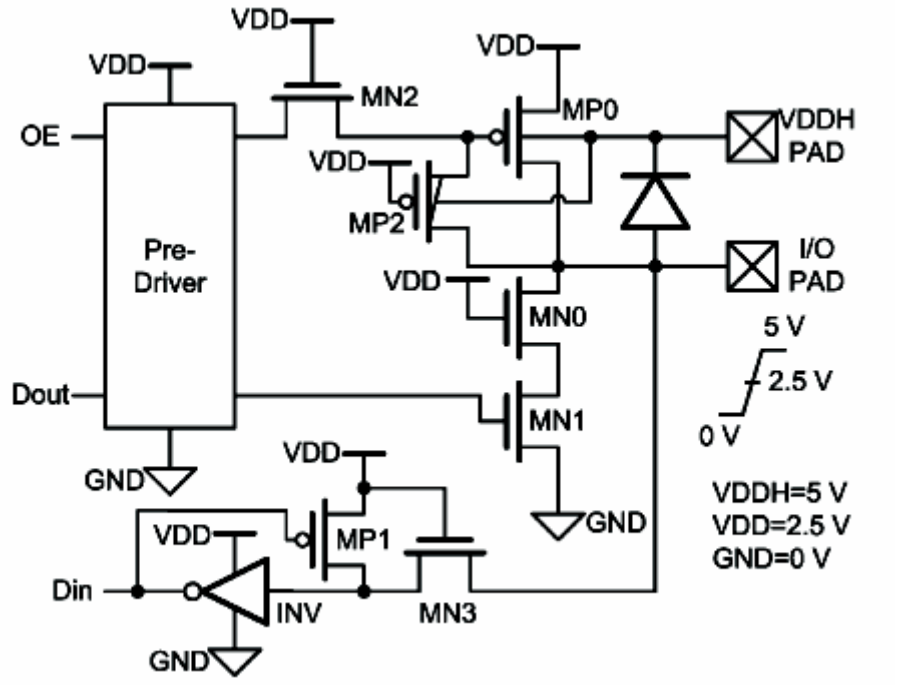


Fig. 2.6. Mixed-voltage I/O buffer with a depletion PMOS device MP2 [18].

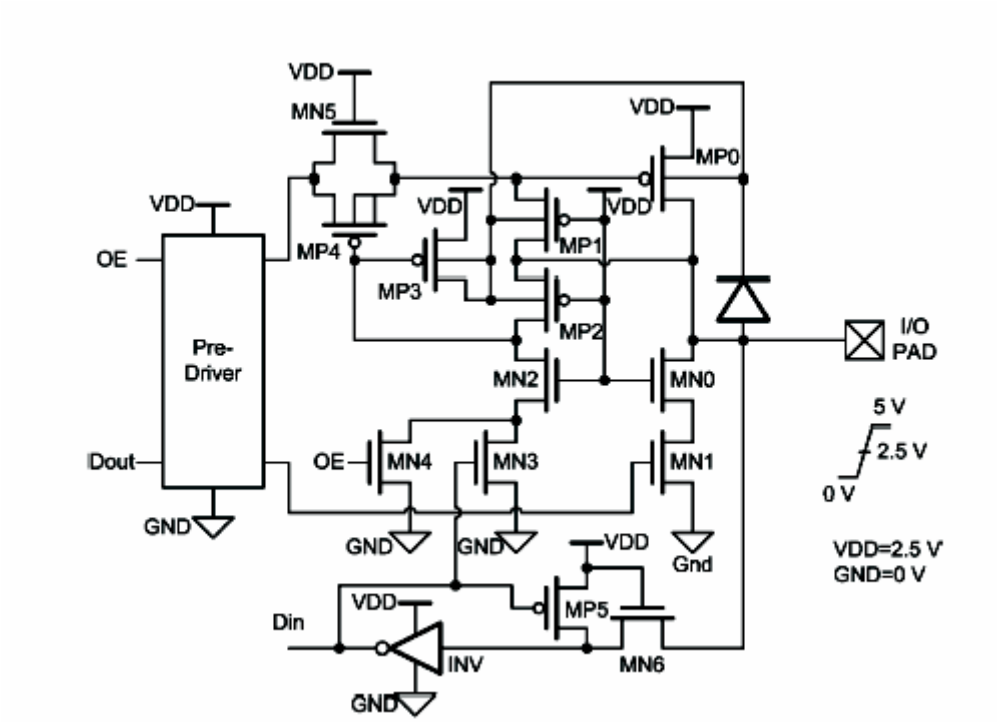


Fig. 2.7. Mixed-voltage I/O buffer realized with only thin-oxide devices [26].

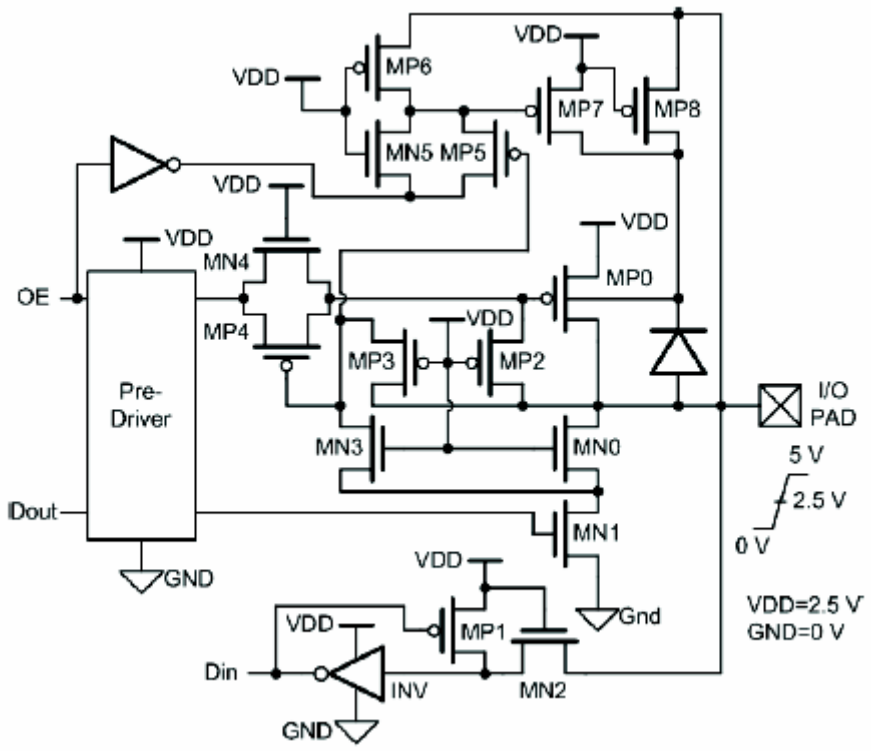


Fig. 2.8. Mixed-voltage I/O buffer realized with only thin-oxide devices [19].

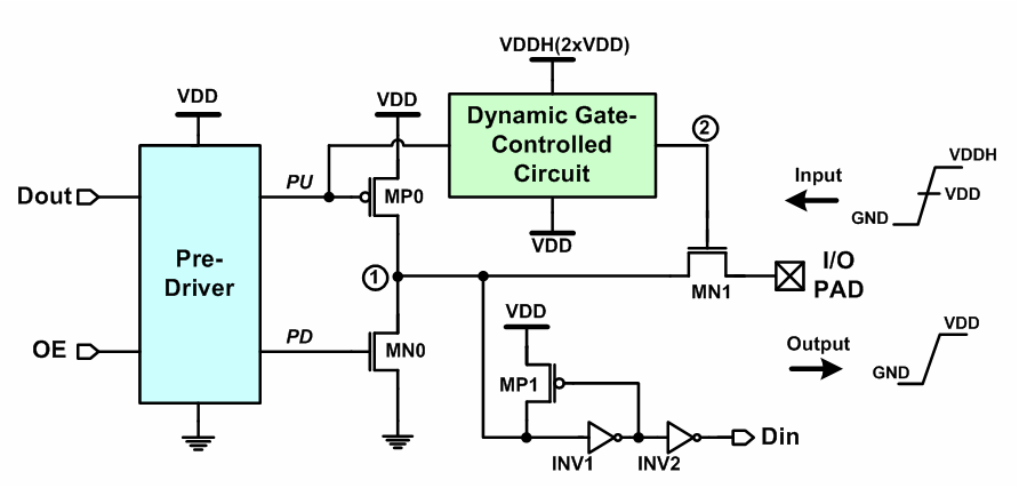


Fig. 2.9 The mixed-voltage I/O buffer with a blocking NMOS and a dynamic gate-controlled circuit.

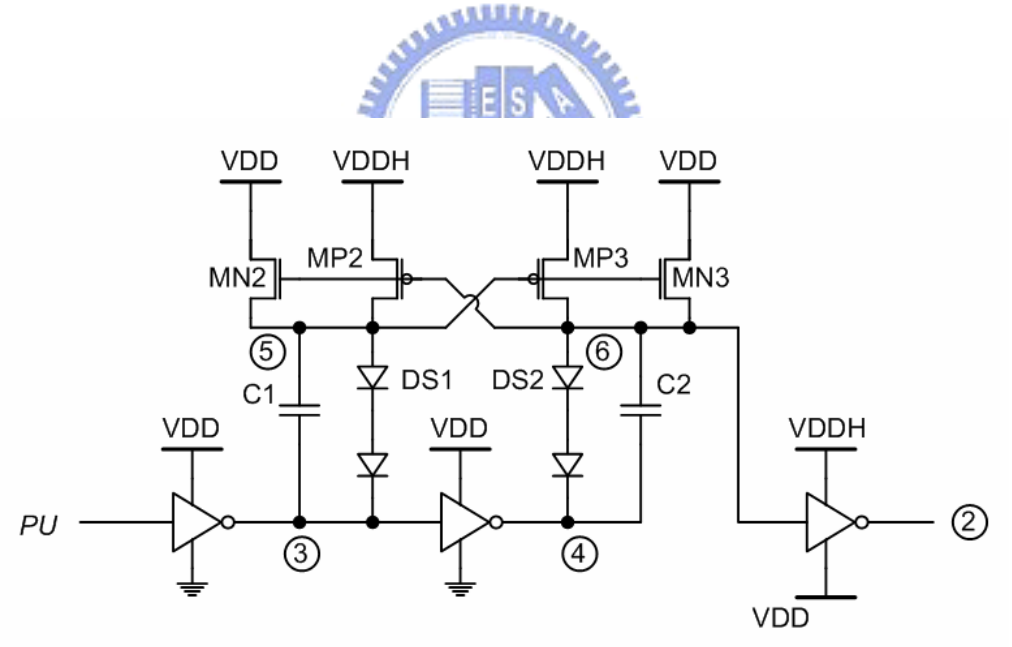


Fig. 2.10 Circuit implementation of the dynamic gate-controlled circuit in the Fig. 2.9.

Chapter 3

1.2/2.5-V Mixed-Voltage I/O Buffer with Gate-Tracking Circuit and Dynamic N-well Bias Circuit by Only Using Thin Gate-Oxide Devices

3.1 INTRODUCTION

There are a lot of drawbacks in the previous mixed-voltage I/O interface design with a dual-oxide option, like as extra voltage source and process cost. The prior designs of I/O interface are complicated and had been described in the chapter 2 already. In this chapter, a better mixed-voltage I/O interface is presented and proposed without extra process and voltage source in [21]. The presented design of mixed-voltage I/O interface buffer is simpler than the prior designs.

3.2 DESIGN CONCEPT

Fig. 3.1 shows the presented mixed-voltage I/O buffer realized with a dynamic n-well bias circuit, and a gate-tracking circuit by only using thin gate-oxide devices [18]-[19], [24]-[26]. The stacked NMOS devices, MN0 and MN1, are used to avoid the high-voltage overstress on their gate oxide. The gate-tracking circuit shown in Fig. 3.1 is used to prevent the leakage current path which is resulted from the incorrect conduction of the pull-up PMOS device when the input signal is higher than VDD. As the mixed-voltage I/O buffer is operating in the transmit mode, the gate-tracking circuit must transmit the signal from the pre-driver circuit to the gate terminal of the

pull-up PMOS device, MP0, exactly. In the receive mode (tri-state input mode) with an input signal of 2xVDD, the gate-tracking circuit will charge the gate terminal of the MP0 to 2xVDD to completely turn off the MP0, and to avoid the leakage current from the I/O pad to the power supply (VDD). On the contrary, the gate-tracking circuit will keep the gate terminal of the MP0 at VDD to completely turn off the MP0, and to prevent the overstress on the gate oxide of the MP0 when the 0-V input signal is received from I/O PAD. Moreover, the dynamic n-well bias circuit shown in Fig. 3.1 is designed to prevent the leakage current path due to the parasitic drain-to-well pn-junction diode in the pull-up PMOS device MP0. In the transmit mode, the dynamic n-well bias circuit must keep the floating n-well bias at VDD so that the threshold voltage of the pull-up PMOS device isn't increased due to the body effect. In the receive mode with an input signal of 2xVDD, the dynamic n-well bias circuit will charge the floating n-well to 2xVDD to prevent the leakage current from the I/O pad to the power supply (VDD) through the parasitic pn-junction diode. On the other hand, the dynamic n-well bias circuit will bias the floating n-well at VDD when the input signal at the I/O pad is 0V.

As shown in Fig. 3.1, the extra transistors, MN2 and MP1, which are compared to Fig. 2.3, are added in the input circuit. The transistor MN2 is used to limit the voltage level of input signal reaching to the gate oxide of inverter INV1. The transistor MP1 is used to prevent unnecessary leakage current in the inverter INV1. Because the gate terminal of transistor MN2 is connected to the power supply voltage (VDD), the input terminal of inverter INV1 will rise up to "VDD-V_{th}" when the input signal at the I/O pad is 2xVDD in the receive mode. The transistor MP1 will pull the input node of inverter INV1 up to VDD when the output node of inverter INV1 is pulled down to 0V. Therefore, the gate-oxide reliability problem of the input buffer can be solved.

3.3 CIRCUIT DESCRIPTION

Fig. 3.2 shows the mixed-voltage I/O buffer with the dynamic n-well bias circuit and gate-tracking circuit proposed in [21]. When the output control signal OE is at VDD (logic "1"), the mixed-voltage I/O buffer is operated in the transmit mode. The signal at the I/O pad follows the signal Dout, which is controlled by the internal circuits of IC. The pull-down signal, *PD*, produced by pre-driver is directly connected to the gate terminal of the pull-down NMOS device, MN1. The pull-up signal, *PU*, is connected to the gate terminal of the pull-up PMOS device, MP0, through the gate-tracking circuit which is composed of NMOS transistors MN2-MN4 and PMOS transistors MP2, MP3 and MP5. The transistors MN2 and MP2 comprise a transmission gate. The transistor MN3 in Fig. 3.2 is used to protect the transistor MN4 from gate-oxide reliability problem. The dynamic n-well bias circuit is composed of transistors MP4 and MP6. If the mixed-voltage I/O buffer is operating in transmit mode (OE = VDD), the gate terminal of MP4 will be biased at 0V to keep the floating n-well at VDD by turning on the transistor MP4. At this time, the *PU* signal is fully transmitted to the gate terminal of the pull-up PMOS device MP0 through the transmission gate, MN2 and MP2. As 0-V output signal is transmitted, the *PD* signal is set to VDD to turn on the transistor MN4. In the meanwhile, the *PU* signal is set to VDD to turn off the pull-up device MP0. Consequently, the voltage at the I/O pad and the gate voltage of transistor MP5 are discharged to 0 V through transistors MN0 and MN1. Transistor MP5 is turned on until the gate terminal of transistor MP2 is discharged to $|V_{tp}|$ through transistors MN3 and MN4, where V_{tp} is the threshold voltage of PMOS device.

When the proposed I/O buffer is operated in the receive mode, the *PU* and *PD* signals are kept at VDD and 0V, respectively, to turn off transistors MP0 and MN1.

Signal Din follows the signal at the I/O pad in the receive mode. In order to prevent the undesired leakage current from the I/O pad to the power supply (VDD) through the pull-up PMOS device MP0, transistor MP3 is used to track the signal at the I/O pad and to control the gate voltage of transistor MP0. When the voltage level at the I/O pad exceeds "VDD+$|V_{tp}|$," such as 2xVDD, transistor MP3 is turned on to charge the gate terminal of transistor MP0 up to 2xVDD. Thus, transistor MP0 is completely turned off to prevent the leakage current through its channel. If a 0-V input signal is received at I/O PAD, the floating n-well is biased at VDD through transistor MP4. As the mixed-voltage I/O is operating in the receive mode with an input signal of 2xVDD, another PMOS device MP6 is turned on to bias the floating n-well at 2xVDD. Also, transistor MP4 is turned off to prevent the leakage path by pulling up the gate terminal of MP4 to 2xVDD through transistor MP5. As a result, there is no leakage current path from the I/O pad to the power supply (VDD). Whenever the proposed mixed-voltage I/O buffer is in the transmit mode or the receive mode, the floating n-well is biased at VDD or 2xVDD directly. Thus, the subthreshold leakage problems do not occur in this proposed I/O buffer. Besides, transistor MP5 is also turned on to keep transistor MP2 off in order to prevent another leakage path from the gate terminal of transistor MP0 to the UP signal when the signal at the I/O pad is 2xVDD.

Transistors MN0 and MP1 with inverters INV1 and INV2 are used to transmit the input signal from the I/O pad to the internal node Din in the receive mode. Transistor MN0 is used to limit the voltage level of input signal reaching to the gate oxide of inverter INV1. The signal at the I/O pad can be successfully transmitted to the internal input node Din. This I/O buffer can be correctly operated with neither gate-oxide reliability problem nor any circuit leakage issue in the receive mode.

3.4 SIMULATION RESULTS

In this work, a completed I/O cell is constructed. The function block diagram is shown in Fig. 3.3 and the circuit schematic is shown in Fig. 3.4. This mixed-voltage I/O cell circuit includes input stage and output stage, pull-up resistor for floating I/O PAD, pre-driver circuit, gate-tracking circuit, floating n-well circuit and ESD protect device. The SPICE simulation waveforms of the mixed-voltage I/O cell with a 20-pF load at I/O pad are shown in Fig. 3.5 in UMC 0.13-μm 1.2-V CMOS process. Fig. 3.5(a) shows the behavior in transmit mode. The signal Dout with 0.5-ns rising and falling time is correctly transmitted to the I/O pad and the voltage level of floating N-well normally keeps at VDD. Fig. 3.5(b) shows that in receive mode (tristate mode). The signal Din correctly follows the signal with 0.5-ns rising and falling time at I/O pad and the voltage level of floating N-well is successfully pulled up to 2xVDD when the signal is 2xVDD at I/O pad. Fig. 3.5(c) shows the simulation waveform of the operation of the pull-up resistor, where the voltage level can be successfully pull up to weakly high when the pull-up resistor is turned on.

3.5 EXPERIMENTAL RESULTS

Fig. 3.6 is the die photo of the 1.2/2.5-V mixed-voltage I/O buffer with gate-tracking circuit and dynamic N-well bias circuit by only using thin gate-oxide devices. Fig. 3.7 shows the layout view of the 1.2/2.5-V mixed-voltage I/O buffer implemented in the UMC 130-nm 1.2-V CMOS process. The cell size of I/O cell is only 187μm×60μm (including the bond pad), which is the same as that of analog or power/ground cell in a standard I/O cell library.

To test the function of proposed I/O cell in transmit mode and receiving mode,

two proposed I/O cells are used and connected as the measurement setup in Fig. 3.8 for receiving 0/1.2-V signal of 1-MHz and 5-MHz. Here, the I/O cell_1 is used as the input cell to receive the external input signal from the pulse generator (81110A). The I/O cell_2 is used as the output cell to transmit the signal to the oscilloscope. As the measurement results shown in Fig. 3.9, the proposed I/O cell can successfully receive the 0/1.2-V input signal at the pad of the I/O Cell_1 and transmit to the pad of the I/O Cell_2.

To test the function of proposed I/O cell for receiving 0/2.5-V signal of 1-MHz and 5-MHz, two proposed I/O cells are used and connected as the measurement setup in Fig. 3.10. Here, the I/O cell_1 is used as the input cell to receive the external input signal from the pulse generator (81110A). The I/O cell_2 is used as the output cell to transmit the signal to the oscilloscope. As the measurement results shown in Fig. 3.11, the proposed I/O cell can successfully receive the 0/2.5-V input signal at the pad of the I/O Cell_1 and transmit to the pad of the I/O Cell_2 with the signal shifted in 0/1.2-V.

In Fig 3.12, the pull-up function is successfully verified with the voltage level at the pad pulled up to 0.92-V. From the measurement results, the 1.2/2.5-V mixed-voltage I/O buffer with gate-tracking circuit and dynamic N-well bias circuit by only using thin gate-oxide devices can be successfully operated in such a 1.2V/2.5V mixed-voltage I/O environment. The maximum operation frequency of the proposed I/O buffer depends on the output load and the device size of output circuit.

3.6 COMPARISONS

Table 3.1 lists the features among these mixed-voltage I/O buffers. Since the new mixed-voltage I/O buffers and the prior I/O buffers reported in [19] and [24]-[26]

use the dynamic n-well biased technique, no extra pad and power supply is required. The new mixed-voltage I/O buffers in this work occupy smaller silicon area than the I/O buffers reported in [18]-[19], [24]-[25]. Although the circuit structures of the mixed-voltage I/O buffers reported in [24], [25] are simpler, these two I/O buffers have the gate-oxide reliability problem. In Fig. 2.4, transistors MN0, MN1, and MP2 have the gate-oxide reliability problem in the tri-state input mode when the input signal has a 5-V voltage level. In Fig. 2.5, transistor MP2 has the gate-oxide reliability problem when the input signal at the I/O pad is 5 V in the tri-state mode. In fig. 2.6, since the depletion PMOS is used to improve the gate-tracking circuit of the mixed-voltage I/O buffer reported in [18], extra mask and process modification are required to realize the depletion device. In fig. 2.4, fig. 2.5 and fig. 2.7 The prior mixed-voltage I/O buffers reported in [24]-[26] may have the subthreshold leakage problem, but the prior mixed-voltage I/O buffer reported in [19] and the new mixed-voltage I/O buffer don't have. However, the new mixed-voltage I/O buffers occupy smaller silicon area than the prior I/O buffers [19], [24]-[26]. Thus, if the subthreshold leakage issue in the given CMOS process is serious, such as the 90-nm, 65-nm or more advanced CMOS process, the new mixed-voltage I/O buffer is recommended.

3.7 CONCLUSION

A new mixed-voltage I/O buffer with the stacked NMOS technique, dynamic n-well technique, and gate-tracking circuit have been successfully designed and implemented in UMC 0.13-μm 1.2-V CMOS process, which can be operated in the 1.2/2.5-V signal environment without the gate-oxide reliability problem. The new mixed-voltage I/O buffer can be applied for high-speed applications without the

gate-oxide reliability problem and the circuit leakage issue. The new mixed-voltage I/O buffer realized with 1xVDD devices can be easily applied in 1xVDD/2xVDD mixed-voltage interface.

Table 3.1

Comparison on features among the mixed-voltage I/O buffer designs.

Mixed-voltage I/O designs	N-well bias	Extra pad	Gate-oxide reliability issue	Special device	Subthreshold leakage issue
Fig. 2.4 [24]	Dynamic bias	No	Yes	No	Yes
Fig. 2.5 [25]	Dynamic bias	No	Yes	No	Yes
Fig. 2.6 [18]	Fixed bias	Yes	No	Yes (Depletion PMOS)	No
Fig. 2.7 [26]	Dynamic bias	No	No	No	Yes
Fig. 2.8 [19]	Dynamic bias	No	No	No	No
Fig. 3.2 (This work)	Dynamic bias	No	No	No	No

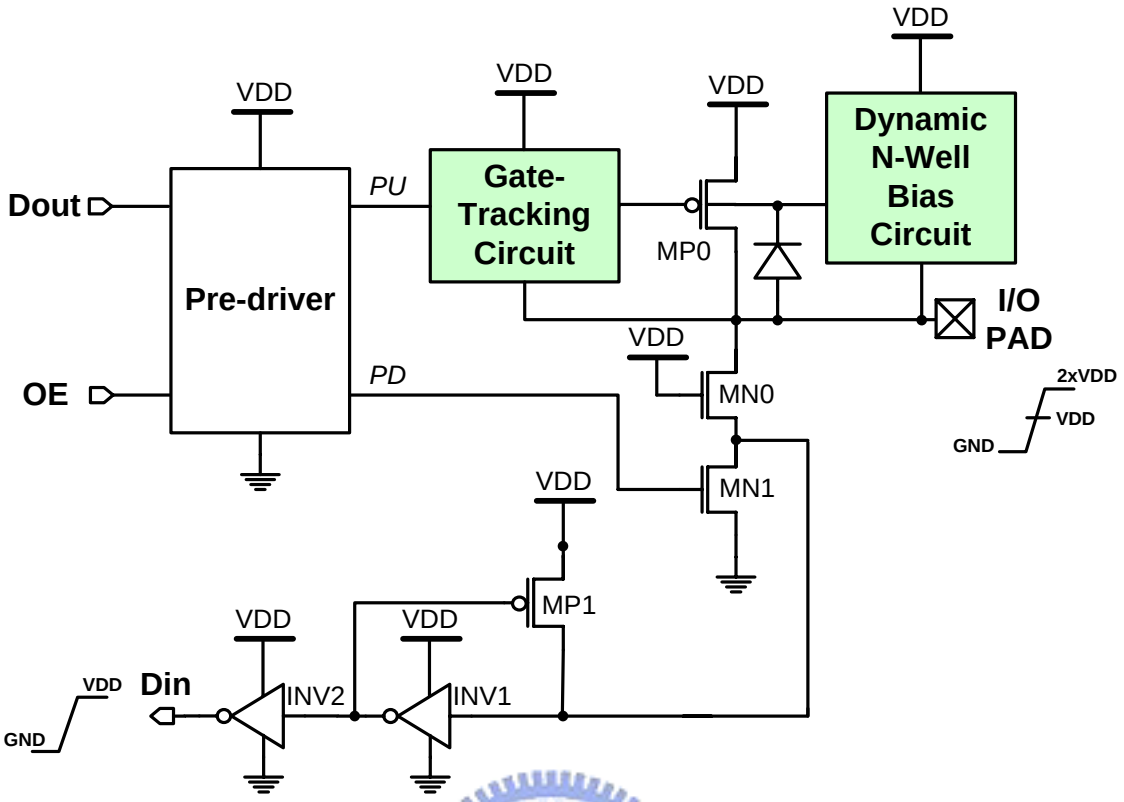


Fig. 3.1 Basic design concept for mixed-voltage I/O buffer realized with only thin-oxide devices.

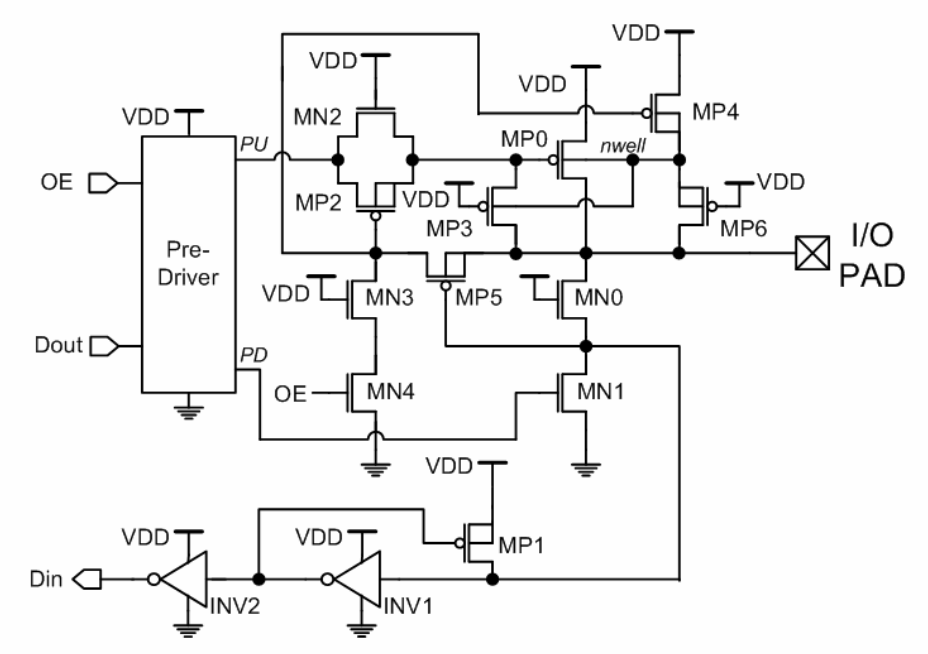


Fig. 3.2 The mixed-voltage I/O buffer with gate-tracking circuit and dynamic n-well bias circuit proposed in [21].

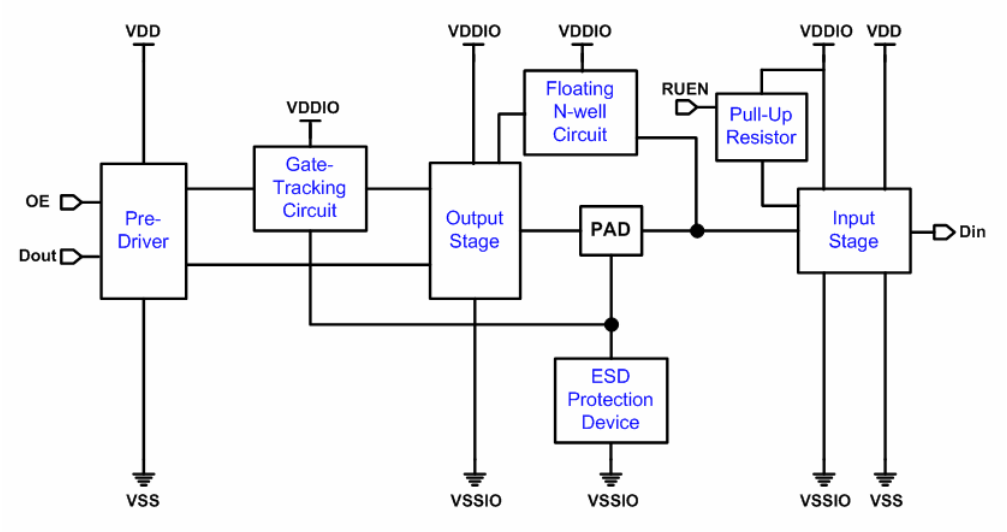


Fig. 3.3 The function block of completed mixed-voltage I/O cell with gate-tracking circuit and dynamic n-well bias circuit.

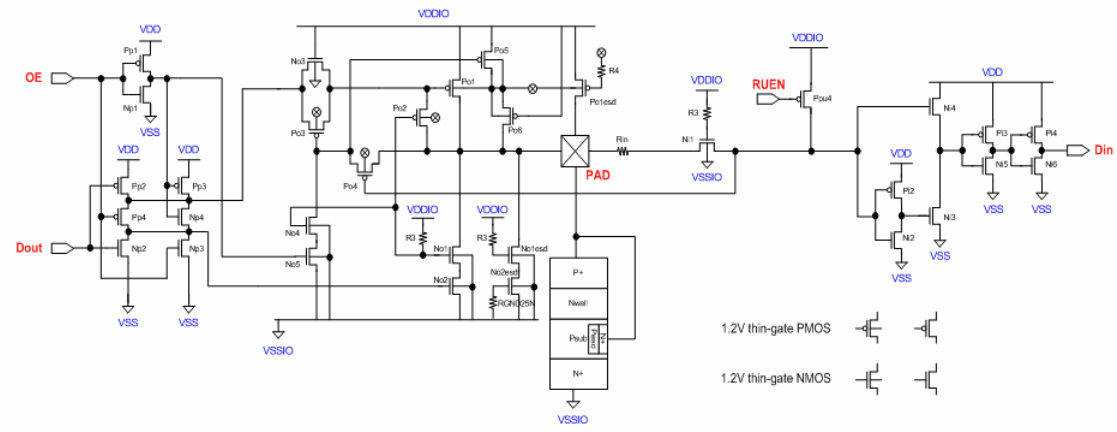
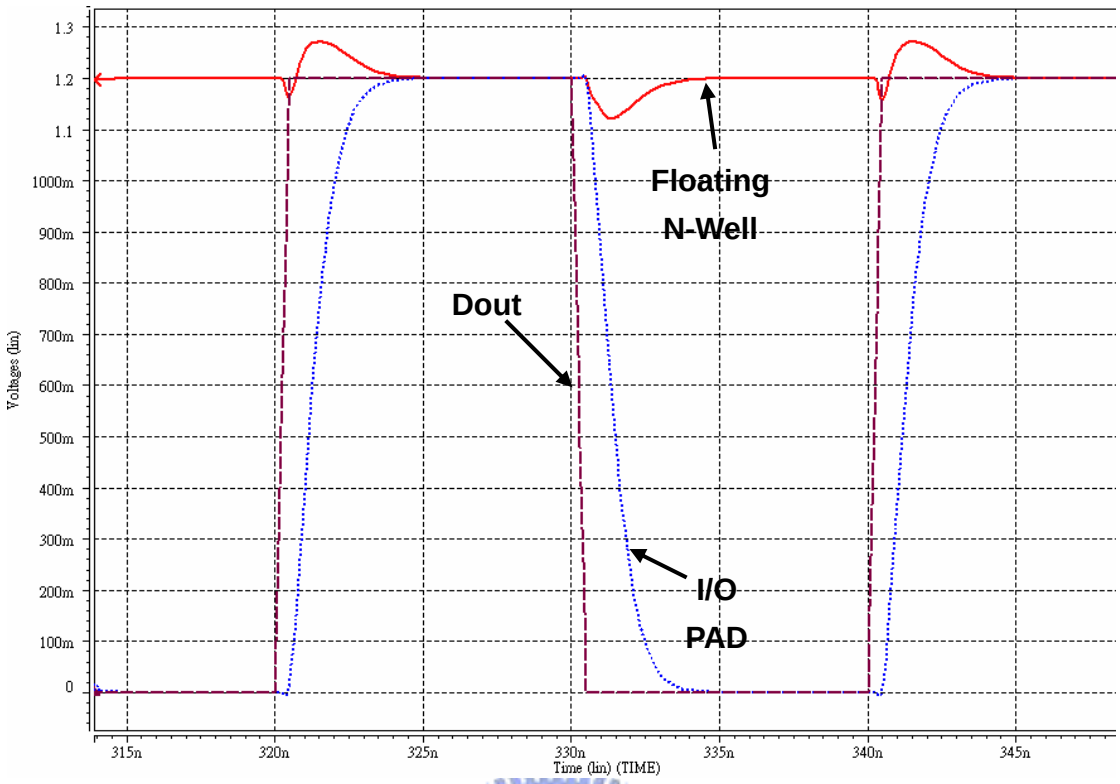
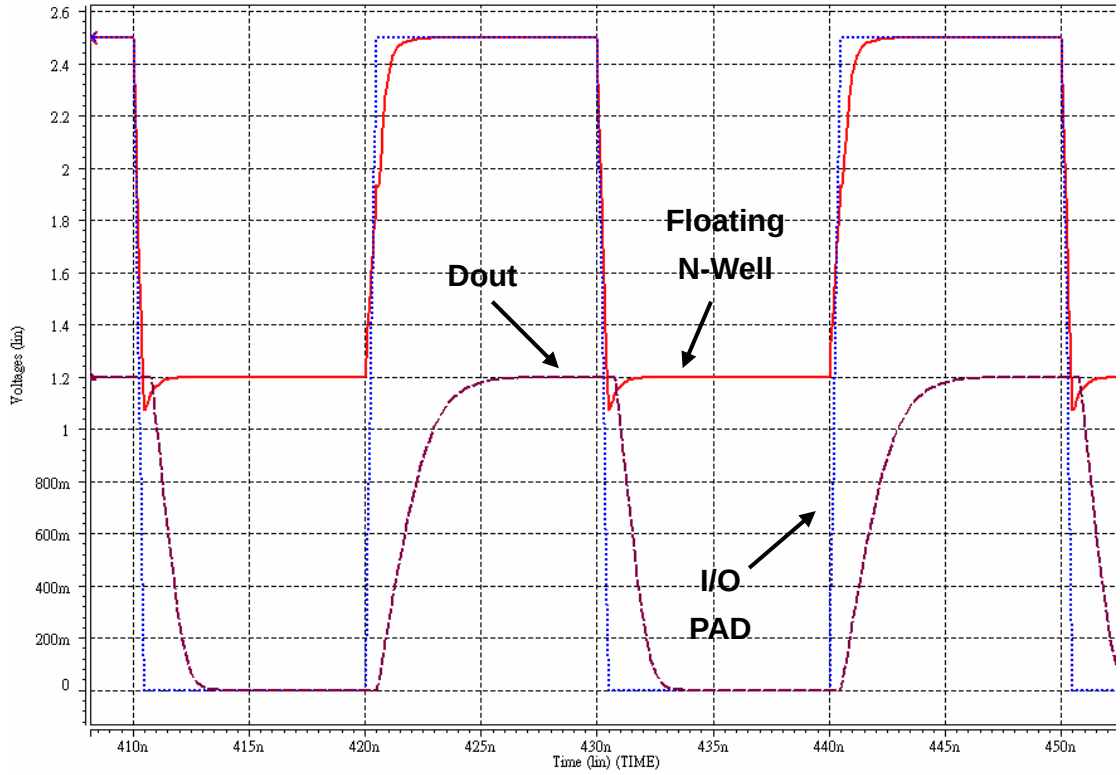


Fig. 3.4 The circuit schematic of completed mixed-voltage I/O cell with gate-tracking circuit and dynamic n-well bias circuit.

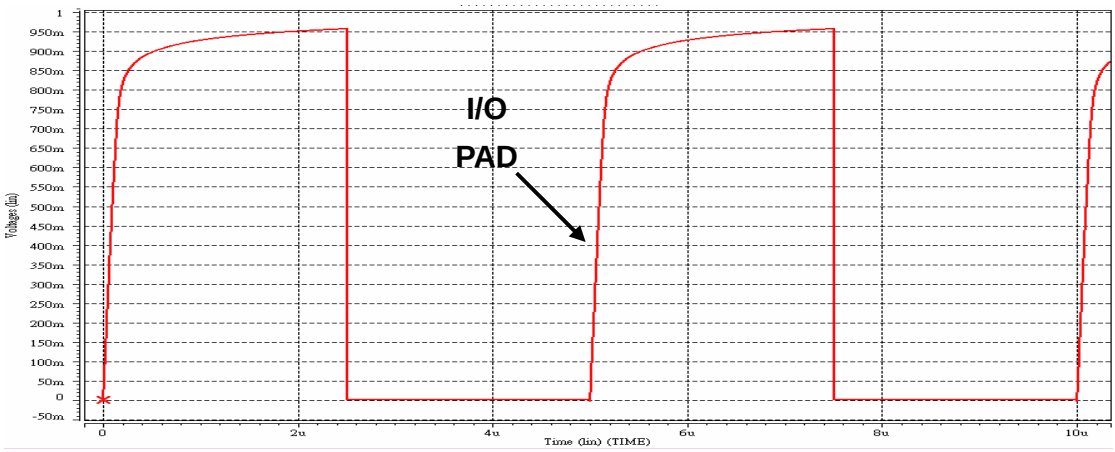


(a)



(b)

(Continued to the next page of Fig. 3.5)



(c)

Fig. 3.5 The simulated waveforms of the new proposed mixed-voltage I/O cell with a 20-pF load and 50-MHz I/O signal in (a) the transmit mode, (b) the tristate input (receive) mode, and (c) the transient simulation of pull-up for floating pad in 200-KHz.

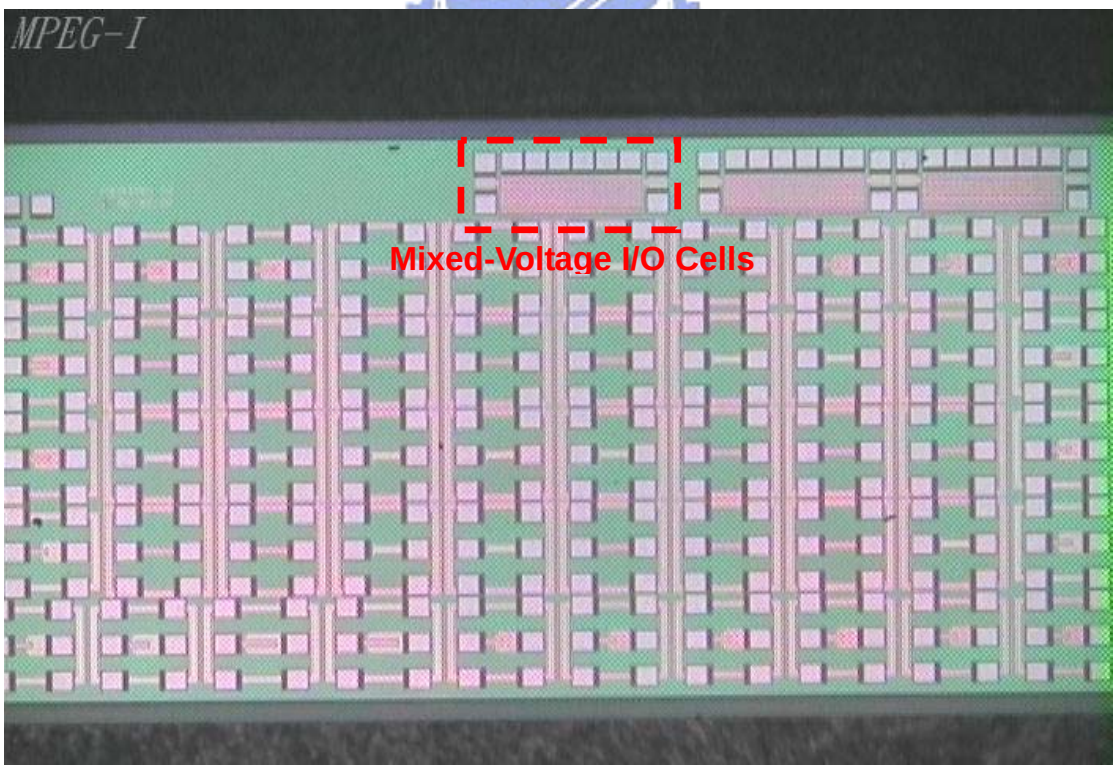


Fig. 3.6 The die photo of the 1.2/2.5-V mixed-voltage I/O cells with gate-tracking circuit and dynamic N-well bias shown by only using only thin oxide devices.

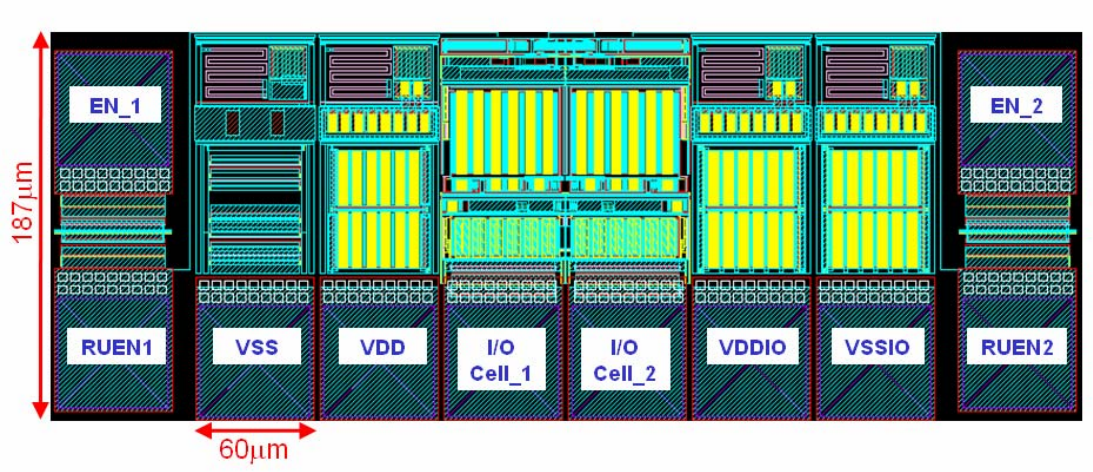


Fig. 3.7 The layout view of the new 1.2/2.5-V mixed-voltage I/O cell with gate-tracking circuit and dynamic n-well bias.

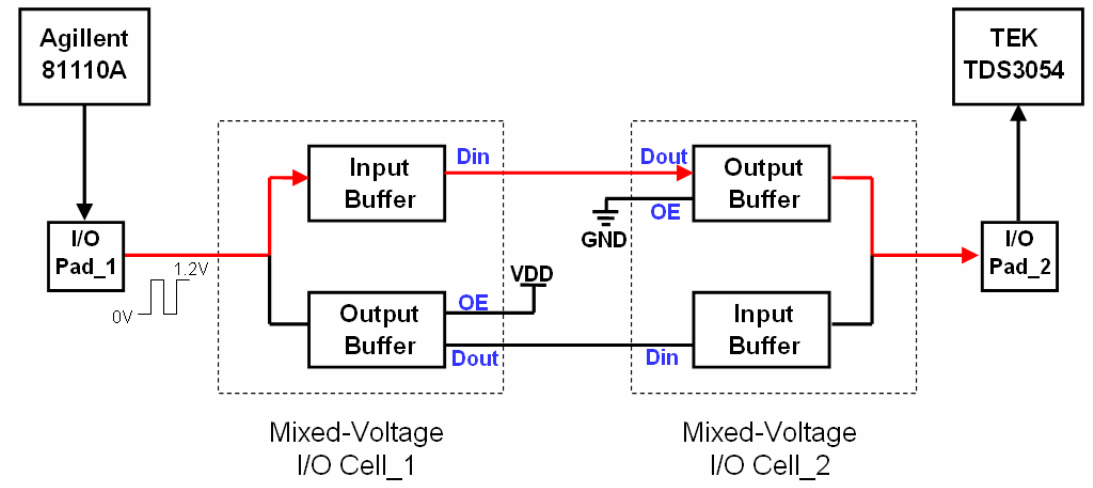
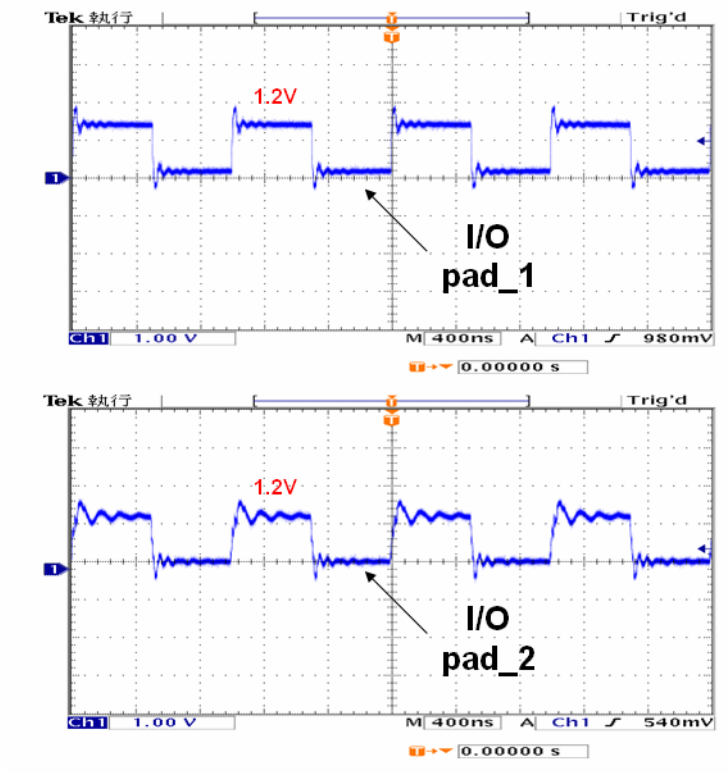
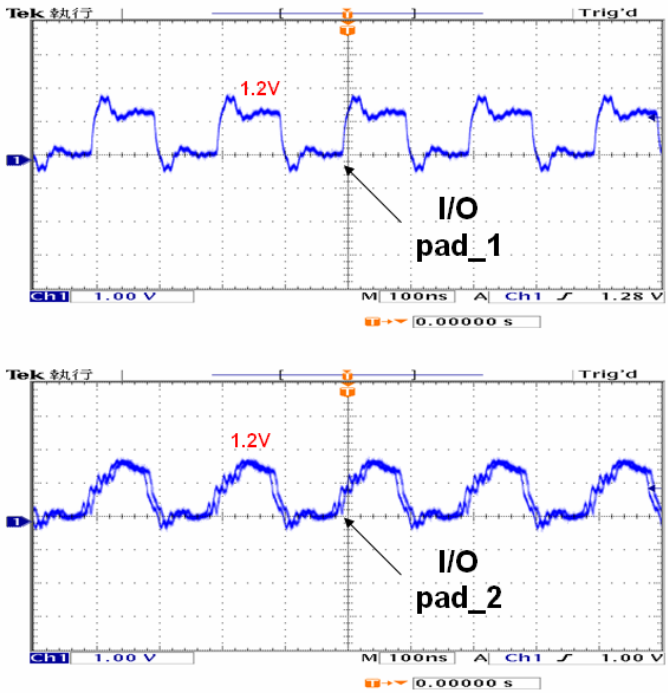


Fig. 3.8 The measurement setup for testing the new 1.2/2.5-V mixed-voltage I/O cell with only thin oxide devices and dynamic n-well bias in transmit mode and receiving mode with 0/1.2-V input signal.



(a)



(b)

Fig. 3.9 The measurement results of the new 1.2/2.5-V mixed-voltage I/O cell in transmit mode and receiving mode with (a)1-MHz and (b)5-MHz 0/1.2-V input signal.

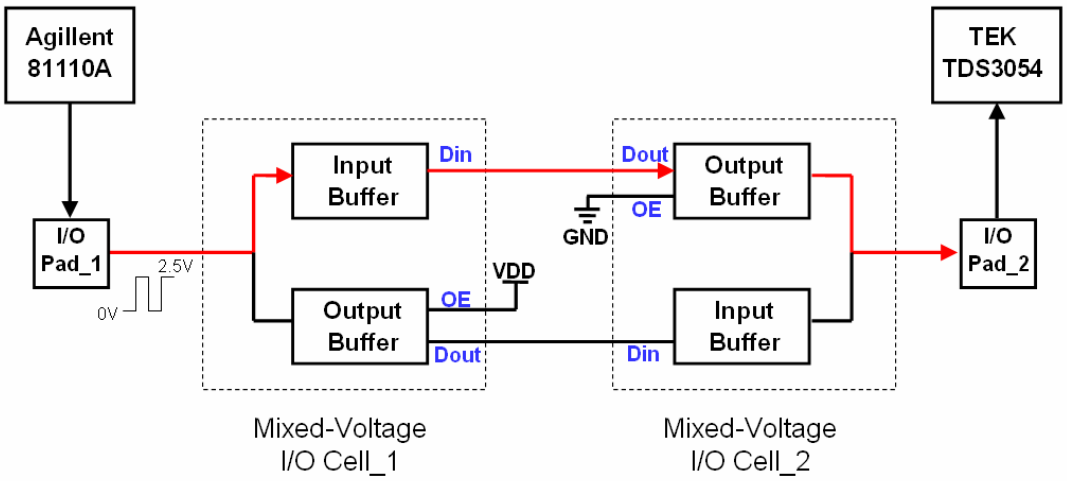
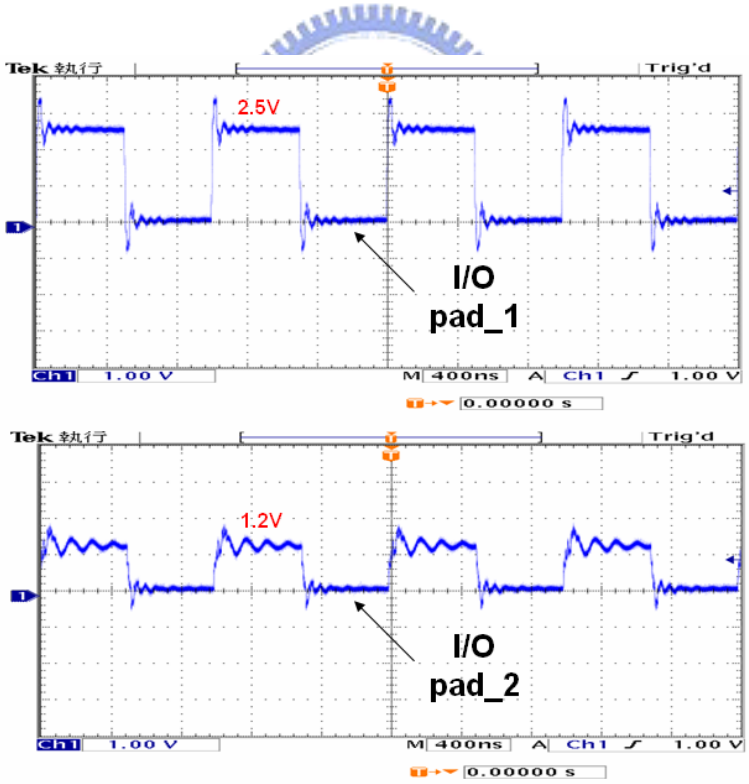
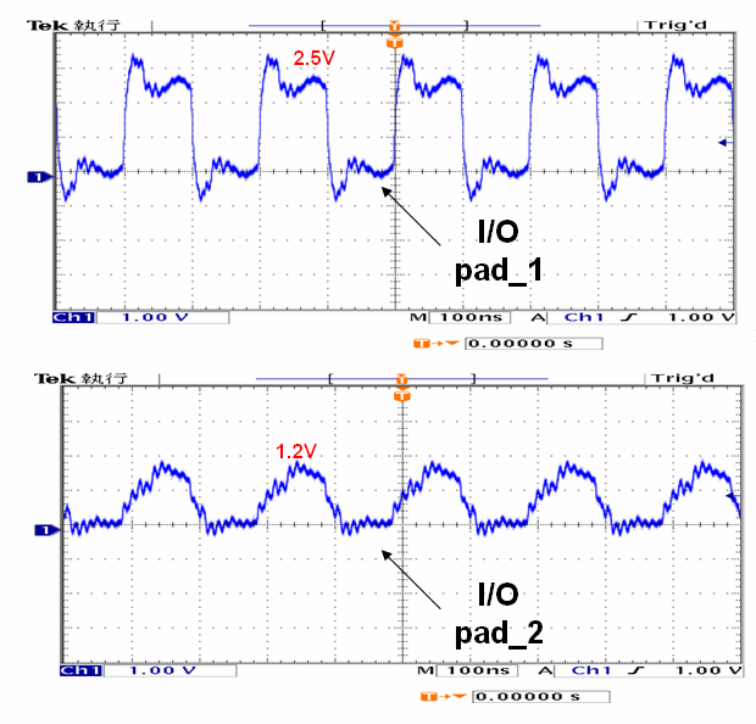


Fig. 3.10 The measurement setup for testing the new 1.2/2.5-V mixed-voltage I/O cell with gate-tracking circuit and dynamic n-well bias in transmit mode and receiving mode with 0/2.5-V input signal.



(a)

(Continued to the next page of Fig. 3.11)



(b)

Fig. 3.11 The measurement results of the new 1.2/2.5-V mixed-voltage I/O cell in transmit mode and receiving mode with (a)1-MHz and (b)5-MHz 0/2.5-V input signal.

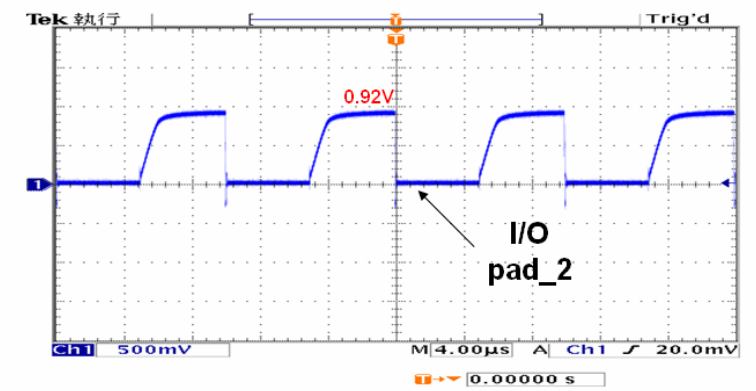


Fig. 3.12 The measurement result of the new 1.2/2.5-V mixed-voltage I/O cell for Pull-up function.

Chapter 4

New Proposed Mixed-Voltage Crystal Oscillator Circuit I

4.1 INTRODUCTION

In the advanced CMOS process technology, the complication and the requirement of precision have greatly increased in ICs, and also the clock rate is getting fast. In the same time, it becomes an important subject to sustain a high stability and precision of clock signal. And that is why a crystal oscillator is one of the most widely used circuits in modern digital ICs due to its stable and precise oscillation frequency.

A conventional crystal oscillator circuit is connected with a crystal between the output (XO) pad and the input (XI) pad for oscillation to generate the stable clock signal in the chip [27], [28]. In some applications, the clock signal will be directly provided from the external clock sources and sent into the chip through the input (XI) pad with the output (XO) pad floating. But, the conventional crystal oscillator circuit design with 1xVDD CMOS devices is unsuitable to receive the external clock signal with voltage level over 1xVDD, due to the gate-oxide reliability issue [5], [15] and the hot-carrier degradation issue [6].

The mixed-voltage I/O circuits had been discussed and presented in some prior papers [18]-[19], [24]-[26], but the mixed-voltage crystal oscillator circuit was never discussed before. In this chapter, a new mixed-voltage crystal oscillator circuit I realized with low-voltage CMOS devices is proposed without suffering the gate-oxide

reliability issue and undesired leakage current path. The new proposed mixed-voltage crystal oscillator circuit I has been designed and realized in UMC 130-nm 1.2-V CMOS process to server 1.2/2.5V mixed-voltage interface applications and TSMC 90-nm 1-V CMOS process to server 1/1.8V mixed-voltage interface applications.

4.1.1 Basic Resonance Theory

Fig. 4.1 shows a basic architecture of an oscillator circuit. This circuit includes two parts, an amplifier that provides a voltage gain $A(s)$ and a feedback network $\beta(s)$. When a trigger signal S_s is applied to the circuit, a total transfer function $A_f(s)$ of the loop can be got by

$$S_f = \beta(s)S_0,\ \ S_S + S_f = S_i,\ \ S_0 = A(s)S_i$$

and hence

$$A_f(s) = \frac{S_0}{S_S} = \frac{A(s)}{1 - A(s)\beta(s)} \tag{4-1}$$

When the loop gain is

$$A(j\omega_0)\beta(j\omega_0)=1 \tag{4-2}$$

$$A_f(s) = \infty \tag{4-3}$$

It means the signal with frequency ω_0 could be held and amplified in the loop without keeping the signal S_s. In order for an oscillator circuit to operate and by the condition of the equation (4-2), two conditions must be met: (A) The loop gain must be equal to unity; (B) The loop phase shift must be equal to 0, 2Pi, 4Pi, etc. radians. And these two conditions are called Barkhausen criterion.

4.1.2 Equivalent Circuit of Crystal

Quartz crystal units serve as the controlling element of oscillator circuits by conversion of mechanical vibrations to electrical current at a specific frequency. This is accomplished by means of the "Piezoelectric" effect. Piezoelectricity is electricity created by pressure. In a piezoelectric material, the application of mechanical pressure along an axis will result in the creation of an electrical charge along an axis at right angles to the first. In some materials, the obverse piezoelectric effect is found, which means that the imposition of an electric field on the ends of an axis will result in a mechanical deflection along an axis at right angles to the first. Quartz is uniquely suited, in terms of mechanical, electrical and chemical properties, for the manufacture of frequency control devices. Quartz crystal units which oscillate within certain frequency and temperature ranges have been developed over the years.

The equivalent circuit of a crystal is shown in Fig. 4.2. R_s is the effective series resistance in the crystal; as well as L_s and C_s are the motional inductance and capacitance of the crystal. C_p is the parasitic shunt capacitance due to the electrodes. In parallel resonant mode, the crystal will look inductive to the circuit. At the resonant frequency, the crystal will look and perform like a low resistance. And some typical crystal parameters in different oscillation frequency are listed in Table 4.1.

Fig. 4.3 shows the reactance-frequency plot of the crystal. And the equivalent circuit impedance is given by the equation (4-4)

$$Z = \frac{1-\omega^2 C_s L_s}{-j\omega\left[\omega^2 L_s C_s C_p - (C_p + C_s)\right]} \tag{4-4}$$

When the crystal is operating at series resonance, it looks purely resistive and the series resonance frequency (f_s) is given by the equation (4-5)

$$f_s = \frac{1}{2\pi\sqrt{L_s C_s}} \tag{4-5}$$

When the crystal is operating in parallel resonant mode, it looks inductive. In this mode, the frequency (f_a) of oscillation is given by the equation (4-6)

$$f_a = \frac{1}{2\pi\sqrt{L_S \frac{C_S C_P}{C_S + C_P}}} \tag{4-6}$$

4.1.3 Pierce-Type Crystal Oscillator

The conventional Pierce-type crystal oscillator circuit is shown in Fig. 4.4. This circuit consists of two parts. One is an inverting amplifier that supplies a voltage gain and 180 degree phase shift, which is integrated into the chip with the XI and XO pads. The other is a frequency selective feedback network, which is out of the chip. The crystal combined with C_1 and C_2 to form a feedback network that tends to stabilize the frequency and supply 180 degree phase shift to the feedback path. The feedback resistance, R_f, is used to bias the inverting amplifier around half of power supply voltage, therefore the inverting amplifier is operating in the high gain linear region. In steady state, this circuit has an overall phase shift around 360 degree. This satisfies one of the conditions required to sustain oscillation. The other condition for proper start-up and sustaining oscillation is that the closed loop gain should be over or equal to unity.

4.1.4 Evaluation of Minimum Inverting Gain g_m

Fig. 4.5 (a) and Fig. 4.5 (b) show the used Pierce oscillator circuit with its

equivalent circuit diagram, in which the crystal is replaced by L_s, C_s, R_s and C_p. The inverter is replaced by its output impedance Ro and the output current from the transconductance gain: $I_{out}= g_m*V_1$. R_f is a feedback resistance to force the gate input to its threshold level to provide starting up. In most microcontroller-types the feedback transistor R_f is already integrated as a semiconductor resistor parallel to the inverting gate.

A very convenient way and also rather easy to prove the oscillation condition is to transfer all these elements in series with R_s by means of the power dissipation rule, saying that the elements R_o, R_f and g_m*V_1 are replaceable by a resistor in series with R_s, if this gives the same dissipation or damping to the circuit. Then the oscillation condition is true, if the total value of the resistive elements, including the own damping R_s of the crystal is less than zero.

After transferring all resistive elements into the series branch, the simplified resonance calculation model of fig. 4.6 can be used. In this figure, C_o is the total parallel capacitance, including load capacitance C_{load} formed by the capacitances C_1 and C_2 in series and the parasitic capacitance C_{par} at input and output parallel with the gate and C_p as following:

$$C_o = C_p + C_{load} + C_{par}$$

$$C_{load} = C_1 C_2 /(C_1 + C_2)$$

The value of R_t is given by $R_t= R_s + R_f' +R_o' +R_{gm}'$. Assuming that in resonance, $I_{Rt} = I_{Co}$, then it follows for R_f':

$$P_{R_f} = P_{R_f'}$$
$$(V_X)^2 / R_f = I_{R_t}^2 * R_f'$$
$$I_{R_t} = I_{C_o} = V_X \omega_0 C_0$$
$$(V_X)^2 / R_f = (V_X \omega_0 C_0)^2 * R_f'$$

$$R_f' = \frac{1}{(\omega_0 C_0)^2 * R_f} \tag{4-7}$$

For the output impedance Ro follows with $P_{Ro} = P_{Ro'}$:

$$\begin{aligned}
&P_{Ro} = P_{Ro'} \\
&(V_2)^2 / R_o = I_{Ro}^2 * R_o' \\
&V_2 = V_X * C_1 / (C_1 + C_2) \\
&I_{Ro} = I_{Co} = V_X \omega_0 C_0 \\
&(V_X * C_1 / (C_1 + C_2))^2 / R_o = (V_X \omega_0 C_0)^2 * R_o'
\end{aligned}$$

$$R_o' = \frac{1}{(\omega_0 C_0)^2 * R_o} * \frac{C_1^2}{(C_1 + C_2)^2} \tag{4-8}$$

Transferring $I_{out} = g_m * V_1$ to R_{gm}' means, with $P_{(gm*V1)} = P_{Rgm}$':

$$\begin{aligned}
&P_{(gm \cdot V_1)} = P_{R'gm} \\
&-gmV_1V_2 = I_{Rt}^2 * R_{gm}' \\
&V_1 = V_X * C_2 / (C_1 + C_2) \\
&V_2 = V_X * C_1 / (C_1 + C_2) \\
&I_{Rt} = I_{Co} \\
&-gm \cdot V_X^2 \cdot C_1 \cdot C_2 / (C_1 + C_2)^2 = (V_X \omega_0 C_0)^2 R_{gm}'
\end{aligned}$$

$$R'_{gm} = \frac{-gm}{(\omega_0 C_0)^2} * \frac{C_1 C_2}{(C_1 + C_2)^2} \tag{4-9}$$

Combining these equations, we obtain for the total series resistance:

$$R_t = R_s + \frac{1}{(\omega_0 C_0)^2} \left\{ \frac{1}{R_f} + \frac{1}{R_0} \left(\frac{C_1}{C_1 + C_2} \right)^2 - g_m \frac{C_1 C_2}{(C_1 + C_2)^2} \right\} \tag{4-10}$$

The circuit will oscillate, if the value of R_t is zero or negative. So the minimum value of gm should be:

$$g_m \geq R_s \times \frac{(\omega_0 C_0)^2 (C_1 + C_2)^2}{C_1 C_2} + \frac{1}{R_f} \frac{(C_1 + C_2)^2}{C_1 C_2} + \frac{1}{R_o} \frac{C_1}{C_2} \tag{4-11}$$

The first two products of this equation are reduced to a minimum value with $C_1 = C_2$.

To achieve minimum requirement of oscillation, both load capacitances should be equal. In this case we find:

$$g_m.\min \geq R_s \times 4(\omega_0 C_0)^2 + \frac{4}{R_f} + \frac{1}{R_o} \tag{4-12}$$

4.2 GATE-OXIDE RELIABILITY ISSUE IN CONVENTIONAL CRYSTAL OSCILLATOR CIRCUIT

In the advanced CMOS process, the devices with thinner gate oxide can be operated at a higher operating speed under a lower VDD supply voltage. The power supply voltage level has been decreased from 2.5V to around 1V to maintain the gate-oxide reliability and to overcome the hot-carrier degradation. However, many other components on the board or in the system are still operated at another higher voltage level such as 3.3V or 5V. This is also a challenge to the interface circuit to avoid the gate-oxide reliability problem.

Fig. 4.7 shows the conventional crystal oscillator circuit realized with the 1×VDD devices. When this circuit was used in the mixed-voltage interface, it will suffer the gate-oxide reliability issues. When the EN signal is kept at VDD and the external input clock signal at the XI pad rises up to 2×VDD. The pull-up PMOS and pull-down NMOS will suffer the gate-oxide overstress issue. In order to avoid the gate-oxide reliability issue, the devices which suffer the gate-oxide overstress could be replaced by the thick-oxide devices. However, with both of the thick-oxide and thin-oxide devices in a chip, the fabrication cost of CMOS process is increased.

4.3 CIRCUIT DESCRIPTION

Fig. 4.8 shows the new proposed mixed-voltage crystal oscillator circuit I realized with only the thin gate-oxide (1×VDD) devices. XI pad and XO pad are the input and output pads of the proposed mixed-voltage crystal oscillator circuit I, respectively. EN and PA signals are controlled by the internal circuits of IC. XC is the clock signal which is produced by crystal oscillator circuit or to receive the external clock signal into the IC.

When the voltage level of PA signal is VDD, the proposed mixed-voltage crystal oscillator circuit I is operated with crystal and two load capacitances to generate the sinusoidal-wave signal at both XI pad and XO pad. Transmission gates TRAN1 and TRAN2 are turned off, so that the sinusoidal-wave signal can't pass through the upper path of this circuit from XI pad to XO pad. Besides, transistor MN4 is turned on to keep transistor MN2 off and transistor MP3 on in order to keep the output terminal of the upper nand gate at VDD. The gate terminal of transistor MP4 is directly connected to the output terminal of the upper nand gate, so the transistor MP4 is turned off. The input terminal (N01) of the upper nand gate will follow the voltage level of XI pad, while the output terminal of upper nand gate keeps at VDD. Meanwhile, transmission gates TRAN3 and TRAN4 are turned on and the generated sinusoidal-wave signal will pass through the lower path of this circuit from XI pad to XO pad. The signal EN can be transmitted to one input terminal of the lower nand gate to enable or disable the lower nand gate. Besides, transistor MN7 and MP7 are turned off.

When the voltage level of PA signal is GND, the proposed mixed-voltage crystal oscillator circuit is operated to receive an external clock input signal whose voltage level could be 1×VDD or 2×VDD. Transmission gates TRAN1 and TRAN2 turn on and the external clock signal will pass through the upper path from XI pad to XC. The

signal EN can be transmitted to one input terminal of the upper nand gate to enable or disable the nand gate. Besides, transistor MN4 is turned off. Transistor MN1 and MP4 with upper nand gate are used to transfer the external clock signal from the XI pad to the XO pad. Transistor MN1 is used to limit the voltage level of external clock input signal reaching to the gate oxide of the upper nand gate. Because the gate terminal of transistor MN1 is connected to the power supply voltage (VDD), the input (N01) voltage of the upper nand gate is limited to VDD-Vt when the voltage level of external clock signal is even up to 2×VDD. Then, transistor MP4 will pull the input node (N01) of the upper nand gate up to VDD, when the output node of upper nand gate is pulled to GND. The external clock signal can be successfully transferred into the internal input node XC. Meanwhile, transmission gates TRAN3 and TRAN4 turn off. Transistor MN7 is turned on to keep transistor MN6 off and transistor MP6 on in order to keep the output terminal of the lower nand gate at VDD. Transistor MP7 is also turned on to keep the node between MN5 and MN6 at VDD. Thus, when the XI pad is with the input signal voltage level of 2×VDD, any voltage drop between the gate terminal and source/drain terminal of transistor MN5 and MP5 is still limited to VDD. So, the new proposed crystal oscillator circuit I can receive external clock signal of 2×VDD without suffering the gate-oxide overstress issue.

4.4 SIMULATION RESULTS

Fig. 4.9 shows the simulation waveforms of the proposed mixed-voltage crystal oscillator circuit I in a 130-nm 1.2-V CMOS process to serve 1.2/2.5-V mixed-voltage interface. As shown in Fig. 4.9(b), with the 30-MHz external clock signal of 2×VDD into XI pad and 20-pF load capacitance in XC, the input terminal (N01) voltage of the upper nand gate can be limited and biased at the desired voltage levels (1.2 V). The

final signal voltage level reaching to the XC node is successfully shifted down to 1×VDD. The proposed mixed-voltage crystal oscillator circuit I can be operated correctly without the gate-oxide reliability issue. In Fig. 4.9(a), the proposed mixed-voltage crystal oscillator circuit I with the crystal of 30-MHz fundamental frequency and a load capacitance 20-pF at the pad can successfully generate the clock signal of 30-MHz at the XC node under the power supply of 1×VDD. As these simulations, the desired functions of this mixed-voltage crystal oscillator circuit I have been verified.

Fig. 4.10 shows the simulation waveform of the proposed mixed-voltage crystal oscillator circuit I in a 90-nm 1-V CMOS process to serve 1/1.8-V mixed-voltage interface. As shown in Fig. 4.10(b), with the 30-MHz external clock signal of 2×VDD into XI pad and 20-pF load capacitance in XC, the input terminal (N01) voltage of the upper nand gate can be limited and biased at the desired voltage levels (1V). The final signal voltage level reaching to the XC node is successfully shifted down to 1×VDD. The proposed mixed-voltage crystal oscillator circuit I can be operated correctly without the gate-oxide reliability issue. In Fig. 4.10 (a), the proposed mixed-voltage crystal oscillator circuit I with the crystal of 30-MHz fundamental frequency and a load capacitance 20-pF at the pad can successfully generate the clock signal of 30-MHz at the XC node under the power supply of 1×VDD. As these simulations, the desired functions of this mixed-voltage crystal oscillator circuit I have been verified.

4.5 EXPERIMENTAL RESULTS

Fig. 4.11 shows the layout view of the new proposed mixed-voltage crystal oscillator circuit I implemented in UMC 0.13-μm CMOS process. The cell size of XI, as well as XO, is only 183μm×60μm (including the bond pad), which is the same as

that of digital or analog I/O cell in a standard I/O cell library. The feedback resistance Rf, implemented by the poly resistance, is also included into the layout. ESD protection is also provided by following the ESD design rules given by the foundry to draw the layout for NMOS and PMOS devices which are directly connected to the pads.

Fig. 4.12 shows the layout view of the new proposed mixed-voltage crystal oscillator circuit I implemented in TSMC 90-nm 1-V CMOS process. The cell size of XI, as well as XO, is only 190.5μm×60μm (including the bond pad), which is the same as that of digital or analog I/O cell in a standard I/O cell library. The feedback resistance R_f, implemented by the poly resistance, is also included into the layout. ESD protection is also provided by following the ESD design rules given by the foundry to draw the layout for NMOS and PMOS devices which are directly connected to the pads.

Fig. 4.13 is the die photo of the new proposed mixed-voltage crystal oscillator circuit I implemented in TSMC 90-nm CMOS process. To test the function of the new proposed mixed-voltage crystal oscillator circuit I in oscillation mode, the measurement setup is shown in Fig. 4.14 for an external crystal of fundamental frequency 4-MHz and 20-MHz. Here, an external crystal is connected between the input pad (XI) and the output pad (XO) of the new proposed mixed-voltage crystal oscillator circuit I with two external capacitors respectively connected in the input pad (XI) and the output pad (XO). The control signal EN and PA are both at VDD. As the measurement results shown in Fig. 4.15 The new proposed mixed-voltage crystal oscillator circuit I can successfully oscillate and correctly generate the clock signals of frequency 4-MHz and 20-MHz at XC node in Figs. 4.15(a) and 4.15(b), respectively.

To test the function of the new proposed mixed-voltage crystal oscillator circuit I in receiving mode, the measurement setup is shown in Fig. 4.16 for a 0/1-V external

clock signal of frequency 4-MHz at the input pad (XI). Here, the XI pad of the new proposed mixed-voltage crystal oscillator circuit I is used as the input pad to receive the external clock signal from the pulse generator and the external clock signal will be transmitted to the oscilloscope by the XC pad. The control signal EN is at VDD and PA is at GND. As the measurement results shown in Fig. 4.17, the new proposed mixed-voltage crystal oscillator circuit I can successfully transmit the 0/1-V clock signal of frequency 4-MHz to the XC node.

To test the function of the new proposed mixed-voltage crystal oscillator circuit I in receiving mode for a 0/1.8-V external clock signal of frequency 4-MHz at the input pad (XI), the measurement setup is shown in Fig. 4.18. Here, the XI pad of the new proposed mixed-voltage crystal oscillator circuit I is used as the input pad to receive the external clock signal from the pulse generator and the external clock signal will be transmitted to the oscilloscope by the XC pad. The control signal EN is at VDD and PA is at GND. As the measurement results shown in Fig. 4.19, the new proposed mixed-voltage crystal oscillator circuit I can successfully transmit the 0/1.8-V clock signal of frequency 4-MHz to the XC node with the input clock signal shifted in 0/1-V. From the measurement results, the new proposed mixed-voltage crystal oscillator circuit I can be successfully operated in such a 1/1.8-V mixed-voltage I/O environment.

4.6 CONCLUSION

A new proposed mixed-voltage crystal oscillator circuit I with a control signal has been successfully designed and implemented in both UMC 130-nm 1.2-V CMOS process and TSMC 90-nm 1-V CMOS process, which can be operated in the 1.2/2.5-V and 1V/1.8V signal environment without the gate-oxide reliability problem, respectively. But the fabrication of new proposed crystal oscillator circuit I in UMC

130-nm 1.2-V CMOS process is still under going, so the measurements need to be followed. The new mixed-voltage crystal oscillator circuit I can be applied for external clock signal in input pad (XI) without the gate-oxide reliability problem. The new mixed-voltage crystal oscillator circuit I realized with 1xVDD devices can be applied in 1xVDD/2xVDD mixed-voltage interface.

Table 4.1

Typical crystal parameters.

Parameter	32 kHz Fundamental Frequency	200 kHz Fundamental Frequency	2 MHz Fundamental Frequency	30 MHz Fundamental Frequency
Rs	200 kΩ	2 kΩ	100 Ω	20 Ω
Ls	7000 H	27 H	529 mH	11 mH
Cs	0.003 pF	0.024 pF	0.012 pF	0.0026 pF
Cp	1.7 pF	9 pF	4 pF	6 pF

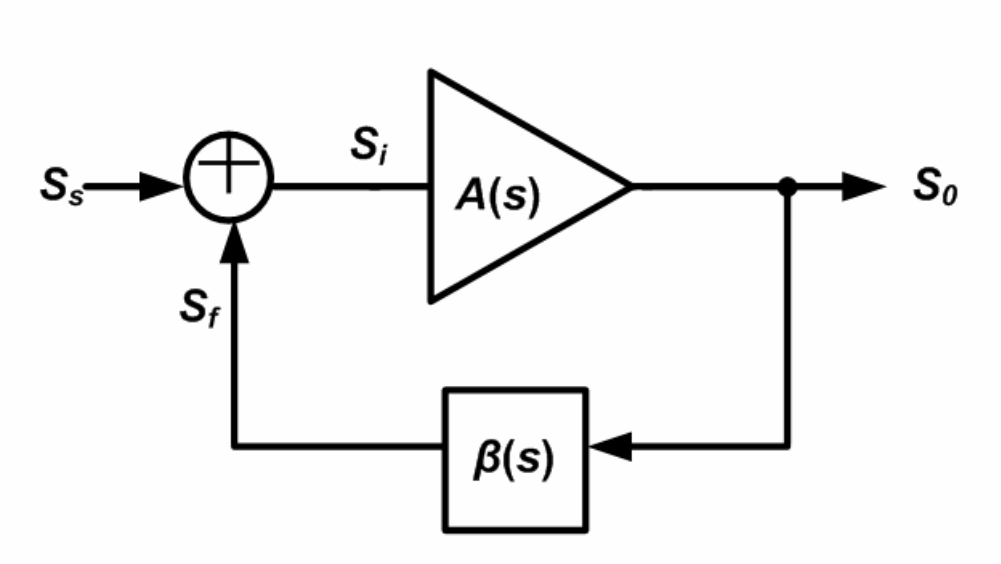


Fig. 4.1 The basic architecture of an oscillation circuit.

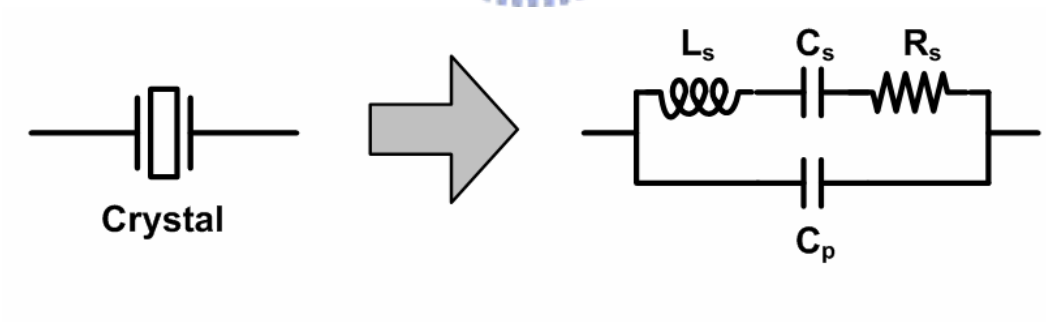


Fig. 4.2 The equivalent circuit of a crystal.

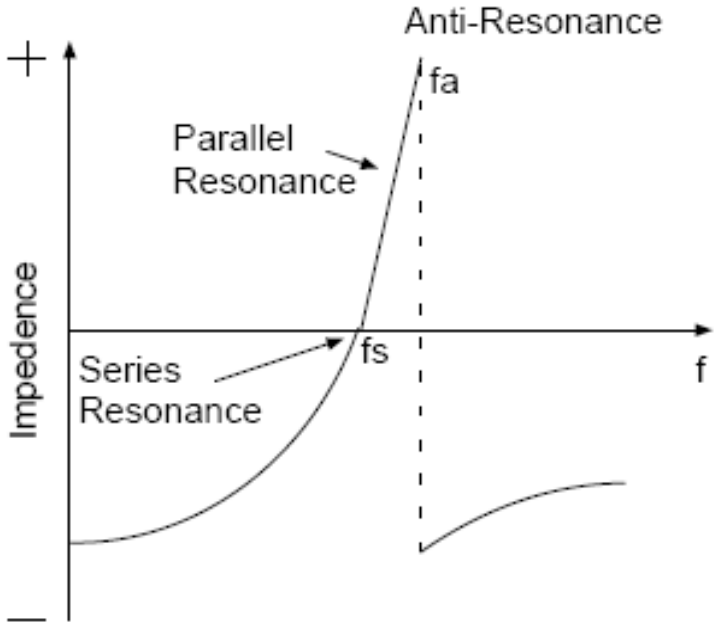


Fig. 4.3 The reactance vs. frequency plot of a crystal.

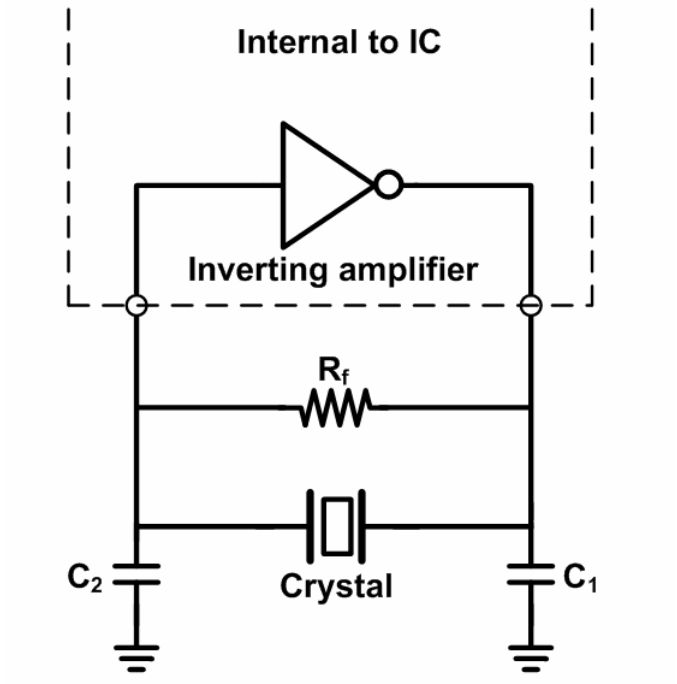
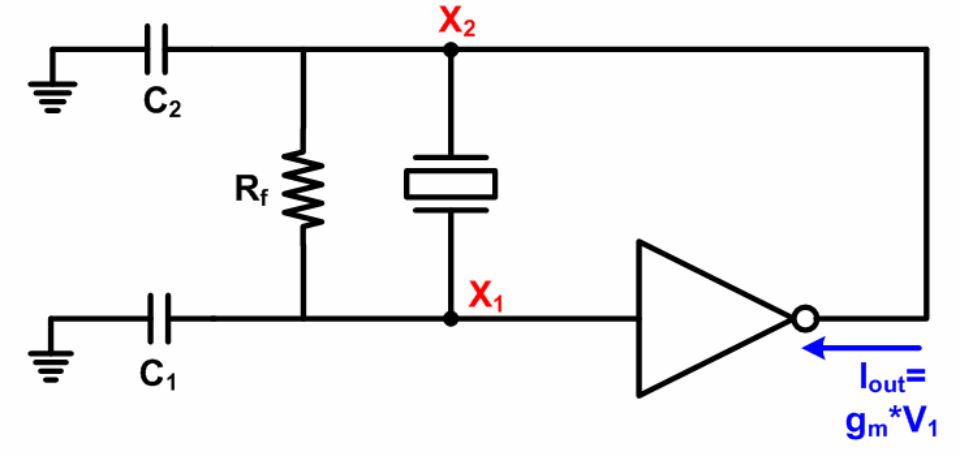
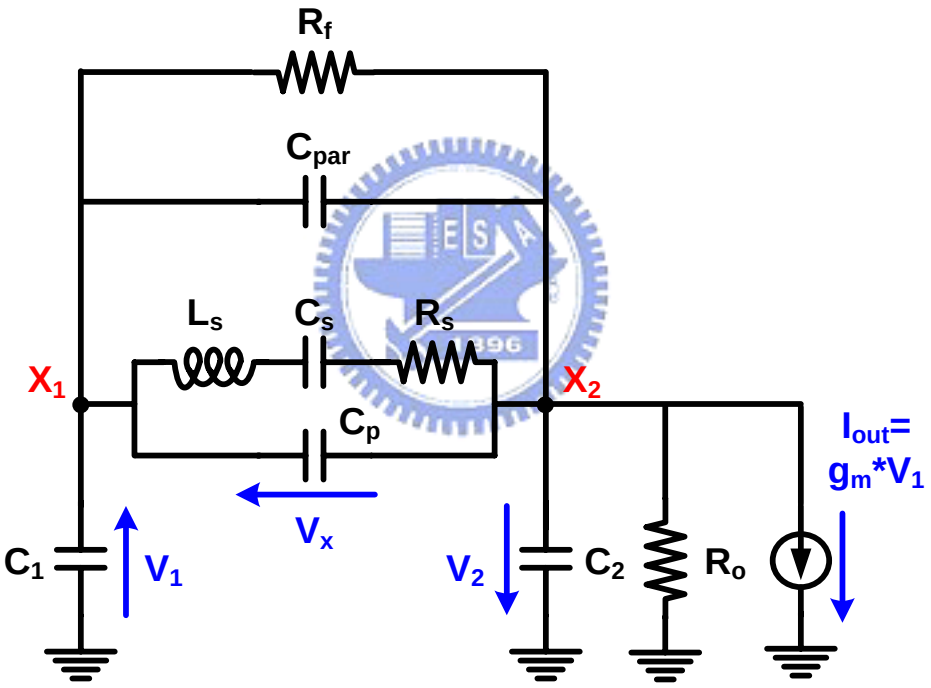


Fig. 4.4 The pierce-type crystal oscillator circuit.



(a)



(b)

Fig. 4.5 (a)The pierce-type crystal oscillator circuit and (b) its equivalent circuit.

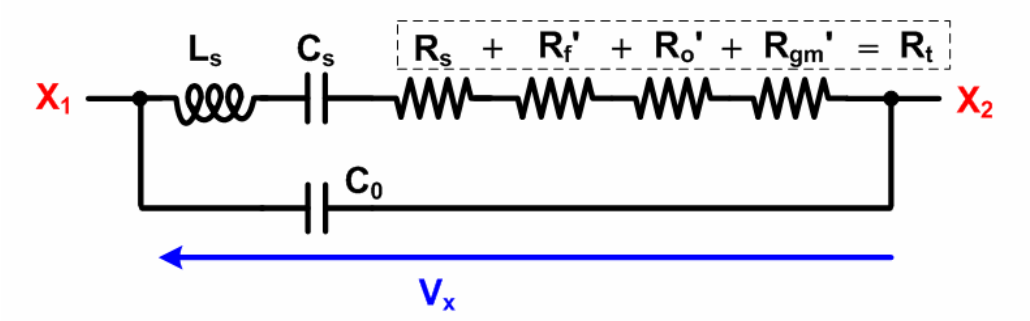


Fig. 4.6 The resonance calculation model.

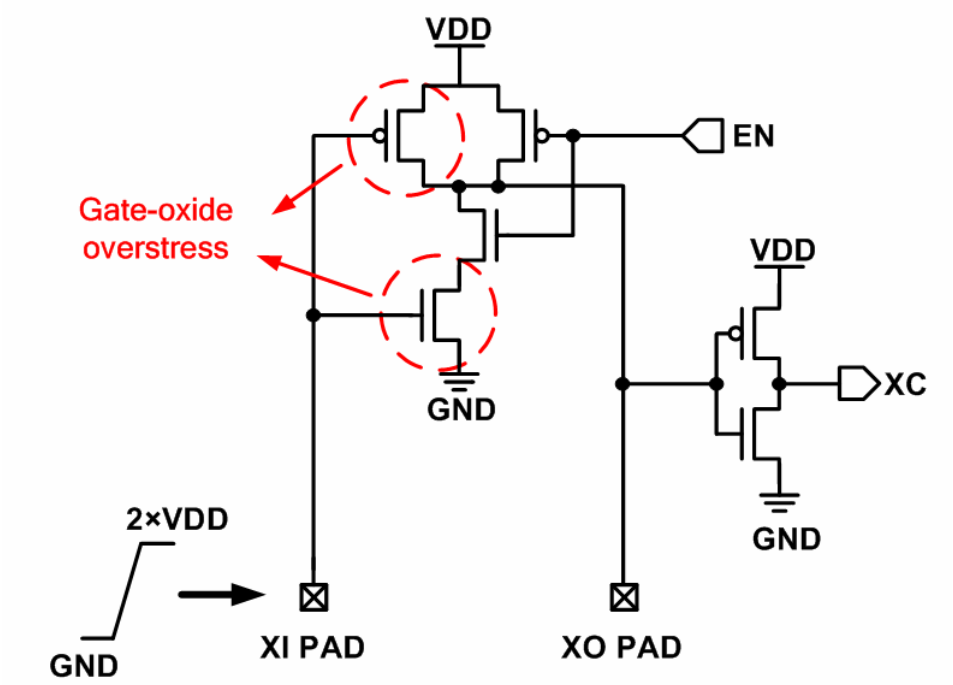


Fig. 4.7 The conventional crystal oscillator circuit suffering the gate-oxide reliability issue for receiving 2×VDD external clock signal.

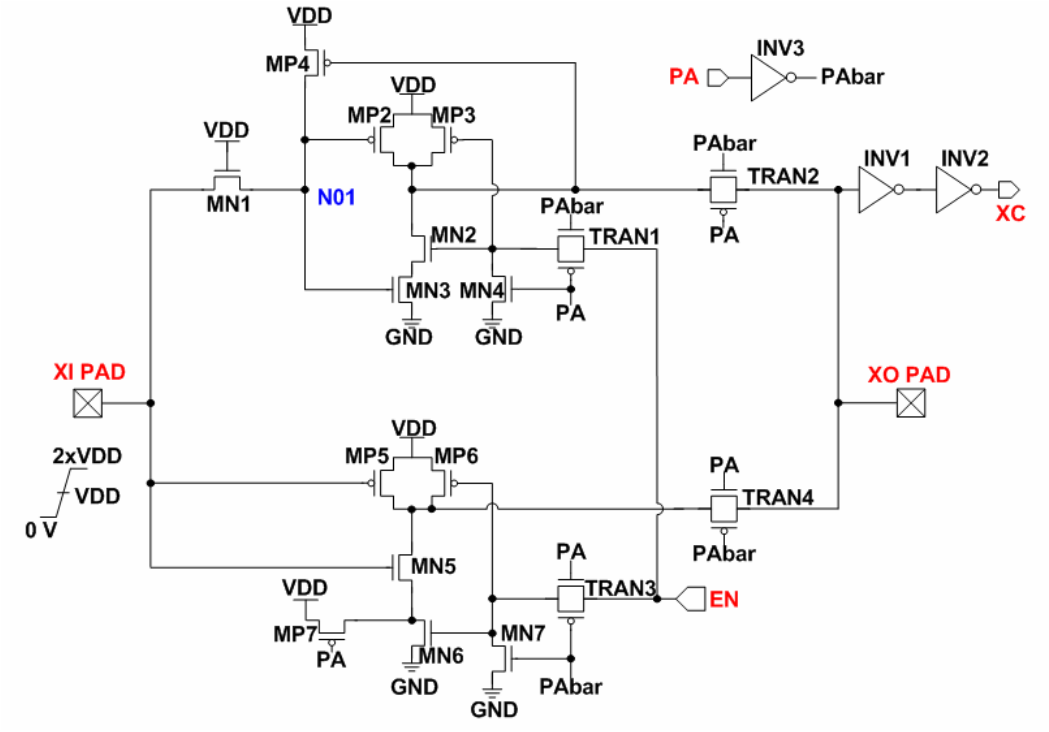
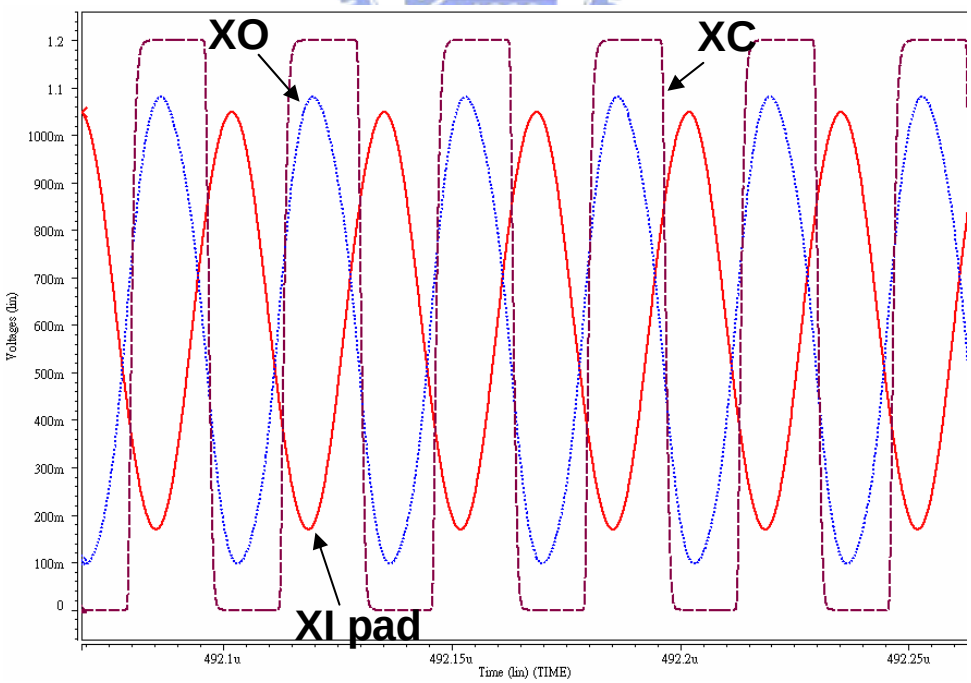
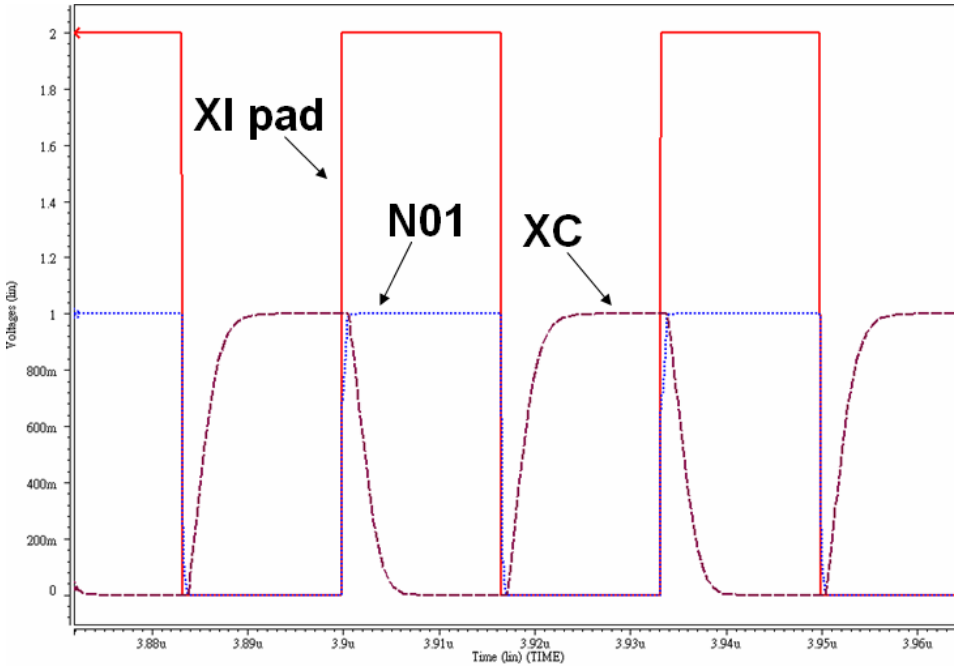


Fig. 4.8 The new proposed mixed-voltage crystal oscillator circuit I.

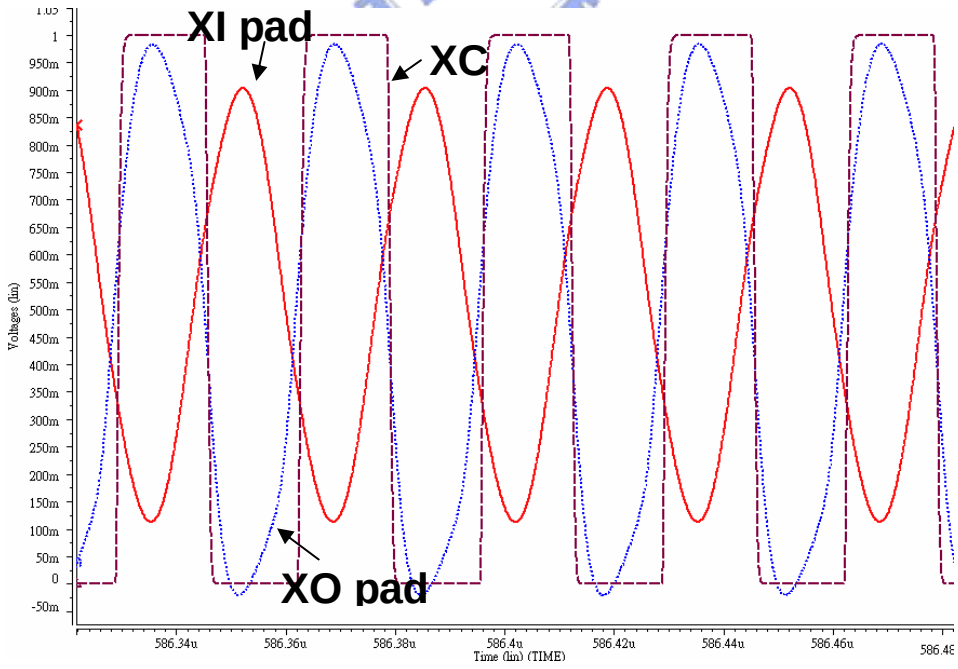


(a)



(b)

Fig. 4.9 The simulated waveforms of the new proposed crystal oscillator circuit I with (a) a crystal of fundamental frequency 30-MHz and load capacitance 20-pF (PA=VDD), and (b) 30-MHz external clock signal of 2×VDD into XI pad and 20-pF load capacitance in XC (PA=GND) in 130-nm 1.2-V CMOS process.



(a)

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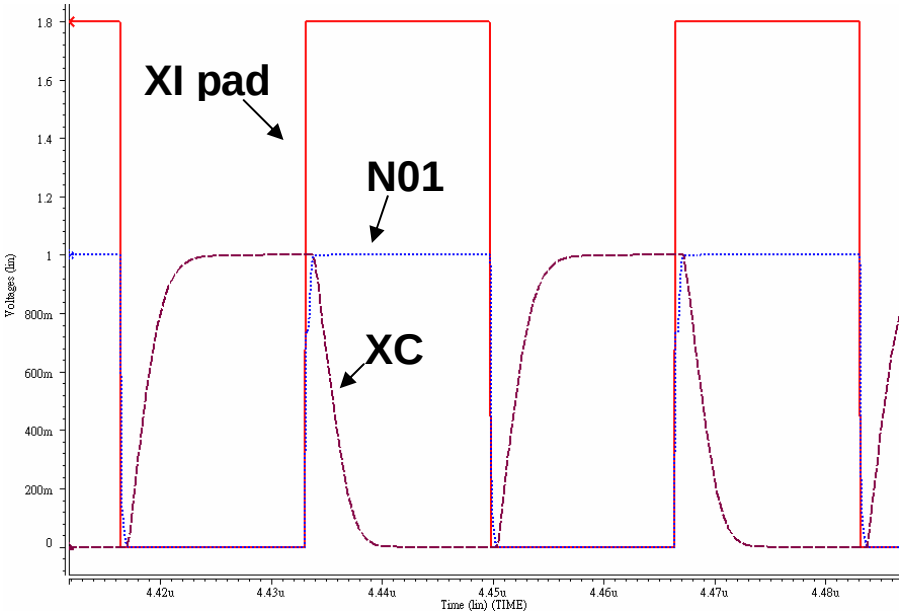


(b)

Fig. 4.10 The simulated waveforms of the new proposed crystal oscillator circuit I with (a) a crystal of fundamental frequency 30-MHz and load capacitance 20-pF (PA=VDD), and (b) 30-MHz external clock signal of 2×VDD into XI pad and 20-pF load capacitance in XC (PA=GND) in 90-nm 1-V CMOS process.

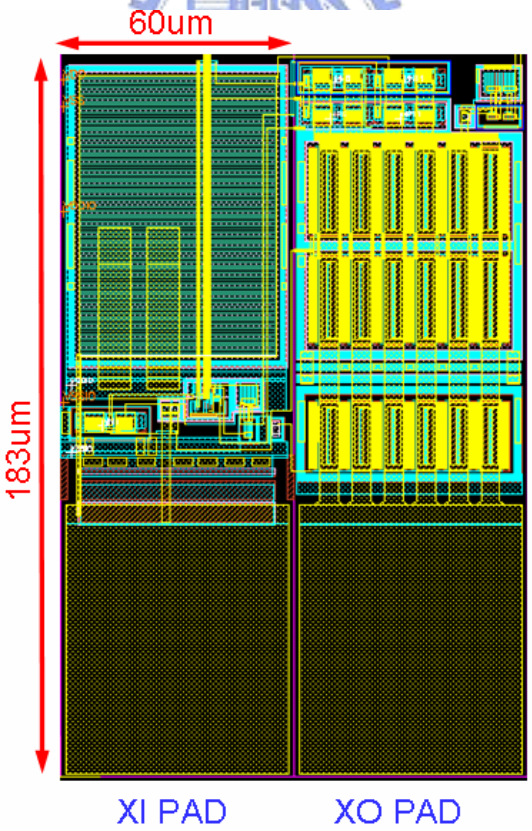


Fig. 4.11 The layout view of new proposed crystal oscillator circuit I realized in UMC 130-nm 1.2-V CMOS process.

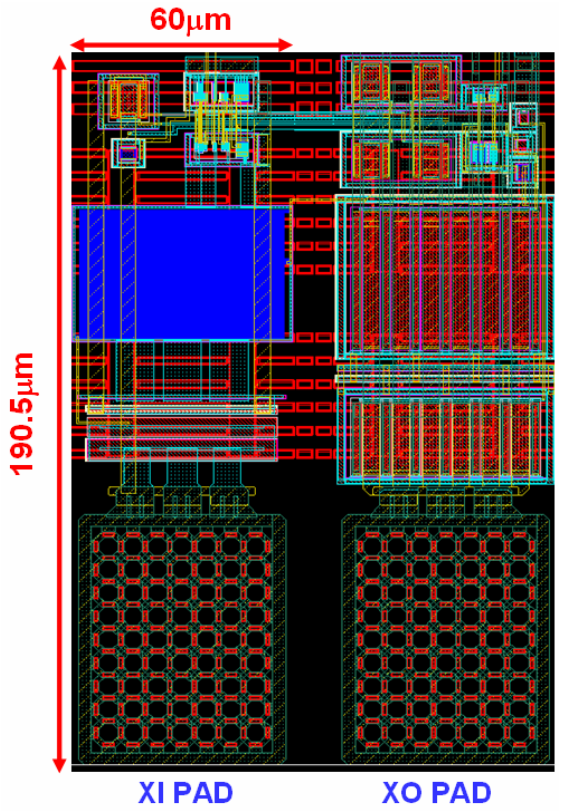


Fig. 4.12 The layout view of new proposed crystal oscillator circuit I realized in TSMC 90-nm 1-V CMOS process.

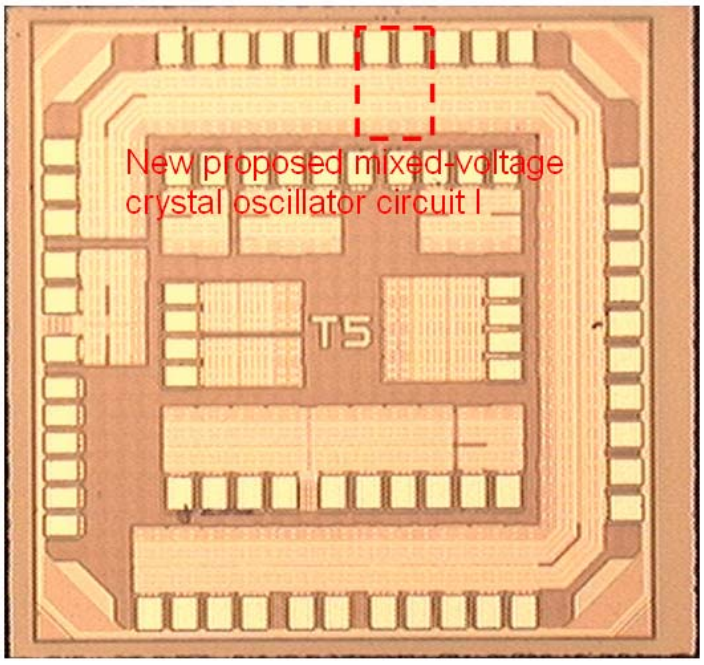


Fig. 4.13 The die photo of new proposed crystal oscillator circuit I realized in TSMC 90-nm 1-V CMOS process.

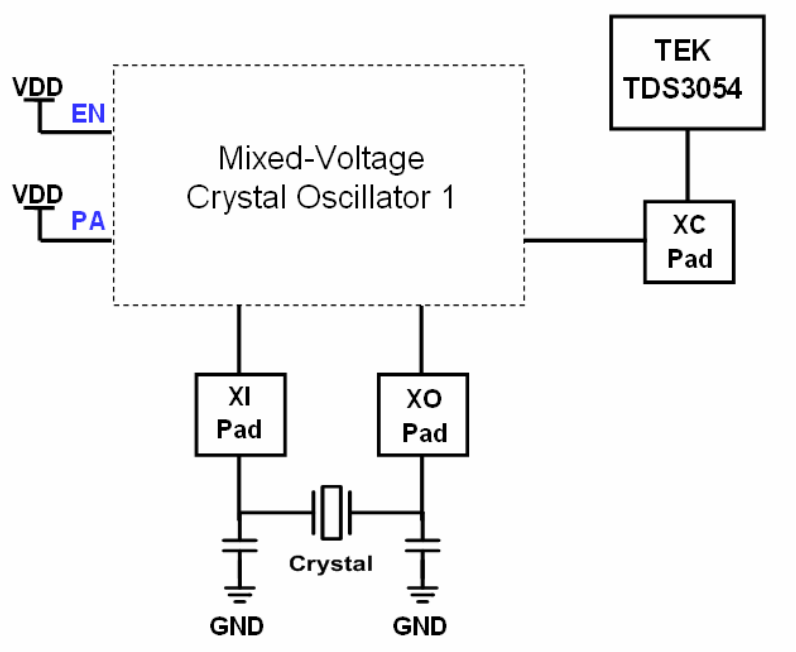
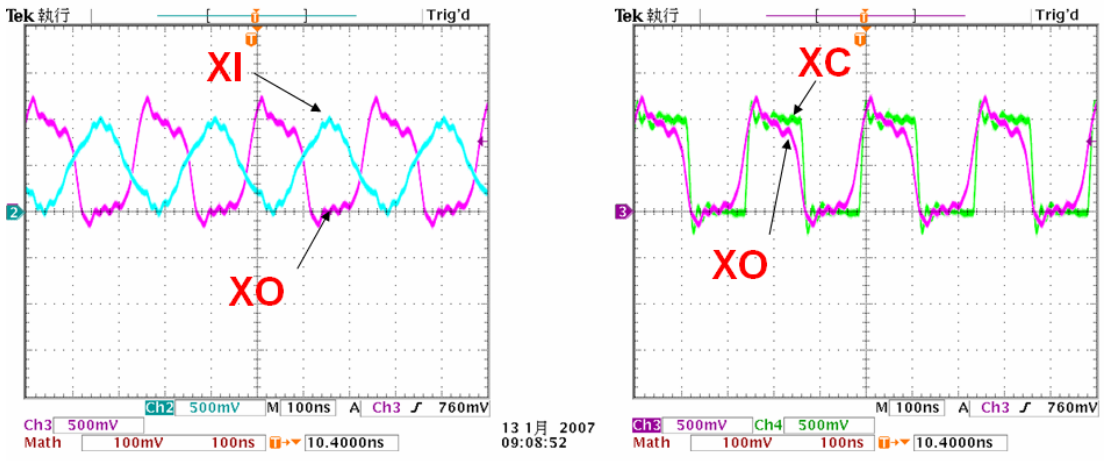


Fig. 4.14 The measurement setup for testing the new proposed mixed-voltage crystal oscillator I in oscillation mode.



(a)

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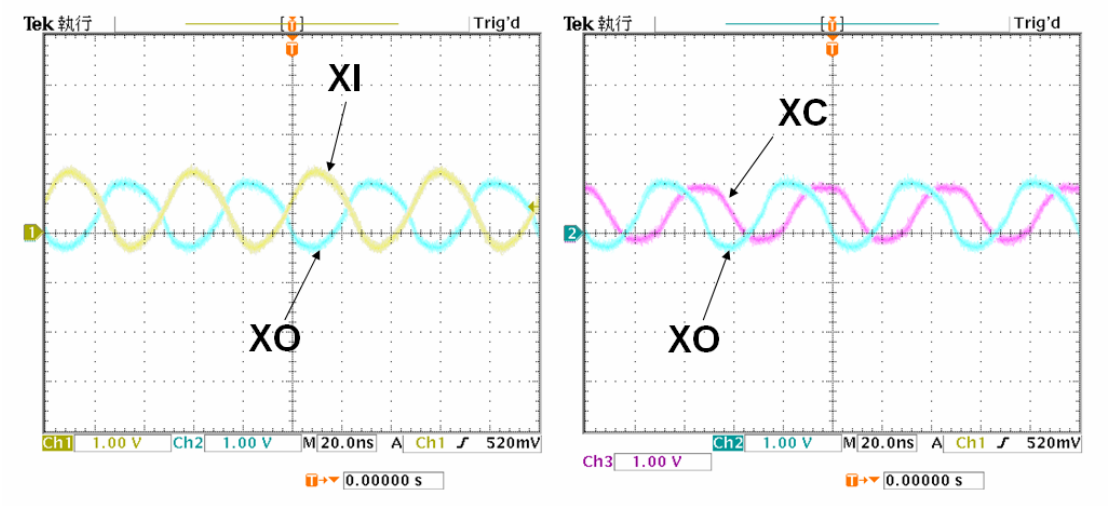


(b)

Fig. 4.15 The measurement results of the new proposed mixed-voltage crystal oscillator I in oscillation mode with a crystal of fundamental frequency (a)4-MHz and (b)20-MHz.

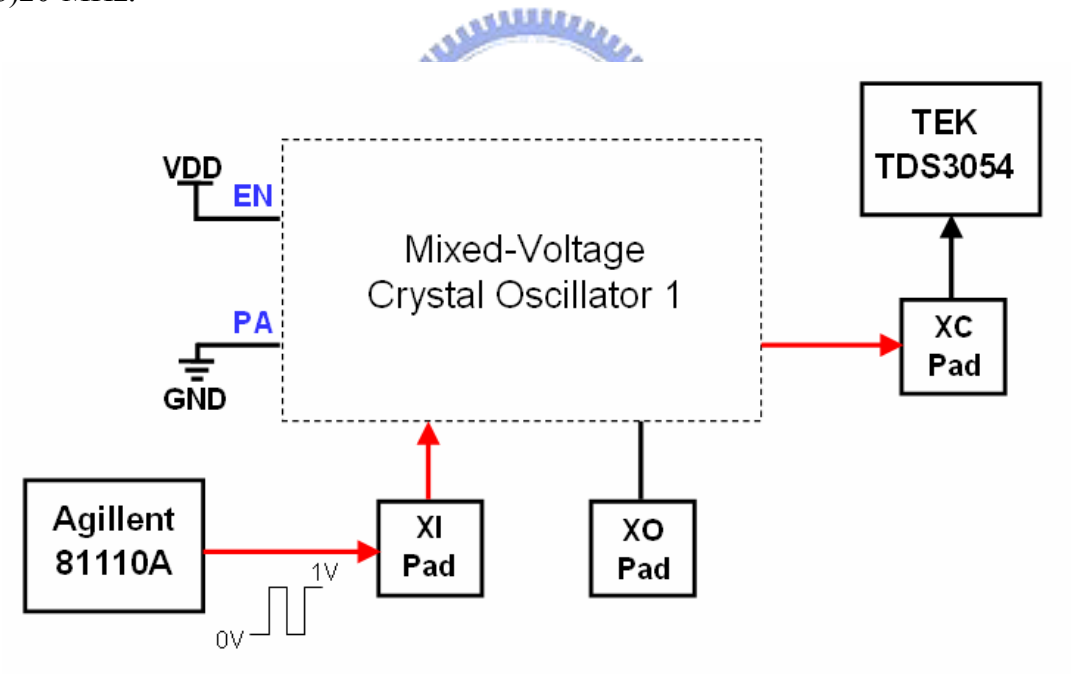


Fig. 4.16 The measurement setup for testing the new proposed mixed-voltage crystal oscillator I in receiving mode with a 4-MHz 0/1-V external input clock signal.

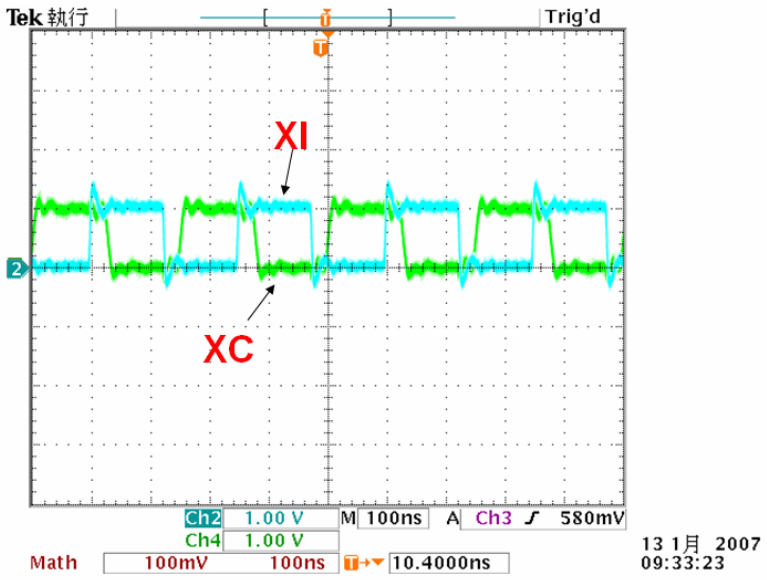


Fig. 4.17 The measurement results of the new proposed mixed-voltage crystal oscillator I in receiving mode with a 4-MHz 0/1-V external input clock signal.

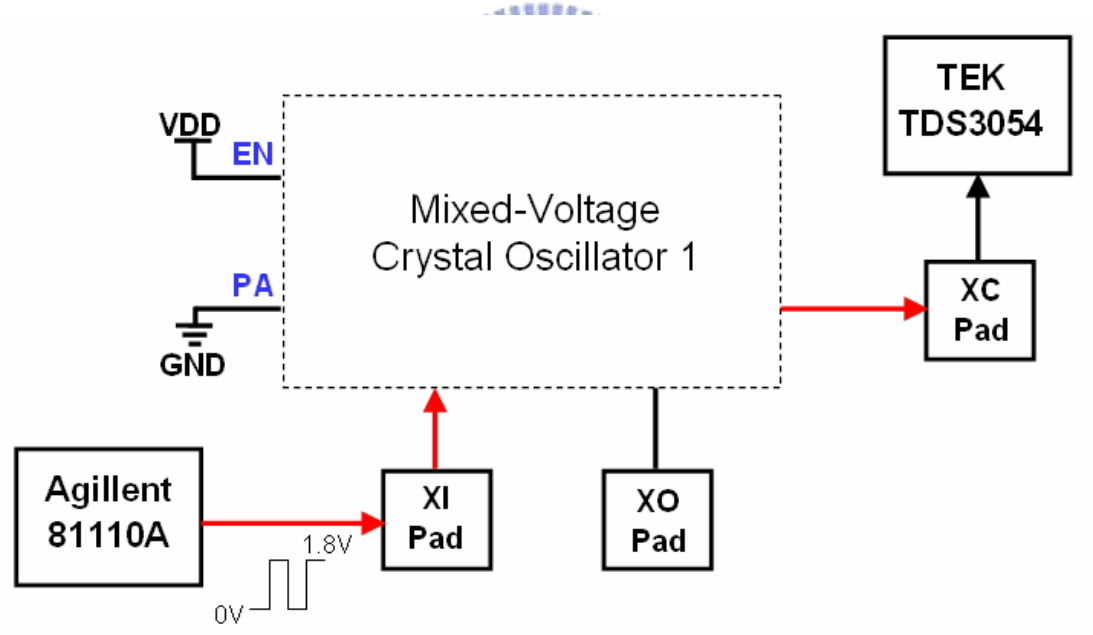


Fig. 4.18 The measurement setup for testing the new proposed mixed-voltage crystal oscillator I in receiving mode with a 4-MHz 0V/1.8-V external input clock signal.

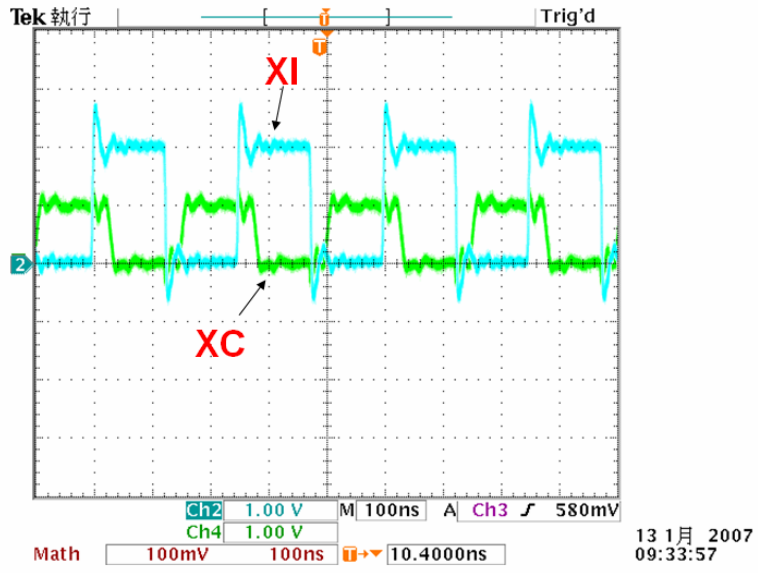


Fig. 4.19 The measurement results of the new proposed mixed-voltage crystal oscillator I in receiving mode with a 4-MHz 0/1.8V external input clock signal.

Chapter 5

New Proposed Mixed-Voltage Crystal Oscillator Circuit II

5.1 INTRODUCTION

In previous chapter, a new crystal oscillator circuit I was proposed. Although it can be operated successfully without gate-oxide reliability issue, it needs an extra control signal to select the oscillation mode or the receiving mode. In this chapter, a new mixed-voltage crystal oscillator circuit II using the gate tracking circuits and the floating n-well technique without an extra control signal is proposed. The new mixed-voltage crystal oscillator circuit II with low-voltage CMOS devices can not only solve the gate-oxide reliability issues but also oscillate completely with an external crystal unit. The new proposed mixed-voltage crystal oscillator circuit II has been designed and realized in UMC 130-nm 1.2-V CMOS process to server 1.2/2.5-V mixed-voltage interface applications and TSMC 90-nm 1-V CMOS process to server 1/1.8-V mixed-voltage interface applications.

5.2 CIRCUIT DESCRIPTION

Fig. 5.1 shows the new proposed mixed-voltage crystal oscillator circuit II realized with only the thin gate-oxide (1×VDD) devices. XI pad and XO pad are the input and output pads of the proposed mixed-voltage crystal oscillator circuit II, respectively. Signal EN is controlled by the internal circuits of IC. XC is the clock signal which is produced by crystal oscillator circuit or to receive the external clock

signal into the IC. The transistors MN2, MN3, MP2 and MP3 form the inverting amplifier of the proposed mixed-voltage crystal oscillator circuit II. Inverters INV4 and INV5 could transfer the sinusoidal-wave signal to a square signal or pass the external clock signal into the internal input node XC.

It is operated to generate the sinusoidal-wave signal at both XI pad and XO pad, when the proposed mixed-voltage crystal oscillator circuit II is with crystal and two load capacitances. Transistors MP4 and MP5 are turned off and transistor MN4 is turned on with the gate terminals connected to power supply (VDD). The sinusoidal-wave signal whose voltage level is less than VDD-Vt can pass through the transistor MN1 to the input terminal (N01) of the nand gate, and oscillation starts up. When the low voltage level is at the input terminal (N01) of the inverter INV1, the transistor MN5 is turned on to bias the gate terminal of the transistor MP1 at GND and the inverters INV2 and INV3 fix the voltage level, so that the sinusoidal-wave signal, even the voltage level is over VDD-Vt, can pass through the transistor MP1 to the input terminal (N01) of the nand gate. It means that the sinusoidal-wave signal could completely pass through the transistors MN1 and MP1 to the gate terminal of the nand gate without distortion. Transistor MP6 is turned on to bias the floating N-well (FNW) at VDD.

For the mixed-voltage interface applications, the proposed mixed-voltage crystal oscillator circuit II could be used to receive an external clock input signal whose voltage level could be 1×VDD or 2×VDD. In order to limit the voltage level of clock input signal reaching to the gate oxide of the nand gate, transistor MP4 is used to track the signal at the XI pad and control the gate voltage of transistor MP1. When the voltage level at the XI pad exceeds VDD+｜Vtp｜, such as 2×VDD, transistor MP4 is turned on to charge the gate terminal of transistor MP1 up to 2×VDD. Transistor MP1 is completely turned off to prevent the voltage level at the input terminal (N01)

of the nand gate from rising up to 2×VDD. Transistor MP5 is turned on and transistor MP6 is turned off to bias the floating N-well (FNW) at 2×VDD. Besides, when the voltage level of XI pad is at GND, the transistor MN5 will be turned on by inverter INV1 to turn on the transistor MP1. Transistor MP5 is turned off and transistor MP6 is turned on to bias the floating N-well (FNW) at VDD.

5.3 SIMULATION RESULTS

Fig. 5.2 shows the simulation waveform of the proposed mixed-voltage crystal oscillator circuit II in UMC 130-nm 1.2-V CMOS process to serve 1.2/2.5-V mixed-voltage interface. As shown in Fig. 5.2(b), with the 30-MHz external clock signal of 2×VDD into XI pad and 20-pF load capacitance in XC, the input terminal (N01) voltage of the nand gate can be limited and biased at the voltage level (1 V). The final signal voltage level reaching to the XC node is successfully shifted down to 1×VDD. The proposed mixed-voltage crystal oscillator circuit II can be operated correctly without the gate-oxide reliability issue. In Fig. 5.2(a), the proposed mixed-voltage crystal oscillator circuit II with the crystal of 30-MHz fundamental frequency and a load capacitance 20-pF at the pad can successfully generate the clock signal of 30-MHz at the XC node under the power supply of 1×VDD. As these simulations, the desired functions of this mixed-voltage crystal oscillator circuit II have been verified.

Fig. 5.3 shows the simulation waveform of the proposed mixed-voltage crystal oscillator circuit II in TSMC 90-nm 1-V CMOS process to serve 1/2-V mixed-voltage interface. As shown in Fig. 5.3(b), with the 30-MHz external clock signal of 2×VDD into XI pad and 20-pF load capacitance in XC, the input terminal (N01) voltage of the nand gate can be limited and biased at the voltage level (0.8V). The final signal

voltage level reaching to the XC node is successfully shifted down to 1×VDD. The proposed mixed-voltage crystal oscillator circuit II can be operated correctly without the gate-oxide reliability issue. In Fig. 5.3(a), the proposed mixed-voltage crystal oscillator circuit II with the crystal of 30-MHz fundamental frequency and a load capacitance 20-pF at the pad can successfully generate the clock signal of 30-MHz at the XC node under the power supply of 1×VDD. As these simulations, the desired functions of this mixed-voltage crystal oscillator circuit II have been verified.

5.4 EXPERIMENTAL RESULTS

Fig. 5.4 shows the layout view of the new proposed mixed-voltage crystal oscillator circuit II implemented in UMC 0.13-μm CMOS process. The cell size of XI, as well as XO, is only 183μm×60μm (including the bond pad), which is the same as that of digital or analog I/O cell in a standard I/O cell library. The feedback resistance Rf, implemented by the poly resistance, is also included into the layout. ESD protection is also provided by following the ESD design rules given by the foundry to draw the layout for NMOS and PMOS devices which are directly connected to the pads.

Fig. 5.5 shows the layout view of the new proposed mixed-voltage crystal oscillator circuit II implemented in TSMC 90-nm CMOS process. The cell size of XI, as well as XO, is only 190.5μm×60μm (including the bond pad), which is the same as that of digital or analog I/O cell in a standard I/O cell library. The feedback resistance Rf, implemented by the poly resistance, is also included into the layout. ESD protection is also provided by following the ESD design rules given by the foundry to draw the layout for NMOS and PMOS devices which are directly connected to the pads.

Fig. 5.6 is the die photo of the new proposed mixed-voltage crystal oscillator circuit II implemented in TSMC 90-nm CMOS process. To test the function of the new proposed mixed-voltage crystal oscillator circuit II in oscillation mode, the measurement setup is the same as Fig. 4.14 without the PA port for the external crystal of fundamental frequency 4-MHz and 20-MHz. Here, an external crystal is connected between the input pad (XI) and the output pad (XO) of the new proposed mixed-voltage crystal oscillator circuit II with two external capacitors respectively connected in the input pad (XI) and the output pad (XO). The control signal EN and PA are both at VDD. As the measurement results shown in Fig. 5.7, the new proposed mixed-voltage crystal oscillator circuit II can successfully oscillate and correctly generate the clock signals of frequency 4-MHz and 20-MHz at XC node, respectively.

To test the function of the new proposed mixed-voltage crystal oscillator circuit II in receiving mode, the measurement setup is the same as Fig. 4.16 without the PA port for a 0/1-V external clock signal of frequency 4-MHz at the input pad (XI). Here, the XI pad of the new proposed mixed-voltage crystal oscillator circuit II is used as the input pad to receive the external clock signal from the pulse generator and the external clock signal will be transmitted to the oscilloscope by the XC pad. The control signal EN is at VDD and PA is at GND. As the measurement results shown in Fig. 5.8, the new proposed mixed-voltage crystal oscillator circuit II can successfully transmit the 0/1-V clock signal of frequency 4-MHz to the XC node.

To test the function of the new proposed mixed-voltage crystal oscillator circuit II in receiving mode for a 0/1.8-V external clock signal of frequency 4-MHz at the input pad (XI), the measurement setup is the same as Fig. 4.18 without the PA port. Here, the XI pad of the new proposed mixed-voltage crystal oscillator circuit II is used as the input pad to receive the external clock signal from the pulse generator and the external clock signal will be transmitted to the oscilloscope by the XC pad. The

control signal EN is at VDD and PA is at GND. As the measurement results shown in Fig. 5.9, the new proposed mixed-voltage crystal oscillator circuit II can successfully transmit the 0/1.8-V clock signal of frequency 4-MHz to the XC node with the input clock signal shifted in 0/1-V. From the measurement results, the new proposed mixed-voltage crystal oscillator circuit II can be successfully operated in such a 1/1.8-V mixed-voltage I/O environment.

5.5 CONCLUSION

A new proposed mixed-voltage crystal oscillator circuit II has been successfully designed and implemented in both UMC 130-nm 1.2-V CMOS process and TSMC 90-nm 1-V CMOS process, which can be operated in the 1.2/2.5-V and 1/1.8-V signal environment without the gate-oxide reliability problem, respectively. But the fabrication of the new proposed crystal oscillator circuit II in UMC 130-nm 1.2-V CMOS process is still under going, so the measurements need to be followed. The new mixed-voltage crystal oscillator circuit II can be applied for external clock signal in the input pad (XI) without the gate-oxide reliability problems. The new mixed-voltage crystal oscillator circuit II realized with 1xVDD devices can be applied in 1xVDD/2xVDD mixed-voltage interface.

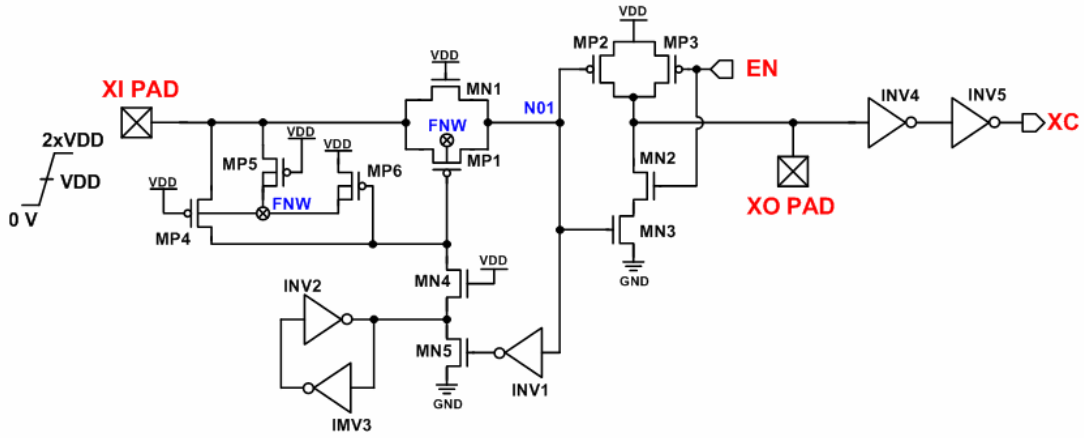
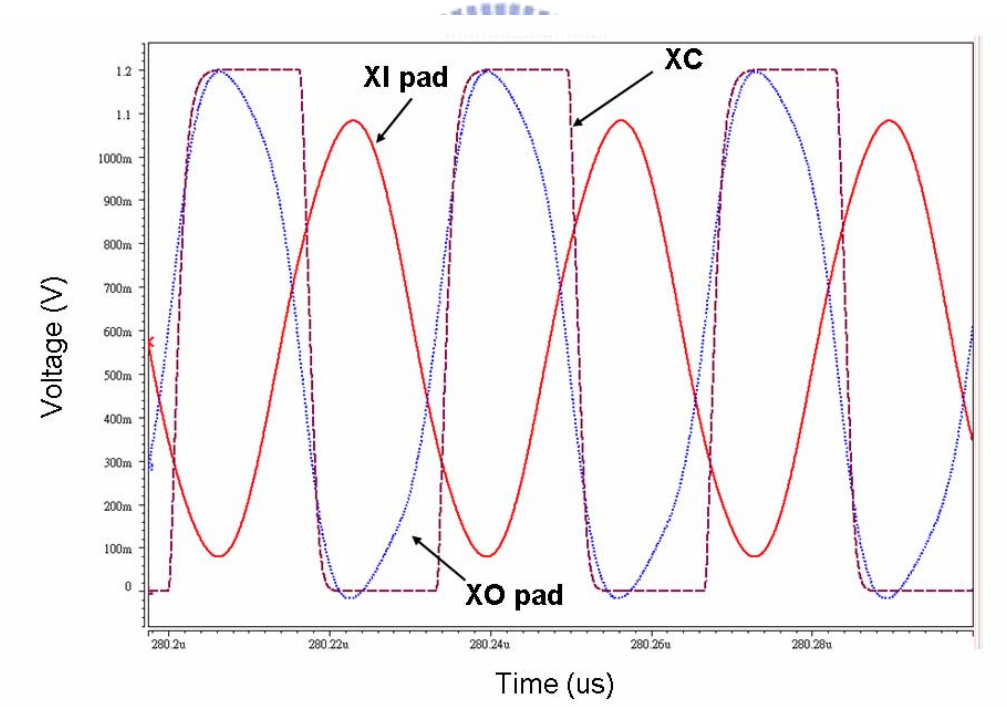
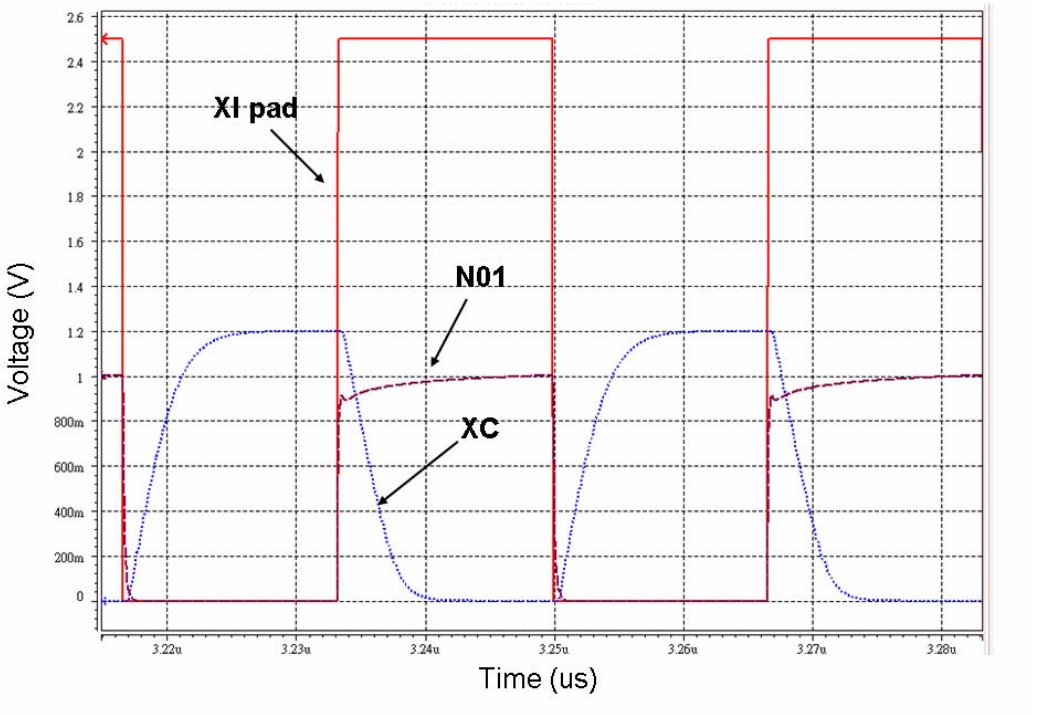


Fig. 5.1 The new proposed mixed-voltage crystal oscillator circuit II.



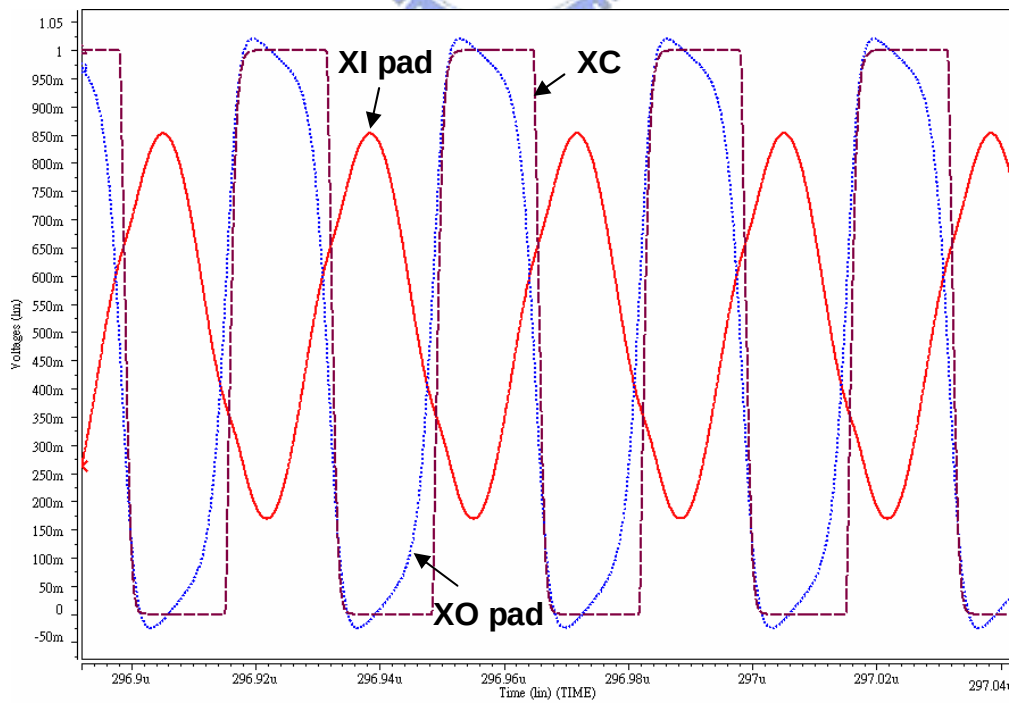
(a)

(Continued to the next page of Fig. 5.2)



(b)

Fig. 5.2 The simulated waveforms of the new proposed crystal oscillator circuit II with (a) a crystal of fundamental frequency 30-MHz and load capacitance 20-pF, and (b) 30-MHz external clock signal of 2×VDD into XI pad and 20-pF load capacitance in XC in UMC 130-nm 1.2-V CMOS process.



(a)

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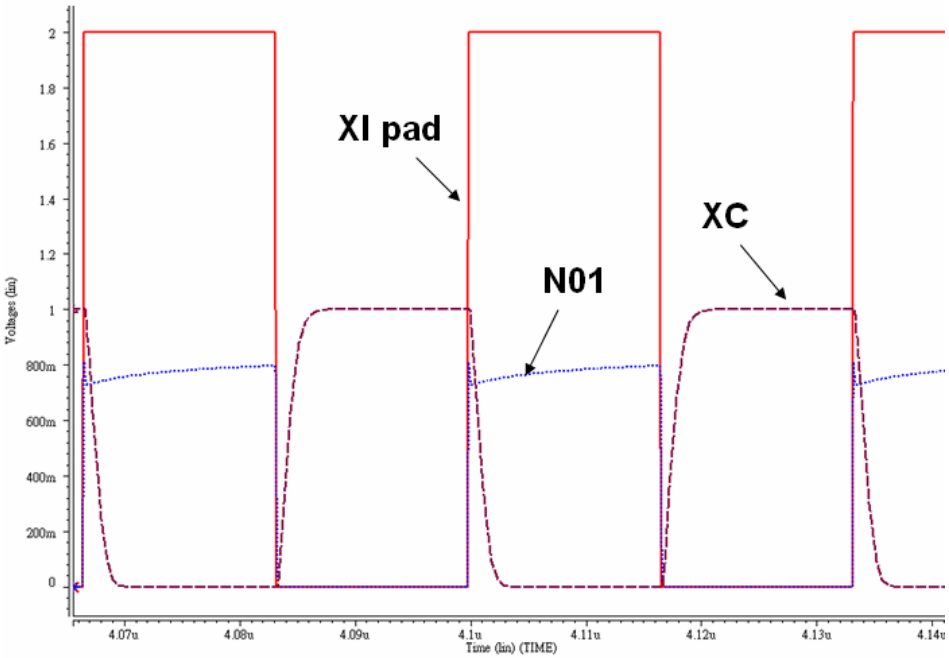


(b)

Fig. 5.3 The simulated waveforms of the new proposed crystal oscillator circuit II with (a) a crystal of fundamental frequency 30-MHz and load capacitance 20-pF, and (b) 30-MHz external clock signal of 2×VDD into XI pad and 20-pF load capacitance in XC in TSMC 90-nm 1-V CMOS process.

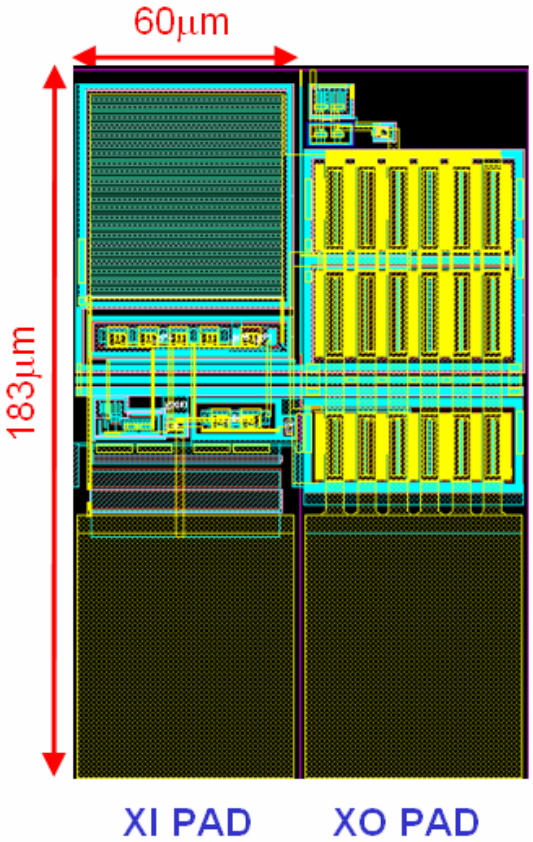


Fig. 5.4 The layout view of new proposed crystal oscillator circuit II realized in UMC 130-nm 1.2-V CMOS process.

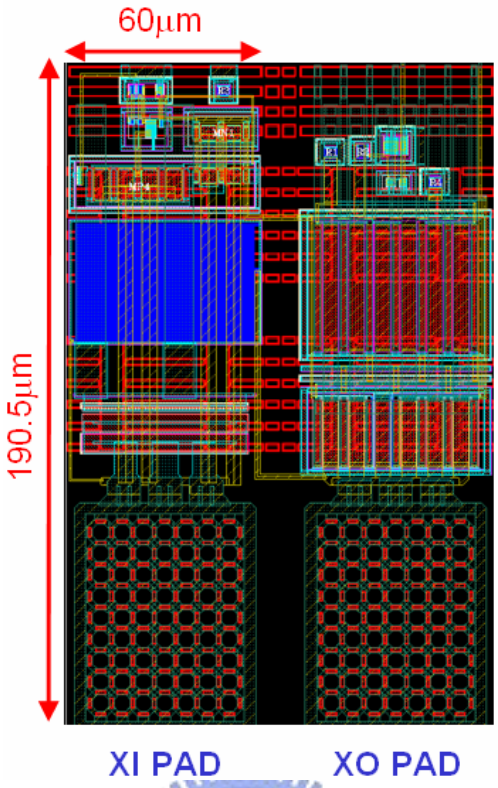


Fig. 5.5 The layout view of new proposed crystal oscillator circuit II realized in TSMC 90-nm 1-V CMOS process.

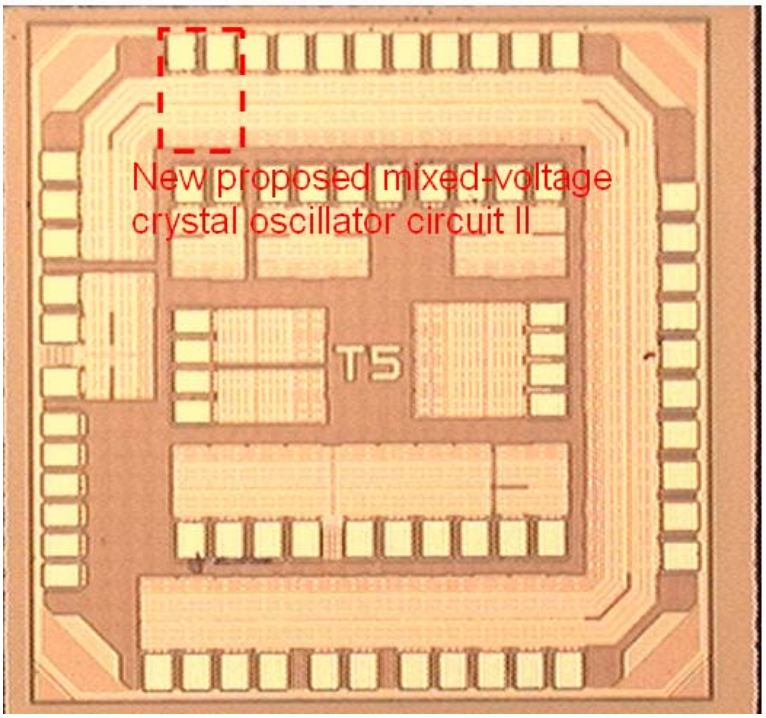
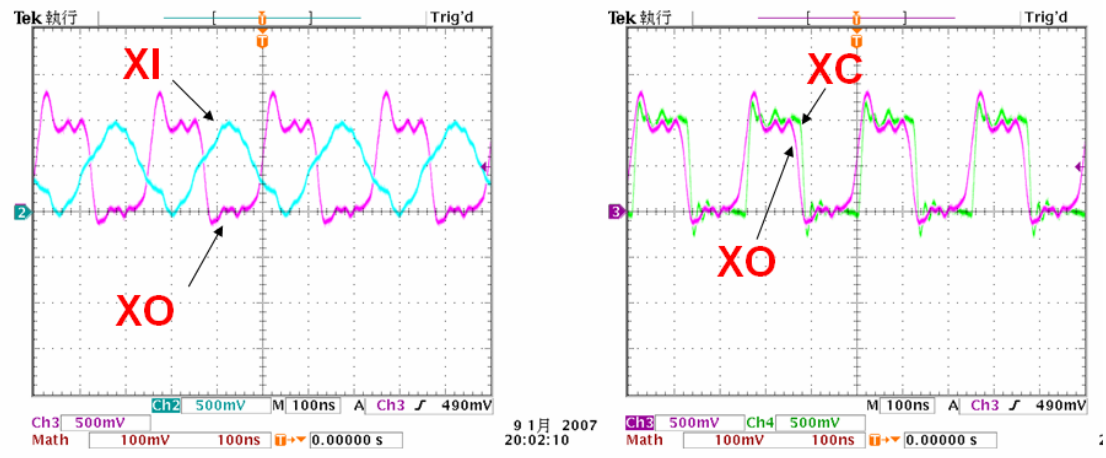
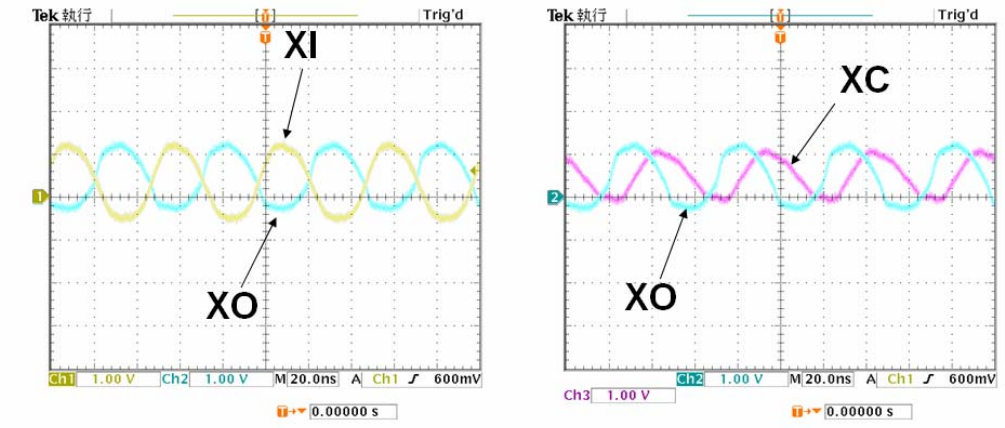


Fig. 5.6 The die photo of new proposed crystal oscillator circuit II realized in TSMC 90-nm 1-V CMOS process.



(a)



(b)

Fig. 5.7 The measurement results of the new proposed mixed-voltage crystal oscillator II in oscillation mode with a crystal of fundamental frequency (a)4-MHz and (b)20-MHz.

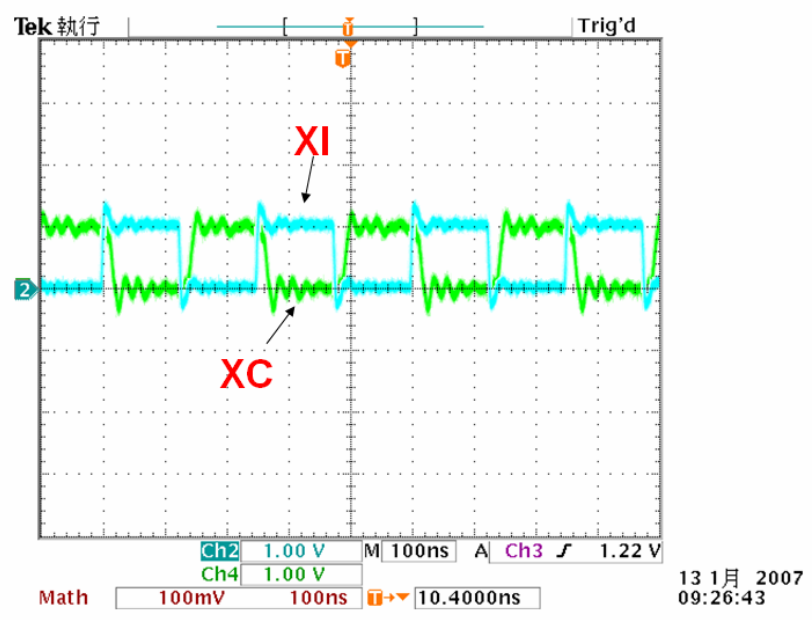


Fig. 5.8 The measurement results of the new proposed mixed-voltage crystal oscillator II in receiving mode with a 4-MHz 0/1-V external input clock signal.

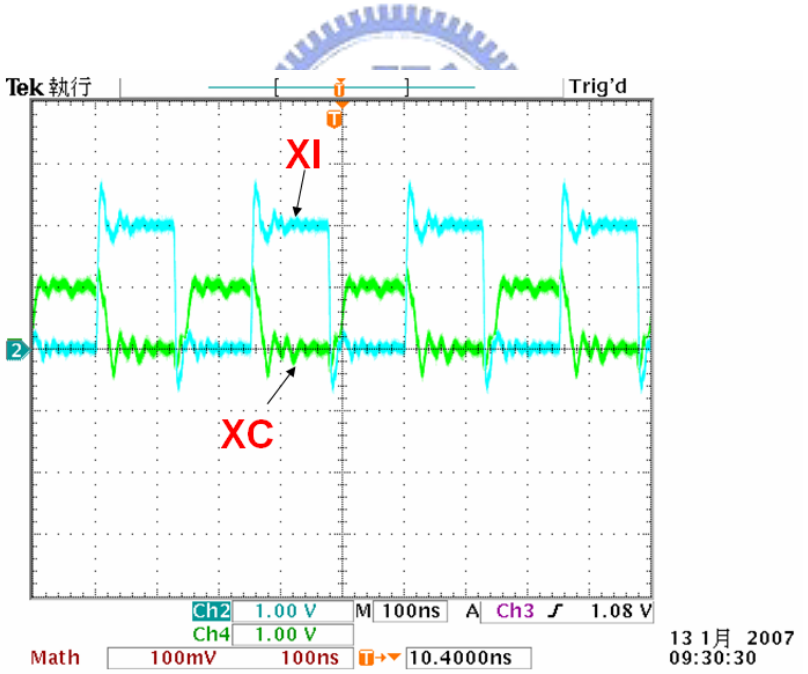


Fig. 5.9 The measurement results of the new proposed mixed-voltage crystal oscillator II in receiving mode with a 4-MHz 0/1.8-V external input clock signal.

Chapter 6

Summary and Future Works

6.1 SUMMARY

To connect circuits operated with different supply voltages, the design issues for mixed-voltage I/O interface and several kinks of prior mixed-voltage I/O interface circuit are introduced in chapter 2. Although the prior solutions can solve the problems in the mixed-voltage application, there are still some drawbacks in the prior mixed-voltage I/O interface circuits.

In the chapter 3, a mixed-voltage I/O buffer with gate-tracking circuit and dynamic N-well bias circuit by only using thin gate-oxide devices has been introduced and implemented in 130-nm CMOS process. The new mixed-voltage I/O buffer is simpler than the prior designs. And according to the measurement results, the new mixed-voltage I/O buffer with gate-tracking circuit and dynamic N-well bias circuit realized with only 1xVDD devices can be applied successfully for 1xVDD/2xVDD mixed-voltage interface.

In the chapter 4, a new proposed mixed-voltage crystal oscillator circuit I with a control signal has been successfully designed and implemented in both 130-nm 1.2-V CMOS process and 90-nm 1-V CMOS process, which can be operated in the 1.2/2.5-V and 1/1.8-V signal environment without the gate-oxide reliability problem, respectively. The new mixed-voltage crystal oscillator circuit I can receive the external clock signal in input pad (XI) without the gate-oxide reliability problem and also oscillates correctly at specified frequency with an external crystal. The new

mixed-voltage crystal oscillator circuit I realized with 1xVDD devices can be applied in 1xVDD/2xVDD mixed-voltage interface.

In the chapter 5, a new proposed mixed-voltage crystal oscillator circuit II with gate tracking circuit and floating N-well technique has been successfully designed and implemented in 130-nm 1.2-V CMOS process and 90-nm 1-V CMOS process, which can be operated in the 1.2/2.5-V and 1/1.8-V signal environment without the gate-oxide reliability problem, respectively. The new mixed-voltage crystal oscillator circuit II can be applied for external clock signal in input pad (XI) without the gate-oxide reliability problem and oscillates correctly with an external crystal for specified frequency. The new mixed-voltage crystal oscillator circuit II realized with 1xVDD devices can be applied in 1xVDD/2xVDD mixed-voltage interface.

6.2 FUTURE WORKS

Although the functions of the designed circuits in this thesis are all verified, there are still some subjects and drawbacks could be studied or improved. The first is the design of the two new proposed crystal oscillator circuits could be considered for the crystal operated in overtone region. The second is the new proposed crystal oscillator circuit II needs to be improved to avoid the huge device size of the transistor MP4 to effectively turn off the transistor MP1 in fig. 5.1. The third is the traditional electrostatic discharge (ESD) protection circuits are not suitable for the mixed-voltage applications. Therefore, new ESD protection circuits realized in low-voltage processes must be developed to achieve a good ESD robustness for the mixed-voltage applications. The fourth is the duty cycle of the generated clock signal by a crystal oscillator circuit will vary with process variation, so a simple duty cycle adjustment circuit [29] may need to be studied. Finally, the fabrication of new

proposed crystal oscillator circuit I and II in UMC 130-nm 1.2-V CMOS process is under going, the measurements need to be followed.

REFERENCES

[1] Semiconductor Industry Association (SIA), *International Technology Roadmap for Semiconductors (ITRS)*, 2006.

[2] J. Williams, "Mixing 3V and 5V ICs," *IEEE Spectrum*, pp. 40-42, 1993.

[3] A. J. Annema, G. Geelen, and P. C. de Jong, "5.5-V I/O in a 2.5-V 0.25-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 528-538, Mar. 2001.

[4] G. P. Singh and R. B. Salem, "High-voltage-tolerant I/O buffers with low-voltage CMOS process," *IEEE J. Solid-State Circuits*, vol. 34, no. 11, pp. 1512-1525, Nov. 1999.

[5] T. Furukawa, D. Turner, S. Mittl, M. Maloney, R. Serafin, W. Clark, L. Longenbach, and J. Howard, "Accelerated gate-oxide breakdown in mixed-voltage I/O buffers," in *Proc. IEEE Int. Reliability Physics Symp.*, 1997, pp. 169-173.

[6] E. Takeda and N. Suzuki, "An empirical model for device degradation due to hot-carrier injection," *IEEE Electron Device Lett.*, vol. 4, no. 4, pp. 111-113, April 1983.

[7] S. Voldman, "ESD protection in a mixed-voltage interface and multirail disconnected power grid environment in 0.5- and 0.25-μm channel length CMOS technologies," in *Proc. EOS/ESD Symp*, 1994, pp. 125-134.

[8] S. Dabral and T. Maloney, *Basic ESD and I/O Design*. New York: Wiley, 1998.

[9] G. W. Neudeck, *The PN Junction Diode*. Reading, MA: Addison- Wesley, 1989.

[10] K.-H. Lee, B. R. Jones, C. Burke, L. V. Tran, J. A. Shimer, and M.-L. Chen, "Lightly doped drain structure for advanced CMOS (Twin-Tub IV)," in *IEDM Tech. Dig.*, 1985, pp. 242−245.

[11] T.-Y. Huang, I-W. Wu, and J.-Y. Chen, "A MOS transistor with self-aligned polysilicon source-drain," *IEEE Electron Device Lett.*, vol. 7, no. 5, pp. 314-316, May 1986.

[12] M.-L. Chen, C.-W. Leung, W. T. Cochran, W. Hungling, C. Dziuba, and T. Yang, "Suppression of hot-carrier effects in submicrometer CMOS technology," *IEEE Trans. Electron Devices*, vol. 35, no. 12, pp. 2210-2220, Dec. 1988.

[13] I.-C. Chen, J.-Y. Choi, and C. Hu, "The effect of channel hot-carrier stressing on gate-oxide integrity in MOSFETs," *IEEE Trans. Electron Devices*, vol. 35,

no. 12, pp. 2253−2258, Dec. 1988.

[14] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, "Design on mixed-voltage I/O circuit with blocking NMOS and dynamic gate-controlled circuit for high-voltage-tolerant applications," *IEEE Int. Symp. on Circuits and Systems*, 2005, pp. 1859-1862.

[15] R. S. Scott, N. A. Dumin, T. W. Hughes, D. J. Dumin, and B. T. Moore, "Properties of high-voltage stress generated traps in thin silicon oxide," *IEEE Trans. Electron Devices*, vol. 43, no. 7, pp. 1133-1143, July 1996.

[16] K. bult, "Analog broadband communication circuit in pure digital deep sub-micron CMOS," in *ISSCC Dig. Tech. Papers*, pp. 76-77, 1999

[17] S. Poon, C. Atwell, C. Hart, D. Kolar, C. Lage, and B. Yeargain, "A Versatile 0.25-micron CMOS technology," in *IEDM. Tech. Dig.*, 1998, pp. 751-754

[18] M. Takahashi, T. Sakurai, K. Sawada, K. Nogami, M. Ichida, and K. Matsuda, "3.3V-5V compatible I/O circuit without thick gate oxide," in *Proc. of IEEE Custom Integrated Circuits Conference*, 1992, pp. 23.3.1-23.3.4.

[19] M. J. M. Pelgrom and E. C. Dijkmans, "A 3/5-V compatible I/O buffer", *IEEE J. Solid-State Circuits*, vol. 30, no. 7, pp. 823-825, July 1995.

[20] C.-H. Chuang and M.-D. Ker, "Design on mixed-voltage-tolerant I/O interface with novel tracking circuits in a 0.13-μm CMOS technology." *IEEE Int. Symp. on Circuits and Systems*, 2004, pp .577-580.

[21] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, "Overview and design of mixed-voltage I/O buffers with low-voltage thin-oxide CMOS transistors," *IEEE Trans. on Circuits and Systems I: Regular Paper,* vol. 53, no. 9, pp. 1934-1945, Sep. 2006.

[22] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, "Design of charge pump circuit with consideration of gate-oxide reliability in low-voltage CMOS processes," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1100-1107, May 2006.

[23] M.-D. Ker, C.-Y. Chang, and H.-C. Jiang, "Design of negative charge pump circuit with polysilicon diodes in a 0.25-μm CMOS process," in *Proc. IEEE Asia-Pacific Conf. Advanced System Integrated Circuits*, 2002, pp. 145-148.

[24] H.-C. Chow, "Bidirectional buffer for mixed-voltage applications," in *Proc. IEEE Int. Symp. Circuits Syst.*, 1999, pp. 270-273.

[25] R. D. Adams, R. C. Flaker, K. S. Gray, and H. L. Kalter, "CMOS off-chip driver circuit," U.S. Patent 4782250, Nov. 1, 1988.

[26] D.-Y. Chen, "Design of a mixed 3.3 V and 5 V PCI I/O buffer," in *Proc. IEEE Int. ASIC Conf.*, 1996, pp. 336-339.

[27] M. Shinji and K. Mitsuharu, "Complementary MOS transistor crystal oscillator

circuit," US Patent 3,935,546, Dec. 12, 1973.

[28] H. Eiichi and O. Haruhiko, "Crystal oscillator circuit with crystal reducing resistance and integrated circuit therefor," US Patent 5,635,860, Jan. 8, 1998.

[29] W. M. Lin and H. Y. Huang, "A low-jitter mutual-correlated pulsewidth control loop circuit," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1366-1369, Aug. 2004.

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Publication List

[1] Ming-Dou Ker and Hung-Tai Liao “Mixed-voltage crystal oscillator circuit with low-voltage devices,” pending for U.S.A. and R.O.C. Patents.

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[4] Ming-Dou Ker and Hung-Tai Liao “Design of mixed-voltage-tolerant crystal oscillator circuit in low-voltage CMOS technology,” submitted to *IEEE Trans. on Circuits and Systems II*.