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博 士 論 文

低溫複晶矽薄膜電晶體之氟鈍化製程與可靠度的研究

Study on Fluorine Passivation Techniques and the Reliability for Low Temperature Polycrystalline Silicon Thin-Film Transistors

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中華民國 九十四 年 九 月

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摘　　要

此論文提出多種氟鈍化(passivatation)技術以製作高效能且高可靠度的複晶矽薄膜電晶體(poly-Si TFTs)。此外，我們亦研究在電壓應力(electrical stress)測試下，複晶矽薄膜電晶體之開啟電流(On-current)及關閉電流(Off-current)的不穩定性。最後，我們利用高解析度的掃描式電容顯微鏡(scanning capacitance microscopy, SCM)系統開發出一種探測氧化層崩潰(oxide breakdown)點的技術。

首先，我們提出與現有製程具高度匹配性的四氟化碳電漿處理(CF_4 plasma treatment)技術，用以製作高效能的固態結晶(solid-phase-crystallized)之複晶矽薄膜電晶體。利用此技術，氟原子可以有效地被導入複晶矽薄膜中以消除薄膜中的載子補獲態(trap states)，進而有效地提升元件特性。經由四氟化碳電漿處理的複晶矽薄膜電晶體具有好的臨限擺幅(subthreshold swing)、低的臨界電壓(threshold voltage)及高的元件開關電流比(On/Off current ratio)；其載子電致遷移率(field-effect mobility)也提升了 22.8 %。此外，四氟化碳電漿處理也提升元件的抗熱載子(hot-carrier)破壞的能力。之後，我們在將此技術搭配準分子雷射退火(exciner laser annealing)，應用於製作高性能的雷射處理之複晶矽薄膜電晶體

(ELA poly-Si TFTs)。實驗結果證明氟電漿處理能有效地鈍化複晶矽中及氧化層與複晶矽界面上的缺陷。因此，元件的特性可獲得大幅的提升。最重要的是因為矽-氟的高強度鍵結能，經過熱載子應力(hot carrier stress)測試後，發現摻入氟原子的複晶矽薄膜電晶體具有較好的可靠度。另外，我們亦提出一種利用氟矽玻璃(fluorinated silicate oxide, FSG)當緩衝層的複晶矽薄膜電晶體製程。利用此方法亦可有效的鈍化複晶矽缺陷，進而大幅改善元件特性、均勻性及可靠度。其中，氟在氟矽玻璃中最佳的含量大約介於 2% 到 4% 間。

接著，本論文探討複晶矽薄膜電晶體在不同電壓應力測試下的開啟電流(On-current)及關閉電流(Off-current)的不穩定性。利用施加不同的閘極及汲極電壓來研究應力測試下所產生的元件劣化情形。經由結果我們歸納出，氧化層的捕獲電荷(trap charges)及複晶矽通道中的載子補獲態(trap states)之數量與空間分佈是造成開啟電流(On-current)及關閉電流(Off-current)的變化的最主要因素。我們利用此技術完成一個完整的模型以解釋複晶矽薄膜電晶體的開啟電流及關閉電流之不穩定性的原因。

在論文的最後，我們開發出一種利用掃描式電容顯微鏡(scanning capacitance microscopy, SCM)搭配原子力顯微鏡(atomic force microscopy, AFM)的探針掃描技術以研究氧化層的崩潰(oxide breakdown)現象。此技術可以清楚地掃描出氧化層崩潰點(breakdown spots) 的局部分佈。這些崩潰點因為具高度導通性(conductivity)因而顯示出非常低的微分電容值(dC/dV)訊號。由結果顯示出，氧化層的崩潰點的直徑大概為 6 奈米(nm)到 13.5 奈米之間。此外，根據原子力顯微鏡的結果，我們亦發現氧化層的崩潰現象並不會造成其表面平坦度的改變。

Study on Fluorine Passivation Techniques and the Reliability for Low Temperature Polycrystalline Silicon Thin-Film Transistors

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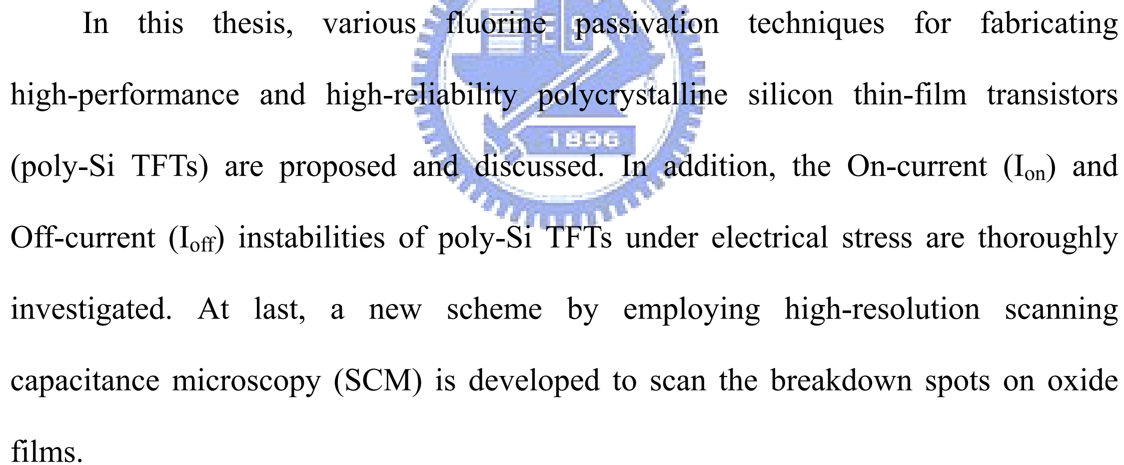
ABSTRACT



In this thesis, various fluorine passivation techniques for fabricating high-performance and high-reliability polycrystalline silicon thin-film transistors (poly-Si TFTs) are proposed and discussed. In addition, the On-current (I_{on}) and Off-current (I_{off}) instabilities of poly-Si TFTs under electrical stress are thoroughly investigated. At last, a new scheme by employing high-resolution scanning capacitance microscopy (SCM) is developed to scan the breakdown spots on oxide films.

First, a process-compatible CF_4 plasma treatment for fabricating high-performance solid-phase-crystallized (SPC) poly-Si TFTs is demonstrated. Using this technique, fluorine atoms can be introduced into poly-Si films to passivate trap states, and hence the performance of SPC poly-Si TFTs can be significantly improved. The fluorinated SPC poly-Si TFTs exhibit good subthreshold slope, low threshold voltage, and better On/Off current ratio. The fluorinated poly-Si TFT also shows approximately 22.8 % enhancement in the maximum field-effect mobility. Moreover,

the CF_4 plasma treatment also promotes the device's hot-carrier immunity. Then, CF_4 plasma treatment combined with excimer laser annealing (ELA) is proposed to fabricate high-performance ELA poly-Si TFTs. Fluorine can effectively passivate the trap states near the SiO_2/poly-Si interface. With fluorine incorporation, the electrical characteristics of ELA poly-Si TFTs are significantly improved. The CF_4 plasma treatment also improves the device reliability of ELA poly-Si TFTs with respect to hot-carrier stress, which is due to the formation of strong Si-F bonds. Another fluorine passivation technique is also proposed by adopting fluorinated silicate oxide (FSG) as a buffer layer. Experimental results reveal that the device performance, uniformity and reliability can be remarkably improved with appropriate fluorine content (2% to 4%) in the FSG layer.

Then, the On-current (I_{on}) and Off-current (I_{off}) instabilities of poly-Si TFTs are thoroughly investigated under various electrical stress conditions. The stress-induced device degradation is studied by measuring the dependences of I_{on} and I_{off} on the applied drain/gate voltages. From the results, dissimilar variations of I_{on} and I_{off} can be observed, which is attributed to the variances in the amount of trap charges in the gate oxide and the spatial distributions of trap states generated in the poly-Si channel. A comprehensive model for the degradation of I_{on} and I_{off} in poly-Si TFTs under various electrical stress conditions is proposed.

Finally, scanning capacitance microscopy (SCM), combined with atomic force microscopy (AFM), is employed to investigate the dielectric breakdown phenomena in SiO_2 films. The localized breakdown spots can be clearly imaged by this technique. The breakdown spots exhibit signals with low differential capacitance (*dC/dV*) due to high conductivity. The diameters of these breakdown spots are from 6 nm to 13.5 nm. Moreover, according to the corresponding AFM images, their surface morphology shows little change after the occurrence of oxide breakdown.

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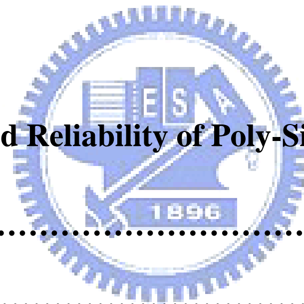

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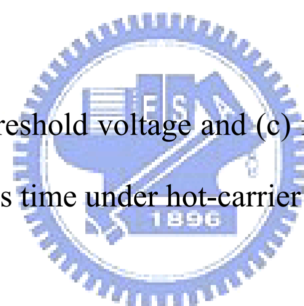

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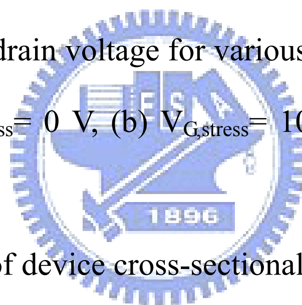

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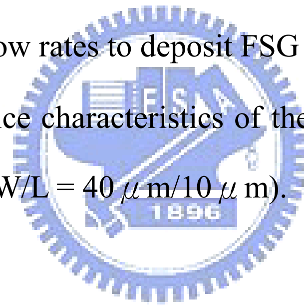

Chapter 1

Introduction

1.1 Overview of Poly-Si Thin-Film Transistors

Thin-film transistors (TFTs) have been widely used in static random access memories (SRAMs) [1], electrical erasable programming read only memories (EEPROMs) [2], linear image sensors [3], thermal printer heads [4], photodetector amplifier [5], scanner [6], and active matrix liquid crystal displays (AMLCDs) [7]-[9]. Over the past decade, the thriving growth of the flat-penal-displays (FPDs) industry has become the main driving force in the development of the TFTs technology. Currently, AMLCD is believed to be the most promising candidate to realize large-area FPDs with high resolution. Conventionally, amorphous silicon (a-Si) TFTs are used for the pixel switching elements. However, due to their low electron mobility ($\leq$1 cm^2/Vs), it is hard to realize the integration of the switching pixels with the peripheral driver circuits in one signal substrate to further reduce the production cost of AMLCDs. In 1966, the first polycrystalline silicon thin film transistors (Poly-Si TFTs) were fabricated by C. H. Fa *et al.* [10]. In comparison with a-Si TFTs, poly-Si TFTs have a superior carrier mobility, higher CMOS capability, and better reliability [11]-[27].

The high driving current of poly-Si TFTs makes the integration of switching pixels and driver circuits possible [11]. Moreover, the aperture ratio and the panel brightness can be also greatly promoted due to small device size needed using poly-Si TFTs [12]. Therefore, the performance of display can be significantly improved. As a

result, poly-Si TFTs have a great potential to realize high-performance large-area AMLCDs applications, and further to accomplish System-on-Panel (SOP).

Process temperature is one of the most important concerns to fabricate poly-Si TFTs on inexpensive, low-melting point and large-area glass substrates. Many crystallization techniques have been proposed to achieve low temperature polycrystalline silicon (LTPS) TFTs (≤ 620℃), such as solid phase crystallization (SPC) [13]-[16], laser annealing crystallization [17]-[21], metal induced crystallization (MIC) [22]-[24], and metal-induced lateral crystallization (MILC)[25]-[27]. In such low temperatures, the quality of poly-Si films plays a critical role in the device performance and reliability. Among these techniques, excimer laser annealing (ELA) is believed to become the mainstream technology for mass production because high-quality poly-Si films can be obtained.

Compared to single crystal silicon, poly-Si is rich in grain boundary defects and intra-grain defects, resulting in numerous trap states. Trap states in the TFT's channel can trap carriers to generate barriers for carrier transport when TFT is turned on, lowering the device's diving current [28]. As the device is off, large trap states enhance the traps-assisted tunneling near the drain, causing a large leakage-current [29]. That is to say, the electrical properties of poly-Si TFT's is strongly related to the amount of defects. Two methods have been developed to reduce the defect density. One is enlarging the poly-Si grain size [30], [31]. This can reduce the number of grain boundaries within the channel and therefore improve the device performance. The other is plasma treatments. Radicals existed in plasmas can terminate defects in the poly-Si, and thus reduce the trap state density. Recently, various plasmas such as H_2 [32], NH_3 [33], N_2O [34] and O_2 plasmas [35] have been intensely investigated to accomplish this goal.

Moreover, novel structure design is another approach to fabricate

high-performance poly-Si TFTs. This technique focuses on the reduction of the electric field near the drain junction, and thus suppresses the device's Off-state leakage current. Many structures including multiple channel structures [36], offset drain/source [37], [38], lightly doped drain (LDD) [39], gate-overlapped LDD [40]-[42], field induced drain [43] and vertical channel [44] have been proposed and investigated intensively.

1.2 Motivation

In the poly-Si TFT's channel, trap states, resulted from grain boundary and intra-grain defects, can trap carriers to form potential barriers, and thus affect the current transport [28]. Moreover, the Off-current in poly-Si TFTs is associated with the amount of trap states in the drain depletion region. The generation of it can be attributed to thermionic emission at a low electric field and the field-enhanced emission (*i.e.* F-P emission or trap-assisted band-to-band tunneling) at a high electric filed [29]. Hence, trap states can lead to a poor device performance, such as low field-effect mobility, large leakage current, bad subthreshold slope and high threshold voltage.

Plasma treatments are believed to be the most effective methods to reduce trap states in the poly-Si. Many kinds of plasma such as H_2/N_2 mixture plasma [45], nitrogen implantation with H_2 plasma [33], pre-oxidation NH_3 annealing with H_2 plasma [33], NH_3 plasma [46] and H_2/O_2 plasma [47] have been proposed. Generally, hydrogen-based plasmas are mostly adopted, because the hydrogen atoms can easily restore the trap states at the poly-Si/SiO_2 interface and in the grain boundaries. However, it is known that hydrogenated poly-Si TFTs have a troublesome issue in the device reliability [48], [49]. The device performance degrades seriously under a

long-term electrical stress. It is known that the poor device reliability of the hydrogenated TFTs is due to the weak Si-H bonds, which might be broken easily during the electrical stress and thus cause the creation of trap states in the poly-Si channel [50]. Recently, fluorination technique has been proposed. It can improve both the device performance and also reliability, because the Si-F bonds are rather strong than Si-H bonds [51]-[56]. In conventional, fluorine ion implantation (FII) technique is mostly adopted to introduce fluorine atoms into the poly-Si. However, this method may be not suitable for large-area electronics. Moreover, a subsequent high temperature process, required to activate implanted fluorine atoms and recover the damage created by implantation, is also not compatible with the current AMLCD fabrication processes. Therefore, effective and process-compatible techniques to introduce fluorine atoms into the poly-Si channel are needed to be developed. In Chapters 2, 3 and 4, new process-compatible fluorination techniques are demonstrated and investigated.

Moreover, it is known that studying the instabilities of the device characteristics in poly-Si TFTs is more complicated than doing so in the case of single-crystal MOSFETs, which is due to the random distribution of grain boundaries and the poor quality of the gate oxide. From the previous reports in studying single-crystal MOSFETs, we believe that the amounts and the spatial distributions of the trap states (or charges) in the gate oxide and in the poly-Si play important roles in the instabilities of poly-Si TFTs. On-current (I_{on}) and Off-current (I_{off}) are two of the most important parameters in designing poly-Si TFT circuits, related to the driving capacity and the charge storage, which are very sensitive to the oxide trap charges and trap states in the poly-Si. Their instabilities, particularly with regard to the electrical stress, have constrained poly-Si TFTs applications. Although several groups have studied the variations in the device characteristics of poly-Si TFTs at the On-state or Off-state

after the electrical stress separately [49], [57], [58], a comprehensive mechanism for the degradation of both I_{on} and I_{off} under various stress conditions is not yet well known. In Chapter 5, a new strategy for studying the mechanism of the I_{on} and I_{off} instabilities in poly-Si is adopted.

In addition, due to the continuous scaling down of metal-oxide-semiconductor field-effect transistors (MOSFETs), the quality of the thin gate oxide has become more and more important. Oxide breakdown (OBD) is one of the most critical concerns for integrated circuit device reliability [59], [60]. The OBD process is thought to be a local phenomenon within the nano-scale region, not occurring throughout the total oxide area [61], [62]. However, conventional electrical measurements, made through MOS capacitors, only detect general information about the whole oxide area under the electrode, and the localized OBD behavior is missed. To characterize the localized OBD evens in detail, highly sensitive measurement tools with a good spatial resolution are necessary. Scanning capacitance microscopy (SCM), combined with atomic force microscopy (AFM), has been used to study local charge trapping in gate oxides and dynamic device operation images [63], [64], which is a powerful technique to synchronously measure the differential capacitance (*dC/dV*) images and the corresponding topographic images of thin films. Thus, in Chapter 6, we demonstrate a new technique for mapping oxide breakdown spots by adopting SCM with corresponding AFM images.

1.3 Thesis Organization

This thesis is organized as follow:

In Chapter 1, the overview of poly-Si TFTs and motivations of this thesis are described.

In Chapter 2, a novel fluorine-based plasma treatment, CF_4 plasma treatment, is employed to treat the solid-phase-crystallized (SPC) poly-Si TFT. The electrical characteristics and reliability of the CF_4 plasma-treated poly-Si TFTs are explored. The fluorine passivation effect on SPC ploy-Si TFTs using CF_4 plasma is investigated.

In Chapter 3, CF_4 plasma treatment, combined with excimer laser annealing (ELA), is proposed to fabricate CF_4 plasma-treated ELA poly-Si TFTs. The electrical characteristics as well as the device reliability of the ELA poly-Si TFTs are greatly improved. The mechanisms responsible to the device improvements are comprehensively discussed.

In Chapter 4, fabricating poly-Si TFTs on an FSG buffer layer is proposed and demonstrated. Experimental results reveal that remarkably improved device performance and uniformity can be achieved with appropriate fluorine incorporation in the poly-Si. Furthermore, the fluorine also increases the poly-Si TFTs reliability against hot carrier stressing, which is attributed to the formation of Si-F bonds. However, too much fluorine incorporation causes an unwanted degradation phenomenon. The relation between the device characteristics and the amount of fluorine incorporated is analyzed.

In Chapter 5, the I_{on} and I_{off} instabilities of poly-Si TFTs are investigated under various electrical stress conditions. The stress-induced device degradation is studied by measuring the dependences of I_{on} and I_{off} on the drain/gate voltages. From the experimental results, dissimilar variations in I_{on} and I_{off} are observed, which can be attributed to the variances in the amount of trap charges in the gate oxide and the spatial distributions of the trap states generated in the poly-Si channel. A comprehensive model for the degradation of I_{on} and I_{off} in poly-Si TFTs under various stress conditions is presented.

In Chapter 6, scanning capacitance microscopy (SCM), combined with atomic

force microscopy (AFM), is employed to investigate the dielectric breakdown phenomena in thin SiO_2 films. The localized breakdown spots can be clearly imaged by SCM. Moreover, these breakdown spots are carefully analyzed, which exhibit signals with low differential capacitance (*dC/dV*) signals.

In Chapter 7, conclusions of this thesis and recommendations for further research are given.

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Chapter 2

CF_4 Plasma Treatment on Solid-Phase-Crystallized (SPC) Poly-Si TFTs

2.1 Introduction

In comparison with conventional a-Si TFTs, poly-Si TFTs have many advantages including high driving current, superior carrier mobility and great CMOS capability, which make the integration of switching-pixels and their peripheral driver circuits on a single glass substrate possible. It is known that trap states in the poly-Si can degrade the carrier transport and also increase the device leakage current [1], [2]. To eliminate these trap states has become the main topic for the current and future production of high performance poly-Si TFTs. Conventionally, hydrogen-based plasma treatment is the most popular method to passivate trap states in the current production [3], [4]. Although hydrogenation can eliminate the intra-grain and grain boundary trap states in the poly-Si film, the hydrogenated poly-Si TFTs suffer from a serious reliability issue, which can be attributed to the weak Si-H bonds.

Recently, several studies have demonstrated the use of fluorine (F) atoms to passivate the poly-Si films, which can improve both the performance and reliability of poly-Si TFTs, particularly when devices are under long-term electrical stress tests [5]-[9]. It is known that fluorine atoms can terminate dangling bonds and replace weak bonds in the grain boundaries and SiO_2/poly-Si interface and thus reduce the trap states in the poly-Si channel. In addition, the strong Si-F bonds, more stable than Si-H bonds, can greatly improve the device reliability under an electrical stress.

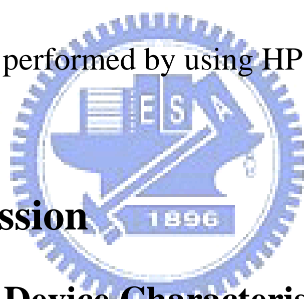
Fluorine ion implantation (FII), the most adoptive fluorinating technique, has been widely investigated [5]-[8]. It is worth noting that ion implantation technique is not suitable for large-sized glass substrate. Moreover, a subsequent high temperature annealing to recover the defects created by FII is required in this method, which is not compatible with current production. Therefore, C. H. Kim *et al.* demonstrated the use of fluorinated oxide (SiO_xF_y) to replace FII, which can be served as a diffusion source [9]. However, this technique increases manufacturing processes since extra film deposition and etching are required.

To date, although the effects of fluorination have been clarified, there is still a lack of a process-compatible technique to effectively introduce fluorine atoms into poly-Si films. In this chapter, we proposed a new fluorine passivation technique by employing CF_4 plasma treatment, which is a simply and efficient process. To avoid an unwanted etching effect, we controlled the RF to apply a very low power (5 Watts) to dissociate fluorine atoms, which were used to fluorinate the poly-Si film. Using this technique, the fluorinated poly-Si TFTs have been fabricated and the device characteristics and reliability were investigated.

2.2 Experimental

The schematic diagram of the fabrication process is illustrated in Fig. 2.1. First, a 100-nm-thick amorphous-silicon layer was deposited on thermally oxidized Si wafer by dissociation of SiH_4 gas in a low-pressure chemical vapor deposition (LPCVD) at 550°C. Subsequently, solid phase crystallization (SPC) was performed at 600°C for 24 hours in N_2 ambient for the phase transformation. Individual active regions were then patterned and defined. After a standard RCA cleaning, samples were subjected to the CF_4 plasma treatment, conducted in a plasma-enhanced chemical vapor deposition

(PECVD) system at 350°C for 15 seconds, with a pressure of 200 mTorr and a power of 5 Watts. Then, a 50-nm-thick tetraethyl orthosilicate (TEOS) oxide was deposited to serve as the gate insulator and a 200-nm-thick poly-Si film was deposited and patterned for the gate electrode. A self-aligned phosphorous ion implantation was preformed with the dosage and energy of 5×10^{15} cm^{-2} and 40 KeV, respectively. The dopant activation was performed at 600°C furnace annealing at N_2 ambient for 24 hours, followed by a deposition of the passivation layer and a definition of contact holes. Finally, a 500-nm-thick Al electrode was deposited and patterned. The control samples were prepared without the fluorinating process. To concentrate on revealing the fluorine passivation effects of the CF_4 plasma treatment, none of additional hydrogenation process was performed on the control samples. The electrical and reliability characteristics were performed by using HP 4156B.



2.3 Results and Discussion

2.3.1 Comparison of Device Characteristics

Figure 2.2(a) shows the transfer characteristics (I_D-V_{GS}) for the control and fluorinated poly-Si TFTs. The measurements were performed at two different drain voltages of V_{DS} = 0.1 V and 5 V. The parameters of the devices, including the threshold voltage (V_{th}) and subthreshold swing (S.S.), maximum On-current (I_{on}) and the minimum Off-current (I_{off}) were measured at V_{DS} = 5 V. The threshold voltage is defined as the gate voltage required to achieve a normalized drain current of I_D = (W/L) ×100 nA. Accordingly, the performance of the fluorinated poly-Si TFT is significantly improved. The V_{th} and *S.S.* of the fluorinated poly-Si TFT were found to be 8.3 V and 1.73 V/dec., which are superior to those of the control one (12 V and 2.06 V/dec., respectively). It's known that the V_{th} and S.S. are strongly influenced by

the deep trap states, associated with dangling bonds in the channel, which have energy states near the middle of the silicon band gap. Therefore, one can infer that CF_4 plasma treatment can terminate the dangling bonds in the poly-Si and SiO_2/poly-Si interface. Additionally, the I_{on} and On/Off current ratio of the fluorinated TFT are also better than those of the control TFT.

The minimum Off-current of the fluorinated device is nearly unsuppressed, which is consistent with the previous reports by Chern *et al.* [6] and Kim *et al.* [9] However, while the applied gate voltage was toward more negative (V_{GS} < -2 V), the fluorinated poly-Si TFT shows smaller leakage current compared with that of the control TFT. It is known that under a high electric field leakage current of the poly-Si TFT mainly comes from the trap-assisted band to band tunneling near the drain edge [10]. This observation suggests that there must be fewer trap states existed in the fluorinated poly-Si TFT, and thus the leakage current under a high electric field is reduced.

Figure 2.2(b) shows field-effect mobility versus the gate voltage of control and fluorinated poly-Si TFTs. The field-effect mobility was calculated from the value of transconductance at V_{DS} = 0.1V. The fluorinated poly-Si TFT shows approximately 22.8 % enhancement in the maximum field-effect mobility. Note that the field-effect mobility is significantly affected by the tail states near the band edge, which is resulted from the strain bonds in poly-Si and SiO_2/poly-Si interface [1]. These results imply that the CF_4 plasma treatment may not only terminate the dangling bonds, but also relieve the strain bonds. The extracted device parameters are listed in Table 2.1.

2.3.2 Extraction of Trap State Density

The grain boundary trap state densities (Q_T) of the conventional and fluorinated poly-Si TFTs were estimated by Levison and Proano method [11], [12]. Figure 2.3

exhibits the plots of the $\ln[I_D/(V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ curves at low V_{DS} and high V_{GS}. The Q_T was extracted from the slopes of these curves. The fluorinated poly-Si TFT exhibits a Q_T of 1.32×10^{13} cm^{-2}, whereas the control TFT has 1.67×10^{13} cm^{-2}. This result implies that the CF_4 plasma treatment can terminate the grain boundary trap states in the poly-Si film. To further study the fluorine passivation effect near the interface, the effective interface trap states densities (N_T) near the SiO_2/poly-Si interface were also calculated. From the S.S., by neglecting the depletion capacitance, the N_t can be expressed as [13]:

$$N_T = [(S.S./\ln 10)(q / kT)-1)](C_{ox}/q) \qquad (1)$$

where the C_{ox} is the capacitance of the gate oxide. The N_T of the control TFT and the fluorinated TFT are 1.45×10^{13} cm^{-2} and 1.21×10^{13} cm^{-2}, respectively. The N_T values reflect trap states near the SiO_2/poly-Si interface.

Figure 2.4 shows the SIMS (secondary ion mass spectroscopy) profiles of the control and fluorinated poly-Si films. The SIMS profiles exhibit that substantial amount of fluorine were introduced into the poly-Si layer by CF_4 plasma treatment, not carbon atoms. The SIMS analysis also shows a notably high concentration of fluorine atoms piling up near the SiO_2/poly-Si interface, instead of in the deep ploy-Si layer. These piled-up fluorine atoms is believed that they can provide more effective passivation of trap states, because the quality of SiO_2/poly-Si interface are the main issue for carrier transport.

Therefore, these results figure that trap states in both grain boundaries and the SiO_2/poly-Si interface were reduced by using CF_4 plasma treatment, which resulting the great improvement in the device performance. Based on these results, a schematic cross section view of the SiO_2/poly-Si interface is illustrated in Fig. 2.5. It is suggested that strong Si-F bonds replace the dangling and strain bonds for the fluorinated poly-Si films, and thus improve the device performance.

2.3.3 Output Characteristics and Activation Energy

Figure 2.6 shows the output characteristics (I_D-V_{DS}) of the fluorinated and control poly-Si TFTs. As can be seen, the driving current increases significantly for the fluorinated poly-Si TFT compared with that of the control TFT. This is due to the higher mobility and smaller threshold voltage of the fluorinated poly-Si TFT. The driving current increased 130%, 84% and 55% at V_{DS}= 20 V with V_{GS}= 10 V, 15 V and 25 V, respectively.

Figure 2.7 exhibits the activation energy (E_a) versus the gate voltage for the control and fluorinated poly-Si TFTs at V_{DS} = 1 V. In Off-region (low V_{GS}), the value of E_a reflects the required energy for carriers to leak by means of traps, whereas in On-region (high V_{GS}), the value of E_a reflects the carrier transport barrier caused by the trap states within the poly-Si channel [14]. Compared with the control TFT, the extracted E_a of the fluorinated poly-Si TFT decreases in On-region and increases in Off-region. That is to say, for fluorinated poly-Si TFT, fluorine atoms can passivate the trap states and hence reduce the barrier height for carrier transport when device is turned on. On the other hand, in Off-region fewer trap states after fluorinating process resulting in the increasing of E_a and thus the trap-assisted leakage current is suppressed. Moreover, in the subthreshold region, a steeper profile can be found for the fluorinated TFT, which proves that the interface quality of the fluorinated TFT is much better than that of the control TFT.

2.3.4 Device Reliability

Additionally, the hot carrier stress was carried out to examine the reliability of the device. The device degradation under hot carrier stress can be attributed to two mechanisms: oxide trap charges and the creation of trap states in the poly-Si. This can be attributed to channel-hot-electron (CHE) and self-heating (SH) phenomenon. For

CHE, electrons were injected and trapped in the gate oxide; then, the carrier flow in the channel is disturbed, therefore reducing the Ion. SH-induced damage is due to the large Joule heat, resulted from a high drain current [15], [16]. Because TFTs are fabricated on a poor thermal-conducting substrate, devices can reach a very high temperature during operation. Such high temperature enhances bonds breaking to generate trap states in the poly-Si, and thus degrade the TFT performance.

Figure 2.8 shows the variation of On-current under a hot carrier stress. The stress condition is performed at V_{DS}=30V and V_{GS}=30V for 4500 s. The variation in I_{on} is defined as $(I_{on,stressed}-I_{on,initial})/\ I_{on,initial}\times100\%$, where the $I_{on,initial}$ and $I_{on,stressed}$ are the measured I_{on} prior to and after the electrical stress. As can be seen, the fluorination process can greatly alleviate the On-current degradation under a hot carrier stress. We deduce that the the interface quality is greatly improved because of the fluorine incorporation after CF_4 plasma treatment,. The improved interface can result in a great enhancement of gate oxide integrity [17]. Moreover, Si-F bonds are form to replace weak bonds in the poly-Si, and therefore the bonds breaking can be eliminated. Hence, damage caused by channel-hot-electron and self-heating was suppressed for the fluorinated sample. As a result, device reliability was great improved for the fluorinated poly-Si TFT.

2.4 Summary

A new fluorinating technique of SPC poly-Si TFTs by employing CF_4 plasma treatment is demonstrated. Using this technique, significant improvements in the performance of fluorinated poly-Si TFTs have been presented. A steeper *S.S.*, smaller V_{th} and better ON/OFF current ratio can be obtained. Moreover, the fluorinated poly-Si TFT shows approximately 22.8 % enhancement in the maximum field-effect

mobility. These results can be attributed to the reduction of the trap states in the poly-Si and the SiO_2/poly-Si interface. Moreover, the CF_4 fluorinating process also improves the hot-carrier immunity. It is concluded that CF_4 plasma treatment can provide a simple, effective and process-compatible method to introduce fluorine atoms into poly-Si film to fabricate high-performance and high-reliability poly-Si TFTs.

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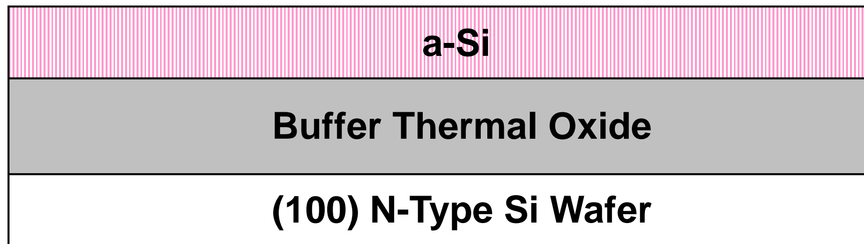
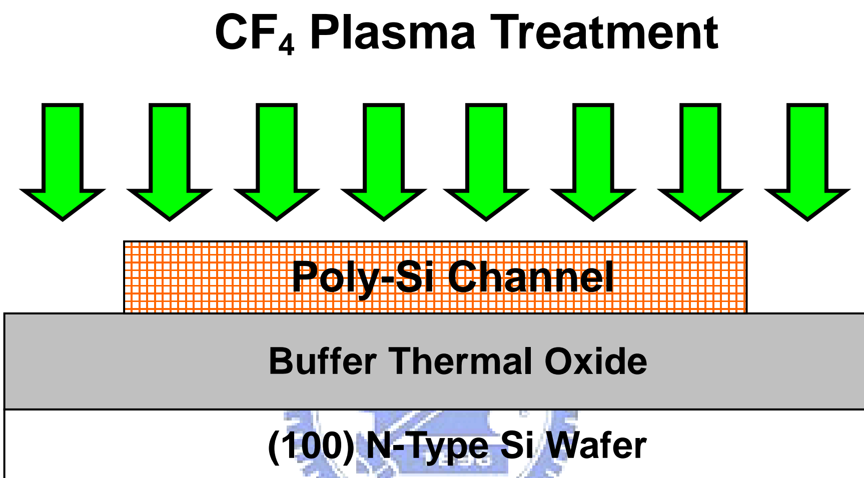
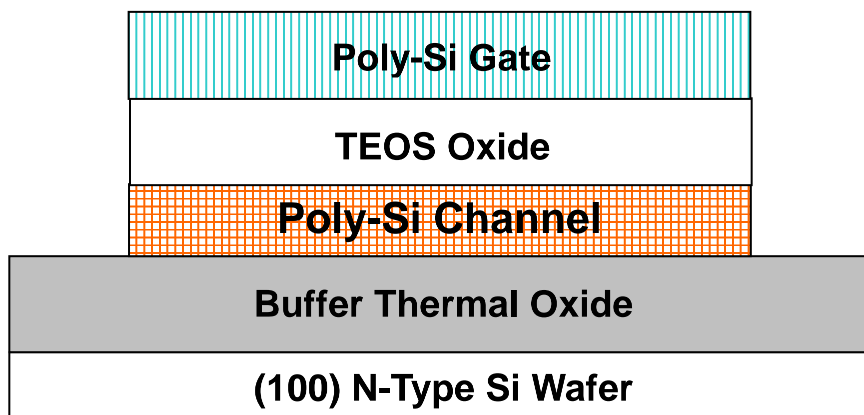


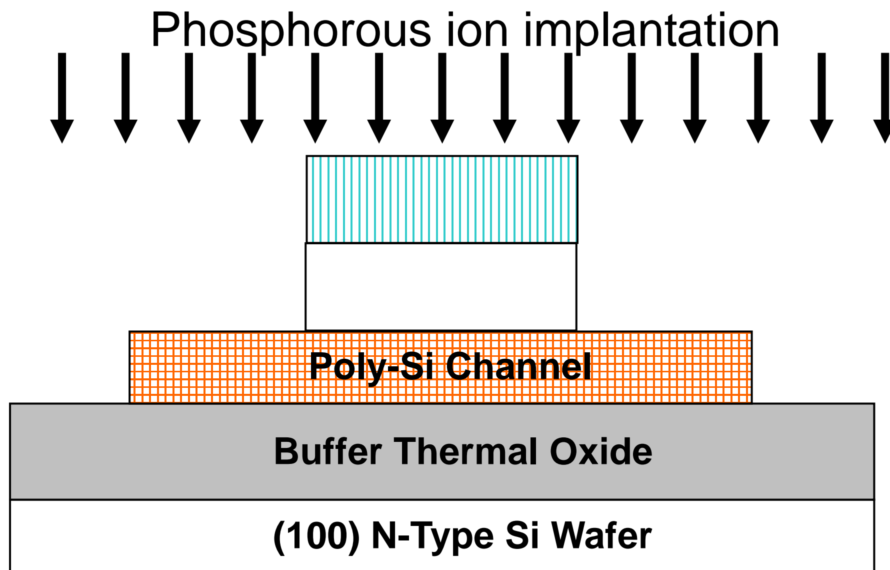
(a) Thermal oxidation, depositing amorphous-silicon.



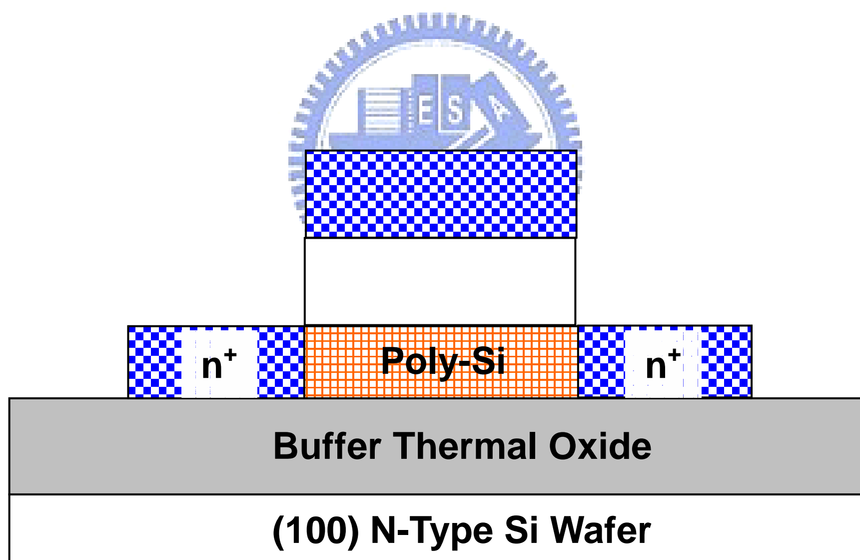
(b) Recrystallization by SPC, defining active region and CF_4 plasma treatment.



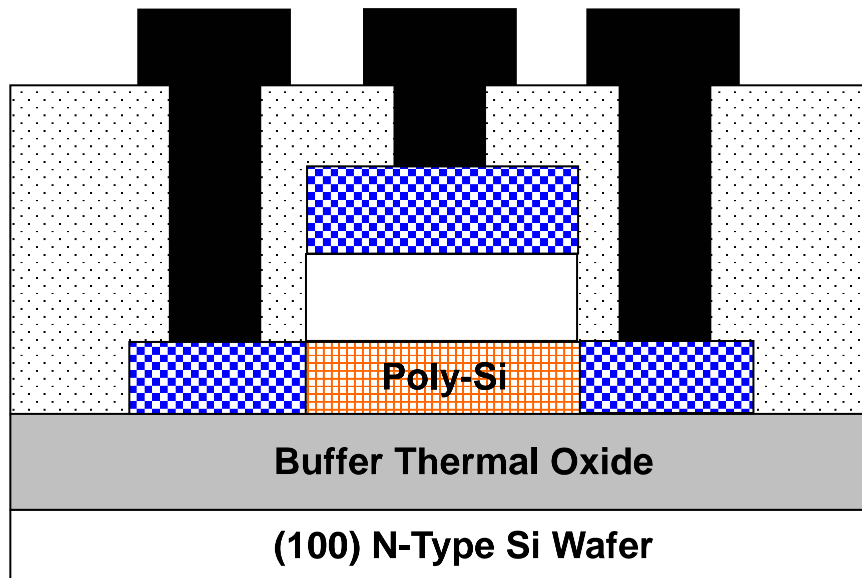
(c) Deposition of TEOS gate oxide by PECVD and poly-Si gate by LPCVD.



(d) Defining the gate electrode and self-aligned S/D implantation.



(e) Dopant activation by furnace annealing.



(f) Depositing passivation oxide, opening contact holes and patterning metal pads.

Fig. 2.1 Schematic diagram of fabrication process for SPC poly-Si TFTs with CF_4 plasma treatment.

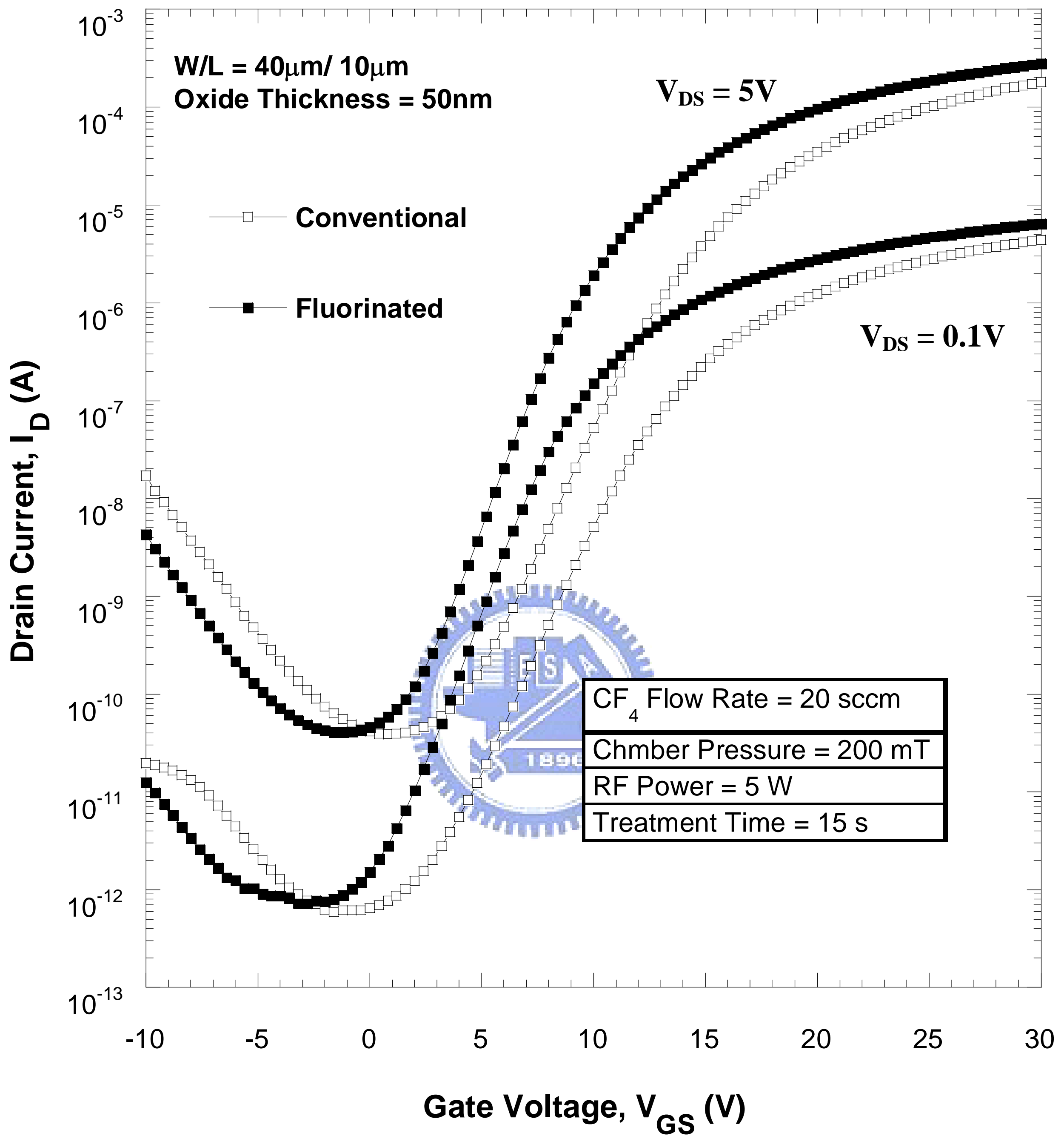


Fig. 2.2(a) Transfer characteristics of the control and fluorinated SPC poly-Si TFTs with V_{DS}=0.1V and 5V.

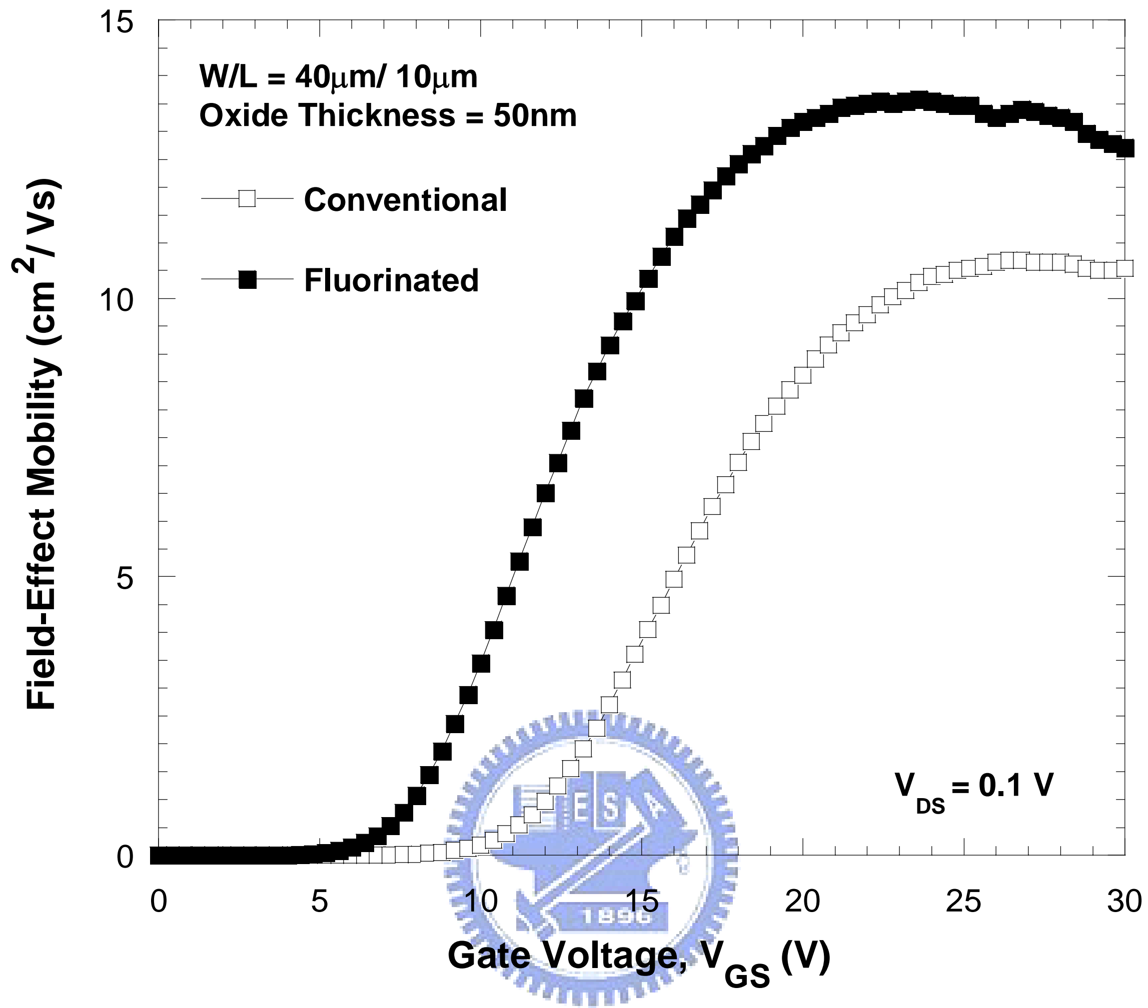


Fig. 2.2(b) Field-effect mobility of the control and fluorinated SPC poly-Si TFTs with V_{DS}=0.1V.

Table 2.1 Comparison of device characteristics of the control and fluorinated SPC poly-Si TFTs.

SPC Poly-Si TFTs	***Conventional***	***Fluorinated***
V_{th} (V)	12	8.3
S.S.(V/dec.)	2.06	1.73
μ_{eff} (cm^2/V.s)	10.5	13.6
I_{on} (μA)	180	279
I_{off} (pA)	38.7	40.7
On/Off Ratio (10^6)	4.65	6.85
Q_T (10^{13} cm^{-2})	1.67	1.32
N_T (10^{13} cm^{-2})	1.45	1.21

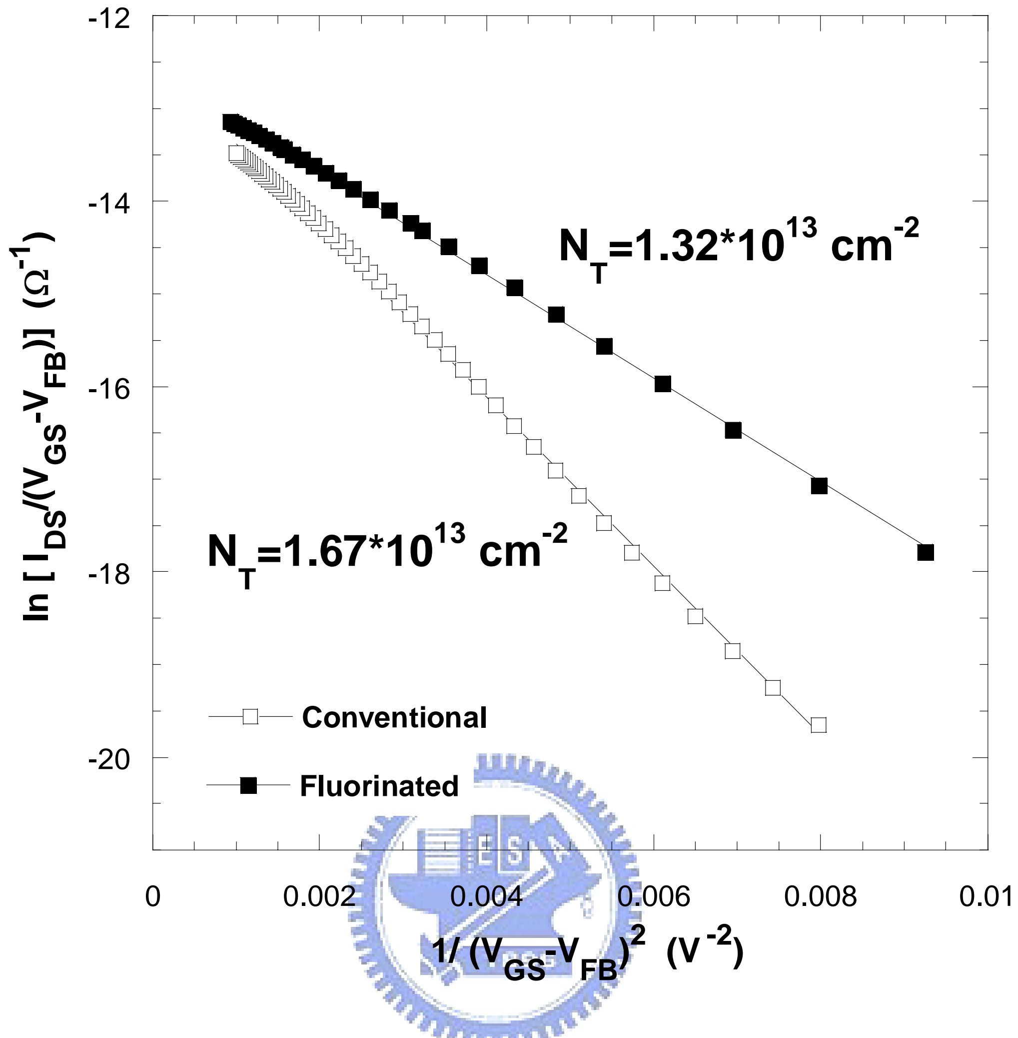
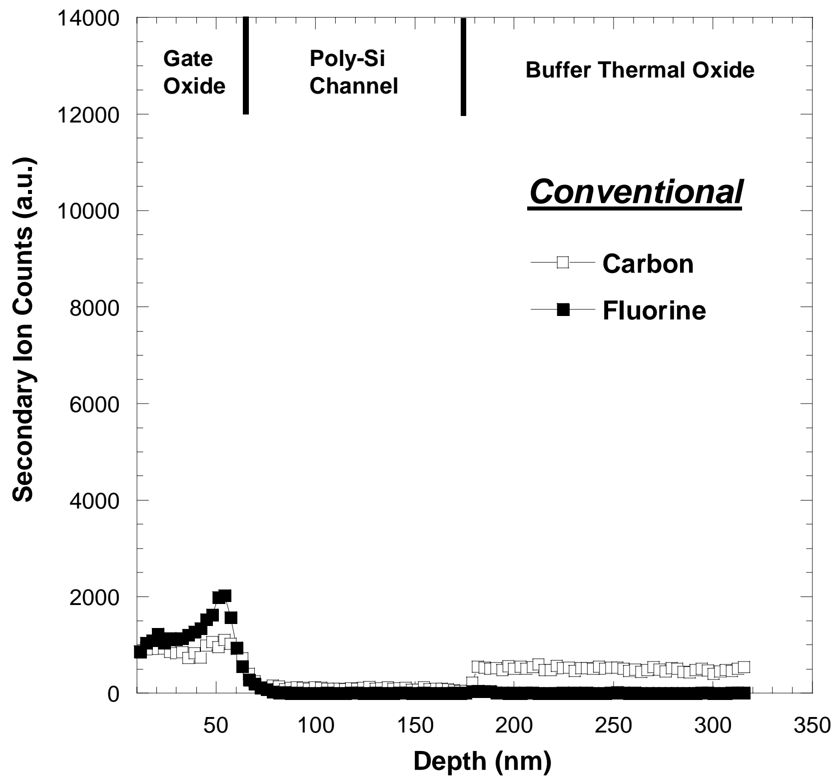
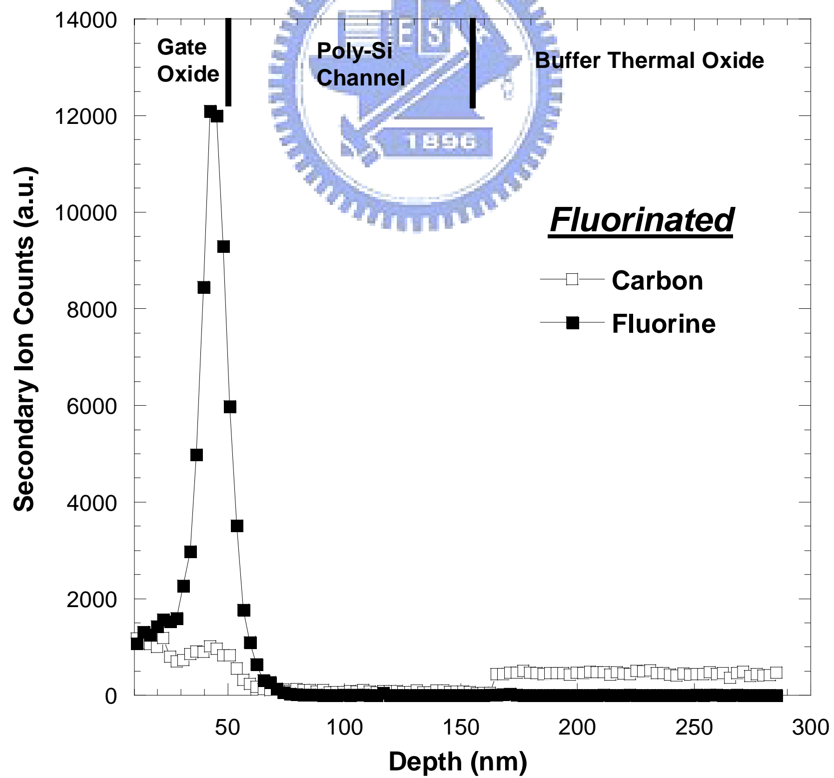


Fig. 2.3 ln[I_D/(V_{GS}-V_{FB})] versus 1/(V_{GS}-V_{FB})^2 curves at V_{DS} = 0.1V and high V_{GS} for control and fluorinated SPC poly-Si TFTs.

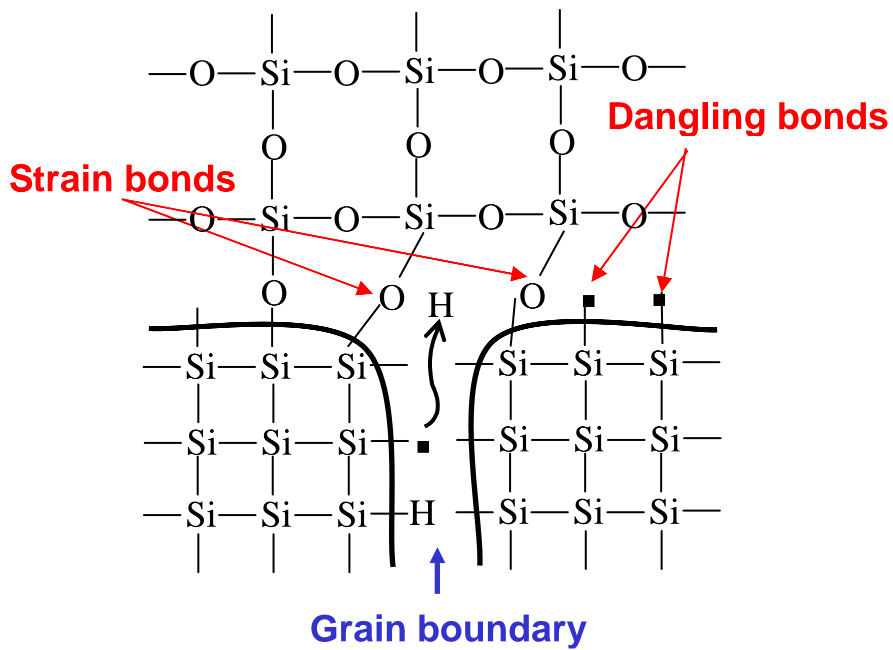


(a) Conventional poly-Si

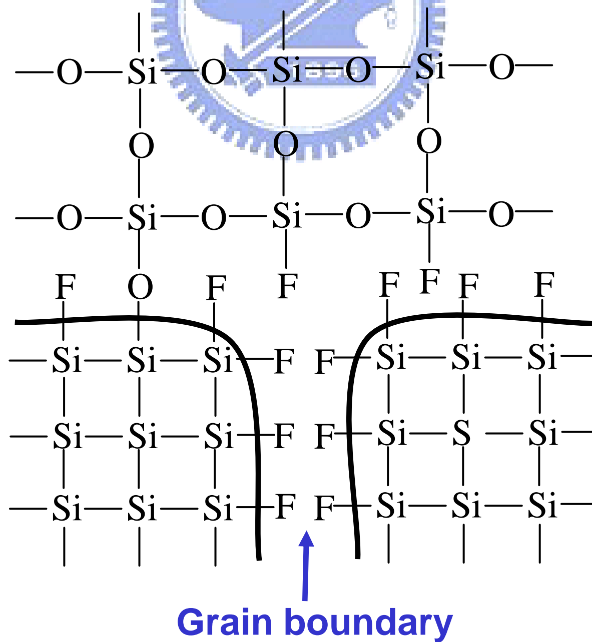


(b) Fluorinated poly-Si

Fig. 2.4 SIMS analyses of (a) control and (b) fluorinated SPC poly-Si films.



(a) Without CF_4 plasma



(b) With CF_4 plasma

Fig. 2.5 Schematic cross-sectional view of SiO_2/poly-Si interface (a) without CF_4 plasma and (b) with CF_4 plasma treatment.

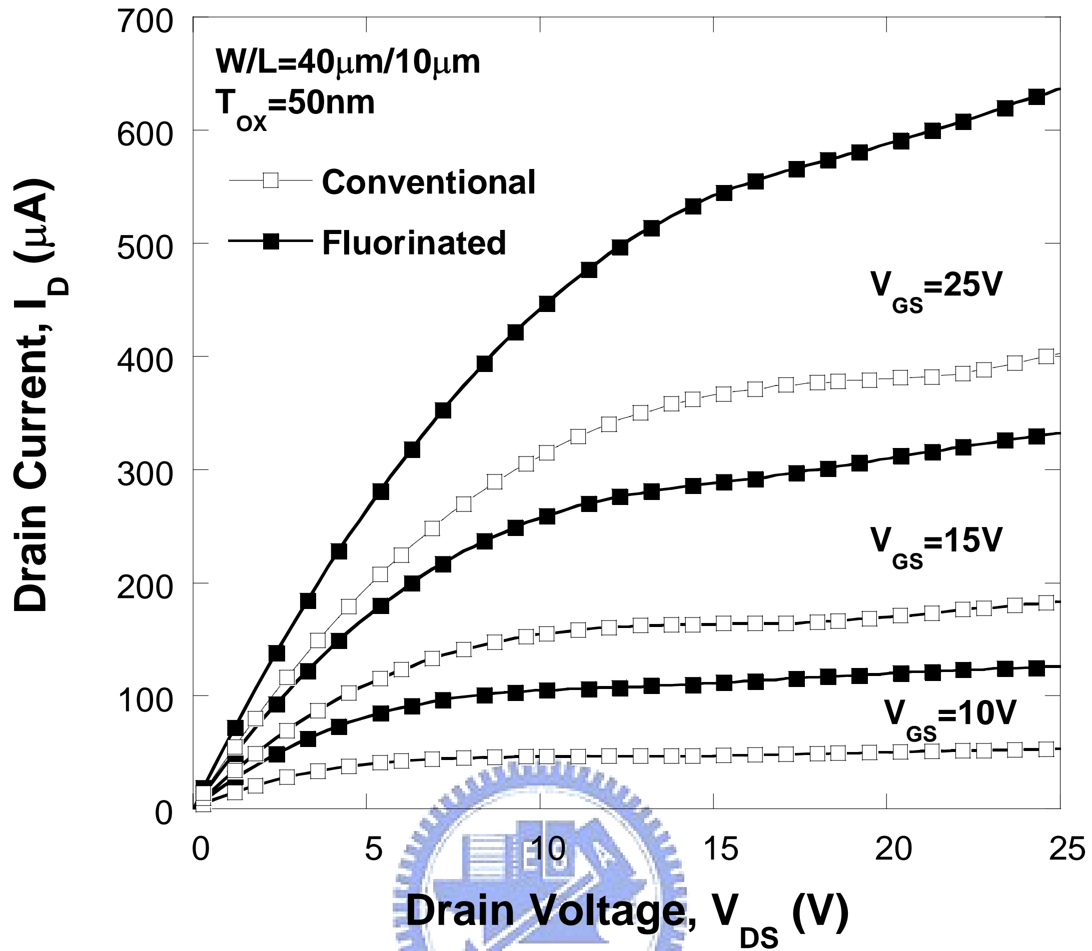


Fig. 2.6 Output characteristics of the control and fluorinated SPC poly-Si TFTs with V_{GS}= 10V, 15V and 25V.

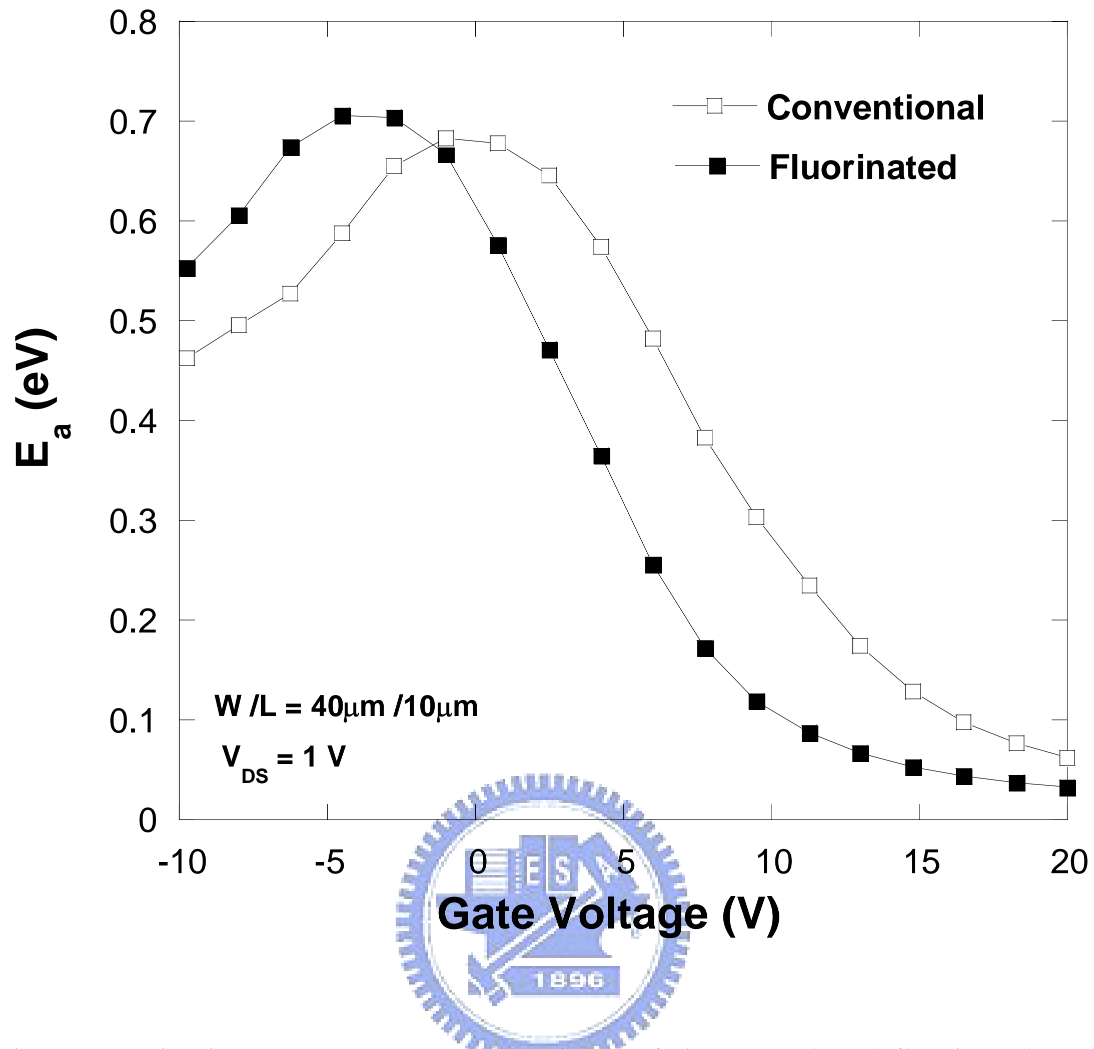


Fig. 2.7 Activation energy versus gate voltage of the control and fluorinated SPC poly-Si TFTs.

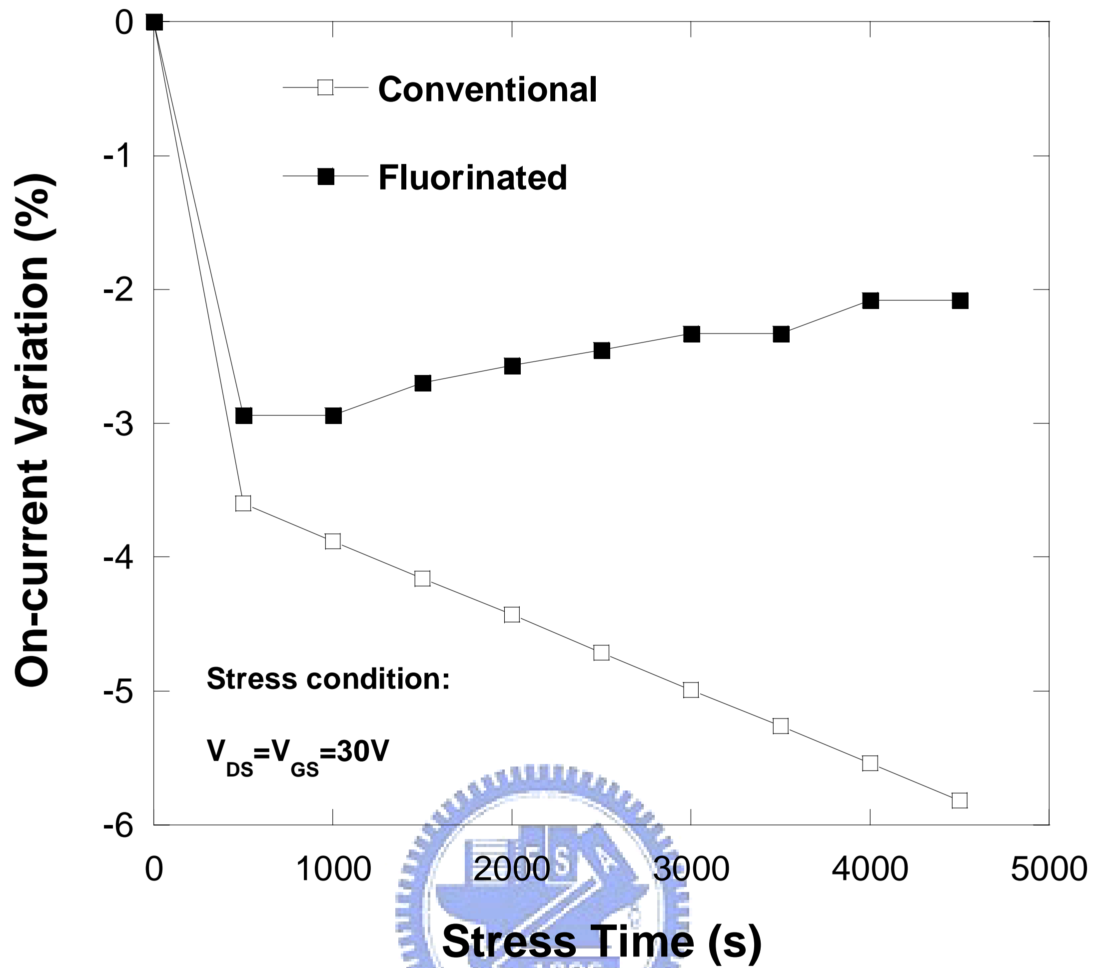


Fig. 2.8 On-current variation as a function of stress time under a hot carrier stress of the control and fluorinated SPC poly-Si TFTs.

Chapter 3

Improved Performance and Reliability of Excimer-Laser-Annealed (ELA) Poly-Si TFTs with CF_4 plasma treatment

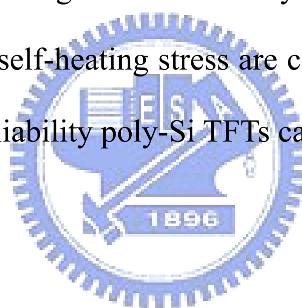
3.1 Introduction

Poly-Si TFTs have been used to integrate driving circuits and pixel elements on one glass substrate in active matrix liquid crystal displays (AM-LCDs) [1]. Recently, much attention has been paid on their potential to realize the System-on-Panel (SOP). To accomplish this goal, high-performance poly-Si TFTs with excellent device reliability are required. Excimer laser annealing (ELA) has been utilized to gain the device performance of poly-Si TFTs [2], [3]. ELA process can enlarge poly-Si grain size to enhance carrier mobility of TFT devices. Hydrogenation process is also used to terminate the trap states in the ELA-processed poly-Si. Unfortunately, although the device performance can be improved due to the hydrogen termination, hydrogenated poly-Si TFTs have a very serious instability issue due to the Si-H bonds breaking under an electrical stress [4], [5]. To solve this problem, it has been reported that fluorine can both terminate the trap states of the poly-Si, and maintain the device characteristics under a long-term electrical stress [6]-[11]. This reliability improvement is believed to be due to the high binding energy of Si-F bonds.

It is known that conventional ion implantation may be not so suitable for large-sized glass substrate. Moreover, a subsequent high temperature annealing is

required to activate the fluorine atoms and to recover the implantation-induced defects, which is not compatible with the current low-melting point glass substrates. Therefore, fluorinated oxide (SiO_xF_y) films have been proposed to serve as a fluorine diffusion source [10]. However, extra film deposition and etching are required. Low process-temperature and good process-compatibility are demanded in current TFTs production. For these reasons, a fluorine-based plasma treatment seems to be a very good solution to fluorinate ELA poly-Si TFTs.

In this chapter, ELA poly-Si TFTs are demonstrated with a novel CF_4 plasma treatment technique. This technique is a simple and process-compatible method to effectively reduce trap states of ELA poly-Si and thus improve the device performance. Moreover, to investigate the reliability of the CF_4 plasma-treated ELA poly-Si TFTs, hot-carrier and self-heating stress are carried out. Using this technique, high-performance and high-reliability poly-Si TFTs can be achieved.



3.2 Experimental

The schematic diagram of fabrication processes is illustrated in Fig. 3.1. First, a 100-nm-thick amorphous silicon layer was deposited on thermally oxidized Si wafer by dissociation of SiH_4 gas in a low-pressure chemical vapor deposition (LPCVD) system at 550℃. Next, a semi-Gaussian-shaped KrF excimer laser (λ= 248 nm) with an energy density of 420 mJ/cm^2 was performed for the phase transformation from amorphous-Si to poly-Si. The average grain size of the poly-Si is approximately 300 nm. Individual active regions were then patterned and defined. After RCA clean, the samples were subjected to the CF_4 plasma treatment, conducted in a plasma-enhanced chemical vapor deposition (PECVD) system at 350℃ for 15 seconds, under a pressure of 200 mTorr and a power of 10 Watts. Then, a 100-nm-thick TEOS oxide

and a 200-nm-thick poly-Si were deposited to serve as the gate dielectric and the gate electrode. A self-aligned phosphorous ion implantation was preformed with the dosage and energy of 5×10^{15} cm^{-2} and 40 keV, respectively. The dopant activation was performed by excimer laser annealing (ELA), followed by a deposition of passivation layer and the definition of contact holes. Finally, a 500-nm-thick Al electrode was deposited and patterned. For comparison, the control sample was prepared without the CF_4 plasma treatment process. No hydrogenation process was carried out on these devices. The dimensions of the transistors tested in this study are W/L = 40/20 μm.

3.3 Results and Discussion

3.3.1 Material Analysis

To exclude the plasma cleaning effect, the surface contaminations of the poly-Si samples after RCA clean were examined using Total Reflection X-Ray Fluorescence (TRXRF), and the results show that no significant surface contamination were detected. Also, the thickness variations of the poly-Si films before and after CF_4 plasma treatment measured using ellipsometer were within 5 %. Therefore, both the plasma cleaning effect and the poly-Si thinning by the CF_4 plasma treatment are eliminated.

Figure 3.2 exhibits the SIMS profiles of the control and CF_4 plasma-treated poly-Si films. As can be seen, lots of fluorine atoms were introduced into the SiO_2/poly-Si interface by using the CF_4 plasma treatment. We believe that these piled-up fluorine atoms provide an effective trap states passivation, because the channel is formed near the interface. Moreover, Electron Spectroscopy for Chemical Analysis (ESCA) was carried out to identify the incorporation of fluorine in the ploy-Si film with the CF_4 plasma treatment, as shown in Fig. 3.3. A strong signal of F

bonds is detected in the CF_4 plasma treated sample. Also, Fourier Transform Infrared Spectroscopy (FTIR) spectra of the conventional and CF_4 plasma-treated poly-Si films are also shown in Fig. 3.4. The spectra exhibit absorption peaks corresponding to Si-F bonds and Si-O bonds centered at round 940 and 1100 cm^{-1}. The strong peak of Si-O bond is related to the SiO_2 substrate. These results indicate that by employing this CF_4 plasma treatment technique not only the fluorine atoms were introduced into the poly-Si but also the Si-F bonds were formed in the SiO_2/poly-Si interface.

3.3.2 Device Characteristics

The transfer characteristics (I_D-V_{GS}) and field-effect mobility (μ_{eff}) versus the gate voltage of devices are shown in Fig. 3.5. The measurements were performed at V_{DS} = 0.5 V and 5 V. The threshold voltage (V_{th}) was defined as the gate voltage required to achieve a normalized drain current of $I_D = (W/L) \times 100$ nA at V_{DS} = 5 V. As can be seen, excellent device characteristics are observed for the CF_4 plasma-treated TFT. The V_{th} and the subthreshold slope (*S.S.*) of the CF_4 plasma-treated TFT are 4.35 V and 1.28 V/dec., respectively, which are superior to 5.75 V and 1.92 V/dec. of the control TFT. The leakage current of the CF_4 plasma treated TFT is more than one order in magnitude lower than that of the control TFT, especially at V_{GS} = -5V. Moreover, the corresponding *On/Off* current ratio of the CF_4 plasma-treated TFT is approximately 8 times larger than that of the control one. Also, the CF_4 plasma-treated TFT has an about 50% enhancement in the maximum field-effect mobility (μ_{eff}). The comparison of the extracted device parameters for the control TFT and the CF_4 plasma-treated TFT is listed in Table 3.1. We believe that these significant device characteristic improvements are due to the effective fluorine passivation effect in poly-Si TFTs by using the CF_4 plasma treatment. Figure 3.6 shows the output characteristics (I_D-V_{DS}) of the control and the CF_4 plasma treated poly-Si TFTs. As can

be seen, the driving currents of the CF_4 plasma-treated poly-Si TFT increase dramatically due to the fluorine passivation. The driving current at V_{GS} = 17.5 V and 25 V with V_{DS} = 20 V increase 176.3 % and 92.6 %, respectively. Therefore, the output characteristics can be greatly improved with the CF_4 plasma treatment.

It is worth noting that compared with SPC poly-Si TFTs with CF_4 plasma treatment (Chapter 2), we found that the V_{th} shift was smaller and the leakage current improvement was more significant in ELA poly-Si TFTs. We attribute these to the reasons discussed below. Considering the SPC poly-Si TFTs, during the long-time source/drain activation process (600℃ for 24 hours), we believe that fluorine atoms would be evolved and diffused into the gate oxide to induce oxide trap charges, whereas, for in ELA poly-Si TFTs, the gate oxide above the poly-Si channel would screen the laser energy during the source/drain activation. Therefore, few fluorine atoms were evolved in ELA poly-Si TFTs. As a result, the SPC poly-Si TFTs with CF_4 plasma treatment show more V_{th} shift than ELA poly-Si TFTs .

On the other hand, there are two types of tarp states in poly-Si affecting the carrier transport. One is the grain boundary trap states, the other is interface states. For the ELA poly-Si TFTs, the grain boundary trap states are fewer than those in the SPC poly-Si TFTs, so the interface states dominate the device performance. However, for SPC poly-Si TFTs, grain boundary trap states dominate. With CF_4 plasma treatment, the pilled-up fluorine atoms near the interface provide great interface state passivation. Therefore, the device characteristics of ELA poly-Si TFTs including the I_{on}, I_{off}, and μ_{ef} are improved more significantly than those in SPC poly-Si TFTs.

3.3.3 Extraction of Trap State Density

In order to verify the fluorine passivation effect of the devices, the effective trap states densities (N_t) were calculated from the *S.S.*. the N_t can be expressed as [11]:

$N_t = [(S.S./\ln 10)(q / kT)-1)](C_{ox}/q)$ (1)

where the C_{ox} is the capacitance of the gate oxide. The N_t of the control TFT and the CF_4 plasma treated TFT are 6.72×10^{12} cm^{-2} and 4.42×10^{12} cm^{-2}, respectively. The N_t values reflect both interface sates and grain boundary trap states near the SiO_2/poly-Si interface. Therefore, those traps near the SiO_2/poly-Si interface were effectively terminated by fluorine atoms using CF_4 plasma treatment. Also, the grain boundary trap densities (Q_T) of the devices were evaluated using Proano's method [12], [13]. As shown in Fig. 3.7, the Q_T of the CF_4 plasma-treated TFT and the control TFT are 3.47×10^{12} cm^{-2} and 4.11×10^{12} cm^{-2}, respectively. This proves that the grain boundaries trap states of the poly-Si TFT were effectively reduced with the CF_4 plasma treatment.

To clarify how the fluorine passivate the trap states of poly-Si TFTs, the density of states (*DOS*) in the energy band gap were calculated using field-effect conductance method [14]. As shown in Fig. 3.8, both deep states and tail states are significantly reduced in the CF_4 plasma treated TFT. We deduce that for the control TFT, there exist many dangling bonds and strain bonds at the SiO_2/poly-Si interface, resulting in high deep states and tail states [15], [16]. However, for the CF_4 plasma treated TFT, fluorine atoms were introduced into the SiO_2/poly-Si network to terminate the dangling bonds, release the strain bonds and form the S-F bonds, reducing the trap states and resulting in a great improvement of the device characteristics. This fluorine termination effect in the SiO_2/poly-Si interface network has been discussed in Chapter 2 and has been schematically plotted in Fig. 2.5.

3.3.4 Gate oxide integrity

It is known that the oxide integrity is an important challenge for law temperature poly-Si TFTs. It has been reported that fluorine incorporation can improve the

integrity of the gate dielectric [17], [18]. The effect of the CF_4 plasma treatment on the gate oxide of the poly-Si TFT has been also investigated. Figure 3.9 shows the cumulative distributions of the time-zero-dielectric-breakdown (TZDB) characteristics and leakage current of the gate oxides with and without CF_4 plasma treatment. As can be seen, the CF_4 plasma treated oxide exhibits approximately 65 % enhancement in the breakdown voltage compared to the control. Also, the leakage current of the gate oxide is significantly suppressed by using CF_4 plasma treatment. These improved breakdown voltage and leakage current can be attributed to the formation of Si-F bonds to replace weak bonds at the SiO_2/poly-Si interface [18]. Those results prove that the CF_4 plasma treatment can effectively improve in both gate dielectric integrity and the device performance of poly-Si TFT due to the fluorine termination.

3.3.5 Device Reliability

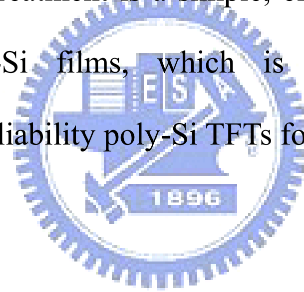
The instability issue of devices is the bottleneck for poly-Si TFT circuits developing. To investigate the reliability of the CF_4 plasma-treated poly-Si TFT, two accelerating electrical stress tests were carried out. One is hot-carrier stress (HCS) and the other is self-heating stress (SHS), as shown in Fig. 3.10. The HCS, which occurs at $V_{th} \leq V_{GS} \leq V_{DS}$, have been reported can cause the most severe device degradation in poly-Si TFTs. The HCS-induced damage is attributed to the creation of numerous trap states near the drain side, and the degradation rate depends on the strength of the drain electric field [15], [19]-[21]. On the contrary, the SHS-induced damage is attributed to the large Joule heat, resulted from a high drain current under a condition of $V_{GS} \geq V_{DS}$ [22]-[25]. Because poly-Si TFTs are fabricated on a poor thermal-conducting substrate, devices can reach a very high temperature during operation. Such high temperature enhances bonds breaking to generate dangling bonds in the poly-Si, and

thus degrade the TFT performance [25]. The degradation rate of the SHS increases with the drain current. In this study, the stress conditions of HCS are V_{GS} = 10 V and V_{DS} = 25 V, whereas the conditions of SHS are V_{GS} = 25 V and V_{DS} = 20 V. The variations of maximum On-current (I_{on}) and maximum field-effect mobility (μ_{eff}) are defined as $(I_{on,stressed} - I_{on,0}) / I_{on,0} \times 100$ % and $(\mu_{eff,stressed} - \mu_{eff,0}) / \mu_{eff,0} \times 100$ %, where $I_{on,0}$, $\mu_{eff,0}$, $I_{on,stressed}$, and $\mu_{eff,stressed}$ indicate the measured values prior to and after the electrical stress.

Figure 3.11 shows the variations of (a) the I_{on} and (b) the μ_{eff} versus stress time under HCS. As can be seen, the degradation rate of the control TFT is almost twice that of the CF_4 plasma-treated TFT. We deduce that during the impact ionization, the drain junction of the control TFT was damaged seriously by drain-avalanche-hot-carrier, and lots of trap states were generated, which raised the channel resistance near the drain [22]. On the contrary, the CF_4 plasma treated TFT shows small degradation due to the strong Si-F bonds formed in the poly-Si. Therefore, The CF_4 plasma treated TFT has high stress immunity against the HCS. Figure 3.12 shows the variations of (a) the I_{on} and (b) the μ_{eff} versus stress time under SHS. The I_{on} decreases seriously in the control TFT. Moreover, although not shown, there is a large distortion found in the subthreshold region for the control TFT after SHS. This is attributed to the generation of dangling bonds throughout the channel, resulted from the increase of interface states under a high temperature [25]. However, for the CF_4 plasma-treated TFT, the device characteristics stay nearly unchanged even after 1000s stress. Therefore, the CF_4 plasma-treated TFT also shows high stress immunity against the SHS. As a result, the CF_4 plasma treatment can greatly alleviate the device degradation under two kinds of electrical stress. This is attributed to the stable Si-F bonds formed at the SiO_2/poly-Si interface and the nearby grain boundaries.

3.4 Summary

A process-compatible fluorination technique of poly-Si TFTs by using CF_4 plasma treatment combined with excimer laser annealing is proposed. Using this technique, the device performance, including V_{th}, *S.S.*, leakage current, μ_{eff} , *On/Off* ratio, and gate dielectric integrity can be significantly improved. This is due to the fluorine passivation of interface states and grain boundary trap states. The reliability of the poly-Si TFTs with CF_4 plasma treatment has been investigated by employing hot-carrier stress and self-heating stress. Under these stress tests, CF_4 plasma-treated TFTs exhibit excellent stress immunity, which is due to the formation of Si-F bonds. As a result, the CF_4 plasma treatment is a simple, effective, and process-compatible method to passivate poly-Si films, which is very promising to fabricate high-performance and high-reliability poly-Si TFTs for future SOP applications.



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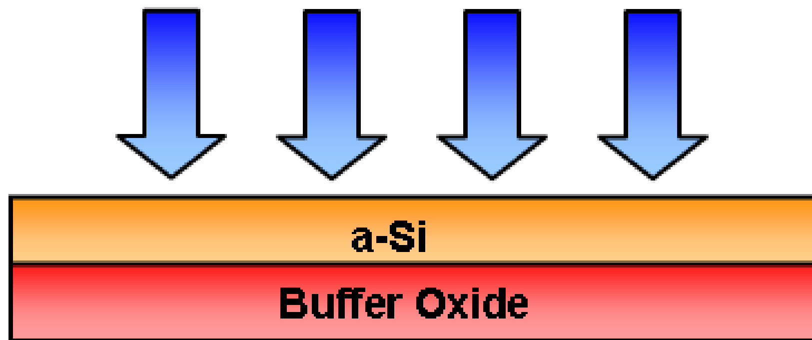
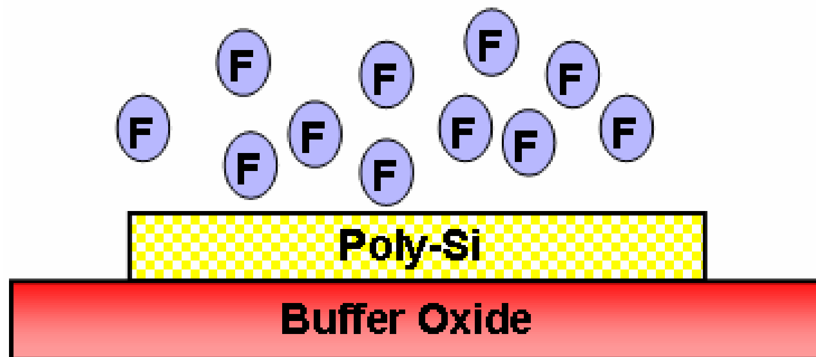
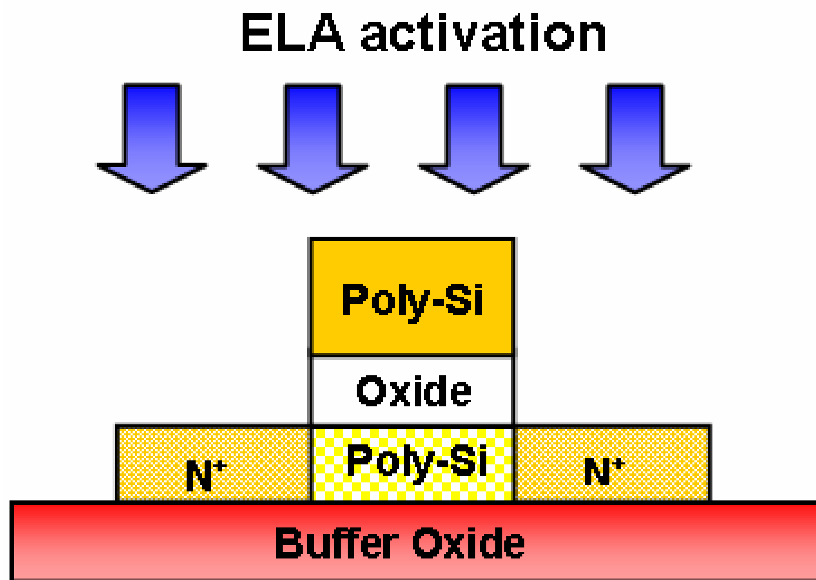


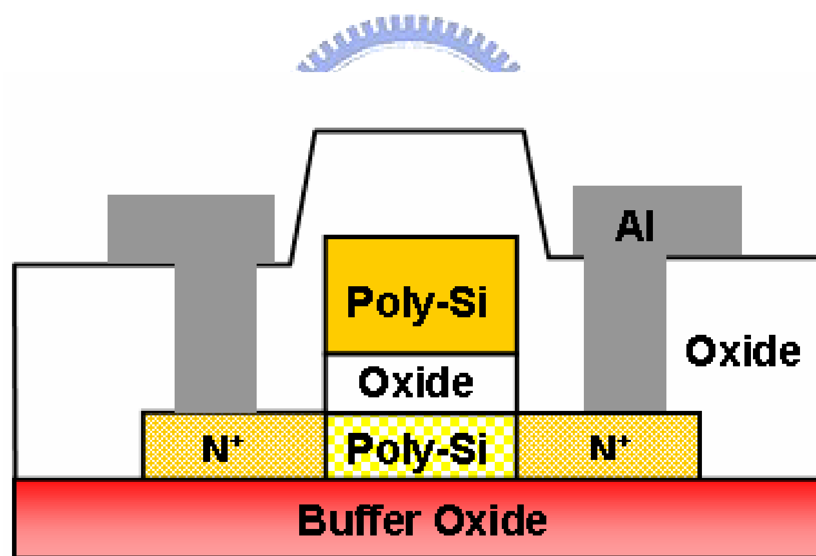
(a) Depositing amorphous silicon and ELA processing.



(b) Defining active region and CF_4 plasma treatment.



(c) S/D implantation and dopand activation by ELA.



(d) Depositing passivation oxide, opening contact holes, depositing metal, and patterning metal.

Fig. 3.1 Schematic diagram of the fabrication process for ELA poly-Si TFTs with CF_4 plasma treatment.

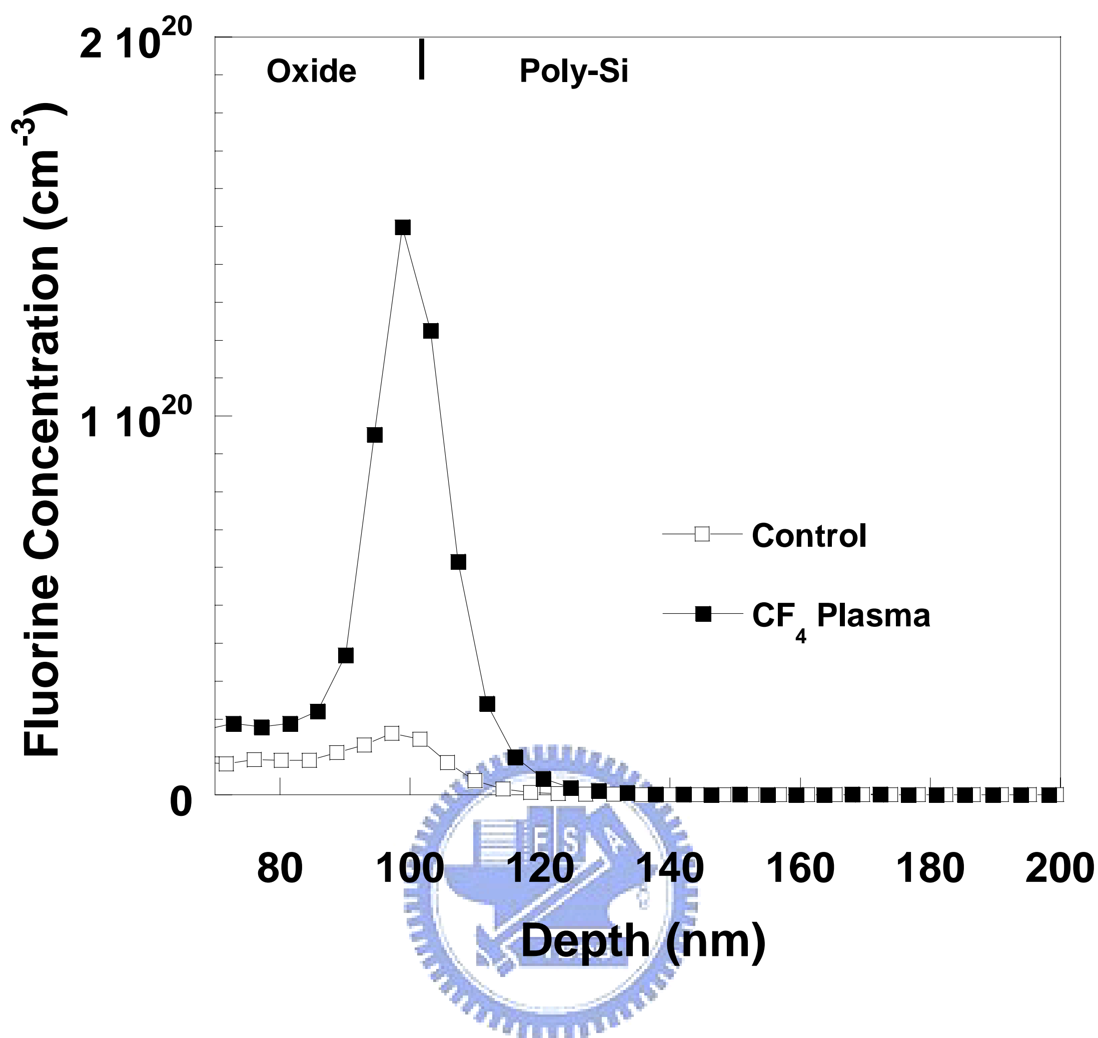


Fig. 3.2 SIMS profiles of the control and the CF_4 plasma-treated ELA poly-Si films.

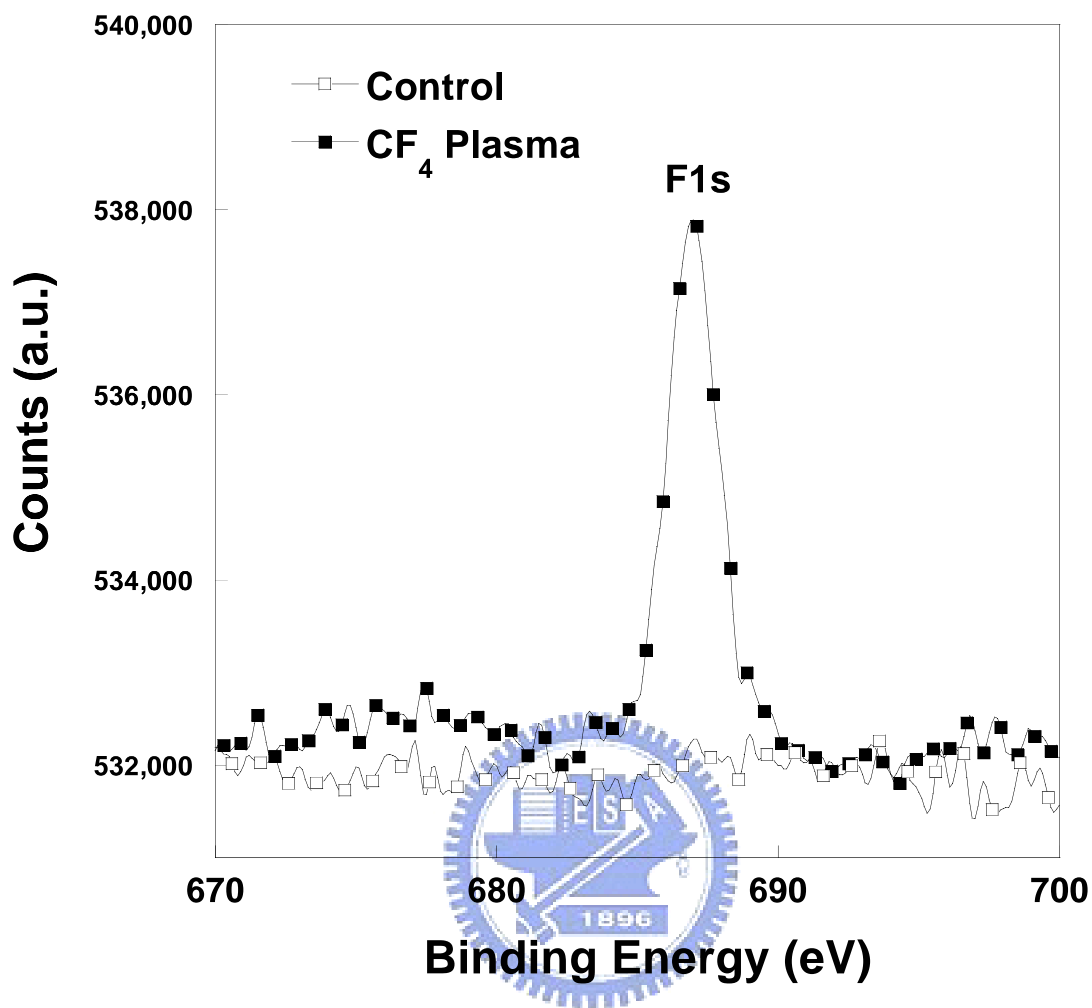


Fig 3.3 ESCA profiles of the control and the CF_4 plasma-treated ELA poly-Si films.

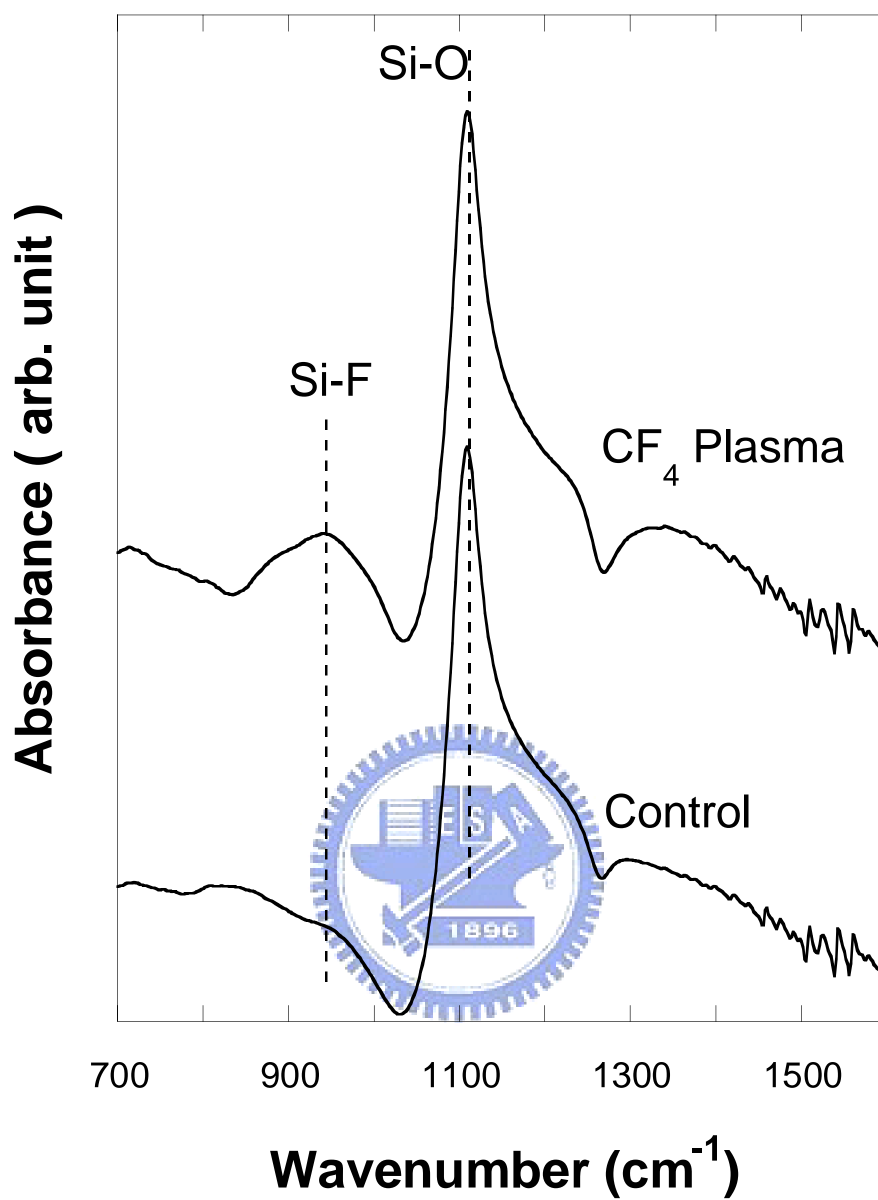


Fig. 3.4 FTIR spectra of the conventional and the CF_4 plasma-treated ELA poly-Si films.

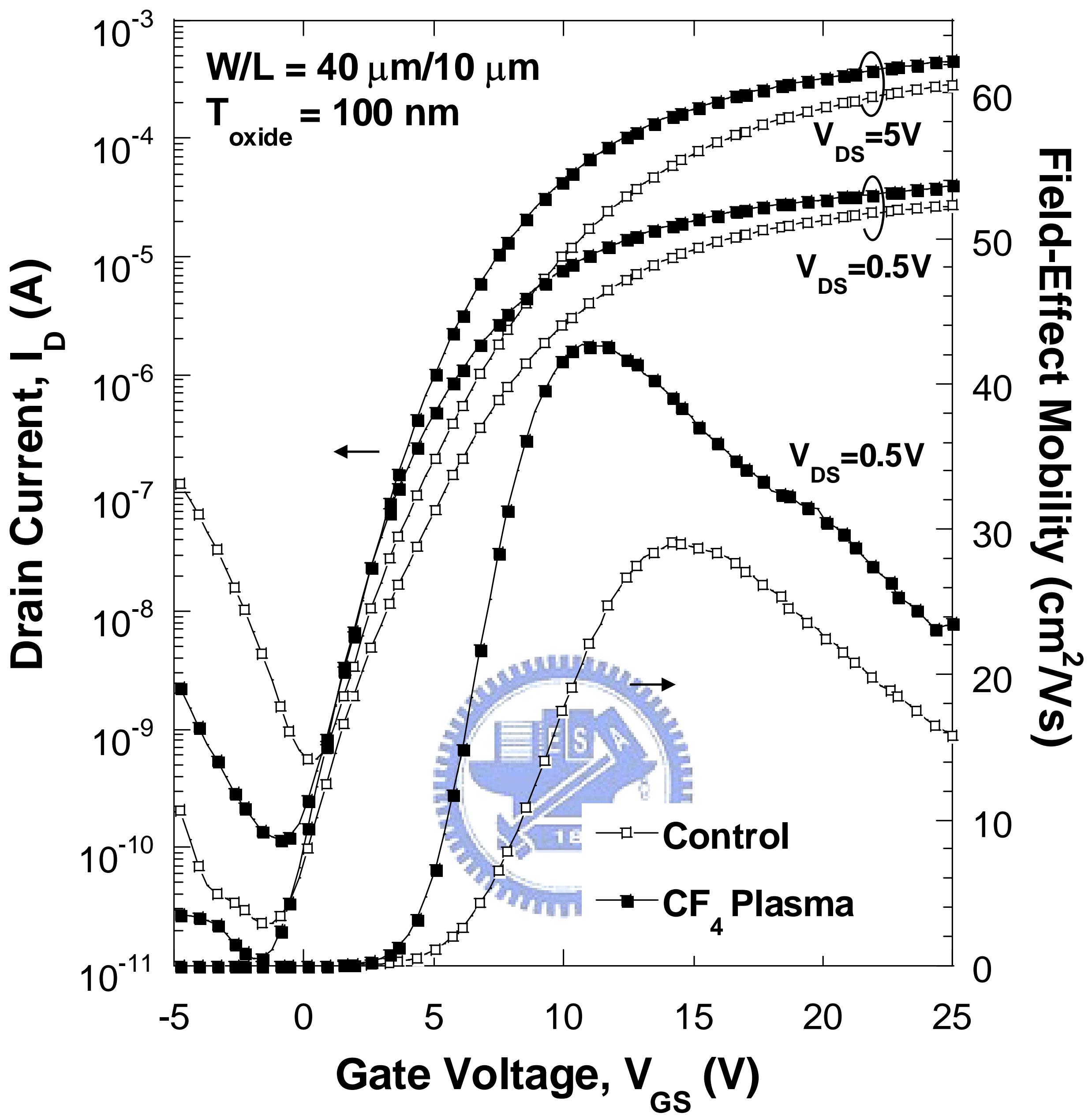


Fig 3.5 Transfer characteristics and field-effect mobility versus gate voltage for the control and the CF_4 plasma-treated ELA poly-Si TFTs.

Table 3.1 Comparison of the extracted device parameters for the control and the CF_4 plasma-treated ELA poly-Si TFTs.

ELA Poly-Si TFTs	***Control***	***CF_4 plasma***
V_{th} (V)	5.75	4.35
S.S.(V/dec.)	1.92	1.28
μ_{eff} (cm^2/V.s)	29.1	43.2
I_{on} (μA)	287	467
I_{off} (pA)	55.5	11.6
On/Off Ratio (×10^6)	0.52	4.03
Off-current @V_{GS} = - 5 V	1.52×10^{-7}	3.31×10^{-9}
Q_T (×10^{12} cm^{-2})	6.72	4.42
N_T (×10^{12} cm^{-2})	4.11	3.47

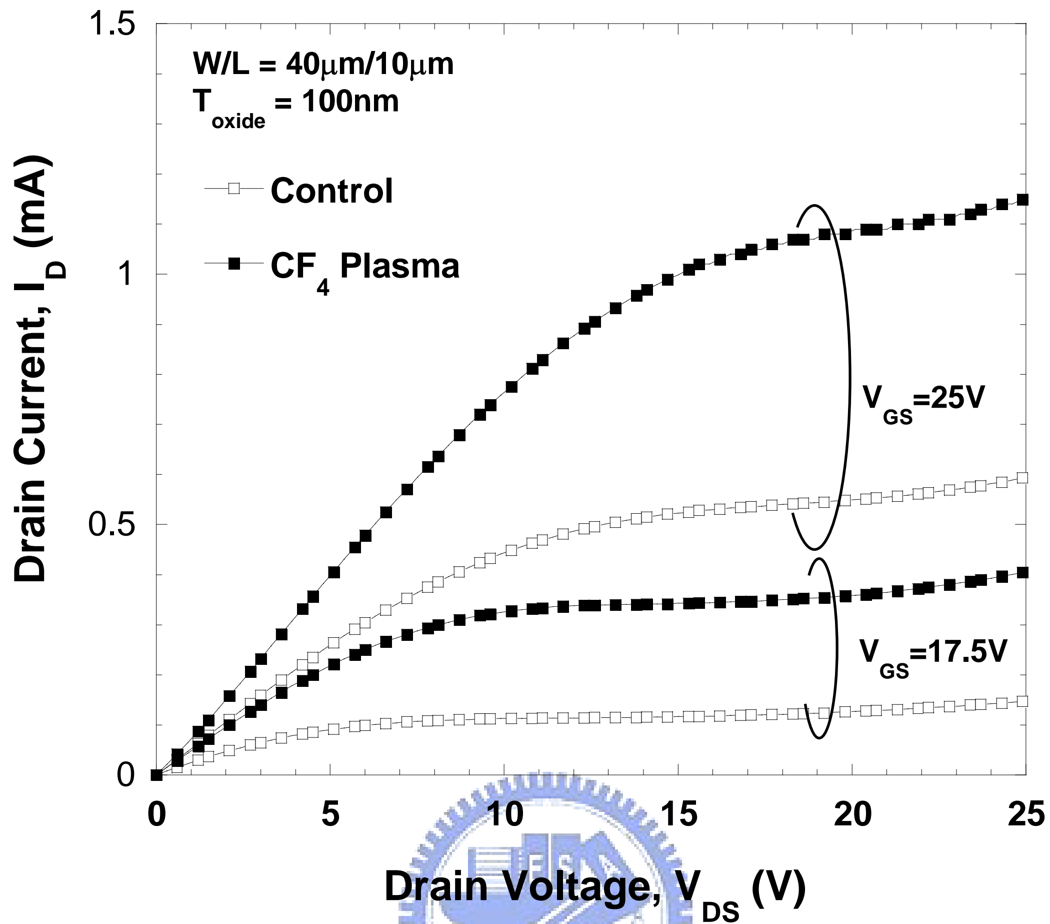


Fig 3.6 Output characteristics of the control and the CF_4 plasma treated ELA poly-Si TFTs.

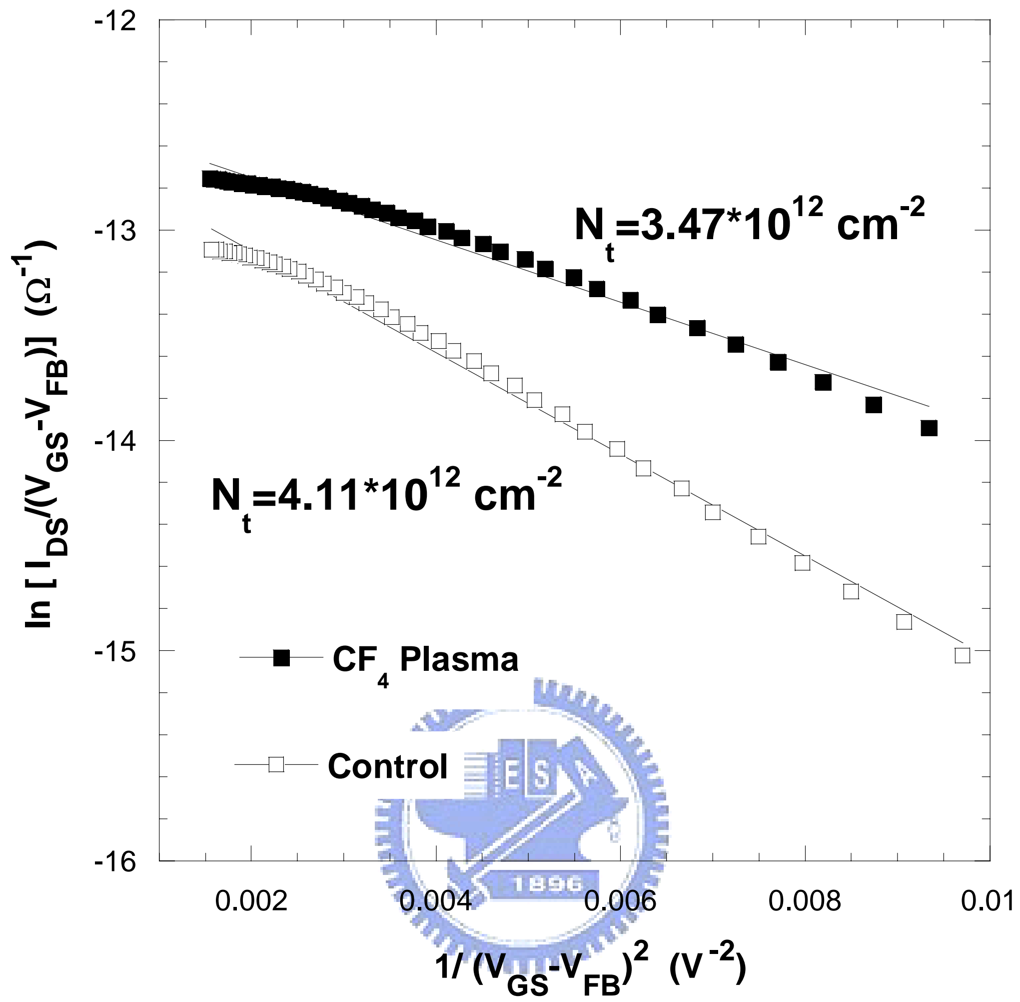


Fig. 3.7 $\ln[I_D/(V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ curves at $V_{DS} = 0.1V$ and high V_{GS} for control and fluorinated ELA poly-Si TFTs.

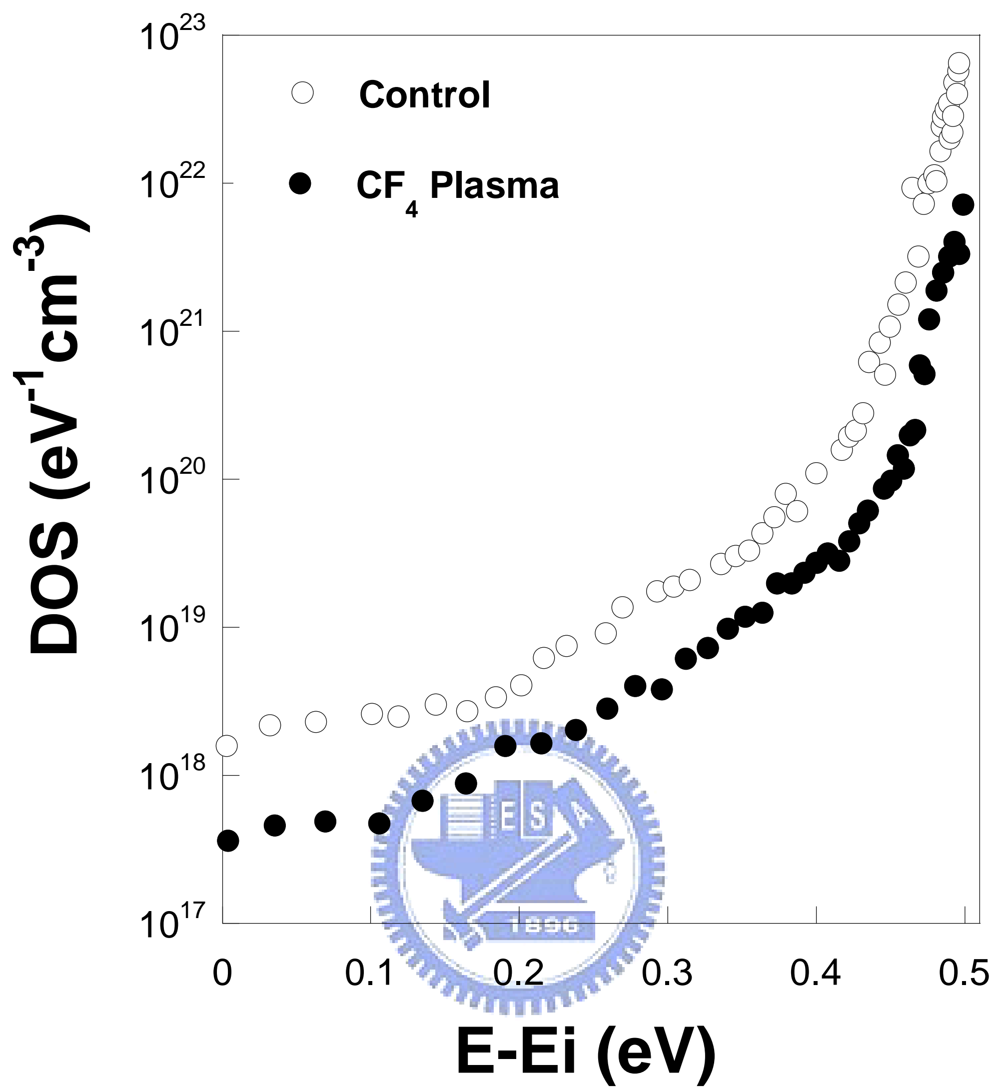
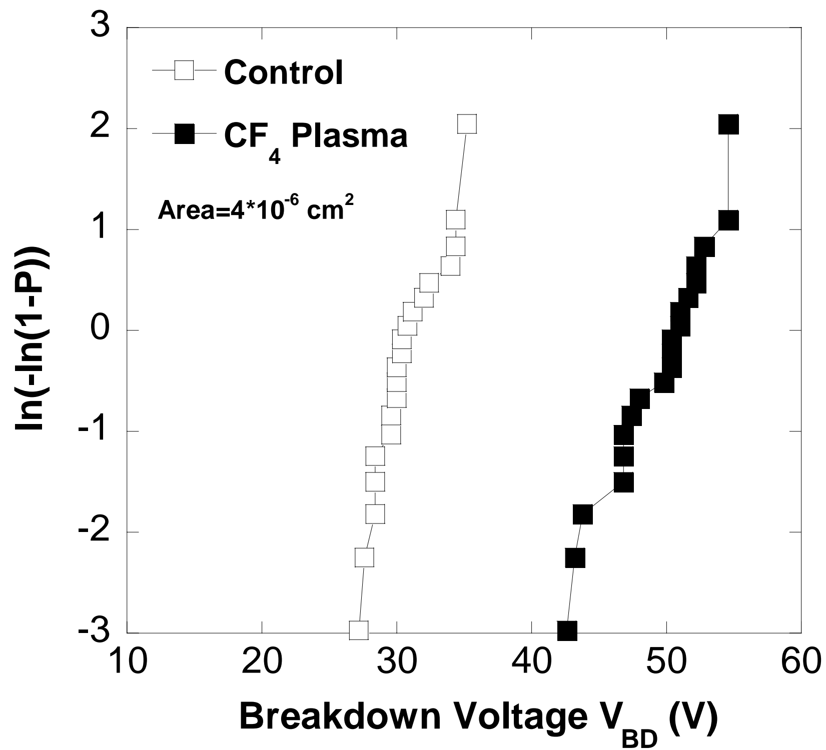
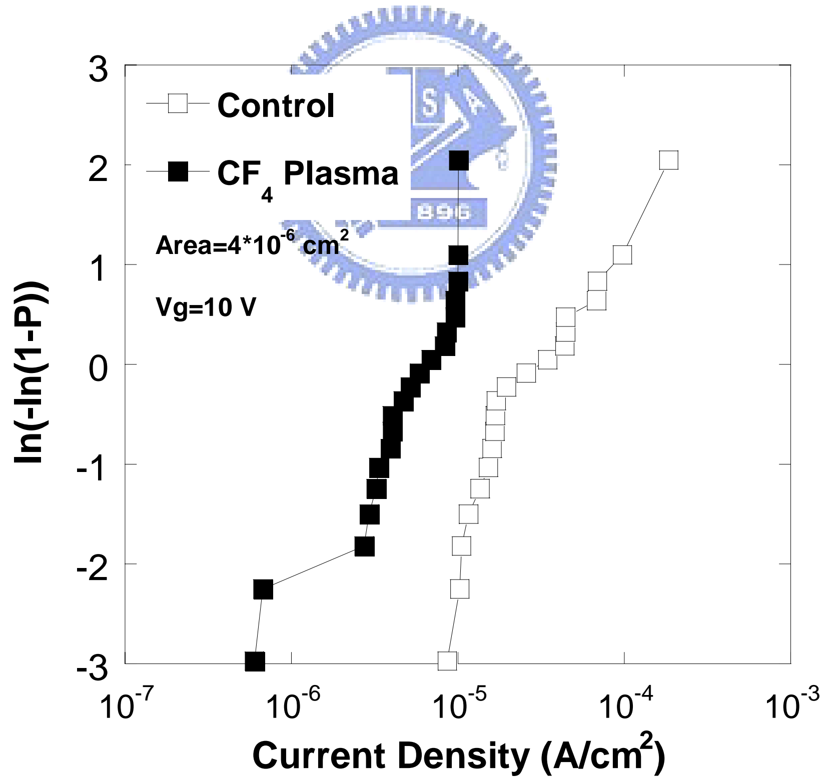


Fig 3.8 Density of states (DOS) in the energy band gap of the control and the CF_4 plasma-treated ELA poly-Si TFTs.



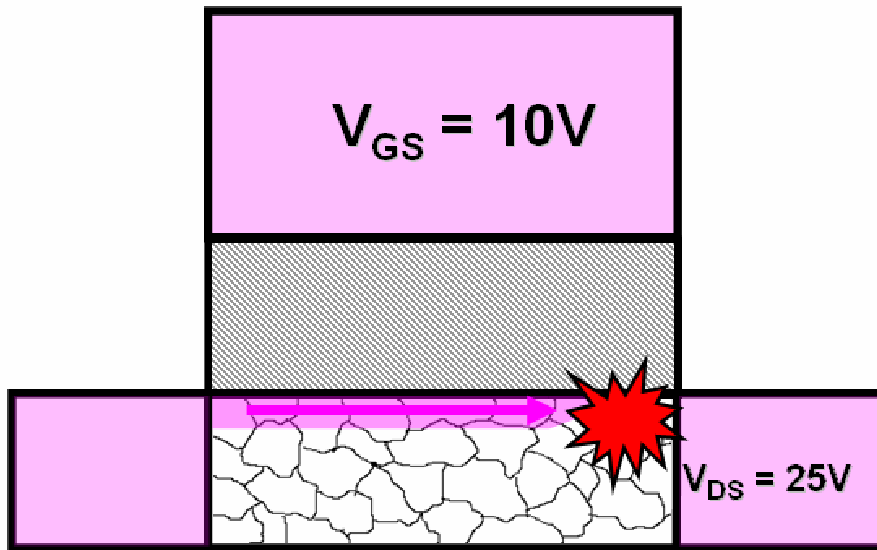
(a)



(b)

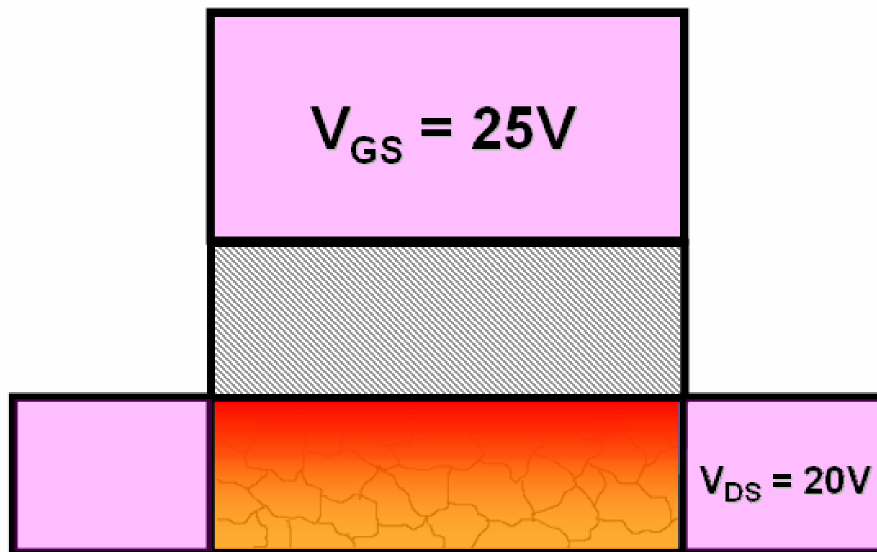
Fig. 3.9 Cumulative distributions of (a) the time-zero-dielectric-breakdown (TZDB) characteristics (b) leakage current of the gate dielectrics with and without CF_4 plasma treatment.

HCS (Hot-Carrier Stress)



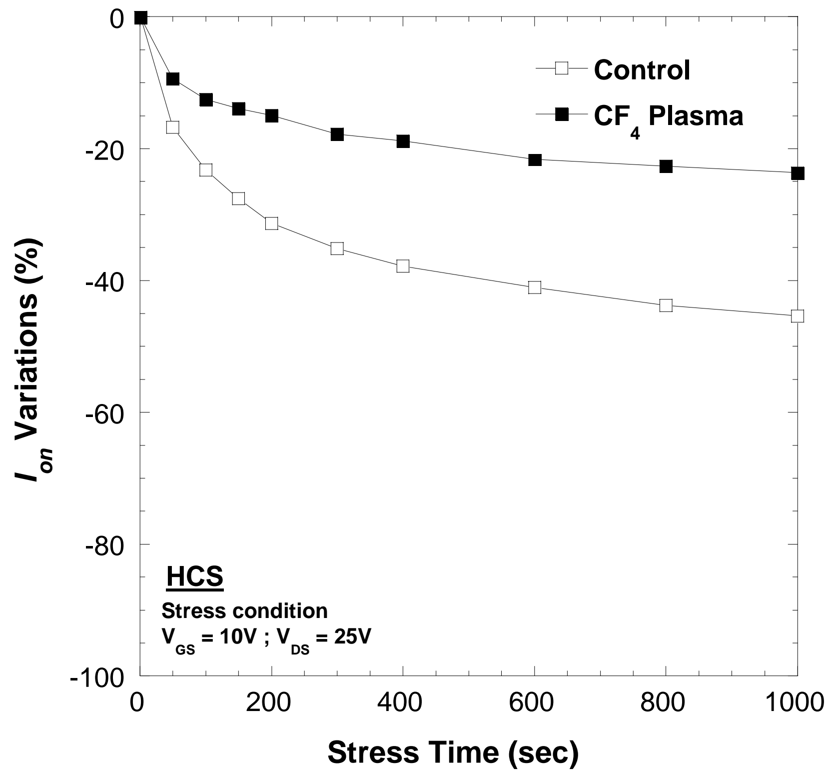
(a)

SHS (Self-Heating Stress)

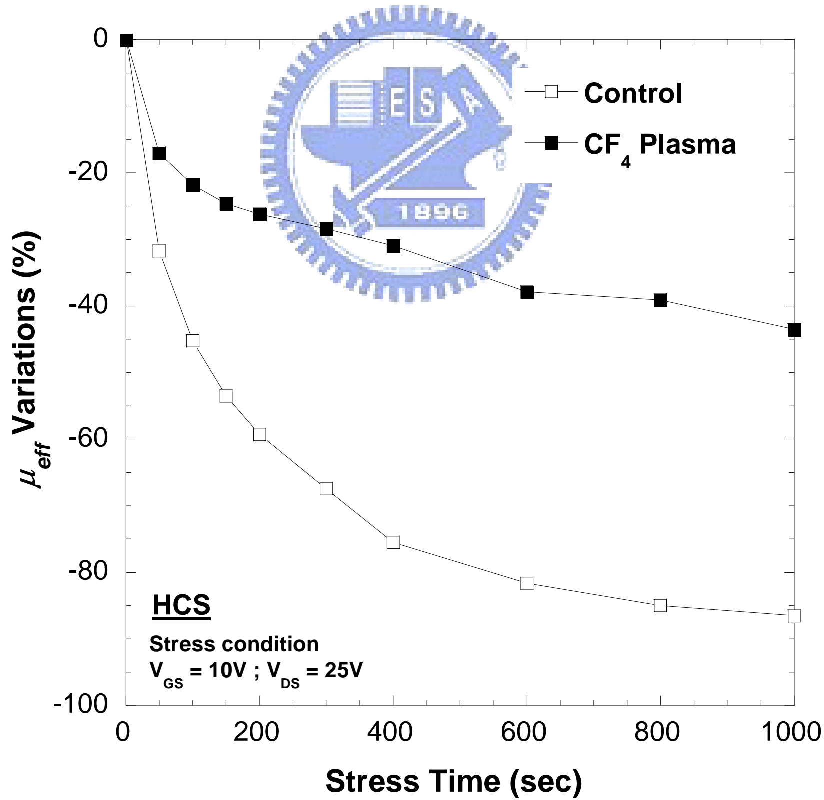


(b)

Fig. 3.10 Two accelerating electrical stress tests. (a) hot-carrier stress (HCS), (b) self-heating stress (SHS)

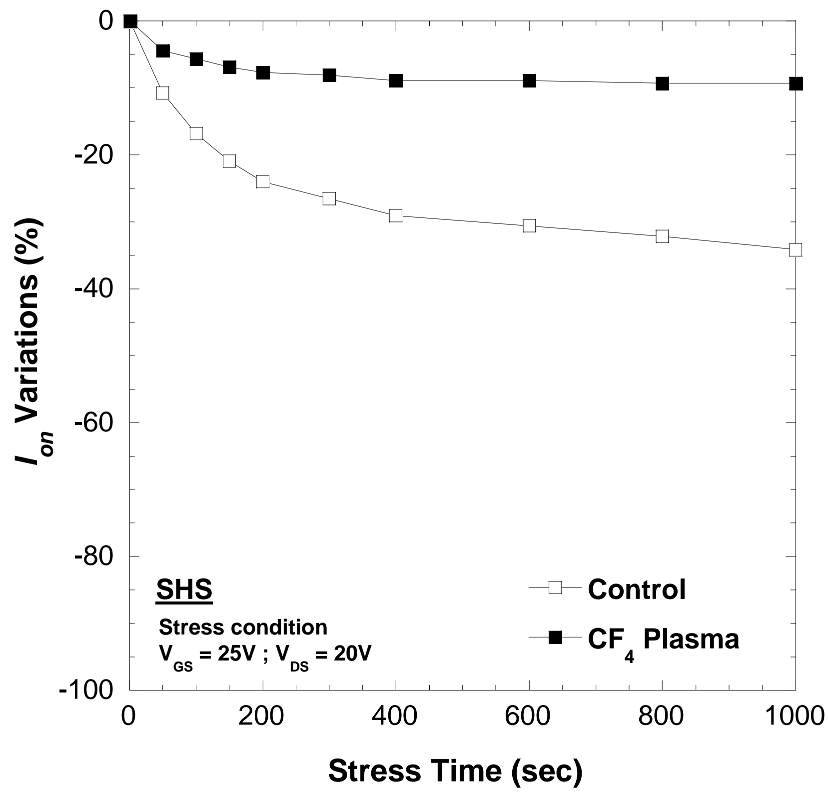


(a)

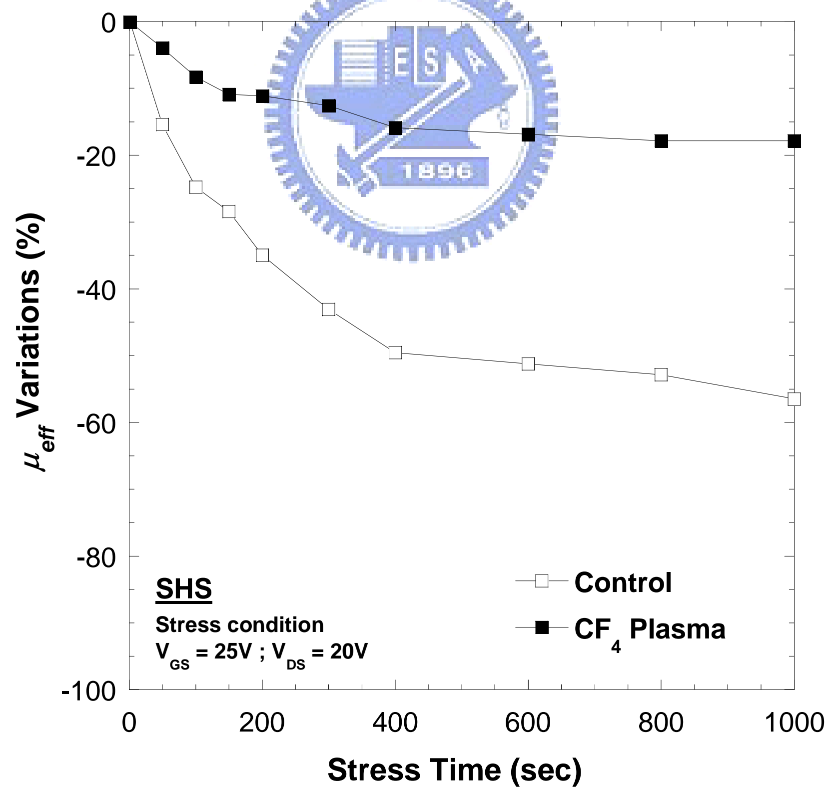


(b)

Fig. 3.11 Variations in (a) the On-current and (b) the field-effect mobility as a function of stress time under hot-carrier stress for the control and CF_4 plasma-treated ELA poly-Si TFTs.



(a)



(b)

Fig. 3.12 Variations in (a) the On-current and (b) the field-effect mobility as a function of stress time under self-heating stress for the control and CF_4 plasma-treated ELA poly-Si TFTs.

Chapter 4

Performance and Reliability of Poly-Si TFTs on FSG Buffer Layer

4.1 Introduction

Over the past decade, many efforts have been made in fabricating high-performance and high-reliability poly-Si TFTs to accomplish System-on-Panel (SOP) [1]. For instance, excimer laser annealing (ELA) has been utilized in enlarging the grains of the poly-Si to reduce trap states, leading to an excellent device performance [2]. However, the random distribution of grain boundaries in poly-Si films still causes a large leakage current and poor device uniformity. Hydrogenation process has been utilized to terminate the grain boundary trap states [3]. However, hydrogenated poly-Si TFTs suffer from an instability issue due to weak Si-H bonds [4].

On the other hand, a low-temperature PECVD-oxide buffer layer is conventionally adopted to block the contaminations from the inexpensive glass or flexible plastic substrate. Nevertheless, the mismatch between the thermal expansion coefficient of the poly-Si and that of the oxide causes considerable mechanical tensile stress at the interface during ELA, leading to the degradation in device performance [5]-[8]. All these drawbacks limit the applications of poly-Si TFTs. Fluorine passivation has been proposed to terminate trap states in the poly-Si [9]-[12]. The formation of Si-F bonds improves the device reliability. However, ion implantation is not appropriate for extremely large-sized glass substrate in current productions.

Therefore, a new method must be found to introduce fluorine atoms into poly-Si

films. Fluorinated silicate oxide (FSG) has been known easy to integrate using plasma-enhanced chemical vapor deposition (PE-CVD) systems. The out-diffused fluorine atoms form FSG can terminate trap states and also release the strain bonds at the interface [13]. In this Chapter, we propose a new fluorine passivation technique using a FSG film as a buffer layer. The Poly-Si TFTs fabricated on FSG buffer layers exhibit high device performance, uniformity and reliability.

4.2 Experimental

Figure 4.1 schematically depicts the cross-section of the proposed poly-Si TFT. All the experimental devices in this study were fabricated on thermally oxidized Si wafers. First, a 50-nm-thick FSG buffer layer was deposited using a PECVD system at 350°C with SiH_4, CF_4 and N_2O as process gases. To determine the effect of fluorine content in FSG layers, varying CF_4 flow rates of 10, 20, and 40 sccm, with a SiH_4 flow rate of 90 sccm and a N_2O rate of 5 sccm, were used to grow various FSG buffer layers, denoted by FSG1, FSG2 and FSG3, respectively. Table 4.1 lists the conditions of precursors to grow FSG buffer layers. Figure 4.2 shows SIMS profiles of fluorine for the as-deposited FSG layers. The fluorine contents in FSG1, FSG2 and FSG3 were calculated to be about 2%, 4%, and 7%, respectively.

Then, 100-nm-thick amorphous silicon layers were deposited on the FSG layers in a low-pressure chemical vapor deposition (LPCVD) system. Next, a semi-Gaussian-shaped KrF excimer laser (λ= 248 nm) with an energy density of 420 mJ/cm^2 was performed for the phase transformation from amorphous to polycrystalline silicon. The average grain size of the poly-Si is approximately 300 nm. Individual active regions were then patterned and defined. After a clean process, a 100-nm-thick TEOS oxide and a 200-nm-thick poly-Si were deposited to serve as the gate insulator and the gate electrode.

A self-aligned phosphorous ion implantation was preformed at the dosage and energy of 5×10^{15} cm^{-2} and 40 keV, respectively. The dopant activation was performed by ELA, followed by a deposition of passivation layer and the definition of contact holes. Finally, a 500-nm-thick Al electrode was deposited and patterned. For comparison, the control samples were fabricated on a 50-nm-thick conventional PECVD-oxide buffer layer.

4.3 Results and Discussion

4.3.1 Device Characteristics

Figure 4.3 shows the transfer characteristics of the conventional and the proposed poly-Si TFTs at V_{DS}=5V. The poly-Si TFTs fabricated on the FSG buffer layers exhibit better On-state and Off-state characteristics than those of the control sample. Notably, under a large negative gate bias (V_{GS}=-10 V), the leakage currents of the TFTs on FSG layers (3.08×10^{-9}A, 3.32×10^{-10}A, and 9.95×10^{-10}A for FSG1, FSG2, and FSG3, respectively) are over one order of magnitude lower than that (1.14×10^{-7}A) of the conventional device. Moreover, the threshold voltage and subthreshold swing of the poly-Si TFTs on FSG layers (4.77 V & 1.42 V/dec., 4.82 V & 1.44 V/dec., and 4.96 V & 1.45 V/dec. for FSG1, FSG2, and FSG3, respectively) are superior to those of the control sample (5.07 V & 1.55 V/dec.). It is known that the threshold voltage and subthreshold swing are more sensitive to the density of deep trap states near midgap associated with the dangling bonds. It is inferred that the dangling bonds within the poly-Si channel and SiO_2/poly-Si interface were effectively passivated by fluorine atoms. Therefore, we can ascribe these improved device characteristics to the facts that the reduced the traps by the incorporation of fluorine in the poly-Si films during ELA [12] and the released tensile stress at the poly-Si/buffer-oxide-layer interface [13].

The evidence of the fluorine incorporation can be firmly demonstrated with the

SIMS profiles of fluorine shown in Fig. 4.4. It is clearly observed that considerable fluorine atoms are detected in the poly-Si for the FSG samples and, in particular, two fluorine peaks are located at the top and bottom interfaces. Therefore, we believe that the weak bonds and dangling bonds in the poly-Si grain boundaries and both top and bottom interfaces, resulting in lots of trap states and interface states, are terminated by fluorine [10]. In order to verify the effect of fluorine passivation, the effective trap state density (N_T) was calculated from the square root of the slope of the $\ln(I_D V_{DS}/V_{GS})$ versus $1/V_{GS}^2$ plots, as shown in Fig. 4.5, proposed by Proano *et al.* [14]. The N_T for the control, FSG1, FSG2, FSG3 were 5.64×10^{12}, 3.91×10^{12}, 3.97×10^{12}, and 4.01×10^{12}, respectively. These figures strongly hint that the fluorine can effectively terminate the present trap states. However, the FSG3 shows a detrimental effect on the performance of the resulting TFT. This is attributed to the moisture absorption. According to previous report, the moisture absorption increased with increasing fluorine content in the FSG layers [15]. The absorbed moisture would easily form OH or react with fluorine to form HF, which in turn corrode the devices and result in the degraded performance and reliability [16]. The comparison of device characteristics of the conventional and the proposed poly-Si TFTs is listed in Table. 4.2.

4.3.2 Device Uniformity

Fig. 4.6 displays the statistical distributions of the field-effect mobility (μ_{eff}) and the leakage current (I_{off}) of the poly-Si TFTs fabricated on different buffer layers. The vertical bars in the figure indicate the minimum and maximum values of the devices characteristics and the squares present the average values. The average values of the μ_{eff} for the control, FSG1, FSG2 and FSG3 samples were 57.7, 66.7, 63.9 and 45.2 with standard deviations of 4.05, 2.98, 3.09 and 4.15, respectively. This tendency indicates that with moderate fluorine content in FSG layers the average values and the deviations of μ_{eff}

can be greatly improved. Also, the average values of the I_{off} for the control, FSG1, FSG2, and FSG3 samples were 6.8×10^{-8}, 7.8×10^{-9}, 1.3×10^{-9} and 1.8×10^{-9} with standard deviations of 8.14×10^{-8}, 2.46×10^{-9}, 6.55×10^{-10} and 1.93×10^{-9}, respectively. The uniformity of the poly-Si TFTs is strongly affected by the random distribution of grain boundaries. Therefore, using fluorine to terminate those trap states can effectively alleviate the influence of grain boundaries.

4.3.3 Device Reliability

Hot-carrier-stress was performed at V_{DS} = 20 V and V_{GS} = 10 V for 1000s to investigate the device reliability. Fig. 4.7 plots the variations of On-current (I_{on}), threshold voltage (V_{th}) and μ_{eff} over hot carrier stress time. The variations of I_{on}, V_{th} and μ_{eff} were defined as $(I_{on,stressed}-I_{on,0})/I_{on,0}\times100$ %, $(V_{th,stressed}-V_{th,0})/V_{th,0}\times100$ % and $(\mu_{eff,stressed}-\mu_{eff,0})/\mu_{eff,0}\times100$ %, respectively, where $I_{on,0}$, $V_{th,0}$, $\mu_{eff,0}$ and $I_{on,stressed}$, $V_{th,stressed}$, $\mu_{eff,stressed}$, represent the measured values before and after stress. Notably, the control shows relatively large variations in both V_{th} and μ_{eff} after 1000s stress, whereas the FSG2 stays almost unchanged. These results imply that poly-Si TFTs fabricated on the FSG layer greatly reduced the device degradation under hot carrier stress, which is due to the formation of the Si-F bonds.

Since the calculated percentages of F content in the FSG layers are 2%, 4% and 7% for FSG1, FSG2, and FSG3, respectively, we deduce based on the above experimental results that the trap states can be effectively terminated when the fluorine content in the FSG is above 2%; while the absorbed moisture in the FSG as the content is above 4% starts to induce visible corrosion of the poly-Si structures after competing with the trap states termination. Definitely, the corrosion becomes more severe as the content reached 7%. As a result, the optimized condition of fluorine content of FSG is probably within 2% to 4%.

4.4 Summary

A novel fabricating scheme for poly-Si TFTs on an FSG buffer layer is proposed. Significant improvements in the device performance and uniformity have been successfully demonstrated with fluorine incorporation in the poly-Si layer. The incorporation of fluorine also promotes the hot-carrier immunity. Fabricating poly-Si TFTs on FSG buffer layers with appropriate fluorine contents (2% to 4%) improves not only the electrical performance, uniformity, but also the device reliability.

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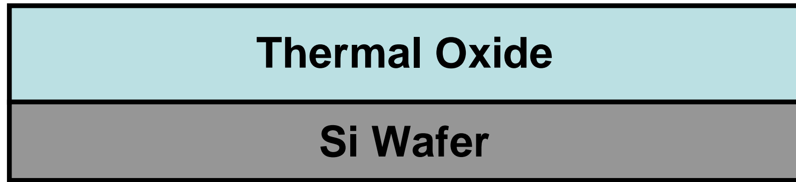
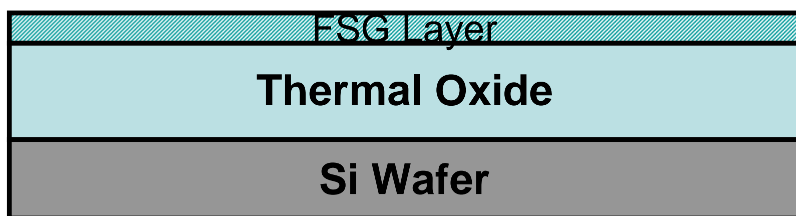
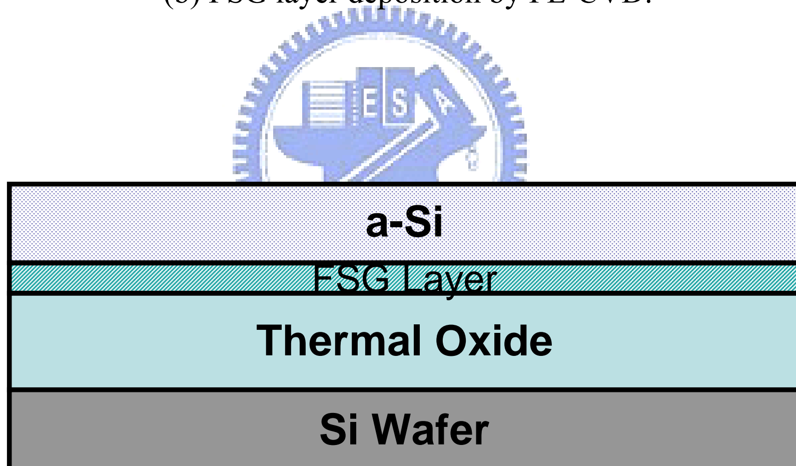


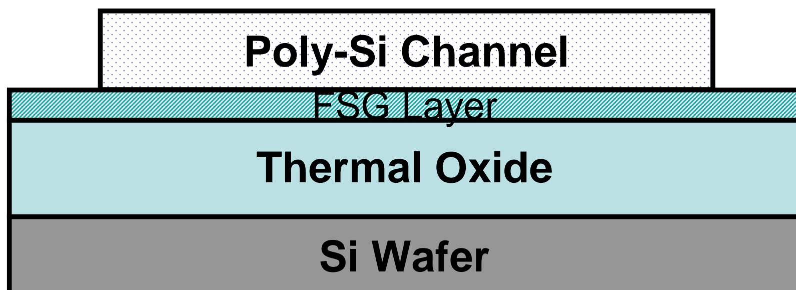
(a) Thermal oxidation by furnace.



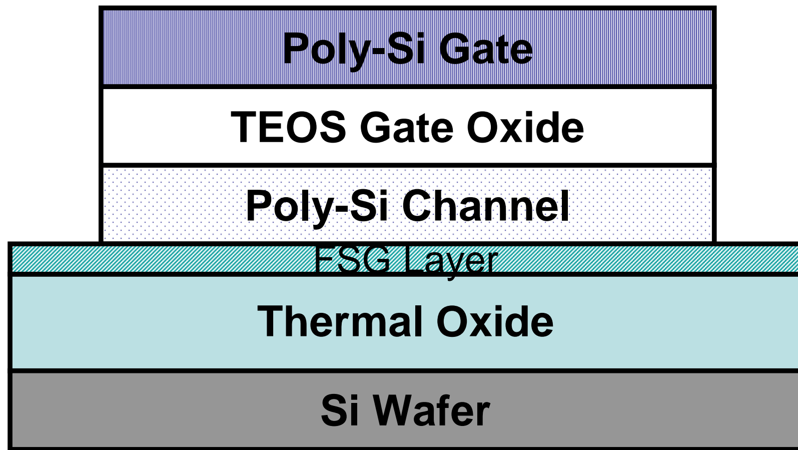
(b) FSG layer deposition by PE-CVD.



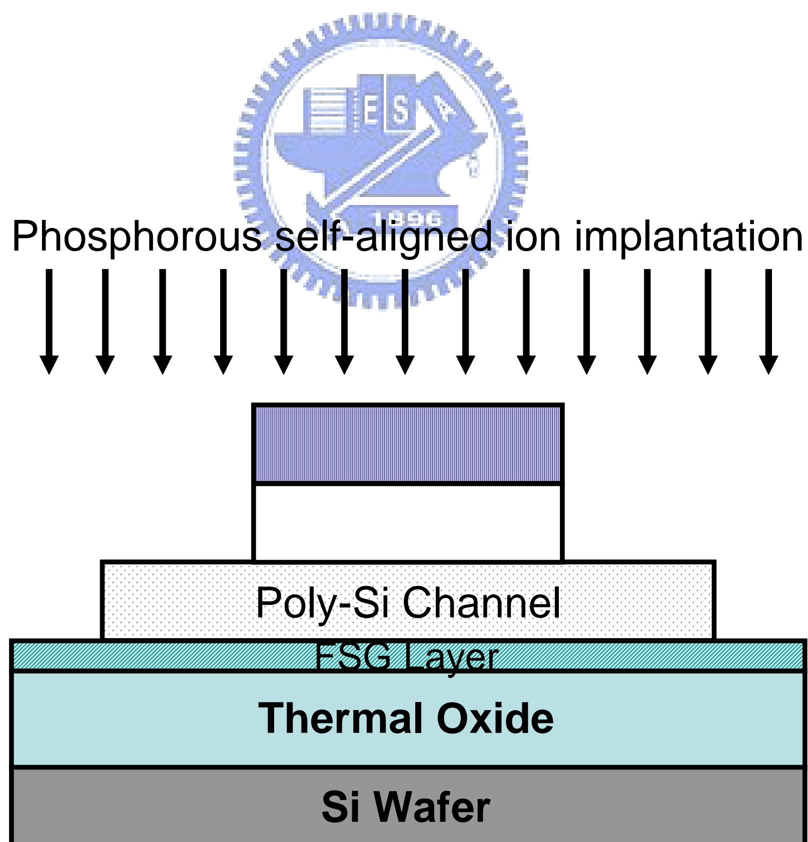
(c) Amorphous Si (a-Si) deposition by LPCVD.



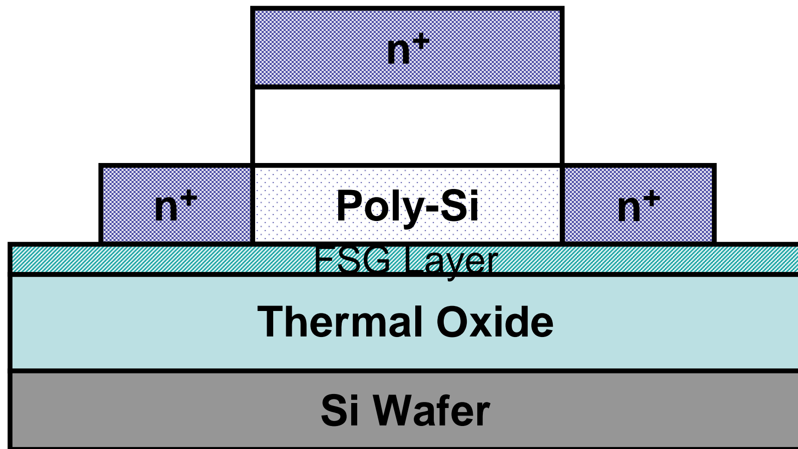
(d) Recrystallization of a-Si into poly-Si by ELA and defining active region d.



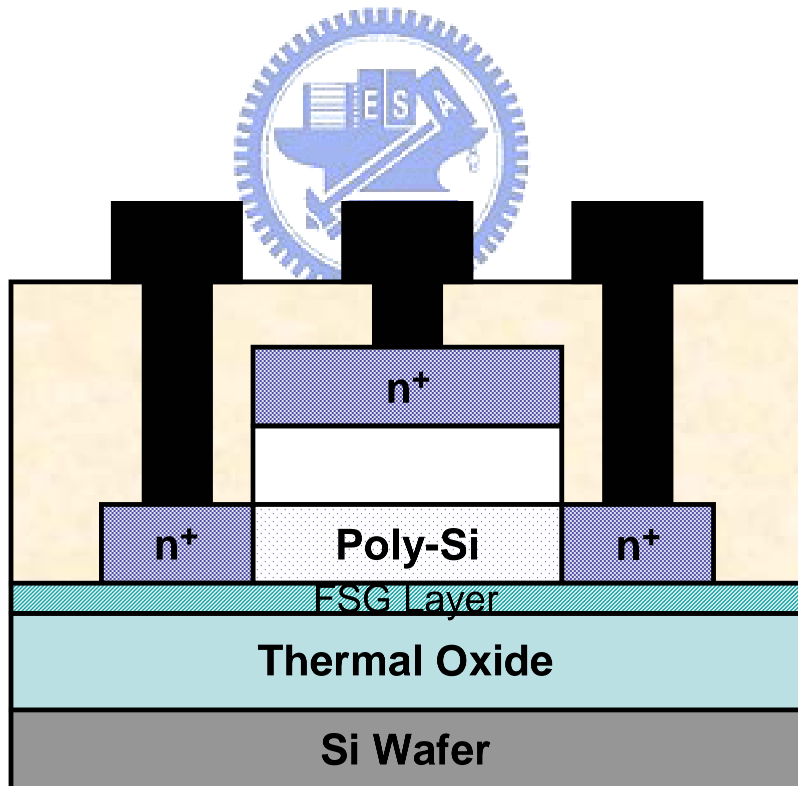
(e) Deposition of TEOS gate oxide and poly-Si gate.



(f) Defining gate electrode and self-aligned phosphorous ion implantation.



(g) Dopant activation by ELA.



(h) Deposition of passivation oxide, opening contact holes and defining metal pads.

Fig. 4.1 Schematic diagram of the fabrication process for the proposed poly-Si TFTs with a FSG buffer layer.

Table 4.1 Conditions of gas flow rates to deposit FSG buffer layers.

Sample \ Gas	CF_4	N_2O	SiH_4
Control	0	90	5
FSG1	10	90	5
FSG2	20	90	5
FSG3	40	90	5

Unit : sccm

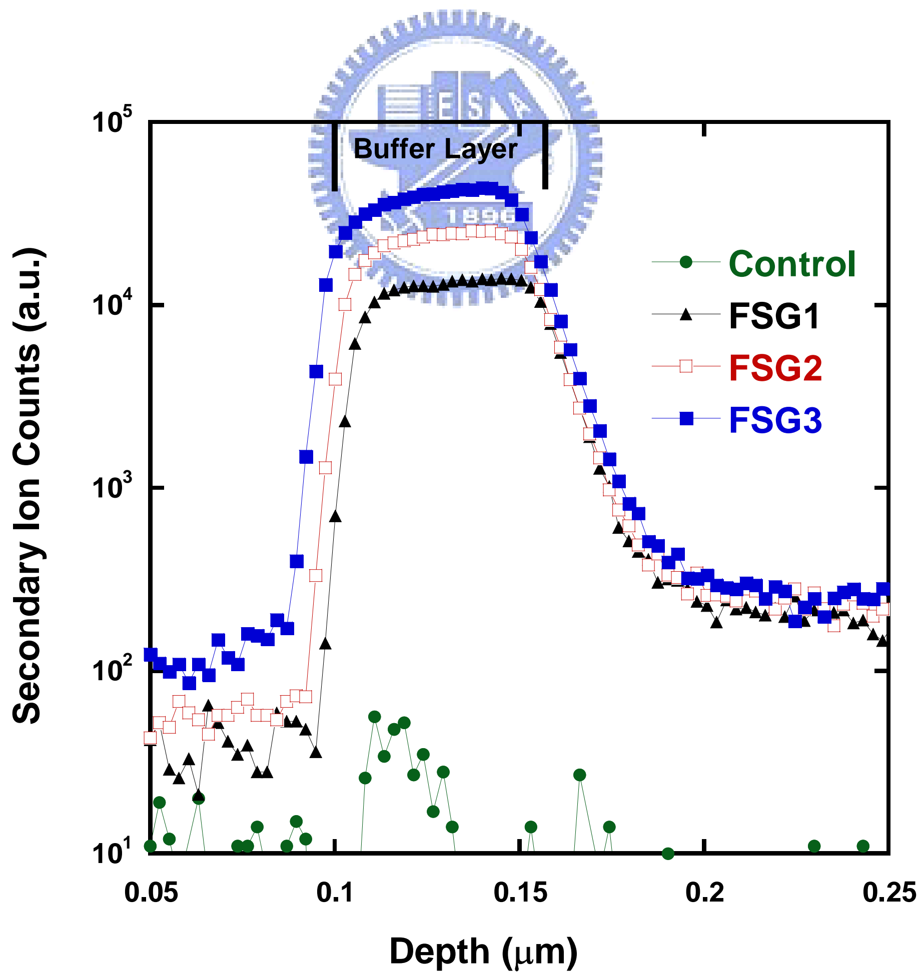


Fig. 4.2 SIMS profiles of the as-deposited FSG samples.

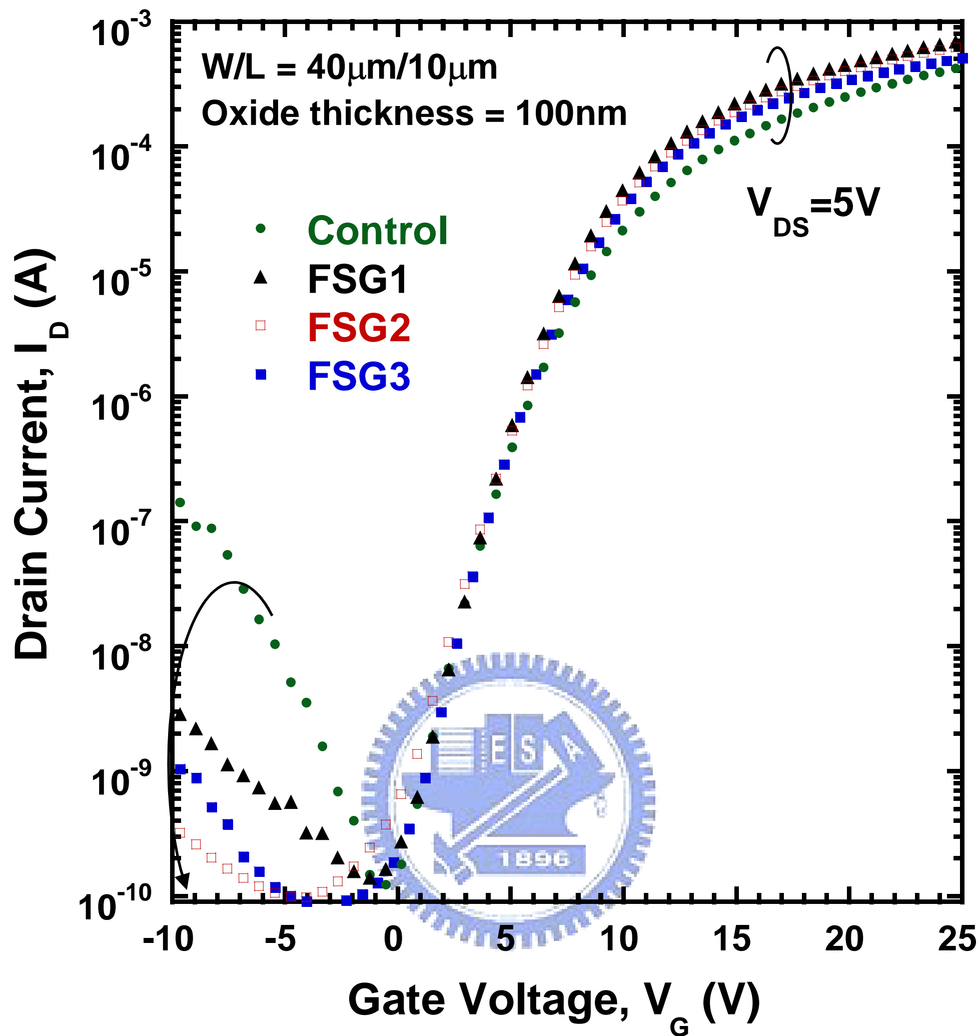


Fig. 4.3 Transfer characteristics of the conventional and the proposed poly-Si TFTs with different FSG layers.

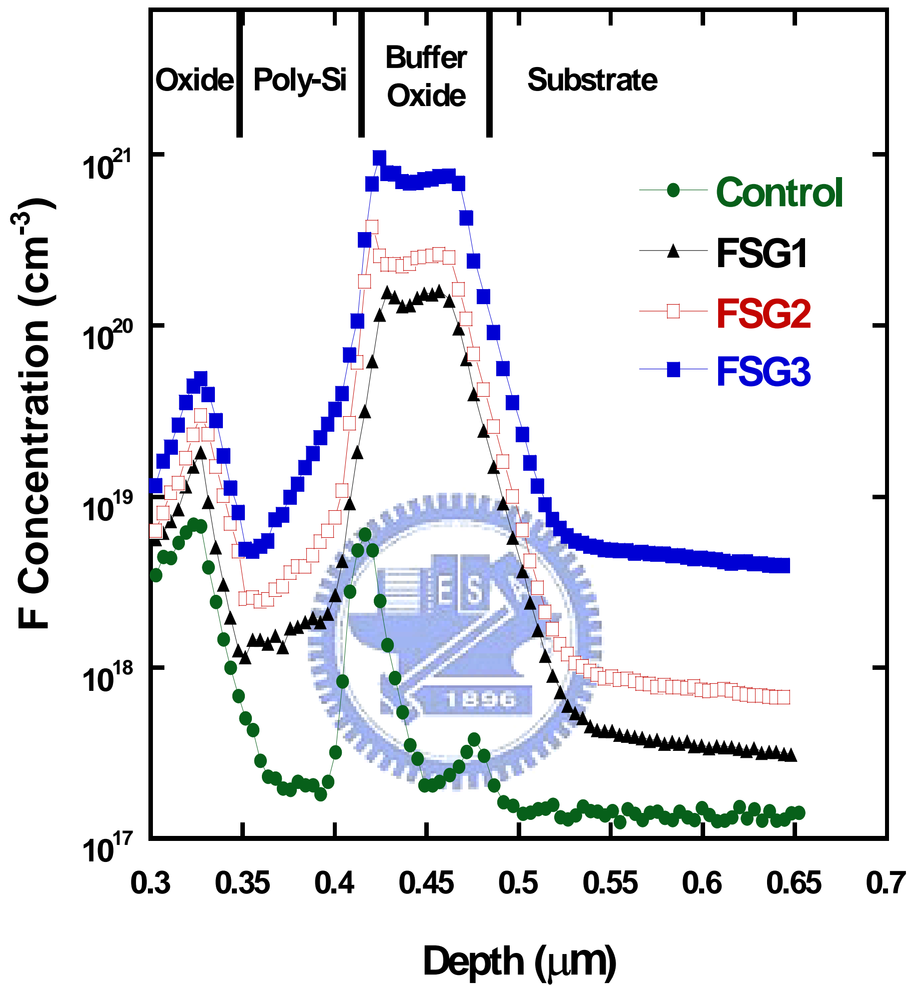


Fig. 4.4 SIMS profiles of the conventional and the proposed poly-Si TFTs with different FSG layers.

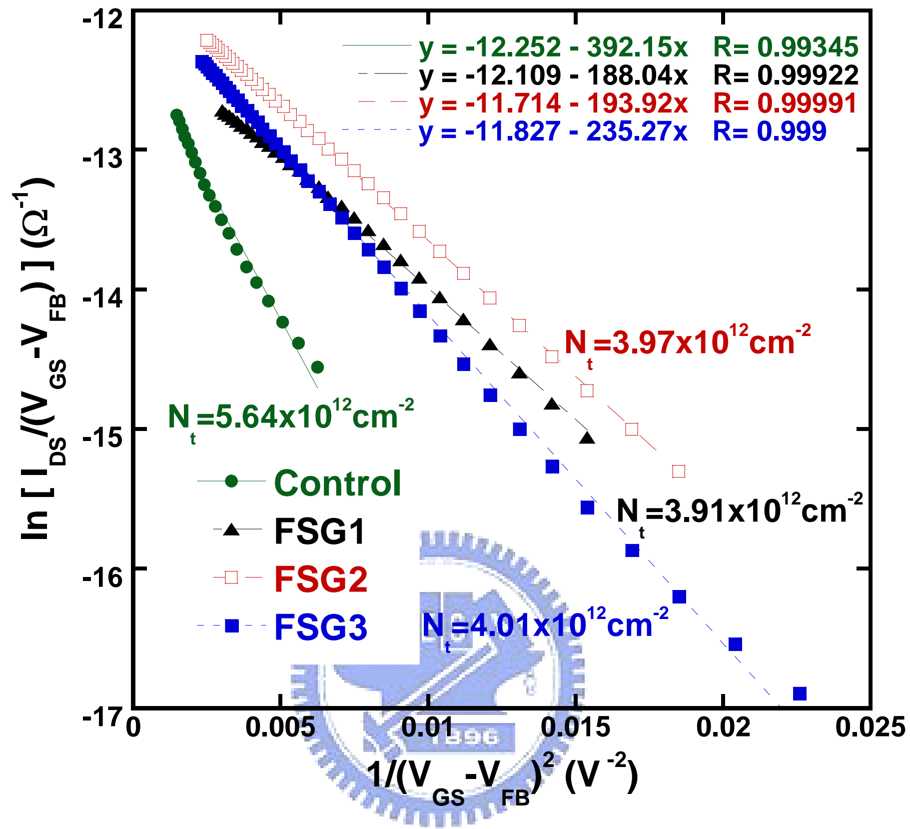
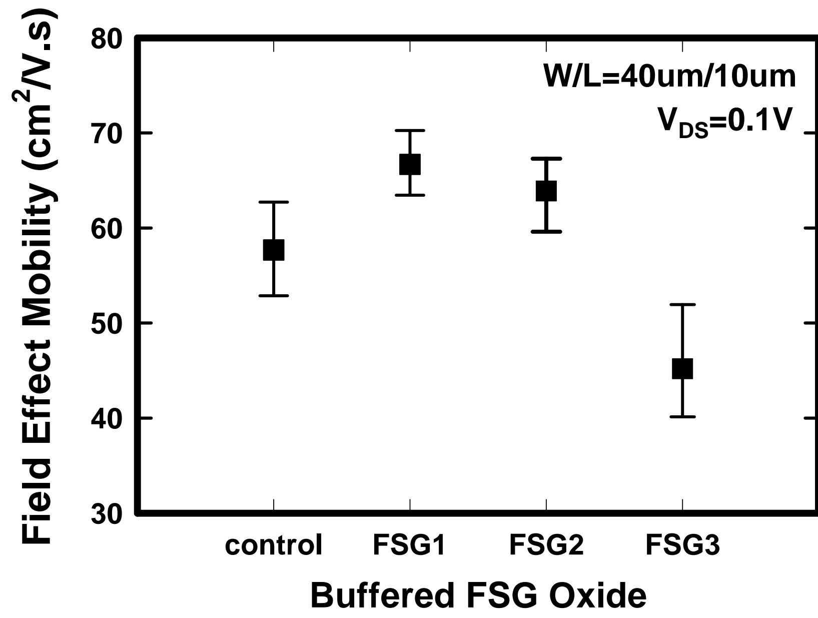


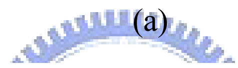
Fig. 4.5 Trap state density extraction of the conventional and proposed poly-Si TFTs with different FSG layers.

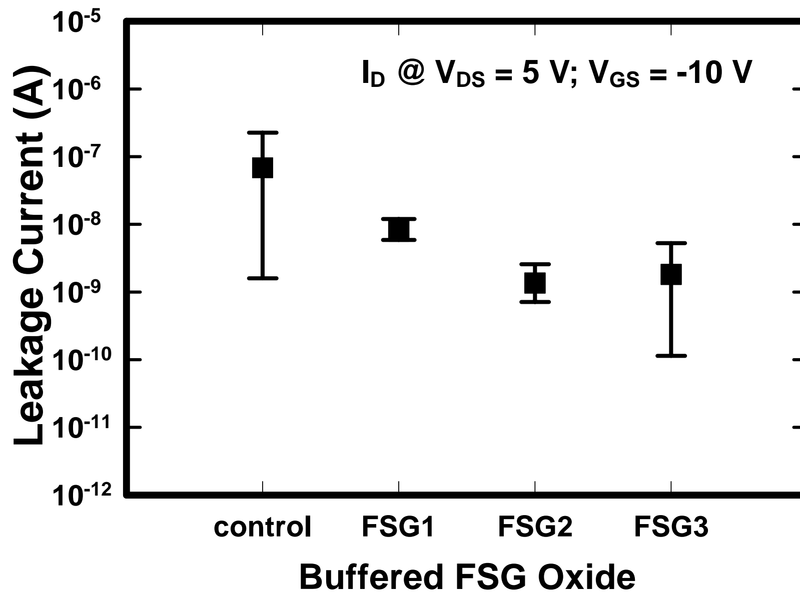
Table 4.2 Comparison of device characteristics of the conventional and the proposed poly-Si TFTs (W/L = 40 μ m/10 μ m).

Poly-Si TFTs	Control	FSG1	FSG2	FSG3
V_{th} (V)	5.07	4.77	4.82	4.96
S.S (V/dec.)	1.55	1.42	1.44	1.45
μ_{eff} (cm2/Vs)	57.5	69.1	65.4	43.1
Maximum I_{on} (A)	4.33×10^{-4}	7.01×10^{-4}	6.39×10^{-4}	5.11×10^{-4}
Minimum I_{off} (A)	1.45×10^{-10}	1.12×10^{-10}	9.73×10^{-11}	8.79×10^{-11}
On/Off Ratio	2.98×10^{6}	6.26×10^{6}	6.56×10^{6}	1.12×10^{6}
I_{off} @ V_G = -10V(A)	1.14×10^{-7}	3.08×10^{-9}	3.32×10^{-10}	9.95×10^{-10}
N_T(cm-2)	5.64×10^{12}	3.91×10^{12}	3.97×10^{12}	4.01×10^{12}



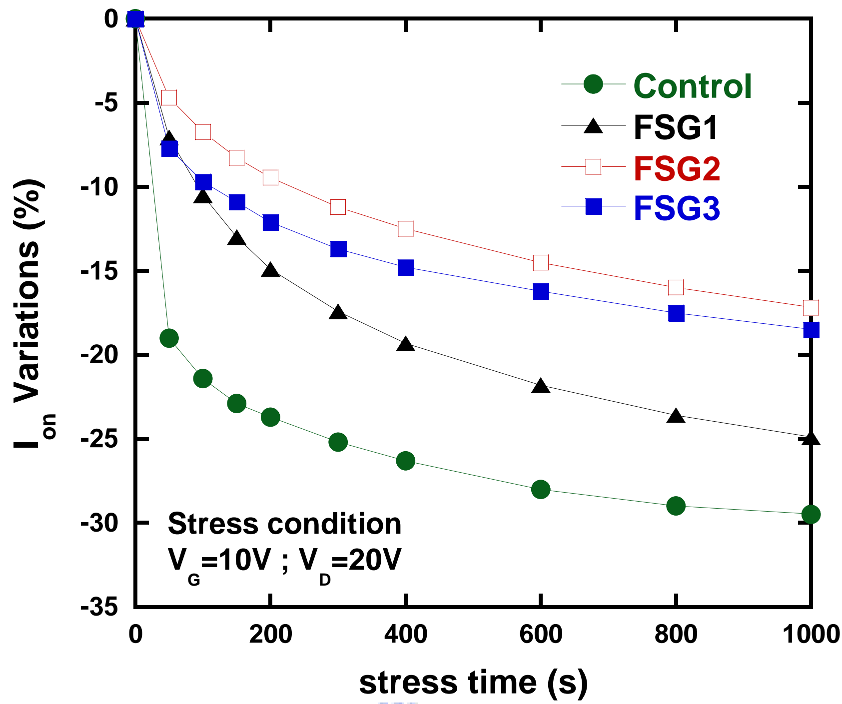
(a)



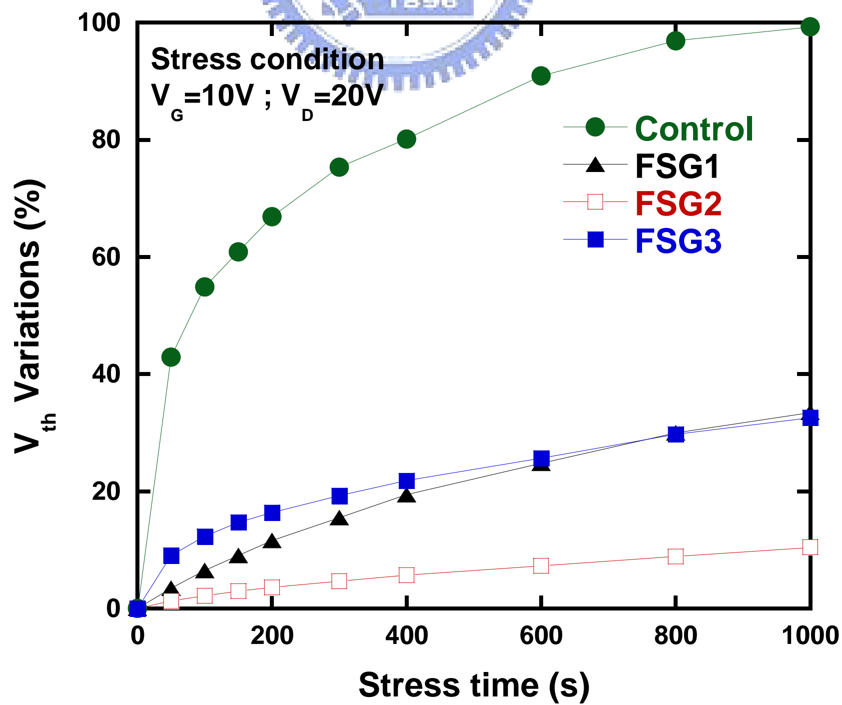


(b)

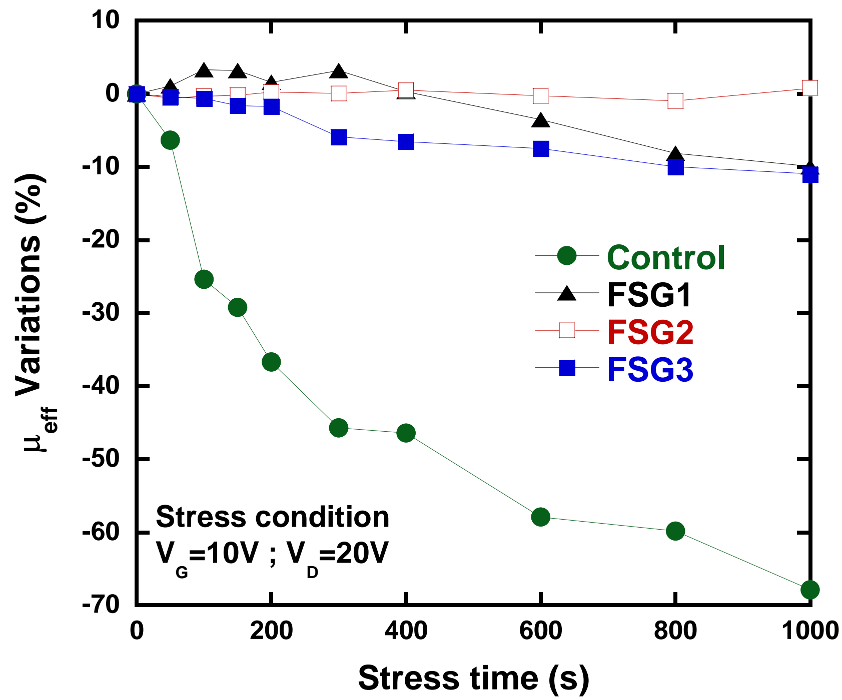
Fig. 4.6 Distribution of (a) filed-effect mobility and (b) leakage current of the poly-Si TFTs on different buffer layers. The vertical bars indicate the minimum and maximum values of the device characteristics and the squares are the average values.



(a) On-current degradation with stress time



(b) Threshold voltage degradation with stress time



(c) Field-effect mobility degradation with stress time

Fig. 4.7 (a) On-current, (b) threshold voltage and (c) field-effect mobility degradation as a function of stress time under hot-carrier stress.

Chapter 5

Drain/Gate-Voltage-Dependent On-Current and Off-Current Instabilities in Poly-Si TFTs under Electrical Stress

5.1 Introduction

Poly-Si TFTs have higher driving current and greater carrier mobility compared with conventional a-Si TFTs [1] [2]. However, due to low-temperature processes, numerous defects in grains and grain boundaries of the poly-Si channel degrade device characteristics. Traps resulted from these defects raise the potential barrier for carrier transport in the On-state and enhance the leakage current by the field-enhanced emission in the Off-state [3], [4]. Moreover, these defects are also responsible for the instability of device characteristics, particularly under electrical stress tests [5]. It is known that studying the instabilities in the device characteristics of poly-Si TFTs is more complicated than doing that in single-crystal metal-oxide-semiconductor field-effect transistors (MOSFETs), which is due to the random distribution of grain boundaries in the poly-Si and the poor quality of the gate oxide as well as the oxide/poly-Si interface. From the previous reports in studying single-crystal MOSFETs, we believe that the amounts and the spatial distributions of the trap states (or charges) in the gate oxide and in the poly-Si play important roles in the instabilities of poly-Si TFTs.

On-current (I_{on}) and Off-current (I_{off}) are two of the most important parameters in designing poly-Si TFT circuits, which are related to the driving capacity and the

charge storage. Also, they are very sensitive to the oxide trap charges and trap states (or charges) in the poly-Si. Their instabilities, with regard to the electrical stress, have constrained poly-Si TFT applications. Although several groups have studied the variations in the device characteristics of poly-Si TFTs in the On-state or Off-state after the electrical stress separately, a comprehensive mechanism for the degradation of both I_{on} and I_{off} under various stress conditions is not yet well known [6]-[8].

In this chapter, we adopt a new strategy for investigating the mechanism of the I_{on} and I_{off} instabilities in poly-Si TFTs. On the basis of correlations between the trap states (or charges) and the applied drain/gate voltages, the effects of the trap states (or charges) on the variations of I_{on} and I_{off} are investigated. From systematic measurements, a comprehensive model is proposed, which thereby extends our understanding of the correlation between the defects and the instabilities of device characteristics in poly-Si TFTs.

5.2 Experimental

The device structure used in this study is illustrated schematically in Fig. 5.1(a). N-channel non-LDD (non-lightly-doped-drain) excimer-laser-annealed poly-Si TFTs were used in this study. First, a 100-nm-thick amorphous silicon layer was deposited on a thermally oxidized Si wafer by LPCVD. Subsequently, a semi-Gaussian-shaped KrF excimer laser with a wavelength of 248 nm was used to induce phase transformation. Individual active regions were then patterned and defined. After a 100-nm-thick TEOS oxide was deposited by PECVD at 350°C, a 200-nm-thick poly-Si film was deposited and patterned. Next, a self-aligned phosphorous ion implantation was conducted at a dose of 5×10^{15} cm^{-2}. The dopant was activated by excimer laser annealing, followed by ammonia plasma hydrogenation. A passivation

oxide was then deposited and contact holes were defined. Finally, a 500-nm-thick Al electrode was deposited and patterned.

The gate width and length of the devices investigated in this study were 40 μm / 8 μm, respectively. The average grain size of the poly-Si is approximately 300 nm. Figure 5.1(b) shows the transfer curves of the poly-Si TFT before electrical stress. The electrical stress conditions were applied at various stress gate voltages ($V_{G,stress}$), with a fixed stress drain voltage ($V_{D,stress}$) of 20 V and a grounded source for 1000 s. I_{on} and I_{off} were defined at a drain voltage of 5 V and gate voltages of 25 V and -7 V, respectively. The variations in I_{on} and I_{off} were defined as $(I_{on,stress} - I_{on,0})/ I_{on,0} \times 100$ % and $(I_{off,stress} - I_{off,0})/ I_{off,0} \times 100$ %, where $I_{on,0}$, $I_{on,stress}$, $I_{off,0}$ and $I_{off,stress}$ are the currents measured prior to and after the electrical stress.

5.3 Results and Discussion

Figure 5.2 shows plots of the variations in I_{on} with various stress conditions. As can be seen, while $V_{G,stress} < V_{th}$, the channel is not formed yet and therefore a slight current leads to little damage under these stress conditions; consequently, minimal degradation of I_{on} can be observed. As $V_{G,stress}$ increases, the device will be turned on and operate in the saturation mode. Then, carriers are greatly accelerated by the lateral electric field and become "hot". Subsequently, the impact-ionization phenomenon occurs, which is also called drain-avalanche-hot-carrier (DAHC) injection. Numerous hot carriers are generated, which damage the device and create a substantial amount of trap states or charges (negative) near the drain region, degrading I_{on}. For $V_{G,stress}$ larger than 15 V, the electric field near the drain region decreases with increasing $V_{G,stress}$ and the acceleration of carriers drops. Thus, the degradation of I_{on} is small.

In the poly-Si TFT's channel, defects in grain boundaries and intra-grains would

trap carriers and form potential barriers, affecting the current transport [9]-[11]. During the DAHC injection, more trap states (acceptor-like) or negative charges are created, raising the barrier height [12]-[14]. Therefore, serious degradation on I_{on} can be observed clearly. Figure 5.3 shows plots of the potential barrier for carrier transport induced by filled negative trap states (or negative charges) in the poly-Si channel. It is worth noting that the trap states (or charges) created by DAHC are crowded near the drain region, not distributed uniformly throughout the entire channel. To evaluate the increase in the number of trap states in the poly-Si channel after electrical stress, the trap state density (N_T) was calculated from the square root of the slope of the $\ln(I_D V_{DS}/V_{GS})$ versus $1/V_{GS}^2$ plots, which was proposed by Proano *et al.* [15]. The N_T for the sample before stress is approximately 4.04×10^{12} cm^{-2}. After electrical stress, the N_T for samples with $V_{G,stress}$ = 0 V, 5 V, 7.5 V, 10 V and 20 V are 4.67×10^{12}, 5.72×10^{12}, 6.07×10^{12}, 5.70×10^{12}, and 5.12×10^{12} cm^{-2}, respectively. These results therefore indicate that DAHC most seriously damages poly-Si TFTs, which is consistent with the observation in other reports [12]-[14].

Considering that I_{off} is associated with the amount of defects or traps in the drain depletion region, the schematic diagram of the depletion region and the corresponding energy band diagram of the drain in the Off-state are shown in Fig. 5.4. The generation of I_{off} is attributed to thermionic emission at a low electric field and the field-enhanced emission (*i.e.*, F-P emission or trap-assisted band-to-band tunneling) at a high electric filed [4]. Hence, the magnitude of the electrical field and the amount of traps within the drain depletion region are the two important factors considered in studying the variations in I_{off}. On the basis of these inferences, the instabilities of I_{off} in poly-Si TFTs after electrical stress are investigated. Figure 5.5 shows the variations of I_{off} under various $V_{G,stress}$ with a fixed $V_{D,stress}$ of 20 V for 1000 s. As can be seen, while $V_{G,stress}$ is small, I_{off} is reduced after the stress. This is because some positive

charges are created in the poor-quality gate oxide (PE-TEOS oxide) near the drain. These positive oxide charges lower the local electric field in the drain depletion region. The electric field near the drain side before and after the creation of positive oxide charges is schematically depicted in Fig. 5.6. The positive oxide charges lift the electric field in the gate oxide but reduce that in the poly-Si. Thus, the reduction of the local electric field in the drain depletion region decreases I_{off}. However, as $V_{G,stress}$ increases, the DAHC-induced damage in the drain depletion region dominates the variation of I_{off}, leading to the marked increase in I_{off}. For $V_{G,stress}$ larger than 15 V, the variation of I_{off} decreases, which is due to the reduction of the impact ionization with increasing $V_{G,stress}$.

Now we know that for poly-Si TFTs in the On-state, I_{on} is strongly affected by the barrier height raised by the trap states (or charges) in the poly-Si channel. In the Off-state, the magnitude of the electric field and the amount of traps near the drain side are the two main factors determining the instability of I_{off}. To further investigate the effects of these trap states (or charges) and the oxide charges on the instabilities of I_{on} and I_{off}, a new strategy based on the correlations between the trap states (or charges) and the applied drain/gate voltages was adopted. Figure 5.7 shows the schematic diagrams of the experimental processes. I_{on} and I_{off} were measured and compared before and after subjection to various electrical stress conditions with the same stress time of 1000 s by applying different drain or gate voltages. Figure 5.8 shows ΔI_{off}, defined as $I_{off,stress} - I_{off,0}$, as a function of drain voltage (V_{DS}). As can be seen, when V_{DS} is low, a very slight ΔI_{off} is observed, which can be attributed to thermionic emission. The ΔI_{off} becomes larger for $V_{DS} > 6$ V because field-enhanced emission dominates. For the curve of $V_{G,stress} = 0$ V, we found that the positive charges in the gate oxide reduce the local electrical field in the poly-Si and make ΔI_{off} negative. However, as the drain depletion region increases with V_{DS}, the number of trap sites in

the depletion region also increases and thus the curve shows a turnaround point near V_{DS} = 11 V. For the curve of $V_{G,stress}$ = 10 V, the dominance of DAHC-generated trap states increases ΔI_{off}. However, for the curve of $V_{G,stress}$ = 20 V, ΔI_{off} remains nearly unchanged. In fact, under this stress conditions ($V_{G,stress}$ = $V_{D,stress}$ = 20 V), although not shown, the degradation of the subthreshold swing is more severe than that of I_{on} and I_{off}. The main mechanism involves the creation of interface states and intra-grain defects [7]. Under this high current stress, some weak bonds (Si-H bonds) are broken by the self-heating phenomenon, generating interface states at the oxide/poly-Si interface [16], [17]. Notably, these states distribute uniformly throughout the channel, rather than accumulating near the drain side. Therefore, ΔI_{off} shows a weak dependence on the drain voltage.

Figure 5.9 shows plots of the variations of I_{on} as a function of drain voltages under three stress conditions. As can be seen, increasing the drain voltage increases I_{on}. This result reveals that the increasing V_{DS} reduces the potential barrier established by the trap states (or charges) near the drain side, minimizing the effects of traps on the transport of carriers [3], [18]. This drain-induced trap state barrier lowering phenomenon is schematically depicted in Fig. 5.10. For $V_{G,stress}$= 0 V, the variations in I_{on} become positive for V_{DS} > 8V. This implies that after the trap-induced barrier is reduced with increasing V_{DS}, the positive charges in the gate oxide govern the increase in the variation of I_{on}, making the variations of I_{on} positive. For the curve of $V_{G,stress}$= 10 V, the numerous traps created by DAHC lead to a large degradation of I_{on}. However, for the curve of $V_{G,stress}$ = 20 V, I_{on} remains unchanged, because the distribution of the interface states is uniform throughout the channel. Moreover, by measuring the dependence of the variations of I_{on} on the drain voltage, one can also monitor the positions of the traps distributed in the poly-Si channel. For example, the variations of I_{on} measured at low a V_{DS} reveal the effect of the traps located near the

drain side. In contrast, the variations of I_{on} measured at a high V_{DS} reveal the effect of the traps located toward the channel. As can be seen in Fig. 5.9, for $V_{G,stress}$=10 V, a severe degradation of the variations of I_{on} is found at a low V_{DS}, which suggests that a substantial number of traps are generated near the drain side during DAHC stress. Comparing the three stress conditions, $V_{G,stress}$=10 V causes the most serious damage, which is distributed from drain to channel. However, for $V_{G,stress}$= 0 V, the damage is mostly located near the drain side. For $V_{G,stress}$= 20 V, the damage of interface states is distributed throughout the channel uniformly and the amounts are less than those caused by DAHC stress.

On the other hand, as we know, traps are generated in the poly-Si during the electrical stress. One considers that two types of traps are possibly created in the poly-Si channel of TFTs during the stress. One is the acceptor-like trap state; the other is the negative trap charge. The difference between them in terms of the potential barriers is shown in Fig. 5.11. For the negative trap charge, as V_{GS} increases, the potential barrier for carriers is simply suppressed. However, for acceptor-like trap states, the amount of trap charges depends on the position of the Fermi level (E_F), and therefore the number of filled acceptor-like trap states increases with increasing V_{GS}. Thus, the potential barrier is strongly related to the applied V_{GS} and it does not decrease as fast as in the case of negative trap charges. On the basis of these inferences, the dependence of the variations of I_{on} on the applied gate voltage (V_{GS}) was investigated. Figure 5.12 shows the variations of I_{on} versus the drain voltage for various gate voltages under different stress conditions. As can be seen, all the I_{on} variations increased toward more positive values with decreasing V_{GS}. This implies that acceptor-like trap states dominated the I_{on} variations after stress. Therefore, the potential barrier raised by the filled acceptor-like trap states degrades I_{on} more seriously with increasing V_{GS}. Moreover, for the curve of $V_{G,stress}$ = 0 V, as shown in

Fig. 5.12(a), we found that at a low V_{GS} (few filled acceptor-like trap states) and a high V_{DS} (considerable drain-induced trap state barrier lowering), the positive charges in the gate oxide dominate and lead to the increase in I_{on}.

However, for the curve of $V_{G,stress}$ = 10 V, as shown in Fig. 5.12(b), the negative trap charges in the poly-Si dominate the variations of I_{on} at a small V_{DS}. We deduce that the DAHC injection damages the poly-Si and induces the breaking of weak bonds [14], [19], [20]. They are almost deep-level trap states and behave like negative trap charges, because they are less V_{GS} dependent than tail states at this high V_{GS}. It also reveals that those trap charges accumulate near the drain side, because they were found at low V_{DS}. In contrast, the acceptor-like trap states dominate at a high V_{DS}. These trap states are created in the channel region, which can be attributed to the generation of interface states. For the curve of $V_{G,stress}$ = 20 V, as shown in Fig. 5.12(c), the variations of I_{on} are dominated by the creation of acceptor-like interface states. However, these trap states do not affect I_{on} as strongly as DAHC-induced trap states do due to their uniform distribution throughout the channel. These interface states are created by high-current stress and self-heating, and show a weaker dependence on V_{DS}. At a small V_{GS}, the variations of I_{on} are positive. This is due to the positive charges in the gate oxide, which may have resulted from the evolved hydrogen under self-heating stress.

From these results, dissimilar variations of I_{on} and I_{off} after the electrical stress were observed. These results obtained in experiments yield a comprehensive model for device degradation in Fig. 5.13. At a low $V_{G,stress}$, a small current slightly damages the poly-Si and generates minimal acceptor-like trap states, leaving I_{on} almost unchanged. However, in this case, the reduction of the local electric field, caused by the trapping of positive charges in the gate oxide, reduces I_{off}. At a medium value of $V_{G,stress}$, many negative trap charges generated near the drain side dominate the

increase in I_{off} and the decrease in I_{on}, and also some acceptor-like trap states can be found in the channel region. As $V_{G,stress}$ becomes large, the dependence of I_{on} and I_{off} on the drain voltage is reduced because the high-current stress induces the generation of interface states uniformly throughout the channel.

5.4 Summary

The I_{on} and I_{off} variations of excimer-laser-annealed and hydrogenation-processed poly-Si TFTs under various static stress conditions have been studied. It is found that, under different values of $V_{G,stress}$, the degradations of I_{on} and I_{off} are very dissimilar. The reason for these results is believed to be due to a combination of different amounts of positive charges trapped in the gate oxide and trap states generated in poly-Si. In addition, the strong drain/gate voltage dependences of the variations in I_{on} and I_{off}, including trap-assisted tunneling and drain-induced trap state barrier lowering have also been observed clearly from our measurements. Finally, the models responsible for the degradation of I_{on} and I_{off} under various stress conditions were proposed.

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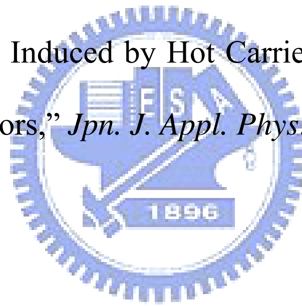
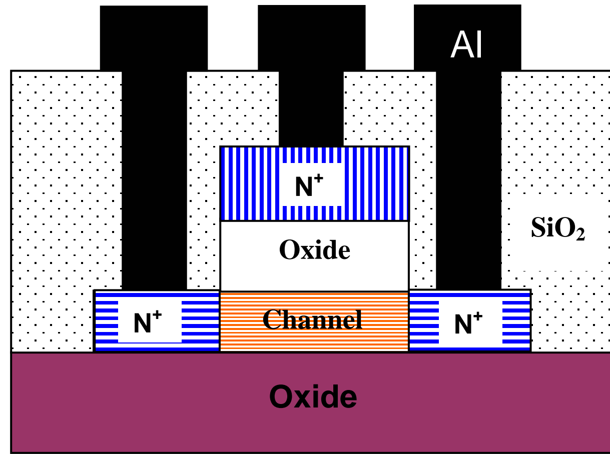
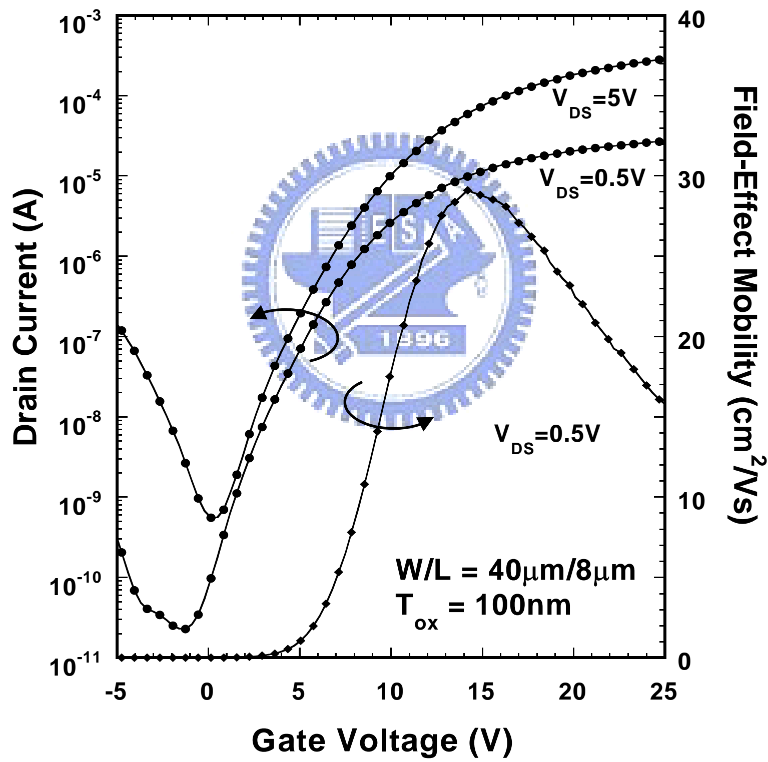




(a)



(b)

Fig. 5.1 (a) Schematic diagram of cross-sectional view of poly-Si TFT used in this study. (b) Transfer curves of poly-Si TFT before electrical stress.

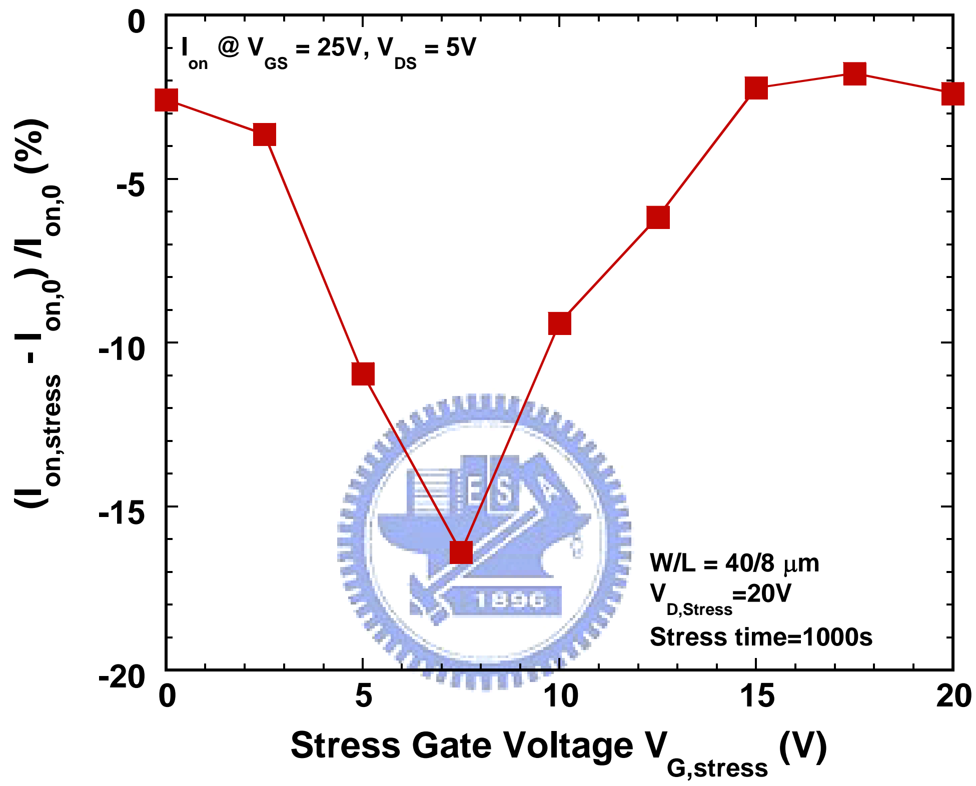


Fig. 5.2 Stress gate voltage dependence of I_{on} degradation of poly-Si TFTs.

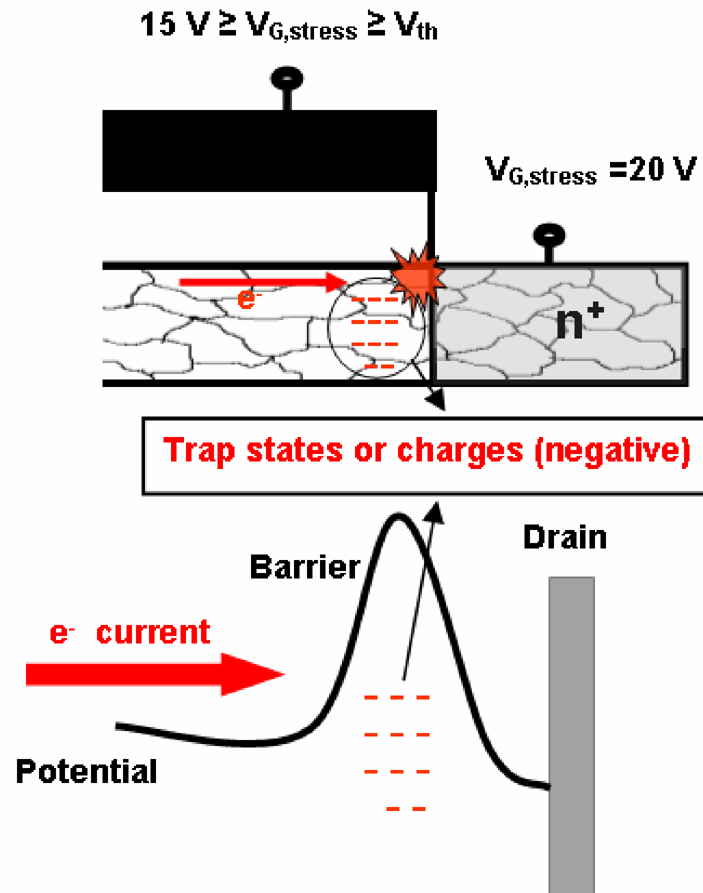


Fig. 5.3 Potential barrier for carrier transport raised by filled negative trap states (or charges) in poly-Si channel near drain.

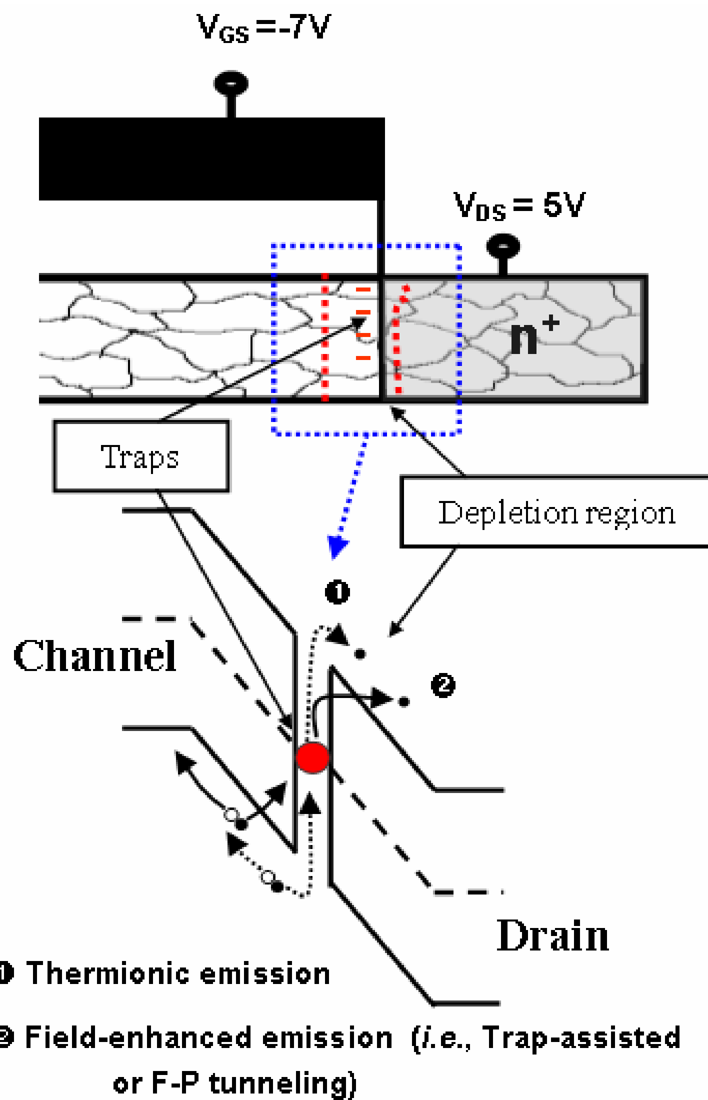


Fig. 5.4 Schematic diagram of traps in drain depletion region and corresponding energy band diagram of Off-stated poly-Si TFT.

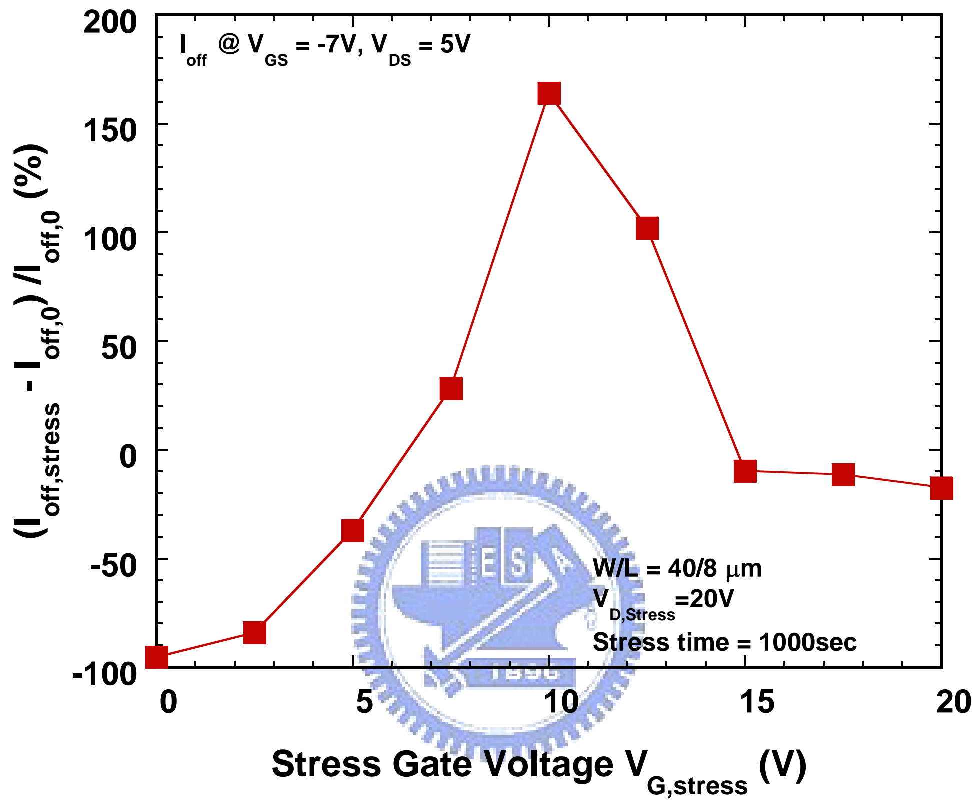


Fig. 5.5 Stress gate voltage dependence of I_{off} degradation of poly-Si TFTs.

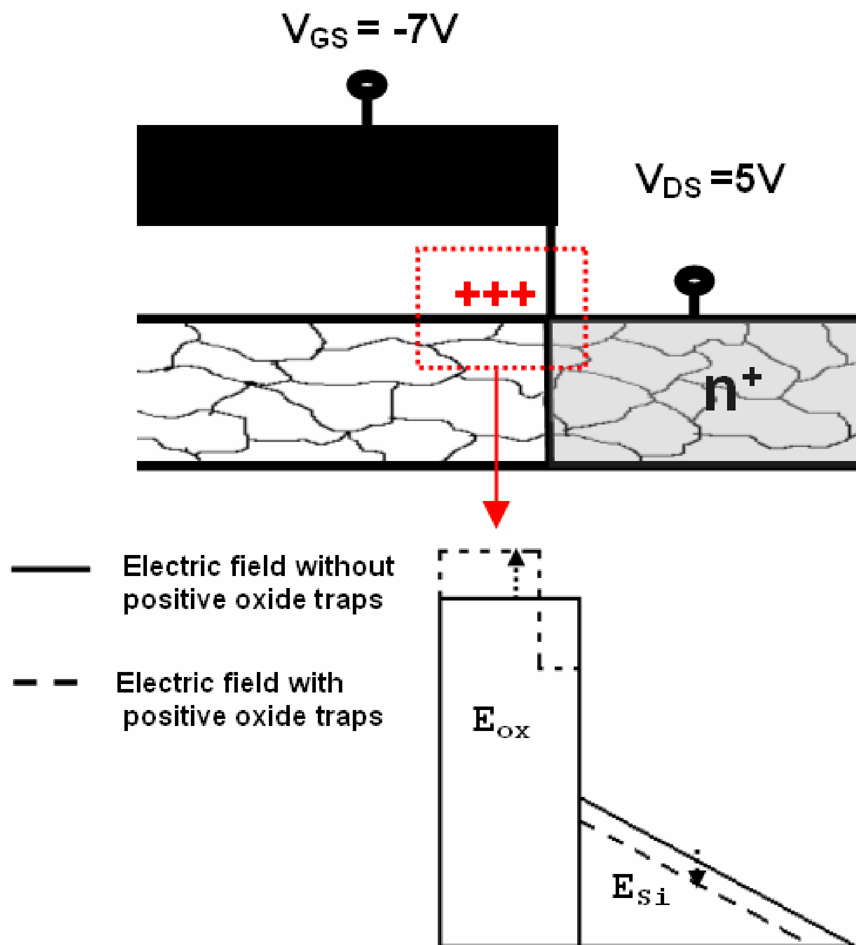


Fig. 5.6 Comparison of electric fields in gate oxide and poly-Si near drain before and after creation of positive oxide charges.

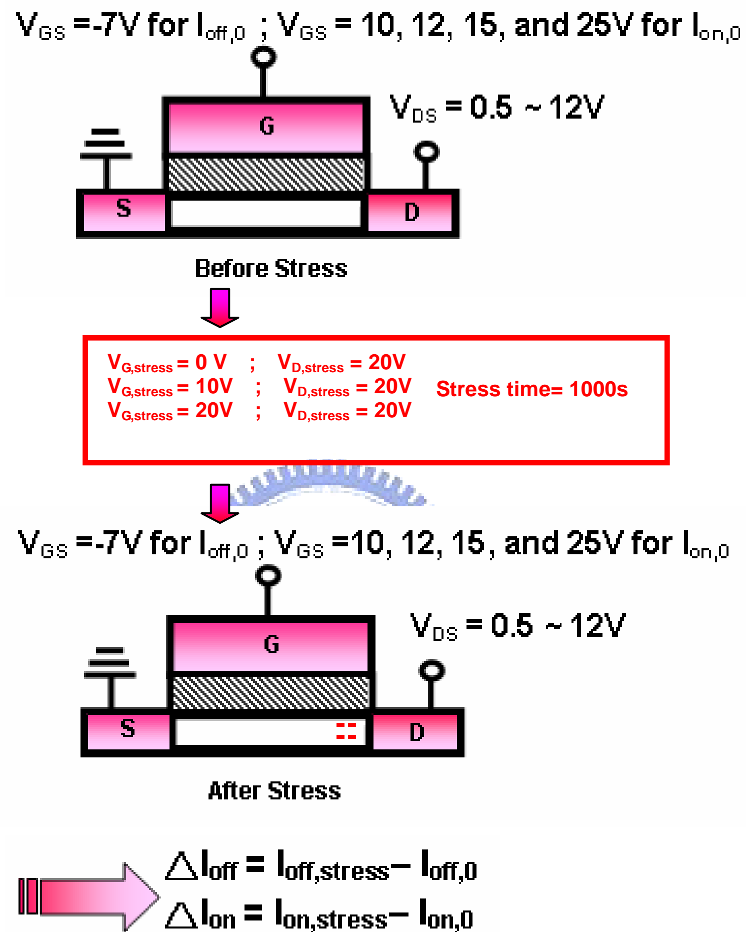


Fig. 5.7 Schematic diagram of our experimental processes. The variations in I_{on} and I_{off} were measured and compared before and after stress under various drain voltages.

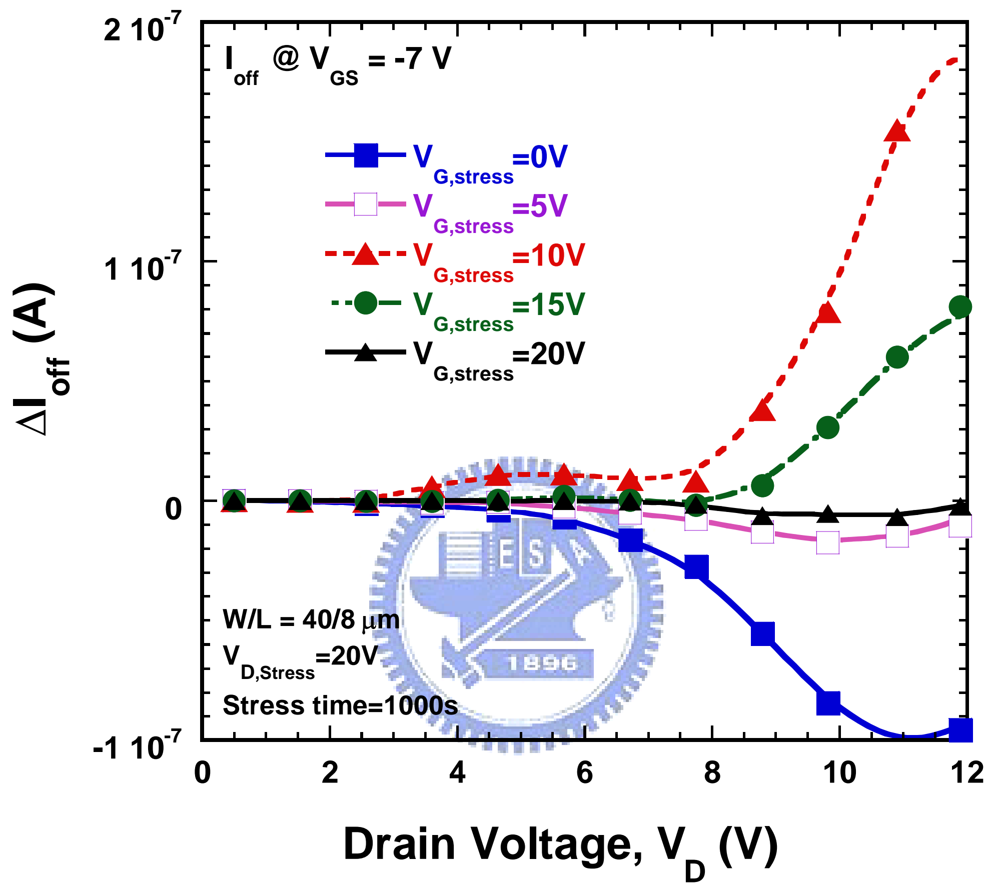


Fig. 5.8 Off-current differences vs. drain voltage under various stress conditions, where $\Delta I_{off} = I_{off,stress} - I_{off,0}$.

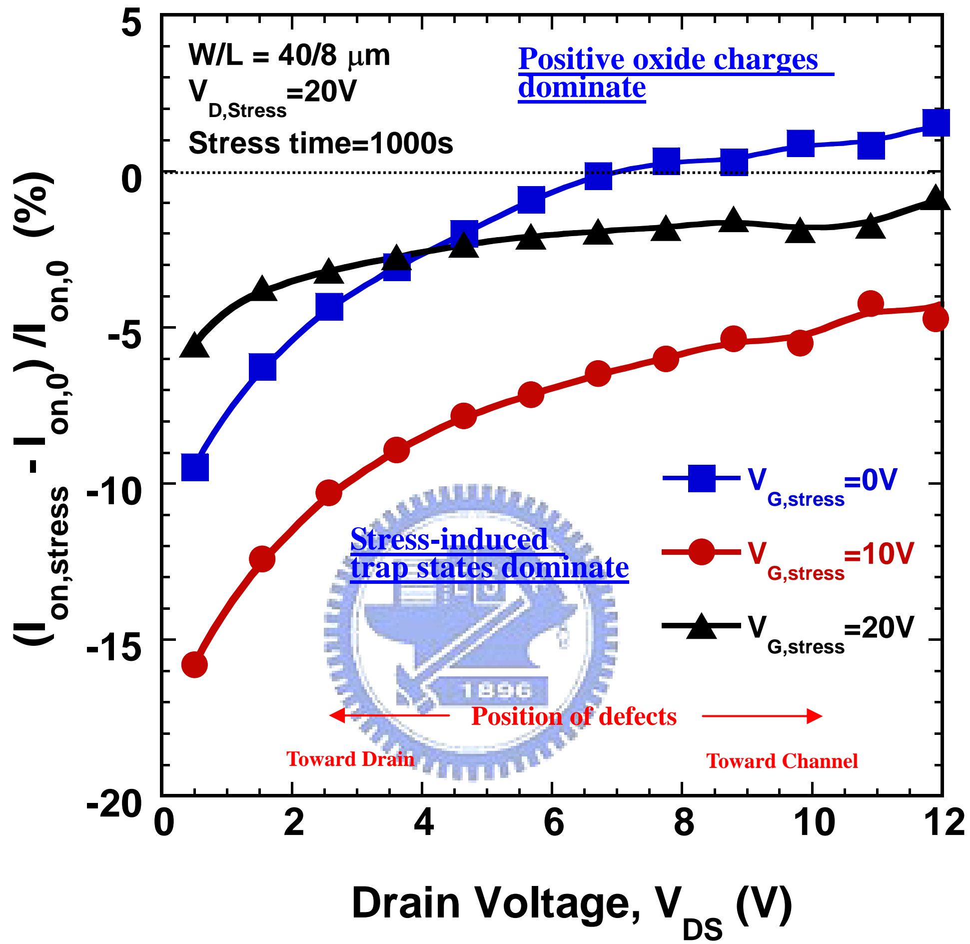


Fig. 5.9 On-current variations as a function of drain voltage under three stress conditions.

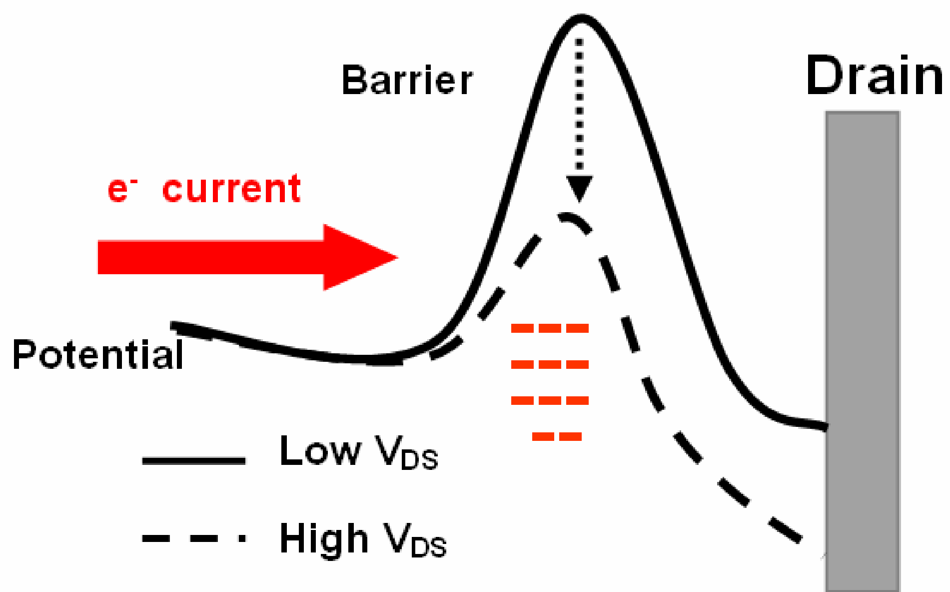


Fig. 5.10 Schematic diagram of effective potential barrier created by trap states near drain under different drain voltages.

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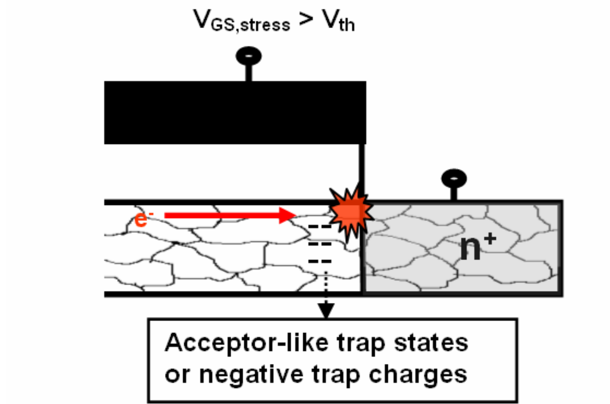


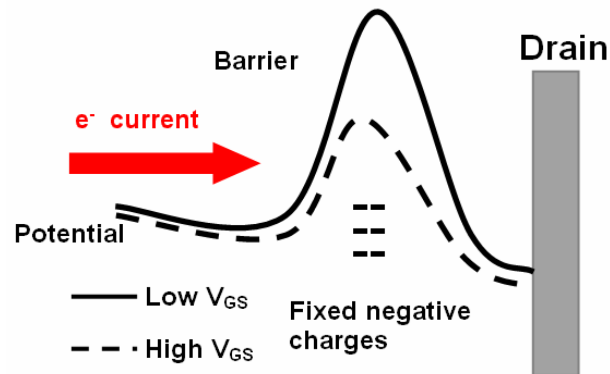


Fig. 11 (a)

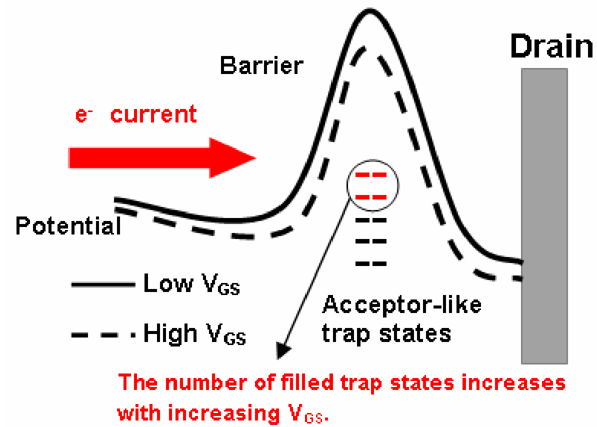
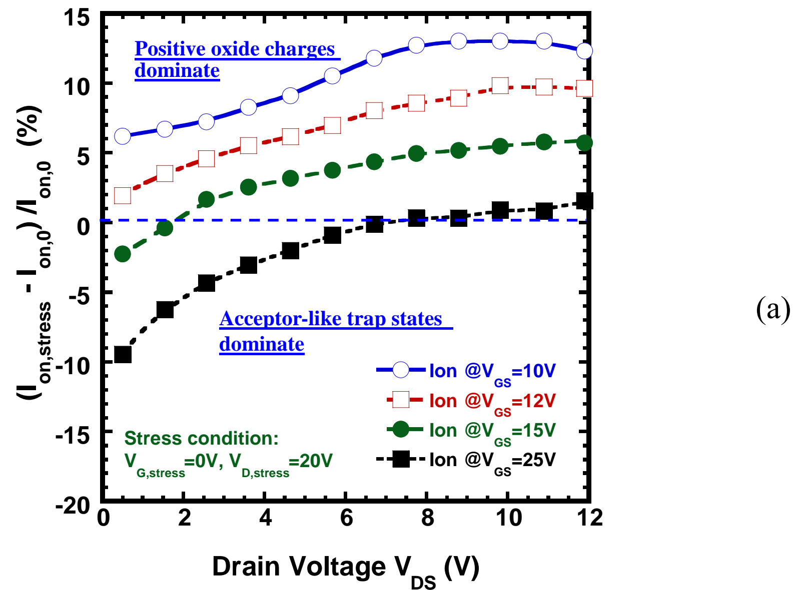
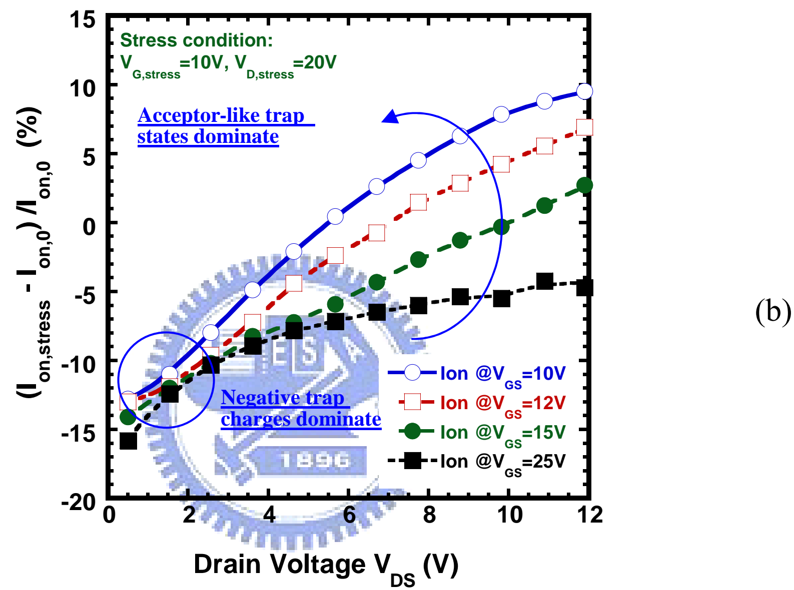


Fig. 11 (b)

Fig. 5.11 Comparison of effective potential barriers created by (a) fixed negative charges and (b) acceptor-like trap states.



(a)



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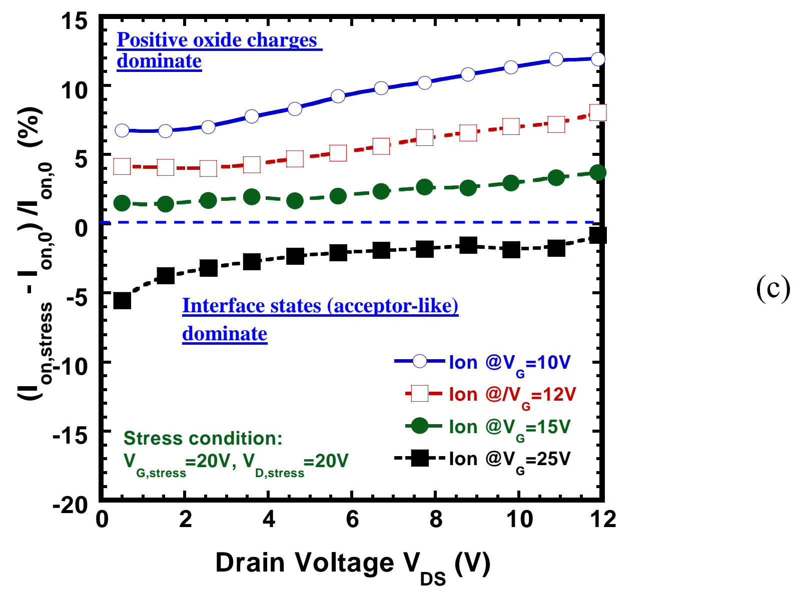

(c)

Fig. 5.12 Variations of I_{on} vs. drain voltage for various gate voltages under three stress conditions (a) $V_{G,stress}$= 0 V, (b) $V_{G,stress}$= 10 V and (c) $V_{G,stress}$= 20 V with $V_{D,stress}$ = 20 V.

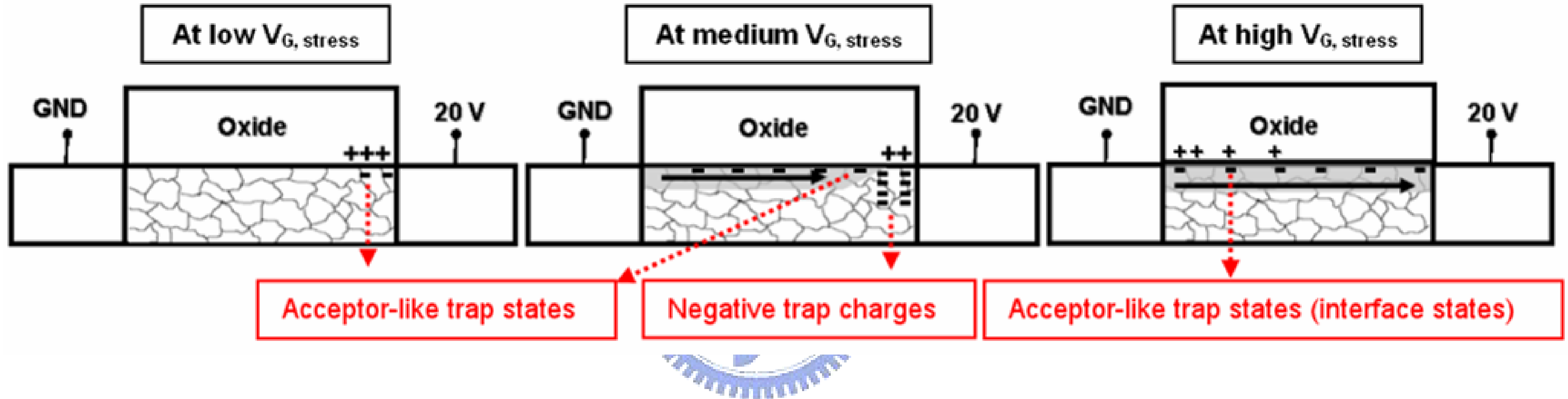

Fig. 13. Schematic diagram of device cross-sectional view under three types of stress conditions. Different amounts and spatial distributions of charges trapped in the gate oxide and trap states created in the poly-Si channel lead to different behaviors of the device degradation.

Chapter 6

Observation of Localized Breakdown Spots in Oxide Films using Scanning Capacitance Microscopy

6.1 Introduction

To achieve AMLCD panels with high resolution, high performance and good reliability poly-Si TFTs are required. However, due to the low process temperature in TFT fabrications, the oxide quality is one of the most critical concerns for device reliability. Also, to enhance the TFT's driving current and lower the device operating voltage, thinning the gate oxide thickness is another important approach. To date, many novel oxidation processes have been proposed to improve the thin oxide integrity, such as N_2O plasma oxide [1], O_2 plasma oxide [2], liquid phase deposited oxide [3] and electron cyclotron resonance (ECR) plasma oxidation [4], [5]. Besides TFT, the gate oxide thickness of MOSFETs has also been scaled down severely. Low temperature oxides are also required in deep submicron MOSFETs fabrications to further reduce the process thermal budget. Therefore, over the past decade, the thin oxide reliability has been a quite interesting subject of high international interest in both TFTs and MOSFETs investigations.

Conventionally, MOS capacitor structure is mostly used to gather the electrical information of thin oxide films including capacitance-voltage curves (C-V), current-voltage curves (I-V), and oxide breakdown phenomena. Currently and in future, oxide breakdown (OBD) is believed to be the most complicated issue in the

device reliability [6], [7]. The OBD phenomenon can be divided into three stages [8]. First, lots of defects are generated within localized regions in the oxide layer. This is called the wearout phase. Percolation paths then occur, which allow currents to leak through the oxide. Finally, large currents cause thermal damage and may induce OBD propagation. This OBD process is thought to be a local phenomenon within the nano-scale region, not occurring throughout the total oxide area [8], [9]. However, the conventional electrical measurements, made through MOS capacitors, can only detect general information about the whole oxide area under the electrode, and the localized OBD behavior is not mentioned. To characterize the localized OBD evens in detail, highly sensitive measurement tools with a good spatial resolution are necessary. However, conventional electrical measurements, made through MOS capacitors, can only detect general information about the whole oxide area under the electrode, and the localized OBD behavior is not mentioned.

Scanning capacitance microscopy (SCM) system, as shown in Fig. 6.1, combined with atomic force microscopy (AFM) is a powerful way to synchronously measure the differential capacitance (*dC/dV*) images and the corresponding topographic images of sample films. Due to its ability to measure two-dimensional (2-D) carrier concentration profiles with a nanometer-scale resolution, SCM can be employed to determine the effective channel length and interface defects distributions of devices [10]-[12]. In addition, SCM has also been used to study local charge trapping in oxides and dynamic device operation images [13], [14]. The schematic diagram of SCM scanning on a oxide sample to detect the defects or charge trapping regions of a oxide film is shown in Fig. 6.2. Thus, in this chapter, we demonstrate a technique for mapping OBD spots of oxide films using SCM with corresponding AFM images. For preliminary study, thermal oxides (40 Å) are used in this study. We believe this new

method can be adopted to further investigate the breakdown issues in low temperature oxides or other dielectric materials for future poly-Si TFT applications.

6.2 Experimental

Four in. diameter single-crystal (100) oriented p-type silicon wafers were used in this study. The wafers were chemically cleaned using standard RCA cleaning procedure, followed by wet oxidation in an atmospheric pressure furnace to form a 500-nm-thick oxide layer. The active regions were defined by photolithography and wet-chemical-etching. After a standard RCA cleaning process, a 40Å-thick SiO_2 layer was grown at 900°C in diluted O_2 ambient (N_2:O_2=10:1). Then, a 150-nm-thick poly-Si film was deposited using a low pressure chemical vapor deposition (LPCVD) system. Subsequently, phosphorous ion implantation was performed. The dosage was 5×10^{15} cm^{-2} and the energy was 40 KeV. The dopants were activated by a rapid thermal annealing (RTA) system in N_2 ambient at 1000°C for 30s. The n-type poly-Si was then defined to form the gate electrode. Finally, an aluminum film was deposited on the back side of the Si wafer to form the bottom electrode and to complete the MOS capacitor, as shown in Fig. 1(a). The capacitance-voltage (C-V) measurements were performed to measure the effective oxide thickness (EOT) of the oxide film by HP 4284 LCR meter. HP 4156B semiconductor parameter analyzer was used to measure the current versus voltage (I-V) curves and to produce OBD. Ramped voltages, form 0V to -10V, in -0.1 V steps were applied to trigger the OBD events. The current compliance limit was at 100 mA. After the occurrence of OBD, the poly-Si gate was removed by high-selectivity in a KOH solution (10%), to expose the oxide surface. A scanning probe microscope (Digital Instruments D5000) equipped with SCM scanner were used to examine these samples. SCM images with the corresponding AFM images were obtained. Schematic diagrams of the processes are shown in Fig. 6.3. For each oxide films, both with and without OBD, more than 50

samples were observed. The SCM scanner's conductive tips were commercial silicon tips coated with Cr-Co alloy. All the SCM images were acquired using the constant voltage mode, a DC bias of 0 V and an AC bias of 200 mV, at 89 kHz. The capacitance sensor of the SCM system is sensitive to a signal variation as small as 10^{-18} F.

6.3 Results and Discussion

The capacitance versus gate voltage (C-V) characteristic of the thin oxide film, measured from inversion to accumulation at a high frequency (1MHz) is shown in Fig. 6.4(a). An EOT of 4.06 nm could be estimated from the capacitance in the strong accumulation regime and the steeper slope indicates the good quality of the SiO_2/Si interface. The leakage current (I) of the MOS capacitors was measured with ramped-up gate voltages (V). The J-E curves can be calculated from I-V curves, where J = I / (area of the capacitors) and E = V / (EOT of the oxide). Figure 6.4(b) shows the J-E characteristics of MOS capacitors before and after OBD. As can be seen, there was a uniform result shown by different capacitors, which indicated a high breakdown field (~15 MV/cm) and a low leakage current (~10^{-6} A/cm^2 at Vg = -1 V). High-quality and uniform oxide films were obtained in this work. After I-V measurements, the poly-Si gates of the samples were removed and the samples were scanned by SCM.

Figures 6.5 (a) and (b) show the SCM images and the corresponding AFM image of the fresh oxide film. Fig 6.6 (a) and (b) show the SCM images and the corresponding AFM image of the oxide film with OBD occurring, respectively. As can be seen, the surface morphology of the oxide layer is still uniform after the occurrence of OBD. In other words, the OBD phenomena did not change the surface morphology of the thin oxide film. In Fig. 6.5 (a), one can see that constant *dC/dV*

signals were detected in the whole oxide region. This reveals that there were low interface-states and trap charges contained in this fresh oxide [13]. In comparison, three detectable spots with low *dC/dV* signals can be clearly seen in Fig. 6.6 (a). Obviously, these spots are not related to the corresponding surface roughness. We attribute it to localized OBD phenomena in the oxide layer. During the ramped voltage stressing, defects were generated in the oxide. When the critical defect concentration was reached, percolation paths occurred, which connected the anode and cathode of the capacitor. Such percolation paths are conductive, *i.e.* charges cannot be stored in these regions, which results in lower *dC/dV* signals. The other possible cause for the contrast difference is that localized charges collected in the oxide, which would cause a shift in the *dC/dV* signal [13]. However, when various DC biases were applied during the SCM measurement process, no changes in the magnitude of the low *dC/dV* signal were found. Therefore, this possibility can be eliminated. Fig. 6.7 (a) and (b) show the enlargement of SCM images for fresh oxide film and oxide film with a single OBD spot on another sample.

We also found that the number of OBD spots in the samples varied. As shown in Fig. 6.8, three OBD spots are imaged in another sample. This indicates that multiple OBD evens were triggered in this case. It can therefore be seen that SCM is a useful tool not only to map the precise position of OBD spots but also to gather the information about of OBD evens. Fig. 6.9 shows the roughness (rms values) distribution extracted form the corresponding AFM images in Fig. 6.7 (b). As can be seen, the OBD do not change of surface morphology of the thin oxide film. It is also worth noting that these OBD spots did not be further deteriorated and that no new spots were created during the SCM measurements process, because the DC voltage used in SCM can be as low as zero. This implies that using SCM to image OBD spots

is a more stable and reliable method as compared to the use of conductive-AFM [15]-[17].

As seen in Fig. 6.8, the sizes of the spots are different. We believe that thermal damage and OBD propagation caused this difference [4]. Figure 6.10 shows the enlarged SCM image and the cross-sectional view of an OBD spot. The center of the OBD spot has a very low *dC/dV* signal. The full-width-at-half-maximum (FWHM) of this OBD spot is approximately 12.6 nm. From our calculated experimental results, the diameters of the OBD spots (FWHM) vary from approximately 6 nm to 13.5 nm, which is consistent with the order of the magnitude reported in previous reports [11].

From experimental results above, we can clearly image the breakdown spots of oxide films using this technique, although thermal oxides were adopted preliminarily. Actually, low temperature oxides, deposited by PE-CVD using SiH_2 and O_2 gases, were also investigated. We found that the signals were too weak to be sensed because the thickness (200-500 Å) of these samples is too thick. This result infers that the SCM technique may be more suitable to investigate oxide films with thickness below 200 Å. Therefore, we believe this technique can be adopted to investigate the breakdown phenomenon of low temperature thin dialectic films to provide valuable information for future poly-Si TFT applications, such as plasma-grown oxide [1], [2], [4]. However, further study is still needed in this topic.

6.4 Summary

In this preliminary study, we have successfully employed SCM to investigate OBD spots on oxide films with a nanometer-scale resolution. The results reveal that such OBD spots are localized phenomena. After their formation, the oxide film's insulation properties change to conductive properties, resulting in lower *dC/dV* signals. The diameters of the OBD spots vary from approximately 6 nm to 13.5 nm.

According to the corresponding AFM images, the surface morphology after OBD changes little. Furthermore, due to the zero DC bias, we can avoid destroying the OBD spots or creating new spots. These advantages make SCM a very promising way to investigate OBD phenomena in low temperature oxides or other dielectric materials for future poly-Si TFT applications or other nanometer-scale devices. It can provide fruitful information about the OBD behavior in failure analysis of future TFTs or ICs.

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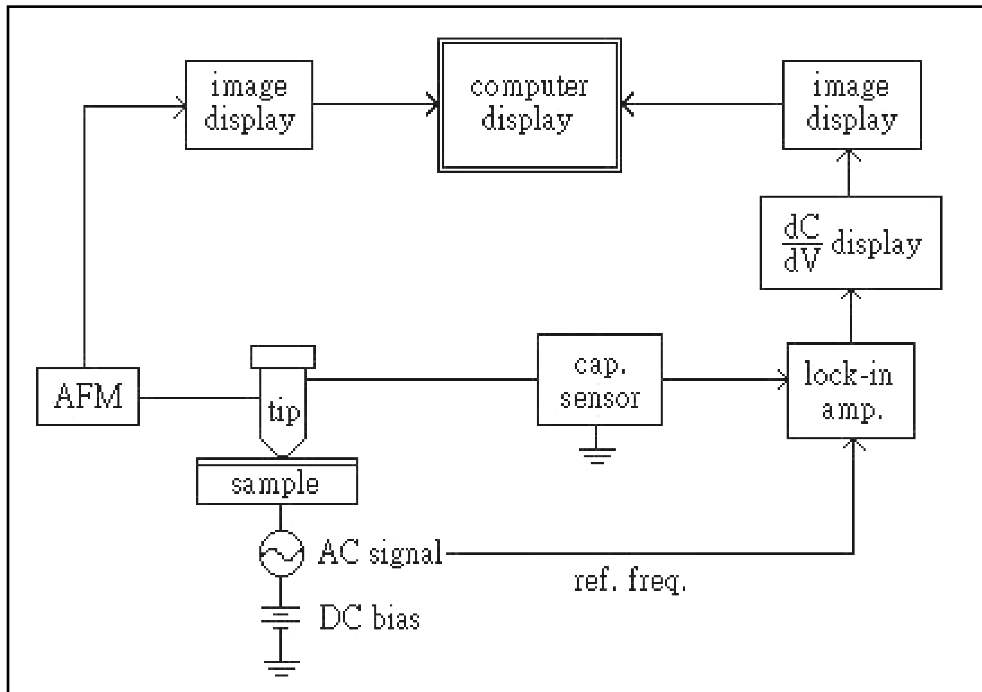


Fig. 6.1 Equipment setup of scanning capacitance microscopy.

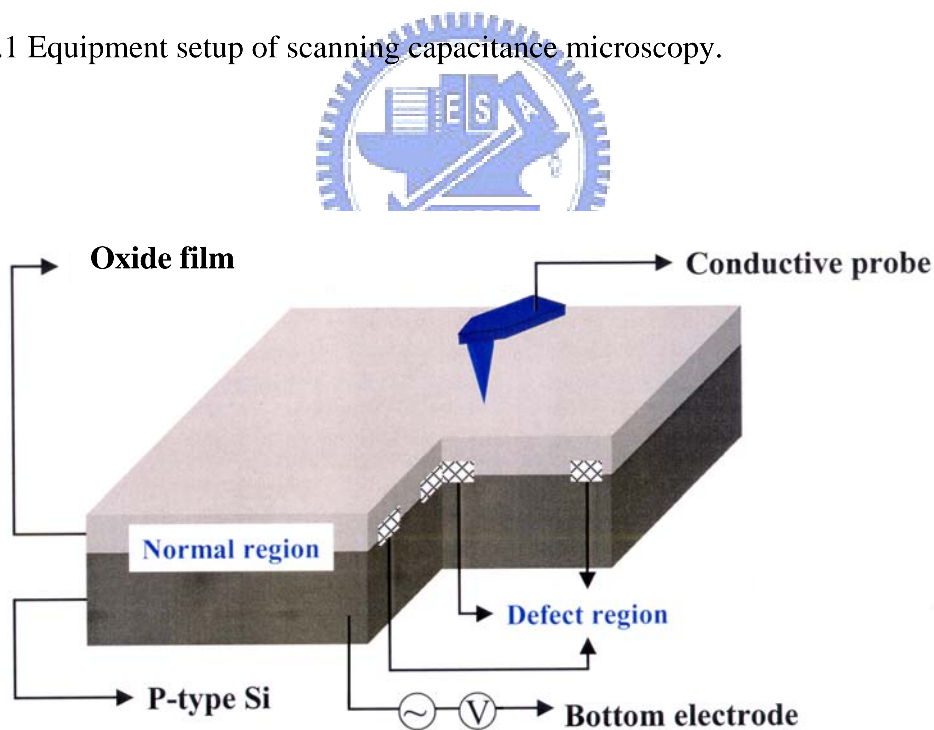


Fig. 6.2 Schematic diagram of SCM scanning on a oxide film to detect the defect regions.

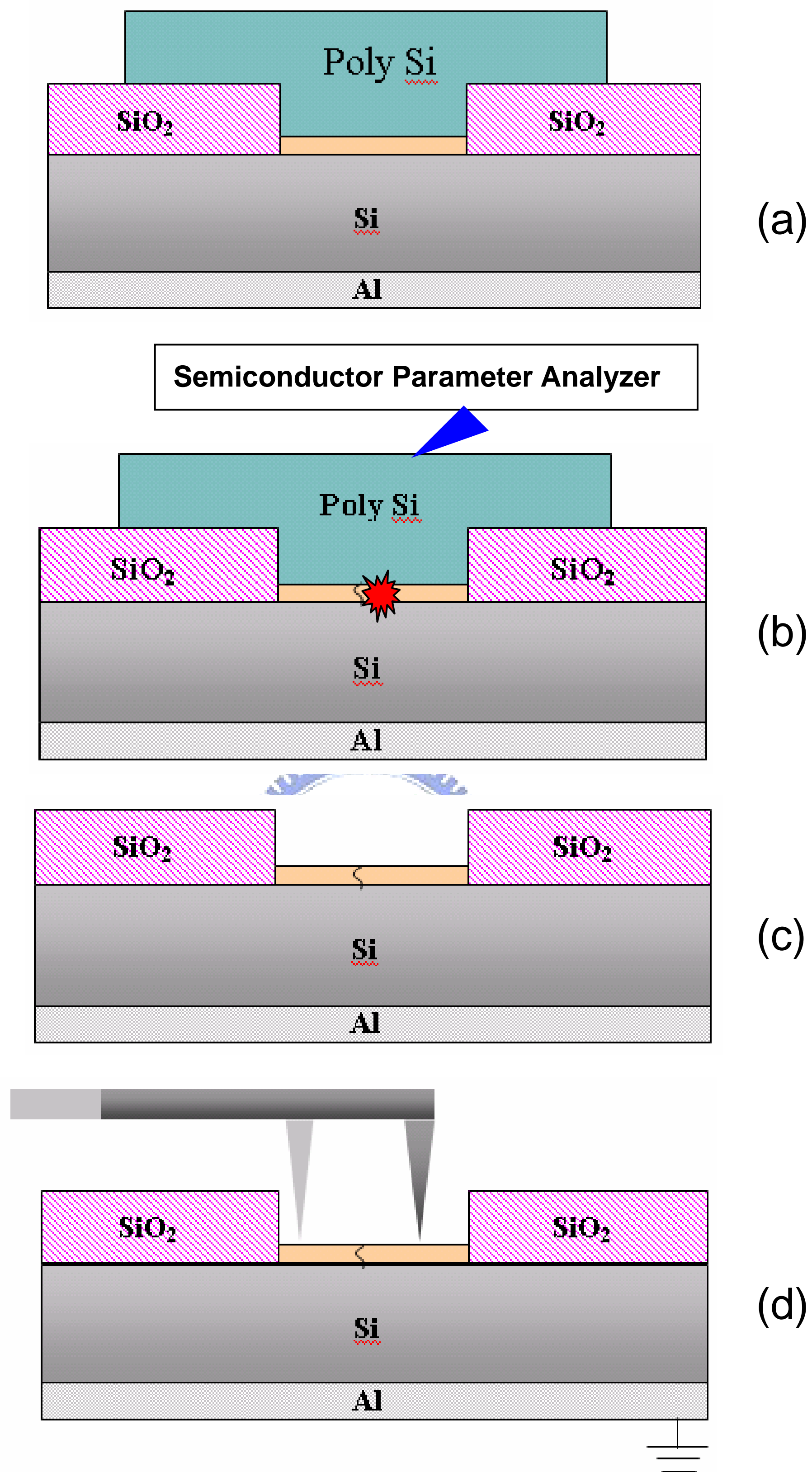
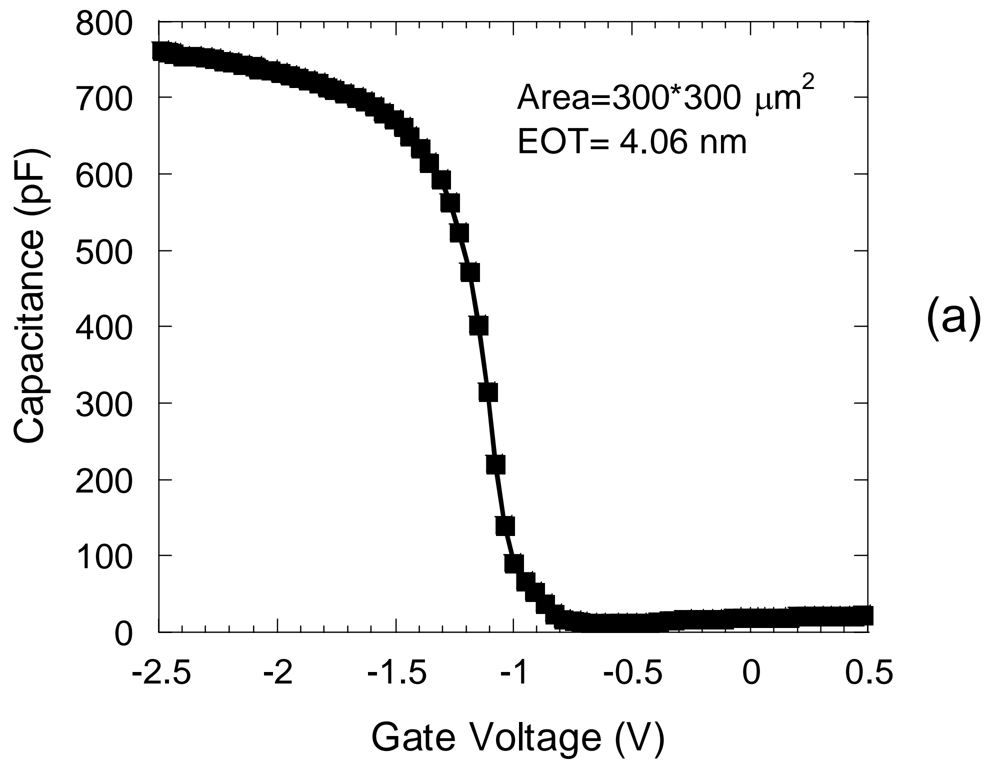


Fig. 6.3 (a) Schematic structure of the MOS capacitor fabricated in this study (b) C-V measurements followed by the OBD achieved by the semiconductor parameter analyzer (c) Removal of the poly-Si gate (d) SCM measurements.



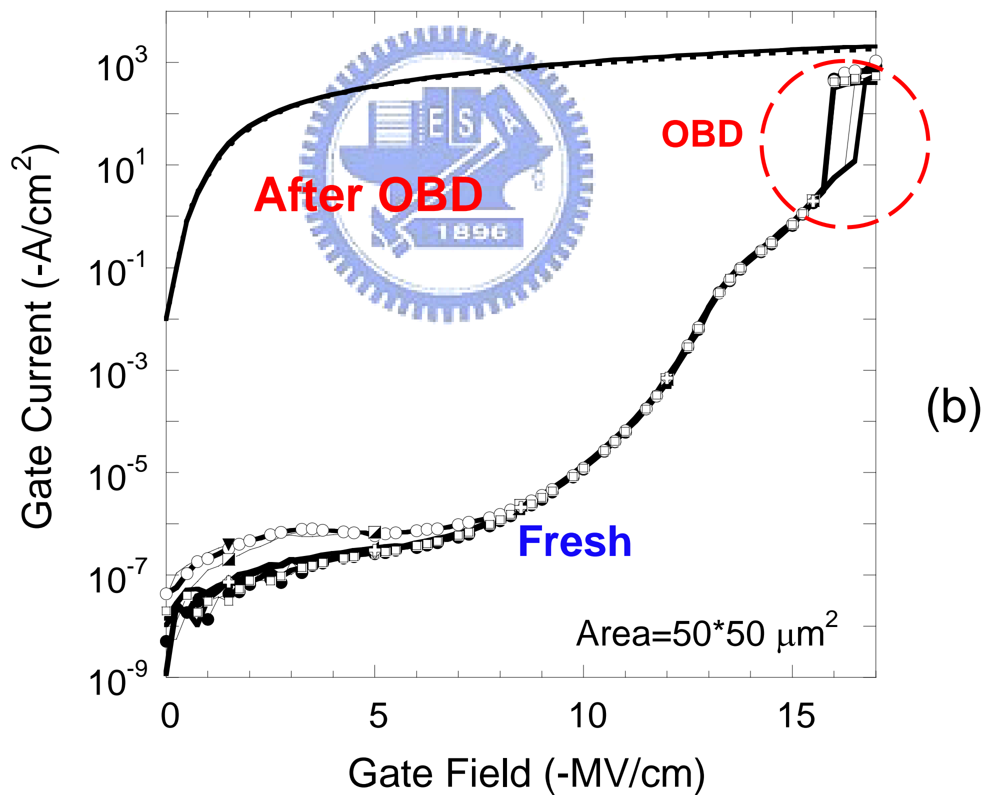


Fig. 6.4 (a) High frequency (1MHz) capacitance versus gate voltage (C-V) characteristic swept from inversion to accumulation. (b) J-E characteristics of the thin oxide under $-V_g$ injection.

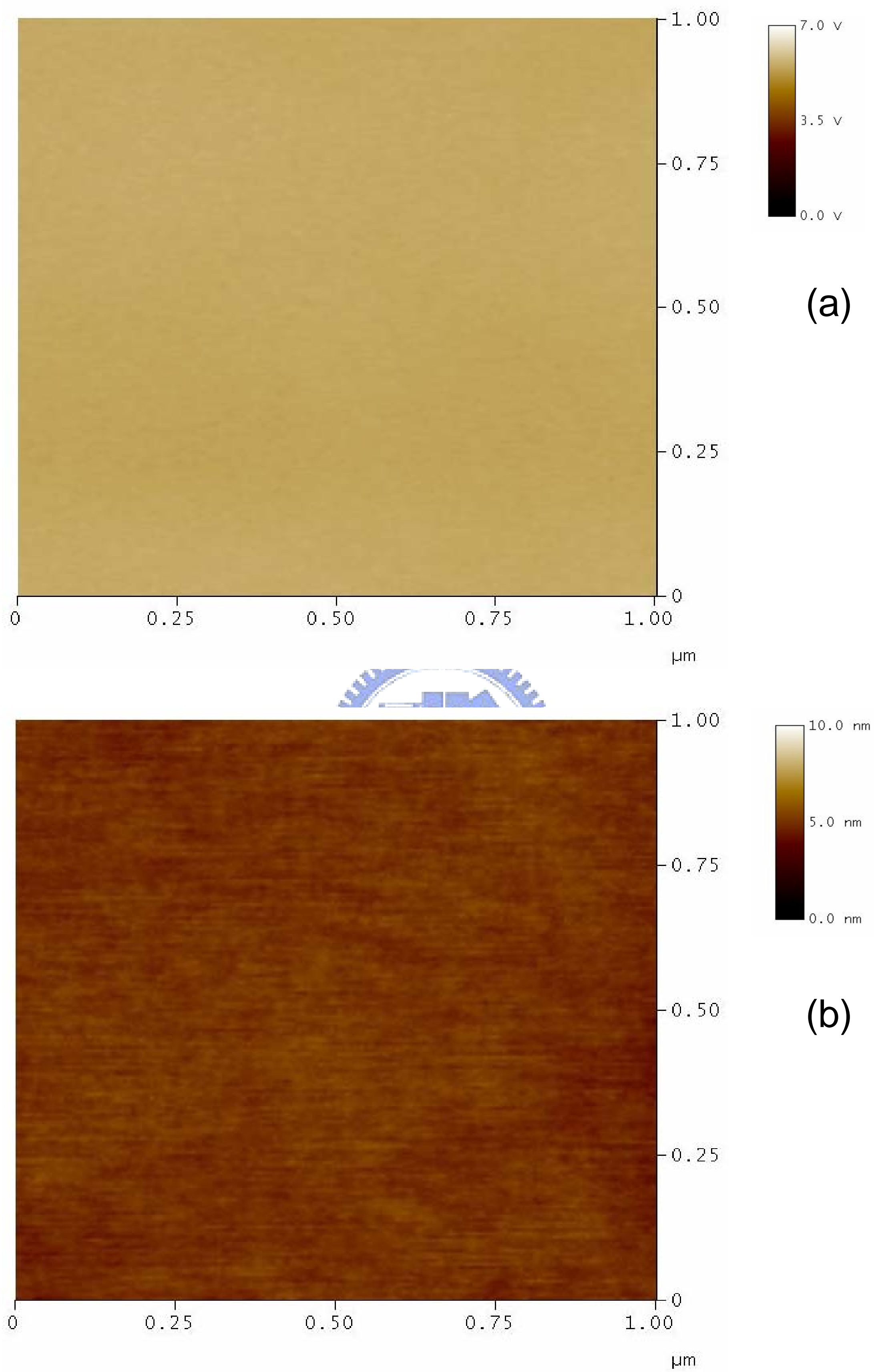
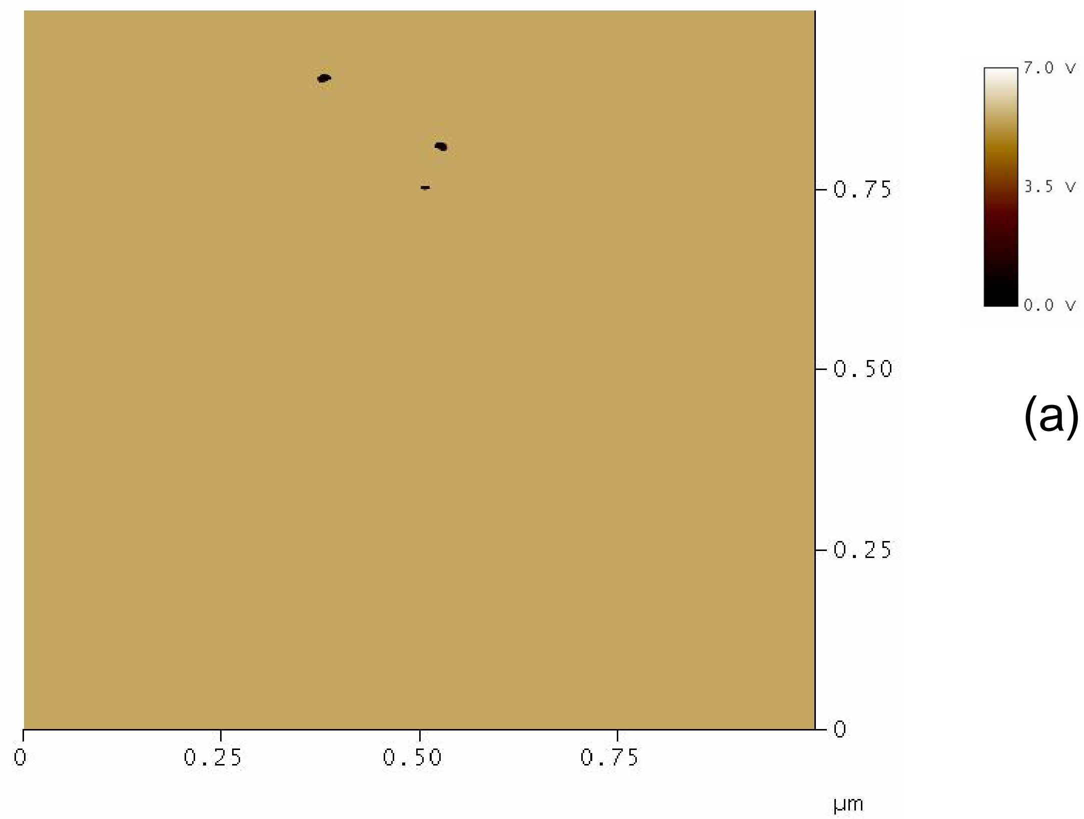


Fig. 6.5 (a) SCM image and (b) the corresponding AFM image of the fresh oxide film.



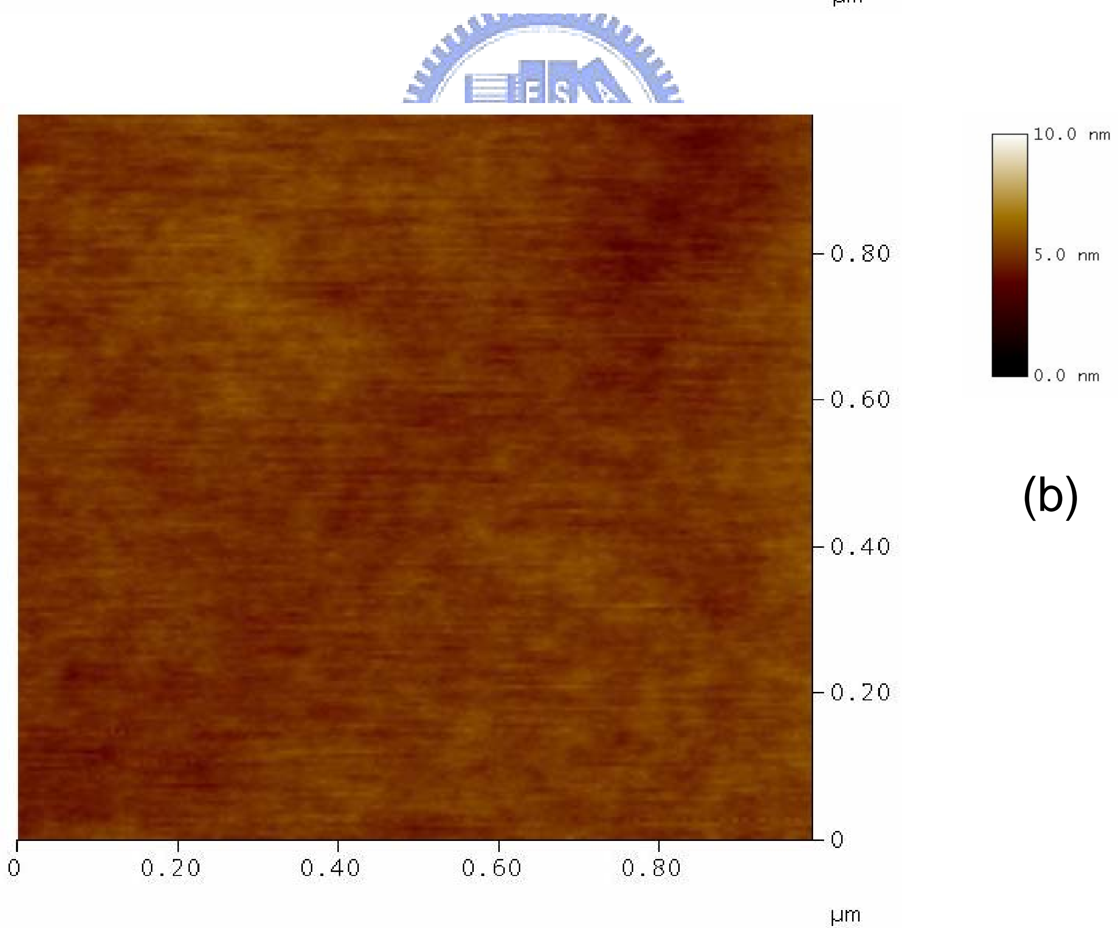
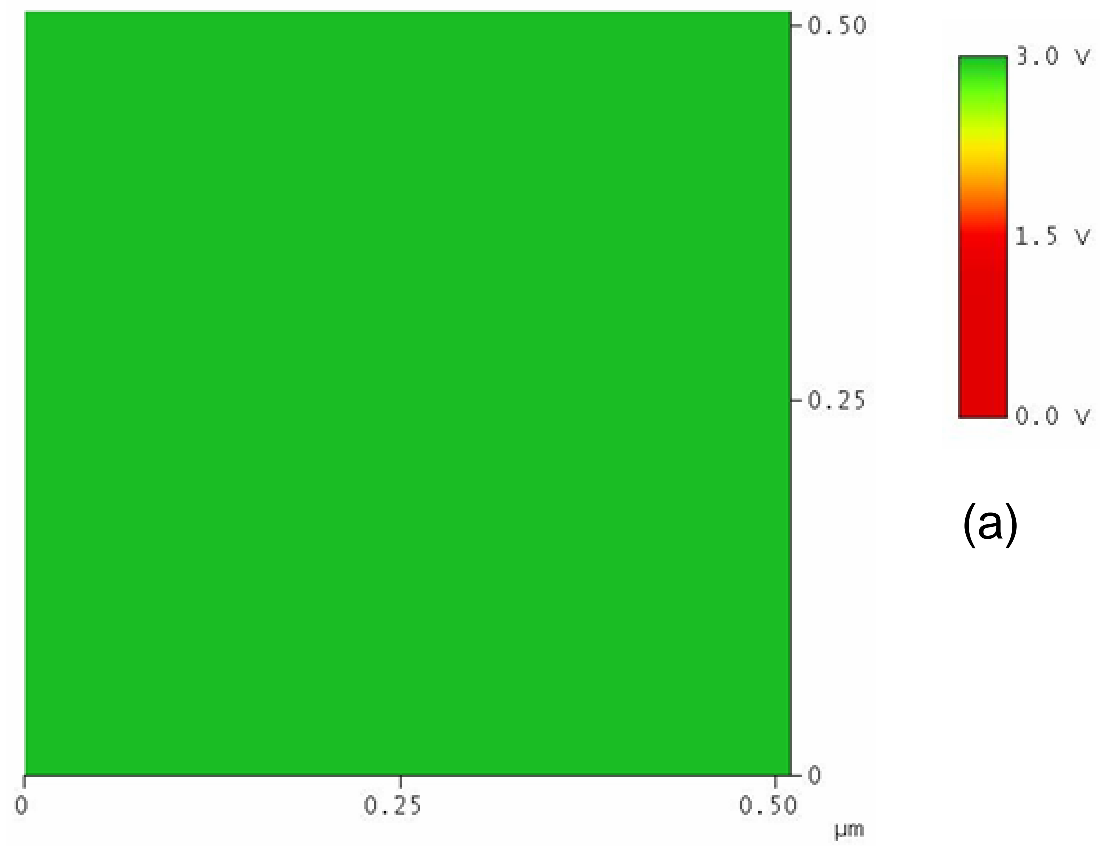


Fig. 6.6 (a) SCM image and (b) the corresponding AFM image of the oxide film after OBD.



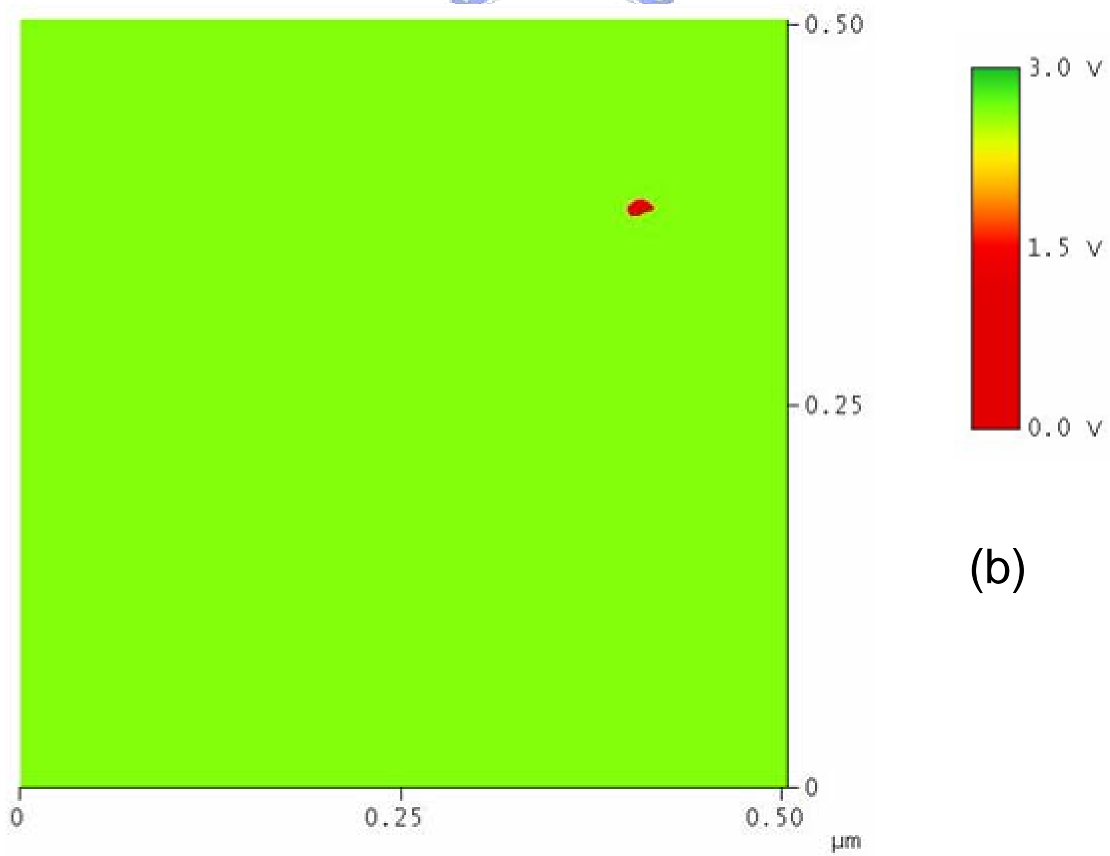


Fig. 6.7 Enlargement of SCM images for (a) fresh oxide film and (b) oxide film with a single OBD spot.

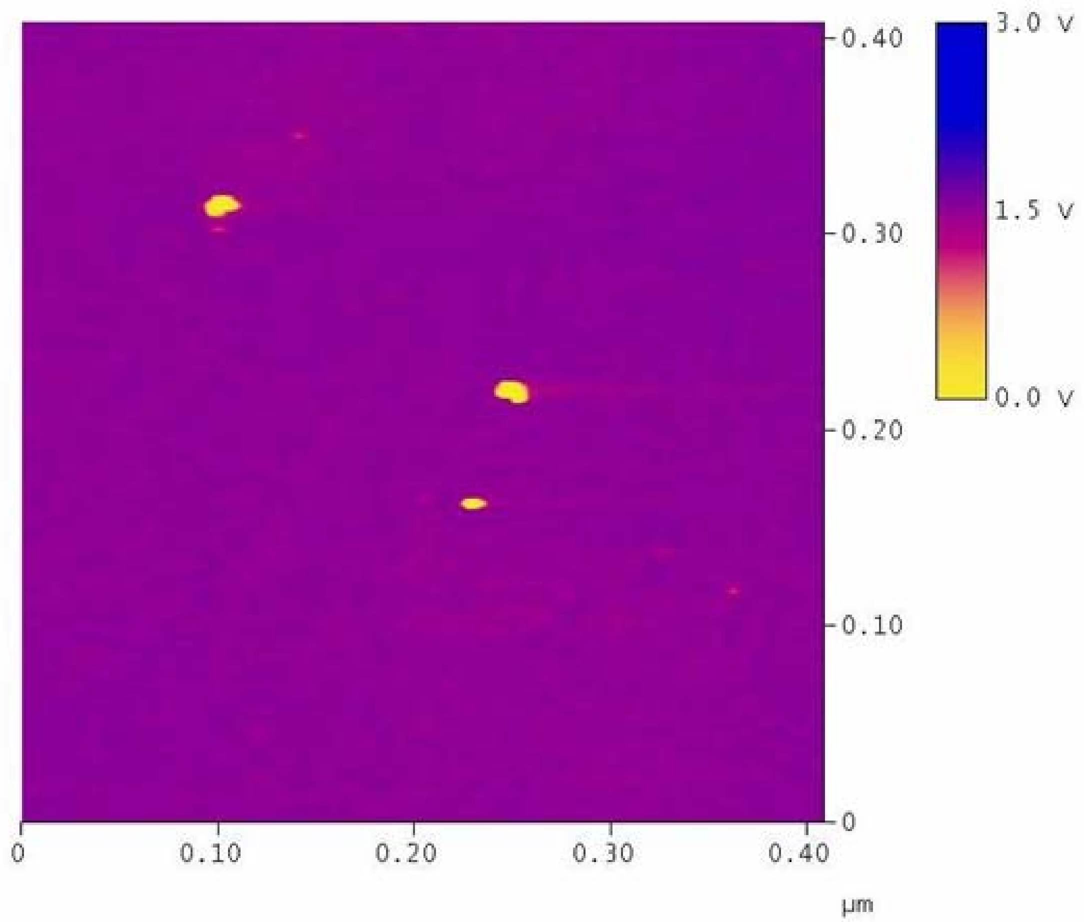


Fig. 6.8 Enlargement of SCM image for an oxide sample with three OBD spots

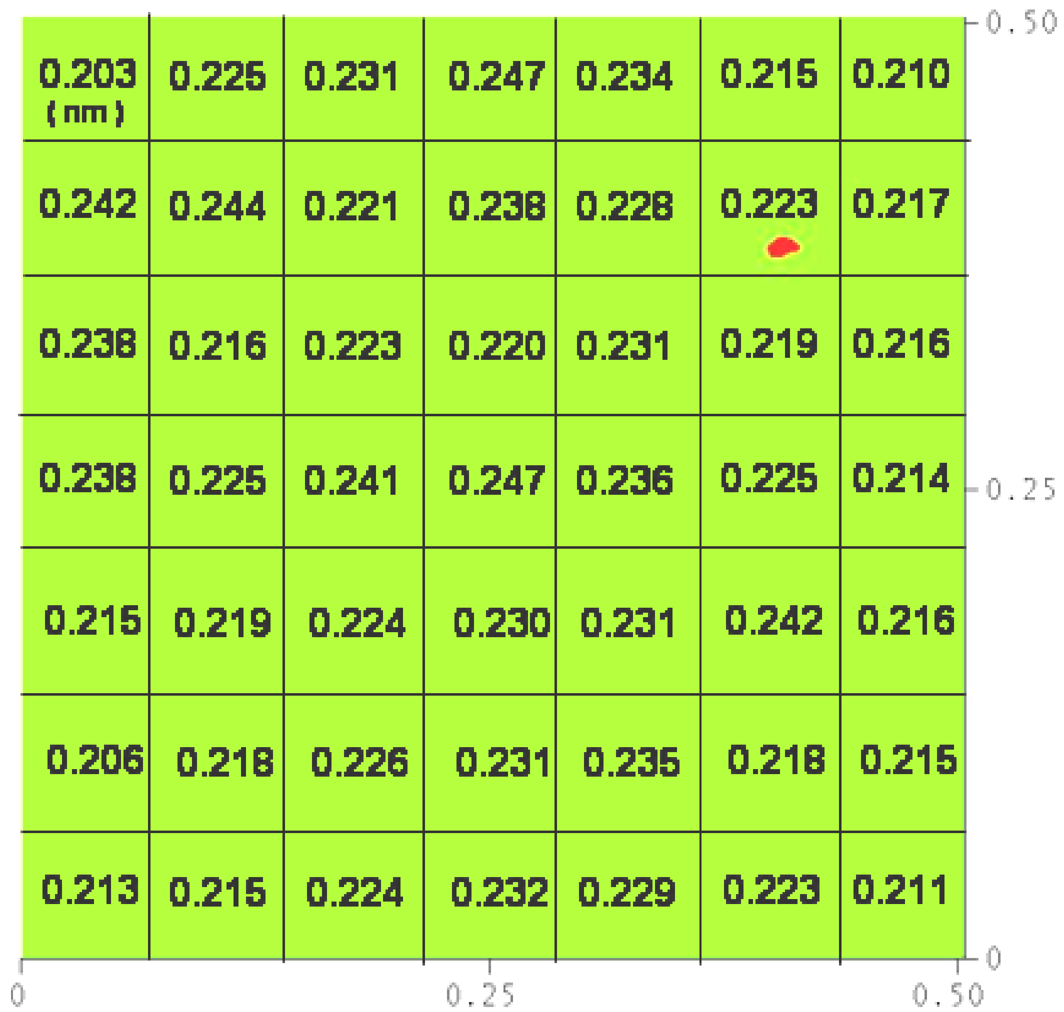


Fig. 6.9 Corresponding roughness (RMS) distributions of the oxide layer with a single OBD spot.

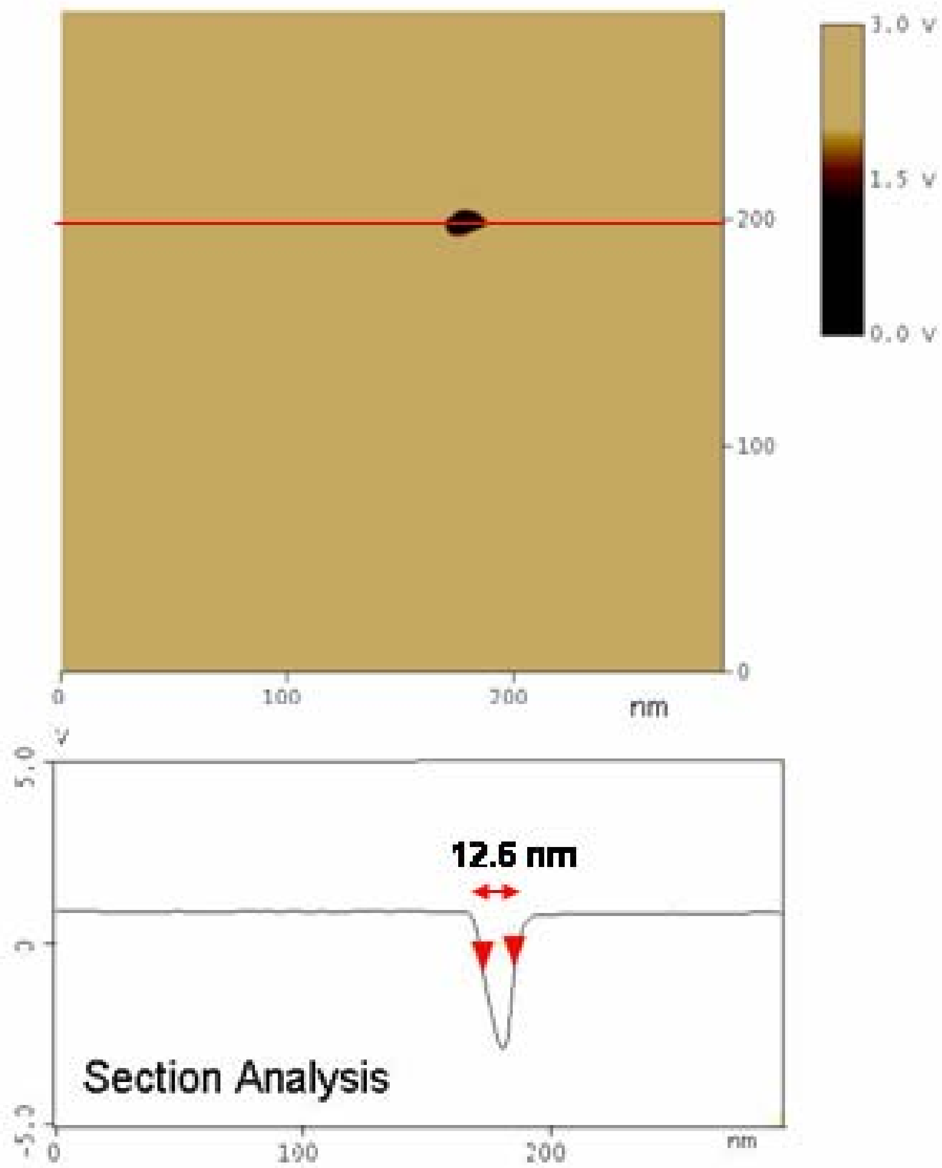


Fig. 6.10 Enlarged SCM image of one OBD spot and a cross-sectional view of the low SCM signal.

Chapter 7

Conclusions and Further Recomendations

7.1 Conclusions

In this thesis, various fluorine passivation techniques for poly-Si TFTs are proposed. The fluorine passivation effects are thoroughly discussed. In addition, the On-current (I_{on}) and Off-current (I_{off}) instabilities of poly-Si TFTs under electrical stress are comprehensively investigated. Finally, high-resolution scanning capacitance microscopy (SCM) is developed to sense the breakdown spots on thin oxide films. The main results of these studies are summarized as below:

In Chapter 2, using CF_4 plasma treatment technique, significant improvements in the performance of fluorinated SPC poly-Si TFTs are presented. A steeper *S.S.*, smaller V_{th} and better *On/Off* current ratio can be obtained. The fluorinated poly-Si TFT shows approximately 22.8 % enhancement in the maximum field-effect mobility (μ_{eff}). These results can be attributed to the reduction of the trap states in the poly-Si and the SiO_2/poly-Si interface. Moreover, the CF_4 plasma treatment also improves the device's hot-carrier immunity.

In Chapter 3, CF_4 plasma treatment combined with excimer laser annealing (ELA) were used to fabricated high-performance ELA poly-Si TFTs. Using this technique, the device performance, including the V_{th}, *S.S.*, leakage current, μ_{eff} , *On/Off* ratio, and gate dielectric integrity can be significantly improved. This is due to the fluorine passivation of interface and grain boundary trap states. Furthermore, the device reliability of the poly-Si TFTs with CF_4 plasma treatment is investigated by

employing hot-carrier stress (HCS) and self-heating stress (SHS). Under these stress tests, CF_4 plasma-treated TFTs exhibit excellent stress immunity, which is due to the formation of Si-F bonds. As a result, the CF_4 plasma treatment is a simple, effective, and process-compatible method to passivate poly-Si films, which is very promising to fabricate high-performance and high-reliability ELA poly-Si TFTs for future SOP applications.

In Chapter 4, another novel fluorine passivation scheme by employing an FSG buffer layer is proposed. Significant improvements in the device performance and uniformity are successfully demonstrated with appropriate fluorine incorporation in the poly-Si. The fluorine incorporation also promotes the device reliability with respect to hot-carrier stress. Therefore, fabricating poly-Si TFTs on FSG buffer layers with appropriate fluorine contents (2% to 4%) can improve not only the TFT's electrical performance, uniformity, but also the device reliability.

In Chapter 5, I_{on} and I_{off} variations of excimer-laser-annealed and hydrogenation-processed poly-Si TFTs under various static stress conditions are studied. It is found that, under different values of $V_{G,stress}$, the degradations of I_{on} and I_{off} are very dissimilar. The reason for these results is believed to be due to a combination of different amounts of positive charges trapped in the gate oxide and trap states generated in the poly-Si channel. In addition, the strong drain/gate voltage dependences of the variations in I_{on} and I_{off}, including trap-assisted tunneling and drain-induced trap state barrier lowering can be also clearly observed from our measurements. Finally, a model responsible for the degradation of I_{on} and I_{off} under various stress conditions is proposed.

In Chapter 6, we have successfully employed SCM to investigate breakdown spots on oxide films with a nanometer-scale resolution. The results reveal that such oxide breakdown spots are localized phenomena. After their formation, the oxide

film's insulation properties change to conductive properties, resulting in lower *dC/dV* signals. The diameters of these spots vary from approximately 6 nm to 13.5 nm. According to the corresponding AFM images, the surface morphology after oxide breakdown changes little. Furthermore, due to the zero DC bias, we can avoid destroying the breakdown spots or creating new breakdown spots. These advantages make SCM a very promising way to investigate breakdown phenomena in future nanometer-scale devices.

7.2 Further Recomendations

There are some interesting topics for further study.

(1) As described in Chapter 1, 2 and 3, CF_4 plasma treatment provides a good passivation of trap states near the SiO_2/poly-Si interface. However, in this thesis, the CF_4 plasma is generated by a conventional PE-CVD system. High-density plasma (HDP) and electron cyclotron resonance (ECR) plasma are suggested to further dissociate the fluorine atoms and thus improve the efficiency of fluorine passivation. Furthermore, remote-plasma is believed that it can avoid plasma-induced damage in the poly-Si film during plasma treatment. Some further studies of this CF_4 plasma treatment can be done by adopting these three plasma systems.

(2) Using FSG layer to replace the passivation oxide of poly-Si TFTs may be a feasible way to achieve fluorine passivation. Moreover, using the mixture of SiH_4 and CF_4 gases to deposit an *in-situ* fluorine-doped a-Si by adopting PE-CVD or LP-CVD systems is also an interesting topic worthy to be investigated.

(3) The I_{on} and I_{off} variations of poly-Si TFTs under various electrical stress conditions have been studied. However, only correlations between

Current-Voltage (I-V) curves and trap states (or charges) are considered in this thesis. We suggested that novel Capacitance-Voltage (C-V) or charge-pumping (CP) techniques should be developed to get more information about the effects of trap states (or charges) on poly-Si TFTs. Also, using the experimental results, a further study to establish a precise device simulation model is suggested.

(4) Thermal oxides were studied preliminarily in this thesis; the study on low temperature thin oxides is need. Also, although SCM can be adapted to image the oxide breakdown spots in oxide films, only MOS capacitor structure have been studied. We can further apply this technique in MOSFETs to analyze the device failure issues, especially when the gate oxide breakdown happens during the device operation. Moreover, the difference between soft breakdown and hard breakdown is one of the hottest topics in device reliability research. We believe that SCM can provide very valuable information about this topic.

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國立交通大學電子研究所博士班 [91 年 8 月- 94 年 9 月]

博士論文題目:

低溫複晶矽薄膜電晶體之氟鈍化製程與可靠度的研究

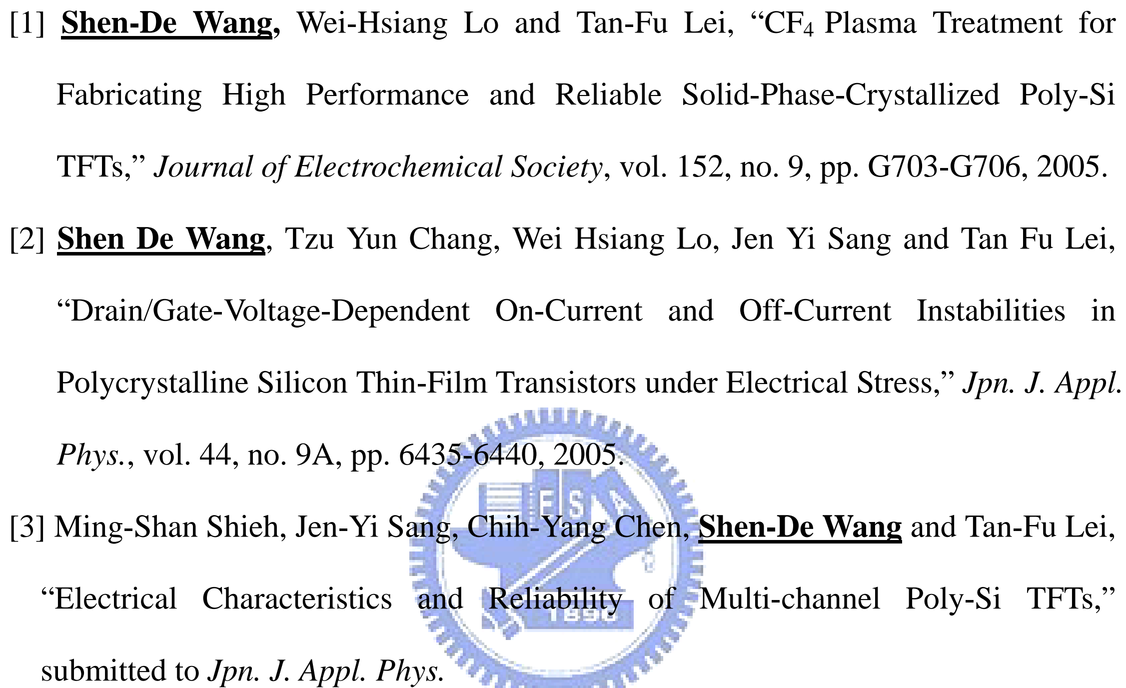
Study on Fluorine Passivation Techniques and the Reliability for Low Temperature Polycrystalline Silicon Thin-Film Transistors

Publication Lists

1. International Journal:

[1] **Shen-De Wang,** Wei-Hsiang Lo and Tan-Fu Lei, "CF_4 Plasma Treatment for Fabricating High Performance and Reliable Solid-Phase-Crystallized Poly-Si TFTs," *Journal of Electrochemical Society*, vol. 152, no. 9, pp. G703-G706, 2005.

[2] **Shen De Wang**, Tzu Yun Chang, Wei Hsiang Lo, Jen Yi Sang and Tan Fu Lei, "Drain/Gate-Voltage-Dependent On-Current and Off-Current Instabilities in Polycrystalline Silicon Thin-Film Transistors under Electrical Stress," *Jpn. J. Appl. Phys.*, vol. 44, no. 9A, pp. 6435-6440, 2005.



[3] Ming-Shan Shieh, Jen-Yi Sang, Chih-Yang Chen, **Shen-De Wang** and Tan-Fu Lei, "Electrical Characteristics and Reliability of Multi-channel Poly-Si TFTs," submitted to *Jpn. J. Appl. Phys.*

2. International Letter:

[1] **Shen-De Wang**, Wei-Hsiang Lo, Tzu-Yun Chang and Tan-Fu Lei, "A Novel Process-Compatible Fluorination Technique with Electrical Characteristics Improvements of Poly-Si TFTs," *IEEE Electron Device Lett.*, vol. 26, no. 6, pp. 372-374, 2005.

[2] **Shen De Wang**, Tzu Yun Chang, Chao Hsin Chien, Wei Hsiang Lo, Jen Yi Sang, Jam Wen Lee and Tan Fu Lei, "Performance and Reliability of Poly-Si Thin-Film Transistors on FSG Buffer Layer," *IEEE Electron Device Lett.*, vol. 26, no. 7, pp. 467-469, 2005.

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3. International Conference:

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[5] **Shen De Wang**, Tzu Yun Chang, Wei Hsiang Lo and Tan Fu Lei, “Mechanism of On-current and Off-current Instabilities under Electrical Stress in Polycrystalline Silicon Thin-Film Transistors” *IEEE International Reliability Physics Symposium* (*IRPS 2005*), pp. 702-703.

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4. Local Conference:

[1] **Shen De Wang**, Jer Chyi Wang, Tan Fu Lei, Chung Len Lee, and Jam Wem Lee, “High Reliability Ultra-Thin Interpoly-Oxynitride Dielectrics Prepared by N_2O Plasma Annealing”, *Symposium on Nano Device Technology* (*SNDT 2003*), Taiwan.

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