高速輸出入介面電路之靜電放電防護設計

學生: 黃 俊　　指導教授: 柯 明 道 教授

國立交通大學

電機學院 IC 設計產業研發碩士班

摘要

本篇論文主旨在設計適用於高速輸出入介面之靜電放電防護電路。隨著互補式金氧半元件越來越薄的閘極氧化層和高速輸出入介面電路的工作頻率越來越快的情況下，如何在高速的頻段中設計即時有效的靜電放電防護，並降低由靜電放電防護電路所導致的負面影響，是一個相當大的挑戰。本論文所提出的靜電放電防護方式既可以達到商業規格的靜電放電耐受度要求，也可有效地降低靜電放電防護元件產生的寄生效應對高速輸出入介面電路性能的影響。本篇論文分為二大部分，透過理論的推導以及實驗晶片的量測，來驗證適用於高速輸出入介面的靜電放電防護設計。

本論文的第一部分是在 0.13 微米 CMOS 製程中，藉由高頻量測系統、傳輸線脈衝產生系統(Transmission Line Pulsing System, TLP)，以及靜電放電耐受度量測系統，分別對不同尺寸的靜電放電防護元件進行測試。利用雙埠接地-訊號-接地(Ground-Signal-Ground, GSG)的晶片上(On-Wafer)量測方式萃取靜電放電防護元件的高頻特性，經過分析及計算後，已建立符合高速輸出入介面電路使用之靜電放電防護元件資料庫，可提供實際應用上最適合的靜電放電防護元件組合。

本論文的第二部分，提出適用於高速輸出入介面電路的靜電放電防護設計。憑藉本研究建立的資料庫，可適當地選擇符合需求的靜電放電防護元件尺寸，此方式既可滿足商業規格的靜電放電耐受度要求，並且可以將靜電放電防護元件之寄生效應對核心電路的衝擊降至最低。此外可將靜電放電防護元件置於銲墊(Pad)底下，除了可以減少靜電放電防護元件佔用的晶片面積，還可利用銲墊寄生電容與靜電放電防護元件寄生電容相互串聯的效應，進一步降低輸入輸出接點的寄生

電容值。

本論文已經透過實驗晶片的量測，成功驗證本研究所提出的高速輸出入介面電路之靜電放電防護設計架構，實驗結果證實此設計適用於高速輸出入介面電路的靜電放電防護設計。

ESD Protection Design for High-Speed I/O Interface Circuit

Student: Chun Huang Advisor: Prof. Ming-Dou Ker

Department of Electronics Engineering & Institute of Electronics
National Chiao-Tung University

ABSTRACT

This thesis focuses on the ESD protection design for high-speed input/output (I/O) interface circuit. The gate oxide of the MOSFET transistor becomes thinner as the CMOS technology scales, which enables the high-speed I/O interface circuits with higher operating frequency. Unfortunately, there exists a challenge to design an ESD protection circuit with satisfactory ESD robustness and low parasitic effects to the gigahertz high-speed I/O circuit. This thesis presents a design methodology to design the ESD protection circuit for gigahertz high-speed I/O circuits with high ESD robustness and low parasitic capacitance.

There are two major designs in this thesis, in first part, the two-port ground-signal-ground (GSG) measurement setup in the radio-frequency band (~GHz) is used to measure the high-frequency characteristics of ESD devices and the TLP measurement system is used to measure the ESD robustness of the ESD devices in a 0.13-μm CMOS process. Therefore, the relationship between the high-frequency characteristics and ESD robustness under different ESD device dimensions can be obtained.

The second part presents the most suitable ESD device for gigahertz high-speed

applications based on the database which had been established in the first part. With the database, the optimal ESD device dimensions can be obtained as long as the requirement of parasitic capacitance and ESD robustness are determined. Besides, placing the ESD protection device under the bond pad can further reduce the parasitic capacitance and the total chip area.

The test devices and the ESD protection design in this thesis have been fabricated in a 0.13-μm CMOS process, and the experimental results have shown that this ESD protection design is suitable for gigahertz high-speed I/O interface circuits.

誌謝

ACKNOWLEDGEMENT

首先要感謝的是我的指導教授柯明道博士，這兩年來的教導和鼓勵。記得在剛進入 ESD 的領域時，幾乎是完全沒有任何 ESD 的觀念，從最基本的物理觀念一直到 ESD 元件的特性再到整個 ESD 電路的設計，一路上不厭其煩的給予我更正和指導，特別是柯教授認真及嚴謹的研究態度，還有指導學生的做人處事方法等等。使我在靜電放電防護設計這個領域當中獲益不少。

另外還要感謝的是智原科技曾玉光博士在整個合作計畫上所提供的協助和幫忙與指導，同是奈米電子與晶片系統實驗室的許勝福、蕭淵文、陳榮昇、張瑋仁、顏承正、李健銘、陳世宏、王文傑、徐新智、王暢資、林群祐、賴泰翔、陳佳惠、廖宏泰、邱柏硯等學長姐和同學學弟們，大家不僅在學業上互相照顧幫忙，也共同為整個實驗室的運作和良好的傳統而一起努力，謝謝你們不管是在專業上還是生活上所遇到的問題都能適切誠懇地幫助關心我度過難關，尤其是蕭淵文學長的大力幫忙與指導，讓整個研究過程進行的相當順利。

最後要感謝我的父母及兄長，無論是在經濟上或是精神上都能充分的支持和鼓勵，在兩年的研究生活當中能夠無需憂慮的專心地致力於論文研究，讓我能夠順利地完成學業，在此由衷致謝。

黃 俊

九十六年二月

CONTENTS

TABLE CAPTIONS

CHAPTER 2

CHAPTER 3

CHAPTER 4

FIGURE CAPTIONS

CHAPTER 2

CHAPTER 3

CHAPTER 4

CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

With the advantage of low cost high integration, more and more high-speed communication circuits had been fabricated in CMOS processes, including the high-speed input/output (I/O) interface circuits. Electrostatic discharge (ESD) has been a one of the most important reliability issues for integrated circuits (ICs) in CMOS processes, especially in nanoscale CMOS processes. There are two main design considerations in ESD protection design for giga-hertz (GHz) high-speed I/O applications. First, ESD protection circuits for high-speed I/O circuits must sustain enough ESD robustness to effectively protect ICs from being damaged by ESD stresses. Second, the high-speed performance degradation due to parasitic effects of ESD protection devices needs to be minimized.

Unfortunately, traditional ESD protection devices, such as gate-grounded NMOS (GGNMOS), have large parasitic capacitance, which causes intolerable high-speed performance degradation. Therefore, traditional ESD protection schemes are no longer suitable for high-speed I/O circuits because of the undesired parasitic effects. It had been reported that the largest design budget on parasitic capacitance at I/O pads, which includes the parasitic capacitances of the bond pads and ESD protection circuits, in 2-GHz high-frequency applications are 200 fF [1]. This implies that the ESD protection circuit should be carefully designed to have the smallest parasitic capacitance. With proper design, the double-diode structure in cooperation

with a power-rail ESD clamp circuit can still be used to realize the ESD protection scheme for high-speed I/O circuits [1]-[2]. ESD protection schemes are also included of ESD protection circuits with coil [3]-[4], equal-size distributed ESD protection circuits [5]-[7], decreasing-size distributed ESD protection circuits [8]-[10], and π-model distributed ESD protection circuits [11]-[12]. In order to minimize the parasitic capacitance of the ESD devices, the high-frequency (HF) characteristics of ESD devices in a 0.13-μm CMOS process had been evaluated in this work to establish the database for high-speed I/O applications. With this database, the optimal device dimensions can be obtained as long as the requirements of parasitic capacitance and ESD robustness are determined.

1.2 Thesis Organization

In chapter 2, the HSPICE simulation to evaluate the parasitic capacitance of ESD diodes are described. Besides, device structure and layout description for (shallow-trench-isolation) STI diodes and MOS-bounded diodes are presented.

In chapter 3, the experimental results on DC I-V characteristics, TLP I-V curves, ESD robustness, and parasitic capacitance of the fabricated ESD diodes in a 0.13-μm CMOS process are reported and discussed. Furthermore, the design example of an ESD protection circuit for 5-GHz high-speed I/O applications in a 0.13-μm CMOS process is proposed.

In chapter 4, a high-speed I/O interface circuit with this ESD protection scheme had been designed and fabricated in a 0.13-μm CMOS process to verify the performance, including ESD robustness and parasitic effects. The high-speed I/O interface circuit includes the transmitter and receiver interface circuit. Simulation had been performed to ensure that the total parasitic capacitance of ESD devices and bond

pad is below 500 fF. The experimental results had demonstrated that the ESD robustness with this ESD protection scheme can sustain a HBM ESD robustness of more then 2 kV. Finally, the future works about the modified design on the ESD protection circuit is given in Chapter 5.

CHAPTER 2

INVESTIGATION ON HIGH-FREQUENCY CHARACTERISTICS OF DIFFERENT ESD DIODE STRUCTURES

With the increased operating frequency of modern high-speed I/O circuits, the maximum tolerated parasitic capacitance at the I/O pad is decreased. However, there is a tradeoff between the capacitance at the I/O pad and the ESD robustness. The parasitic loading effect of ESD protection devices for gigahertz high-speed I/O applications becomes more and more serious because the dimensions of the ESD protection devices can not be shrunk unlimitedly in order to maintain the required ESD robustness. From circuit perspectives, the protection circuits must be transparent to the internal circuit, and must not affect the signal under normal circuit operating conditions. The on-chip ESD protection circuit is placed between the I/O pad and the internal circuits, as shown in Fig. 2.1. The ESD clamp device at the I/O pad can be realized with various devices, such as diode, gate-grounded NMOS (GGNMOS), or silicon-controlled rectifiers (SCR). Traditionally, the GGNMOS is designed with large device dimensions and large drain-contact-to-poly-gate spacing in order to sustain acceptable ESD level [13]-[14]. The gate-coupled technique [15]-[17] or the substrate-triggering technique [18] had been used to uniformly turn on the multiple fingers in the GGNMOS to improve the ESD level. However, the large device dimensions consume much chip area and cause large parasitic capacitance. The wide drain diffusion junction contributes large parasitic capacitance at the I/O signal pad, which degrades the circuit performance. Thus, the GGNMOS is not suitable for

gigahertz high-speed applications. The other ESD device suitable for low-capacitance consideration is SCR, because SCR can sustain high ESD level in a small device size [19]-[20]. However, the high trigger voltage of SCR should be taken into consideration. For example, in a 0.25-μm CMOS process, the gate oxide breakdown voltage is around 10V, and the trigger voltage of SCR is higher than the gate oxide breakdown voltage. Therefore, extra trigger circuits should be used to turn on the SCR in time. The ESD devices shunt ESD current from the I/O pad to the power supply rails away from the internal circuit during ESD stresses. However, the ESD devices contribute parasitic capacitances and resistances on the signal path under normal operating conditions, which causes serious performance degradation at high frequency bands. A poorly designed ESD protection scheme may cause impedance mismatches, signal reflection, corruption of signal integrity, and inefficient power transfer. In order to provide efficient ESD protection without extra trigger circuits, diodes are commonly used for ESD protection in high-speed I/O applications, as shown in Fig. 2.2 [21]-[22]. Besides, low-capacitance bond pad design had been reported to enhance the high-speed performance [23].

In this chapter, the parasitic capacitance of STI and MOS-bounded diodes are calculated and simulated. In addition, the layout patterns of the diodes are reported and discussed.

2.1 Diode

Generally, the ESD diode is designed to be operated in the forward-biased condition to discharge the ESD current during ESD stresses, and is designed to be operated in the reverse-biased region under normal circuit operating conditions. The diode current abruptly rises at around 0.6V~0.7V, which is the cut-in voltage. The

turn-on resistance is around 1Ω to 5Ω in the forward-bias condition. In the reverse-biased condition, the diode current rises after the junction breakdown occurs. This is because the current conduction begins when the junction goes into avalanche breakdown under reverse-biased conduction.

In the forward bias condition, the parasitic capacitance will be increased due to the decreased depletion region. The width of the depletion region will increase to avoid the minority carrier to pass through the depletion region when the ESD diode is in the reverse-biased condition, so the parasitic capacitance of ESD diode is decreased in the reverse-biased condition.

The ESD level of diodes operating in the forward-biased condition is better than that in the reverse-biased condition. By using the turn-on efficient power-rail ESD clamp circuit, the diodes can operate in forward-biased condition when ESD current comes to promote overall ESD level [24]. Therefore, the size of ESD diodes did not need very large. Moreover, the power-rail ESD clamp circuit does not contribute any parasitic effect to the internal circuit. Diode in the forward-biased condition is very useful in ESD protection design for high-speed applications.

2.1.1 STI Diode

The STI diode is the typical diode structure, and the foundry provides the STI diode. The schematic cross-sectional view of the p+/n-well STI diode (P-type diode) is shown in Fig. 2.3(a). The N+ diffusion (cathode) and P+ diffusion (anode) are separated by the shallow trench isolation (STI). The N+ diffusion surrounds the P+ diffusion. The schematic cross-sectional view of the n+/p-well STI diode (N-type diode) is shown in Fig. 2.3(b). The P+ diffusion (anode) and N+ diffusion (cathode) are also separated by the shallow trench isolation (STI). The P+ diffusion surrounds

the N+ diffusion. The n-well/p-well diode (NW-type diode) is shown in Fig. 2.3(c), The P+ diffusion in P-well (anode) and the N+ diffusion in N-well (cathode) are separated by the shallow trench isolation (STI). The P+ diffusion in P-well surrounds the N+ diffusion in N-well. When the abovementioned ESD diodes are under forward-biased ESD stress condition, the ESD current would flow from P+ diffusion to N+ diffusion.

2.1.2 MOS-Bounded Diode

The MOS-bounded diode had been reported with its ESD robustness verified in a 0.35-μm CMOS process, but the high-frequency device characteristics were not reported [25]. In a 0.13-μm high-speed (HS) CMOS process, the ESD robustness and the high-frequency characteristics of MOS-bounded diodes were investigate in this thesis. The cross-sectional views of the NMOS-bounded diode and PMOS-bounded diode are shown in Fig. 2.4(a) and 2.4(b), respectively. The NMOS-bounded (PMOS-bounded) diode has a NMOS (PMOS) inserted in the diode structure. The MOS-bounded diodes have the cathode (anode) of N+ (P+) diffusion, which does not touch the P+ (N+) diffusion in the diode structure. The anode (cathode) of P+ (N+) diffusion directly touches another N+ (P+) diffusion in the NMOS-bounded (PMOS-bounded) diode, where this N+ (P+) is floating. In this NMOS-bounded (PMOS-bounded) diode, the poly gate is fully covered by the N+ (P+) implementation. With the poly gate between the anode and cathode, the turn-on speed can be enhanced to bypass the ESD stress current. Therefore, the MOS-bounded diode can provide more effective ESD protection to the internal circuits.

The NMOS-bounded (PMOS-bounded) diode is fully compatible to the general

CMOS processes without any additional process step or extra mask layer. The MOS-bounded diodes were implemented to evaluate its characteristic and ESD robustness in this work.

2.2 ESTIMATION FOR PARASITIC EFFECTS OF ESD DIODES

The equivalent circuit model of diode is shown in Fig. 2.5. The diode capacitance is modeled by cd. The capacitance cd is the combination of diffusion capacitance (*cdiff*), depletion capacitance (*cdep*), metal (*cmetal*), and poly capacitance (*cpoly*). The capacitance cd can be expressed as

$$cd = cdiff + cdep + cmetal + cpoly$$

where

cdiff is the diffusion capacitance,

cdep is the depletion capacitance,

cmetal is the metal capacitance (depends on routing strategy),

and *cpoly* is the capacitance (depends on routing strategy).

Using diffusion capacitance equations when the transit time (TT) models the diffusion capacitance, cause by injected minority carriers. In practice, TT is estimated from the pulsed time-delay:

$$cdiff = TT \bullet \frac{\partial id}{\partial vd}$$

TT (s) is the transit time with the default value of zero. Using depletion capacitance equations when the depletion capacitance is modeled by junction bottom and junction periphery capacitances:

$$cdep = CJeff \bullet \left(1 - \frac{vd}{PB}\right)^{-MJ} + CJPeff \bullet \left(1 - \frac{vd}{PHP}\right)^{-MJSW}$$

$$CJeff = CJ \bullet AREAeff$$

$$CJPeff = CJP \bullet CJPeff$$

$$AREAeff\ (m^2) = \left[(Weff + Leff) \bullet M\right]$$

$$PJeff\ (m) = \left[(2W + 2L) \bullet M\right]$$

$$cmetal = \left(\frac{\varepsilon_{ox}}{XOM}\right) \bullet (WMeff + XMeff) \bullet (LMeff + XMeff) \bullet M$$

$$cpoly = \left(\frac{\varepsilon_{ox}}{XOI}\right) \bullet (WPeff + XPeff) \bullet (LPeff + XPeff) \bullet M$$

$$\varepsilon_{ox} = 3.9 \times 8.85 \times 10^{-14}\ F/cm$$

where

M : multiplier,

WMPeff (m) : default = 0,

LMPeff (m) : default = 0,

XMeff (m) : accounts for masking and etching effects, default = 0,

PB : area junction contact potential,

MJ : area junction grading coefficient,

PHP : periphery junction contact potential,

MJSW : periphery junction grading coefficient,

XOM : thickness of the metal to bulk oxide,

XOI : thickness of the poly to bulk oxide.

By the foundry junction model perimeters and the diode capacitance modeled as above, the estimation for parasitic effects of ESD diodes can be calculated via computer-aided-tool (CAD) such as SPICE or other simulation tools.

2.3 SIMULATION ON PARASITIC EFFECTS OF ESD DIODES

The three types of ESD diodes will be chosen in proper dimensions. Basically, the sizes of ESD diode in high-frequency applications should be as small as possible because the parasitic capacitance degrades performance. Besides, the ESD diode should sustain the required ESD level. In the first step, some proper sizes with the estimated parasitic capacitance below 100fF were selected, as shown in Table 2.1. All the parasitic capacitance of the three types of ESD diodes had been simulated by the simulator HSPICE to estimate the parasitic capacitance by the equations listed above.

2.4 LAYOUT DESCRIPTION OF ESD DIODES

The layout description of ESD diodes includes STI and MOS-bounded diodes. Not only the ESD robustness but also the parasitic capacitances of these diodes are investigated. In this work, two-port GSG layout was adopted to facilitate the on-wafer probing to evaluate the parasitic capacitance contributed by the ESD devices. The layout top view of the experimental test chip includes the STI diodes and MOS-bounded diodes, as shown in Fig. 2.6. The device dimensions of the ESD devices are summarized in Table 2.2. The total layout area is 1500μm x 4500μm. With the experimental results of the ESD devices, the optimal ESD device dimension can be obtained for high-speed applications.

2.5 SUMMARY

Two kinds of ESD diode structures for high-frequency applications have been simulated and thoroughly estimated, the proper device sizes had been chosen among the three types of STI diodes and two types of MOS-bounded diodes. All the diodes were fabricated in a 0.13-μm CMOS process. In order to obtain the complete data efficiently, the estimation of diode sizes by simulation must be done accurately, and the size ranges of diodes are very important. If the size ranges is too large, large amount of diode may cause too large chip area. Besides, too large diode sizes may cause large parasitic capacitance, which is not suitable for high-frequency applications.

Table 2.1 Simulation on parasitic effects of ESD diodes.

Diode Device	W/L (μm/μm)	M	Parasitic Capacitance (fF)
DION_L130E	4/5	5	68.6947
DION_L130E	10/10	1	64.0783
DIOP_L130E	4/5	5	87.7954
DIOP_L130E	10/10	1	82.9880
DIONW_L130E	4/5	5	95.5736
DIONW_L130E	10/10	1	49.7544

Table 2.2 Layout dimensions of three types STI and two types MOS-bounded of ESD diodes.

Item	Pad	Diode Type	Width (μm)	Length (μm)	M	Periphery (μm)	Area $(\mu m)^2$	Pre-Sim Cap. (fF)
1	M8 ~ M1	DIONW_L130E_DC2	20	5	1	50	100	66.10
2		DION_L130E_DC2	20	5	1	50	100	77.17
3		DIOP_L130E_DC2	20	5	1	50	100	75.24
4		DIONW_L130E_DC2	20	5	2	100	200	132.20
5		DION_L130E_DC2	20	5	2	100	200	154.33
6		DIOP_L130E_DC2	20	5	2	100	200	150.48
7		DIONW_L130E_DC2	20	5	3	150	300	198.30
8		DION_L130E_DC2	20	5	3	150	300	231.50
9		DIOP_L130E_DC2	20	5	3	150	300	225.71
10		DIONW_L130E_DC2	20	5	4	200	400	264.40
11		DION_L130E_DC2	20	5	4	200	400	308.66
12		DIOP_L130E_DC2	20	5	4	200	400	300.95
13		DIONW_L130E_DC2	20	5	5	250	500	330.50
14		DION_L130E_DC2	20	5	5	250	500	385.83
15		DIOP_L130E_DC2	20	5	5	250	500	376.19
16		Empty(De-Embedding)						
17		Open(De-Embedding)			1			
18		Short(De-Embedding)			1			
19		Open(De-Embedding)			2			
20		Short(De-Embedding)			2			
21		Open(De-Embedding)			3			
22		Short(De-Embedding)			3			
23		Open(De-Embedding)			4			
24		Short(De-Embedding)			4			
25		Open(De-Embedding)			5			
26		Short(De-Embedding)			5			
27	M8 ~ M6	DIONW_L130E_DC8	20	5	1	50	100	66.10
28		DION_L130E_DC8	20	5	1	50	100	77.17
29		DIOP_L130E_DC8	20	5	1	50	100	75.24
30		DIONW_L130E_DC8	20	5	2	100	200	132.20
31		DION_L130E_DC8	20	5	2	100	200	154.33
32		DIOP_L130E_DC8	20	5	2	100	200	150.48
33		DIONW_L130E_DC8	20	5	4	200	400	264.40
34		DION_L130E_DC8	20	5	4	200	400	308.66
35		DIOP_L130E_DC8	20	5	4	200	400	300.95
36		DIONW_L130E_DC8	20	5	5	250	500	330.50
37		DION_L130E_DC8	20	5	5	250	500	385.83
38		DIOP_L130E_DC8	20	5	5	250	500	376.19
39		Empty(De-Embedding)						
40		Open(De-Embedding)			1			
41		Short(De-Embedding)			1			
42	M8 Only	Empty(De-Embedding)						
43	M8 ~ M1	NMOS_BOUNDED_DIODE_L130E	20	5	1	50	100	
44		NMOS_BOUNDED_DIODE_L130E	20	5	5	250	500	
45		PMOS_BOUNDED_DIODE_L130E	20	5	1	50	100	
46		PMOS_BOUNDED_DIODE_L130E	20	5	5	250	500	
47		NMOS_BOUNDED_DIODE_L130E	20	5	10	500	1000	
48		PMOS_BOUNDED_DIODE_L130E	20	5	10	500	1000	

Table 2.3 Layout dimensions of three types STI ESD diodes.

Diode					
Item	Type	W (μm)	L (μm)	M	PJ (μm)
1	P	5	5	1	20
2		5	5	2	40
3		5	5	3	60
4		15	5	1	40
5		15	5	2	80
6		15	5	3	120
7		150	30	1	360
8		150	30	3	1080
9		150	30	5	1800
10	N	5	5	1	20
11		5	5	2	40
12		5	5	3	60
13		15	5	1	40
14		15	5	2	80
15		15	5	3	120
16		150	30	1	360
17		150	30	3	1080
18		150	30	5	1800
19	NW	5	5	1	20
20		5	5	2	40
21		5	5	3	60
22		15	5	1	40
23		15	5	2	80
24		15	5	3	120
25		150	30	1	360
26		150	30	3	1080
27		150	30	5	1800

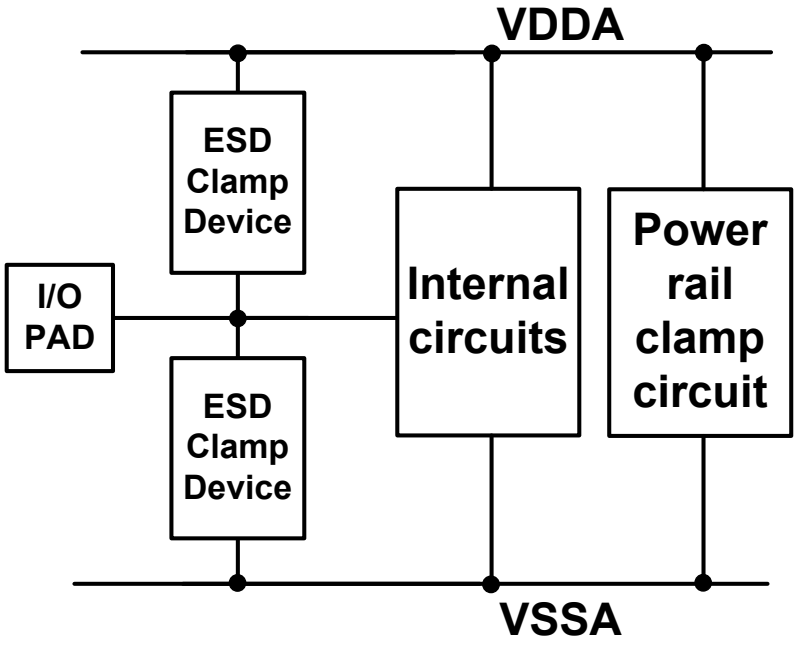


Fig. 2.1 Typical on-chip ESD protection design for input/output (I/O) pad with power rail ESD clamp circuit.

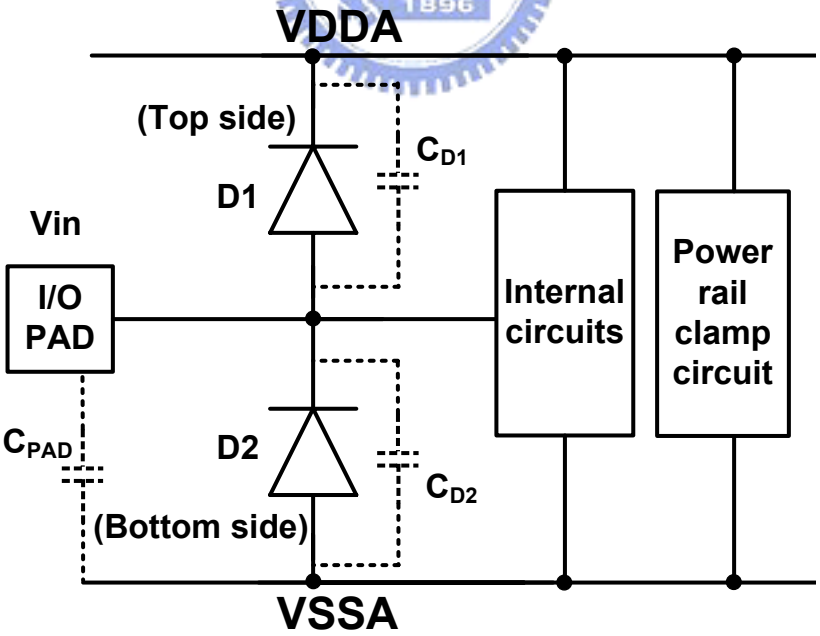
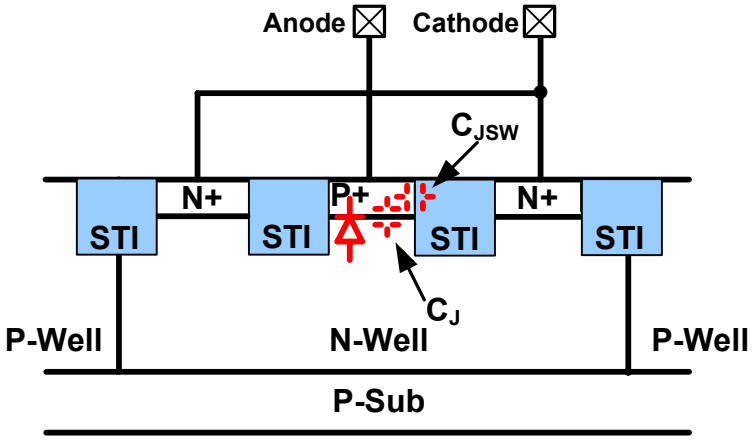
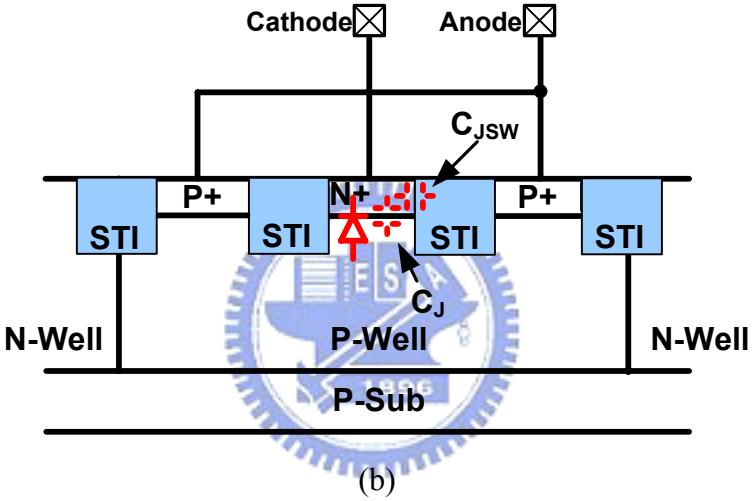


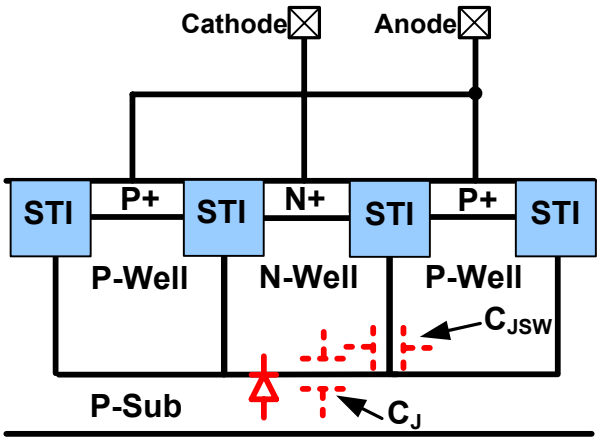
Fig. 2.2 The typical I/O ESD protection circuit constructed by double diodes in CMOS IC.



(a)

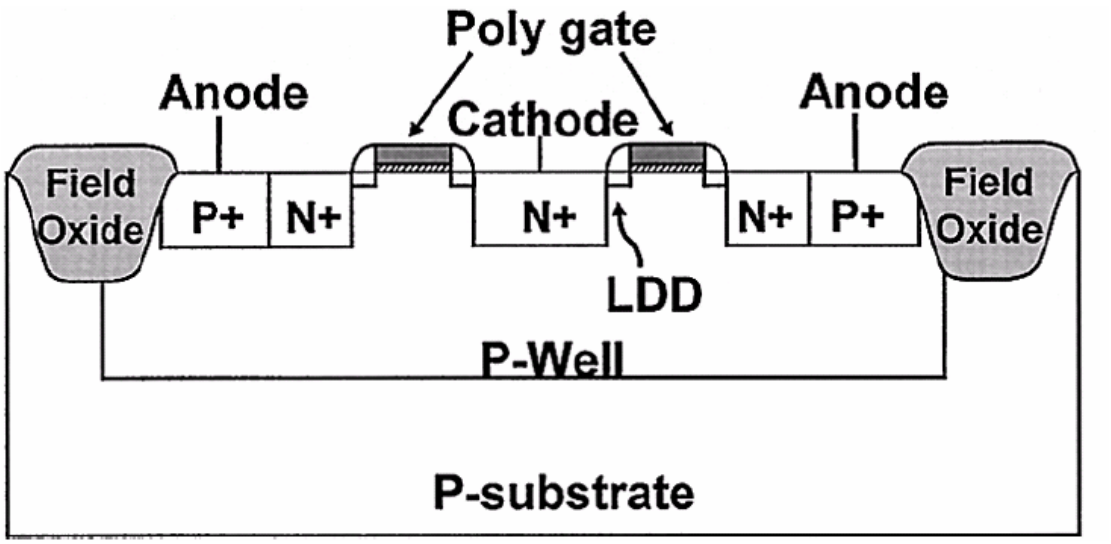


(b)

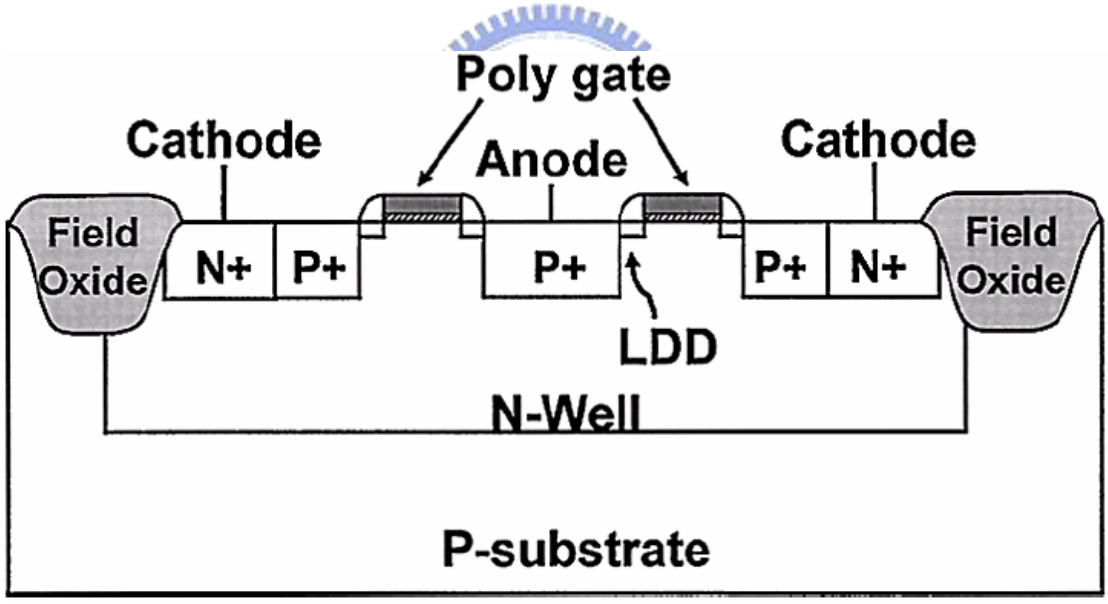


(c)

Fig. 2.3 The schematic cross-sectional view of a STI diode structures (a) P-type (b) N-type, and (c) NW-type.



(a)



(b)

Fig. 2.4 The cross-sectional views of (a) NMOS-bounded diode, and (b) PMOS-bounded diode.

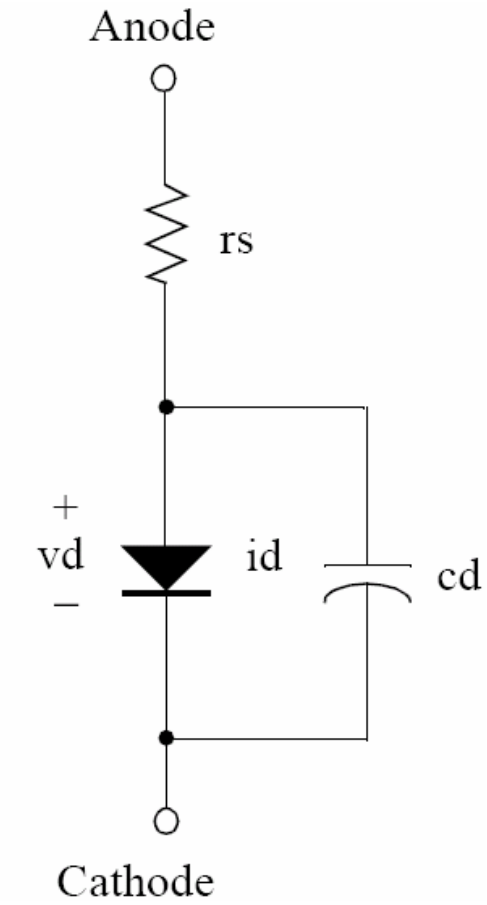


Fig. 2.5 Equivalent circuit model for diodes.

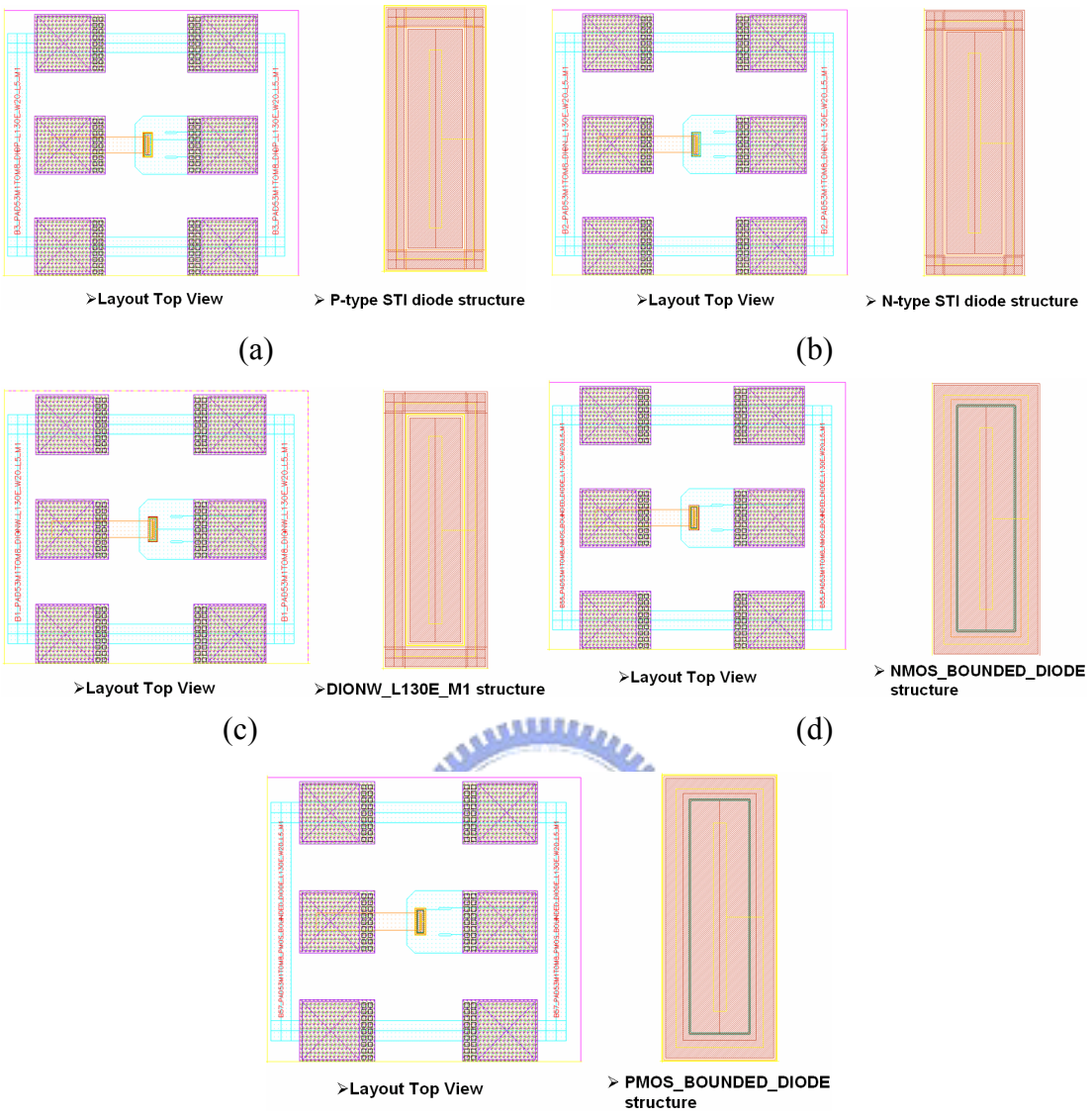


Fig. 2.6 (a) P-type, (b) N-type, (c) NW-type STI diode structures and (d) NMOS-bounded, (e) PMOS-bounded diode structures and (f) layout top view (1500 μm × 4500 μm) of the ESD diode devices with wo-port GSG blocks in a testchip.

CHAPTER 3

EXPERIMENTAL RESULTS ON DIFFERENT ESD DIODE STRUCTURES AND AN EXAMPLE OF ESD PROTECTION DESIGN FOR 5-GHz HIGH-SPEED I/O APPLICATIONS

In this chapter, the experimental results on different ESD diodes are investigated, including the ESD robustness and high-frequency characteristics. The first step is to make sure the right dc I-V curves of diode characteristics when test chips are backed, otherwise we can not confirm the test chips is the right characteristics of ESD diodes or not. When the diode characteristic is confirm, we can start the transmission line pulse generator (TLPG) to measure I-V curves, the purpose is in order to predict the performance of ESD robustness. Besides, the high-frequency S-parameter measurement system is used to evaluate the high-frequency characteristics of different ESD diodes and different bond pad structures. Base on the extracted capacitances of different ESD diodes and different bond pad structures, an example of ESD protection design for 5-GHz high-speed I/O applications is provided. With the design example, the input ESD protection scheme can be quickly designed if the specifications on ESD level and input parasitic capacitance of ESD devices and bond pad are assigned.

3.1 DC I-V CHARACTERISTICS

The curve tracer HP4145B is a semiconductor parameter analyzer, which is shown in Fig. 3.1 is used to measure the devices for investigating the dc

characteristics of ESD diodes. The dc leakage of normal STI diode is around in the order of pA (in 0.13-μm CMOS processes). The dc I-V characteristics of the STI diodes are shown in Fig.3.2, the breakdown voltage is around below 10V and the leakage current of normal operation on voltage 1.2V is around several pA. The dc I-V characteristics of the MOS-bounded diodes are shown in Fig.3.3, the breakdown voltage is around below 2.9V and the leakage current of normal operation voltage on 1.2V is around several nA. Besides, the forward-biased current was compliance due to measurement setup.

3.2 TLP I-V CHARACTERISTICS SECONDARY BREAKDOWN CURRENT (IT2)

The transmission line pulse generator (TLPG) with a pulse width of 100ns [26] is used to investigate ESD robustness of the fabricated diode devices and predict the ESD robustness of ESD devices; include the second breakdown current (It2). The human-body-model (HBM) ESD level (HBM V_{ESD}), and machine-model (MM) ESD level (MM V_{ESD}) can also be estimated by the proper adjustment of TLPG. The setup measurement are combine with high-voltage pulse generator (Keithley 2410), oscilloscope and triple-output power supply (Agilent E3631A) shown as Fig. 3.4. For three types of N-type diodes under forward stress conditions, the R_{ON} resistance is around 1.6Ω, the It2 current is over 6A. However, the It2 current was below 0.7A, which was very weak when under reversed stress condition as shown in Fig. 3.5. For three types of P-type diodes under forward stress conditions, the R_{ON} resistance is around 1.24Ω, the It2 current is over 6A. However, the It2 current was below 0.9A, which was very weak when under reversed stress condition as shown in Fig. 3.6. The

TLP It2 of the P-type diodes with W/L=5μm/5μm and different perimeters (20μm, 40μm, and 60μm) under forward ESD stress conditions are below 1.6A. The TLP It2 of the P-type diodes with W/L=15μm/5μm and different perimeters (40μm, 80μm, and 120μm) under forward ESD stress conditions are below 6A. The TLP It2 of the P-type diodes with W/L=150μm/30μm and different perimeters (360μm, 1080μm, and 1800μm) under forward ESD stress conditions are over 6A. The TLP It2 of the N-type diodes with W/L=5μm/5μm and different perimeters (20μm, 40μm, and 60μm) under forward ESD stress conditions are below 1.58A. The TLP It2 of the N-type diodes with W/L=15μm/5μm and different perimeters (40μm, 80μm, and 120μm) under forward ESD stress conditions are below 6A. The TLP It2 of the N-type diodes with W/L=150μm/30μm and different perimeters (360μm, 1080μm, and 1800μm) under forward ESD stress conditions are over 6A. The TLP It2 of the NW-type diodes with W/L=5μm/5μm and different perimeters (20μm, 40μm, and 60μm) under forward ESD stress conditions are below 1.7A. The TLP It2 of the NW-type diodes with W/L=15μm/5μm and different perimeters (40μm, 80μm, and 120μm) under forward ESD stress conditions are below 6A. The TLP It2 of the NW-type diodes with W/L=150μm/30μm and different perimeters (360μm, 1080μm, and 1800μm) under forward ESD stress conditions are over 6A. The TLP I-V curves of the P-type, N-type, and NW-type ESD diodes under different perimeters were characterized, as shown in Fig. 3.7 – Fig. 3.15 and Table 3.1 – Table 3.3. The experimental result shows that under the same perimeters, the ESD robustness is improved with larger width of the ESD diode.

3.3 HUMAN-BODY-MODEL (HBM) ESD ROBUSTNESS

The human body model is today the most commonly used discharge model in the microelectronic industry. The intention of the model is to reduce a discharge of a charged human being to a device with at least one pin grounded. Although the risk of an IC was getting touched by a charged human being has decreased significantly due to automatic handing. The HBM ESD test standard is well defined by international standards [27]-[29]. The It2 level and HBM ESD level of three types of N-type diodes with different total junction perimeters under forward and reversed ESD stress conditions are shown in Fig. 3.16 and Fig. 3.17. Under forward ESD stress conditions, the It2 level of N-type diode with 50-μm junction perimeters is ~2A, and the HBM ESD level is above 2kV. Under forward ESD stress conditions, the It2 level of N-type diode with 100-μm junction perimeters is ~4A, and the HBM ESD level is above 2kV. Under forward ESD stress conditions, the It2 level of N-type diode with 150-μm junction perimeters is over 6A, and the HBM ESD level is above 2kV. Under forward ESD stress conditions, the It2 level of N-type diode with 200-μm junction perimeters is over 6A, and the HBM ESD level is above 2kV. Under forward ESD stress conditions, the It2 level of N-type diode with 250-μm junction perimeters is over 6A, and the HBM ESD level is above 2kV. Under reversed ESD stress conditions, the It2 level of N-type diode with 50-μm junction perimeters is below 0.2A, and the HBM ESD level is 0.5kV. Under reversed ESD stress conditions, the It2 level of N-type diode with 100-μm junction perimeters is below 0.3A, and the HBM ESD level is 1kV. Under reversed ESD stress conditions, the It2 level of N-type diode with 150-μm junction perimeters is below 0.5A, and the HBM ESD level is 1kV. Under reversed ESD stress conditions, the It2 level of N-type diode with 200-μm junction perimeters is below 0.6A, and the HBM ESD level is 1kV. Under reversed ESD stress conditions, the It2 level of N-type diode with 250-μm junction perimeters is below 0.7A, and the

HBM ESD level is 1.5kV. Under forward ESD stress conditions, the It2 level of NW-type diode with 50-μm junction perimeters is ~2A, and the HBM ESD level is above 2kV. Under forward ESD stress conditions, the It2 level of NW-type diode with 100-μm junction perimeters is ~4A, and the HBM ESD level is above 2kV. Under forward ESD stress conditions, the It2 level of NW-type diode with 150-μm junction perimeters is over 6A, and the HBM ESD level is above 2kV. Under forward ESD stress conditions, the It2 level of NW-type diode with 200-μm junction perimeters is over 6A, and the HBM ESD level is above 2kV. Under forward ESD stress conditions, the It2 level of NW-type diode with 250-μm junction perimeters is over 6A, and the HBM ESD level is above 2kV. Under reversed ESD stress conditions, the It2 level of NW-type diode with 50-μm junction perimeters is below 0.3A, and the HBM ESD level is 0.5kV. Under reversed ESD stress conditions, the It2 level of NW-type diode with 100-μm junction perimeters is below 0.3A, and the HBM ESD level is 0.5kV. Under reversed ESD stress conditions, the It2 level of NW-type diode with 150-μm junction perimeters is below 0.5A, and the HBM ESD level is 1kV. Under reversed ESD stress conditions, the It2 level of NW-type diode with 200-μm junction perimeters is below 0.6A, and the HBM ESD level is 1.5kV. Under reversed ESD stress conditions, the It2 level of NW-type diode with 250-μm junction perimeters is below 0.7A, and the HBM ESD level is 1.5kV. Under forward ESD stress conditions, the It2 level of NMOS-bonded-type diode with 50-μm junction perimeters is ~2A, and the HBM ESD level is 1.5kV. Under forward ESD stress conditions, the It2 level of NMOS-bonded-type diode with 250-μm junction perimeters is over 6A, and the HBM ESD level is above 2kV. Under forward ESD stress conditions, the It2 level of NMOS-bonded-type diode with 500-μm junction perimeters is over 6A, and the HBM

ESD level is above 2kV. Under reversed ESD stress conditions, the It2 level of NMOS-bonded-type with 50-μm junction perimeters is below 0.2A, and the HBM ESD level is 0.5kV. Under reversed ESD stress conditions, the It2 level of NMOS-bonded-type diode with 250-μm junction perimeters is below 0.4A, and the HBM ESD level is 1kV. Under reversed ESD stress conditions, the It2 level of NMOS-bonded-type diode with 500-μm junction perimeters is below 1.4A, and the HBM ESD level is 2kV. The HBM ESD levels are greater then 2kV and the It2 currents are larger than 6A when perimeters of the three types of N-type diodes are greater then 150 μm. By interpolation, the diode junction perimeters can be determined (around above 35.4μm) when It2 current on 1.4A in order to sustain 2kV HBM ESD level, thus, the minimum sizes of N-type diodes can be evaluated. Under forward ESD stress conditions, the It2 level of P-type diode with 50-μm junction perimeters is ~3A, and the HBM ESD level is above 2kV. Under forward ESD stress conditions, the It2 level of P-type diode with 150-μm junction perimeters is over 6A, and the HBM ESD level is above 2kV. Under forward ESD stress conditions, the It2 level of P-type diode with 200-μm junction perimeters is over 6A, and the HBM ESD level is above 2kV. Under forward ESD stress conditions, the It2 level of P-type diode with 250-μm junction perimeters is over 6A, and the HBM ESD level is above 2kV. Under reversed ESD stress conditions, the It2 level of P-type diode with 50-μm junction perimeters is below 0.2A, and the HBM ESD level is 1kV. Under reversed ESD stress conditions, the It2 level of P-type diode with 150-μm junction perimeters is ~0.5A, and the HBM ESD level is 1.5kV. Under reversed ESD stress conditions, the It2 level of P-type diode with 200-μm junction perimeters is below 0.7A, and the HBM ESD level is 2kV. Under reversed ESD stress conditions, the It2 level of P-type

diode with 250-μm junction perimeters is below 0.9A, and the HBM ESD level is 2kV. Under forward ESD stress conditions, the It2 level of PMOS-bonded-type diode with 50-μm junction perimeters is ~3A, and the HBM ESD level is above 2kV. Under forward ESD stress conditions, the It2 level of PMOS-bonded-type diode with 250-μm junction perimeters is over 6A, and the HBM ESD level is above 2kV. Under forward ESD stress conditions, the It2 level of PMOS-bonded-type diode with 500-μm junction perimeters is over 6A, and the HBM ESD level is above 2kV. Under reversed ESD stress conditions, the It2 level of PMOS-bonded-type with 50-μm junction perimeters is below 0.2A, and the HBM ESD level is 0.5kV. Under reversed ESD stress conditions, the It2 level of PMOS-bonded-type diode with 250-μm junction perimeters is below 0.6A, and the HBM ESD level is 1.5kV. Under reversed ESD stress conditions, the It2 level of PMOS-bonded-type diode with 500-μm junction perimeters is below 1.4A, and the HBM ESD level is 2kV. The It2 level and HBM ESD level of two types of P-type diodes with different total junction perimeters under forward and reversed ESD stress conditions are shown in Fig. 3.18 and Fig. 3.19. The HBM ESD levels are greater then 2kV and the It2 currents are larger than 6A when perimeters of the two types of P-type diodes are greater then 150 μm. By interpolation, the diode junction perimeters can be determined (around above 24.1μm) when It2 current on 1.4A in order to sustain 2kV HBM ESD level, thus, the minimum sizes of P-type diodes can be evaluated.

3.4 MACHINE-MODEL (MM) ESD ROBUSTNESS

The reverse bias and forward bias of three types of N-type diodes with different total junction perimeters under MM ESD stress conditions are shown in Fig. 3.20.

Under forward ESD stress conditions, the MM ESD level of N-type diode with 50-μm junction perimeters is 250V. Under forward ESD stress conditions, the MM ESD level of N-type diode with 100-μm junction perimeters is 200V. Under forward ESD stress conditions, the MM ESD level of N-type diode with 150-μm junction perimeters is 300V. Under forward ESD stress conditions, the MM ESD level of N-type diode with 200-μm junction perimeters is 350V. Under forward ESD stress conditions, the MM ESD level of N-type diode with 250-μm junction perimeters is 350V. Under reversed ESD stress conditions, the MM ESD level of N-type diode with 50-μm junction perimeters is 50V. Under reversed ESD stress conditions, the MM ESD level of N-type diode with 100-μm junction perimeters is 50V. Under reversed ESD stress conditions, the MM ESD level of N-type diode with 150-μm junction perimeters is 100V. Under reversed ESD stress conditions, the MM ESD level of N-type diode with 200-μm junction perimeters is 100V. Under reversed ESD stress conditions, the MM ESD level of N-type diode with 250-μm junction perimeters is 100V. Under forward ESD stress conditions, the MM ESD level of NW-type diode with 50-μm junction perimeters is 200V. Under forward ESD stress conditions, the MM ESD level of NW-type diode with 100-μm junction perimeters is 250V. Under forward ESD stress conditions, the MM ESD level of NW-type diode with 150-μm junction perimeters is 350V. Under forward ESD stress conditions, the MM ESD level of NW-type diode with 200-μm junction perimeters is 400V. Under forward ESD stress conditions, the MM ESD level of NW-type diode with 250-μm junction perimeters is 400V. Under reversed ESD stress conditions, the MM ESD level of NW-type diode with 50-μm junction perimeters is 100V. Under reversed ESD stress conditions, the MM ESD level of NW-type diode with 100-μm junction perimeters is 100V. Under reversed

ESD stress conditions, the MM ESD level of NW-type diode with 150-μm junction perimeters is 150V. Under reversed ESD stress conditions, the MM ESD level of NW-type diode with 200-μm junction perimeters is 150V. Under reversed ESD stress conditions, the MM ESD level of NW-type diode with 250-μm junction perimeters is 150V. Under forward ESD stress conditions, the MM ESD level of NMOS-bonded-type diode with 50-μm junction perimeters is 100V. Under forward ESD stress conditions, the MM ESD level of NMOS-bonded-type diode with 250-μm junction perimeters is 200V. Under forward ESD stress conditions, the MM ESD level of NMOS-bonded-type diode with 500-μm junction perimeters is 450V. Under reversed ESD stress conditions, the MM ESD level of NMOS-bonded-type diode with 50-μm junction perimeters is 50V. Under reversed ESD stress conditions, the MM ESD level of NMOS-bonded-type diode with 250-μm junction perimeters is 100V. Under reversed ESD stress conditions, the MM ESD level of NMOS-bonded-type diode with 500-μm junction perimeters is 150V. Under forward ESD stress conditions, the MM ESD level of P-type diode with 50-μm junction perimeters is 200V. Under forward ESD stress conditions, the MM ESD level of P-type diode with 150-μm junction perimeters is 300V. Under forward ESD stress conditions, the MM ESD level of P-type diode with 200-μm junction perimeters is 350V. Under forward ESD stress conditions, the MM ESD level of P-type diode with 250-μm junction perimeters is 400V. Under reversed ESD stress conditions, the MM ESD level of P-type diode with 50-μm junction perimeters is 50V. Under reversed ESD stress conditions, the MM ESD level of P-type diode with 150-μm junction perimeters is 100V. Under reversed ESD stress conditions, the MM ESD level of P-type diode with 200-μm junction perimeters is 100V. Under reversed ESD stress conditions, the MM ESD level of

P-type diode with 250-μm junction perimeters is 100V. Under forward ESD stress conditions, the MM ESD level of PMOS-bonded-type diode with 50-μm junction perimeters is 250V. Under forward ESD stress conditions, the MM ESD level of PMOS-bonded-type diode with 250-μm junction perimeters is 250V. Under forward ESD stress conditions, the MM ESD level of PMOS-bonded-type diode with 500-μm junction perimeters is 500V. Under reversed ESD stress conditions, the MM ESD level of PMOS-bonded-type diode with 50-μm junction perimeters is 50V. Under reversed ESD stress conditions, the MM ESD level of PMOS-bonded-type diode with 250-μm junction perimeters is 100V. Under reversed ESD stress conditions, the MM ESD level of PMOS-bonded-type diode with 500-μm junction perimeters is 150V. The MM ESD level of maximum diode junction perimeters is above 300V when under forward stress conditions. However, the MM ESD level of maximum diode junction perimeters is below 150V when under reverse stress conditions. The reverse bias and forward bias of two types of P-type diodes with different total junction perimeters under MM ESD stress conditions are shown in Fig. 3.21. The MM ESD level of maximum diode junction perimeters is above 400V when under forward stress conditions. However, the MM ESD level of maximum diode junction perimeters is below 100V when under reverse stress conditions.

3.5 PARASITIC CAPACITANCE OF ESD DIODES AT 5-GHz

About the high frequency S-parameter measurement system, combine with network analyzer (HP 8510C), S-parameters test set (HP 8517B), synthesized sweeper (HP 83651A), DC source monitor (HP 4142B), RF probe station & microscope as

shown in Fig. 3.22, are used for investigate the parasitic characteristics at 5-GHz. The measured parasitic capacitance of stand-alone pads (70 μm × 60 μm) is shown in Fig. 3.23 and Table 3.4. The diodes were investigated by two-port GSG pad structure to measure the parasitic capacitance. At the first, we simulated the parasitic capacitance of diodes under different junction perimeters in zero bias conditions are shown in Fig. 3.24 and Table 3.5 for reference. After GSG de-embedded, the N-type diodes parasitic capacitance under zero biases is shown in Fig. 3.25 and Table 3.6, the parasitic capacitance at 5-GHz is 18.16fF of N-type diode with 60-μm perimeters, and the parasitic capacitance at 5-GHz is 62.25fF of N-type diode with 120-μm perimeters, and the parasitic capacitance at 5-GHz is 628.87fF of N-type diode with 1800-μm perimeters. The P-type diodes parasitic capacitance under zero biases are shown in Fig. 3.26 and Table 3.7, the parasitic capacitance at 5-GHz is 42.62fF of P-type diode with 60-μm perimeters, and the parasitic capacitance at 5-GHz is 52.85fF of P-type diode with 120-μm perimeters, and the parasitic capacitance at 5-GHz is 410.88fF of P-type diode with 1800-μm perimeters. The NW-type diodes parasitic capacitance under zero biases is shown in Fig. 3.27 and Table 3.8, the parasitic capacitance at 5-GHz is 60.97fF of NW-type diode with 60-μm perimeters, and the parasitic capacitance at 5-GHz is 55.04fF of NW-type diode with 120-μm perimeters, and the parasitic capacitance at 5-GHz is 290.65fF of NW-type diode with 1800-μm perimeters.

3.6 ESD PROTECTION DESIGN EXAMPLE FOR 5-GHz HIGH-SPEED I/O APPLICATIONS

In order to achieve the minimum parasitic capacitance, and above 2kV HBM

ESD level, the junction perimeter of the N-type diode can be determined by interpolation (which is around 35.4μm), and the junction perimeter of the P-type diode can be determined by interpolation (which is around 24.1μm) to have the It2 current of 1.4A, which corresponds 2kV HBM ESD level. The parasitic capacitance combine with three types of bond pad structures and three types of diodes under different junction perimeters are listed. The total parasitic capacitance of bond pad in structure I (metal 1 to metal 8) with the N-type diode size determined by interpolation (which is around 35.4μm) and the P-type diode size determined by interpolation (which is around 24.1μm) is around 420.77fF. The total parasitic capacitance of bond pad in structure II (metal 6 to metal 8) with the N-type diode size determined by interpolation (which is around 35.4μm) and the P-type diode size determined by interpolation (which is around 24.1μm) is around 120.47fF. The total parasitic capacitance of bond pad in structure III (metal 8) with the N-type diode size determined by interpolation (which is around 35.4μm) and the P-type diode size determined by interpolation (which is around 24.1μm) is around 103.87fF. The optimize design example are summarize and listed as shown in Fig. 3.28 and Table 3.9 – Table 3.11.

3.7 SUMMARY

The ESD robustness and high-frequency characteristics of different ESD diode structures are investigated, under the same perimeter, the parasitic capacitance of P-type ESD diode is greater then the other types due to heavy doping of p-n junction. Besides, the ESD robustness of NW-type is greater then the other types because large p-n junction can discharge ESD current more efficiently. The high-speed I/O ESD

protection design with low enough parasitic capacitance and high enough ESD level had been actually verified in a 0.13-μm CMOS process. This extracted database can be further referenced for high-speed I/O design in 0.13-μm CMOS processes.

Table 3.1 The ESD robustness of P-type diode.

Item	P-type Diode									
	W (μm)	L (μm)	M	PJ (μm)	DC Parasitic Cap. (fF)	ESD Robustness				
						It2 (A)	HBM (kV)	MM (V)	CDM (V)	
									(+)	(-)
1	5	5	1	20	25.93	0.62	1	50	350	> 500
2			2	40	51.85	1.17	2	100	500	> 500
3			3	60	77.78	1.60	2.5	150	> 500	> 500
4	15	5	1	40	75.68	1.47	3	150	> 500	> 500
5			2	80	151.35	4.18	6	200	> 500	> 500
6			3	120	227.03	> 6.00	> 8	250	> 500	> 500
7	150	30	1	360	10374.30	> 6.00	> 8	400	> 500	> 500
8			3	1080	31122.90	> 6.00	> 8	800	> 500	> 500
9			5	1800	51871.50	> 6.00	> 8	1000	> 500	> 500

Table 3.2 The ESD robustness of N-type diode.

Item	N-type Diode									
	W (μm)	L (μm)	M	PJ (μm)	DC Parasitic Cap. (fF)	ESD Robustness				
						It2 (A)	HBM (kV)	MM (V)	CDM (V)	
									(+)	(-)
1	5	5	1	20	20.04	0.55	1	100	> 500	500
2			2	40	40.07	0.97	2	100	> 500	> 500
3			3	60	60.11	1.58	3	150	> 500	500
4	15	5	1	40	58.12	1.56	3	100	> 500	> 500
5			2	80	116.24	3.75	6	200	> 500	> 500
6			3	120	174.36	> 6.00	> 8	250	> 500	> 500
7	150	30	1	360	7875.10	> 6.00	> 8	100	> 500	> 500
8			3	1080	23625.20	> 6.00	> 8	150	> 500	> 500
9			5	1800	39375.30	> 6.00	> 8	200	> 500	> 500

Table 3.3 The ESD robustness of NW-type diode.

Item	NW-type Diode									
	W (μm)	L (μm)	M	PJ (μm)	DC Parasitic Cap. (fF)	ESD Robustness				
						It2 (A)	HBM (kV)	MM (V)	CDM (V)	
									(+)	(-)
1	5	5	1	20	24.10	0.61	1	50	> 500	450
2			2	40	48.20	1.38	2	100	> 500	> 500
3			3	60	72.30	1.70	3	100	> 500	> 500
4	15	5	1	40	52.10	1.84	3	100	> 500	> 500
5			2	80	104.20	3.90	6	150	> 500	> 500
6			3	120	156.30	> 6.00	> 8	200	> 500	> 500
7	150	30	1	360	2472.60	> 6.00	> 8	500	> 500	> 500
8			3	1080	7417.80	> 6.00	> 8	700	> 500	> 500
9			5	1800	12363.00	> 6.00	> 8	1050	> 500	> 500

Table 3.4 The measured parasitic capacitance of empty pads (70 μm × 60 μm) under different DC biases for different pad structures.

Pad/Cap.		Capacitance (fF)			
		DC=0V	DC=0.1V	DC=0.5V	DC=1V
Metal 1 - Metal 8	2.5 GHz	74.81	73.62	68.53	63.75
	5 GHz	65.03	64.1	58.9	55.51
metal 6 - Metal 8	2.5 GHz	52.21	52.25	52.25	52.29
	5 GHz	47.3	47.26	47.28	47.25
Metal 8	2.5 GHz	3.72	3.75	3.75	3.65
	5 GHz	1.7	1.72	1.62	1.62

Table 3.5 The parasitic capacitance of diodes under different junction perimeters in zero bias conditions.

Parasitic Capacitance			
PJ (μm)	DION_L130E (fF)	DIONW_L130E (fF)	DIOP_L130E (fF)
50	77.17	66.10	100.55
100	154.33	132.20	201.10
150	231.50	198.30	301.65
200	308.66	264.40	402.20
250	385.83	330.50	502.75

Table 3.6 The N-type diodes parasitic capacitance under zero biases.

N-Type Diode						
W (μm)	L (μm)	M	PJ (μm)	Zero-Biased Parasitic Capacitance (fF)		
				Freq. 0.1GHz	Freq. 2.5GHz	Freq. 5GHz
5	5	1	20	48.75	37.87	37.27
5	5	2	40	77.35	59.68	37.15
5	5	3	60	99.91	35.23	18.16
15	5	1	40	124.26	66.32	48.78
15	5	2	80	203.50	89.71	56.51
15	5	3	120	228.04	116.86	62.25
150	30	1	360	3842.41	410.26	121.66
150	30	3	1080	686.09	628.82	309.69
150	30	5	1800	5056.51	879.12	628.87

Table 3.7 The P-type diodes parasitic capacitance under zero biases.

P-Type Diode						
W (μm)	L (μm)	M	PJ (μm)	Zero-Biased Parasitic Capacitance (fF)		
				Freq. 0.1GHz	Freq. 2.5GHz	Freq. 5GHz
5	5	1	20	57.77	27.92	28.36
5	5	2	40	38.93	44.09	32.86
5	5	3	60	58.66	54.94	42.62
15	5	1	40	32.36	51.14	44.71
15	5	2	80	88.39	77.70	48.82
15	5	3	120	159.91	112.98	52.85
150	30	1	360	845.29	428.25	306.57
150	30	3	1080	2269.96	540.34	470.54
150	30	5	1800	2001.79	603.51	410.88

Table 3.8 The NW-type diodes parasitic capacitance under zero biases.

NW-Type Diode						
W (μm)	L (μm)	M	PJ (μm)	Zero-Biased Parasitic Capacitance (fF)		
				Freq. 0.1GHz	Freq. 2.5GHz	Freq. 5GHz
5	5	1	20	30.97	40.47	39.98
5	5	2	40	79.24	55.68	48.27
5	5	3	60	100.88	71.03	60.97
15	5	1	40	85.25	69.27	49.74
15	5	2	80	107.27	81.92	50.98
15	5	3	120	110.17	122.38	55.04
150	30	1	360	1365.59	347.58	215.16
150	30	3	1080	1336.02	508.89	421.73
150	30	5	1800	2221.19	485.70	290.65

Table 3.9 The combinations of parasitic effects by using metal 1 to metal 8 layers of bond pad structure.

PJ (μm)	C_{pad1} (fF)		C_{DIOP_L130E} (fF)		C_{DION_L130E} (fF)		C_{Total1} (fF)
25.00	342.00	+	38.36	+	29.56	=	409.92
30.00			50.80		39.10		431.90
35.00			63.24		48.60		453.84
40.00			75.68		58.12		475.80
45.00			88.11		67.64		497.75
50.00			100.55		77.17		519.72
100.00			201.10		154.33		697.43
150.00			301.65		231.50		875.15
200.00			402.20		308.66		1052.86
250.00			502.75		385.83		1230.58
PJ (μm)	C_{pad1} (fF)		C_{DIOP_L130E} (fF)		C_{DIONW_L130E} (fF)		C_{Total1} (fF)
25.00	342.00	+	38.36	+	31.10	=	411.46
30.00			50.80		38.10		430.90
35.00			63.24		45.10		450.34
40.00			75.68		52.10		469.78
45.00			88.11		59.10		489.21
50.00			100.55		66.10		508.65
100.00			201.10		132.20		675.30
150.00			301.65		198.30		841.95
200.00			402.20		264.40		1008.60
250.00			502.75		330.50		1175.25

Table 3.10 The combinations of parasitic effects by using metal 6 to metal 8 layers of bond pad structure.

PJ (μm)	C_{pad2} (fF)		C_{DIOP_L130E} (fF)		C_{DION_L130E} (fF)		C_{Total2} (fF)
25.00	41.70	+	38.36	+	29.56	=	109.62
30.00			50.80		39.10		131.60
35.00			63.24		48.60		153.54
40.00			75.68		58.12		175.50
45.00			88.11		67.64		197.45
50.00			100.55		77.17		219.42
100.00			201.10		154.33		397.13
150.00			301.65		231.50		574.85
200.00			402.20		308.66		752.56
250.00			502.75		385.83		930.28
PJ (μm)	C_{pad2} (fF)		C_{DIOP_L130E} (fF)		C_{DIONW_L130E} (fF)		C_{Total2} (fF)
25.00	41.70	+	38.36	+	31.10	=	111.16
30.00			50.80		38.10		130.60
35.00			63.24		45.10		150.04
40.00			75.68		52.10		169.48
45.00			88.11		59.10		188.91
50.00			100.55		66.10		208.35
100.00			201.10		132.20		375.00
150.00			301.65		198.30		541.65
200.00			402.20		264.40		708.30
250.00			502.75		330.50		874.95

Table 3.11 The combinations of parasitic effects by using only metal 8 layer of bond pad structure.

PJ (μm)	C_{pad3} (fF)		C_{DIOP_L130E} (fF)		C_{DION_L130E} (fF)		C_{Total3} (fF)
25.00	25.10	+	38.36	+	29.56	=	93.02
30.00			50.80		39.10		115.00
35.00			63.24		48.60		136.94
40.00			75.68		58.12		158.90
45.00			88.11		67.64		180.85
50.00			100.55		77.17		202.82
100.00			201.10		154.33		380.53
150.00			301.65		231.50		558.25
200.00			402.20		308.66		735.96
250.00			502.75		385.83		913.68
PJ (μm)	C_{pad3} (fF)		C_{DIOP_L130E} (fF)		C_{DIONW_L130E} (fF)		C_{Total3} (fF)
25.00	25.10	+	38.36	+	31.10	=	94.56
30.00			50.80		38.10		114.00
35.00			63.24		45.10		133.44
40.00			75.68		52.10		152.88
45.00			88.11		59.10		172.31
50.00			100.55		66.10		191.75
100.00			201.10		132.20		358.40
150.00			301.65		198.30		525.05
200.00			402.20		264.40		691.70
250.00			502.75		330.50		858.35

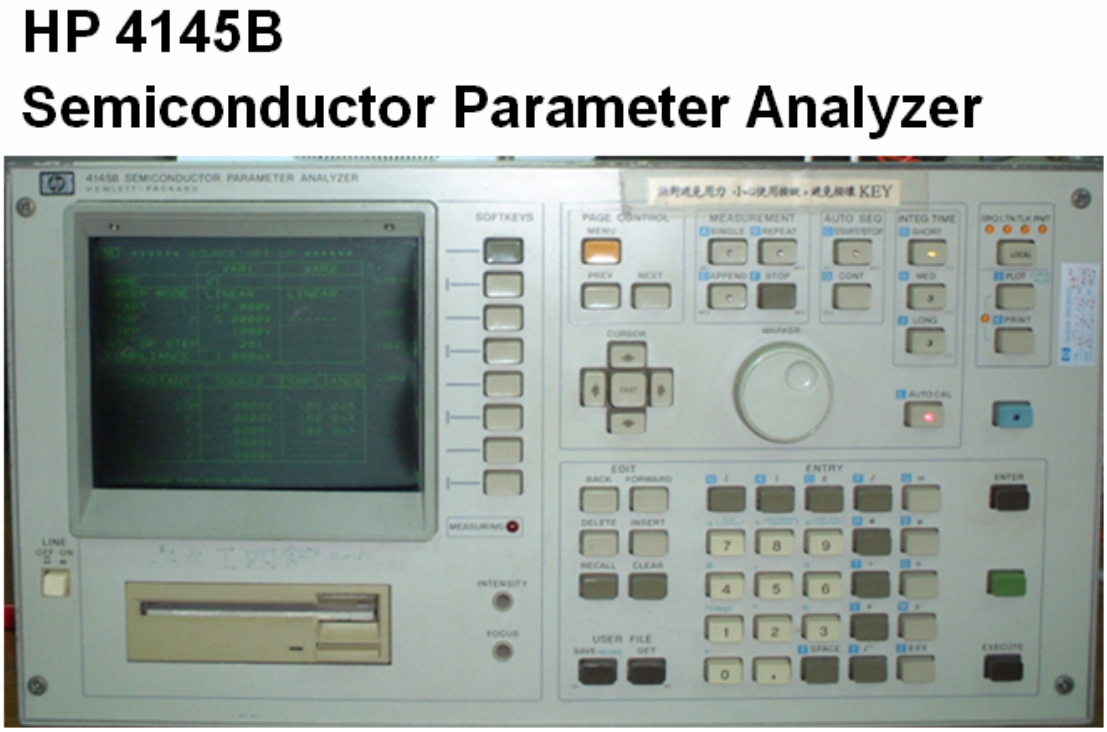


Fig. 3.1 The curve tracer HP 4145B.

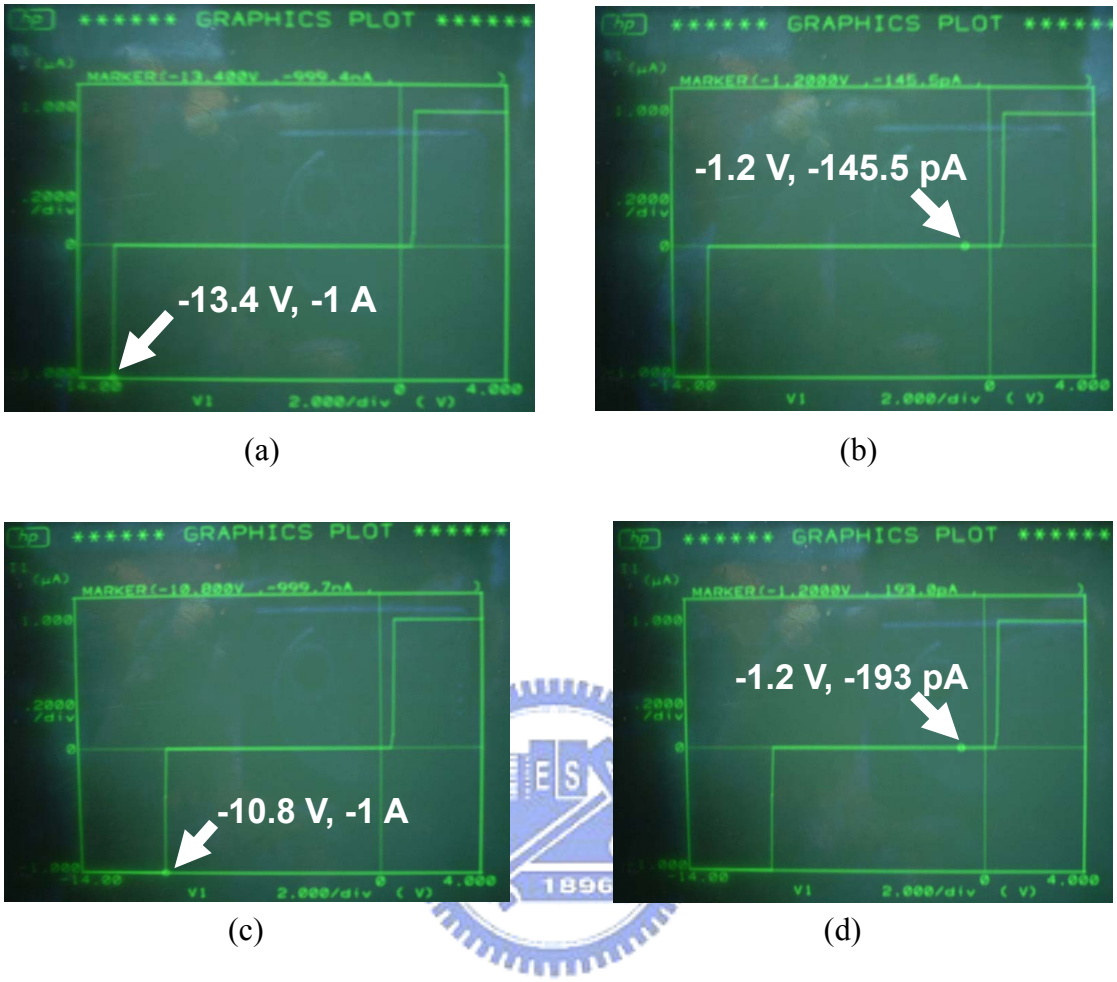


Fig. 3.2 The (a) DC I-V characteristic and (b) leakage currents of N-type diodes, and the (c) DC I-V characteristic and (d) leakage currents of P-type diodes, and the (e) DC I-V characteristic and (f) leakage currents of NW-type diodes.

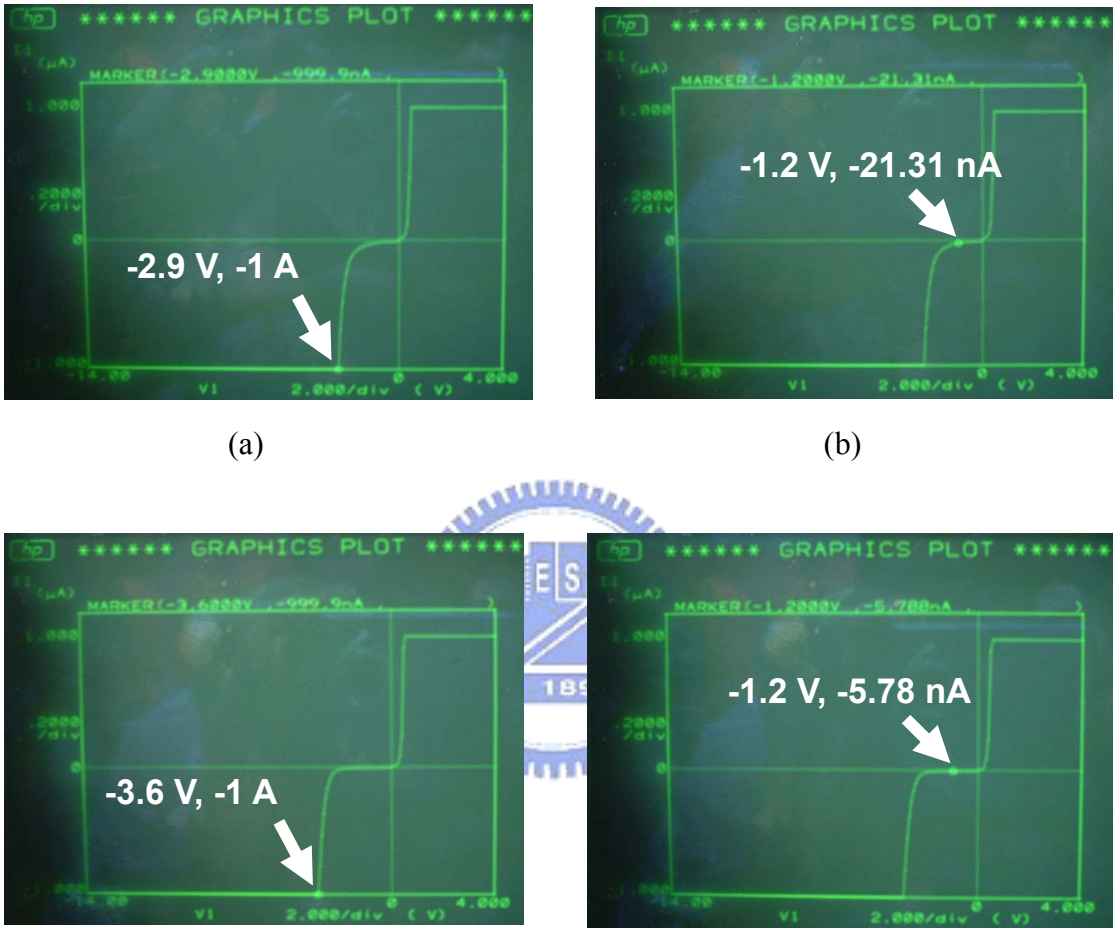


Fig. 3.3 The (a) DC I-V characteristic and (b) leakage currents of NMOS-Bounded diodes, and the (c) DC I-V characteristic and (d) leakage currents of PMOS-Bounded diodes.

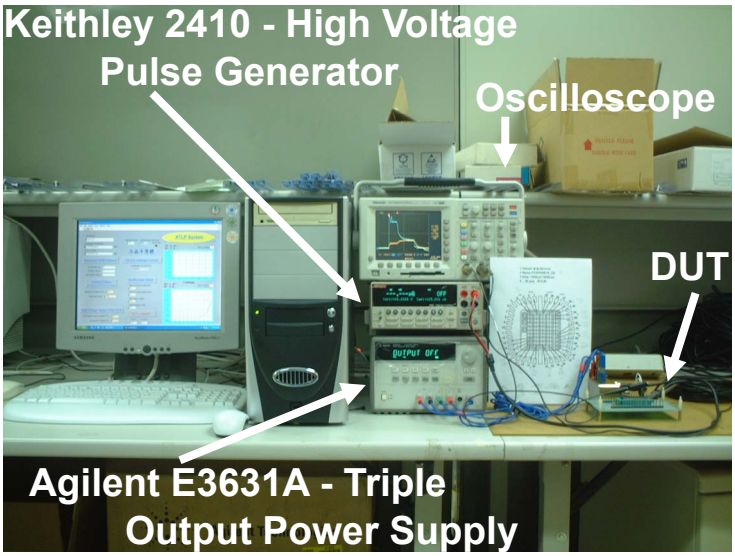


Fig. 3.4 The transmission line pulse generator (TLPG) setup environment.

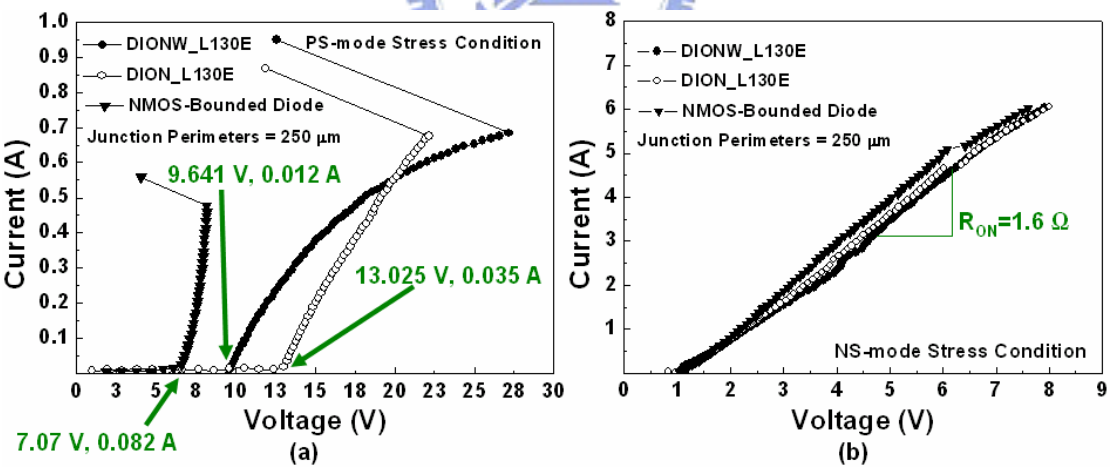


Fig. 3.5 The TLP-measured I-V characteristics of N-type diodes (a) under reversed mode stress and (b) forward mode stress conditions.

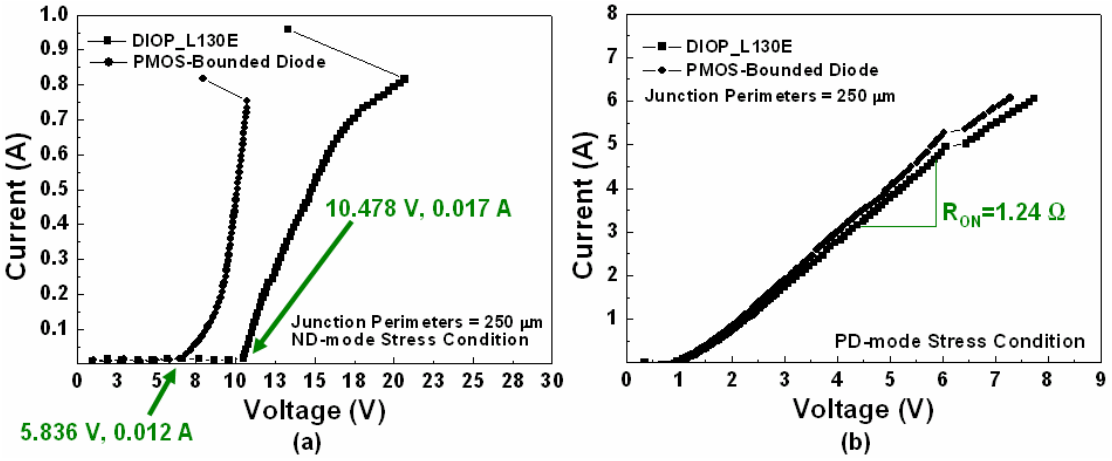


Fig. 3.6 The TLP-measured I-V characteristics of P-type diodes (a) under reversed mode stress and (b) forward mode stress conditions.

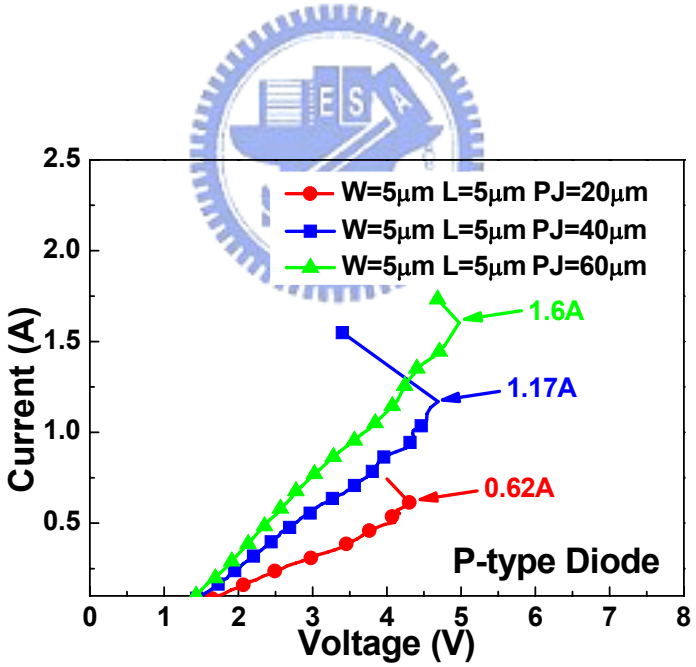


Fig. 3.7 The It2 level of P-type diode (W=5μm, L=5μm) with different fingers under forward mode ESD stress conditions.

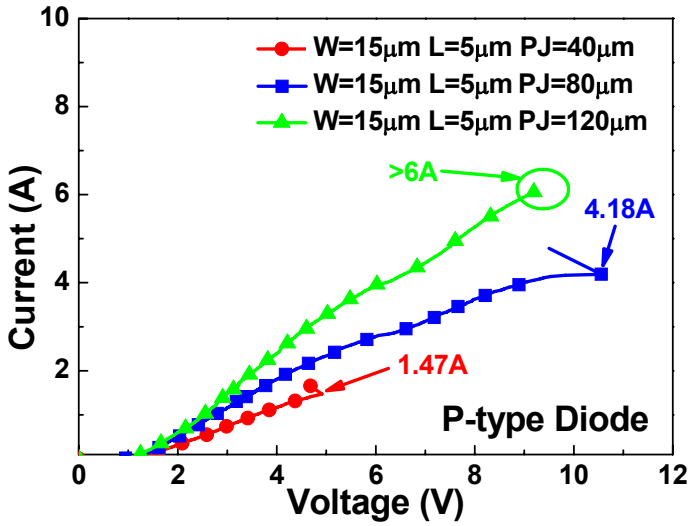


Fig. 3.8 The It2 level of P-type diode (W=15μm, L=5μm) with different fingers under forward mode ESD stress conditions.

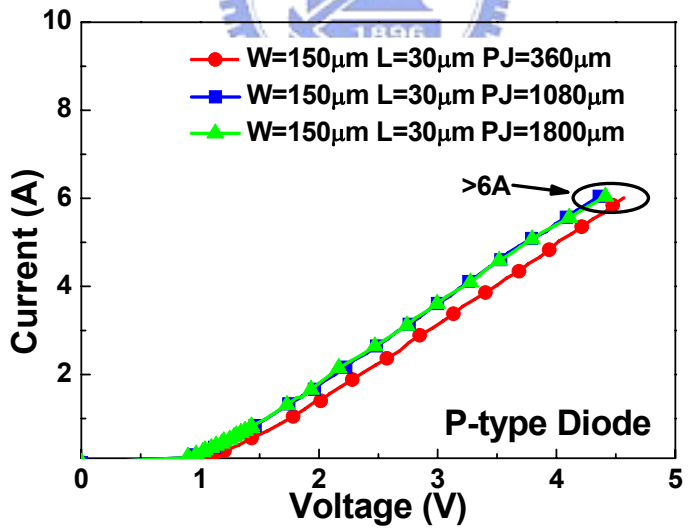


Fig. 3.9 The It2 level of P-type diode (W=150μm, L=30μm) with different fingers under forward mode ESD stress conditions.

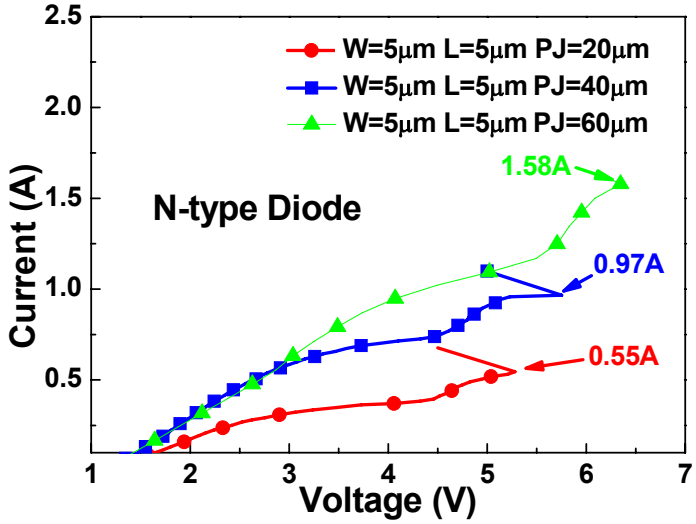


Fig. 3.10 The It2 level of N-type diode (W=5μm, L=5μm) with different fingers under forward mode ESD stress conditions.

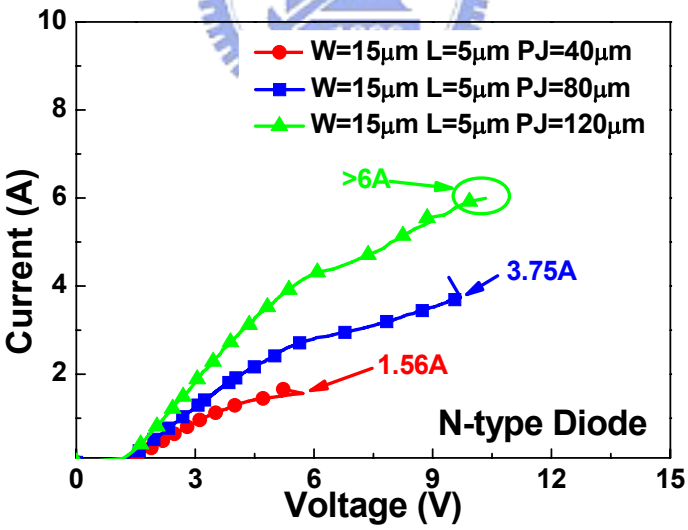


Fig. 3.11 The It2 level of N-type diode (W=15μm, L=5μm) with different fingers under forward mode ESD stress conditions.

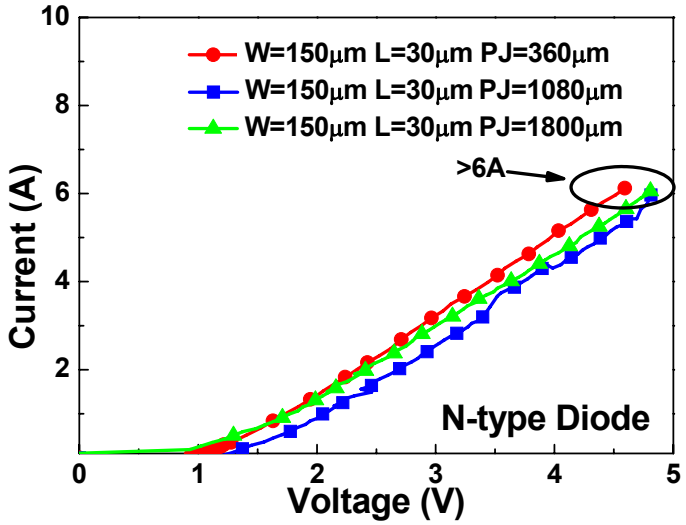


Fig. 3.12 The It2 level of N-type diode (W=150μm, L=30μm) with different fingers under forward mode ESD stress conditions.

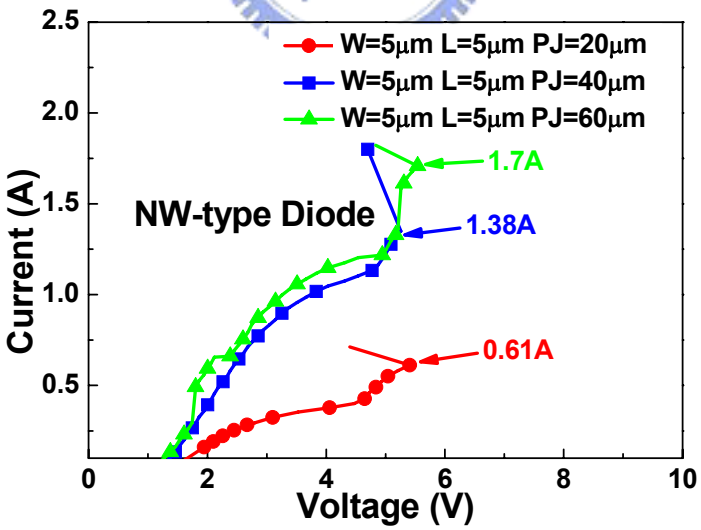


Fig. 3.13 The It2 level of NW-type diode (W=5μm, L=5μm) with different fingers under forward mode ESD stress conditions.

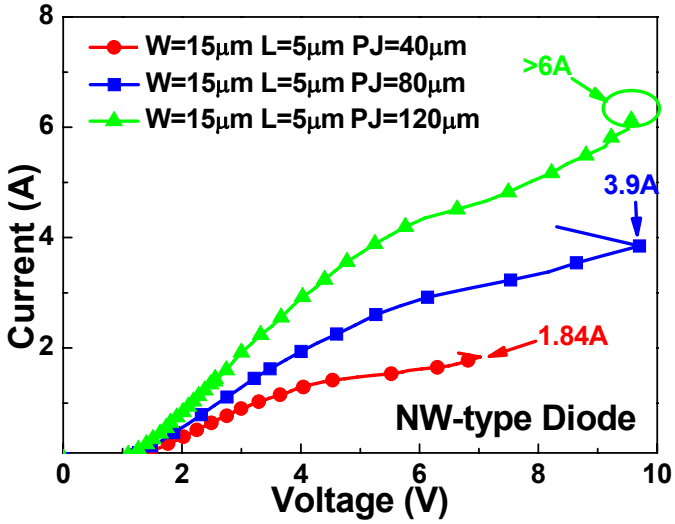


Fig. 3.14 The It2 level of NW-type diode (W=15μm, L=5μm) with different fingers under forward mode ESD stress conditions.

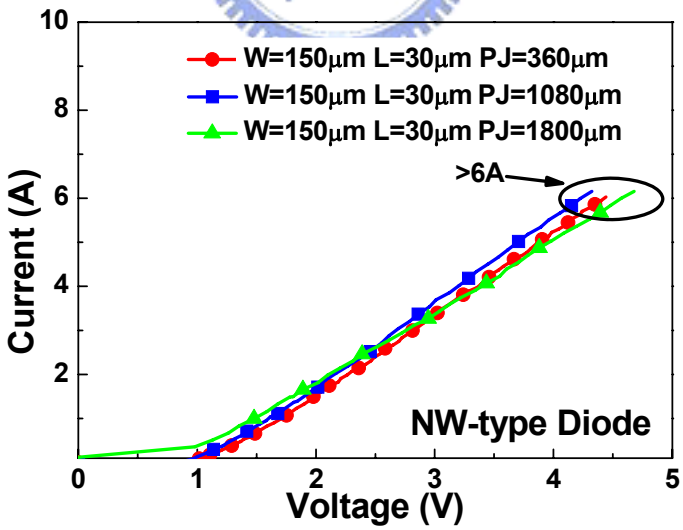


Fig. 3.15 The It2 level of NW-type diode (W=150μm, L=30μm) with different fingers under forward mode ESD stress conditions.

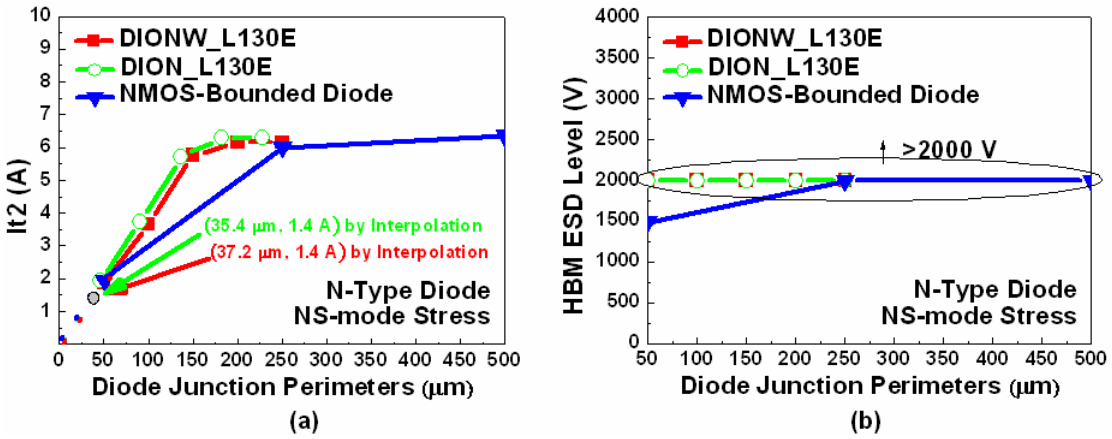


Fig. 3.16 The (a) It2 level, and (b) HBM ESD level, of N-type diode with different total junction perimeters under forward mode ESD stress conditions.

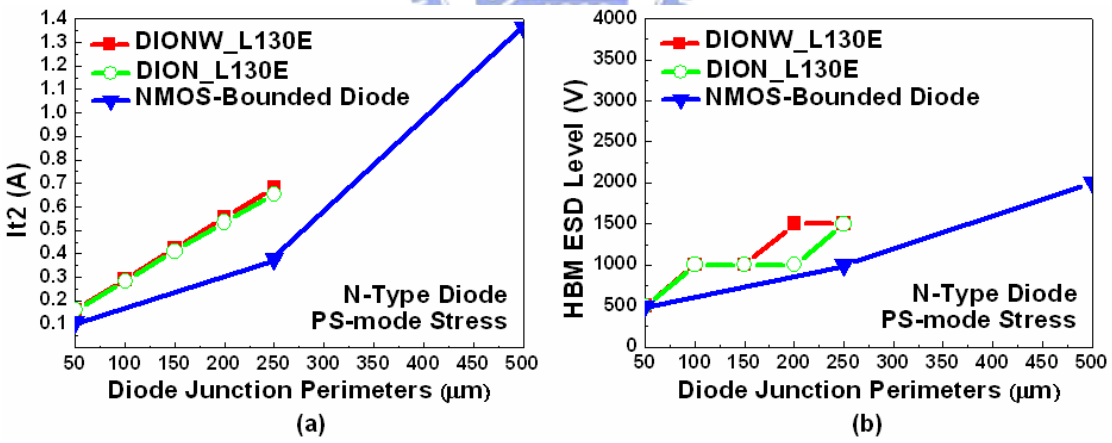


Fig. 3.17 The (a) It2 level, and (b) HBM ESD level, of N-type diode with different total junction perimeters under reversed mode ESD stress conditions.

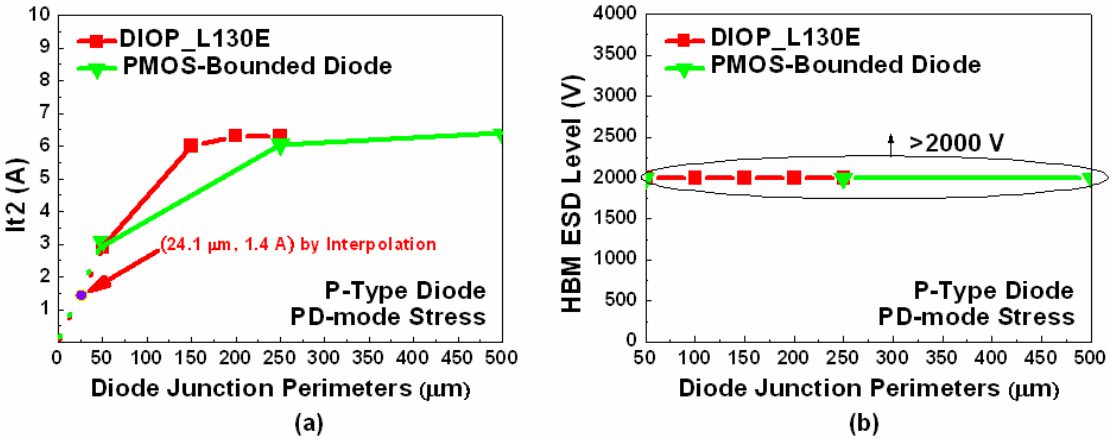


Fig. 3.18 The (a) It2 level, and (b) HBM ESD level, of P-type diode with different total junction perimeters under forward mode ESD stress conditions.

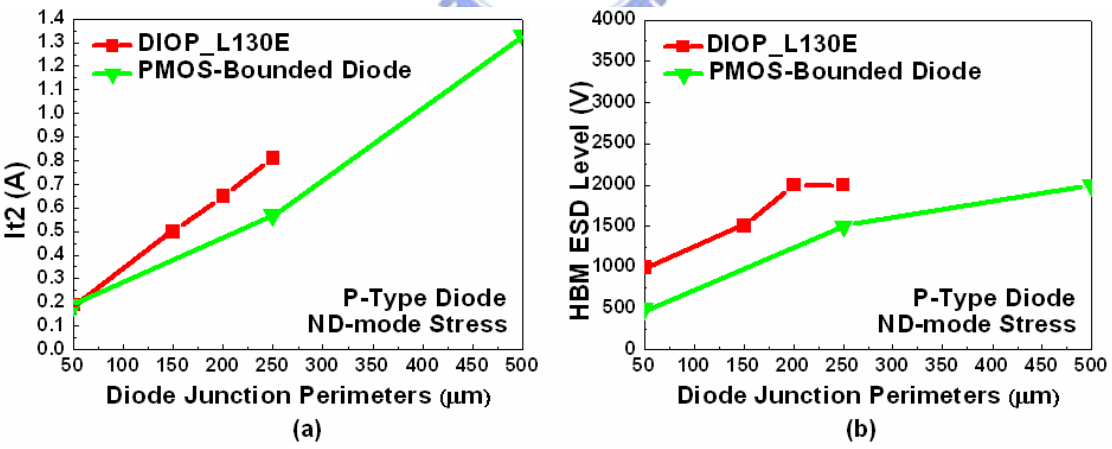


Fig. 3.19 The (a) It2 level, and (b) HBM ESD level, of P-type diode with different total junction perimeters under reversed mode ESD stress conditions.

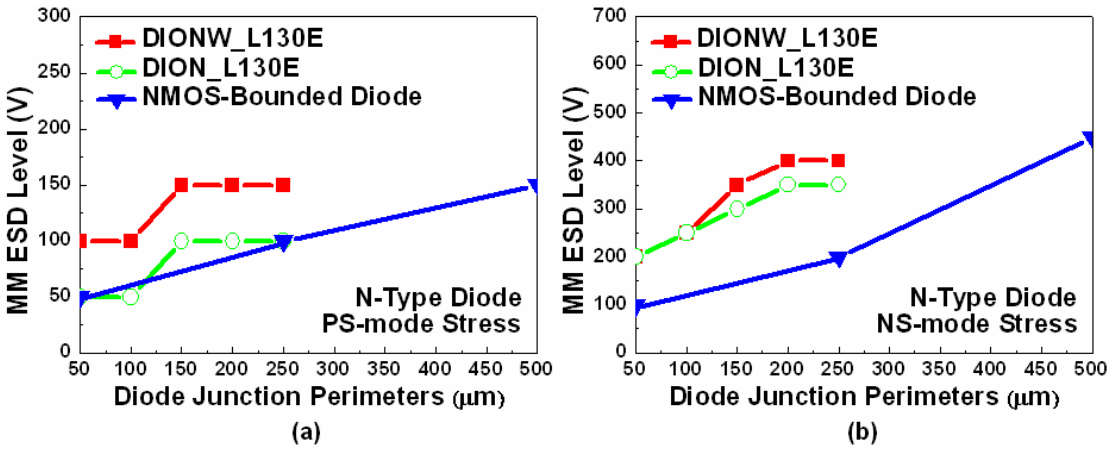


Fig. 3.20 The (a) reverse bias, and (b) forward bias, of N-type diodes with different total junction perimeters under MM ESD stress conditions.

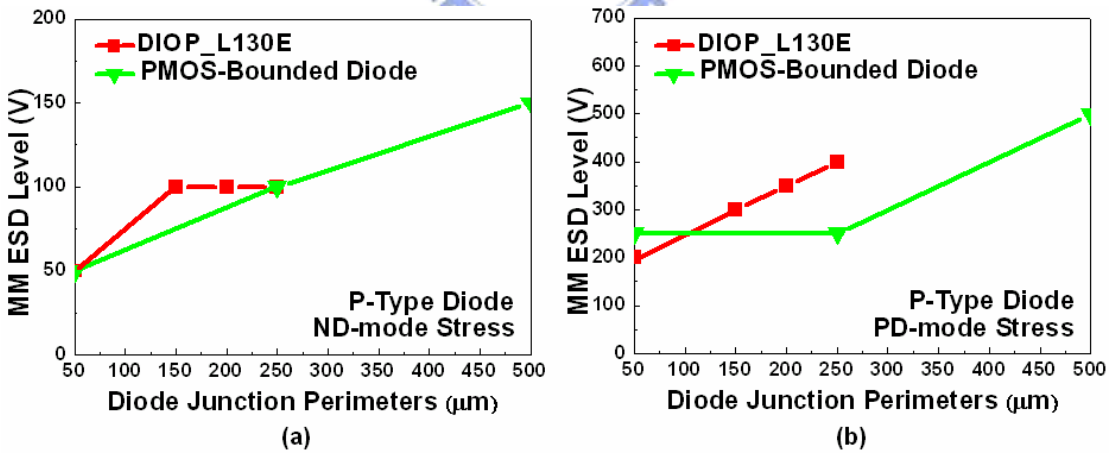


Fig. 3.21 The (a) reverse bias, and (b) forward bias, of P-type diodes with different total junction perimeters under MM ESD stress conditions.

Fig. 3.22 The high frequency S-parameter measurement system.

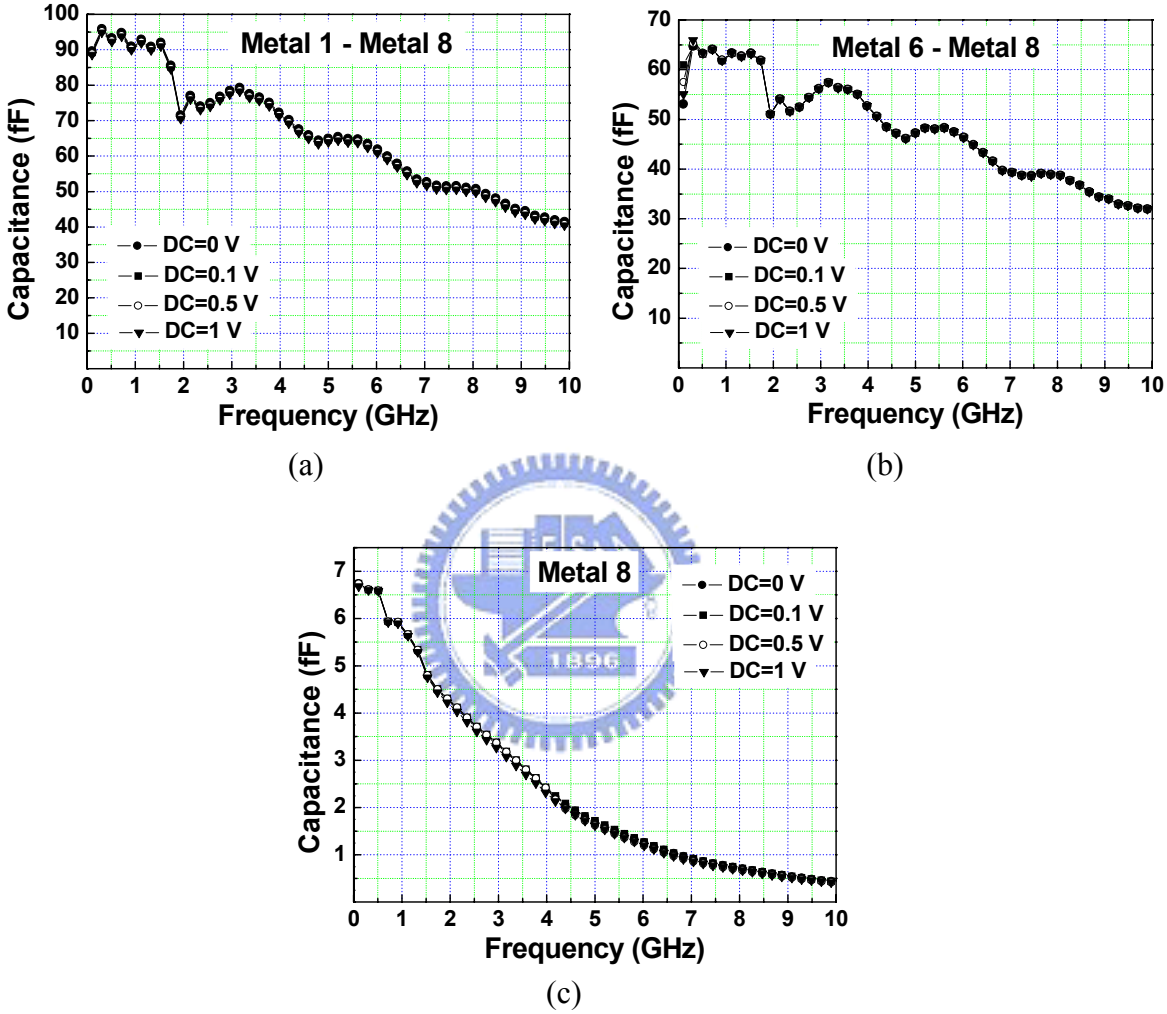


Fig. 3.23 The measured parasitic capacitance of stand-alone pads (70 μm× 60 μm under different DC biases for different pad structures (a) metal 1 to metal 8, (b) metal 6 to metal 8, and (c) metal 8 only.

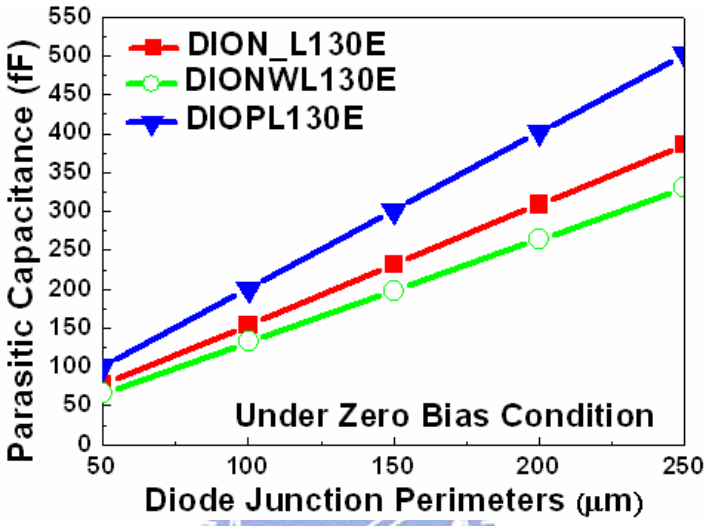


Fig. 3.24 The parasitic capacitance of diodes under different junction perimeters in zero bias conditions.

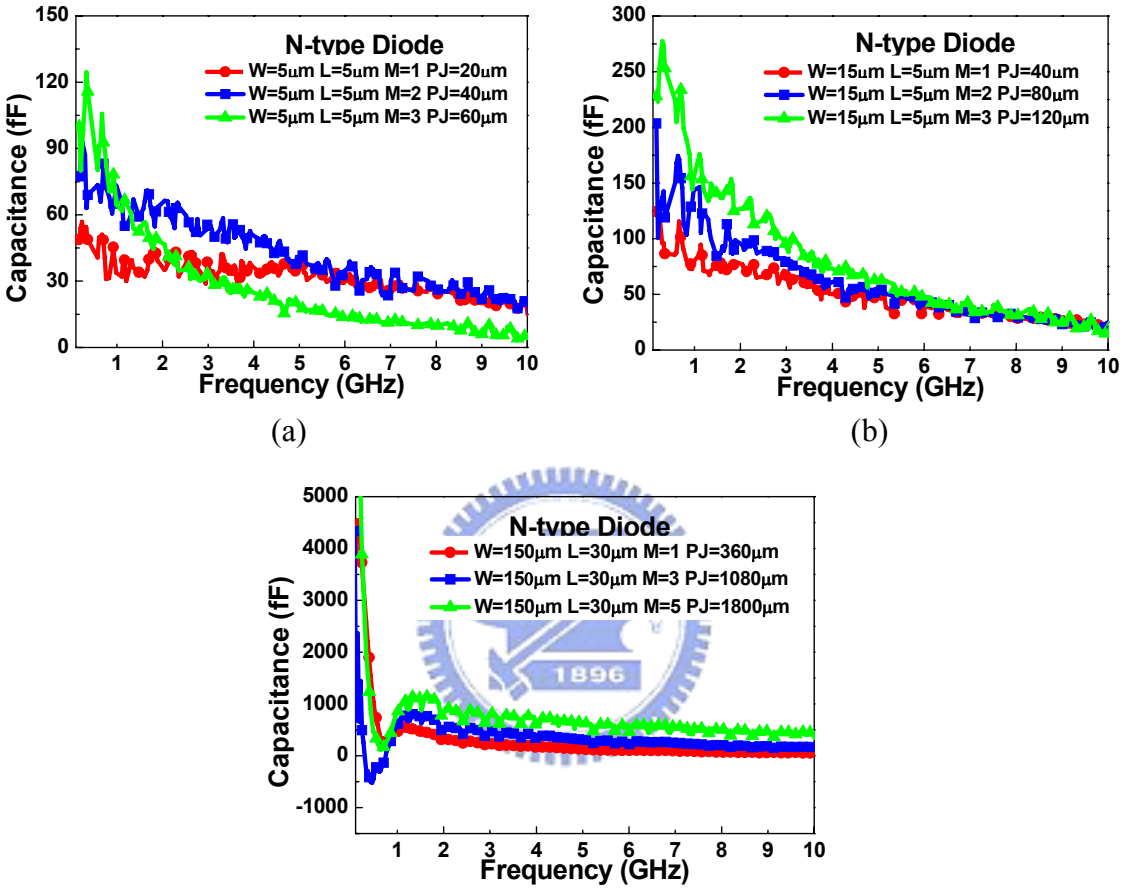


Fig. 3.25 The N-type diodes parasitic capacitance under different perimeters in (a) W=5μm, L=5μm, (b) W=15μm, L=5μm, (c) W=150μm, L=30μm.

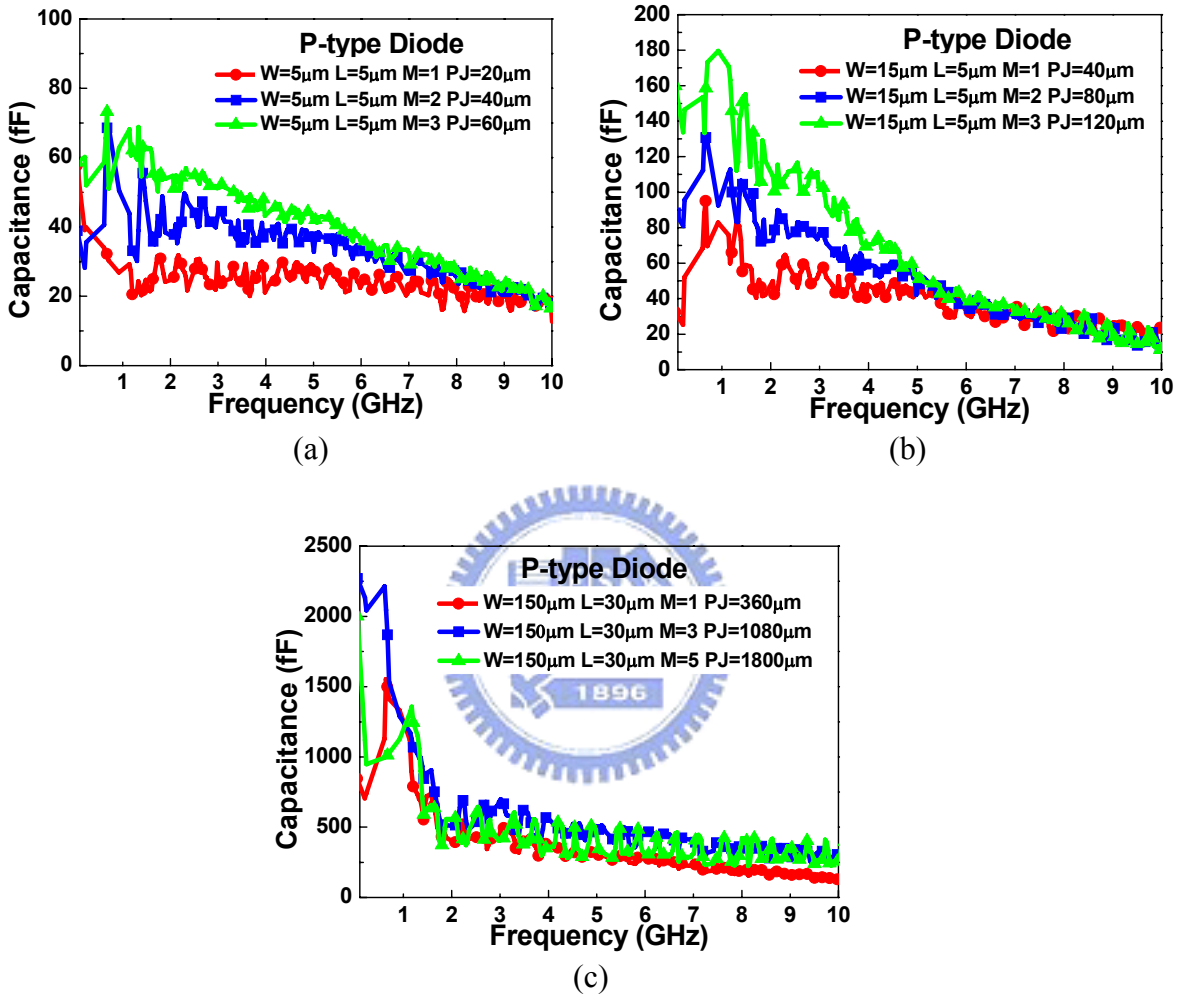


Fig. 3.26 The P-type diodes parasitic capacitance under different perimeters in (a) W=5μm, L=5μm, (b) W=15μm, L=5μm, (c) W=150μm, L=30μm.

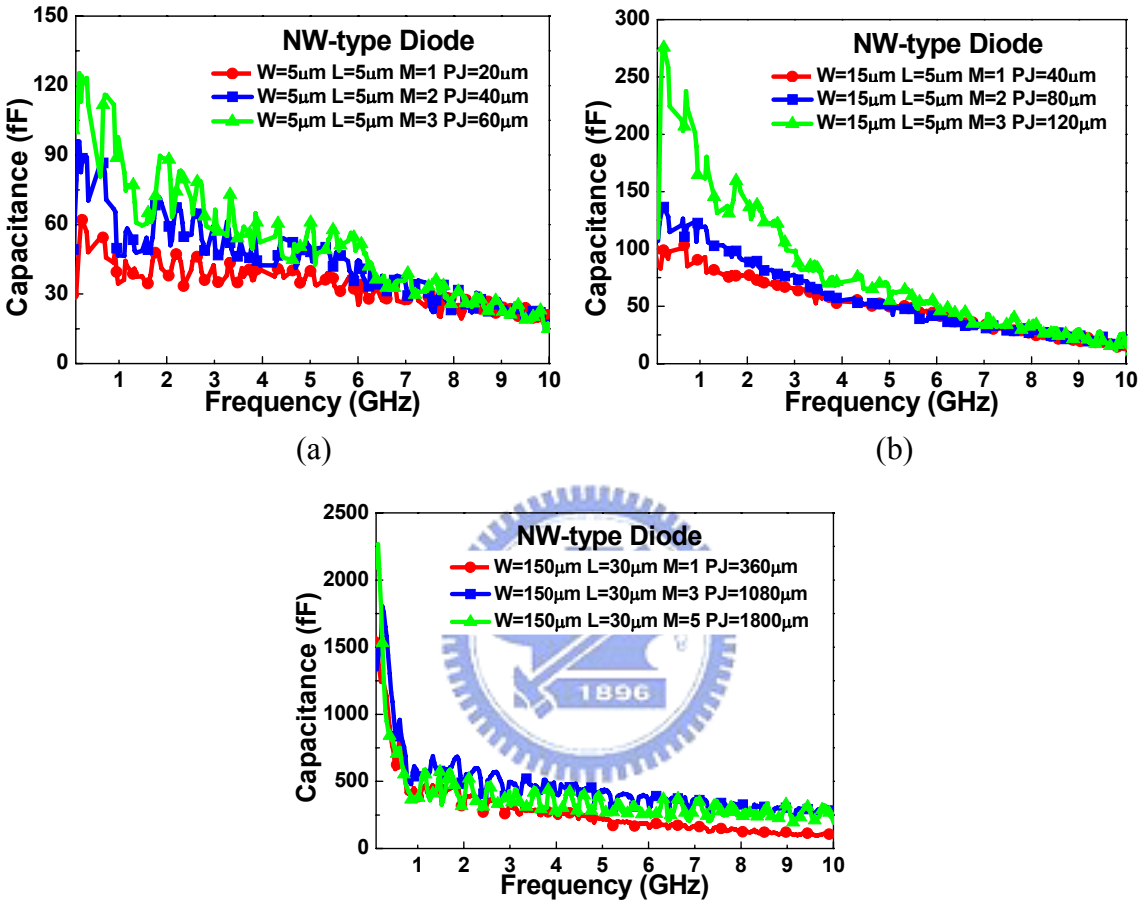
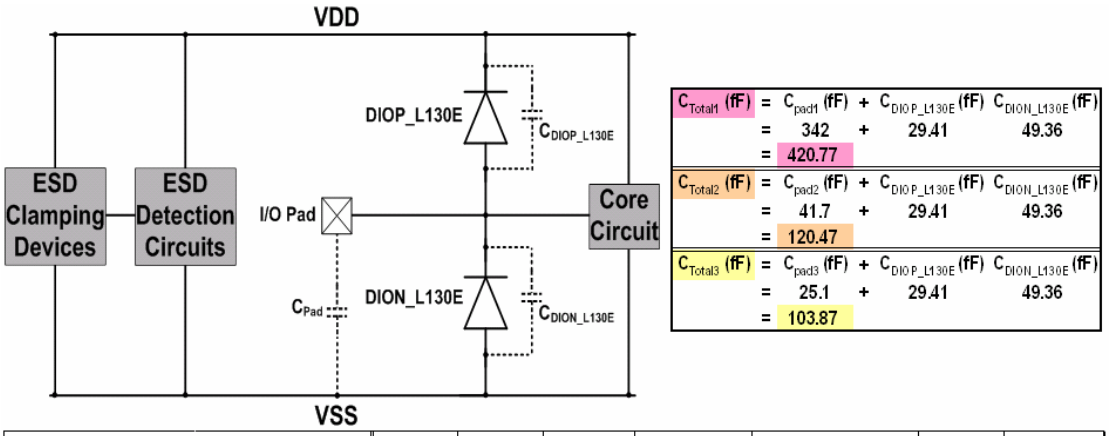


Fig. 3.27 The NW-type diodes parasitic capacitance under different perimeters in (a) W=5μm, L=5μm, (b) W=15μm, L=5μm, (c) W=150μm, L=30μm.



Types		W (μm)	L (μm)	PJ (μm)	AREA (μm²)	Parasitic Capacitance (fF)	It2 (A)	V_{HBM} (KV)
C_{pad}	M1 - M8 (C_{Pad1})	70.00	60.00	260.00	4200.00	342		
	M6 - M8 (C_{Pad2})	70.00	60.00	260.00	4200.00	41.7		
	M8 (C_{Pad3})	70.00	60.00	260.00	4200.00	25.1		
DIOP_L130E (C_{DIOP_L130E})		5.70	5.00	21.40	28.50	29.41	1.40	2.10
DION_L130E (C_{DION_L130E})		12.70	5.00	35.40	63.50	49.36	1.40	2.10
DIONW_L130E (C_{DIONW_L130E})		13.60	5.00	37.20	68.00	48.18	1.40	2.10

Fig. 3.28 The design example for high-speed interface circuits with ESD protection.

CHAPTER 4

5-GHz TRANSMITTER (TX) AND RECEIVER (RX) INTERFACE CIRCUITS WITH ESD PROTECTION

This chapter presents the commercial high-speed interface circuit operating at 5-GHz with ESD protection circuit. Two types of ESD protection schemes under different dimensions were investigated, and the double diodes with the turn-on efficient power-rails ESD clamp circuit are used in the transmitter (TX) and receiver (RX) interface circuits. Besides, additional diode test device under different dimensions and ESD protection schemes are designed and evaluated. Further more, the simulated results of RX interface circuit with ESD protection under different schemes also be evaluated. At a required ESD level, the method to reduce the parasitic capacitance of the ESD protection devices and to achieve good high-speed circuit performance will be reported.

4.1 TX/RX TEST CIRCUITS WITH ESD PROTECTION

In order to sustain the required ESD level and to reduce the drain junction width of the output MOSFET in the TX interface circuit, the TX interface circuit with the power-rail ESD clamp circuits realized by the MOSFET M_{NESD} (W_{TOTAL}=400μm) have three different DX (the drain side contact to poly edge spacing) are used to have reduced parasitic capacitance and better high-speed circuit performance. Besides, to reduce the drain junction width of the output MOSFET in the TX interface circuit, the TX interface circuit with the power-rail ESD clamp circuits realized by the embedded

P-type trigger silicon-controlled rectifier (EPTSCR) (W=59.6μm) have four different DX (the drain side contact to poly edge spacing) are used to have reduced parasitic capacitance and better high-speed circuit performance. The two aforementioned ESD protection schemes are shown in Fig. 4.1 and Table 4.1 – Table 4.2. The RX interface circuit with the power-rail ESD clamp circuits formed by the MOSFET M_{NESD} (W_{TOTAL}=400μm) and the embedded P-type trigger silicon-controlled rectifier (EPTSCR) (W=59.6μm) uses the devices with two operating voltages, which are shown in Fig. 4.2 and Table 4.3 – Table 4.4. In the TX test circuit, the bond pad is connected to the drain terminal of the output MOSFET, which means the drain junction of the output MOSFET will be stressed under ESD conditions. In the RX test circuit, the bond pad is connected to the gate terminal of the input MOSFET, which means the gate oxide of the input MOSFET will be stressed under ESD conditions. Besides, the EMMI (photon emission microscope) photograph to locate the failure location in ESD diode D_P is shown in Fig. 4.3. This means under the non-socket negative CDM ESD test, the negative charge is first stored in the substrate and then discharged to the I/O pad, the ESD protection capability of the ESD diode D_P is smaller then that of the power-rail ESD clamp device, so the ESD diode D_p is damaged under the non-socket negative CDM ESD test. The EMMI photograph shows the failure location is in the ESD diode D_P. Therefore, the ESD diode D_P may need to be modified for higher ESD robustness.

4.2 SIMULATED RESULTS OF INTERFACE CIRCUITS WITH ESD PROTECTION

The RX interface circuit with ESD double diodes and power-rail ESD clamp

circuit is shown in Fig. 4.4. The core circuit was blocked. The ESD double diodes were placed between core circuit and bond pad to co-operate with power-rail ESD clamp circuit. With the power-rail ESD clamp circuit, the ESD diodes will operated in the forward-biased conduction, rather than the junction breakdown condition, and provide the ESD discharge current path more efficiently to get higher ESD robustness when under ESD stresses. During the design of the 5-GHz RX interface circuit with ESD protection, the parasitic effect of the bond pad and ESD clamp devices should be taken into considered. The parasitic effect of the bond pad and ESD clamp devices can be referred in "ESD Protection Design Example for 5-GHz High-Speed I/O Applications" in Chapter 3. The input stage of the RX interface circuit is a differential pair and the test patterns for 5-GHz specification are shown in Fig. 4.5. A capacitor from the input node to bond pad with the capacitance between 75 nF to 200 nF is used for DC blocking purpose. A 25-fF capacitor is used as the output loading. To verify the performance of the core circuit with ESD protection circuit, the simulated output waveform of RX interface in typical corner are all over 120mV$_{p\text{-}p}$ with input test patterns 1 and 2. The test pattern1 has alternative series 1 and 0 differential signals, and the test pattern 2 has alternative five continuous 1 and 0 differential signals. The two test patterns as shown in Fig. 4.6. The simulated results in five different process corners are listed in Table 4.5. The minimum peak-to-peak output voltage is 126mV in TT corner when input test pattern 1, and the minimum peak-to-peak output voltage is 126mV in TT corner when input test pattern 2. The minimum peak-to-peak output voltage is 63mV in SS corner when input test pattern 1, and the minimum peak-to-peak output voltage is 63mV in SS corner when input test pattern 2. The minimum peak-to-peak output voltage is 102mV in FF corner when input test pattern 1, and the minimum peak-to-peak output voltage is 102mV in FF corner when input

test pattern 2. The minimum peak-to-peak output voltage is 98mV in FS corner when input test pattern 1, and the minimum peak-to-peak output voltage is 98mV in FS corner when input test pattern 2. The minimum peak-to-peak output voltage is 127mV in SF corner when input test pattern 1, and the minimum peak-to-peak output voltage is 127mV in SF corner when input test pattern 2. Two ESD protection schemes were designed in the experimental test chip. Type I includes the ESD dual diodes under different perimeters and the power-rail ESD clamp circuits with EPTSCR. Type II includes ESD diodes under different perimeters at the top side, the bottom-side-embedded-P-type-trigger-silicon-control-rectifier (BSEPTSCR) under different perimeters at the bottom side, and the power-rail ESD clamp circuit with EPTSCR (W=59.6μm), as shown in Fig. 4.7 and Table 4.6. In order to mitigate high-speed circuit performance degradation caused by the parasitic capacitance of the bond pad, some of the ESD devices were placed under the bond pad to reduce the total parasitic capacitance. Moreover, the chip area can be saved by placing some ESD device under the bond pad. The parasitic capacitance of the ESD device with bond pad under different conditions is shown in Table 4.7. By placing the ESD devices under bond pad structure can achieve more then 4fF and 3 percent decrease in parasitic capacitance. The simulated results shows that the ESD devices under the bond pad can further reduce the total parasitic capacitance.

4.3 LAYOUT DESCRIPTION OF INTERFACE CIRCUITS WITH ESD PROTECTION

Base on two types of ESD protection schemes, some of the ESD devices are place under the bond pad. For example, the “EPTSCR” device and the MOSFETs

"M_P" and "M_N" can be placed under the bond pad. For type I ESD protection circuit, which includes double ESD diodes under different perimeters and power-rail ESD clamp circuit structures, the ESD diodes "D_P" and "D_n" were placed under the two sides of the bond pad. The power-rail ESD clamp device EPTSCR was placed under the center of the bond pad. Besides, the power-rail ESD clamp device M_P and M_N can be placed between EPTSCR and ESD diodes. The EPTSCR shares the same N-Well / P-Well with the M_P / M_N of power-rail ESD clamp device in order to save more chip area. The cross-sectional view of the ESD devices under the bond pad as shown in Fig. 4.8 and Fig. 4.9. For type II ESD protection circuit, which includes top side ESD diode device and bottom side BSEPTSCR device, the ESD diode and BSEPTSCR devices were placed under the bond pad, which means this method can further reduce the total parasitic capacitance. Besides, the layout is the same as type I, except replacing D_n by EPTSCR. The layout top view of the ESD devices under pad is shown in Fig.4.10. The total layout area is 1300 μm × 1371.4 μm. The layout top view of the ESD devices with two types of ESD protection schemes is shown in Fig. 4.11.

4.4 ESD ROBUSTNESS OF INTERFACE CIRCUITS WITH ESD PROTECTION

The ESD robustness of M_{NESD} ESD protection scheme under different dimensions of TX_NMOS was not shown due to layout error. The ESD robustness of EPTSCR ESD protection scheme under different dimensions of TX_NMOS is shown in Table 4.8. Under PS mode ESD test, the It2 level of TX_NMOS with DX=2.15μm and 55μm of D_P and D_n junction perimeters is 3.2A, and the HBM and MM ESD level of this structure is 7.5kV and 450V, respectively. Under NS mode ESD test, the It2 level of TX_NMOS with DX=2.15μm and 55μm of D_P and D_n junction perimeters

is 1.7A, and the HBM and MM ESD level of this structure is above 8kV and 650V, respectively. Under PD mode ESD test, the It2 level of TX_NMOS with DX=2.15μm and 55μm of D_P and D_n junction perimeters is 1.7A, and the HBM and MM ESD level of this structure is 4.5kV and 450V, respectively. Under ND mode ESD test, the It2 level of TX_NMOS with DX=2.15μm and 55μm of D_P and D_n junction perimeters is 4.57A, and the HBM and MM ESD level of this structure is 7.5kV and 350V, respectively. Under non-socket CDM positive ESD test, the ESD level of TX_NMOS with DX=2.15μm and 55μm of D_P and D_n junction perimeters is above 2kV. Under non-socket CDM negative ESD test, the ESD level of TX_NMOS with DX=2.15μm and 55μm of D_P and D_n junction perimeters is 350V. The experimental results showed much stronger ESD robustness with DX=2.15μm and large perimeters of ESD devices. Besides, the experimental results show that increasing ESD device perimeters can have higher ESD robustness. The It2 level is 1.07A and HBM ESD level is 2.5kV and MM ESD level is 200V under PS mode ESD test, when the M_{NESD} is realized with 1.2V device and the Dp and Dn are realized with 139.8μm and 140.5μm, respectively. The It2 level is above 6A and HBM ESD level is 8kV and MM ESD level is 200V under NS mode ESD test, when the M_{NESD} is realized with 1.2V device and the Dp and Dn are realized with 139.8μm and 140.5μm, respectively. The It2 level is above 6A and HBM ESD level is 4.5kV and MM ESD level is 150V under PD mode ESD test, when the M_{NESD} is realized with 1.2V device and the Dp and Dn are realized with 139.8μm and 140.5μm, respectively. The It2 level is 4.2A and HBM ESD level is 4.5kV and MM ESD level is 350V under ND mode ESD test, when the M_{NESD} is realized with 1.2V device and the Dp and Dn are realized with 139.8μm and 140.5μm, respectively. The ESD level is 1kV under non-socket CDM positive ESD test, when the M_{NESD} is realized with 1.2V device and the Dp and Dn are realized with

139.8μm and 140.5μm, respectively. The ESD level is 400V under non-socket CDM negative ESD test, when the M_{NESD} is realized with 1.2V device and the Dp and Dn are realized with 139.8μm and 140.5μm, respectively. The It2 level is 2.87A and HBM ESD level is 5.5kV and MM ESD level is 350V under PS mode ESD test, when the M_{NESD} is realized with 3.3V device and the Dp and Dn are realized with 139.8μm and 140.5μm, respectively. The It2 level is above 6A and HBM ESD level is 8kV and MM ESD level is 550V under NS mode ESD test, when the M_{NESD} is realized with 3.3V device and the Dp and Dn are realized with 139.8μm and 140.5μm, respectively. The It2 level is above 6A and HBM ESD level is above 8kV and MM ESD level is 500V under PD mode ESD test, when the M_{NESD} is realized with 1.2V device and the Dp and Dn are realized with 139.8μm and 140.5μm, respectively. The It2 level is 4.3A and HBM ESD level is 4.5kV and MM ESD level is 350V under ND mode ESD test, when the M_{NESD} is realized with 1.2V device and the Dp and Dn are realized with 139.8μm and 140.5μm, respectively. The ESD level is above 2kV under non-socket CDM positive ESD test, when the M_{NESD} is realized with 3.3V device and the Dp and Dn are realized with 139.8μm and 140.5μm, respectively. The ESD level is 1300V under non-socket CDM negative ESD test, when the M_{NESD} is realized with 3.3V device and the Dp and Dn are realized with 139.8μm and 140.5μm, respectively. The ESD robustness of M_{NESD} ESD protection scheme under different dimensions of RX_NMOS is shown in Table 4.9. The experimental results show that the thick gate oxide RX_NMOS has higher ESD robustness then thin gate oxide RX_NMOS. The It2 level is 1.49A and HBM ESD level is 3kV and MM ESD level is 150V under PS mode ESD test, when the EPTSCR is realized with 1.2V device and the Dp and Dn are realized with 55μm and 55μm, respectively. The It2 level is 1.68A and HBM ESD level is 4kV and MM ESD level is 200V under NS mode ESD test, when the EPTSCR

is realized with 1.2V device and the Dp and Dn are realized with 55μm and 55μm, respectively. The It2 level is 1.71A and HBM ESD level is 4kV and MM ESD level is 150V under PD mode ESD test, when the EPTSCR is realized with 1.2V device and the Dp and Dn are realized with 55μm and 55μm, respectively. The It2 level is 2.68A and HBM ESD level is 4kV and MM ESD level is 250V under ND mode ESD test, when the EPTSCR is realized with 1.2V device and the Dp and Dn are realized with 55μm and 55μm, respectively. The ESD level is 300V under non-socket CDM positive ESD test, when the EPTSCR is realized with 1.2V device and the Dp and Dn are realized with 55μm and 55μm, respectively. The ESD level is 300V under non-socket CDM negative ESD test, when the EPTSCR is realized with 1.2V device and the Dp and Dn are realized with 55μm and 55μm, respectively. The It2 level is 3.79A and HBM ESD level is 8kV and MM ESD level is 350V under PS mode ESD test, when the EPTSCR is realized with 3.3V device and the Dp and Dn are realized with 55μm and 55μm, respectively. The It2 level is 1.77A and HBM ESD level is 4kV and MM ESD level is 350V under NS mode ESD test, when the EPTSCR is realized with 3.3V device and the Dp and Dn are realized with 55μm and 55μm, respectively. The It2 level is 2.41A and HBM ESD level is 4.5kV and MM ESD level is 300V under PD mode ESD test, when the EPTSCR is realized with 3.3V device and the Dp and Dn are realized with 55μm and 55μm, respectively. The It2 level is 3.52A and HBM ESD level is 4kV and MM ESD level is 350V under ND mode ESD test, when the EPTSCR is realized with 3.3V device and the Dp and Dn are realized with 55μm and 55μm, respectively. The ESD level is above 2kV under non-socket CDM positive ESD test, when the EPTSCR is realized with 3.3V device and the Dp and Dn are realized with 55μm and 55μm, respectively. The ESD level is 300V under non-socket CDM negative ESD test, when the EPTSCR is realized with 3.3V device and the Dp

and Dn are realized with 55μm and 55μm, respectively. The ESD robustness of EPTSCR ESD protection scheme under different dimensions of RX_NMOS is shown in Table 4.10. These experimental results show that the thick gate oxide RX_NMOS has higher ESD robustness then thin gate oxide RX_NMOS.

4.5 DISCUSSION AND SUMMARY

The TX_NMOS/RX_NMOS interface circuits with ESD protection circuits have been designed and investigated. The experimental results of TX_NMOS interface circuits with ESD protection circuits in the 0.13-μm CMOS process show much stronger ESD robustness with DX=2.15μm of TX_NMOS with large perimeters of ESD devices. Increasing ESD device perimeters can have higher ESD robustness. Besides, the experimental results of RX_NMOS interface circuits with ESD protection circuits in the 0.13-μm CMOS process also showed that the thick gate oxide RX_NMOS has higher ESD robustness then thin gate oxide RX_NMOS. The post-layout simulated result shows that the parasitic capacitance of the ESD devices can be further reduced by placing the ESD devices under the bond pad. Two types of RX interface circuit with ESD protection circuit have been designed and verified. Besides, the ESD levels of TX_NMOS and RX_NMOS with ESD protection also have been evaluated in the 0.13-μm CMOS process.

Table 4.1 The combinations of M_{NESD} ESD protection schemes under different dimensions of TX_NMOS drain side.

Item	D_P					D_n					TX_NMOS	M_{NESD}	
	W (μm)	L (μm)	M	PJ (μm)	DC Parasitic Cap. (fF)	W (μm)	L (μm)	M	PJ (μm)	DC Parasitic Cap. (fF)	DX (μm)	W_{TOTAL} (μm)	L (μm)
1	7.5	5	1	25	38.36	7.5	5	1	25	31.1	0.64	400	0.18
2	17.5			35	63.24	17.5			35	45.1	0.64		
3	22.5			45	88.11	22.5			45	59.1	0.64		
4	27.5			55	117.99	27.5			55	73.1	0.64		
5	64.9			129.8	323.9	65.24			130.48	192.8	0.64		
6	7.5	5	1	25	38.36	7.5	5	1	25	31.1	1.36	400	0.18
7	17.5			35	63.24	17.5			35	45.1	1.36		
8	22.5			45	88.11	22.5			45	59.1	1.36		
9	27.5			55	117.99	27.5			55	73.1	1.36		
10	64.9			129.8	323.9	65.24			130.48	192.8	1.36		
11	7.5	5	1	25	38.36	7.5	5	1	25	31.1	2.15	400	0.18
12	17.5			35	63.24	17.5			35	45.1	2.15		
13	22.5			45	88.11	22.5			45	59.1	2.15		
14	27.5			55	117.99	27.5			55	73.1	2.15		
15	64.9			129.8	323.9	65.24			130.48	192.8	2.15		

Table 4.2 The combinations of EPTSCR ESD protection schemes under different dimensions of TX_NMOS drain side.

Item	D_P					D_n					TX_NMOS	EPTSCR	
	W (μm)	L (μm)	M	PJ (μm)	DC Parasitic Cap. (fF)	W (μm)	L (μm)	M	PJ (μm)	DC Parasitic Cap. (fF)	DX (μm)	W (μm)	L (μm)
1	7.5	5	1	25	38.36	7.5	5	1	25	31.1	0.64	59.6	8.4
2	17.5			35	63.24	17.5			35	45.1			
3	22.5			45	88.11	22.5			45	59.1			
4	27.5			55	117.99	27.5			55	73.1			
5	64.9			129.8	323.9	65.24			130.48	192.8			
6	7.5	5	1	25	38.36	7.5	5	1	25	31.1	1.14	59.6	8.4
7	17.5			35	63.24	17.5			35	45.1			
8	22.5			45	88.11	22.5			45	59.1			
9	27.5			55	117.99	27.5			55	73.1			
10	64.9			129.8	323.9	65.24			130.48	192.8			
11	7.5	5	1	25	38.36	7.5	5	1	25	31.1	1.65	59.6	8.4
12	17.5			35	63.24	17.5			35	45.1			
13	22.5			45	88.11	22.5			45	59.1			
14	27.5			55	117.99	27.5			55	73.1			
15	64.9			129.8	323.9	65.24			130.48	192.8			
16	7.5	5	1	25	38.36	7.5	5	1	25	31.1	2.15	59.6	8.4
17	17.5			35	63.24	17.5			35	45.1			
18	22.5			45	88.11	22.5			45	59.1			
19	27.5			55	117.99	27.5			55	73.1			
20	64.9			129.8	323.9	65.24			130.48	192.8			

Table 4.3 The combinations of M_{NESD} ESD protection schemes under different dimensions of RX_NMOS gate side.

Item	D_P					D_n					TX_NMOS	M_{NESD}	
	W (μm)	L (μm)	M	PJ (μm)	DC Parasitic Cap. (fF)	W (μm)	L (μm)	M	PJ (μm)	DC Parasitic Cap. (fF)	DX (μm)	W_{TOTAL} (μm)	L (μm)
1	64.9	5	1	139.8	323.9	65.24	5	1	140.48	192.8	1.2V_W 5	400	0.18
2	64.9			129.8	323.9	65.24			130.48	192.8	3.3V_W 5		

Table 4.4 The combinations of EPTSCR ESD protection schemes under different dimensions of RX_NMOS gate side.

Item	D_P					D_n					TX_NMOS	EPTSCR	
	W (μm)	L (μm)	M	PJ (μm)	DC Parasitic Cap. (fF)	W (μm)	L (μm)	M	PJ (μm)	DC Parasitic Cap. (fF)	DX (μm)	W (μm)	L (μm)
1	7.5	5	1	25	38.36	7.5	5	1	25	31.1	1.2V_W 5	59.6	8.4
2	17.5			35	63.24	17.5			35	45.1			
3	22.5			45	88.11	22.5			45	59.1			
4	27.5			55	117.99	27.5			55	73.1			
5	64.9			129.8	323.9	65.24			130.48	192.8			
6	7.5	5	1	25	38.36	7.5	5	1	25	31.1	3.3V_W 5	59.6	8.4
7	17.5			35	63.24	17.5			35	45.1			
8	22.5			45	88.11	22.5			45	59.1			
9	27.5			55	117.99	27.5			55	73.1			
10	64.9			129.8	323.9	65.24			130.48	192.8			

Table 4.5 The simulation results under difference corners.

Vo-pp-min (mV)		
Corner	Pattern1	Pattern2
TT	126	126
SS	63	63
FF	102	102
FS	98	98
SF	127	127

Table 4.6 The combinations of two types of ESD protection schemes.

Item	ESD Device													
	Top Site Device						Bottom Site Device						EPTSCR	
	Type	W (μm)	L (μm)	M	PJ (μm)	DC Parasitic Cap. (fF)	Type	W (μm)	L (μm)	M	PJ (μm)	DC Parasitic Cap. (fF)	W (μm)	L (μm)
1	P-type Diode	7.5	5	1	25	38.36	NW-type Diode	7.5	5	1	25	31.1	59.6	8.4
2		17.5			35	63.24		17.5			35	45.1		
3		22.5			45	88.11		22.5			45	59.1		
4		27.5			55	117.99		27.5			55	73.1		
5		64.9			129.8	323.9		65.24			130.48	192.8		
6	P-type Diode	7.5	5	1	25	38.36	BSEPTSCR	20					59.6	8.4
7		17.5			35	63.24								
8		22.5			45	88.11								
9		27.5			55	117.99								
10		64.9			129.8	323.9								
11	P-type Diode	7.5	5	1	25	38.36	BSEPTSCR	30					59.6	8.4
12		17.5			35	63.24								
13		22.5			45	88.11								
14		27.5			55	117.99								
15		64.9			129.8	323.9								
16	P-type Diode	7.5	5	1	25	38.36	BSEPTSCR	50					59.6	8.4
17		17.5			35	63.24								
18		22.5			45	88.11								
19		27.5			55	117.99								
20		64.9			129.8	323.9								
21	Core Circuit Only													

Table 4.7 The parasitic capacitance under different simulated results.

PJ (μm)	C_n (fF)	C_p (fF)	C_{pad}(fF) (57μm×69μm)		Pre-sim			Post-sim	
					C_{total} (fF)			C_{total} (fF)	
			M8 - M3	M8 - M6	$C_n+C_p+C_{padM8-M3}$	$C_n+C_p+C_{padM8-M6}$		$C_n+C_p+C_{padM8-M3}$	$C_n+C_p+C_{padM8-M6}$
25	29.55	38.36	77.20	39.10	145.11	107.01	Not under pad	152.51	130.30
							Under pad	150.26	126.36
							Reduction	2.25	3.94
							Enhancement	1.48%	3.02%
35	48.60	63.27			189.07	150.97	Not under pad	172.50	171.80
							Under pad	170.34	171.76
							Reduction	2.16	0.04
							Enhancement	1.25%	0.02%
45	67.64	88.11			232.95	194.85	Not under pad	216.45	194.65
							Under pad	215.23	192.79
							Reduction	1.22	1.86
							Enhancement	0.56%	0.96%
55	86.68	112.98			276.86	238.76	Not under pad	260.43	217.12
							Under pad	259.02	212.35
							Reduction	1.41	4.77
							Enhancement	0.54%	2.20%

Table 4.8 The combinations of EPTSCR ESD protection schemes under different dimensions of TX_NMOS drain side.

Item	D_p PJ (μm)	D_n PJ (μm)	TX_NMOS DX (μm)	PS It2 (A)	PS HBM (kV)	PS MM (V)	NS It2 (A)	NS HBM (kV)	NS MM (V)	PD It2 (A)	PD HBM (kV)	PD MM (V)	ND It2 (A)	ND HBM (kV)	ND MM (V)	Non-Socket CDM (V) Positive	Non-Socket CDM (V) Negative
1	25	25	0.64	1.09	2	200	1.59	4	250	1.19	2	200	1.76	6	250	> 2kV	< 300
2	35	35	0.64	1.13	2.5	150	1.69	6	250	1.32	2.5	250	1.42	6	300	> 2kV	< 300
3	45	45	0.64	1.71	3	200	1.81	7	300	1.67	3.5	300	1.78	6	350	> 2kV	< 300
4	55	55	0.64	2.62	3	100	1.81	2.5	150	1.71	4	400	1.75	6	350	> 2kV	< 300
5	139.8	140.5	0.64	1.78	3	300	1.45	> 8	350	1.65	> 8	350	1.73	3.5	300	> 2kV	< 300
6	25	25	1.14	1.00	2.5	300	1.62	6.5	350	1.29	2	250	1.73	6.5	250	> 2kV	< 300
7	35	35	1.14	1.27	3	350	1.58	7	400	1.36	2.5	250	1.43	7	300	> 2kV	< 300
8	45	45	1.14	1.79	3	300	1.73	7.5	450	1.63	3.5	400	1.50	6.5	300	> 2kV	< 300
9	55	55	1.14	3.09	3.5	300	1.64	> 8	450	1.60	4.5	450	1.45	6.5	350	> 2kV	< 300
10	139.8	140.5	1.14	1.86	3	300	1.32	> 8	450	1.71	> 8	250	1.95	3.5	250	> 2kV	< 300
11	25	25	1.65	1.27	3	400	1.24	6.5	500	1.17	2	250	3.86	6.5	250	> 2kV	< 300
12	35	35	1.65	1.32	3.5	350	1.77	7	450	1.21	2.5	250	3.51	7.5	300	> 2kV	< 300
13	45	45	1.65	1.41	4.5	350	1.64	8	550	1.64	3.5	300	4.21	7.5	400	> 2kV	< 300
14	55	55	1.65	1.51	5	400	3.25	> 8	650	2.18	4.5	450	4.28	6.5	350	> 2kV	< 300
15	139.8	140.5	1.65	1.39	3.5	450	1.52	> 8	550	1.73	> 8	400	1.72	3	300	> 2kV	< 300
16	25	25	2.15	1.52	3.5	400	1.81	7	450	0.67	2	200	3.73	6.5	250	> 2kV	< 300
17	35	35	2.15	1.52	3.5	400	1.55	7	450	1.25	2.5	200	3.56	7	300	> 2kV	< 300
18	45	45	2.15	2.15	6.5	500	1.62	8	550	1.76	3.5	300	4.01	7	350	> 2kV	350
19	55	55	2.15	3.20	7.5	450	1.70	> 8	650	1.70	4.5	450	4.57	7.5	350	> 2kV	350
20	139.8	140.5	2.15	1.79	3.5	500	1.57	> 8	550	1.73	> 8	400	1.70	3.5	300	> 2kV	< 300

Table 4.9 The combinations of M_{NESD} ESD protection schemes under different dimensions of RX_NMOS gate side.

Item	D_p PJ (μm)	D_n PJ (μm)	RX_NMOS	PS It2 (A)	PS HBM (kV)	PS MM (V)	NS It2 (A)	NS HBM (kV)	NS MM (V)	PD It2 (A)	PD HBM (kV)	PD MM (V)	ND It2 (A)	ND HBM (kV)	ND MM (V)	Non-Socket CDM (V) Positive	Non-Socket CDM (V) Negative
1	139.8	140.5	1.2V Device	1.07	2.5	150	> 6	> 8	200	> 6	4.5	150	4.20	4.5	350	1kV	400
2	139.8	140.5	3.3V Device	2.87	5.5	350	> 6	> 8	550	> 6	> 8	500	4.30	4.5	350	> 2kV	1300

Table 4.10 The combinations of EPTSCR ESD protection schemes under different dimensions of RX_NMOS gate side.

Item	D_p PJ (μm)	D_n PJ (μm)	RX_NMOS	PS It2 (A)	PS HBM (kV)	PS MM (V)	NS It2 (A)	NS HBM (kV)	NS MM (V)	PD It2 (A)	PD HBM (kV)	PD MM (V)	ND It2 (A)	ND HBM (kV)	ND MM (V)	Non-Socket CDM (V) Positive	Non-Socket CDM (V) Negative
1	25	25	1.2V Device	0.73	1.5	100	0.29	2	100	1.77	2	100	1.26	2	100	400	< 300
2	35	35	1.2V Device	0.94	2	100	1.73	3	150	1.73	2.5	100	1.87	2.5	150	400	< 300
3	45	45	1.2V Device	1.31	2.5	100	1.53	3	200	1.66	3	100	2.71	3.5	200	350	< 300
4	55	55	1.2V Device	1.49	3	150	1.68	4	200	1.71	4	150	2.68	4	250	300	< 300
5	139.8	140.5	1.2V Device	1.67	3	100	1.15	2.5	150	1.24	3.5	200	1.72	3.5	250	1100	< 300
6	25	25	3.3V Device	2.65	2	150	1.64	2	150	1.57	2	150	1.02	2	200	400	< 300
7	35	35	3.3V Device	3.34	2.5	200	1.77	2.5	200	1.73	2.5	150	2.18	2.5	200	500	< 300
8	45	45	3.3V Device	3.77	3.5	250	1.50	3.5	250	1.67	3.5	250	2.98	3.5	250	1050	< 300
9	55	55	3.3V Device	3.79	8	350	1.77	4	350	2.41	4.5	300	3.52	4	350	1200	350
10	139.8	140.5	3.3V Device	1.78	3	250	> 6	> 8	350	> 6	> 8	300	1.73	3.5	250	> 2kV	< 300

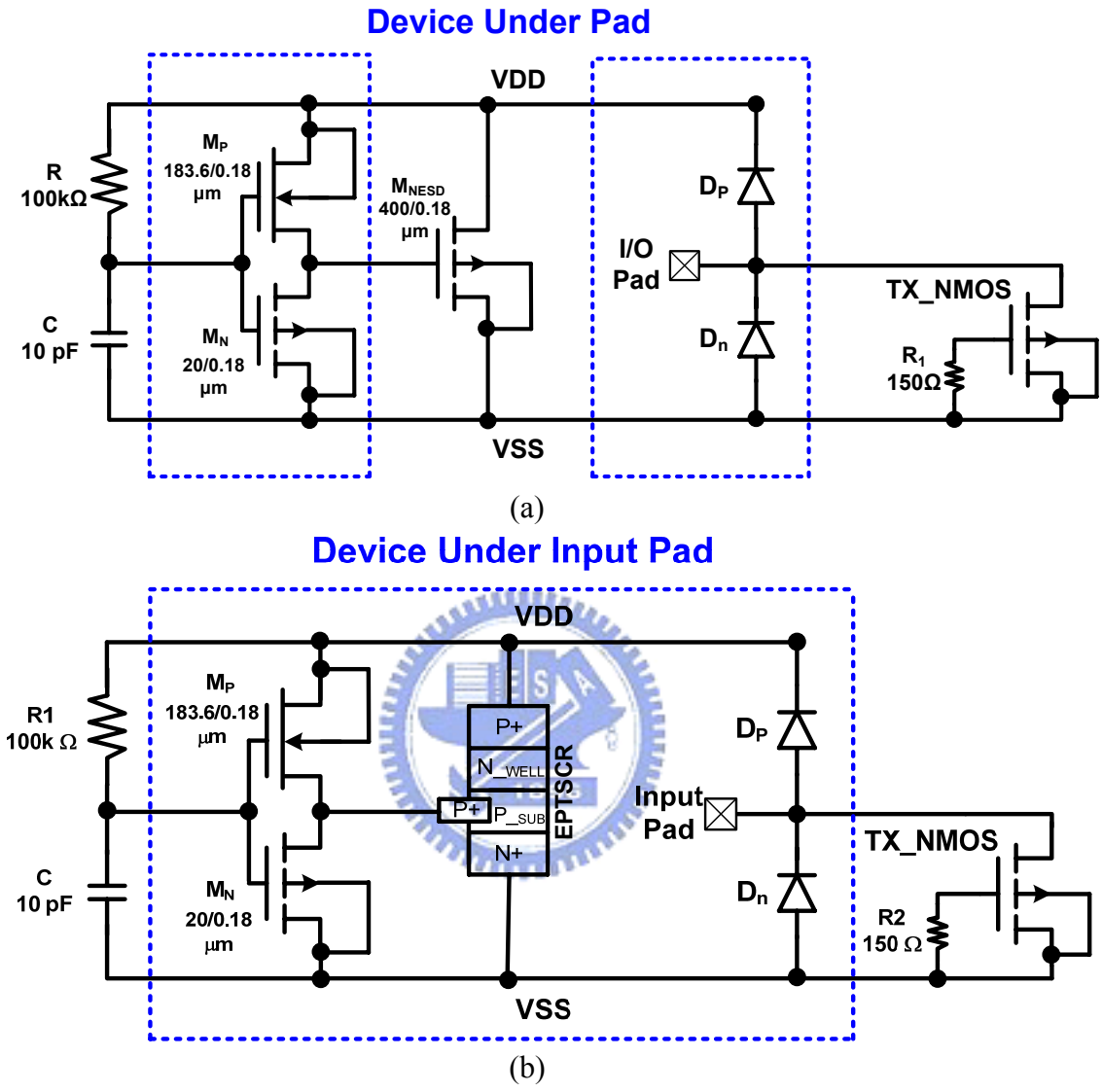


Fig. 4.1 To simulate TX interface circuit with TX_NMOS of ESD protection schemes of (a) M_{NESD} device, (b) EPTSCR device.

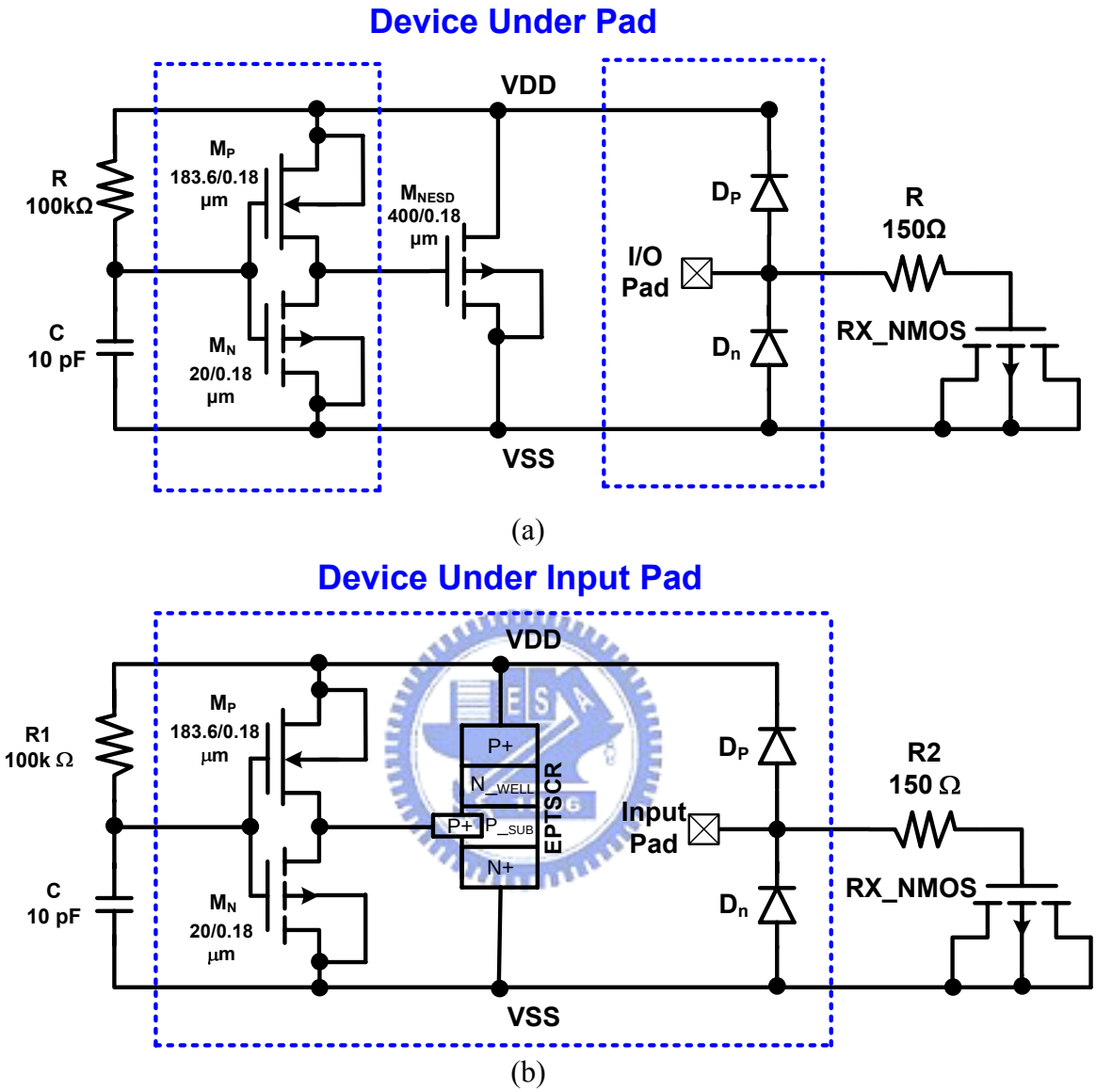


Fig. 4.2 To simulate RX interface circuit with RX_NMOS of ESD protection schemes of (a) M_{NESD} device, (b) EPTSCR device.

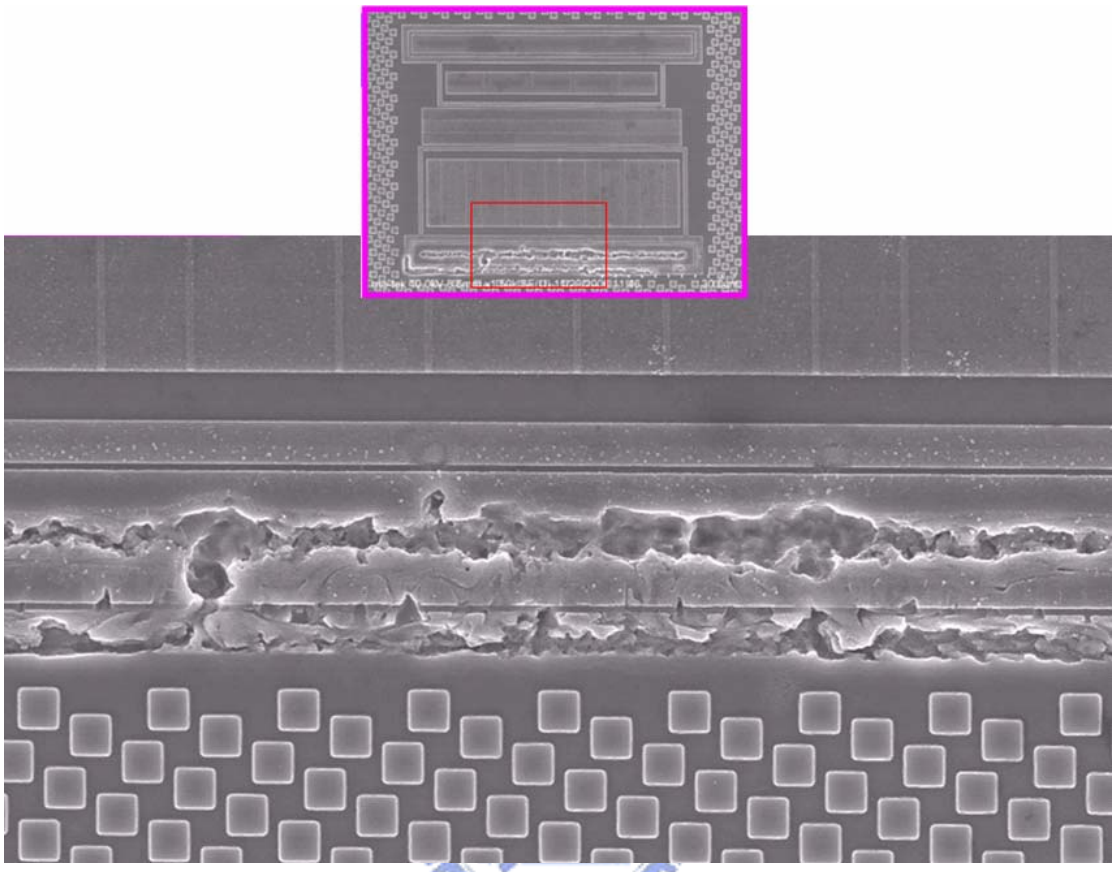


Fig. 4.3 The EMMI (photon emission microscope) photograph to locate the failure location in ESD diode D_P.

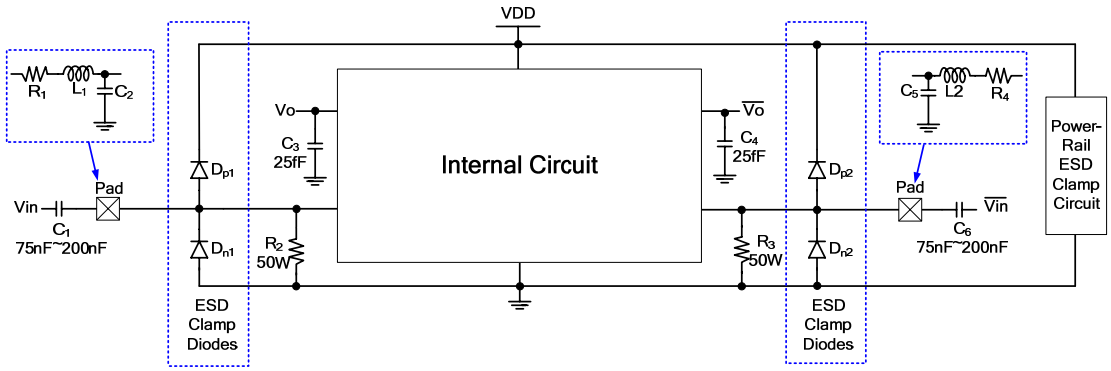


Fig. 4.4 The RX interface circuit with ESD protection scheme.

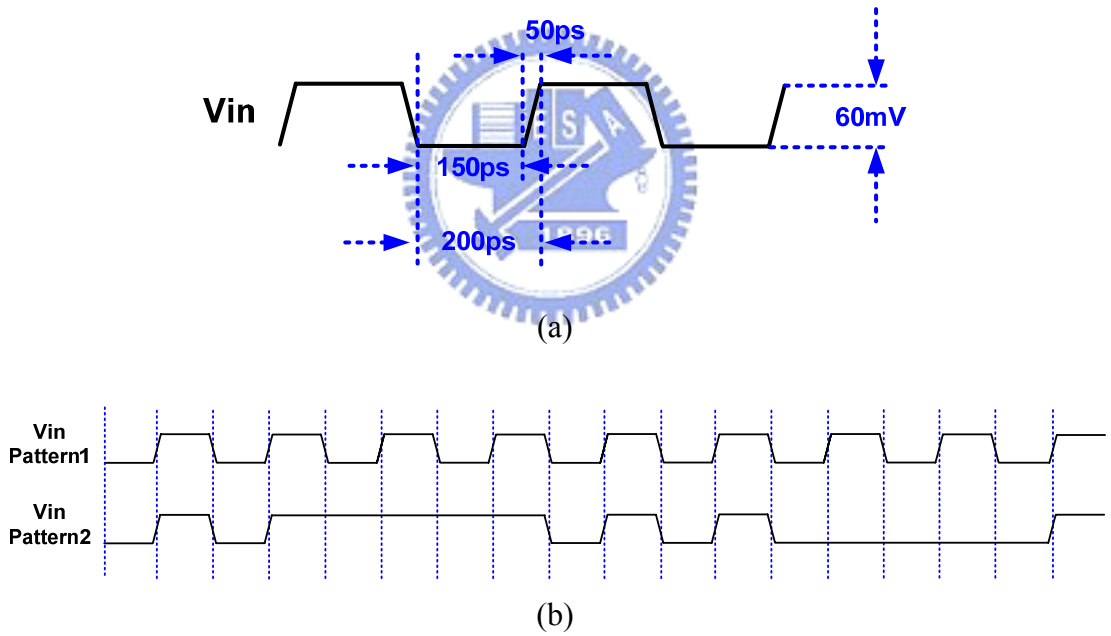


Fig. 4.5 (a) The test signal specifications and (b) test patterns for RX interface circuit.

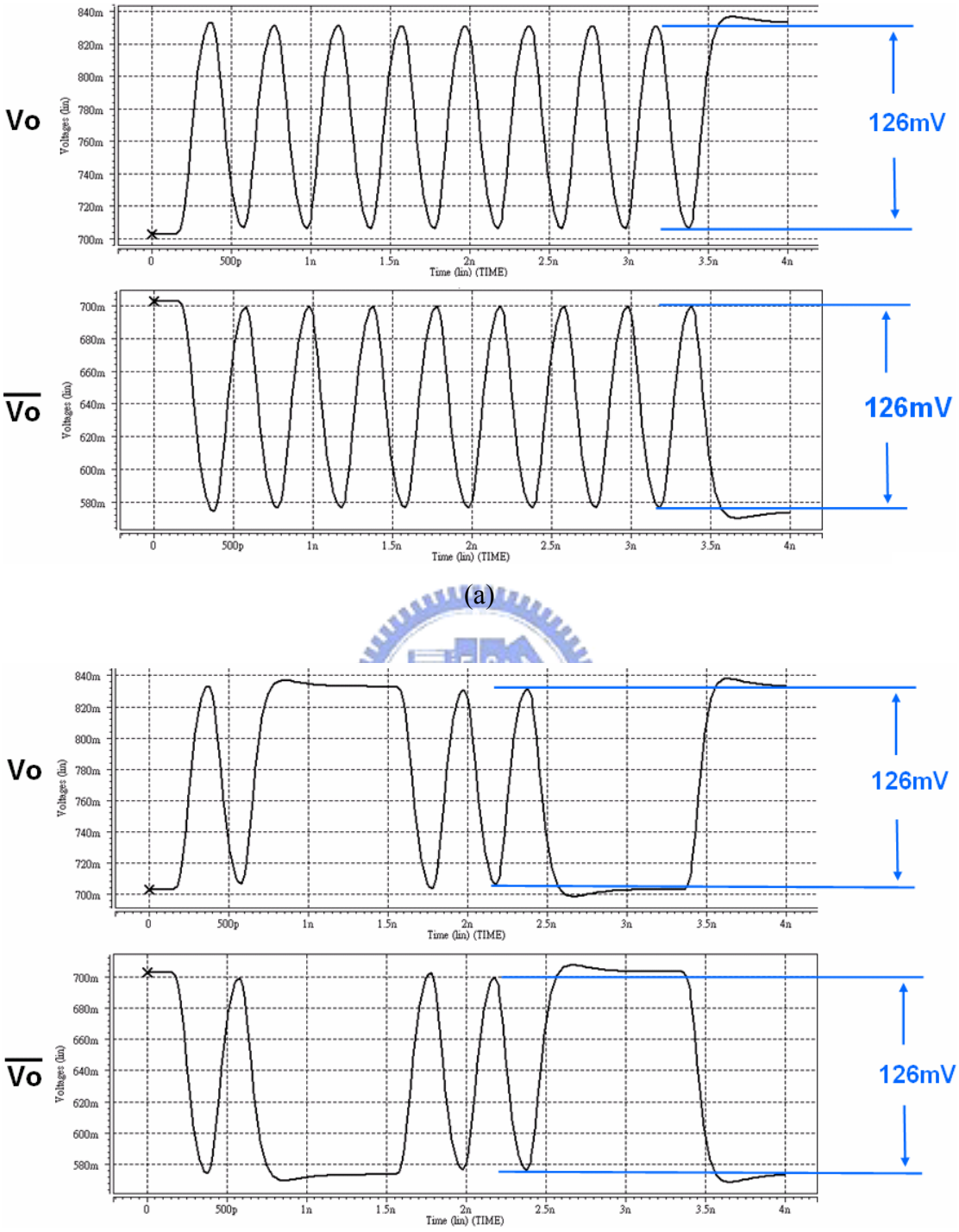
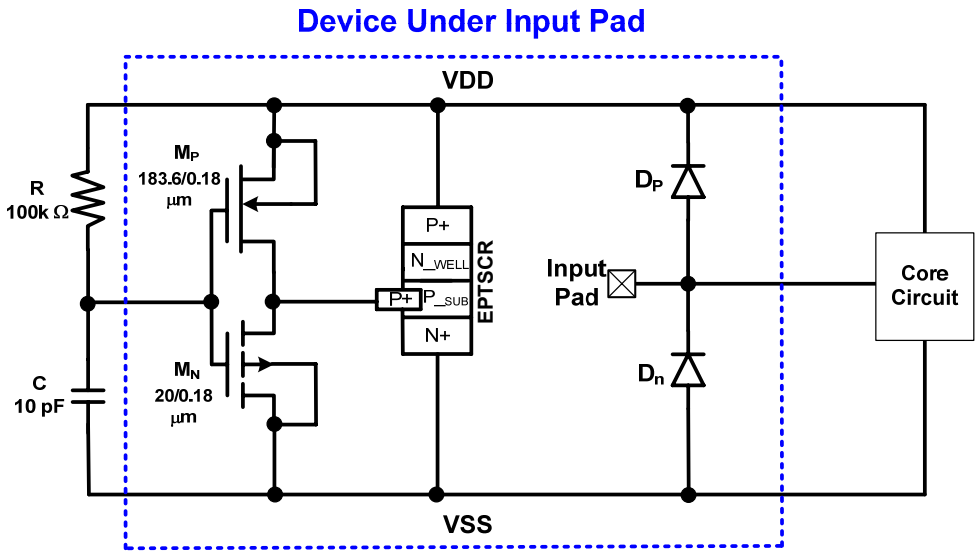
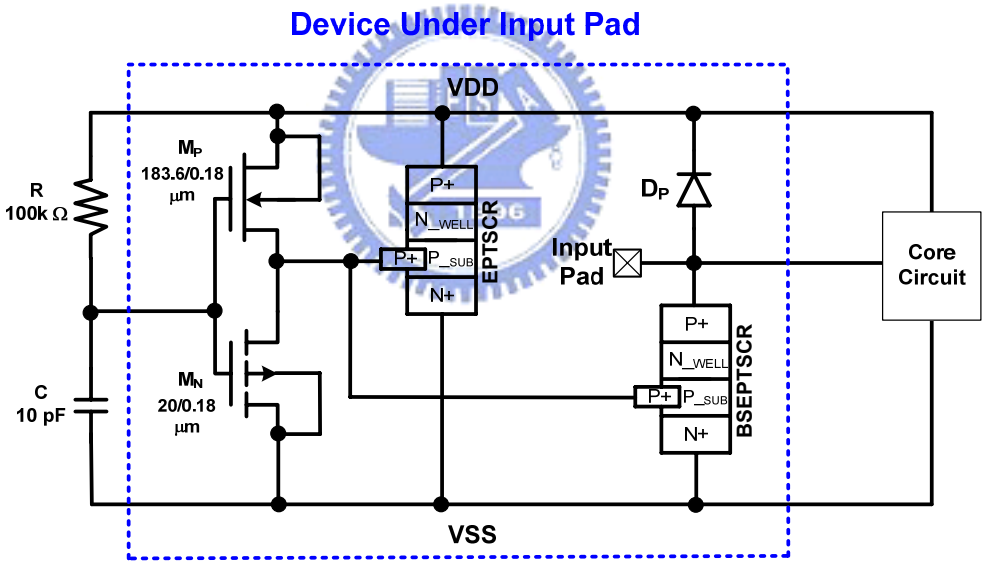


Fig. 4.6 The output waveform of RX interface circuits in typical corner when input (a) test pattern 1 and (b) test pattern 2.



(a)



(b)

Fig. 4.7 Two types of ESD protection schemes of (a) type I and (b) type II.

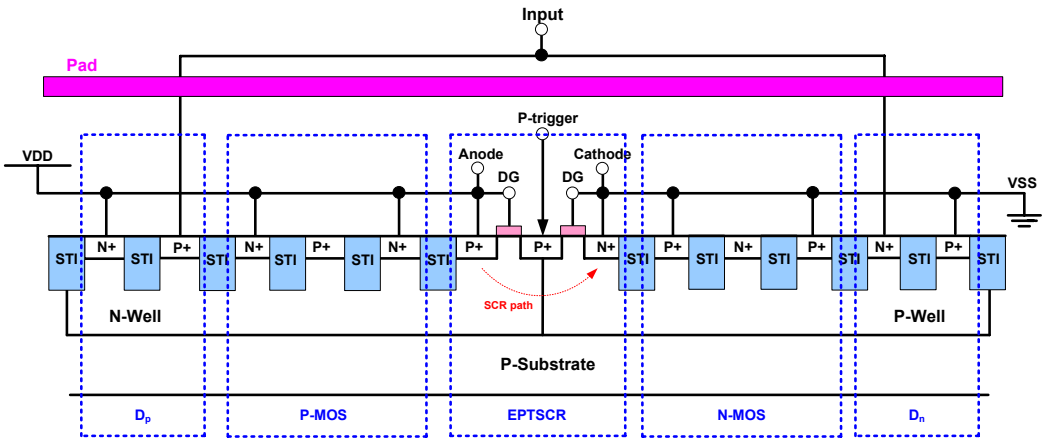


Fig. 4.8 Cross-sectional view of ESD devices under input pad.

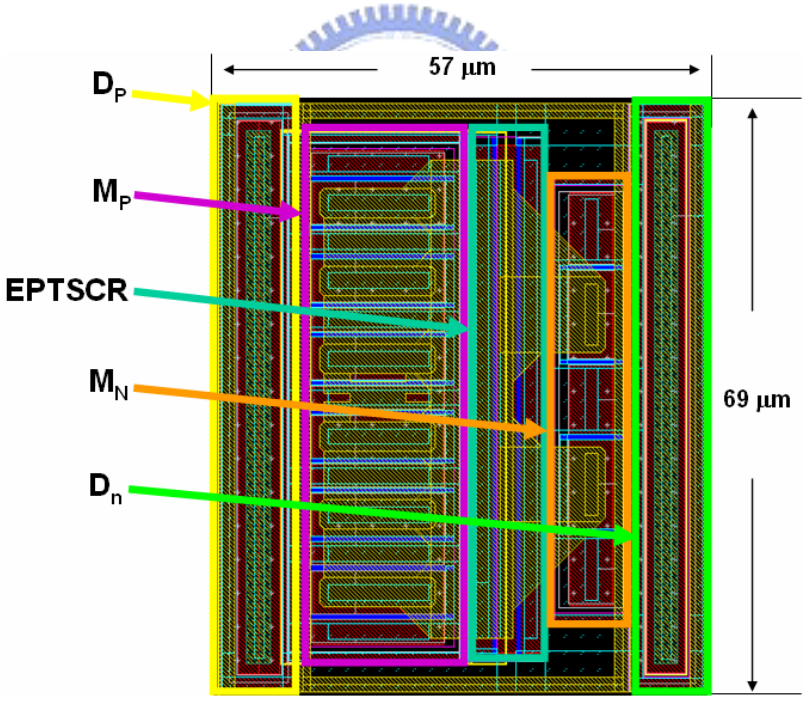


Fig. 4.9 Layout top view of ESD devices under pad (type I).

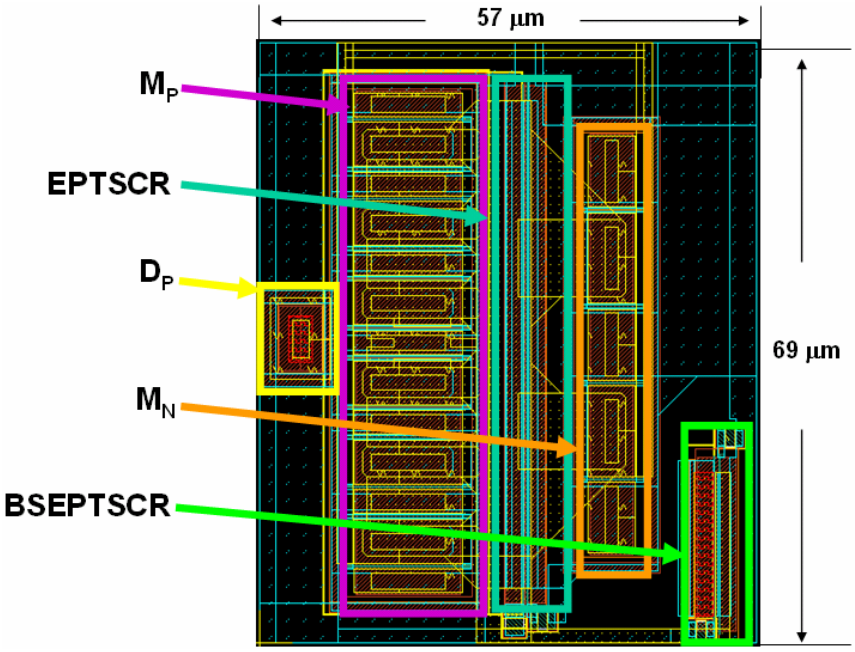


Fig. 4.10 Layout top view of ESD devices under pad (type II).

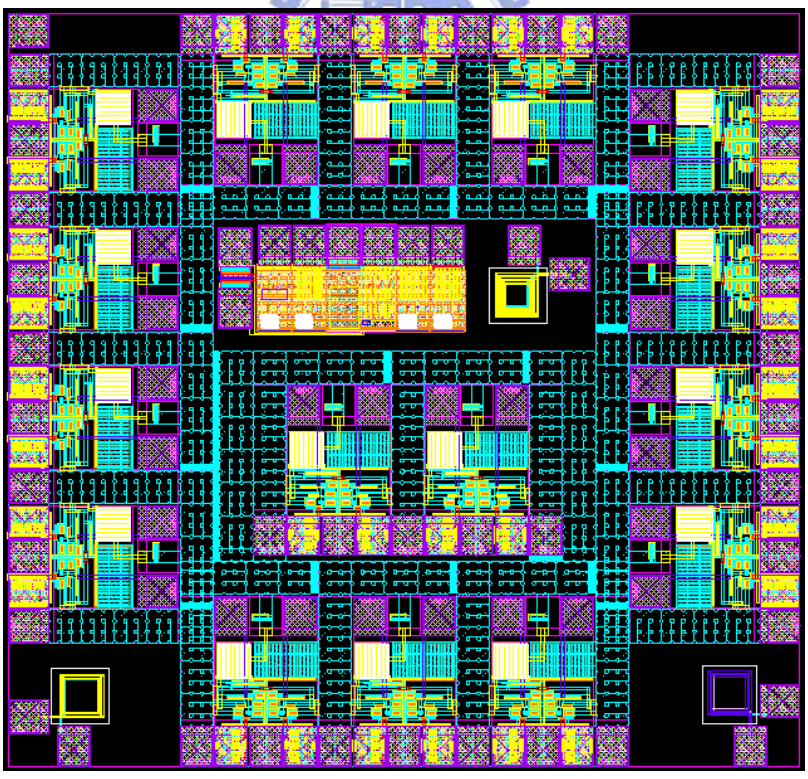


Fig. 4.11 Layout top view (1300 μm × 1371.4 μm) of the two types of ESD protection scheme blocks in a test chip.

CHAPTER 5
CONCLUSIONS AND FUTURE WORKS

5.1 Main Results of This Thesis

The high-frequency characteristics of the ESD diodes have been investigated by on-wafer two-port GSG measurement. From the experimental results, the parasitic capacitance of the ESD devices becomes larger when the ESD device has larger layout area. However, lower parasitic capacitance was observed in higher operating frequency. In a 0.13-μm CMOS process, the optimized dimensions of ESD diodes for the 5-GHz high-speed I/O interface circuits with 2-kV HBM ESD robustness have been obtained.

An ESD protection design example for the high-speed I/O interface circuits has also been proposed in this thesis. By including two types of turn-on efficient power-rail ESD clamp circuits into the high-speed I/O interface circuits, the ESD clamp devices at the input pin are operated in the forward-biased conduction, rather than the junction breakdown condition. Therefore, the dimension of ESD devices for the input pin could be reduced to reduce the input capacitive loading effect. By placing the ESD devices under the bond pad, the input capacitive load can be further reduced. This work has been successfully verified in a 0.13-μm CMOS process. The database of parasitic capacitance and ESD robustness of the ESD diodes were established. The experimental results have confirmed that the ESD robustness is more than 2kV under the HBM ESD test with proper ESD device.

5.2 Future Works

To further decrease the dimensions of the ESD device, and to enhance ESD robustness, other ESD device models, such as SCR, may need to be established. SCR is suitable for ESD protection design with low-capacitance consideration, because SCR can sustain high ESD level in a small device size. Besides, latchup issue can be avoided, because the holding voltage of SCR is higher than the operation voltage of the internal circuits which are fabricated in advanced CMOS processes, such as the 65-nm CMOS process. However, the high trigger voltage of SCR should be taken into consideration. With suitable triggering circuit to turn on SCR quickly, SCR will become the most promising ESD device for ESD protection design for high-speed I/O applications.

REFERENCES

[1] C. Richier, P. Salome, G. Mabboux, I. Zaza, A. Juge, and P. Mortini, "Investigation on different ESD protection strategies devoted to 3.3V RF applications (2 GHz) in a 0.18μm CMOS process", in *Proc. EOS/ESD Symp.*, 2000, pp. 251-259.

[2] R. Gauthier and C. Putnam, "Evaluation of diode-Based and nMOS/L_{npn} based ESD protection strategies in a triple gate oxide thickness 0.13μm CMOS logic technology," in *Proc. EOS/ESD Symp.*, 2001, pp. 205-215.

[3] S. Galal and B. Razavi, "Broadband ESD protection circuits in CMOS technology," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2003, pp. 182-183.

[4] S. Galal and B. Razavi, "Broadband ESD protection circuits in CMOS technology," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2334-2340, Dec. 2003.

[5] B. Keleveland, T. Maloney, I. Morgan, L. Madden, T. Lee, and S. Wong, "Distributed ESD protection for high-speed integrated circuits," *IEEE Electron Device Lett.*, vol. 21, no. 8, pp. 390-392, Aug. 2000.

[6] C. Ito, K. Banerjee, and R. Dutton, "Analysis and optimization of distributed ESD protection circuits for high-speed mixed-signal and RF applications," in *Proc. EOS/ESD Symp.*, 2001, pp. 355-363.

[7] C. Ito, K. Banerjee, and R. Dutton, "Analysis and design of distributed ESD protection circuits for high-speed mixed-signal and RF ICs," *IEEE Trans. Electron Devices*, vol. 49, no. 8, pp. 1444-1454, Aug. 2002.

[8] M.-D. Ker and B.-J. Kuo, "ESD protection design for broadband RF circuits with decreasing-size distributed protection scheme," in *IEEE Radio Frequency Integrated Circuits Symp*. Dig., 2004, pp. 383-386.

[9] M.-D. Ker and B.-J. Kuo, "Decreasing-size distributed ESD protection scheme for broad-band RF circuits," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 2, pp. 582-589, Feb. 2005.

[10] M.-D. Ker, Y.-W. Hsiao, and B.-J. Kuo, "ESD protection design for 1-to-10 GHz distributed amplifier in CMOS technology," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 9, pp. 2672-2681, Sep. 2005.

[11] M.-D. Ker, B.-J. Kuo, and Y.-W. Hsiao, "Optimization of broadband RF performance and ESD robustness by π-model distributed ESD protection scheme," *J. Electrostatics*, Feb., 2006.

[12] M.-D. Ker and B.-J. Kuo, "Optimization of broadband RF performance and ESD robustness by π-model distributed ESD protection scheme," in *Proc. EOS/ESD Symp.*, 2004, pp. 32-39.

[13] S. Daniel and G. Krieger, "Process and design optimization for advanced CMOS I/O ESD protection devices," in *Proc. EOS/ESD Symp.*, 1990, pp. 206-213.

[14] S. Deebe, "Methodology for layout design and optimization of ESD protection transistors," in *Proc. EOS/ESD Symp.*, 1996, pp. 265-275.

[15] C. Duvvury and C. Diaz, "Dynamic gate coupling of nMOS for efficient output ESD protection," in *Proc. IRPS*, 1992, pp. 141-150.

[16] M.-D. Ker, C.-Y. Wu, T. Cheng, and H.-H. Chang, "Capacitor-couple ESD protection circuit for deep-submicron low-voltage CMOS ASIC," *IEEE Trans. VLSI Syst.,* vol. 4, no. 3, pp. 307-321, Sept. 1996.

[17] C. Richier, N. Maene, G. Mabboux, and R. Bellens, "Study of the ESD behavior of different clamp configurations in a 0.35μm CMOS technology," in *Proc. EOS/ESD Symp.*, 1997, pp. 240-245.

[18] M.-D. Ker, H.-C. Jiang, and C.-Y. Chang , "Design of low-capacitance bond pad for high-frequency I/O applications in CMOS integrated circuits," in *Proc. ASIC/SOC Conf.*, 2000, pp.293-296.

[19] J.-H. Lee, K.-R. Peng, R.-Y. Chang, T.-L. Yu and T.-C. Ong, "The embedded SCR NMOS and low capacitance ESD protection device for self-protection schemes and RF application," in *Proc. IEEE Custom Integrated Circuits Conf.*, 2002, pp. 93-96.

[20] H. Feng, K. Gong, and A. Wang, "A novel on-chip electrostatic discharge protection design for RF ICs," *J. Microelectronics*, pp. 189-195, 2001.

[21] S. Galal and B. Razavi, "40-Gb/s Amplifier and ESD protection circuit in 0.18-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2389-2396, Dec. 2004.

[22] J. Lee, Y. Huh, P. Bendix and S.-M. Kang, "Design-for-ESD-reliability for high-frequency I/O interface circuits in deep-submicron CMOS technology," in *Proc. IEEE Int. Symp. on Circuits and Systems,* vol. 4, pp. 746-749, May 2001.

[23] T. Holloway, G. Dixit, D. Grider, S. Ashburn, R. Aggarwal, A. Shih, X. Zhang, G. Misium, A. Esquivel, M. Jain, S. Madan, T. Breedijk, A. Singh, G. Thakar, G. Shinn, B. Riemenschneider, S. O'Brien, D. Frystak, J. Kittl, A. Amerasekera, S. Aur, P. Nicollian, D. Aldrich, and B. Eklund, "0.18-μm CMOS technology for high-performance, low-power, and RF applications," in *Proc. VLSI technology Symp.*, 1997, pp. 13-14.

[24] M.-D. Ker, "Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuit for submicron CMOS VLSI," *IEEE Trans. Electron Devices,* vol. 46, no. 1, pp. 173-183, Jan. 1999.

[25] M.-D. Ker and C.-H. Chuang, "ESD protection circuits with novel MOS-bounded diode structures," *Proc. IEEE Int. Symp. on Circuits and Systems,* vol. 5, pp. 26-29, May 2002.

[26] A. Amerasekera, L. van Roozendaal, J. Abderhalden, J. Bruines, and L. Sevat, "An analysis of low voltage ESD damage in advance CMOS process," in *Proc. EOS/ESD Symp.,* 1990, pp. 143-150.

[27] MIL-STD-883E method 3015.7, Military Standard Test Methods and Proc. for Microelectronics, Dept. of Defense, Washington D.C., U.S.A., 1996.

[28] Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM), 1997. EIA/JEDEC Standard EIA/JESD22-A114-A.

[29] Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM), 1997. EIA/JEDEC Standard EIA/JESD22-A115-A.

簡歷

姓　　名：黃 俊

學　　歷：

國立台北科技大學電子工程系　　(89 年 9 月~92 年 1 月)

國立交通大學 IC 設計產業碩士專班　　(94 年 2 月~96 年 2 月)

PUBLICATION LIST

PATENTS

[1] Ming-Dou Ker, Chun Huang, and Yuh-Kuang Tseng, “ESD Protection Design for Low-Capacitance Specification,” pending for U.S.A. and R.O.C. Patents.