國立交通大學

電機學院光電顯示科技產業研發碩士班

碩士論文

五環素沈積溫度對有機薄膜電晶體電性影響之研究

Effect of Deposition Temperature on the Device Properties of Pentacene Thin-Film Transistors

研 究 生：陳映頻

指導教授：陳方中 教授

中華民國九十六年五月

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研究生：陳映頻　　Student：Ying-Pin Chen
指導教授：陳方中博士　　Advisor：Dr. Fang-Chung Chen

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碩士論文

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摘　　要

本研究以沈積溫度為變因，探討五環素未經歷嚴重晶相變化時，晶粒形貌對薄膜電晶體電性的影響。除了部分嚴重相變與高於表面處理物玻璃轉移溫度的元件外，電洞遷移率與橫向晶粒都有隨溫度升高而增加的趨勢。透過電阻萃取的方式，我們得到下述結果：通道電阻隨溫度升高而下降，此為升溫增大橫向晶粒所致；接面電阻亦隨晶粒增大而降低；塊體電阻則與晶相變態的嚴重程度有關。此外，基板經表面處理的電晶體，即使表面晶粒相似也可大幅提昇遷移率。

對表面處理的基板而言，平躺五環素的發生是一重大特徵。過去的研究仍未明確指出此位向的分子對傳輸機制有何影響。另外，文獻表示五環素於二氧化矽基板之縱向成長為丘狀成長，此將造成較深的縫道（晶界），而丘狀形貌也是 Ehrlich-Schwoebel 能障存在的表徵。

我們使用 AFM 觀察 8nm 厚(五層分子)的五環素試片，發現經表面處理的試片，其五環素晶界間有模糊化的現象，這暗示了當平躺分子存在時，E-S 能障降低。我們認為平躺五環素的存在能提昇遷移率的原因，在於此時五環素塊體的晶緣（step edge），其 E-S 能障較低，使得晶界填補較為容易。因此，即使平躺位向之分子可能導致基板表面的排列較亂，但遷移率仍舊可提升，這說明了晶界對遷移率而言仍為最具支配力的因素。

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Student: Ying-Pin Chen Advisor: Dr. Fang-Chung Chen

Industrial Technology R & D Master Program of
Electrical and Computer Engineering College
National Chiao Tung University

ABSTRACT

By varying the temperature during the deposition of pentacene, the effect of substrate temperature on the electrical performance of OTFTs, without serious disturbance of phase transition of pentacene is investigated.

First, the channel resistance is sensitive to the deposition temperature due to the difference size of grains. Second, the contact resistance reduces with increasing deposition temperature, which is likely attributed from the difference of the molecular orientation. Finally, the bulk resistance is more fluctuant to the deposition temperature for P MS-treated devices, whereas the case for HMDS-treated ones is less fluctuant probably arising from phase boundary.

Additionally, the existence of flat-lying pentacene is an important characteristic for the treated devices. However, it is unclear what role the in-plane π system plays. Based on Ehrlich-Schwoebel barrier effect, mound growth governs the vertical evolution, forming deeper crevices. According to the AFM images of initial layer, it suggests that flat-lying pentacene could lower the E-S barrier, leading to shallow boundaries. Consequently, effect of grain boundary is still the most dominant factor to the mobility.

Acknowledgement

研究所入學通知好像上星期才剛收到，兩年五千次的鐘聲卻已經從耳邊飛走了。這一路的酸甜苦辣，回味無窮卻難以細數。本文順利完成，歸功大家的鼎力相助，在這邊先向各位說一聲：謝了！

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Table of Contents

Chapter 1 Introduction

Chapter 2 Review and Principles

Chapter 3 Experimental Methods

Chapter 4 Results and Discussions

Figure Captions

Chapter 1 Introduction

Chapter 2 Review and Principles

Chapter 3 Experimental Methods

Chapter 4 Results and Discussions

List of Tables

CHAPTER 1

Introduction

1.1 Preface

“Plastic transistors” open the future of flexible displays, smart cards, radio frequency identification tags, as well as light-emitting diodes and lasers [1]. Progress in this field has been made improving the material properties and the process techniques rapidly.

For the applications of organic thin film transistors (OTFTs), the materials of active layer has to attain a minimal mobility of 1 cm^2/Vs, and a switching speed of 10^8 Hz, to compete with amorphous hydrogenated silicon (a-Si:H) [2]. Since the late 1940s, there has been a lot of research on the development of such materials [3]. These organic semiconductors, both the small molecules and polymers, have alternating single and double bonds in common. This is because that large π-conjugation length along the long axis of the molecules and close π-stacking are responsible for high carrier mobility [3].

Figure 1.1 The applications of plastic transistors: flexible displays, smart cards, RFID tags, and the nervous system of robot skin.
[Adapted from http://tech.sina.com.cn/digi/2006-04-20/1204911539.shtml]

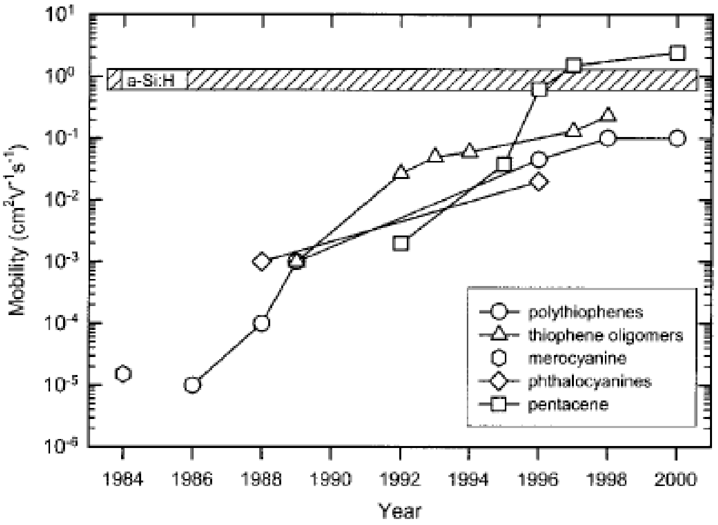


Figure 1.2 Evolution of hole mobility for the most common p-type organic semiconductors [3].

As in traditional inorganic semiconductors, organic ones can function either as p-type or n-type. Pentacene ($C_{14}H_{22}$), a rod-like aromatic molecule composed of five benzene rings, is among the most promising candidate of the p-type TFTs. It exhibits a strong tendency to form highly ordered films which depend on the surface properties of substrates and the growth conditions [4].

Substrate temperature, deposition rate, basal pressure, and roughness of the dielectrics play a crucial role on film morphology of pentacene [4] [5]. Besides, it is well known that there are two crystallographic phases of pentacene typically [6]. This requires a thorough study of the film morphology and the crystal structure as a function of the electrical properties of pentacene.

1.2 Objective and Motivation

Organic thin-film transistors (OTFTs) are of increasing interest owing to their unique properties, such as low-temperature and low-cost fabrication processes, light-weight, and mechanical flexibility. To obtain high performance, many reports [7] elevated the substrate temperature during the deposition of the active organic material. Although it has been suggested that the enhancement is due to the improved thin-film morphology, the details of mechanism is still not well-understood yet.

Unlike the inorganic crystals formed by atoms, the structure in organic materials is formed by weakly bonded molecules by van der Waals force [2]. So, to vary a factor in this kind of materials is possible to make another alteration simultaneously. For instance, by varying the temperature during the deposition of pentacene, it not only makes the grains become larger, but also leads the crystals to another phase. Although many results on growth-related electrical property of OTFTs have been published, it still disregarded the latent influence. Hence, a more complete research should be fulfilled.

In this thesis, the effect of deposition temperature on the performance of pentacene-based TFTs is investigated. Apparently, varying the temperature during the deposition seems only to make change in grain size of pentacene. Moreover, something else accompanies the substrate heating: phase transition. We will study the polymorphs of pentacene macroscopically, and the crystal structure microscopically at various deposition temperatures. Afterwards, it will afford some keys to relate the device characteristics to the crystal structure, which is a method to get insight in the fundamental transport properties.

1.3 Organization

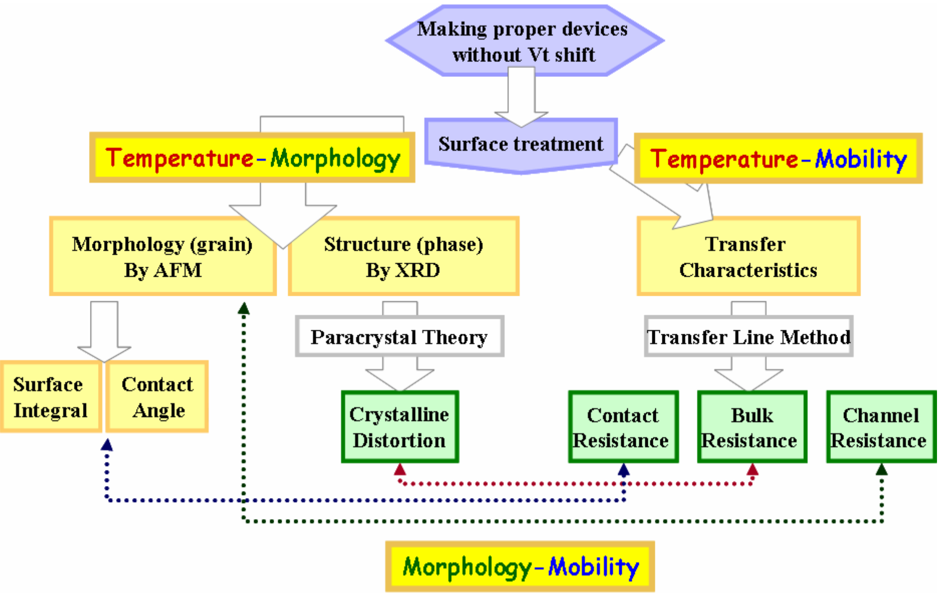
This thesis is organized as following. In this chapter, the background of this study is described briefly.

In the following chapter, we have introduced basic knowledge about TFT and organic crystals. The useful tools of analysis are also presented in this part.

Our experimental details are shown in chapter 3. From the surface treatments to electrode deposition, the procedures are illustrated. Apart from the device fabrication, the analysis methods are included.

The effect of substrate temperature on the performance of pentacene-based TFTs is presented in chapter 4. Information about electrical properties is obtained by I-V measurement. And the results are rationalized by means of Atomic Force Microscopy (AFM) and X-ray Diffraction techniques. At the beginning, we will study the relationship of mobility to deposition temperature and grains. Next, the transfer line method is employed to analyze at which part the mobility is more sensitive. Furthermore, the deduction of paracrystal theory and Ehrlich-Schwoebel barrier help us to get a more insight into the origins.

In the final chapter, we will make a conclusion.



CHAPTER 2

Review and Principles

2.1 Organic Thin-Film Transistors

2.1-1 Fundamental of Device Physics

Generally speaking, there are two methods to measure carrier mobility: time of flight (TOF) and current-voltage characteristics. But in this study, we will focus on the electrical information of pentacene-based TFTs from the current- voltage characteristics.

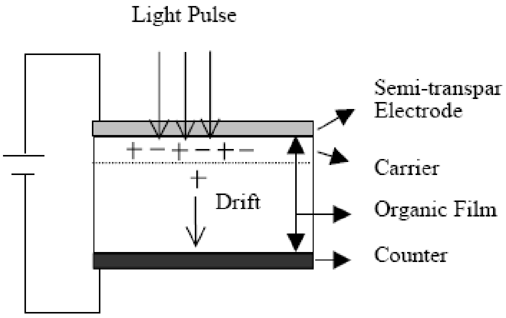


Figure 2. 1 Schematic diagram for the TOF system which could measure the carrier mobility directly. [8]

It uses a light pulse on the organic film, which absorbs photons to generate hole-electron pairs. Next, to apply a bias to the two electrodes of the film, the electrical field will force hole-electron pairs to separate. After that, there will be a transient photocurrent whose life time could determine the drift velocity.

Modeling of the Field-Effect Transistors

At lower V_D, which means $-V_D << -(V_G-V_T)$, I_D increases linearly with V_D, and determined from the following equation:

$$I_D = \frac{WC_i\mu}{L}(V_G - V_T - \frac{V_D}{2})V_D \;=>\; g_m = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D=\text{constant}} = \frac{WC_i}{L}\mu V_D$$

At higher V_D, which means $-V_D > -(V_G-V_T)$, I_D tends to saturate, and determined by the equation:

$$I_D = \frac{WC_i\mu}{2L}(V_G - V_T)^2 \quad => \quad \sqrt{|I_D|} = \sqrt{\frac{WC_i\mu}{2L}}(V_G - V_T)$$

Mobility calculated from the linear and saturation regime should be identical in single crystal. If the two mobility values have large difference, the origin could be the high concentration of trap states in the channel [3].

Limitation

Note that W/L has to be larger 10 to prevent from the effects of fringe currents flowing outside the channel, resulting in mobility overestimation [3]. Moreover, above equations are deduced from the MOSFET model, and is only valid when μ is constant. But in some situations, mobility is gate bias dependent.

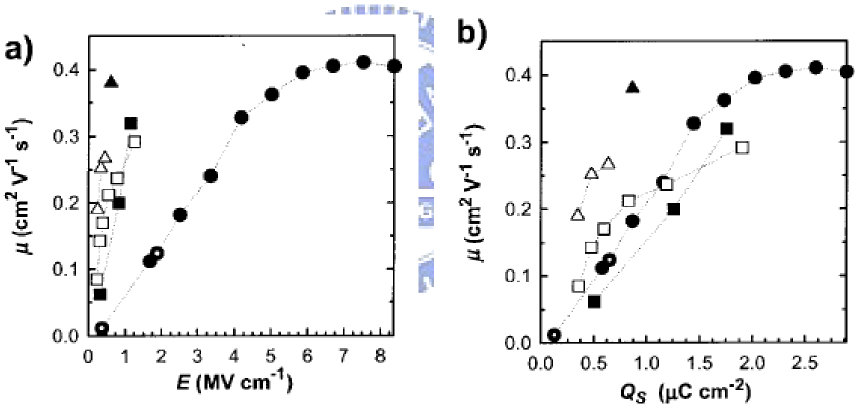


Figure 2. 2 (a) Dependence of field-effect mobility on gate field, E. (b) Dependence of field-effect mobility on charge per unit area, Qs.[3]

2.1-2 Density of States (DOS) [9]

Commonly, a distribution in energy of trapping states determines the electronic characteristics of semiconductor layer, and therefore, the performance of the TFT. The density of states (DOS) can be divided into deep states and tail states. Based on a great deal of research about a-Si:H, it demonstrates that the trap distribution in mobility gap may be modeled as:

$$N_t(E) = N_{tail}\exp(-\frac{E}{kT_t}) + N_{deep}\exp(-\frac{E}{kT_d}),$$

where kT_t and kT_d are the associated slope of the exponential distribution, N_{tail} and N_{deep} are the DOS per volume and energy at the valence band edge of the tail and deep states, respectively.

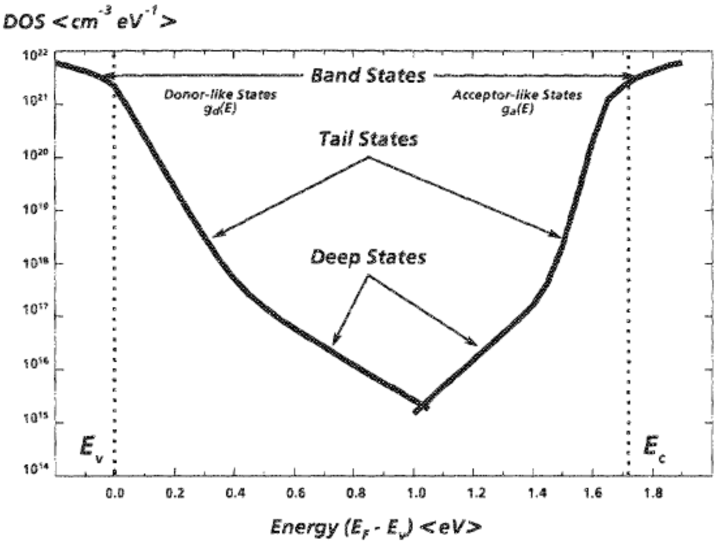


Figure 2. 3 Density states in the band gap of intrinsic a-Si:H. [10]

2.1-3 Static Characteristics and Trapping States [9]

It is believed that the deep states arose from impurities influence the threshold voltage and subthreshold behavior, while the tail states caused by disorder affect the performance when the TFT is switches on [11]. For a-Si TFTs, four regimes of operation can be identified: above-threshold, forward subthreshold, reverse subthreshold, and Poole-Frenkel emission. However, the reverse subthreshold regime is usually absent for OTFT.

Above-Threshold & Forward Sub-threshold Region

In the above-threshold regime, the Fermi level enters the tail states of the valence band. The carriers trapped in tail states play a more important role than those trapped in interface states due to the exponential increase of tail stats. In contrast, in the sub-threshold regime, the Fermi level moves into the middle gap close to its intrinsic level. So, most of the induced carriers fill the deep localized states in the pentacene bandgap and the interface states at the pentacene/insulator interfaces.

Poole-Frenkle Emission

While the molecules cannot form a perfect crystal leading to a unity energy level, some localized levels are occurred. The carriers have to overcome the discrepancy of each level to hop between molecules [8]. The barrier arising from the disparity of energy level can be lowered by an applied electric field. Consequently, the mobile carriers are produced by Poole-Frenkel field-enhanced thermionic emission at the gate/drain overlap region.

The Poole-Frenkel region is lowered the barrier by an applied field, and a current density can be expressed by

$$J \sim E \exp(\frac{2A\sqrt{E} - B\phi}{kT})$$

where E is the applied electric field.

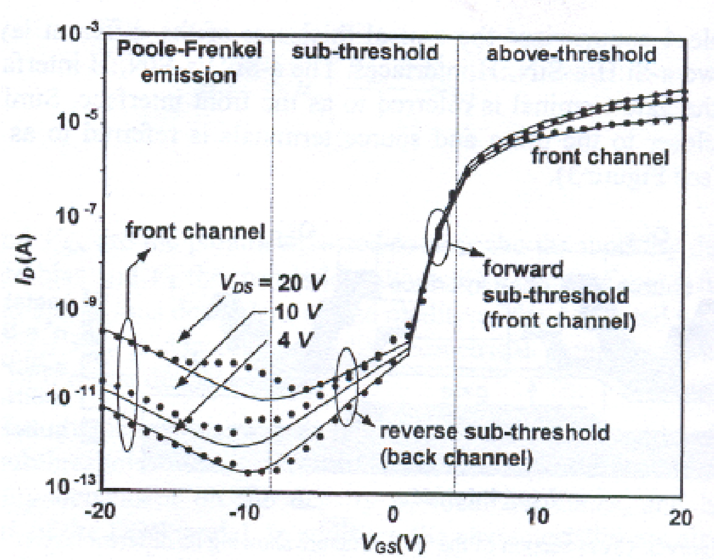


Figure 2. 4 The plot of drain current as a function of gate voltage shows four regimes of operation. [9]

2.2 Organic Conductors

2.2-1 Conduction Mechanism

In the late 1970s, the first conducting polymer, doped polyacetylene, was discovered by Heeger, MacDiarmid and Shirakawa. Doped polymers reach conductivities of 10^5 S/cm, which is much better than that of 10^{-5} S/cm in the general polymers [2]. It is a challenge to gain insight into the conduction mechanism.

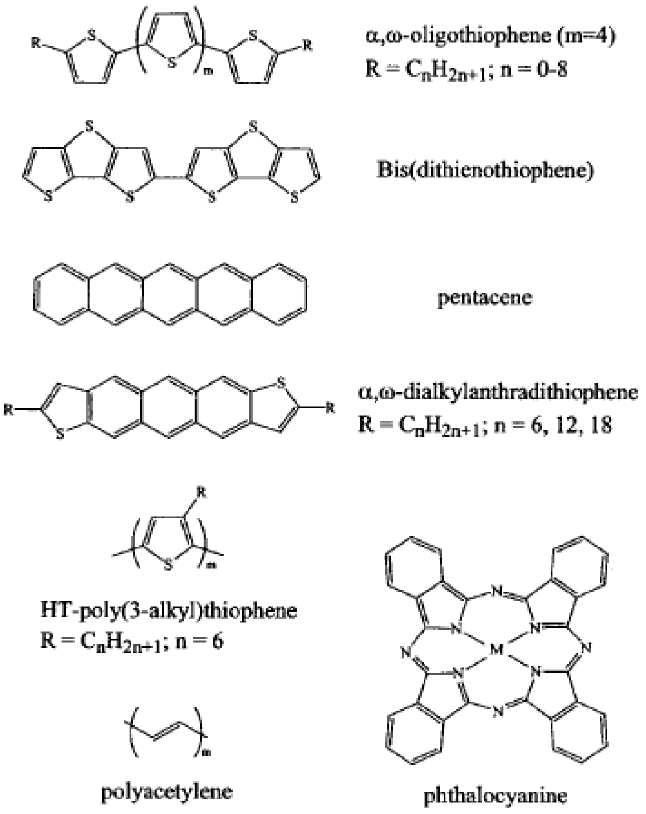


Figure 2. 5 Molecular structures of common p-type organic semiconductors [3].

Schön, Kloc and Batlogg have performed space-charge-limited-current measurements on pentacene crystals [12]. The observed charge transport behavior was, at low temperatures, described as band like transport, which crosses over, at high temperatures, to a hopping mechanism.

Band Transport [3] [12]

At low temperatures, coherent band transport of delocalized carriers is the prevalent mechanism in single crystals of pentacene. In the case, carriers move as highly delocalized plan waves in wide bands. But the lattice vibration could disintegrate the perfect plan waves in periodicity, resulting in interaction between the carriers and lattice atoms. The "bandwidth" decreases with increasing temperature due to coupling with phonons (lattice vibration) to scatter the carriers.

Hopping [3] [12]

At higher temperatures, the strong electron-phonon coupling directs to another mechanism. Because the interplay between carriers and intermolecular vibrations leading to the charge localization, it forms a "lattice polaron". Consequently, the incoherent hopping motion would be improved by thermal activation. The charge carrier has a certain probability to migrate to its neighboring molecules by either energetically vertical hopping or horizontal tunneling.

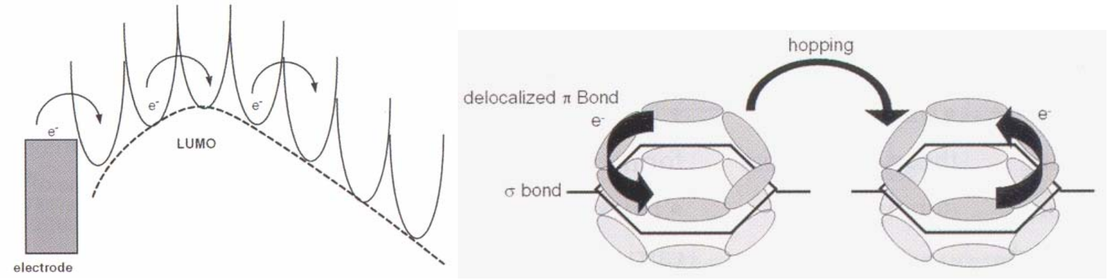


Figure 2. 6 Carrier transport in the organic semiconductors. [13]

Anisotropy

The pentacene molecules within the a-b plane are arranged in a herringbone stacking as shown in Figure 2. 7. Schön et al. [12] also have found that the conductivity of pentacene single crystals is strongly anisotropic.

Although an even higher mobility of 3.2 cm^2/Vsec has been obtained for the transport path along the d direction, it is noticeable that the charge transport mechanism in all directions is the same, even the direction perpendicular to the a-b plane (c' axis).

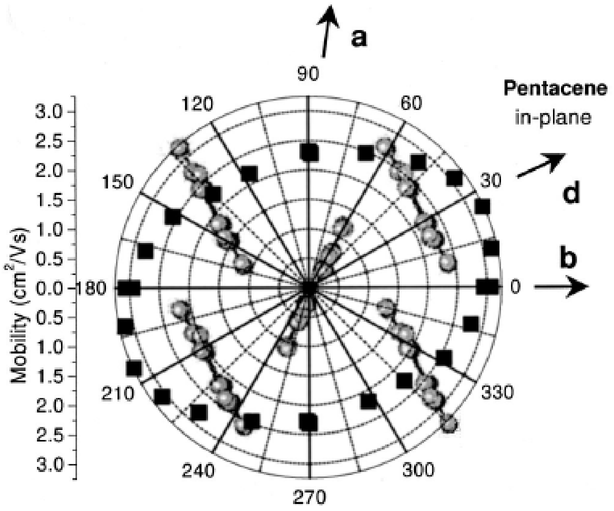


Figure 2. 7 Hole mobility within the a-b plane of pentacene single crystals at room temperature. The d direction is the high-mobility direction for hole transport. [12]

2.2-2 Crystal Structure

Gautam and Gavezzotti have studied on a lot of planar aromatic hydrocarbons [14]. There are four basic structures recognized as shown in Figure 2. 8. The basis used to distinguish between these four is the length of the shortest axis and the angle between the molecules. For example, the longest axis length is a sandwiched herringbone structure.

Because of the complex shape of molecules, it is not possible to form a FCC lattice, resembling the close-packed structure of inorganic crystals. For disk shaped molecule, it tends to form in β structure, while elongated one prefers to crystallize in herringbone stacking. But, structure prediction is still difficult due to polymorphism.

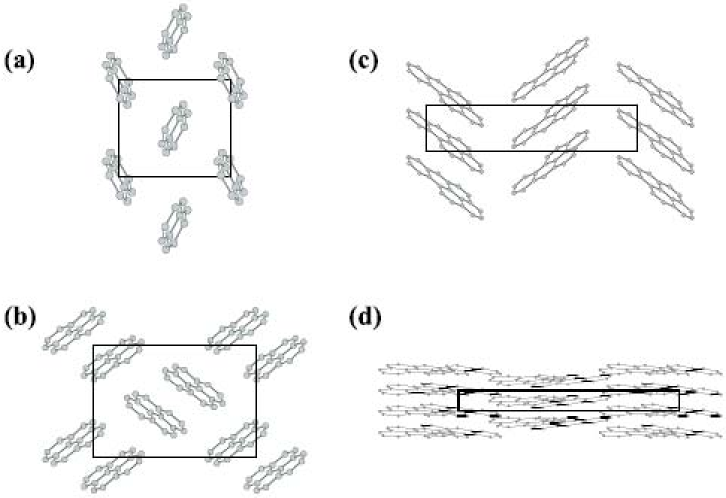


Figure 2. 8 Four basic structural types were defined for these planar hydrocarbons. (a)Naphthalene, forms in a herringbone structure. (b)Pyrene, forms in a sandwiched herringbone structure. (c)Benzoprrene, an example of a γ structure. (d) Violanthrene, an example of a β structure [14].

For pentacene, it is a herringbone structure.

2.3 Pentacene

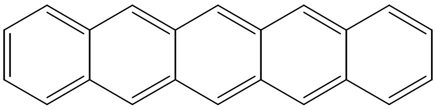


Figure 2. 9 Lewis structure of pentacene.

The first identification of pentacene structure was performed by Campbell and coworkers in 1961 [15], with a unit cell of dimension a=7.93, b=6.14, c=16.03Å, α = 101.9°, β = 112.6°, γ=85.8°, and a d-spacing of 14.4Å. Since 1990s, pentacene has been frequently used in TFTs. A new d-spacing was recognized to be 15.4Å. The two observed d(001) values of 14.4 and 15.4Å are commonly referred to as the "bulk phase" and "thin film phase," respectively [3].

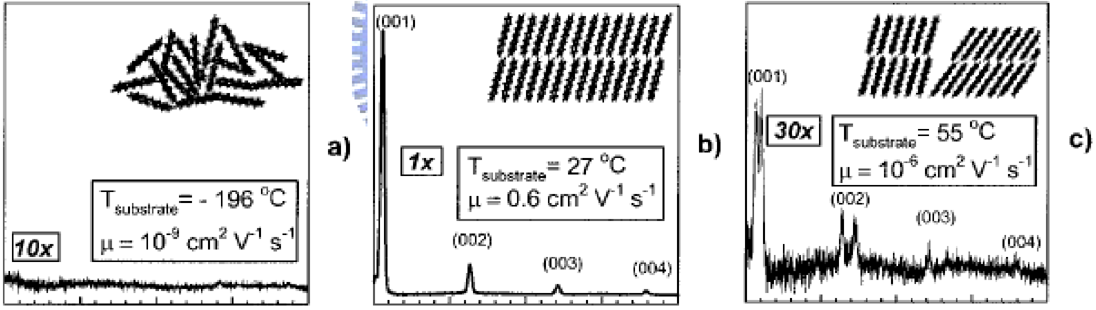


Figure 2. 10 X-ray patterns, schematic structural order, field effect mobility corresponding to 3 substrate temperatures.[3]

It is believed that large π-conjugation length along the long axis of molecules and close packing along the short axis are two key conditions for high mobility. As shown in Figure 2. 10 (a), amorphous pentacene produced at -196℃ is practically insulating due to the fact that the overlap of the molecular orbitals is very limited. However, when the substrate temperature rises, the high order is formed, and the mobility is better than the case of (a).

From the (b) and (c), we have to distinguish between the “thin film phase” and “bulk phase” of pentacene. Although the temperature is higher than RT, another phase is started growing, the mobility of this mixture is very low, possibly due to the high defect arising from the phase boundaries.

Actually, at least four polymorphs of pentacene are present, characterizing by d-spacing of 14.1, 14.5, 15.0, and 15.4Å [16] [17]. Typically two, 14.5 and 15.4Å, are the “thin film phase” and “bulk phase,” respectively. They have been reported to depend on the film thickness and the substrate temperature during deposition [4]. The former is usually grown at RT, while the latter is presented above a critical thickness and at a higher substrate temperature. The uncommon two, 14.1 and 15.0Å, is strongly depending on what type of substrates is employed: ex. Kapton, a commercial polyimide.

Finally, purity of the pentacene is also important. For example, iodine-doped pentacene is a p-type material, but alkaline metal-doped pentacene is an n-type one [3].

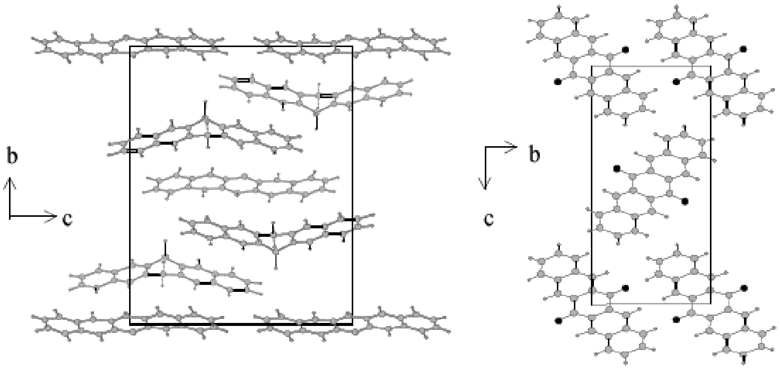


Figure 2. 11 Common impurity in pentacene. Left: 6,13-dihydropentacene. Right: 6,13-pentacenequinone. The unit cell is also indicated. [2]

2.4 The Growth of Thin Film

2.4-1 The Mechanism of Deposition of Thin-Film [18]

Traditionally in inorganic system, the deposition of thin film can be divided into several parts as follows:

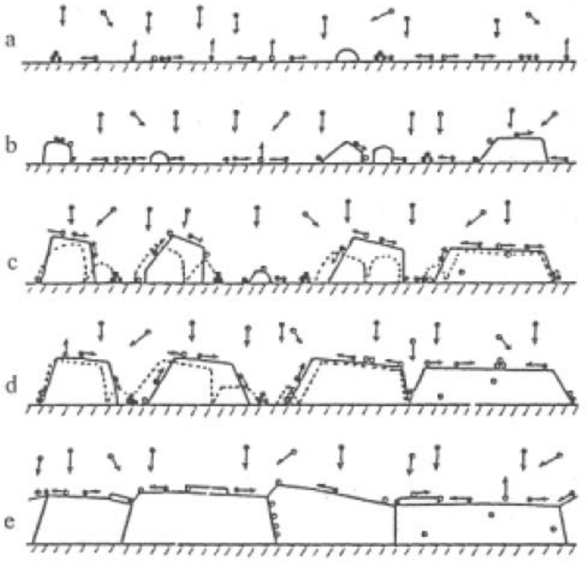


Figure 2. 12 The 5 steps of deposition of thin film.
(a) Nucleation, (b)Grain growth, (c)Coalescence, (d)Filling of channels, (e)Film growth. [18]

Nucleation

Firstly, when the energetic molecules pass through the boundary layer, most parts of them have to stay a sufficient period of time to diffuse. The energy of these molecules is consumed in the horizontal direction until they are adsorbed physically by the surface, but the energy in the vertical direction is still retained. Subsequently, the adatoms is likely to release condensation heat to form a stable cluster chemically, or to desorb into vapor phase.

If the adatoms can form a stable cluster, the total free energy has to be negative. From the Figure 2. 13, at the beginning of radius enlarging, the total free energy presents a positive slope, which is unfavorable for grain growth. However, as long as the radius larger than a critical value, the total free energy has a negative slope, which is favorable for grain growth [19].

The model described above does not involve into interface between grains and substrates. For the heterogeneous nucleation, it is not proper to assume the grain shape is spherical. The wetting angle should be considered.

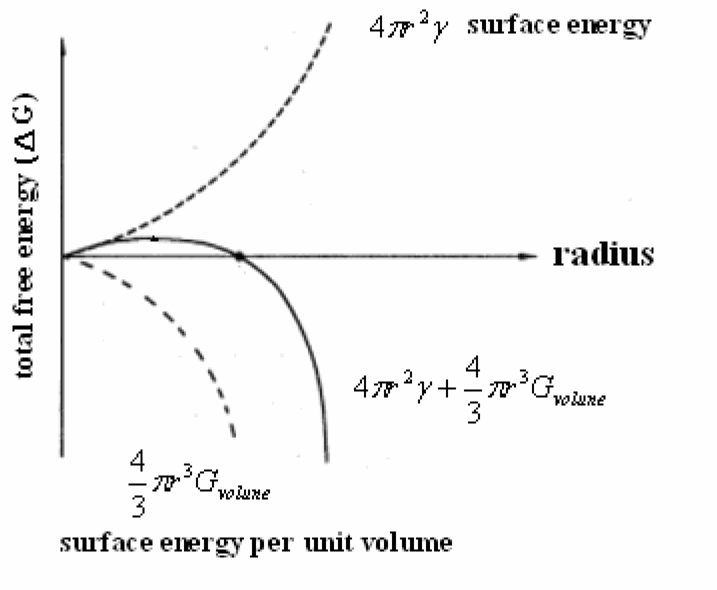


Figure 2. 13 The relationship of free energy to radius of grains.
γ is the surface energy per unit of the clusters, and G_{volume} is the surface energy per unit volume. [19]

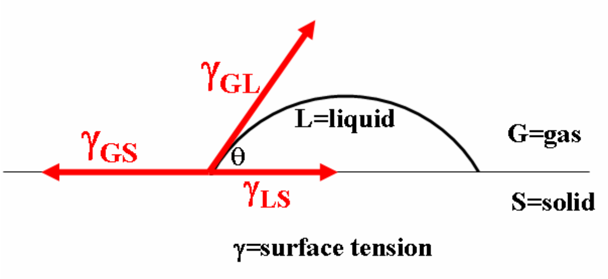


Figure 2. 14 Wetting angle in the heterogeneous nucleation.[19]

Grain Growth and Coalescence

After clusters possessing a critical radius, the grain growth (step b) starts. Unlike the previous step, the growing grains can catch the molecules from vapor phase directly, not localized the adatoms.

When the individual grain is large enough to contact each other, coalescence occurs. In order to decrease the surface energy, inter diffusion between each grain proceed to fill the neck.

However, if the crystal structure of both grains is not identical, one is <111> and the other is <110> for instance, it has to be through recrystallization, stabilizing the energy states of new grains [18].

2.4-2 Fractal –Mound Growth of Pentacene Film

The mechanism of pentacene growth on SiO_2 substrate has been studied [20]. The model of Diffusion-Limited Aggregation (DLA) governs the lateral growth, while the Ehrlich-Schwoebel barrier effect disrupts the desired epitaxial growth for the subsequent layers, leading to mound growth.

Diffusion-Limited Aggregation

With sufficiently low nucleation density, the terraces of pentacene islands have a fractal dimension of 1.6~1.7, agreeing a lateral DLA shape [1]. After the molecule sticks to the edge, the transient diffusion at the step edges might occur immediately and continue until it finds a suitable site.

Ehrlich-Schwoebel Barrier

Step-flow growth is often under the assumption that adatoms bond to ascending and descending steps with equal rates. However, an excess energy barrier to migration over descending steps exists, which produces an adatom “uphill current.” For example, if a terrace is larger than its upper neighbor, it will receive more adatoms flux which preferentially attach to the ascending step [21][22].

From the left of Figure 2. 17, the subsequent layer does not start forming until the first one completes. It denotes a layer-by-layer mechanism as opposed to the mound growth.

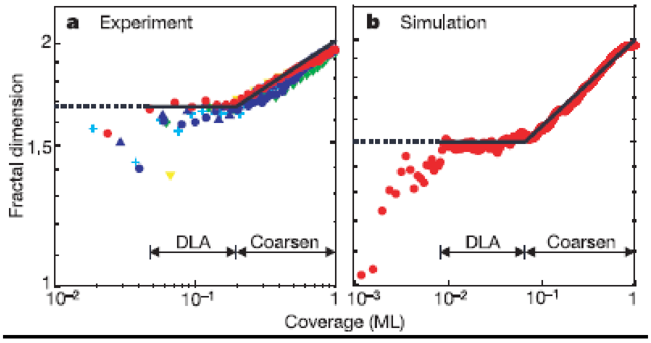


Figure 2. 15 Coverage-dependent fractal dimension of single-molecular-layer pentacene islands on cyclohexane-saturated Si(001). [1]

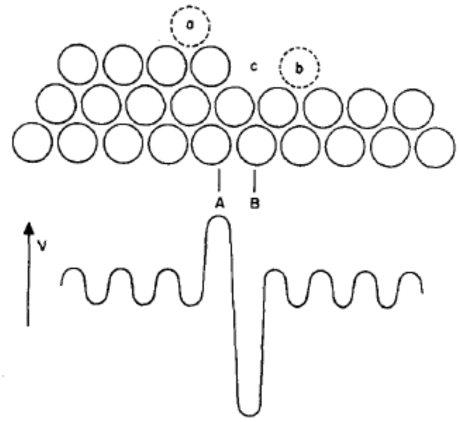


Figure 2. 16 The cross section of a monatomic step in a surface and the hypothetical potential associated with the diffusion of an atom over such a surface.[22]

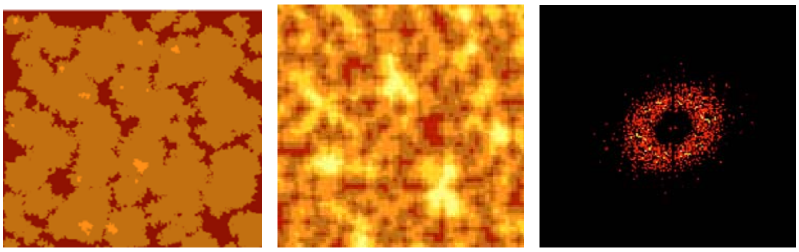


Figure 2. 17 (Left) A simulated surface without the presence of the Ehrlich-Schwoebel barrier, (Meddle)A simulated surface approaching real situation, (Right) Fourier transform of a typical pentacene surface. Ring structure is a sign of mound growth. [20]

2.5 X-Ray Diffraction Analysis

2.5-1 The Scherrer Equation [23] [24]

$$L_{hkl} = \frac{K\lambda}{\beta \cos\theta}$$

where L_{hkl} is the average of the crystallite size perpendicular to the planes (h k l), β is the breadth at intensity of half-maximum in radians, and K is a constant commonly assigned a value of unity. The normal form can be expressed the reflection breadth in δs units as follows:

$$L_{hkl} = \frac{K}{[2\cos\theta/\lambda]\delta\theta} \approx \frac{1}{\delta s}, \text{ where } s=2(\sin\theta)/\lambda$$

2.5-2 Distortion of the First and Second Kinds [24]

Hosemann postulates that a real crystal is subject to two distortions: first and second kinds, as shown in Figure 2. 18.

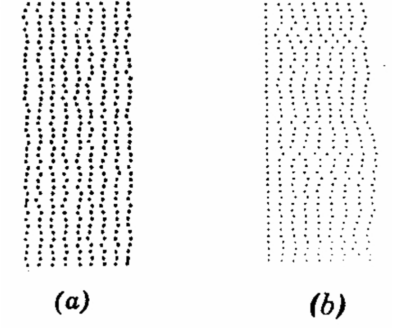


Figure 2. 18 Optical diffraction models of lattice with 1-D distortions (a) of the first kind, and (b) of the second kind. [24]

Distortion of First Kind (g_I)

If a lattice is influenced only by the distortion of first kind, the long-range periodicity is preserved. It means that the distortion is displacements of the structural elements, such as atoms or motifs, from the ideal lattice points.

Assume the distribution of displacements from the ideal sites is Gaussian:

$$D(m) = \exp(-4\pi^2 g_I^2 m^2),$$

the effect of distortion (I) on the diffraction patterns will be indistinguishable from the effect of thermal vibration. Thus, the distortion (I) is regarded as frozen-in thermal displacements, resulting in a falling off of the intensity of a set of reflections with increasing order, m. However, it makes no broadening.

Distortion of Second Kind (g_{II})

If a lattice possesses the distortion of second kind, the long-range periodicity is lost. It means that each lattice point varying in position only relates to its neighboring ones rather than to the ideal sites. Compared to the distortion (I), the distortion (II) results in both a decrease of intensity and an increase of breadth with higher reflection order m.

2.5-3 Paracrystal Theory [24]

For semicrystalline systems, the Scherrer equation is used to describe the relationship of the breadth to crystallite size. However, the breadth is always broader than the expectation of crystallite-size effect due to the distortion of second kind. Thus, the Sherrer equation should be replaced by:

$$(\delta s)^2 = (\delta s)_c^2 + (\delta s)_{II}^2 = \frac{1}{L_{hkl}^2} + \frac{\pi^4 g_{II}^4 m^4}{\bar{d}_{hkl}^2}, \text{ where } \delta s = \frac{2\cos\theta\delta\theta}{\lambda},$$

which is valid if $2\pi^2 g_{II}^2 m^2$ is much smaller than unity, and the broadening profiles are Gaussian shape exhibiting the polydispersity is small.

In this equation, (δs) is the total broadening excluding instrumental broadening, λ is the X-ray wavelength, $\delta\theta$ is the breadth expressed in radians, $(\delta s)_c$ and $(\delta s)_{II}$ is the broadening from the crystal size and lattice distortion of second kind, respectively. As to $\overline{d_{hkl}}$, it is the spacing of (hkl) planes from Bragg's law.

CHAPTER 3

Experimental Methods

3.1 Device Fabrication

3.1-1 Preparation of Substrates

In our work, heavily doped n-type silicon wafer with thermal SiO_2 was chosen as the device substrate. The 200nm-thick SiO_2 grown on the polished side of the wafer was served as the gate dielectric, and the Al metallic layer deposited on the other side formed the gate contact.

Subsequently, the SiO_2 surface was cleaned with “half RCA procedure” which means de-ionic water, H_2SO_4-H_2O_2 solution (3:1 by volume), de-ionic water, in order. The details were illustrated in Figure 3.1.

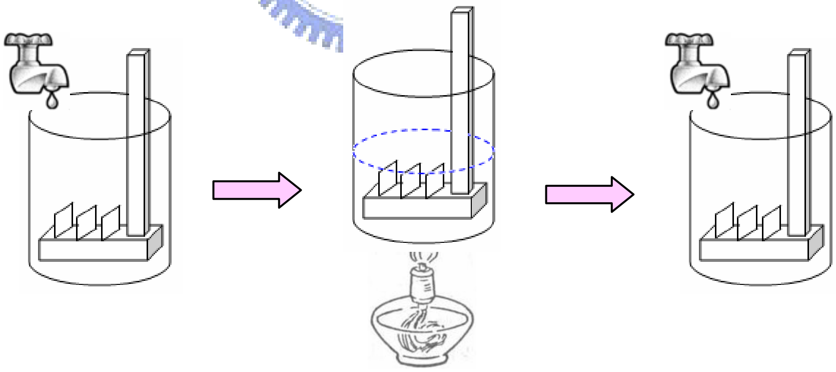


Figure 3.1 The procedure of substrate cleaning.

Step 1: *Place the wafers on the Teflon carrier, and pre-rinse the wafers in the D.I. water for 5 minutes.*

Step 2: *Submerge the carrier with wafers in the* H_2SO_4-H_2O_2*(3:1) solution, and keep the temperature at 85 ℃ for 20 minutes.*

Step 3: *Remove the carrier from the acidic bath, and rinse it again in the D.I. water beaker for 5 minutes.*

Step 4: *Blow the wafers dry with nitrogen gun.*

3.1-2 Surface Treatment

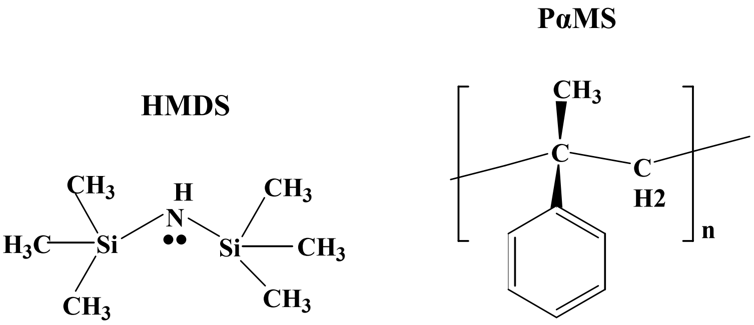
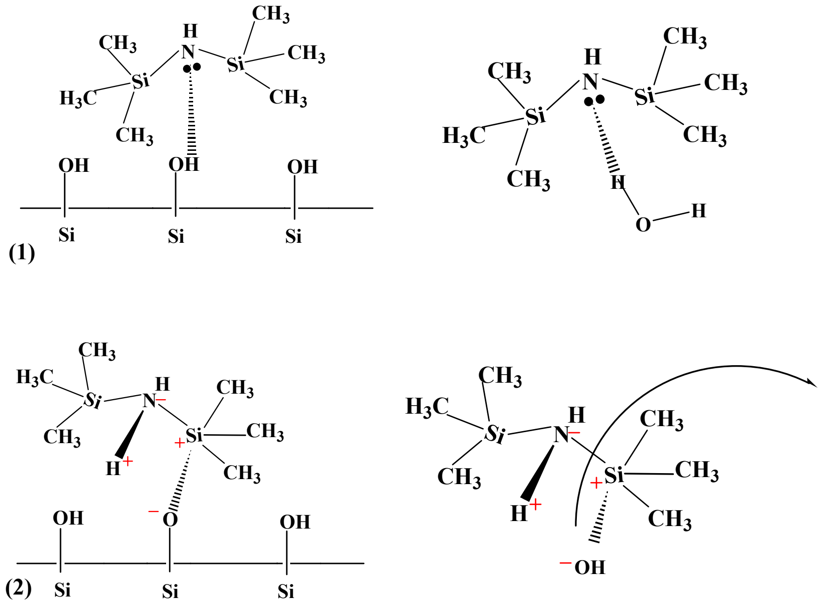


Figure 3.2 The chemical formula of 1,1,1,3,3,3- hexamethyldisilazane and poly(α-methylstyrene).

After the substrate cleaning, we tried 3 types of surface treatments. Two chemicals,1,1,1,3,3,3- **h**exa**m**ethyl**d**i**s**ilazane (HMDS)and **p**oly(**α**- **m**ethyl**s**tyrene) (P MS), were spread onto the SiO_2 surface, and bare one was used as a reference.

For the two modifications, one was evaporated in the HMDS oven at 150℃, while the other was spin coated with 0.3wt% solution of PαMS in toluene. Further postbaking was not applied to the HMDS -treated substrate to prevent any change of surface properties. On the contrary, postbaking was done for the PαMS-treated one at 80℃ for 1 hour to remove residual solvent. The HMDS film was too skinny to be estimated, and the P MS film was about 8-nm-thick.



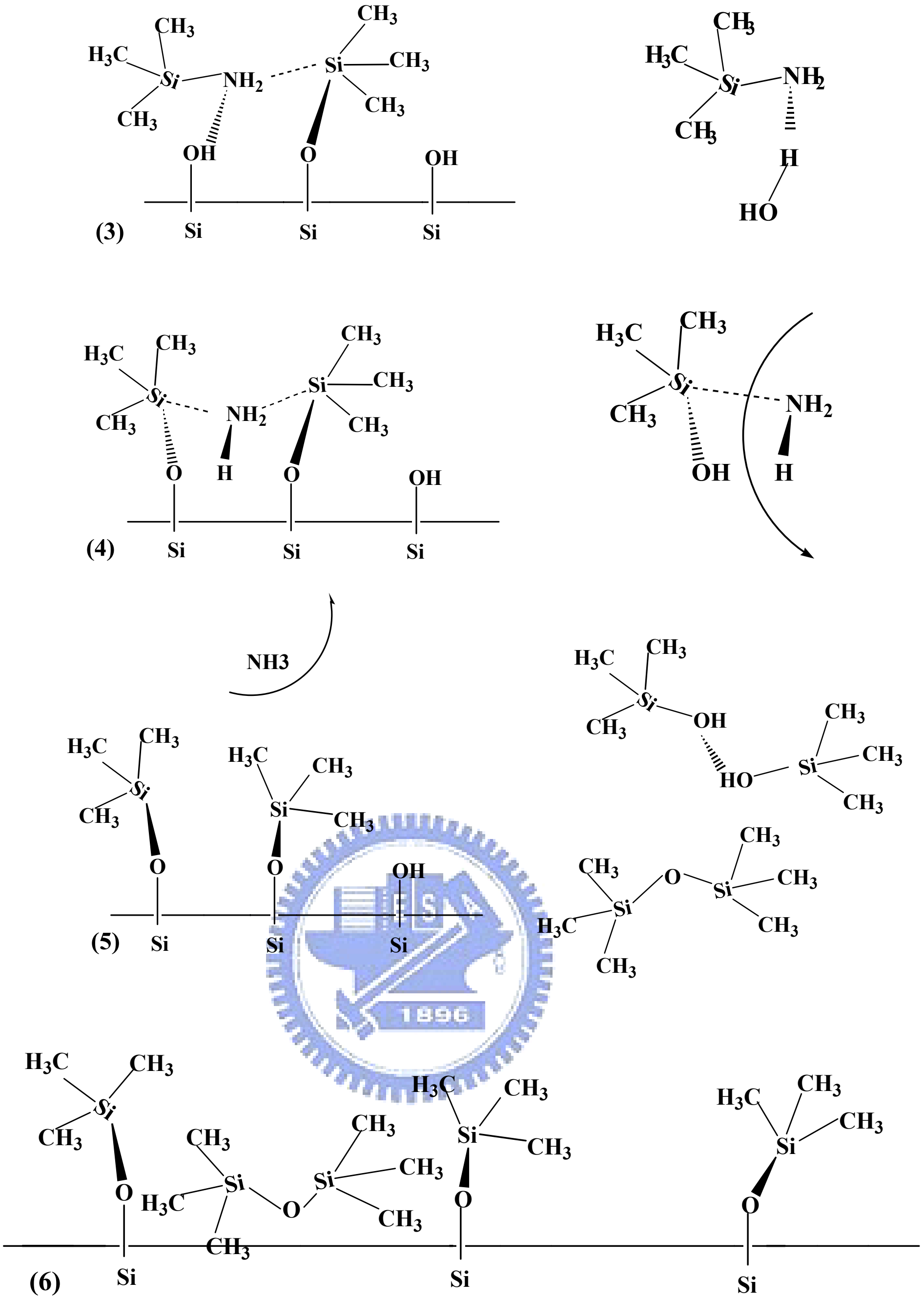


Figure 3.3 A probable mechanism for the chemical reaction of HMDS.
HMDS can change the OH-terminated SiO_2 to a $(CH_3)_3$-Si-terminated one.

3.1-3 Growth of Thin Film and Electrodes

Next, 99.9% pentacene purchased from Fluka without additional purification, was employed as the active layer. It was sublimated by thermal coater under a back pressure below 1.1×10^{-6} torr. The substrate could be heated from 17℃ to 90℃, and measured with an Al-Cr thermocouple. As for deposition rate, it was controlled at a rate of 0.5 Å/sec by a quartz oscillator during the thin-film formation. A shutter allowed the stable pentacene flux to pass until the total thickness approached 60 nm.

In order to match the work function of pentacene, whose HOMO is about 5.1eV, gold is appropriate for pentacene-based OTFTs as source/drain electrodes. Accordingly, 35-nm-thick Au, as top contacts, was deposited at a rate of 2~3 Å/sec through a shadow mask under 3×10^{-6} torr. The channel width (W) was 2000µm for all devices in this study, and channel lengths (L) were varied as 75, 95, 130, 160µm.

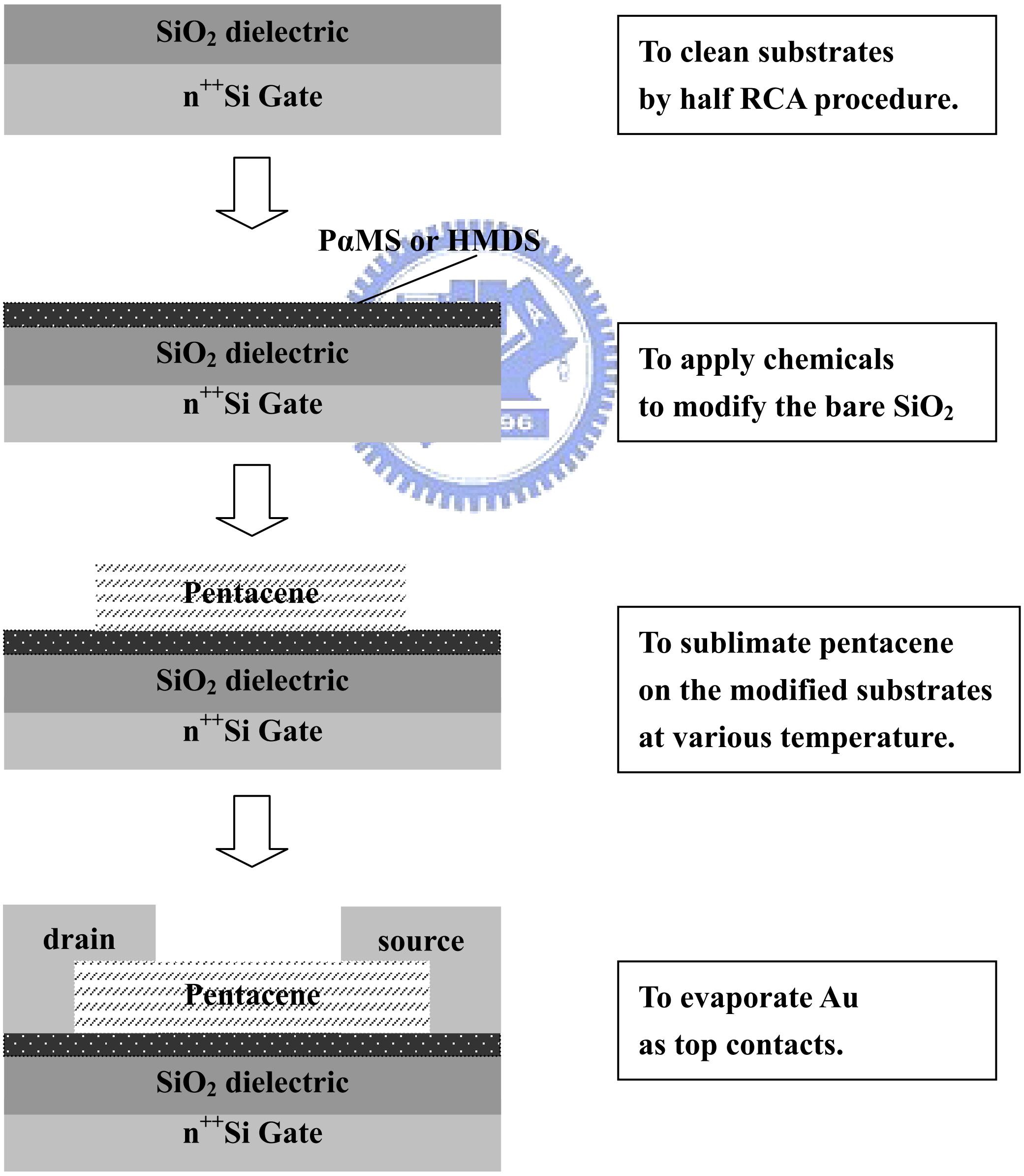


Figure 3.4 The flow chart of experimental procedure.

3.2 Device Measurement

Electrical characterization was taken in a light-isolated probe station, connected to a semiconductor parameter analyzer (Keithley 4200) at room temperature in atmosphere.

For pentacene-based devices, a negative bias of gate voltage was applied to accumulate holes in the p-type active layer. In the I_D-V_D measurement, the drain bias was swept from 0 to -60 Volts and the gate voltage step were 0, -15, -30, -45, -60 Volts, respectively. In the I_D-V_G measurement, the gate bias ranged from +20 to -60 Volts, and the drain voltage step were 0, -15, -30, -45, and -60 Volts. However, it could be modulated in special case.

3.3 Instrument and Chemicals

Name	**Type Specification**
Vacuum Oven	Yield Engineering Systems, **YES** - 5
Spin coater	Chemat Technology, KW-4A
Thermal coater	ULVAC, CRTM-6000
Semiconductor parameter analyzer	Keithley 4200
AFM	DI3100
XRD	M18 XHF, MacScience
Contact angle	Kruss Universal Surface Tester, GH100
Pentacene	Fluka
poly(α-methylstyrene)	Aldrich M.W.= 4000

CHAPTER 4

Results and Discussions-
Electrical properties vs. Morphology

4.1 Review of Prior Arts

At the beginning, we will introduce a similar research about the effect of substrate temperature on the device properties. Jiyoul Lee et al. [25] has reported that the grain size of the pentacene enlarges with the substrate temperature accompanies by a phase transition. Nevertheless, the hole mobility is not improved much by varying the temperature as expected. In addition, Lee has observed that the XRD peak intensities of large grains were much lower than those with small grains. It seems to suggest that the large grains may contain more defects or disordering. Consequently, they have attributed the little fluctuation of mobility to a higher density of traps at higher temperature.

Although a similar research has been done, the result cannot distinguish the thin-film phase and bulk phase, which are affected by the substrate temperature simultaneously. Otherwise, different crystal systems may have different absorption coefficient of X-ray [23] [24], which means the XRD intensities may not compare with each other simply. In other words, lower intensity is not necessary to stand for less ordering. It is probably to make the XRD spectra to become invalid in the study. In contrast, we have separated the two factors, the enlargement of grain size and the phase transition, successfully. That will make the XRD more significant for the conclusion.

4.2 A Preparation by Making Use of SiO_2 Substrate

Part A: Morphology Evolution

4.2-1 The Relationship between the Deposition Temperature to the Grain Size

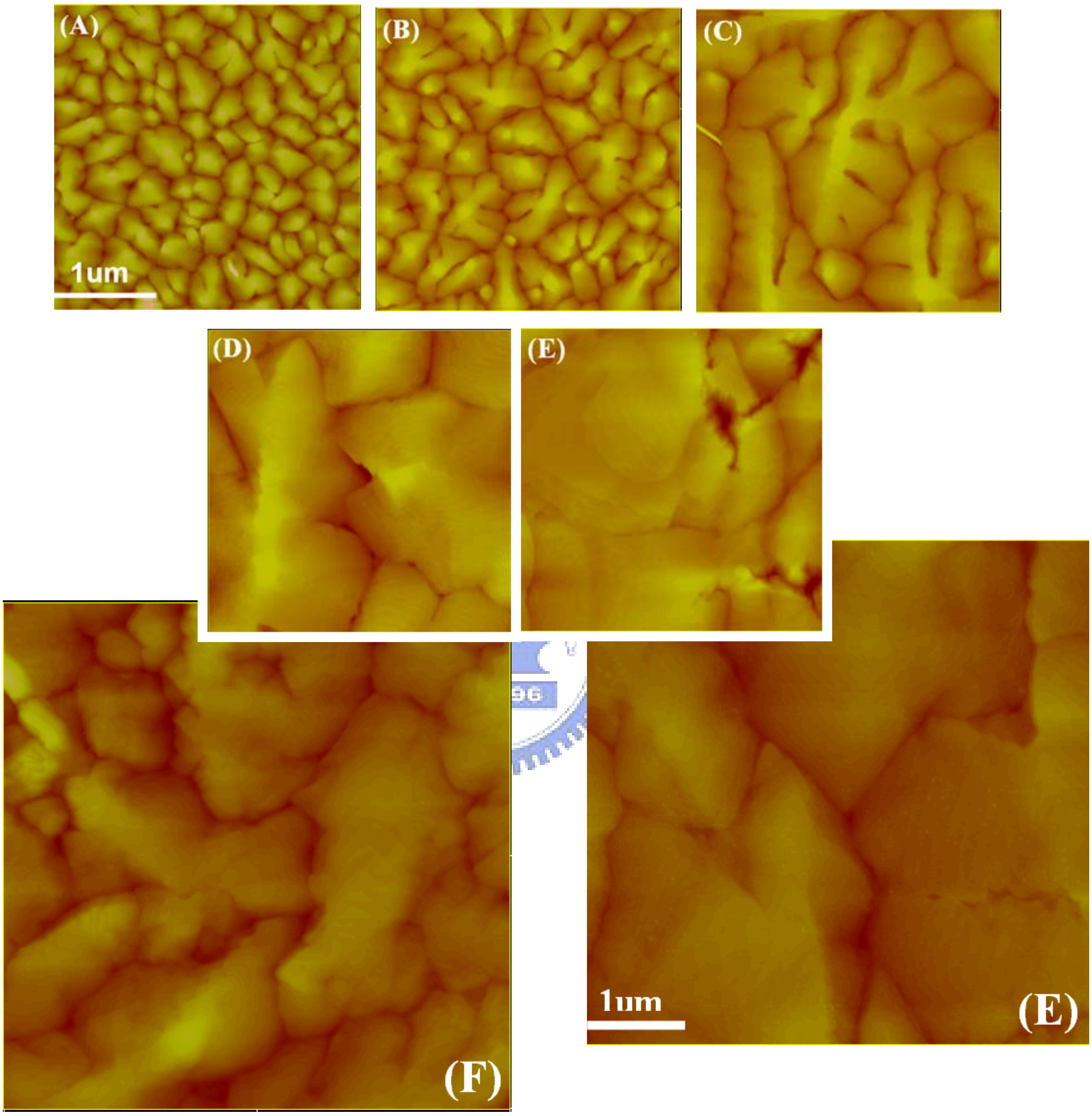


Figure 4. 1 AFM images of 60-nm-thick pentacene deposited at a fixed flux rate of 0.5Å/sec on a 200-nm-thick SiO_2 substrate without surface treatment at various deposition temperatures. The focus position is between the source/drain electrodes. (A)T =17℃, R=10.273nm. (B) T =30℃, R=9.610nm. (C) T =50℃, R=8.976nm. (D) T =70℃, R=6.680nm. (E) T =90℃, R=7.105nm. (F) T =110℃, R=8.570nm.

All the images are 3×3μm^2 except the bigger two which are 5×5μm^2.
(R: roughness presented by root-mean-square form)

The AFM images of Figure 4. 1 display the surface morphology of 60-nm-thick pentacene deposited on bare SiO_2 substrate at 17℃, 30℃, 50℃, 70℃, 90℃, and 110℃ respectively. The rms surface roughness of each film varied in the range of 6-10nm. Note that it merely forms stable film until the substrate is heated at 120℃ which is probably due to the equal rate of adsorption and desorption.

According to the evolution of morphology, the grains show a progress enlargement conspicuously as the substrate temperature goes up. Since the grain boundaries behave as a barrier against carrier hopping [11], it is believed that larger grain sizes, which mean less grain boundaries, should be more conductive.

Part B: I-V Characteristics

4.2-2 The Mobility Calculation

In the following section, we will extract the mobility (μ) from the saturation regime of the field-effect transistor model.

At higher V_D, which means $-V_D > -(V_G-V_T)$, I_D tends to saturate, and is approximately determined by the equation:

$$I_D = \frac{WC_i\mu}{2L}(V_G - V_T)^2 \quad => \quad \sqrt{|I_D|} = \sqrt{\frac{WC_i\mu}{2L}}(V_G - V_T)$$

We have obtained μ from the maximum tangent in the plot of $\sqrt{|I_D|}$ versus V_G, i.e. slope=$\sqrt{\frac{WC_i\mu}{2L}}$. It is important to note that this equation is only valid when μ is constant. Thus, despite of the most widespread use, it should be treated as an approximate value.

4.2-3 The Transfer Characteristics

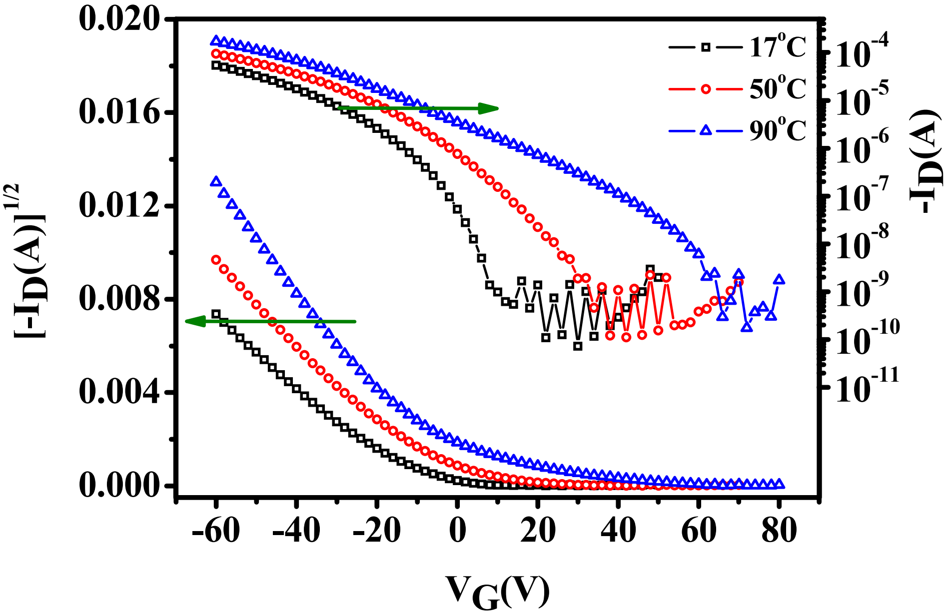


Figure 4. 2 The transfer characteristics of the OTFTs, which were fabricated at various deposition temperatures with bare SiO_2 substrate, obtained under V_D=-60V.

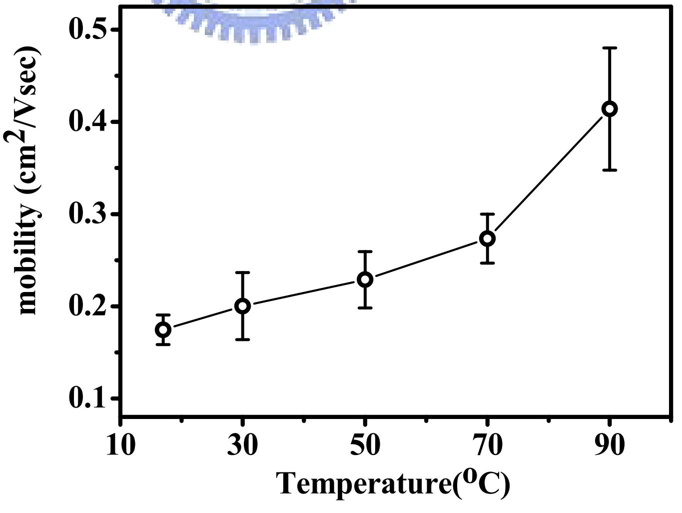


Figure 4. 3 The results of the mobility calculation from the saturation regime of the modeling of field-effect transistor. Circle: the average obtained from the maximum tangent in the plot of $\sqrt{|I_D|}$ versus V_G.

The relationship of the hole mobility to deposition temperature is revealed in Figure 4. 3. For the device without surface treatment, the average mobility goes up from 0.17 to 0.41 $cm^2/Vsec$ by deposition temperature elevated. It demonstrates that the higher the temperature is, the better the device performance becomes.

However, the corresponding transfer characteristics of the OTFTs as shown in Figure 4. 2 present a threshold voltage (V_T) shift which moves toward a more positive bias with the higher deposition temperature. The early turn on at higher temperature may result from the higher trap density [25] or more dipoles in the insulator/pentacene interface.

In addition, the slop of the ($\sqrt{}$-I_D) plots in Figure 4. 2 exhibits two gradations at higher temperature seriously: a slow slope nearby the turn on point while a steep one away from it. It is well known that the mobility in some OTFTs is gate bias dependent. Strictly speaking, it is more relative to the (V_G-V_T). If we extract each mobility from the secant to obtain the average value, the device prepared at 90℃ will not perform outstandingly as before. Hence, the mobility estimated from the FET model might be overestimated for the device fabricated at high temperature.

<u>Part C: Crystal Structure</u>

4.2-4 The Phase Transition

Figure 4. 4 illustrates the XRD spectra of pentacene structures on various conditions. There are two sets of diffraction peaks in the spectra: *(00l’*) is for 2θ of a multiple of 5.7 degrees, and *(00l*) is for a multiple of 6.2 degrees.

By Bragg’s law: $2d\sin\theta = n\lambda$, the set, *(00l’)*, is determined with vertical periodicity of 15.4Å, while the other set, *(00l)*, reveals the d-spacing of 14.4Å. The set of *(00l’)* has been identified as “thin-film phase”, and (*00l*) is so-called “bulk phase.”

[6] [25]

In terms of the full widths at half maximum, the films deposited through substrate heating show slightly higher crystalline quality than the ones deposited at RT. We ascribe the formation of higher order to annealing during pentacene deposition. However, as indicated by the rectangle of Figure 4. 4 not only thin-film phase but also bulk phase grows with deposition temperature. Growth of both phases might bring about incoherence between phase boundaries.

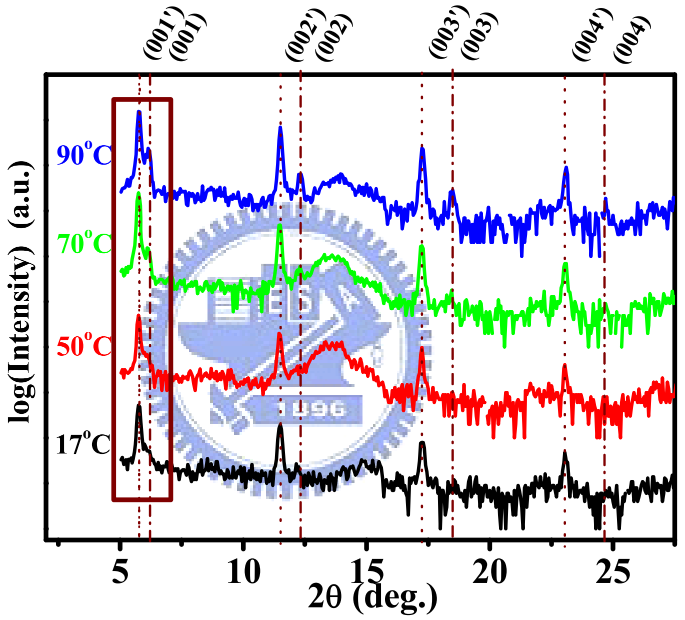


Figure 4. 4 X-ray diffractograms using CuKα (λ=1.54 Å). The samples were prepared by the pentacene deposited at a fixed flux rate of 0.5Å/sec on a 200-nm-thick SiO_2 substrate at various deposition temperatures.

Note that the fatty peak at 2θ of 13.5 degrees belongs to SiO_2, not to pentacene.

4.2-5 Conclusion

In summary, we have prepared pentacene-based TFTs, which were deposited on SiO_2 gate dielectrics at various substrate temperatures. The AFM images show that average grain size enlarges as the substrate temperature increases. It is supposed that more grain boundaries could hamper carrier transport.

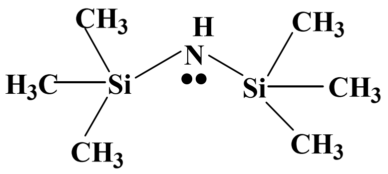
However, the XRD spectra indicate that an incoherence between two phases occurs in spite of the high order growth in thin film phase. Even if we only utilize substrate heating to enlarge grains, other factors would disturb this effect. Too many variables would make the analysis less powerful.

Furthermore, the V_T shift is a thorny problem in mobility estimation especially. The outcome, the better performance due to the higher deposition temperature, seems to jump to a conclusion.

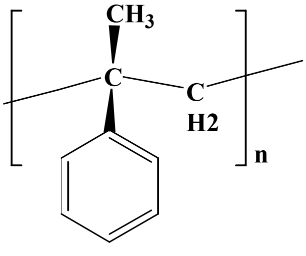
In order to make sense of the XRD spectra and to reduce the V_T shift, it is necessary to inhibit the phase transition and trap density at higher temperature. There is a possible method to come to this objective: to modify the substrates [26]. It might relax the strain of phase transition and simultaneously alter the interfacial states.

In the following sections, we have tried two types of surface treatments: 1,1,1,3,3,3- **h**exa**m**ethyl**d**i**s**ilazane [27] and **p**oly(**α**- **m**ethyl**s**tyrene) [28]. We attempt to find out the relationship of electrical properties to grains without disturbance such as V_T shift and phase transition.

HMDS



PαMS



4.3 The Relationship of the Mobility to the Grains

4.3-1 The Transfer Characteristics without V_T Shift

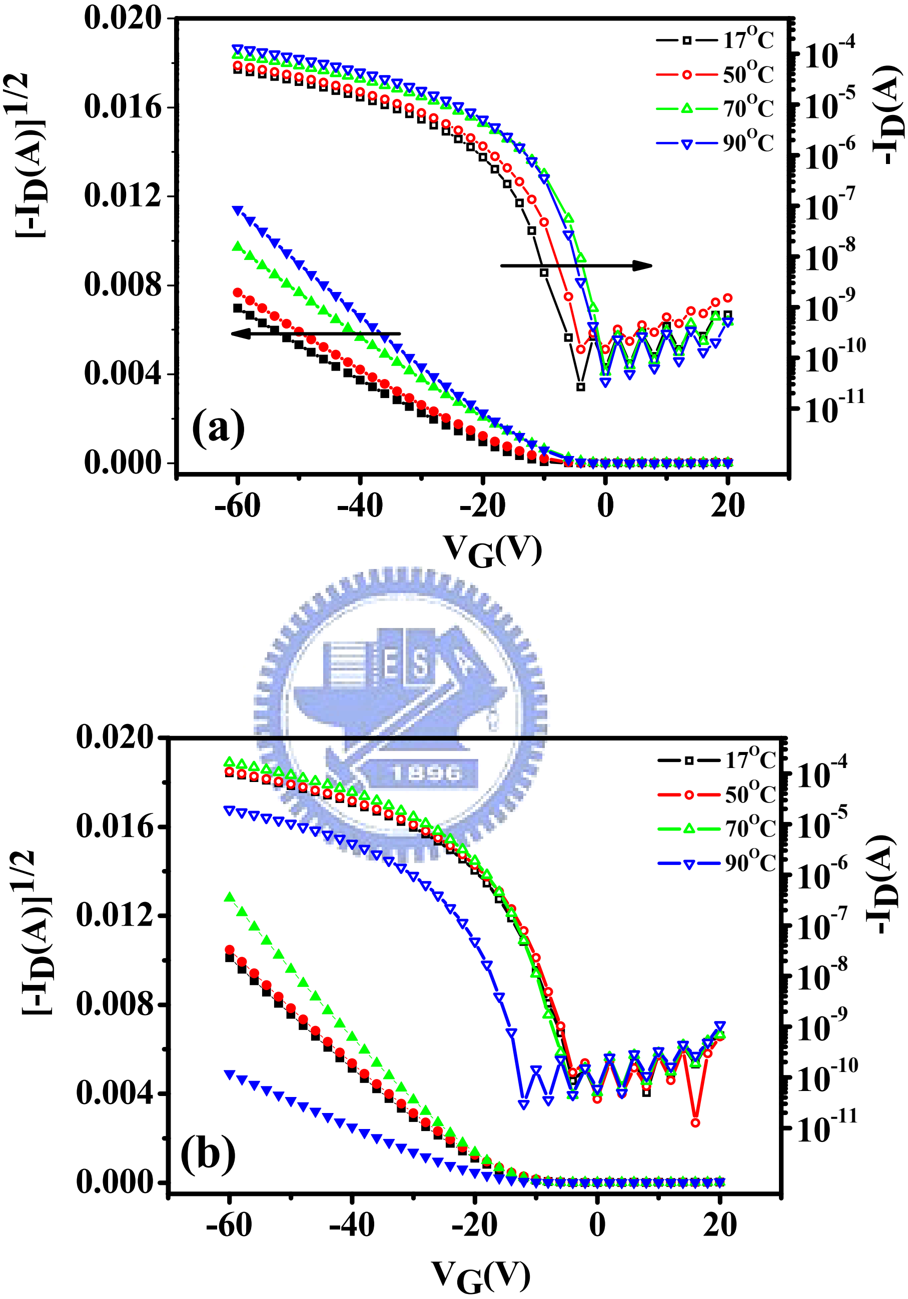


Figure 4. 5 The transfer characteristics of the OTFTs, which were fabricated at various deposition temperatures with (a) HMDS-treated substrate, (b) PαMS-treated substrate, obtained under V_D=-60V.

Compared with Figure 4. 2, Figure 4. 5 illustrates that the V_T shift is not clear, and the devices turn on at negative bias, not at positive bias as before. The V_T shift as shown in Figure 4. 5 is less than 10V, which would solve a basal problem in estimating mobility. It is a good beginning to study the relationship of mobility to grains in the next sections.

But, why the surface treatments work?

It is notice that the contact angle of bare substrates drops dramatically with decreasing temperature. In contrast, however, the contact angles of the two treated substrates are nearly identical. This is likely the reason that V_T shift could be wiped off by surface treatments.

Note that the turn on voltage of PαMS-treated devices center on -5V except for the one prepared at 90℃. It has turned on at a more negative bias than the others. This obvious shift might be due to the glass transition of PαMS, which should be regarded as another modified material.

On the other hand, the devices with surface treatments have turned on at negative bias, whereas the bare ones have actuated at positive bias. This part will be discussed in the section 4.5.

Surface Treatment	**Substrate Temperature (^oC)**	**Contact Angle (H_2O)**
Bare	**20**	**49.8**
	90	**60.0**
HMDS	**20**	**67.5**
	90	**67.0**
PαMS	**20**	**84.0**
	80	**82.8**

Table 4. 1 Contact angles measured on 3 kinds of substrates at various temperatures.

4.3-2 Inhibition of Phase Transition

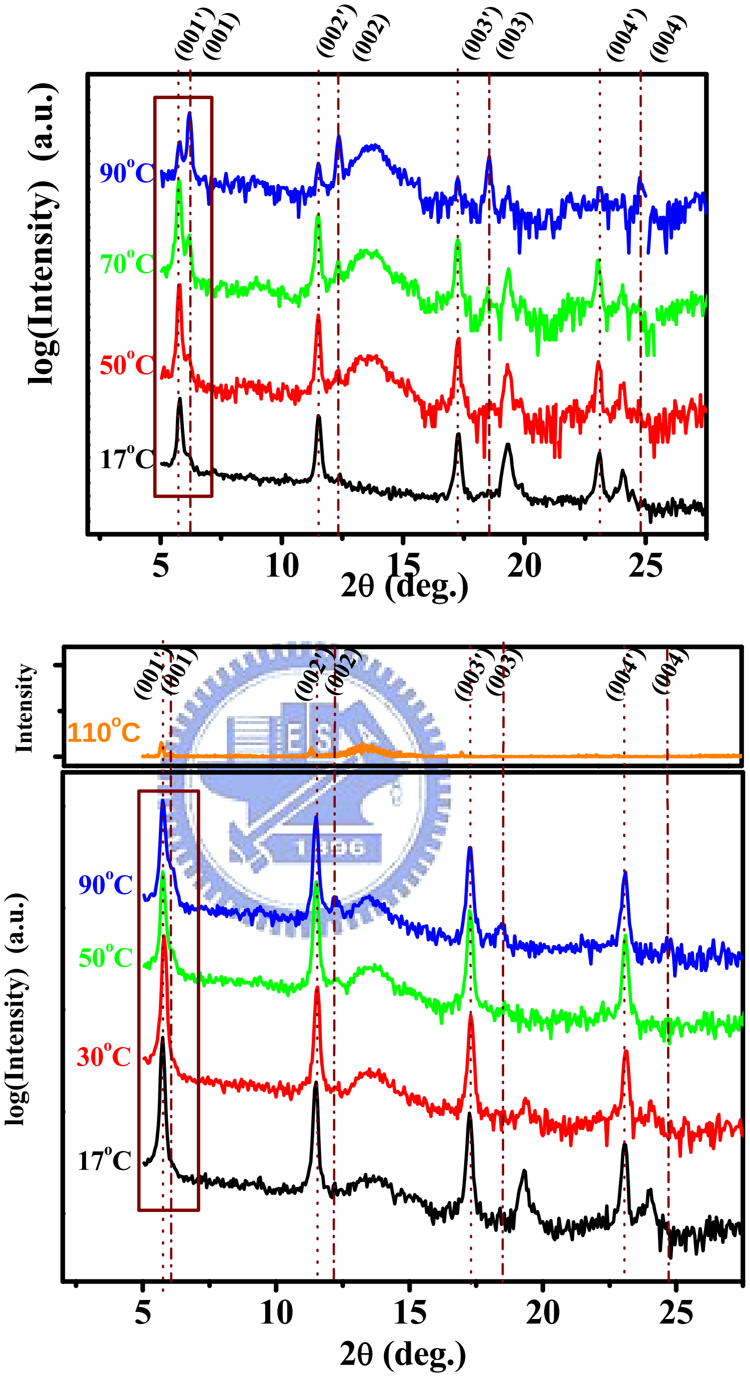


Figure 4. 6 XRD spectra of 60-nm-thick pentacene deposited at a fixed flux rate of 0.5Å/sec on a (top) HMDS-treated substrate, (bottom) PαMS-treated substrate at various deposition temperatures.

Coherence of Phases

As indicated by the rectangle of Figure 4. 6, the crystal progressively evolves into bulk phase *(00l)* on the HMDS-treated substrates, whereas it maintains thin-film phase *(00l')* with the higher substrate temperature on PαMS-treated substrates. It is believed that the phase evolution is related to the strain relaxation of initially strained thin-film phase. This figure proves that the phase transition has been repressed by the PαMS treatment, probably due to the strain release by polymer chains.

Molecular Orientation

In the XRD patterns, the pentacene crystal on the treated substrates demonstrates a strong Bragg reflection at 19.2°, which is absent in the case of bare substrates. This peak is estimated to be an unresolved doublet arising from (110) and (111) reflections with a d-spacing of ~2.5Å [29]. The appearance of (110) and (111) reflections infer that it exists flat-lying molecules on the substrate surface which is likely to make better adhesion between inorganic/organic interface.

Additionally, the flat-lying molecules should make the Ehrlich-Schwoebel barrier lower. If the molecules deposit without E-S effect, the film growth is close to layer-by-layer mechanism.

Intensity

For the HMDS-treated patterns, the intensity becomes stronger with increasing temperature, which is similar to the untreated ones. For the PαMS-treated patterns, however, it is an opposite case. The film deposited at RT shows better reflections than the ones deposited through substrate heating.

4.3-3 Morphology Evolution

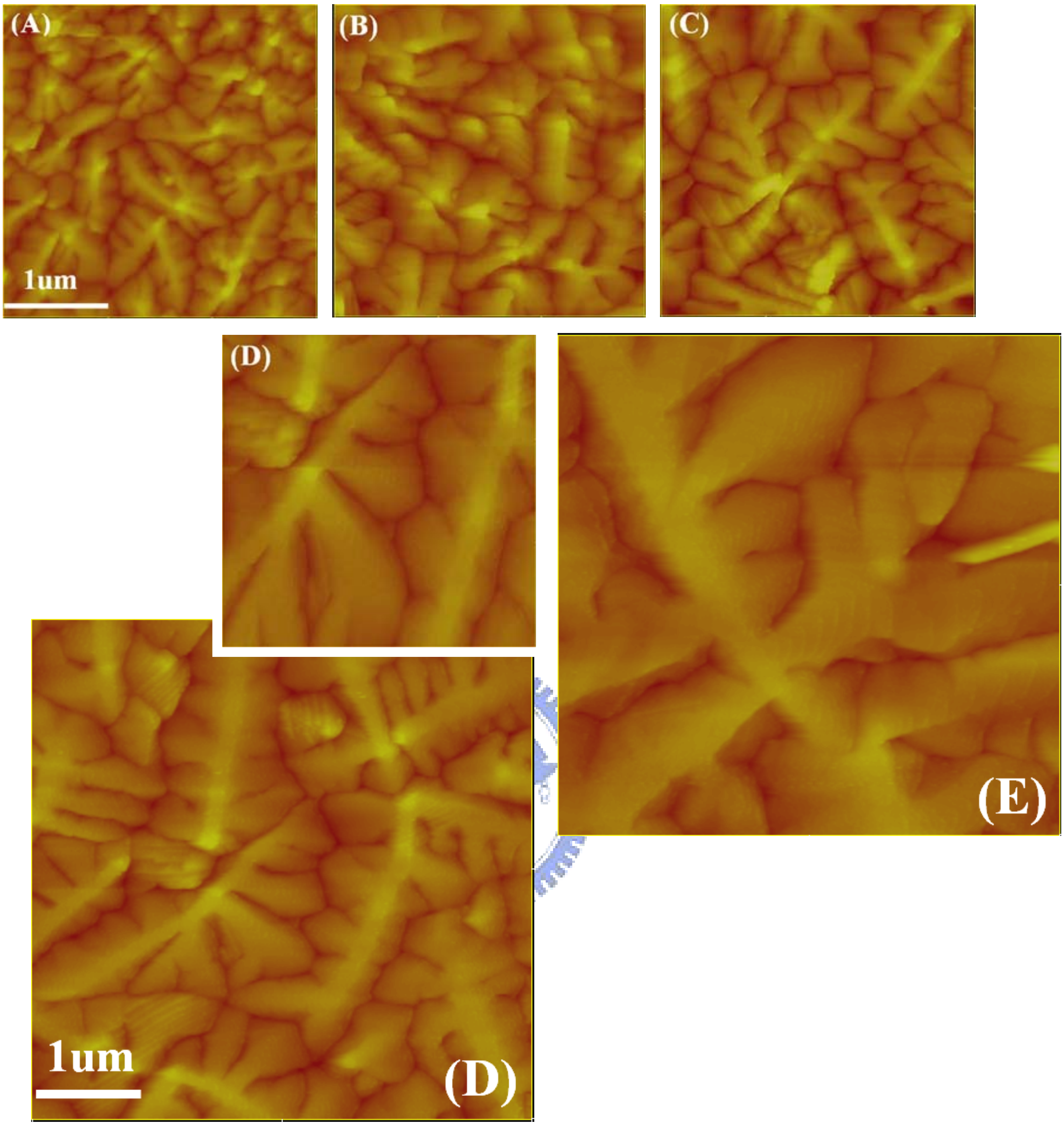


Figure 4. 7 AFM images of 60-nm-thick pentacene deposited at a fixed flux rate =0.5Å/sec on a 200-nm-thick SiO_2 substrate with HMDS treatment at various deposition temperature.

(A)T =17℃, R=10.672nm. (B) T =30℃, R=9.630nm (C) T =50℃, R=12.496nm.
(D) T =70℃, R=9.325nm. (E)T =90℃, R=8.788nm.

All the images are $3\times3\mu m^2$ except the gray (bigger) two which are $5\times5\mu m^2$.
(R: roughness presented by root-mean-square form)

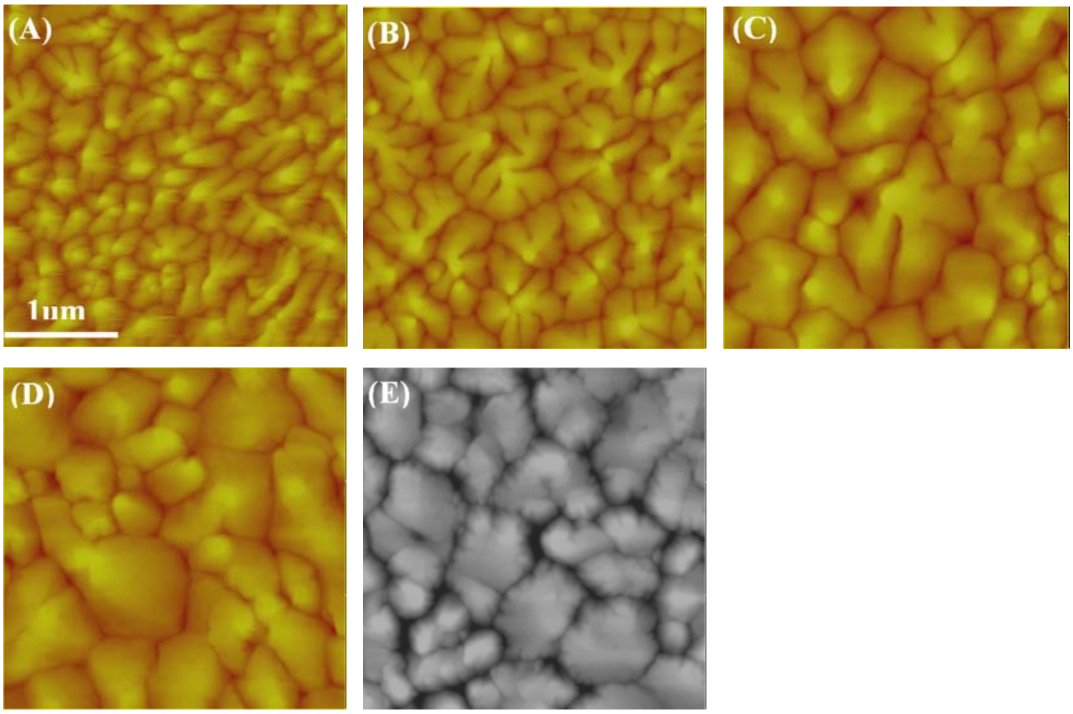


Figure 4. 8 AFM images of 60-nm-thick pentacene deposited at a fixed flux rate =0.5Å/sec on a 200-nm-thick SiO_2 substrate with PαMS treatment at various deposition temperature.

(A)T =17℃, R=9.027nm. (B) T =30℃, R=8.970nm. (C) T =50℃, R=10.102nm.
(D) T =70℃, R=9.071nm. (E) T =90℃, R=10.211nm.

Evolution of Grain Size

Figure 4. 7 is the first group of AFM images of 60-nm-thick pentacene with HMDS-treated substrates, while Figure 4. 8 is the second group with PαMS-treated ones. Similar to bare substrates, HMDS-treated samples also display an obvious enlargement with deposition temperature. But for the PαMS-treated samples, the grain sizes grow in the beginning, slow down at 70℃, and finally become smaller at 90℃. It also shows a pronounced morphological difference in grain gaps between Figure 4. 8(E) and the others.

In common cases, higher substrate temperature favors pentacene to diffuse on the surface and to nucleate on fewer sites. But, a large grain should be formed by lower rate of nucleation and higher rate of lateral growth. The glass transition temperature (Tg) at atmosphere of our PαMS is 85℃, but it should be lower than 85℃ under high vacuum. Above the Tg point, molecule chains could obtain more energy which would raise the nucleus number, and diminish grain size. Accordingly, this morphological difference probably results from the violent molecular motion of PαMS at 90℃.

Evolution of Grain Shape

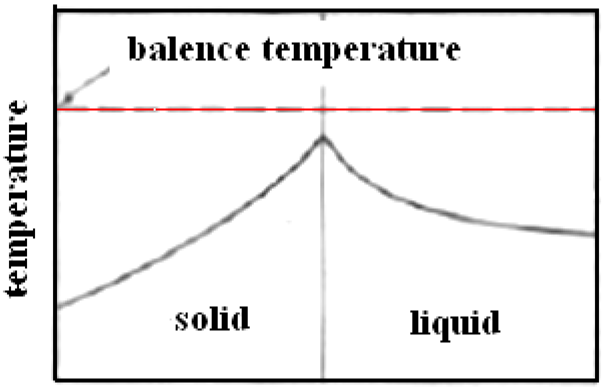
Apart from the grain size, it is noticeable that the dendrite-shaped grains disappear at the medium temperature on the PαMS-treated substrates. It also disappears at the high temperature on the bare substrates. The dendrites are independent of the crystal phase, but dependent on deposition temperature.

The model of Diffusion-Limited Aggregation (DLA) is widely used to explain the growth of dendrites [30]. DLA is the process whereby particles undergo a random walk (Brownian motion) to push the molecules approach the growing clusters. Once the molecules stick to the cluster, the transient diffusion at the step edges occurs immediately.

From the law of heat conduction (Fourier's law),

$$\bar{q} = -\bar{\bar{k}}\nabla T \; ,$$

the direction of heat flow depends on the temperature gradient at the interface. When the films grow into a supercooled liquid, the interface is unstable. Suppose a small protrusion forms at the interface, the negative temperature gradient in the liquid becomes more negative. Therefore, heat is removed more effectively from the protrusion than from the surrounding regions. That will allow the arms to grow preferentially, and hinder the neighboring arms from forming [19] [31].



Review 4.1 The temperature distribution for the dendrite growth. [From Chalmers, B., trans. AIME, 200 519 (1954)] [19]

To return to our system, when the pentacene molecules freeze, the latent heat will be released at the vapor/solid interface. If the latent heat is not removed immediately, it will result in the temperature distribution such as Review 4.1. The dendrites are controlled by the rate at which the latent heat can be removed from the vapor/solid interface, and if the vapor temperature reach a critical supercooling. That is why the dendrites disappear at the relatively high deposition temperature, which is influenced by the thermal property of substrates simultaneously.

Evolution of Initial Layers

While the TFT turns on, the carriers concentrate in the initial several layers to form the channel [27] [32]. From the Figure 4. 7 and Figure 4. 8, surface treatment seems to affect the morphology even with a thickness far beyond the first monolayer. Thus, the underlying morphology might deviate a lot from the appearance. It is more significant to see the 8nm-thick (~5ML) pentacene films rather than 60nm-thick ones.

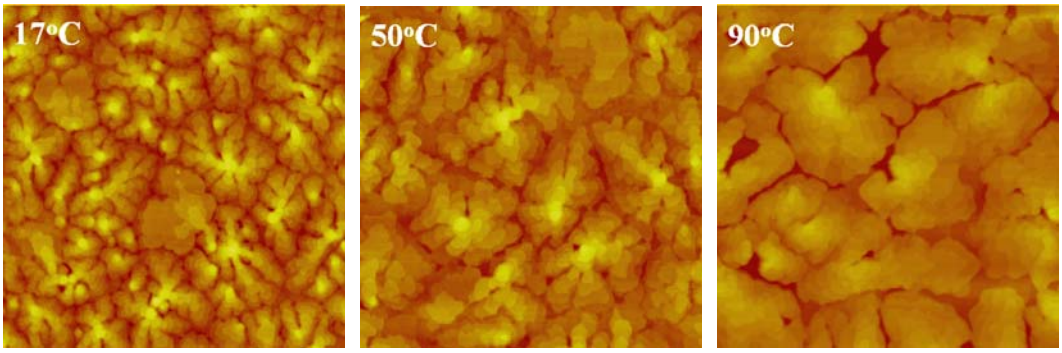


Figure 4. 9 AFM images of 8-nm-thick pentacene deposited on a 200-nm-thick SiO_2 substrate without surface treatment. All the images are 3×3μm^2.

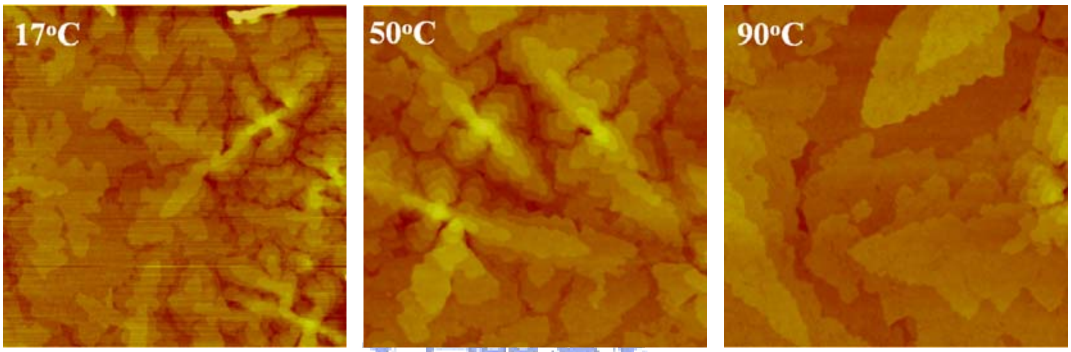


Figure 4. 10 AFM images of 8-nm-thick pentacene deposited on a 200-nm-thick SiO_2 substrate with HMDS treatment. All the images are 3×3μm^2.

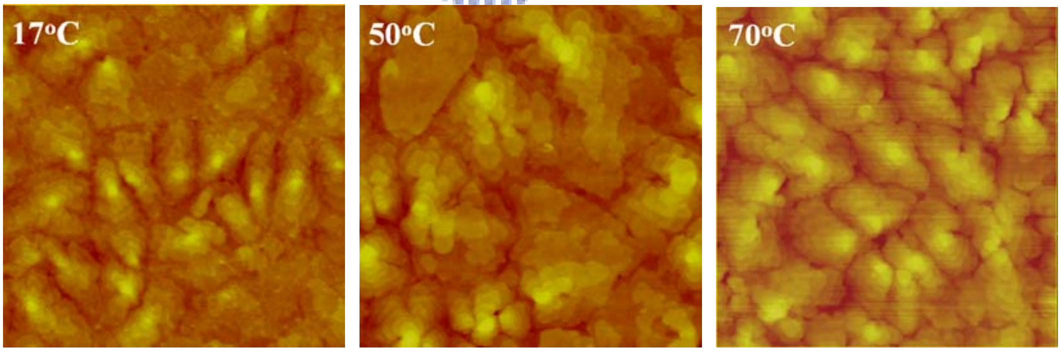


Figure 4. 11 AFM images of 8-nm-thick pentacene deposited on a 200-nm-thick SiO_2 substrate with PαMS treatment. All the images are 3×3μm^2.

Compare Figure 4. 9 with Figure 4. 1, we will see the evolution of underlying grains deposited on the bare substrate is analogous to the case of outlying ones. New layers nucleate on the already existing DLA-like monolayer before the latter coalesce to a complete epitaxial layer. It is reported that the quasi-epitaxial growth of pentacene molecules is disrupted by the upward diffusion bias generated by the Ehrlich-Schwoebel barrier, leading to mound growth [20].

If the Ehrlich-Schwoebel barrier cannot be neglected, there will be an adatom "uphill current." Furthermore, as the uncovered areas are much smaller than the islands, shadowing effect will pronounce. They will cause fast upward growth, bringing deep crevices observed, not blurred boundary.

For the PαMS-treated substrates in contrast, it does not agree with the above finding. Unlike Figure 4. 8, the grain boundary is too blurred to recognize how many grains is (Figure 4. 11). It is divergent from the 60-nm-thick appearance.

But why the E-S barrier seems to be trivial in the PαMS-treated system?

The effect of the Ehrlich-Schwoebel barrier might be either strengthened or mitigated by the deposition temperature [20], and surface treatments. By elevating temperature during deposition, the molecules will get more energy so that their probability of jumping down a step edge would be promoted. On the other hand, surface treatments can make the molecules "lie down," which might change the Ehrlich-Schwoebel barrier. These two factors might help the grains to form layer-by-layer structure. But which one is dominant needs advanced study.

According to both patterns of XRD (Figure 4. 6), the flat-lying pentacene occurs at RT. Moreover, the more blurred boundary, exhibiting lower Ehrlich-Schwoebel barrier of the film, is also shown at low temperature (Figure 4. 11). Consequently, it is deduced that the E-S barrier of the film with flat-lying pentacene is lower than that with oblique-standing one. The film growing on the treated substrate is probably near to the layer-by-layer mechanism, which fills in the deep crevices. To reduce the boundary barrier, layer-by-layer growth is better than the mound growth.

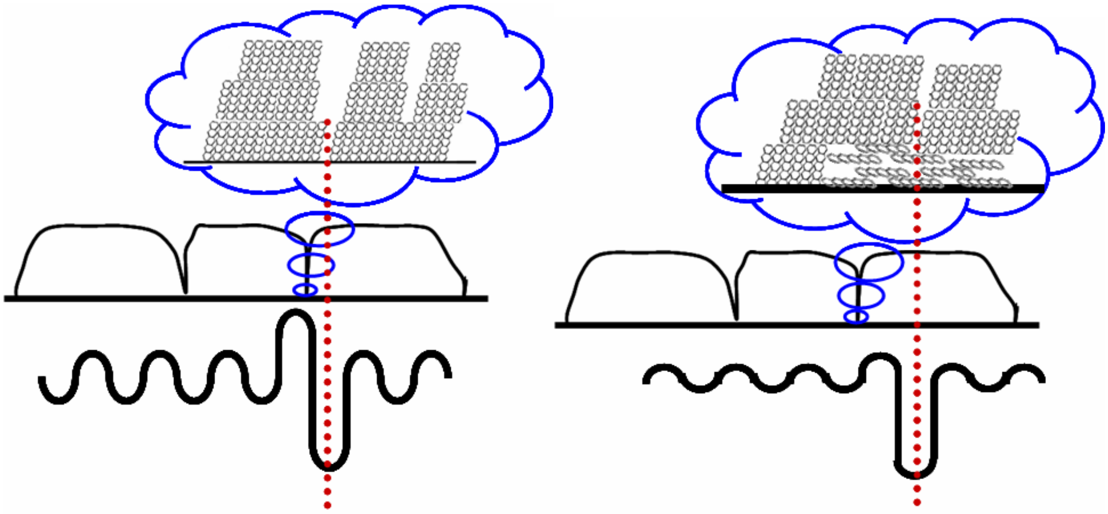


Figure 4. 12 Schematic view of the structure of deposited pentacene on (Left) bare oxide substrates with strong effect of Ehrlich-Schwoebel barrier, exhibiting deep crevices, (Right) surface modified substrates, showing unclear boundaries.

4.3-4 The Comparison of Mobility

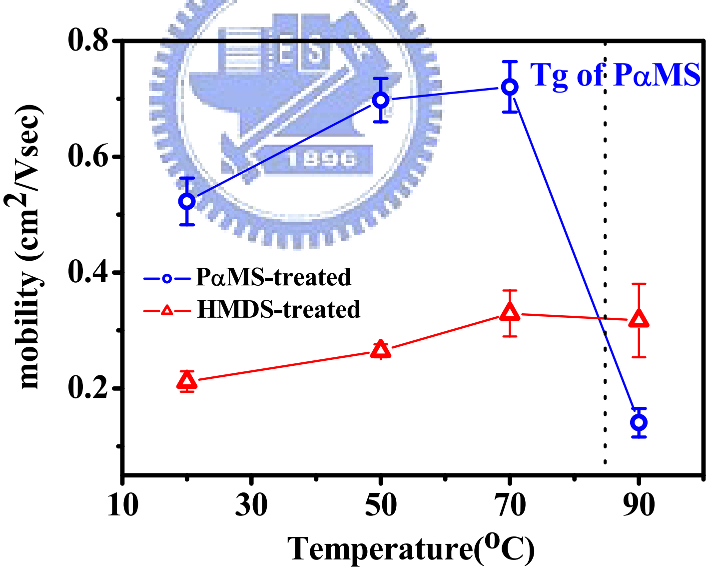


Figure 4. 13 The results of the mobility calculation from the “**saturation regime”** of the modeling of field-effect transistor.

The result of mobility calculation (Figure 4. 13) presents the relationship between the mobility and substrate temperature. For the HMDS-treated devices, the mobility improves with increasing temperature from 0.21 to 0.33 cm^2/Vsec, but reaches a saturation performance at 90℃. In contrast, the mobility of the PαMS-treated device at 70℃ can be as high as 0.72 cm^2/Vsec, which is much better than that of untreated or HMDS-treated ones, while it drops to 0.1cm^2/Vsec at 90℃. It is believed that the grain and interfacial boundary may reduce the carrier mobility. Therefore, the higher substrate temperature, resulting in the larger grains, makes better performance.

However, for the two treated devices, the highest mobility occurs while the grain size is intermediate (at 70℃). Large grains, which mean less density of grain boundary, will not help the charge transport. It is suspected that more traps maybe induced at higher substrate temperature [25]. In our system, boundary traps or bulk boundary may result from the phase transition of HMDS, while interfacial traps may cause from the rubbery state of PαMS. Additionally, Figure 4. 8(E) displays deeper grain gaps which may bring high density of grain boundary. These two negative factors hold the mobility of PαMS-treated device back.

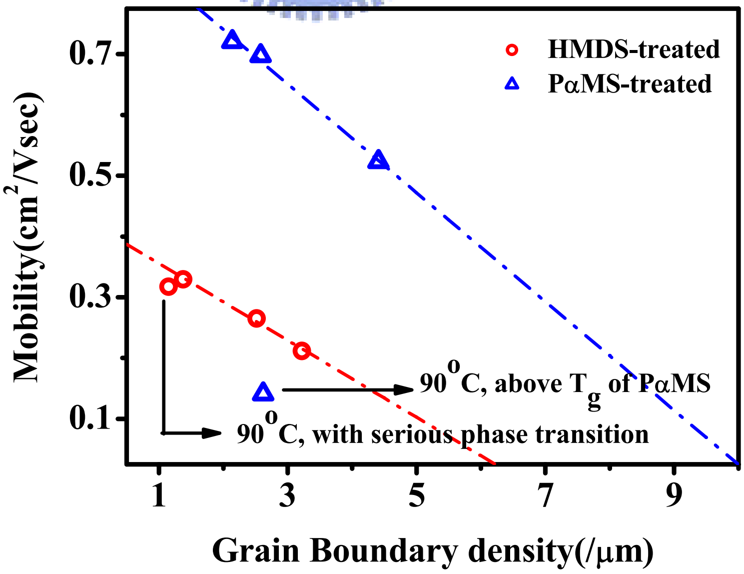


Figure 4. 14 The relationship of mobility to grain boundary density.
The AFM images of 60nm-thick films mentioned in 4.3-4 were dealt by the program1 appendixed at the final of this thesis.

People have already known that the aversion of grain boundaries to the transport properties. Except for the serious phase transition of HMDS-treated device, and the rubber state of PαMS-treated device, the mobility is proportional to the grain boundary density.

Externally, the transport path of PαMS-treated device can bear to meet 10 boundaries per μm, while the case of PαMS-treated one can only bear 6 per μm. It is probably due to the blurred boundary in the initial layer, resulting in the particular better performance.

4.4 Channel and Contact Resistance

In the previous section, OTFTs with different grain sizes were fabricate by controlling the substrate temperature to investigate the relationship between the grain size (boundary) and the carrier mobility.

In this section, we will analyze the electrical characteristics by the transfer line method to extract the minimum effective contact resistance, bulk resistance, and channel resistance, respectively. Thus, we will have more insight into the real situation that how the mobility improves by varying deposition temperature in these three parts.

4.4-1 Transfer Line Method [33] [34]

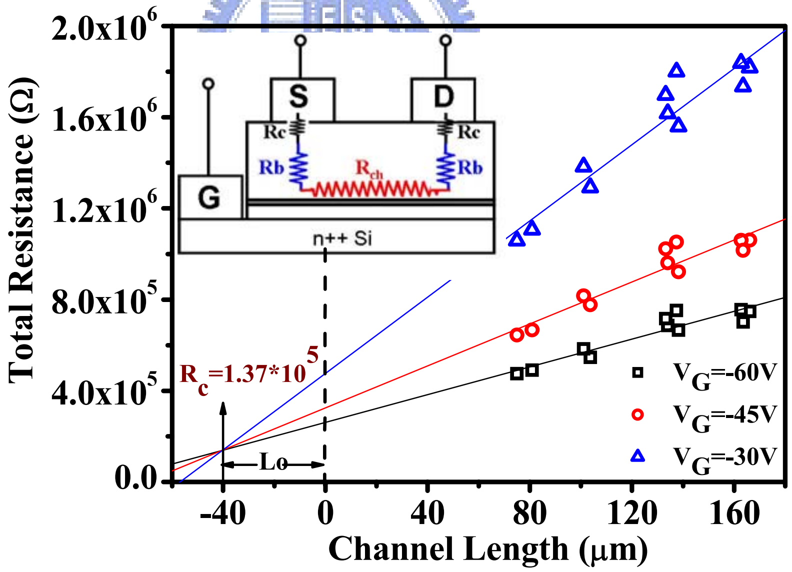


Figure 4. 15 Total resistance as a function of channel length at various gate voltages. The inset shows a simplified equivalent OTFT circuit where the conducting path is divided into three parts of resistance, $(R_c^S + R_c^D)$, $(R_b^S + R_b^D)$, R_{ch}.

Figure 4. 15 presents the transfer line method for resistance extraction. In the linear regime, the total resistance (R_{total}) can be expressed as:

$$R_{total} = \left.\frac{\partial V_D}{\partial I_D}\right|_{V_D \to 0}^{V_G} = R_{ch} + R_p = \frac{L}{W\mu C_i(V_G - V_{th})} + R_p$$

where $R_p = R_C^S + R_C^D + R_b^S + R_b^D$. The channel resistance per μm can be extracted by the slope. On the other hand, the parasitic resistance (R_p) can be extracted by the y-axis intercept of the extrapolated linear fit of R_{total} versus L at various gate voltages. All fitted lines meet at an intersection point which is the minimum effective contact resistance (R_c^S+ R_c^D) at x=-L_0. Consequently, the bulk resistance (R_b^S+ R_b^D) can be obtained by the difference between R_p and (R_c^S+ R_c^D).

4.4-2 The Resistance Extraction from HMDS-Treated Device

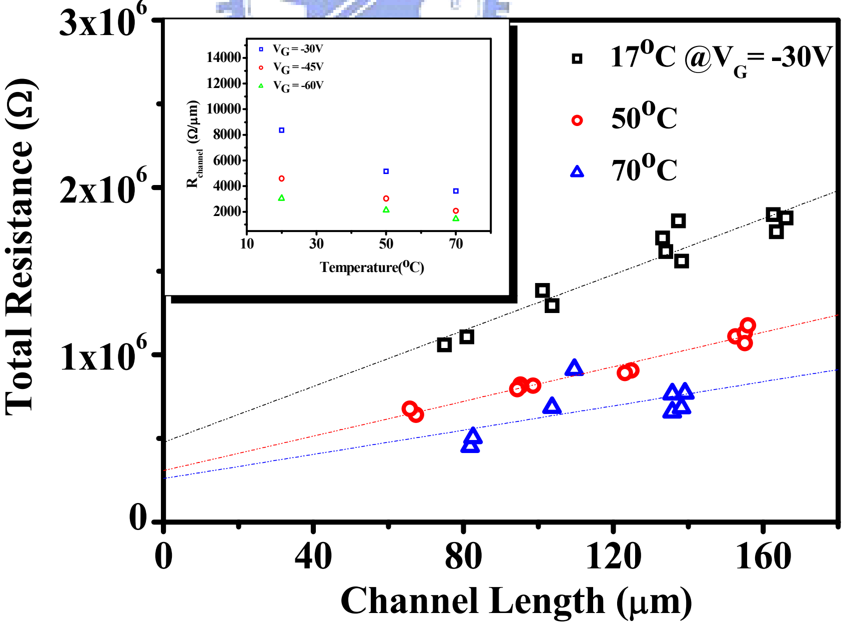


Figure 4. 16 Total resistance as a function of channel length at various deposition temperatures which are extracted from the electrical characteristics of HMDS-treated device.

Channel Resistance

From the change of the slope, it is inferred that the channel resistance per μm reduces with increasing deposition temperature (Figure 4. 16). From the AFM images (Figure 4. 17), less grain boundary density for the device made at higher temperature was observed. Therefore, with the larger the grains, the channel resistance is lower.

Table 4. 2 The parameters of HMDS-treated device obtained under V_G=-30V.

Substrate Temperature (°C)	Mobility (cm^2/Vs)	Contact Resistance (kΩ)	Bulk Resistance (kΩ)	Channel Resistance (kΩ/μm)	Lo/L* (μm)	Area Ratio Surface/substrate	Contact Angle** (H_2O)
20	**0.16**	**137**	**339**	**8.4**	**40/90**	**2.4**	**80.6**
50	**0.21**	**54**	**254**	**5.2**	**49/90**	**2.3**	**82.6**
70	**0.27**	**22**	**239**	**3.6**	**67/90**	**1.7**	**83.8**

*The value of Lo/L exhibits the ratio of bulk resistance to channel resistance (90 μm).

**Assume Cassie model is proper to apply in the pentacene surface [35].

Parasitic Resistance

From the y-axis intercept, it is also found that the parasitic resistance reduces with increasing deposition temperature, too. It is quite interesting to see the origins of the grain size effects on the R_p. From the method described above, we can separate the parasitic resistance into two parts, minimum effective contact resistance ($R_c^S + R_c^D$) and bulk resistance ($R_b^S + R_b^D$) as shown in Table 4. 2. The results are described as the following sections.

Minimum Effective Contact Resistance

Table 4. 2 shows that the contact resistance (R_C^S+R_C^D) reduced with temperature. Assuming the resistance is inverse-proportional to the surface area, the contact surface should be confirmed. Since the surface area cannot deduced directly from the grain

size, Matlab (Program2 in the appendix) was used to calculate the surface area from the AFM images. The result indicates that the contact surface area of the device made at 20^{o}C is about two-fold of that made at 70^{o}C, suggesting a higher specific contact resistance for the device made at 20^{o}C. Further, from the measurement of contact angle, different values were obtained for different devices (Table 4. 2). Therefore, it is inferred that the molecular orientation of the deposited pentacene respective to the surface maybe different, resulting in different hole injection efficiency, and therefore, different specific contact resistance.

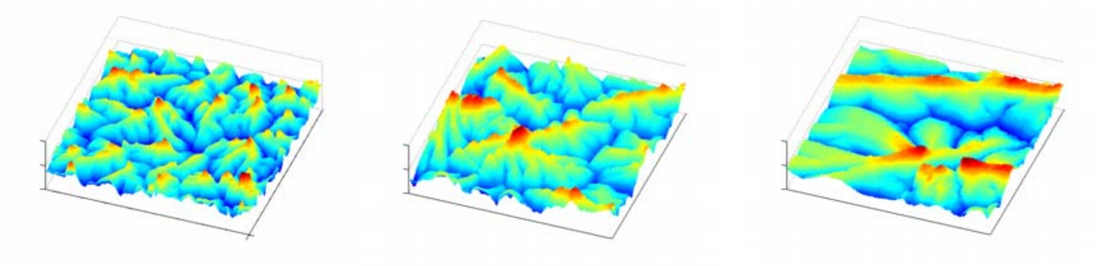

(A) (B) (C)

Figure 4. 17 AFM images of 60-nm-thick pentacene deposited on HMDS-treated SiO_2 substrates at various temperatures. (A) T=20℃, (B)T=50℃, (C) T=70℃.

In fact, it is similar to the 8-nm-thick samples in this case.

Bulk Resistance

From Table 4. 2, it is noted that the bulk resistance ($R_b^S+R_b^D$) is in fact larger than contact resistance. By the value of L_0/L, it means the bulk resistance plays an important role for devices made at higher temperature especially. Moreover, the thickness of pentacene is less than the channel length, but the ($R_b^S+R_b^D$) is comparable to the R_{ch}. It reveals that how to improve the bulk resistance is an issue.

Note that the deposition temperature can reduce the resistance in lateral direction of the thin-film, but have less effect in the vertical direction. The details will discuss in the 4.4-4.

4.4-3 The Resistance Extraction from PαMS-Treated Device

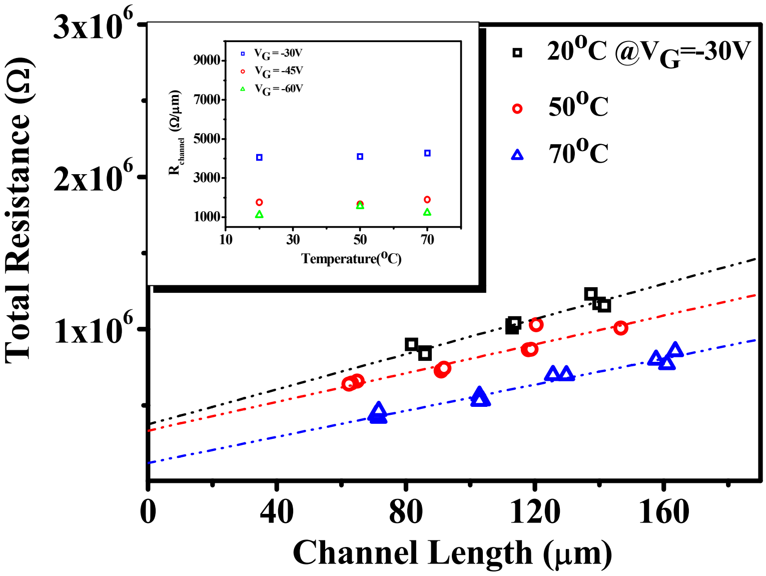


Figure 4. 18 Total resistance as a function of channel length at various deposition temperatures which are extracted from the electrical characteristics of PαMS-treated device.

Table 4. 3 The electrical parameters of PαMS-treated device obtained under V_G=-30V.

Substrate Temperature (°C)	**Mobility (cm^2/Vs)**	**Contact Resistance (kΩ)**	**Bulk Resistance (kΩ)**	**Channel Resistance (kΩ/μm)**	**Grain Boundary (/μm)**	**Area Ratio Surface/substrate**	**Contact Angle (H_2O)**
20	**0.41**	**200**	**175**	**5.8**	**4.4**	**3.0**	**81.2**
50	**0.50**	**54**	**73**	**4.7**	**2.6**	**2.4**	**83.7**
70	**0.58**	**33**	**40**	**4.3**	**2.1**	**2.1**	**83.7**

Channel Resistance

From Table 4. 3, it is also inferred that the channel resistance per μm depends on the deposition temperature slightly. It is probably due to the larger grain size of the pentacene and therefore, less grain boundary in the channel. However, compared to HMDS-treated device, it is less sensitive to deposition temperature (Figure 4. 16 and

Figure 4. 18).

It should be careful to use the morphology of initial layers rather than the upper layers. From the AFM images (Figure 4. 11), it shows the more blurred boundaries. Hence, there is no obvious grain boundary to make the channel resistance to change a lot.

Minimum Effective Contact Resistance

Table 4. 3 shows that the contact resistance ($R_C^S+R_C^D$) reduced with contact area, corresponding to the grain boundary. From the measurement of contact angle, it is indicated that the contact area is relative to a certain surface property. To employ the deduction in the previous section, the difference of contact surface result in different specific contact resistance, i.e. hole injection efficiency. It suggests that larger contact area, which means that new area perpendicular to the substrate is produced, is unfavorable for hole injection.

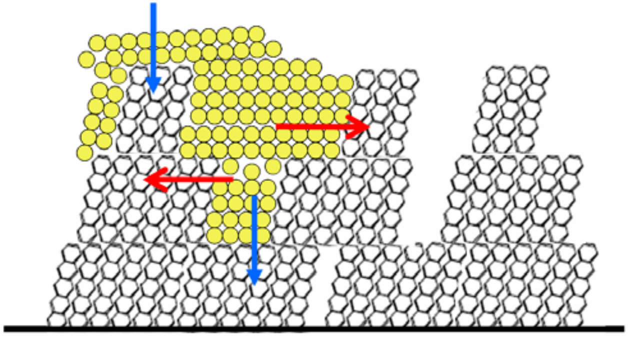


Figure 4. 19 Depiction of the two possible direction of hole injection from gold to pentacene. Yellow balls exhibit Au electrodes.

Bulk Resistance

Based on Table 4. 3, the bulk resistance ($R_b^S+R_b^D$) is close to the contact resistance ($R_C^S+R_C^D$). Note that the deposition temperature not only reduces the resistance in horizontal direction of the thin-film, but also has a little effect in the vertical direction.

In this system, the effect of Ehrlich-Schwoebel barrier is more complex: the barrier height competes against the thermal energy. At low temperature, flat-lying pentacene decreases E-S barrier, and the molecules get less energy. On the contrary, at high temperature, oblique-standing pentacene increases E-S barrier, but the molecules get more energy. Which one is more dominant should be studied.

4.4-4 Paracrystal Theory to Study the Bulk Resistance

For the films with PαMS treatment, it is uncommon to see that the intensity of XRD patterns is weaker with elevating temperature even though the bulk phase is inhibited (bottom of Figure 4. 6). In order to study how the crystalline quality in the vertical direction relates to the bulk resistance, paracrystal theory is employed.

Paracrystal Theory[24]

Crystalline quality, reflecting on the breadth of peak, is characterized by the crystallite size, and the lattice distortions of second kind. Paracrystal theory permits the separation of crystallite-size and lattice-distortion broadening provided at least two resolved reflections from a given set of planes.

$$(\delta s)^2 = (\delta s)_c^2 + (\delta s)_{II}^2 = \frac{1}{\overline{L}_{hkl}^2} + \frac{\pi^4 g_{II}^4 m^4}{\overline{d}_{hkl}^2} \quad ,$$

where $\delta s = \dfrac{2\cos\theta\delta\theta}{\lambda}$, is the total broadening excluding instrumental broadening, λ is 1.54Å for X-ray wavelength of CuKα, $\delta\theta$ is expressed in radians, $(\delta s)_c$ is the broadening from crystallite size, $(\delta s)_{II}$ is the broadening from lattice distortion of second kind, m is the diffraction order, $\overline{d_{hkl}}$ is the spacing of (hkl) planes. $\overline{L_{hkl}}$ and g_{II} are the unknowns, referred to mean dimension of cryastallites perpendicular to the plane (hkl), and mean distance fluctuation between successive (hkl) planes, respectively.

Regardless of the instrumental broadening, the squared breadths $(\delta s)^2$ are plotted against m^4. $\overline{L_{hkl}}$ and g_{II} would be separated with intercept of y-axis, and the slope of the least-square straight line [36]as shown in Figure 4. 20.

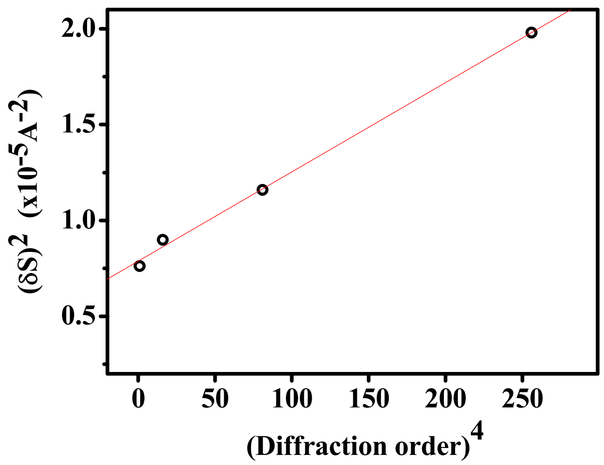


Figure 4. 20 Plot of $(\delta s)^2$ vs. the fourth power of the diffraction order.

Substrate Temperature (°C)	Bulk Resistance (kΩ)	Crystallite Size (Å)	Lattice Distortion (%)	Phase	Flat-lying Pentacene
20	**339**	**309**	**1.9**	***(0 0 l’)***	**O**
50	**254**	**342**	**1.8**	**little *(0 0 l)***	**O**
70	**239**	**289**	**2.0**	**Some *(0 0 l)***	**O**

Table 4. 4 The calculation results of parameters of crystalline quality for HMDS-treated device.

Substrate Temperature (°C)	Bulk Resistance (kΩ)	Crystallite Size (Å)	Lattice Distortion (%)	Phase	Flat-lying Pentacene
20	**175**	**356**	**1.8**	***(0 0 l’)***	**O**
50	**73**	**333**	**1.7**	***(0 0 l’)***	**X**
70	**40**	**305**	**1.1**	***(0 0 l’)***	**X**

Table 4. 5 The calculation results of parameters of crystalline quality for PαMS-treated device.

Lattice Distortion

For the HMDS-treated devices, it exhibits that the deposition temperature has less effect on the bulk resistance, corresponding to the little fluctuation of the second kind distortion (Table 4. 4). The lattice distortion does not improve with temperature, which is probably due to another phase occurs.

By the other point of view, we have already identified that flat-lying pentacene exists whatever the deposition temperature is (top of Figure 4. 6). By the effect of Ehrlich-Schwoebel barrier mentioned above, flat-lying pentacene might decrease the influence of temperature on E-S barrier. While the layer-by-layer mechanism works, the connected area is larger to decrease bulk resistance. This result also fits in with the assumption that the flat-lying pentacene can lower Ehrlich-Schwoebel barrier, and elevating temperature is not the only dominant factor anymore.

By the same token, the bulk resistance for PαMS-treated devices is decreased with elevating temperature, corresponding to the less fluctuation of the second kind distortion, too (Table 4. 5). It could be attributed to the inhibition of the second phase.

As to the effect of Ehrlich-Schwoebel barrier in the PαMS-treated system, it is more complex: the barrier height competes against the thermal energy. At low temperature, flat-lying pentacene decreases E-S barrier, and the molecules get less energy. On the contrary, at high temperature, oblique-standing pentacene increases E-S barrier, but the molecules get more energy. Hence, it is not as simple as the case in the HMDS-treated system.

The term g_{II} is about 1~2%, exhibiting that the structural perfection along the normal direction is high [36].

Crystallite Size

The minimum crystallite size perpendicular to the *(00l)* planes is estimated to be 300~400Å, which is comparable to the film thickness (~600Å). Consequently, the effect of grain boundary is neglected, but the free-surface effect should be considered.

The grain boundary near to the free surface prefers to be perpendicular to the substrate. If the grain size is comparable to the thickness, moving grain boundary away from their groove would increase the surface energy [19]. So, it is likely the reason that post-annealing always has no concern with the morphology [37].

4.5 Turn-On Voltage

4.5-1 Turn-on Voltage Shift with Surface Treatment

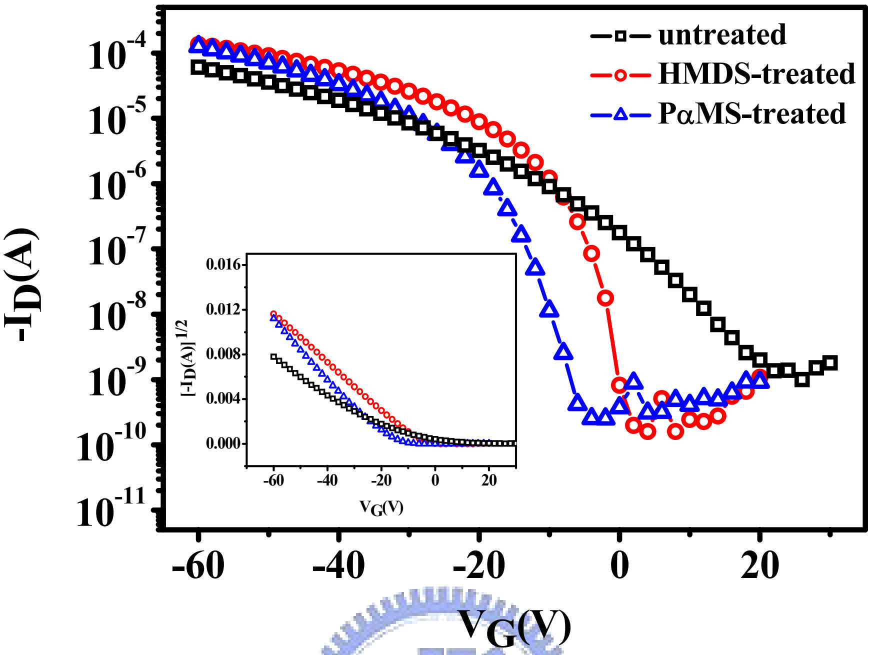


Figure 4. 21 The transfer characteristics of the OTFTs, which were fabricated at room temperature with various surface treatments, obtained under V_D=-60V.

As shown in Figure 4. 21, the untreated devices present a normally on-state, while the treated ones show a normally off-state.

People have known that the dangling bonds of the oxide surface react rapidly with atmospheric water to form Si-OH groups. Once hydroxylated, the surface will cover with a 7-Å-thin layer of water even under high vacuum [38]. If the water layer is trapped at the surface while pentacene deposited, the interface traps are more relative to the pentacene/water, rather than pentacene/SiO_2. Thus, the water layer is likely responsible for the trapping of the pentacene layer.

Hence, while the polar group is sheltered by the modified layer, it returns to an ideal situation which has to apply negative bias to accumulate holes. Although HMDS layer seems too skinny, it can change the OH-terminated oxide to a

$(CH_3)_3$-Si-terminated one [27], which has little polarity. This is why several molecular layers are as effective as a thicker polymer film to block the dipole field.

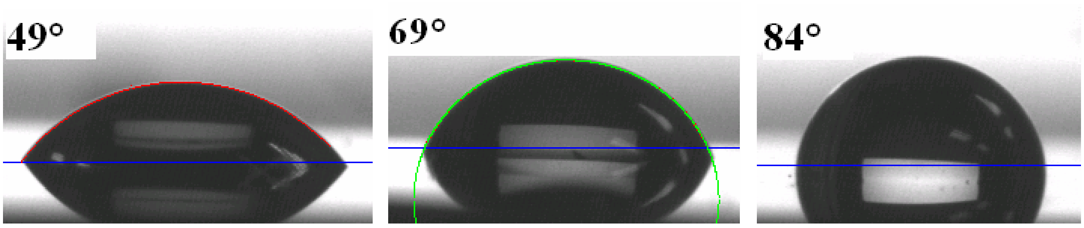


Figure 4. 22 Contact angles of DI water on SiO_2 substrates after various surface treatments. (Left) bare substrate, (Middle) HMDS-treated substrate, and (Right) PαMS-treated substrate.

As can be seen in Figure 4. 22, it shows that the contact angle becomes small with increasing polarity. While the substrates have more strong polarity, the V_T shifts toward more positive direction.

4.5-2 Sub-threshold Behavior

Schön and Batlogg have reported that the bulk trap densities of both dielectrics, Al_2O_3 and Kapton, are similar, but the subthreshold characteristics are widely divergent [11]. The difference is ascribed as traps at the semiconductor/insulator interface. The subthreshold swing [39] could be expressed by

$$S_0 = \frac{\partial V_G}{\partial(\log I_D)} = \frac{kT}{e}(\ln 10)\cdot(1+\frac{C_S}{C_i}) \text{ ....(4.5A)}$$

where C_S is the capacitance of the accumulation layer in the pentacene bulk. If there are a large number of interface traps, they will form a significant capacitance C_{it} to parallel with C_S. Using above equation and substituting (C_S+C_{it}) for C_S, we obtain

$$S = \frac{kT}{e}(\ln 10)\cdot(1+\frac{C_S+C_{it}}{C_i}) \text{ ....………(4.5B)}$$

where S is the subthreshold swing with interface traps, and the interface trap density $N_{it} = C_{it}/e$.

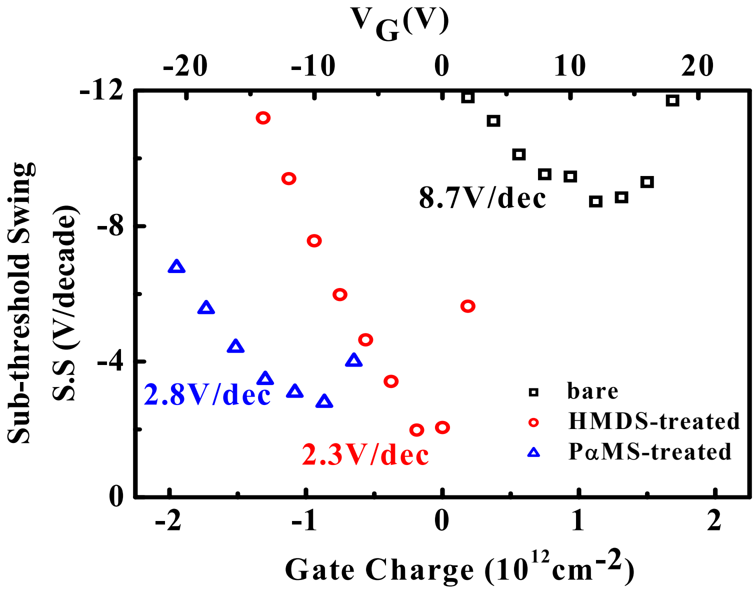


Figure 4. 23 The Subthreshold behavior of the OTFTs, applying HMDS and PαMS as modified layer, respectively. It could be derived from the transfer characteristics shown in Figure 4. 21.

We have obtained a capacitance of $1.5*10^{-8}$ F/cm^2 for the untreated and HMDS-treated SiO_2, and $1.73*10^{-8}$ F/cm^2 for the PαMS-treated one. Applying Eq.(4.5B), we have received :

Table 4. 6 The calculation results of trap density from subthreshold swing.

Substrate Treatment	Turn-on Voltage (V)	Subthreshold Swing (V/dec)	Subthreshold Swing (#/cm^{2}dec)	C_S+C_{it} (μF/cm^2)	Maximum Trap Density (#/cm^{2}V)
Bare	**+20**	**8.7**	**$8.2*10^{11}$**	**2.17**	**$13.6*10^{12}$**
HMDS	**0**	**2.3**	**$2.2*10^{11}$**	**0.56**	**$3.5*10^{12}$**
PαMS	**-5**	**2.8**	**$3.0*10^{11}$**	**0.73**	**$4.9*10^{12}$**

* Maximum trap density: density of accumulation hole + density of interface traps

Knipp et al. [4] have reported that the subthreshold swing is dominated by the material properties of the pentacene itself strongly, implying that trapping occurs in the active layer rather than in the insulators. As seen in above results, the maximum trap density of the untreated devices is much lager than that of the treated devices. It infers that the trapping form in the pentacene layer of bare substrates is different from that of treated substrates.

4.5-3 Turn-on Voltage Shift with Deposition Temperature

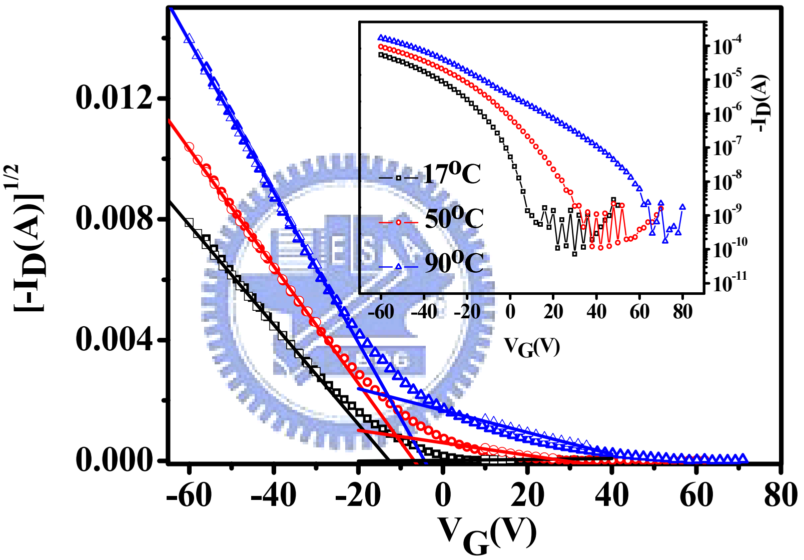


Figure 4. 24 The transfer characteristics of the OTFTs, which were fabricated at various deposition temperature without surface treatments, obtained under V_D=-60V.

Two Gradations of Slope

From the slope of the ($\sqrt{-I_D}$)-V_G plots in Figure 4. 24, it can be separated into two gradations, especially at higher temperature. It is no doubt that the steeper part follows the $\sqrt{\frac{WC_i\mu}{2L}}$ term from the field-effect transistor model at the saturation regime. But the slow part shows deviation from the ideal situation.

It is reported [40] that the humps (in the inset of Figure 4. 24) are caused by the release of deep traps in pentacene layers which are depleted by positive biases. However, why the heater substrates lead the V_T shifts toward more positive direction, and result in a bigger current hump? (To see the following section)

Turn-on Voltage Shift

We have already known that the water layer is likely responsible for the trapping of the pentacene layer. As shown in Figure 4. 24, the V_T shifts toward more positive with the devices made at higher deposition temperature. Furthermore, the slopes of first gradation extracted from the $(\sqrt{}\text{-}I_D)\text{-}V_G$ plot exhibit that the current hump is stronger with increasing temperature. Although high temperature is adverse to water adhesion, it is possible to create a new mixture layer composed by pentacene and water through substrate heating.

Purity of the pentacene is important. For example, iodine-doped pentacene is a p-type material, but alkaline metal-doped pentacene is an n-type one [3]. If the water is doped in the pentacene through heating, the transport properties of this new layer might be different from original pentacene. A build-in potential is common to see between two types of semiconductors. Hence, it behaves like a negative bias applied by the untreated device itself.

4.6 Leakage Current

4.6-1 Channel Length Dependence of Leakage Current

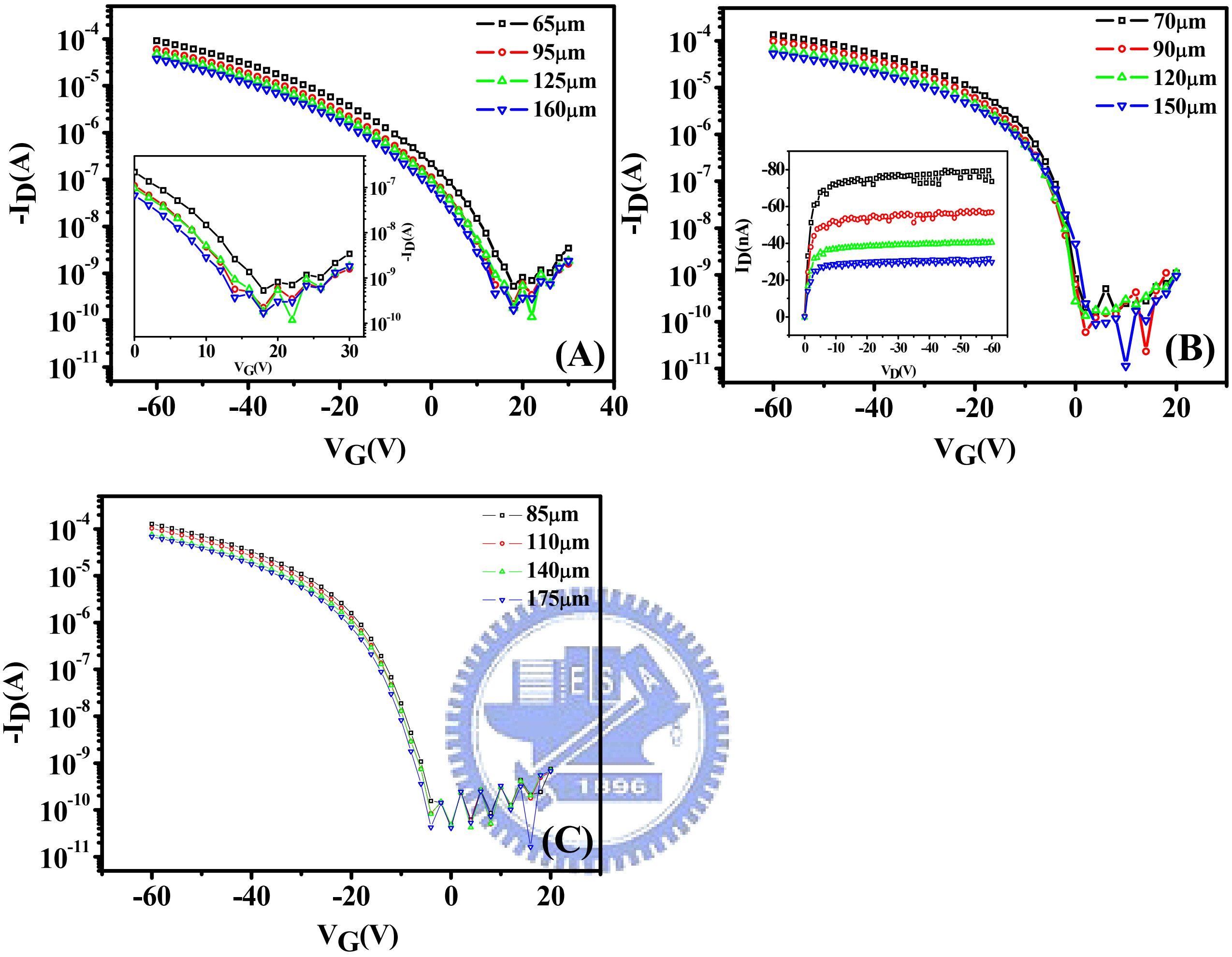


Figure 4. 25 Channel length dependence of transfer characteristics of the OTFTs which are fabricated under room temperature with (A) bare substrate, (B) HMDS-treated substrate, and (C) PαMS-treated substrate.

Poole-Frenkel Emission

For the studies of a-Si TFT, the exponential growth in current at high reverse bias is ascribed to the Poole-Frenkel emission from the defect states [9]. Moreover, for pentacene crystals, hopping is the major mechanism responsible for the carrier transport at room temperature. It is somewhat like amorphous silicon. So, if the carriers are produced by Poole-Frenkel emission, the leakage current of OTFT should be dependent on applied electric field, and therefore, relative to the amount of carrier injection at the gate/drain overlap geometry [9].

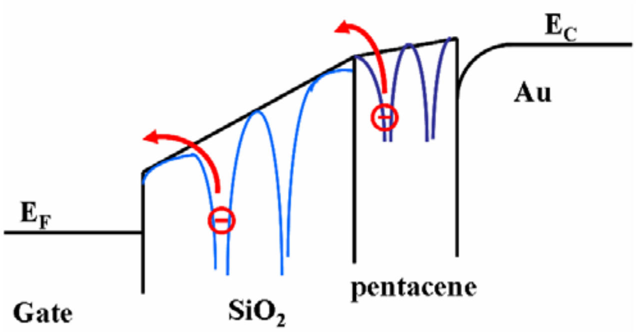


Figure 4. 26 Band diagram of Poole-Frenkel emission.

Poole-Frenkel emission is more apparent for the untreated and HMDS-treated devices, whereas it is unclear for the PαMS-treated ones. This difference is likely due to the better crystalline quality of pentacene for the PαMS-treated substrates, leading to the barrier arising from the disorder is lower. Hence, lower barrier is insensitive to the applied electric field, resulting in unclear Poole-Frenkel emission in the PαMS-treated devices.

Channel Length Dependence

By Figure 4. 25, it is employed to investigate Poole-Frenkel region. It reveals that the leakage current not only increases obviously with higher positive bias, but also rises slightly with shorter channel length.

It is noted that shorter channel also exhibits larger gate/drain overlap vicinity, leading to more carrier injection which enhances off-current (Figure 4. 27). On the other hand, the turn-on point of the devices with shorter channels is higher than in case of longer channels. It is likely due to the carriers are depleted by reverse biases, and form a back channel.

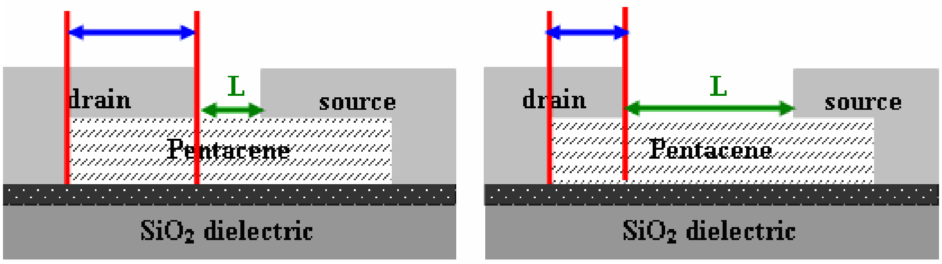


Figure 4. 27 Illustration to show that shorter channel means larger gate/drain overlap vicinity.

4.6-2 Gate Voltage Swept in Both Directions

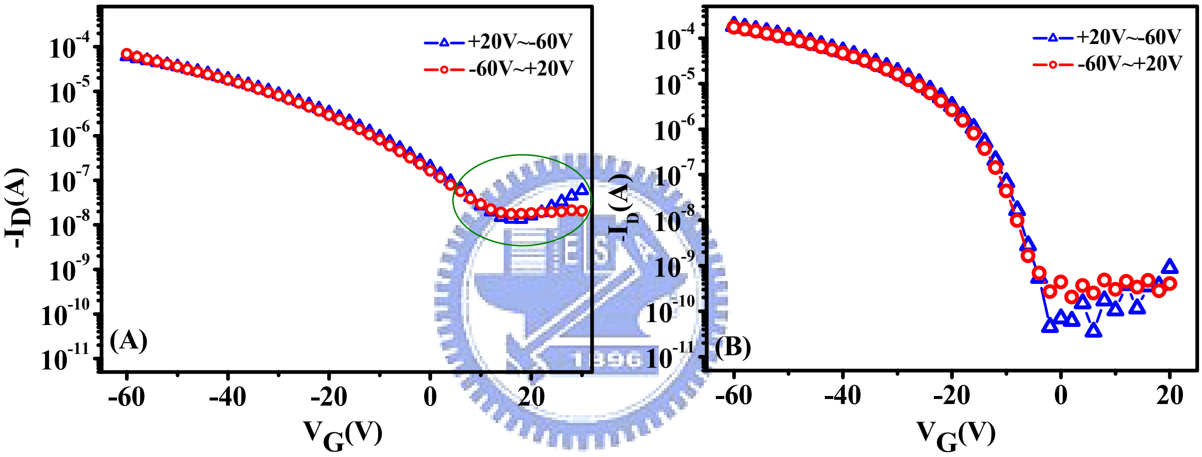


Figure 4. 28 The transfer characteristics of the OTFTs with (A) bare SiO_2 substrate, (B) PαMS treatment, is obtained by sweeping in both directions and under V_D=-60V.

There is no hysteresis [41], or memory effects, as shown in Figure 4. 28. However, it is interesting to see that the difference in off-state. The “tail” of the off-to-on curves raises with increasing positive bias (Poole-Frenkel emission), while the “tail” of the on-to-off ones preserves constant. Secondly, the curves coincide in both directions for the devices without treatments. But for the PαMS treated devices, the leakage current measured in on-to-off direction is larger one order of magnitude than the case in off-to-on scan.

While the device is operated in on-to-off scan, the interface states are filled with electrons at the beginning. If the interface traps do not function as a recombination center, electrons will be kept in the traps, and holes flow in the valence band. In this situation, off-state is dominant by the diffusion or drift of majority carriers rather than Poole-Frenkel emission. That will make the leakage current measured in on-to-off direction is larger than the case in off-to-on scan, such as PαMS treated devices (Figure 4. 28(B)).

Based on the result of section 4.5-2, the density of the maximum traps is 1.4×10^{13} cm^{-2} for the untreated device, and 4.9×10^{12} cm^{-2} for the PαMS-treated one. However, compared to the PαMS-treated devices, it does not show the larger leakage current of on-to-off scan for untreated devices. It is probably due to the carrier recombination at the SiO_2 surface.

CHAPTER 5

Conclusion

By varying the temperature during the deposition of pentacene, the effect of substrate temperature on the electrical performance of OTFTs, without serious disturbance of phase transition of pentacene is investigated.

Except for the serious phase transition of HMDS-treated device, and the rubber state of P MS-treated device, the mobility is promoted with less grain boundary. In order to have more insight into the real situation that how the mobility improves by varying deposition temperature in the conducting path, the transfer line method is employed.

First, the channel resistance is more sensitive to the deposition temperature due to the difference size of grain for HMDS-treated devices, while the case for P MS-treated ones is less sensitive due to no obvious grain boundary in the initial layer to make the channel resistance to change a lot. Second, the both contact resistance reduces with increasing deposition temperature, which is likely attributed from the difference of the molecular orientation. Finally, the bulk resistance should not be ignored especially for the devices with short channel. The bulk resistance is more fluctuant to the deposition temperature for P MS-treated devices, whereas the case for HMDS-treated ones is less fluctuant probably arising from phase boundary.

Additionally, the relationship between pentacene growth to the electrical performance is studied. In our system, roughness of the thermal oxide is identical with the case after surface treatments. The existence of flat-lying pentacene is an important characteristic for the devices applied surface treatments. Hence, the promotion of mobility is probably relative to the flat-lying pentacene.

However, it is unclear what role the in-plane π system plays in the TFT behavior in previous literatures. Based on Ehrlich-Schwoebel barrier effect, mound growth governs the vertical evolution. Furthermore, it also forms deep crevices, and disrupts the quasi-epitaxial layers. According to the AFM images of initial layer (~5ML) and the XRD information, it suggests that flat-lying pentacene could lower the Ehrlich-Schwoebel barrier, leading to blurred and shallow boundaries. Thus, mobility enhancement is due to the low boundary barrier, resulting from the flat-lying pentacene. Effect of grain boundary is still the most important factor to the mobility.

APPENDIX

Program 1, to define the grain boundary density from the N*N matrix of AFM images, is compiled by Matlab.

```
function GB_count (file)

rgb=imread (file);
rgb=imresize(rgb, [512 512]);
r=rgb(:,:,1);
gray2log=(r>139);                % the pink value should be modulated
                                   % to a proper image.

figure; imshow(gray2log);                  % for user to judge the pink value

[u,v]=meshgrid(-255:256, -255:256);     % to define a space for Fourier transform

highpass=1-1./(1+(sqrt(u.^2+v.^2)/60).^4);     % highpass filter

F=fftshift(fft2(double(gray2log)));
y=real(ifft2(fftshift(highpass.*F)));

Y=(y>0.1);                         % to show the pattern obviously

image_i = Y;
dimension = size(image_i);
target = 0;                              % to count how many white pixels is
for i=1 : dimension(1,1)
        for j = 1 : dimension(1,2)
                if image_i(i,j) == 1
                            target = target + 1;
              end;
      end;
end;
```

```
ratio = target/(dimension(1,1)*4)                  % 4 is a constant to make
                                                   % the result normalized.
```

After obtaining the ratio, don’t forget to converse into the unit, per μm.
It is noted that the counting part of this program has some inaccuracy.
If it counts a horizontal or vertical line, there is no erring.
However, if it counts an oblique line of 45 degrees, it will obtain 1.7, not 1.4.

Program 2, to estimate the area of a curved surface from the N*N matrix of AFM images, is compiled by Matlab.

```
function surface_area(file)

n=256;                                          % determine the resolution

image = imread(file);                           % input the image
image1 = image(:,:,1);
image2 = double(imresize(image1,[n,n]));

  x = 1 : n;                                    % create reference surface
  y = 1 : n;
[xx,yy] = meshgrid(x,y);

tri = delaunay(xx,yy);                          % use triangles to plot the surface

ntri=length(tri);                               % find the position vector of triangles
triarea=0;
for k=1: ntri,
      xt = xx(tri(k,:));
      yt = yy(tri(k,:));
      zt = image2(tri(k,:));

      A=[xt(1) yt(1) zt(1)];                    % corner vectors of triangles
      B=[xt(2) yt(2) zt(2)];
```

```
    C=[xt(3) yt(3) zt(3)];

    va=B-C;                         % side vectors of triangles
    vb=A-C;
    vc=A-B;

    a=sqrt(va*va');                 % side lengths of triangle
    b=sqrt(vb*vb');
    c=sqrt(vc*vc');

    if abs(a*b*c)<1e-8              % avoid 1/0
        triarea(k)=0;

    else                            % compute area per triangle
        hh=(vb*vc')^2/((vb*vb')*(vc*vc'));
        triarea(k) = 0.5*c*b*sqrt(1-hh);
end
end
surface = sum(triarea);
substrate = (n-1)^2;
surf_sub = surface/substrate
```

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---

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