Chapter1

Introduction

1.1 Research Motivation

Silicon dioxide (SiO_2) has been used as the gate dielectric of MOSFETs for more than 40 years. Actually, it is still the most popular gate dielectric material in the fabrication of integrated circuits based on Si MOS technologies up to this date. This is because of the extraordinary properties of SiO_2 including excellent Si/SiO_2 interface quality, compatibility with the Si based processes, and its high reliability.

However, the continuous device scaling has made the applications of SiO_2 as the gate dielectric approaching its limit, as ultrathin SiO_2 suffers from many problems such as intolerable high gate leakage current, boron penetration in pMOSFETs, etc [1][2]. Many high-K materials like aluminum-oxide, hafnium-oxide, or zirconium -oxide and their silicate have been proposed to replace the SiO_2. But at this stage most of them still cannot fully satisfy all the conditions that a gate dielectric must posses (i.e., mobility, fixed charge, thermal stability, leakage, reliability, and so on). Before the readiness of these high-K materials, oxynitride (nitrided oxide) is the most likely near-term solution for the upcoming technology node. In comparison with SiO_2, oxynitride has lower gate leakage current, slightly higher K value, greater immunity

to boron penetration, and comparable device performance (if the nitrogen profile and concentration in the gate dielectric are properly engineered). Despite these advantages of oxynitride gate dielectrics, concerns over reliability like aggravated negative-bias-temperature instability (NBTI) in pMOSFETs may rise [3][4]. We therefore devote this thesis to this aspect for better understanding of the effect of incorporated nitrogen and the associated process steps on the device reliability.

1.2 Reliability Issues on Oxynitride Gate Dielectrics

Scaling down of the device size theoretically provides better performance (e.g., current drive) and higher device density in an integrated circuit. However, it also introduces higher power density during circuit operation and increases the chip temperature. The increase in operation temperature accompanied with a thinner gate dielectric significantly worsens the negative-bias-temperature instability (NBTI) of PMOS devices, and presents a serious concern for practical applications. Replacement of SiO_2 gate dielectric with oxynitride may further worsen the situation. These factors enhance the related electrochemical reaction occurring at the interface and lower the activation energy of NBTI. As a result, NBTI could play a major role in limiting device lifetime of deep sub-micron pMOSFETs. It's thus important to clarify the relationship between NBTI and these factors. For this purpose, in this thesis we investigate the NBTI of pMOSFETs with NO annealing oxide, nitride/oxide stack

(N/O stack), and thermal oxide at 25°C and 100°C.

We also studied the effect of hot carrier injection (HCI) of nMOSFETs and explored the associated lifetime by two kinds of stress conditions at 25°C and 100°C. Our purpose is to find how the HCI behaves at high temperature and with nitrogen incorporation. Experimental details and discussion of the results are given in Chapter 3.

1.3 Charge Pumping Measurement Technique

Charge pumping technique has been widely applied in the past two decades to characterize the fast interface traps in MOS transistors [5][6]. This technique was first introduced by Brugler and Jespers [7]. Its concept is based on a recombination process at the gate dielectric/substrate interface involving the surface states. Basic experimental setup of charge pumping is illustrated in Fig. 1-1. The source and drain of the transistor are connected together and held at a certain reverse bias voltage with respect to the substrate. When the transistor is pulsed into inversion, the surface becomes deeply depleted and electrons (taking an nMOSFET as example) will flow from the source and drain into the channel, where some of them will be captured by the surface states. When the gate pulse is driving the surface back into accumulation, the mobile charge drifts back to the source and drain under the influence of the reverse bias, but the charge trapped in the surface states will recombine with the

majority carriers from the substrate and give rise to a net flow of negative charge into the substrate. This substrate current can be directly related to the surface-state density. In this thesis we have used this technique to monitor the change of surface-state density in the recovery process of NBTI degradation. Details of experimental setup, measurement programs, and discussion of results can be found in Chapter 4.

1.4 Thesis Organization

We have performed NBTI and HCI experiments in this work to clarify the effects of temperature and the nitrogen incorporation in gate dielectrics on device reliability. In addition, charge pumping measurements have been conducted to study the relationship between threshold voltage (Vt) recovery of NBTI and surface-state density. In addition to a brief introduction of research background and experimental technique in this chapter, this thesis is organized as follows:

In Chapter 2, we describe the device structure, fabrication steps, and basic electrical characteristics of the test samples. The measurement setups for NBTI and HCI experiments are also described.

In Chapter 3, we present the experimental results of NBTI and HCI stressing. Basic concepts regarding the stress conditions and experimental setup are also included. The impacts of stress temperature and nitrogen incorporation in the gate dielectric on NBTI and HCI lifetime are discussed.

In Chapter 4, we use the charge pumping technique to evaluate surface-state density change during the NBTI recovery process. Detailed illustrations of experimental setup and measurement program are shown. Results of charge pumping experiments are discussed.

Chapter 5 concludes this work by summarizing the major results and findings we obtain. Some suggestions for future work on this topic will also be given.

Chapter2

Device Structure and Basic Electrical Properties

2.1 Device Structure

Test devices characterized in the NBTI and HCI experiments were kindly provided by the Taiwan Semiconductor Manufacturing Company (TSMC). Dual-gate p- and n-channel MOSFETs were fabricated using a standard state-of-the-art CMOS twin-well technology. Three kinds of gate dielectric, i.e., NO annealing oxide, nitride/oxide stack (N/O stack), and thermal oxide, were used. The N/O stack consists of 0.8 nm bottom oxide and 1.4 nm high quality nitride. The bottom oxide was grown by wet oxidation in a catalysis oxidation chamber. Prior to CVD nitride deposition step, a remote plasma nitridation (RPN) treatment was performed by exposing the bottom oxide to a high density remote helicon-based nitrogen discharge at 450°C for 30 sec. This RPN treatment provides a thin oxynitride layer of smooth and high nitrogen concentration on the oxide top surface, and serves to buffer the structural mismatch between the bottom oxide and the nitride film. A post deposition annealing was performed in N_2 ambient to reduce defect density. In the other two splits, the gate oxide was thermally grown by wet oxidation, followed by a RTA treatment in NO ambient for thermal oxide and a high temperature anneal in NO gas for NO annealing

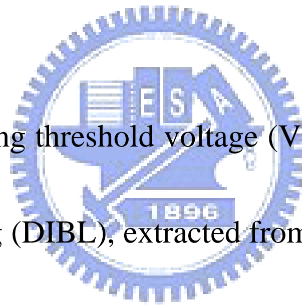
oxide. Equivalent oxide thickness (EOT) for all splits was determined to be about 1.6 nm, using a CV method that takes into account both the quantum mechanism and the poly gate depletion effects. The size of devices which were used in the NBTI and HCI experiments is W = 10 μm and L = 0.13 μm.

2.2 Basic Electrical Properties of Devices

This section shows basic electrical properties of devices used in the NBTI and HCI experiments. Devices with W = 10 μm and L = 0.18 μm were used in this characterization. The data shown here represents average results by measuring a number of devices across the wafers. In most cases, the thickness variation of all devices is under 0.1nm, which introduces 6% variation in drain current.

Figure 2-1 shows the gate leakage current of three kinds of samples. The NO-annealed oxide has the largest leakage current of all splits in both n- and pMOSFETs, while the N/O stack has the lowest one. In general, the incorporation of nitrogen in the gate dielectric will reduce the leakage current due to a higher physical thickness under the same EOT. But in our devices, the NO annealing oxide has larger leakage current than the thermal oxide. Figures 2-2 and 2-3 illustrate the Id-Vd and transconductance (Gm), respectively. From these data, we found that the sample with NO-annealed oxide exhibits the best current drivability while that with thermal oxide exhibits the worst. Figure 2-4 shows Id-Vg characteristics of the three splits. The

NO-annealed oxide has the highest off-state leakage current (gate-induced drain leakage, GIDL). From the results and comparison shown above, we speculate that the sample with NO-annealed oxide has a thinner equivalent-oxide –thickness (EOT) than the other two splits. To confirm this point, C-V measurement and NCSU-CVC method [21] were employed to determine the precise EOT value. The resultant C-V data are shown in Figs. 2-5(a) and (b) for n- and pMOSFET, respectively. We found that EOT of the NO-annealed oxide is indeed roughly 1.0~2.0nm thinner than the other two splits. This explains the difference in characteristics shown in Figs. 2-1 ~ 2-4.



Some parameters including threshold voltage (Vt), subthreshold swing (SS), and drain-induced barrier lowering (DIBL), extracted from Fig. 2-4, are listed in Table 2-1. From this table, it should be noted that p-channel threshold voltages are not well tuned among different splits. In addition, oxynitride samples depict higher SS in nMOSFETs and smaller SS in pMOSFETs, compared to the thermal oxide control. They also show better DIBL characteristics for both n- and p-channel transistors, compared to the thermal oxide samples. These indicate that the substrate doping profile designs in these devices are not yet optimized.

2.3 Influences of Electrical Properties on Reliability Tests

Our reliability tests (NBTI and HCI experiments) were performed with constant

voltage conditions, i.e., all the experimental results were compared under a fixed stress voltage. As a result, the differences in some electrical properties like threshold voltage (Vt) and drain current (Id) may cause unfair comparisons of device lifetime projection. For NBTI test performed on pMOSFETs, this problem is expected to be less severe. This is because the devices are biased at a negative gate voltage to turn the device into inversion during stressing. While zero source and drain biases ensure that there is no drain current flow between source and drain, so the mobility difference among different splits does not play any role. Despite the fact that p-channel threshold voltage is quite different among different splits, its influences on NBTI degradation are expected to be insignificant. This is because the gate bias voltage (Vg) alone is expected to dominate the NBTI effect [8]. For HCI experiments, since the threshold voltage difference is very small in nMOSFETs, its effect can be ignored. However, the differences in drain current may cause problems in HCI lifetime comparison, since drain current has a strong impact on the HCI degradation. Specifically, the HCI degradation depends on drain current, impact ionization rate, and injection rate. Their combined product represents the number of hot carrier injection into the gate dielectric. In this work, we define the device lifetime as 5% degradation of drain current in saturation to minimize the errors caused by the different drive current observed on different splits. In any rate, since we are

comparing lifetime under a fixed voltage basis, the difference in impact ionization rate may introduce unfair factors in comparison of lifetime. This will be carefully checked in the discussion of HCI experiments (Section 3.5).

Chapter 3

NBTI and HCI Experiments

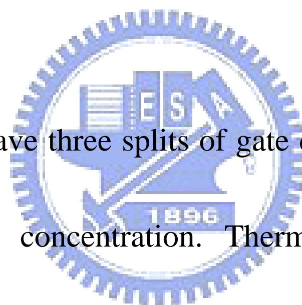
3.1 Measurement Setup

Figs. 3-1(a) and 3-1(b) show configurations of NBTI and HCI experimental setups, respectively. In NBTI experiments, the gate electrode of the test device was subjected to a negative bias (-2.2 ~ -3.0V) with all the other three electrodes grounded. In HCI experiments, the gate and drain electrodes were positively biased (Vd = 1.8 ~ 2.4V, Vg = Vd or Vg @ Isubmax), while the other two electrodes were grounded. Experiments were executed using **Keithley 4200** semiconductor characterization system. Device parameters including threshold voltage (Vt), drain current, and transconductance (Gm) were recorded during stressing at certain time intervals. NBTI and HCI experiments were both performed at 25°C and 100°C.

3.2 Nitrogen Profile Engineering

NBTI of pMOSFETs has become one of the most serious reliability issues for ULSI devices. Moreover, it has been reported that NBTI degradation is remarkably enhanced when nitrogen is incorporated [3][8]. Many theories have been proposed to explain this nitrogen-enhanced NBTI effect. A recent theoretical attempt by Ushio et

al. attributed this effect to lower reaction energies of hole-trapping reactions at the Si/SiO_xN_y interface than that at the Si/SiO_2 interface [22]. Ang et al. speculated that it is due to interfacial nitrogen-induced P_b center [9]. Although the mechanism of nitrogen-enhanced NBTI effect is still not fully understood, it is commonly agreed that nitrogen incorporation in the gate dielectric will enhance NBTI degradation. In addition, it has recently been reported that the nitrogen proximity to the Si/SiO_2 interface has strong influence on NBTI [10][11]. Accordingly, the nitrogen profile and the amount of nitrogen incorporated in the gate dielectric will be important factors for p-channel NBTI lifetime.



In our test devices, we have three splits of gate dielectric. And each has its own unique nitrogen profile and concentration. Thermal oxide is pure oxide with essentially zero nitrogen incorporation. For NO annealing oxide, the peak nitrogen concentration is located near the interface of gate dielectric and substrate [8]. It thus has the highest nitrogen concentration at the interface among all splits. Nitrogen in N/O stack is mainly located at the upper portion (i.e., nitride film) of the stack dielectric. While N/O stack has the highest nitrogen concentration in the bulk of the gate dielectric among all splits, it has significantly less nitrogen at the interface of gate dielectric and substrate, compared to NO annealing oxide. In Section 3.4, we will examine the correlation between nitrogen profile and NBTI lifetime. And we will also

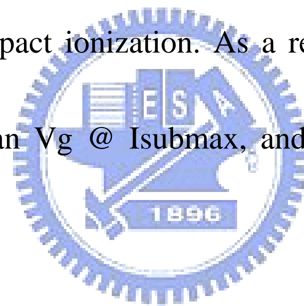
determine the relationships between nitrogen profile and HCI degradation. Experimental results and discussion will be given in Section 3.5.

3.3 Differences between Two Kinds of HCI Stress Conditions

In our HCI experiments, two kinds of stress conditions are used. Specifically, there are two choices for gate bias (Vg) for a given drain bias (Vd). The first one is Vg @ Isubmax, i.e., the gate voltage at maximum substrate current. The second is Vg = Vd, in which the same bias voltage is applied to gate and drain electrodes.

Traditionally, the Vg @ Isubmax represents the worst case for n-channel HCI degradation. However, it has been reported recently that the damage result under Vg = Vd may become more severe than Vg @ Isubmax when the device size and operation voltage are scaled down [13]. It has been explained by the position and energy of the injected carriers. Position of carriers under gate dielectric will affect the efficiency of carriers to create interface-state by bombarding the oxide interface [12]. Fig. 3-2 illustrates the position of carriers at different bias conditions. Under bias at Vg @ Isubmax, the vertical electrical field near the drain is larger than under bias at Vg = Vd (Vg @ Isubmax is about Vg = Vd/3 ~ Vd/2). However, the field direction is such that carriers are guided away from the interface. Although these two bias conditions have similar number of carriers that have sufficient energy to cause impact ionization and generation of interface-state for deep sub-micron devices with ultrathin oxide.

The number of energetic carriers that bombard the interface is greater at Vg = Vd and, thus, it becomes the worst-case HCI stress condition. However, this explanation is not complete, because a similar change in current path also happens in older devices with longer channel length and thicker oxide. Another explanation for the shift in the worst-case stress condition in deep sub-micron nMOSFETs is because of the increased injection of the "high-energy tail" electrons into the gate dielectric as Vg approaches Vd [14]. These high energy electrons can more easily overcome the injection barrier of gate dielectric and cause damage, even though they don't significantly contribute to impact ionization. As a result, Vg = Vd stress condition causes more degradations than Vg @ Isubmax, and becomes the worst-case stress condition.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Traditionally, the Vg = Vd stressing is not the worst-case stress condition for long channel devices. This can be understood from Figs. 3-3(a), (b), and (c), where Isub vs. gate voltage at Vd=2.2V are plotted for devices with N/O stack, NO anneal oxide, and oxide, respectively. For devices with longer channel length (i.e., 0.24 μm), maximum Isub is much larger than Isub at Vg = Vd. This means the number of hot carriers at Vg @ Isubmax stress condition is much more than that at Vg = Vd. Thus, the Vg @ Isubmax represents the worst-case stress condition because of its higher impact ionization rate. However, when the channel length is scaled down to 0.12 μm,

these two stress conditions depict comparable Isub, i.e., the number of hot carriers is nearly equal. In this situation, the HCI damage is dominated by the injection rate, which is higher at Vg = Vd stress condition for devices with ultrathin oxide. So Vg = Vd stressing could become the worst-case condition. Another concern for Vg = Vd is that the source side has a large vertical field, and the degradation in device electrical properties may be caused by source side electron injection into the gate dielectric. This concern can be ruled out since the damage caused by electron injection is much less than that caused by hot carriers. The experimental evidences are shown in Table 3-1. The electron injection under Vg = 2.2V after 5000 sec. only results in about 4mV Vt shift, which is much less than the hot carrier induced damage under Vg = Vd = 2.2V after 2000 sec. In conclusion, the prominent damage under Vg = Vd stress condition is the hot carrier damage at drain side, which is the same as Vg @ Isubmax condition. And it becomes the worst-case as a result of comparable impact ionization rate to Vg @ Isubmax condition and higher injection rate originated from high-energy tail electrons.

Different stress conditions exhibit different stress voltage dependence, leading to different results of lifetime projection, since the slope of projection lines are different. This phenomenon can be seen in Fig. 3-4. In this figure, the Vg = Vd stress condition depicts more severe HCI degradation than the Vg @ Isubmax stress condition at high

drain bias, however, the Vg = Vd stress condition still has a longer extrapolated lifetime at Vg = 1V than the Vg @ Isubmax stress condition. In Section 3.5, we will discuss the stress voltage dependence of HCI lifetime projection for different stress conditions and temperatures.

3.4 Results and Discussion of NBTI Experiments

Figures 3-5(a), (b), and (c) are the NBTI lifetime projection at different temperatures for devices with N/O stack, NO annealing oxide (NO anneal for short in the following discussion), and thermal oxide (oxide for short in the following discussion), respectively. It can be found that the degradation increases when temperature changes from 25°C to 100°C for all splits, since the increase of temperature can help carriers to overcome the activation energy barrier of NBTI chemical reaction at the interface [3]. Figs. 3-6(a) and (b) are lifetime projection of all splits at 25°C and 100°C, respectively. The lifetime extrapolated to normal operation voltage (i.e., |Vg| = 1V) is listed in Table 3-2. As shown in the table, the oxide has the best immunity to NBT stressing and the nitrogen incorporation will reduce the NBTI lifetime. This result is consistent with that shown in [8] and can be explained by activation energy lowering of NBTI chemical reaction due to nitrogen incorporation. From Fig. 3-6, we found that the NO anneal split has longer lifetime projection than the N/O stack one, though it degrades more at higher stress voltage especially in Fig.

3-5(a). This is due to the different slopes of lifetime projection lines, which means that different samples have different voltage dependences. The slope of all lifetime projection lines is summarized in Fig. 3-7. A larger slope means larger voltage dependence, and indicates that the degradation is more sensitive to voltage change. This implies that the voltage has some additional effect on the degradation mechanism. From Fig. 3-7, some experimental observations and speculations to explain these observations are summarized as follows:

1. The slope seems to increase with increasing nitrogen concentration presenting at the interface of gate dielectric and substrate. This will affect the lifetime projection results for devices with comparable nitrogen concentration but different profile.

2. N/O stack structure shows a slightly smaller slope. This might be related to its larger physical thickness and an additional interface in the bulk of gate dielectrics.

3. The slope becomes smaller when temperature changes from 25°C to 100°C. This can be explained by the fact that at higher temperature, the carriers possess higher energy to surmount the activation energy barrier. So the external voltage requires to lowering the barrier may not be as necessary as it is at low temperature.

4. The slope change ratio (from 25°C to 100°C) seems to be strongly related with the nitrogen concentration at the interface of gate dielectric and substrate. This is because for the gate dielectric with higher nitrogen concentration, it has reduced

activation energy barrier and thus is less dependent on elevated temperature to increase the energy of carriers.

Finally, it is worth noting that the slope of the lifetime projection lines is very sensitive to the experimental results and large error might occur for the lifetime projection. More experimental data should therefore be collected to increase the accuracy of the lifetime projection, while the stress voltage should be extended to lower level, which is closer to the real operation voltage in order to reduce projection errors. The data shown in this work are not absolutely foolproof as we don't have sufficient number of devices for measurements, and time and resources are limited. However, we believe the results of this experiment still provide a fundamental guideline for future research.

3.5 Results and Discussion of HCI Experiments

Figs. 3-8(a), (b), and (c) are the HCI lifetime projection for Vg = Vd stress condition at different temperatures for devices with N/O stack, NO anneal, and oxide respectively. While the corresponding results for Vg @ Isubmax stress condition are shown in Figs. 3-9(a), (b), and(c), respectively. When temperature changes from 25°C to 100°C, the two nitrogen-related splits show decreased extrapolated lifetime while the lifetime of the oxide split increases instead. This indicates that the nitrogen incorporation changes the temperature dependence of HCI degradation. Figs. 3-10(a),

(b) and Figs. 3-11(a), (b) are the HCI lifetime projection at 25°C and 100°C for Vg = Vd and Vg @ Isubmax stress conditions, respectively. At high stress voltage, the oxide has the lowest and the N/O stack has the highest degradation in all cases. The oxynitride splits seem to have weaker immunity to HCI and the stack structure has an even worse result. The results of lifetime projection are listed in Table 3-2. Lifetime is reduced when the stress condition is changed from Vg = Vd to Vg @ Isubmax, except for the NO anneal split stressed at 25°C. Most of the results are consistent with those at high stress voltage, except that the NO anneal split has a longer lifetime than oxide at 25°C, due to the different slope of lifetime projection lines.

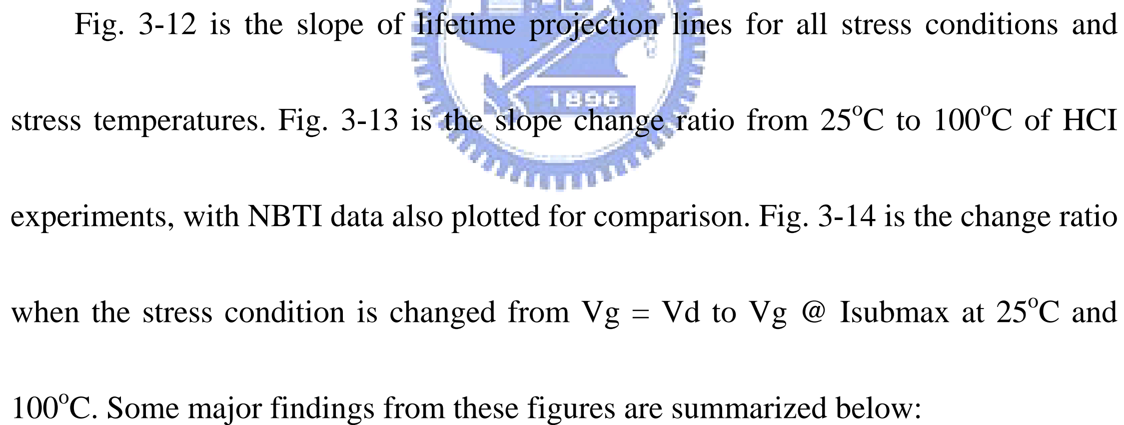

Fig. 3-12 is the slope of lifetime projection lines for all stress conditions and stress temperatures. Fig. 3-13 is the slope change ratio from 25°C to 100°C of HCI experiments, with NBTI data also plotted for comparison. Fig. 3-14 is the change ratio when the stress condition is changed from Vg = Vd to Vg @ Isubmax at 25°C and 100°C. Some major findings from these figures are summarized below:

1. In Fig. 3-12, we can see that the slope with Vg = Vd stress condition is always larger than that with Vg @ Isubmax at the same temperature. As a result, the Vg @ Isubmax will be the worst-case stress condition in lifetime projection. The mechanism behind this phenomenon is explained in Section 3.3.

2. The slope change is positive for the thermal oxide split and negative for

oxynitride splits when temperature changes from 25°C to 100°C (Fig. 3-13). More nitrogen incorporation at the interface of gate dielectric and substrate will induce more negative slope change ratio. This suggests that nitrogen incorporation could be a lifetime killer for high temperature operation. We speculate that this phenomenon is a result of a chemical reaction associated with nitrogen, which is more activated at high temperature (100°C).

3. When comparing the slope change ratio from 25°C to 100°C of HCI and NBTI experiments (Fig. 3-13), we found that the nitrogen incorporation has different effects. In the NBTI experiments, more nitrogen incorporated at the substrate interface exhibits more positive slope change ratio. As mentioned previously, nitrogen incorporation results in the lowering of activation energy for NBT chemical reaction, thus temperature activation becomes less important. However, such condition may not hold true for HCI reaction.

4. The slope change ratio from Vg = Vd stress condition to Vg @ Isubmax condition shows the same trend at 25°C and 100°C (Fig. 3-14). The NO anneal split has lower slope change ratio than the oxide split, which might be due to the nitrogen incorporation in the gate dielectric. This implies that the oxynitride is less sensitive to the change of the carrier energy distribution function [13]. But this explanation cannot apply to the N/O stack split: it exhibits a dramatically large slope change ratio than

the other splits. Note the field inside the N/O stack is reduced during stressing (due to larger physical thickness) and an additional nitride/oxide interface presenting inside the dielectric. These unique properties might be responsible for the very different slope change ratio of the N/O stack sample.

5. The slope change ratio (from Vg = Vd to Vg @ Isubmax) increases in all splits when temperature changes from 25°C and 100°C (Fig. 3-14). This indicates that the temperature has different influence on these two stress conditions, and suggests that different mechanisms are responsible for the HCI degradation in these two stress conditions.

3.6 Worst-Case of Device Reliability

From Table 3-2, we found that the HCI lifetime is longer than NBTI in most cases. The only exception is the N/O stack split under Vg @ Isubmax stress condition at 100°C. By considering possible error in our experiments and the very similar results of NBTI and HCI lifetime under Vg @ Isubmax stress condition for N/O stack, more data are needed to confirm this result. For NO anneal and oxide splits, it is clear that the NBTI is the limiting factor of device lifetime in our W/L = 10/0.13 μm device with 1.6 nm EOT gate dielectric. Since the N/O stack and oxynitride splits have much shorter lifetime than pure oxide, NBTI should be seriously taken into account when nitrogen-incorporated gate dielectric is used.

Chapter 4

Charge Pumping Experiments

4.1 Measurement Setup of Charge Pumping

Fig. 4-1 shows the configuration of measurement setup used in our charge pumping experiment. The bias condition has been described in Section 1.4. An HP 81110A pulse generator is connected with an HP 4156 parameter analyzer through GPIB. A manual switch is used to connect the gate electrode of the device with HP 4156 or HP 81110A. In this experiment, we use HP iBASIC program to perform the charge pumping measurement. Details about the program can be found in Appendix. This program is used to control the HP 81110A for pulse signal generation and the charge pumping measurement in the HP 4156. The GPIB interface is used to communicate with the HP 81110A. A manual switch is used for the convenient switching of the gate electrode of the test device between the HP 81110A when measuring charge pumping current, and HP 4156 when measuring transfer characteristics.

4.2 Experiment

The devices used in this experiment were provided by the courtesy of TSMC.

Dual-gate p- and n-channel MOSFETs were fabricated using a standard CMOS twin-well technology. Two kinds of gate dielectric splits, namely, NH_3-annealed oxide and pure oxide, were characterized. The gate dielectrics of the two splits were both grown by wet oxidation. The NH_3-annealed oxide received an additional 900°C, 60 sec. annealing process in NH_3 ambient. Equivalent oxide thickness (EOT) was determined to be about 1.9 and 2.0nm for NH_3 annealing oxide (NH3 anneal for short in the following discussion) and pure oxide, using CV method that takes into account both the quantum mechanical and the poly gate depletion effects. The size of devices used in this experiments is W = 100 μm and L = 0.18 μm. Devices used in NBTI and HCI experiments mentioned in previous chapters are not suitable for charge pumping measurements, because their gate dielectric thickness is too thin (1.6nm). The accompanying large gate leakage current makes it very difficult to precisely measure the charge pumping current. Besides, the charge pumping current is too small to be distinguished from noise for those small-size devices. We thus choose devices with thicker gate dielectric and large active area for reliable characterization.

In this experiment, we performed NBT stress (Vg = -2.5V) on pMOSFETs for the first 1500 sec, followed by a relaxation period with different biases applied to the gate electrode (Vg = 0, 1.25, and 1.75V) or substrate electrode (Vsub = -2V). All experiments were executed at 150°C. The relaxation period was used to study the

recovery characteristics. Threshold voltage (Vt) and charge pumping current (Icp) were recorded at intervals of 0, 300, 800, and 1500 sec. during NBTI stress and subsequent relaxation periods. The parameters of the pulse bias applied to the gate electrode during charging pumping measurement were: frequency = 1MHz, rise time = fall time = 10 ns, duty cycle = 50%, Vg_High = 1.2V, Vg_Low = -0.6 ~ -1.0V. Five sampling points are set in each Icp measurement, and the Icp data shown in this work represent the average value. To minimize NBTI recovery during the CP measurement, only a few points were measured. The relationship between Vt shift and the amount of interface-state density variation will be discussed in the following section. Influence of applied voltage on the NBTI recovery process will also be addressed.

4.3 Results and Discussion

Figs. 4-2(a), & (b) and Figs. 4-3(a), & (b) show Vt and Icp shifts for oxide and NH_3-anneal splits, respectively. Please note that these data are normalized with respect to peak Vt and Icp shifts immediately before relaxation. It can be seen that more shifts in Vt and Icp are observed for the NH_3-anneal split under the same NBT stress voltage. In addition, most Vt and Icp shifts occur in the first 300 seconds of the stress and recovery cycles. This can be explained by the reaction-diffusion model [3][15][16][18]. Specifically, the stress cycle can be divided into two phases, i.e., the initial reaction phase (0~300 sec.) and the subsequent diffusion phase (300~1500 sec.).

In the reaction phase, the holes from the inversion layer are injected into the gate dielectric. These holes break the Si-H bonds, cause interface-state generation. Both Vt and Icp shift rapidly during this phase, and the rate of shift is dominated by the reaction between holes and Si-H bonds. When Si-H bonds are broken, hydrogen-related species are released from the interface and diffuse into the bulk of the gate dielectric (i.e., the diffusion phase). These species will create defects, which serve as hole-trapping centers, and increase Vt shift monotonically. The rate of shift during the diffusion phase is smaller than that during the reaction phase because the diffusion process is the dominant factor. During the recovery phase, a reversal process occurs. Specifically, hydrogen-related species near the interface rapidly anneals the broken Si-H bonds during the reaction phase. As time evolves, this reaction creates a "diffusion hole" that reduces subsequent annealing of the broken bonds. The recovery process now enters the diffusion phase. The hydrogen-related species in the bulk of the gate dielectric diffuses back to the interface to anneal the broken bonds. Thus, this phase is diffusion dominant [17].

Before the discussion of experimental results, it should be noticed that some Vt data show anomalous behavior (e.g., Vg = 0, 1.75V during the recovery cycle for oxide split, and Vg = 1.25V for NH_3-anneal split). We believe that they are only measurement errors, and do not affect our observation of experimental results. Fig.

4-4 and Fig. 4-5 show Vt and Icp recovery ratios, respectively, measured after 1500 sec. recovery cycle. For comparison, we also performed the "recovery stress" (i.e., Vg = 1.75V) on some virgin devices, it was found that less than 1mV in Vt shift and only 6% increase in Icp after 1500 sec. Moreover, the Vt and Icp shift caused by the Vsub = -2V on the virgin devices is even smaller. From Fig. 4-4, Vt shift recovery does not seem to be greatly affected by the externally applied voltage. The Vsub = -2 V condition has only slightly large recovery ratio than the others. The NH_3 anneal split depicts a slightly higher recovery ratio than the oxide split. This may be due to its higher hydrogen concentration and the incorporation of nitrogen at the interface. For Icp shift ratio, the NH_3-annealed and oxide splits show comparable results and the external applied voltage has no apparent influence on Icp recovery except for Vsub = -2 V. Some conclusions from the experimental results are summarized as follow:

1. The hydrogen-related species appears to be a neutrally charged species, since the external voltage bias doesn't seem to accelerate the diffusion process.

2. The Vt recovery ratio is larger than Icp recovery ratio in all cases. This suggests that there are other sources such as slow states and oxide traps in the bulk of the gate dielectric that also contribute to the Vt recovery in addition to interface-states [19][20]. And their detrapping characteristics are different from those of interface-states.

3. The substrate bias (Vsub = -2V) effectively increases the Icp recovery ratio. This can be attributed to the fact that electrons with higher energy are being injected into the gate dielectric under this bias condition. This causes a more rapid annealing of the broken bonds and a faster recombination rate of the “diffusion holes”. However, this bias condition only shows a slightly higher Vt recovery ratio than other biasing conditions. This is because some parts of the Vt recovery arise from slow states and oxide traps, and these contributions are less affected by the substrate bias.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

In this work, we have characterized NBTI and HCI characteristics at 25°C and 100°C on PMOS devices with three kinds of gate dielectric splits (i.e., N/O stack, NO annealing oxide, and thermal oxide). The effects of gate dielectric structure, nitrogen profile and concentration on NBTI and HCI degradation were thoroughly analyzed. The correlation between these factors and device lifetime projection was also discussed. We found that the nitrogen has different impacts on NBTI and HCI. Some possible mechanisms are proposed to explain the observed phenomena. Special attention should be paid to nitrogen profile engineering for devices with oxynitride gate dielectric because of its negative impacts and influences on device electrical characteristics and reliability.

In the charge pumping experiment, the recovery ratio of Vt and Icp for NH_3-annealed and oxide splits has been compared under different stress and relaxation conditions. From the experimental results, we speculate that the chemical reactions associated with the hydrogen-related species in NBTI are likely to be related to a neutrally charged species, since the recovery ratio does not seem to be affected by

different gate biases during the recovery cycle. Our results also show that the Icp recovery ratio increases significantly under negative substrate bias, when electrons with higher energy are injected, although only little effect is observed on Vt recovery ratio. This indicates that other sources such as slow states and oxide traps whose detrapping characteristics are different from that of interface-states may contribute to the Vt recovery.

5.2 Future Work

Accompanied with the continuous scaling of device size, nitrogen-incorporated dielectric will be inevitably employed in nano-scale CMOS manufacturing. It is thus essential to clarify the correlations between the incorporated nitrogen and reliability degradation mechanisms. In addition, more efforts are needed to obtain in-depth understanding regarding the NBTI and HCI on high-K materials.

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Appendix

Following is the iBASIC program used in our charge pumping experiment.

```
10      ASSIGN @Hp415x TO 800
20      ASSIGN @Form_off TO 800;FORMAT OFF
30      ASSIGN @Hp4155 TO 717
40      ASSIGN @Form_off TO 717;FORMAT OFF
50      COM @Hp415x,@Form_off
60      ASSIGN @Hp8110 TO 710
70      CLEAR @Hp8110
80      OUTPUT @Hp415x;":DISP:WIND:ALL BAS"
90
100     OUTPUT @Hp8110;"*CLS"
110     OUTPUT @Hp8110;"*RST"
120     COM /Meas_info/ REAL Duration,Det_time,Vd,Id,Ib,Vs,Vb,Vg,Ab,Amp
130     COM /Meas_info1/ REAL Delta_v,Area,Vgh,Vgl,Vfl,Vfh,Vth,Vtl,Icp,Freq
140     COM /Meas_data/ INTEGER Step,Loop,Ccy,Clp
150     COM /Meas_data/ REAL Fb(1:1000),Fh(1:1000),Th(1:1000),Qcp(1:1000)
160     COM /Meas_data/ F(1:1000),Ibcp(1:1000),Idcp(1:1000)
170     COM /File_name/ Save_file$[12],Save_file1$[12],Ccy$[12]
180     CALL Init_hp4155
190     Vg=0.
200     Vd=-0.05
210     Ib=0.
220     Vs=-0.05
230     Vb=0.
240     Loop=1
250     Step=1
260     Duration=0.5
270     Det_time=2
280 !=================================
290     Freq=1000000
300     Vgh=1.2
310     Vgl=-0.6
```

```
320     !Amp=0
330     !Vgl=Vgh-Amp
340     !Vgh=Vgl+Amp
350 !=================================
360     FOR Clp=1 TO 5
370     CALL Pulse
380     CALL Samp_setting
390     OUTPUT @Hp8110;":OUTP1 OFF"
400     WAIT 1
410     Vgl=Vgl-0.02
420     !Vgh=Vgh+0.1
430     Step=Step+1
440     NEXT Clp
450     CALL Save_data
460     END
470 !=================================
480 Pulse:SUB Pulse
490      COM /Meas_info/ REAL Duration,Det_time,Vd,Id,Ib,Vs,Vb,Vg,Ab,Amp
500      COM /Meas_info1/ REAL Delta_v,Area,Vgh,Vgl,Vfl,Vfh,Vth,Vtl,Icp,Freq
510      COM /Meas_data/ INTEGER Step,Loop,Ccy,Clp
520      COM /Meas_data/ REAL Fb(1:1000),Fh(1:1000),Th(1:1000),Qcp(1:1000)
530      COM /Meas_data/ F(1:1000),Ibcp(1:1000),Idcp(1:1000)
540      COM /File_name/ Save_file$[12],Save_file1$[12],Ccy$[12]
550      ASSIGN @Hp8110 TO 710
560      OUTPUT @Hp8110;":FREQ "&VAL$(Freq)&"Hz"
570      OUTPUT @Hp8110;":PULS:DCYC1 50PCT"
580      OUTPUT @Hp8110;":PULS:TRAN1:LEAD 10NS"
590      OUTPUT @Hp8110;":PULS:TRAN1:TRA 10NS"
600      OUTPUT @Hp8110;":VOLT1:HIGH "&VAL$(Vgh)&"V"
610      OUTPUT @Hp8110;":VOLT1:LOW "&VAL$(Vgl)&"V"
620      OUTPUT @Hp8110;":OUTP1:IMP:EXT 999KOHM"
630      OUTPUT @Hp8110;":OUTP1 ON"
640      SUBEND
650 Samp_setting:SUB Samp_setting
660      COM @Hp4155,@Form_off
670      COM /Meas_info/ REAL Duration,Det_time,Vd,Id,Ib,Vs,Vb,Vg,Ab,Amp
680      COM /Meas_info1/ REAL Delta_v,Area,Vgh,Vgl,Vfl,Vfh,Vth,Vtl,Icp,Freq
690      COM /Meas_data/ INTEGER Step,Loop,Ccy,Clp
```

```
700     COM /Meas_data/ REAL Fb(1:1000),Fh(1:1000),Th(1:1000),Qcp(1:1000)
710     COM /Meas_data/ F(1:1000),Ibcp(1:1000),Idcp(1:1000)
720     COM /File_name/ Save_file$[12],Save_file1$[12],Ccy$[12]
730     DIM B(1:11)
740     OUTPUT @Hp4155;":PAGE:CHAN:COMM 'Subth IB-T CURVE
        "&VAL$(Step)&"'"
750     OUTPUT @Hp4155;":PAGE:CHAN:MODE SAMP"
760     OUTPUT @Hp4155;":PAGE:CHAN:SMU1:VNAME 'VS'"
770     OUTPUT @Hp4155;":PAGE:CHAN:SMU1:INAME 'IS'"
780     OUTPUT @Hp4155;":PAGE:CHAN:SMU1:MODE V"
790     OUTPUT @Hp4155;":PAGE:CHAN:SMU1:FUNC CONS"
800     OUTPUT @Hp4155;":PAGE:CHAN:SMU2:VNAME 'VG'"
810     OUTPUT @Hp4155;":PAGE:CHAN:SMU2:INAME 'IG'"
820     OUTPUT @Hp4155;":PAGE:CHAN:SMU2:MODE V"
830     OUTPUT @Hp4155;":PAGE:CHAN:SMU2:FUNC CONS"
840     OUTPUT @Hp4155;":PAGE:CHAN:SMU3:VNAME 'VD'"
850     OUTPUT @Hp4155;":PAGE:CHAN:SMU3:INAME 'ID'"
860     OUTPUT @Hp4155;":PAGE:CHAN:SMU3:MODE V"
870     OUTPUT @Hp4155;":PAGE:CHAN:SMU3:FUNC CONS"
880     OUTPUT @Hp4155;":PAGE:CHAN:SMU4:VNAME 'VB'"
890     OUTPUT @Hp4155;":PAGE:CHAN:SMU4:INAME 'IB'"
900     OUTPUT @Hp4155;":PAGE:CHAN:SMU4:MODE V"
910     OUTPUT @Hp4155;":PAGE:CHAN:SMU4:FUNC CONS"
920     OUTPUT @Hp4155;":PAGE:CHAN:VSU1:FUNC CONS"
930     OUTPUT @Hp4155;":PAGE:CHAN:VSU1:VNAME 'VSU1'"
940     OUTPUT @Hp4155;":PAGE:CHAN:VSU2:FUNC CONS"
950     OUTPUT @Hp4155;":PAGE:CHAN:VSU2:VNAME 'VSU2'"
960     OUTPUT @Hp4155;":PAGE:CHAN:UFUN:DEL:ALL"
970     OUTPUT @Hp4155;":PAGE:CHAN:UFUN:DEF 'Q','
        ','INTEG(IB,@TIME)'"
980     OUTPUT @Hp4155;":PAGE:MEAS:SAMP"
990     OUTPUT @Hp4155;":PAGE:MEAS:SAMP:MODE LIN"
1000    OUTPUT @Hp4155;":PAGE:MEAS:SAMP:IINT "&VAL$(Duration)
1010    OUTPUT@Hp4155;":PAGE:MEAS:SAMP:POIN"&VAL$((Det_time
        /Duration)+1)
1020    OUTPUT @Hp4155;":PAGE:MEAS:SAMP:PER:AUTO ON"
1030    OUTPUT @Hp4155;":PAGE:MEAS:SAMP:CONS:SMU1 "&VAL$(VS)
1040    OUTPUT @Hp4155;":PAGE:MEAS:SAMP:CONS:SMU1:COMP 0.1"
```

```
1050      OUTPUT @Hp4155;":PAGE:MEAS:SAMP:CONS:SMU2 "&VAL$(VG)
1060      OUTPUT @Hp4155;":PAGE:MEAS:SAMP:CONS:SMU2:COMP 0.1"
1070      OUTPUT @Hp4155;":PAGE:MEAS:SAMP:CONS:SMU3 "&VAL$(VD)
1080      OUTPUT @Hp4155;":PAGE:MEAS:SAMP:CONS:SMU3:COMP 0.1"
1090      OUTPUT @Hp4155;":PAGE:MEAS:SAMP:CONS:SMU4 "&VAL$(VB)
1100      OUTPUT @Hp4155;":PAGE:MEAS:SAMP:CONS:SMU4:COMP 0.1"
1110      OUTPUT @Hp4155;":PAGE:MEAS:SAMP:CONS:VSU1 0.0"
1120      OUTPUT @Hp4155;":PAGE:MEAS:SAMP:CONS:VSU2 0.0"
1130      OUTPUT @Hp4155;":PAGE:MEAS:MSET:ITIM MED"
1140      OUTPUT @Hp4155;":PAGE:DISP:LIST:DEL:ALL"
1150      OUTPUT @Hp4155;":PAGE:DISP:LIST '@TIME','IB','Q','ID'"
1160      OUTPUT @Hp4155;":PAGE:DISP:GRAP:X:MAX "&VAL$(Det_time)
1170      OUTPUT @Hp4155;":PAGE:DISP:GRAP:Y1:NAME 'IB'"
1180      OUTPUT @Hp4155;":PAGE:DISP:GRAP:Y1:SCAL LOG"
1190      OUTPUT @Hp4155;":PAGE:DISP:GRAP:Y1:MIN -1E-12"
1200      OUTPUT @Hp4155;":PAGE:DISP:GRAP:Y1:MAX -10E-3"
1210      OUTPUT @Hp4155;":PAGE:DISP:GRAP:Y2:NAME 'Q'"
1220      OUTPUT @Hp4155;":PAGE:DISP:GRAP:Y2:SCAL LIN"
1230      OUTPUT @Hp4155;":PAGE:DISP:GRAP:Y2:MIN -1E-15"
1270      OUTPUT @Hp4155;":PAGE:DISP:GRAP:Y2:MAX -1E-6"
1250      OUTPUT @Hp4155;":PAGE:GLIS:LIST"
1260      OUTPUT @Hp4155;":PAGE:SCON:SING"
1270      OUTPUT @Hp4155;"*OPC?"
1280      ENTER @Hp4155;A
1290      OUTPUT @Hp4155;":PAGE:GLIS:MARK:DIR:X MAX"
1300      OUTPUT @Hp4155;":PAGE:GLIS:MARK:DIR:X?"
1310      ENTER @Hp4155;K
1320      OUTPUT @Hp4155;":PAGE:GLIS:MARK:DIR:Y1?"
1330      ENTER @Hp4155;IB
1340      ENTER @Hp4155;Q
1350      Idcp(Step)=ID
1360      Ibcp(Step)=IB
1370      Qcp(Step)=(Q/K)
1380      F(Step)=Freq
1390      Fh(Step)=Vgh
1400      Fb(Step)=Vgl
1410      SUBEND
1420 Init_hp4155:SUB Init_hp4155
```

```
1430      COM @Hp4155,@Form_off
1440      CLEAR SCREEN
1450      CLEAR @Hp4155
1460      OUTPUT @Hp4155;"*RST"
1470      OUTPUT @Hp4155;"*CLS"
1480      OUTPUT @Hp4155;":STAT:PRES"
1490      OUTPUT @Hp4155;"*ESE 60;*SRE 32;*OPC?"
1500      ENTER @Hp4155;A
1510      OUTPUT @Hp4155;":DISP:WIND:ALL BST"
1520      OUTPUT @Hp4155;":DISP ON"
1530      OUTPUT @Hp4155;":PAGE:GLIS:LIST:MARK ON"
1540      SUBEND
1550 Save_data:SUB Save_data
1560      COM @Hp4155,@Form_off
1570      COM /Meas_info/ REAL Duration,Det_time,Vd,Id,Ib,Vs,Vb,Vg,Ab,Amp
1580      COM /Meas_info1/ REAL Delta_v,Area,Vgh,Vgl,Vfl,Vfh,Vth,Vtl,Icp,Freq
1590      COM /Meas_data/ INTEGER Step,Loop,Ccy,Clp
1600      COM /Meas_data/ REAL Fb(1:1000),Fh(1:1000),Th(1:1000),Qcp(1:1000)
1610      COM /Meas_data/ F(1:1000),Ibcp(1:1000),Idcp(1:1000)
1620      COM /File_name/ Save_file$[12],Save_file1$[12],Ccy$[12]
1630      Save_file$="cp.TXT"
1640      CREATE Save_file$,(4*Step)
1650      ASSIGN @File TO Save_file$;FORMAT ON
1660      OUTPUT @File;"Frequency,Vgh,Vgl,Qcp,Ibcp,Idcp"
1670      FOR Clp=1 TO (Step-1)
1680      OUTPUT @File;F(Clp),Fh(Clp),Fb(Clp),Qcp(Clp),Ibcp(Clp),Idcp(Clp)
1690      NEXT Clp
1700      ASSIGN @File TO *
1710      SUBEND
```

Threshold Voltage	Linear |Vd|=0.05V		Saturation |Vd|=1V	
	N	P	N	P
N/O stack	0.348151	-0.41736	-0.02155	-0.12886
NO annealing Oxide	0.329715	-0.29527	-0.04024	-0.00377
Thermal Oxide	0.368867	-0.21238	0.015835	0.031769

Subthreshold Swing (mV/dec.)	Linear |Vd|=0.05V	
	N	P
N/O stack	74	72.9
NO annealing Oxide	74.9	72.7
Thermal Oxide	70	74.5

DIBL (V) @ |Id|=1uA Vd=0.05V&1V		
	N	P
N/O stack	0.129204	0.230554
NO annealing Oxide	0.128247	0.220497
Thermal Oxide	0.141591	0.258312

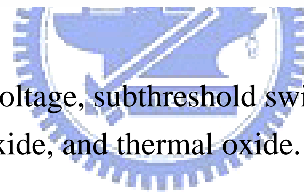


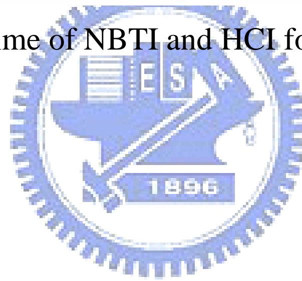
Table. 2-1. Threshold voltage, subthreshold swing, and DIBL of N/O stack, NO annealing oxide, and thermal oxide.

Dimension	after 5000 sec. Vg=2.2 stress at room temperature			
10/0.15	splits	N/O stack	NO anneal	Oxide
Vt shift (mV)		4	4	4
Dimension	after 2000 sec. Vg=Vd=2.2 stress at room temperature			
10/0.13	splits	N/O stack	NO anneal	Oxide
Vt shift (mV)		294	318	28

Table. 3-2. Comparison of Vg=2.2 and Vg=Vd=2.2V stress conditions.

Device Lifetime		
NBTI	25℃	100℃
N/O stack	2.19E+08	5883962
NO annealing Oxide	1.09E+09	52274710
Thermal Oxide	1.52E+12	1.32E+09
HCI Vg=Vd	25℃	100℃
N/O stack	5.42E+14	1.64E+12
NO annealing Oxide	1.09E+17	2.41E+11
Thermal Oxide	7.84E+15	9.29E+23
HCI Vg @ Isubmax	25℃	100℃
N/O stack	8.14E+08	109447.3
NO annealing Oxide	4.36E+17	6.59E+09
Thermal Oxide	4.71E+14	5.45E+18

Table. 3-2. Device lifetime of NBTI and HCI for 1V operation voltage.



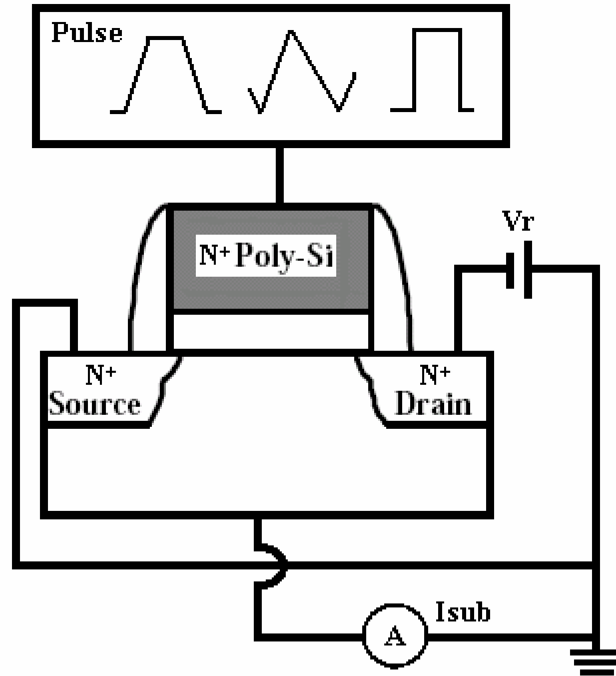


Fig. 1-1. Basic experimental setup of charge pumping measurement.

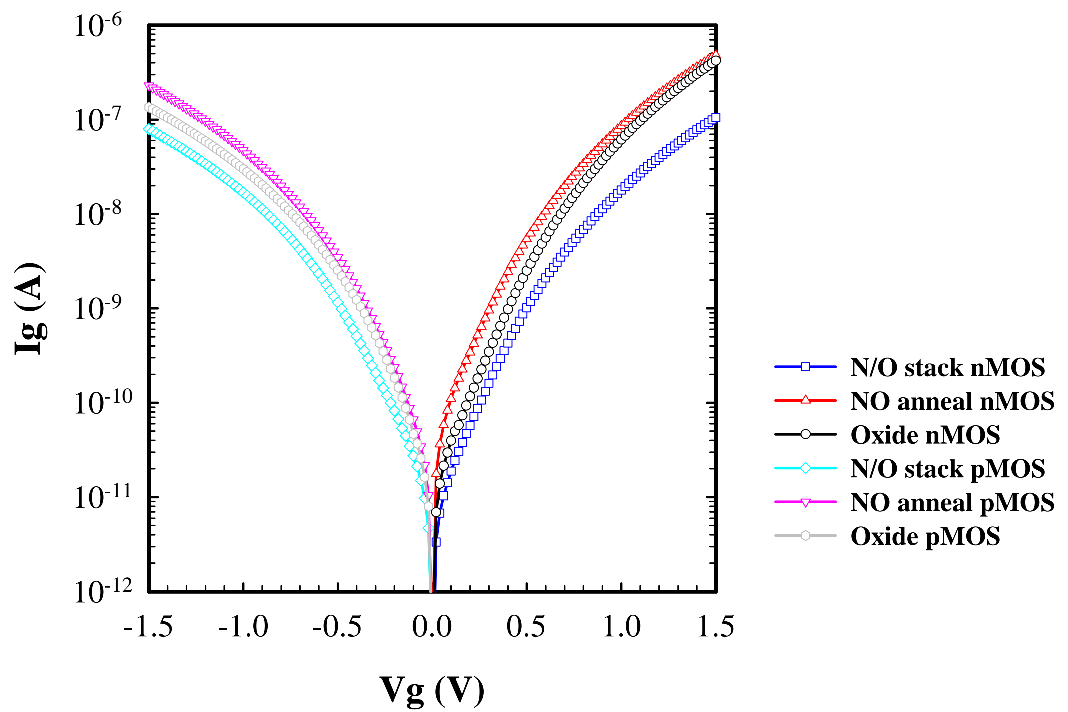


Fig. 2-1. Gate leakage current of three kinds of samples.

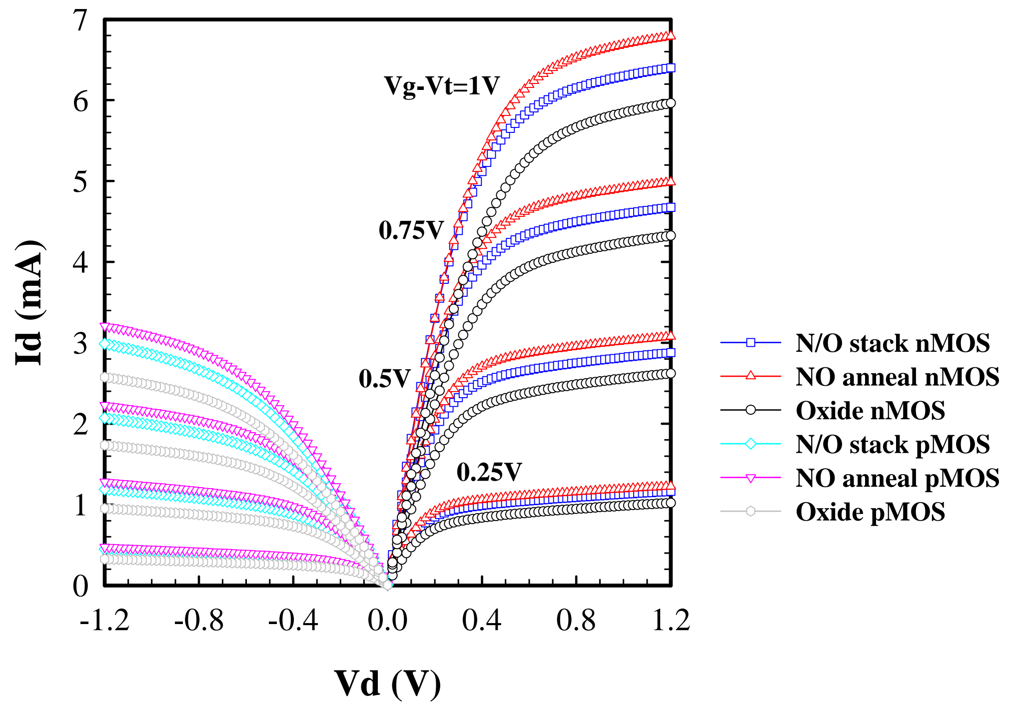


Fig. 2-2. Drain current vs. drain voltage at steps of Vg-Vt = 0.25,0.5,0.75, and 1V.

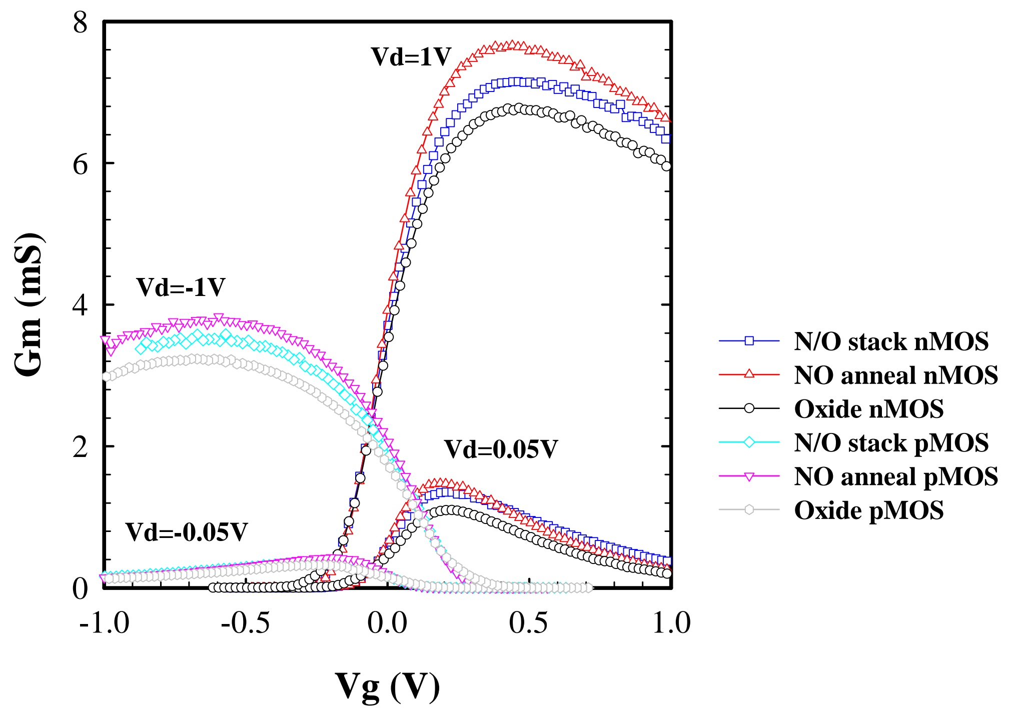


Fig. 2-3. Transconductance (Gm) vs. Vg-Vt at linear (Vd = 0.05V) and saturation (Vd = 1V) bias region.

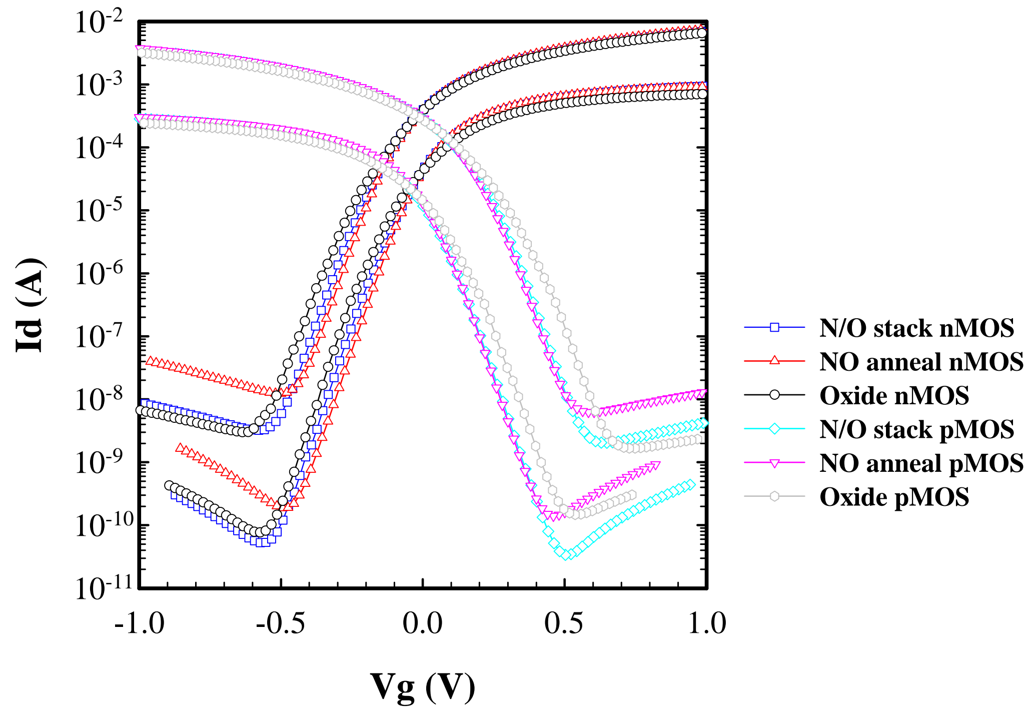


Fig. 2-4. Drain current vs. Vg-Vt at linear (Vd = 0.05V) and Saturation (Vd = 1V).

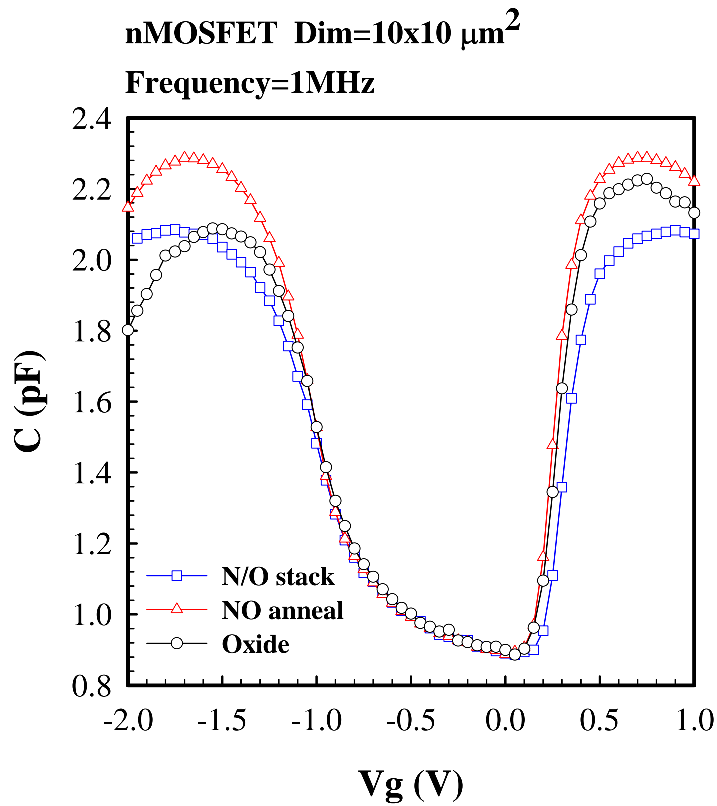


Fig. 2-5(a). C-V curves of nMOSFETs.

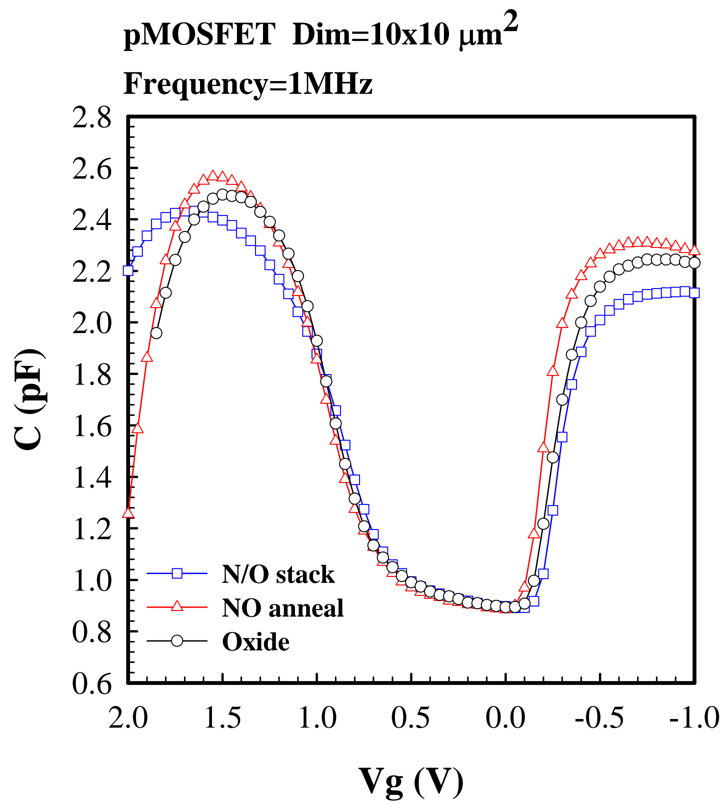


Fig. 2-5(b). C-V curves of pMOSFETs.

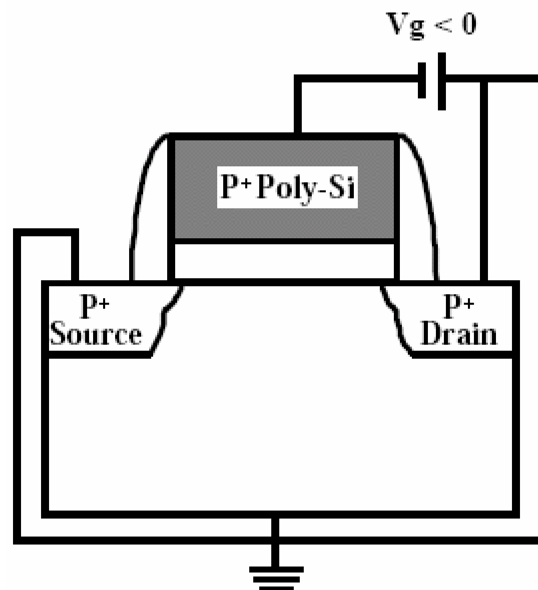


Fig. 3-1(a). Measurement setup of NBTI experiment.

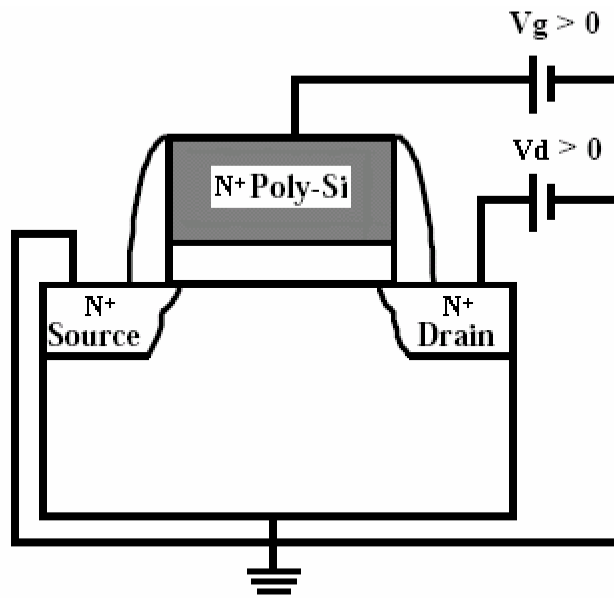


Fig. 3-1(b). Measurement setup of HCI experiment.

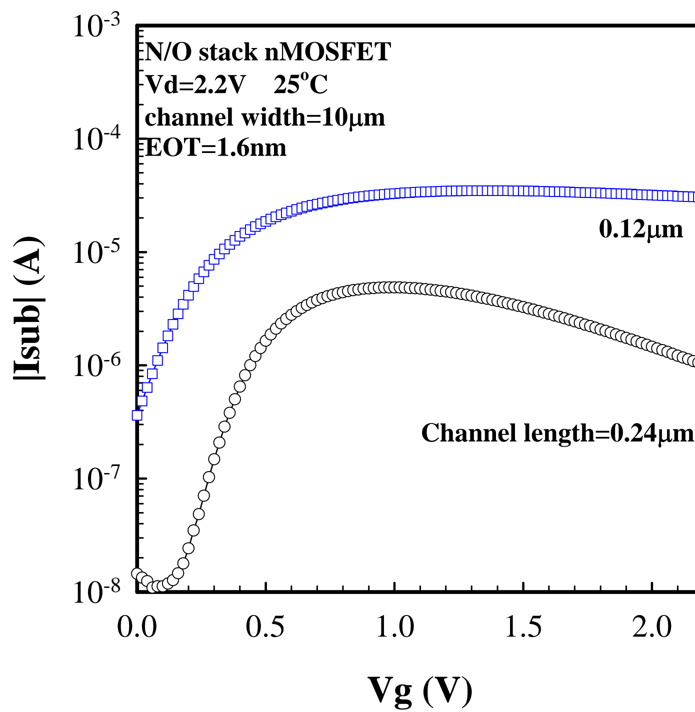


Fig. 3-2(a). Isub vs. gate voltage for N/O stack.

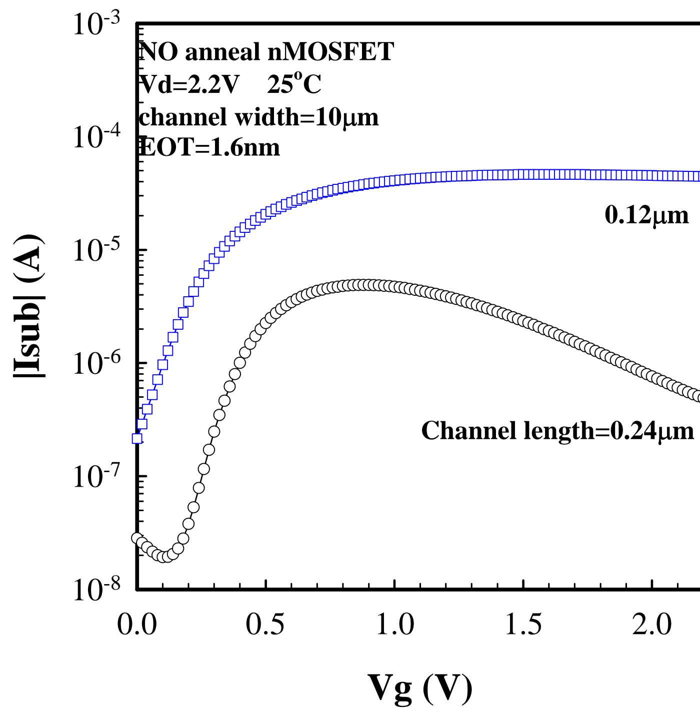
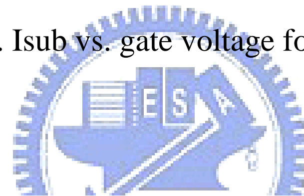


Fig. 3-2(b). Isub vs. gate voltage for NO anneal.



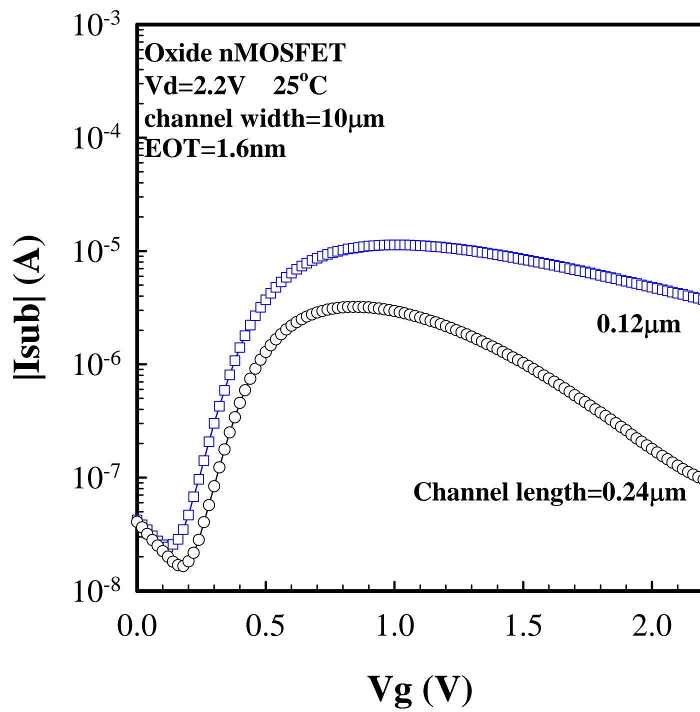


Fig. 3-2(c). Isub vs. gate voltage for oxide.

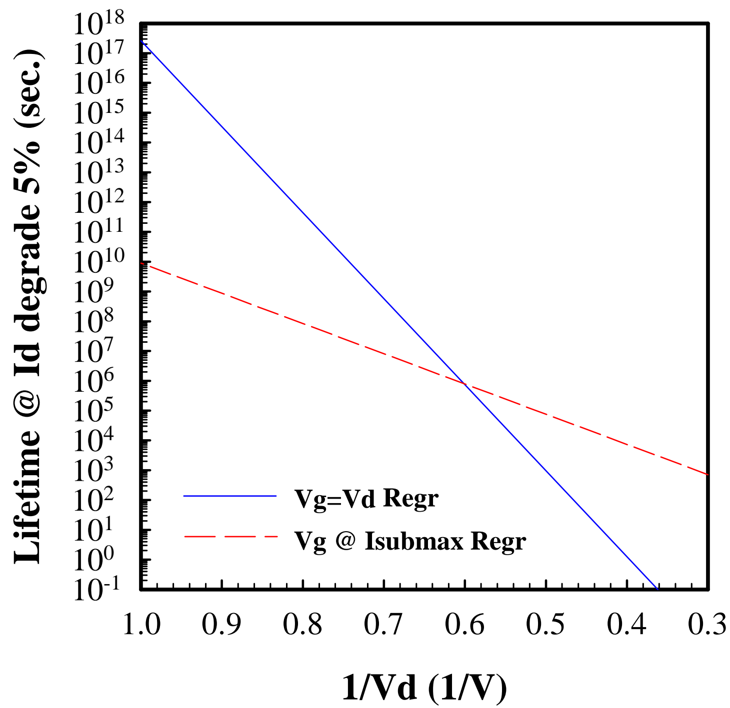


Fig. 3-3. General HCI lifetime projection of Vg = Vd and Vg @ Isubmax stress conditions.

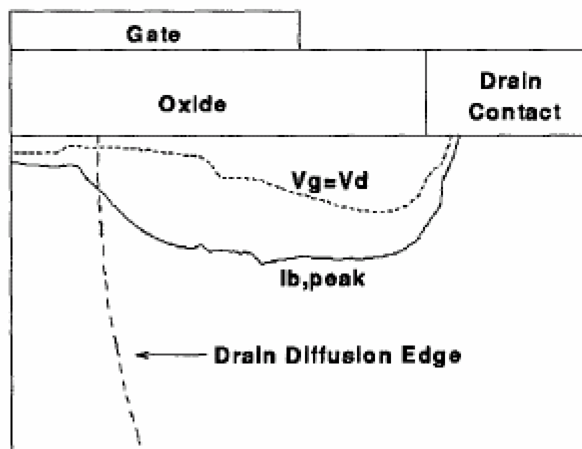


Fig. 3-4. Position of carriers at Vg=Vd and Vg @ Isubmax bias conditions.

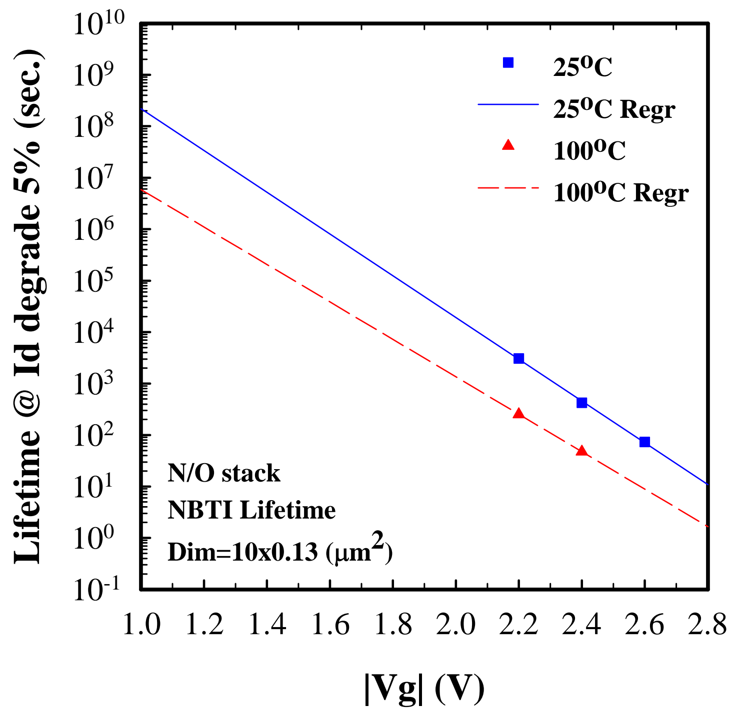


Fig. 3-5(a). NBTI lifetime projection at 25°C and 100°C of N/O stack.

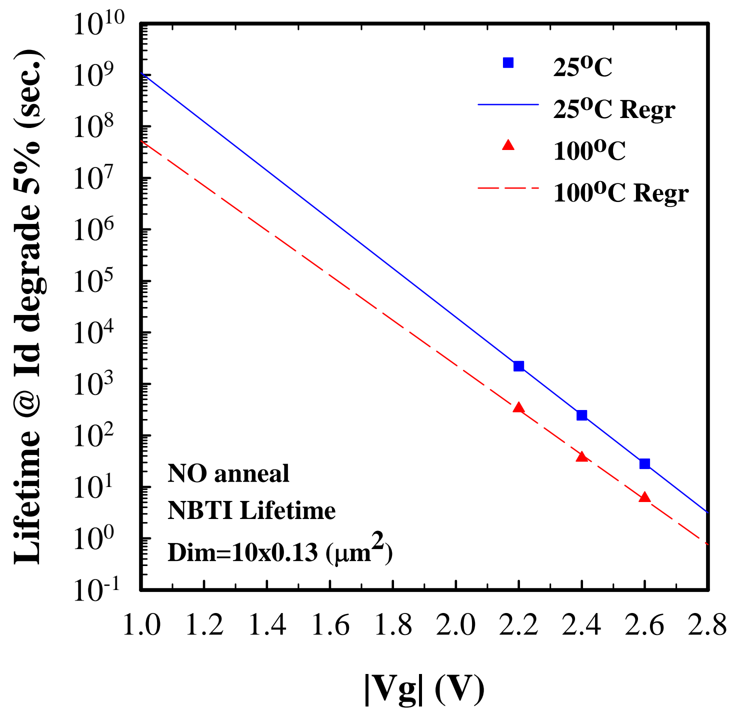


Fig. 3-5(b). NBTI lifetime projection at 25°C and 100°C of NO anneal.

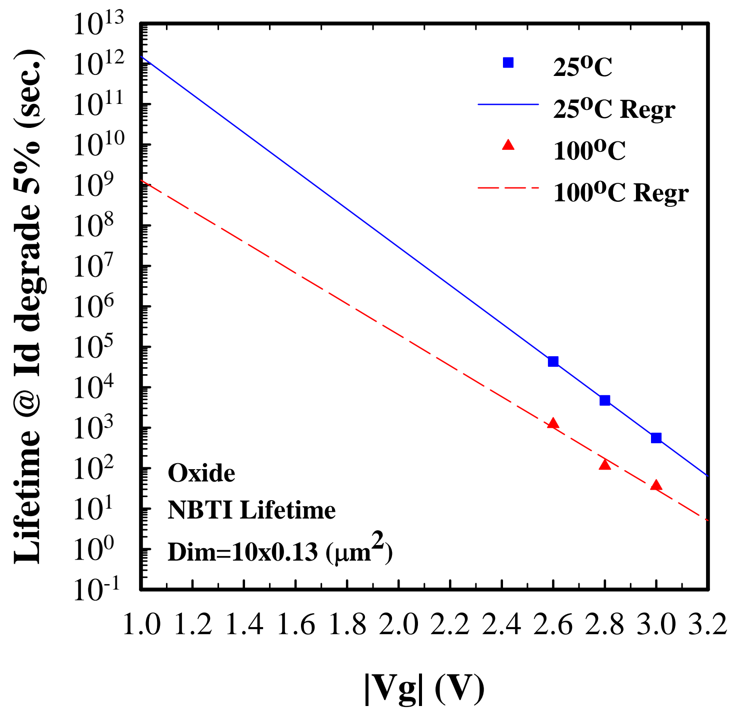


Fig. 3-5(c). NBTI lifetime projection at 25°C and 100°C of oxide.

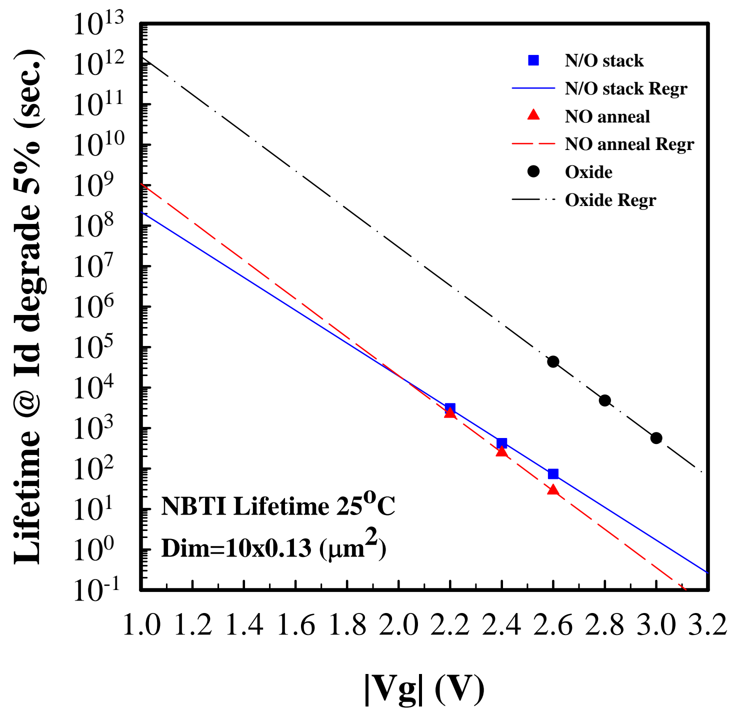


Fig. 3-6(a). NBTI lifetime projection at 25°C of three kinds of samples.

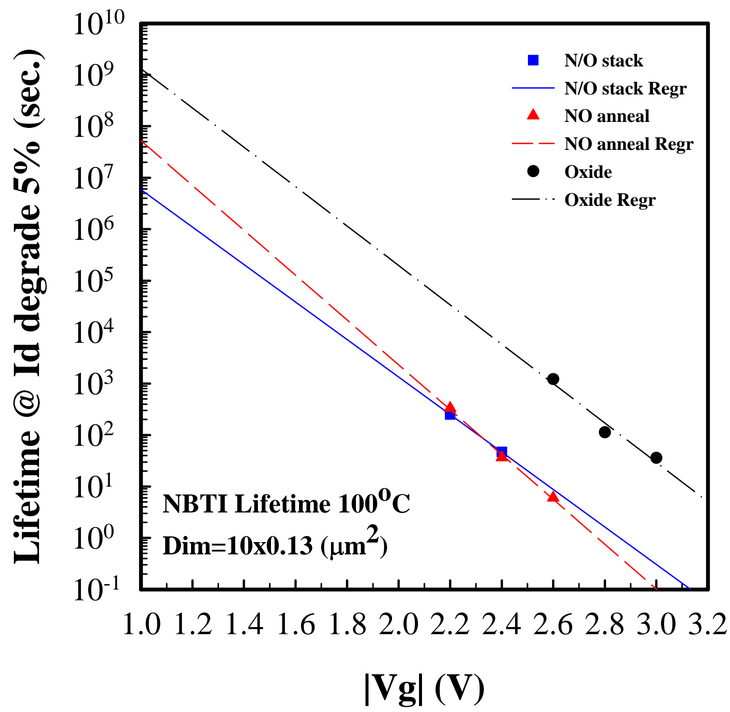


Fig. 3-6(b). NBTI lifetime projection at 100°C of three kinds of samples.

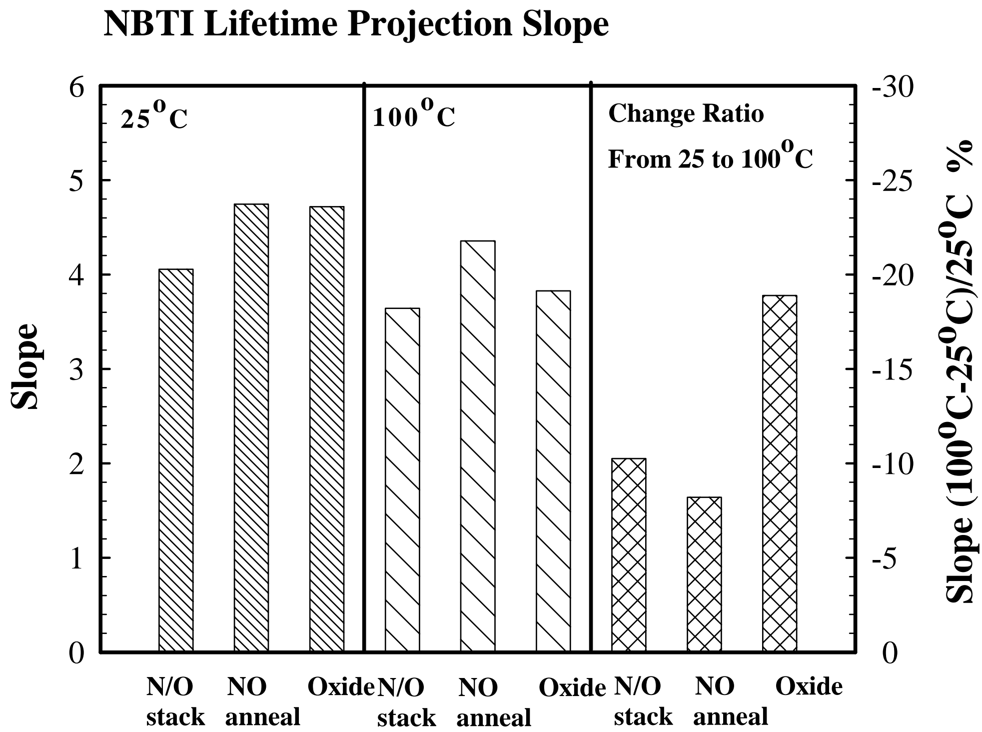


Fig. 3-7. NBTI lifetime projection slope.

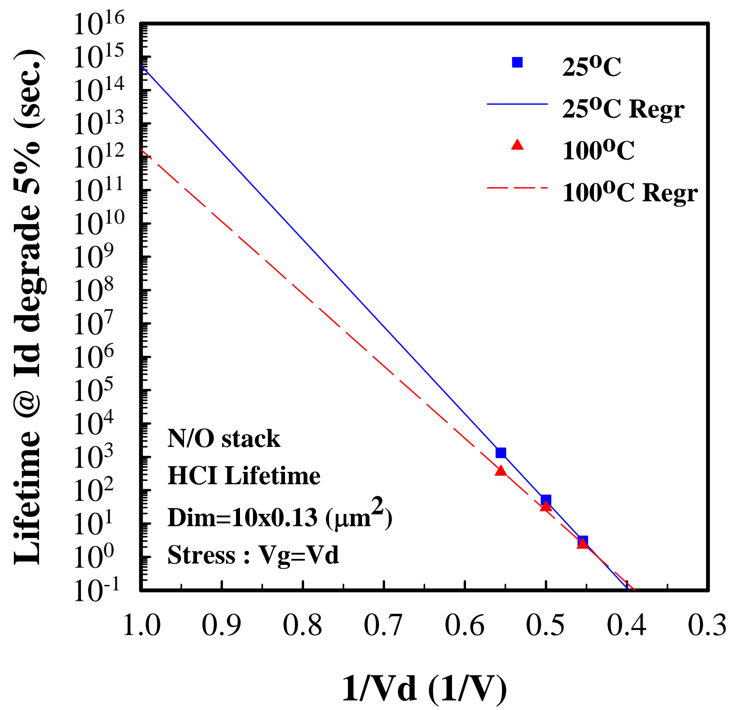


Fig. 3-8(a). HCI lifetime projection at 25°C and 100°C under Vg = Vd stress condition of N/O stack.

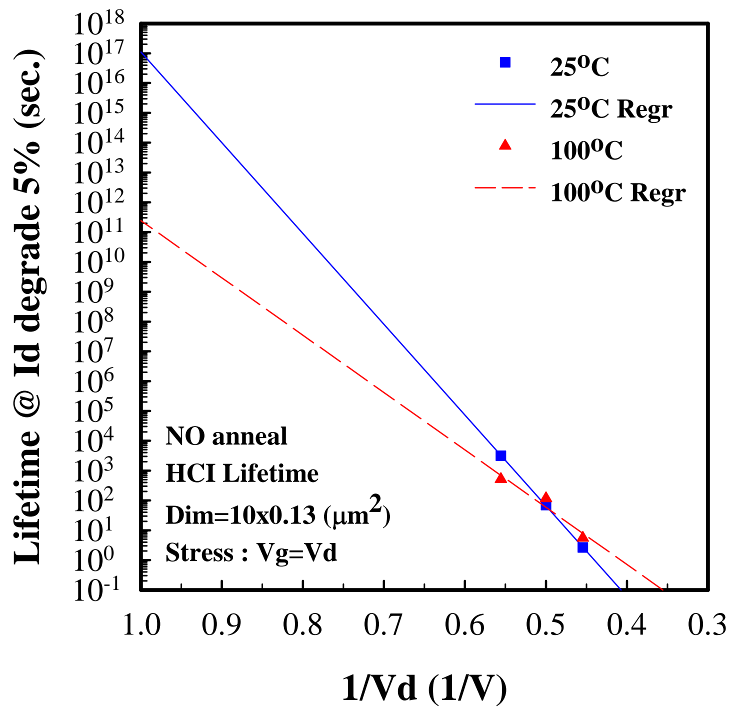


Fig. 3-8(b). HCI lifetime projection at 25°C and 100°C under Vg = Vd stress condition of NO anneal.

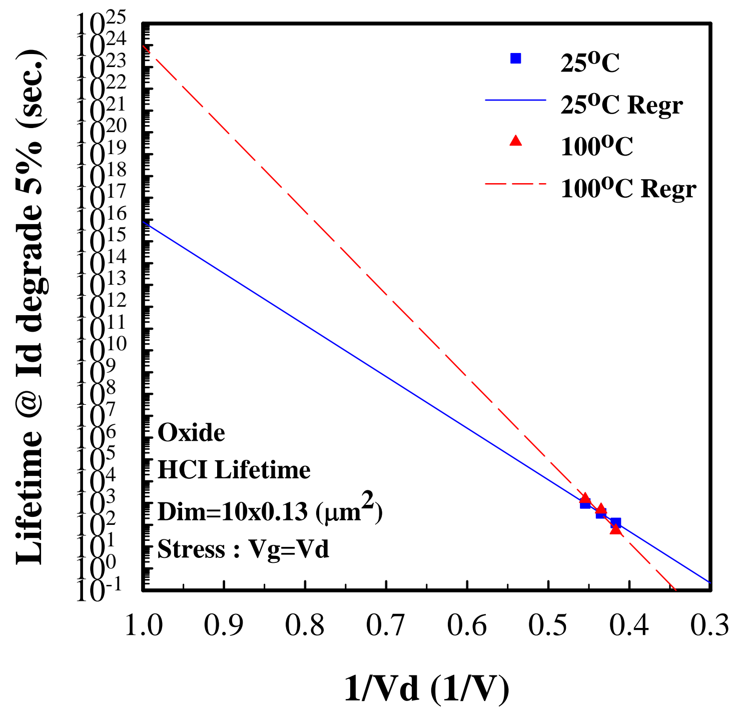


Fig. 3-8(c). HCI lifetime projection at 25°C and 100°C under Vg = Vd stress condition of oxide.

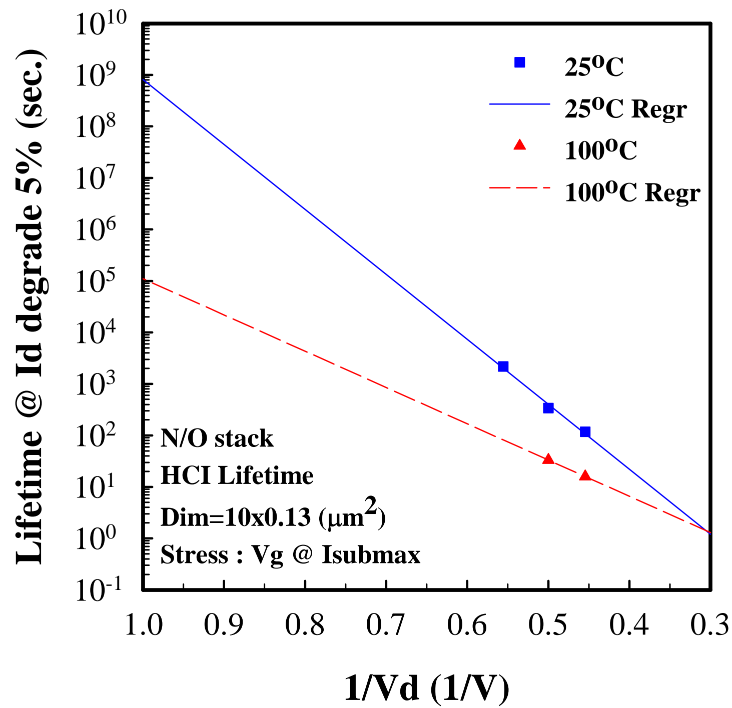


Fig. 3-9(a). HCI lifetime projection at 25°C and 100°C under Vg @ Isubmax stress condition of N/O stack.

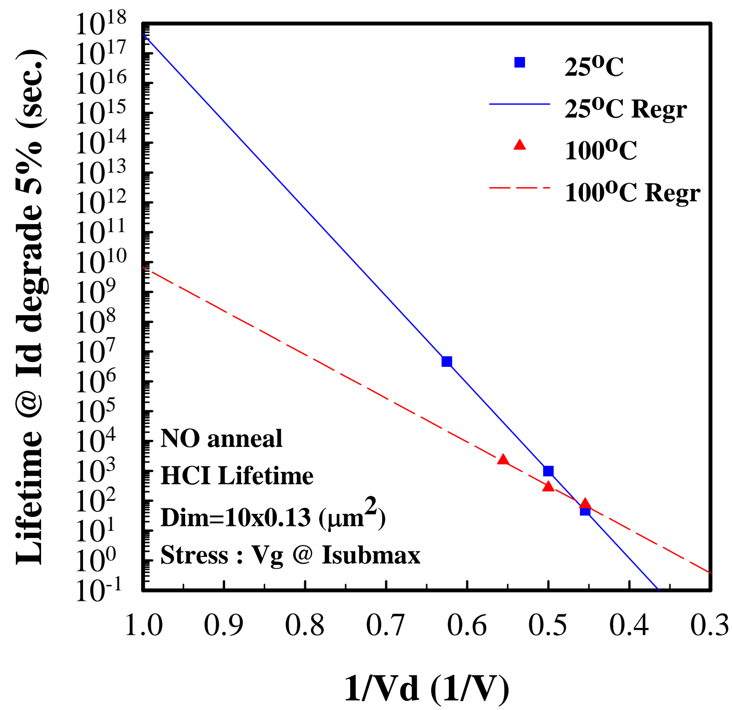


Fig. 3-9(b). HCI lifetime projection at 25°C and 100°C under Vg @ Isubmax stress condition of NO anneal.

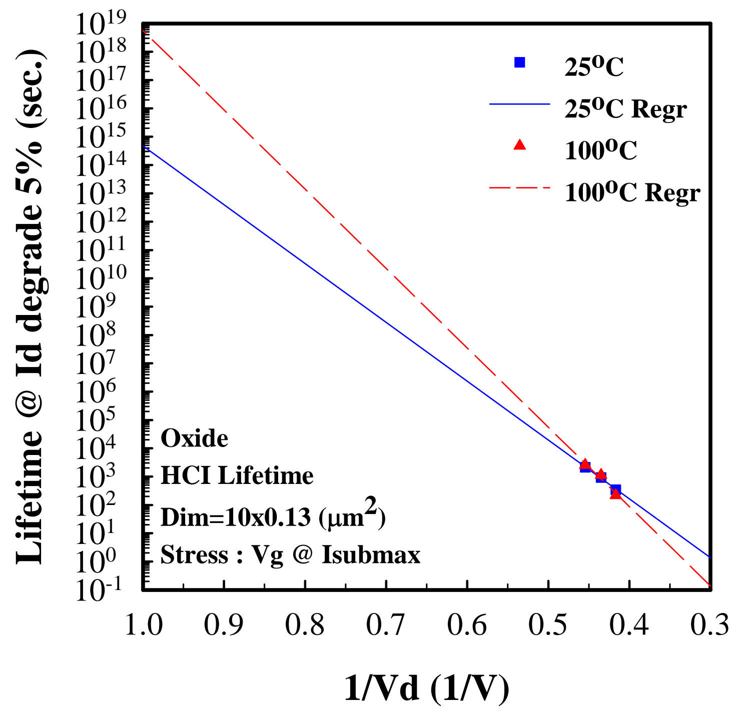


Fig. 3-9(c). HCI lifetime projection at 25°C and 100°C under Vg @ Isubmax stress condition of oxide.

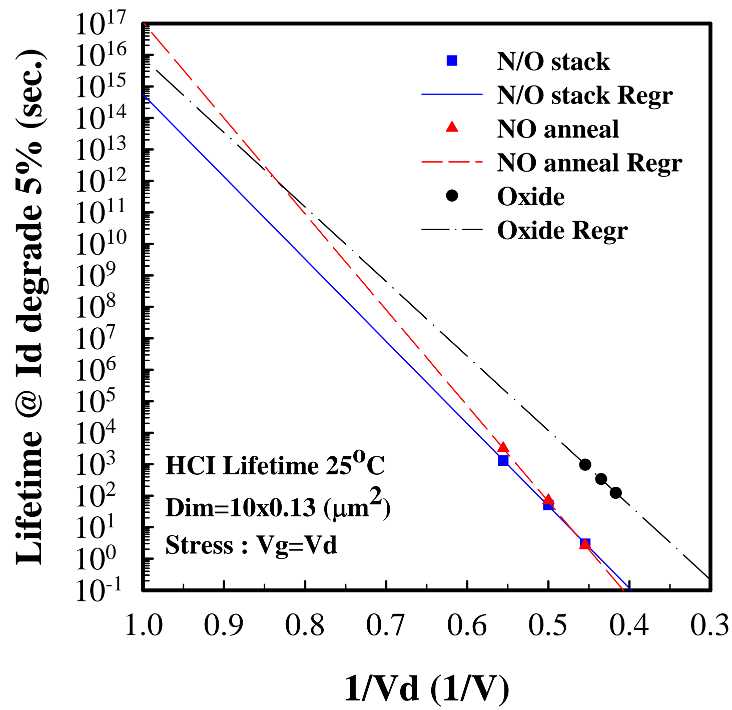


Fig. 3-10(a). HCI lifetime projection at 25°C under Vg = Vd stress condition of three kinds of samples.

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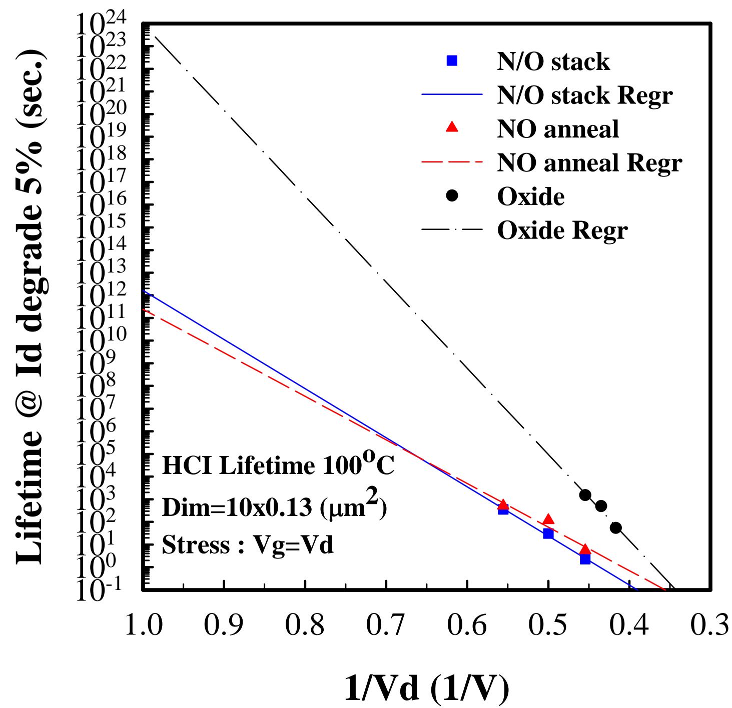

Fig. 3-10(b). HCI lifetime projection at 100°C under Vg = Vd stress condition of three kinds of samples.

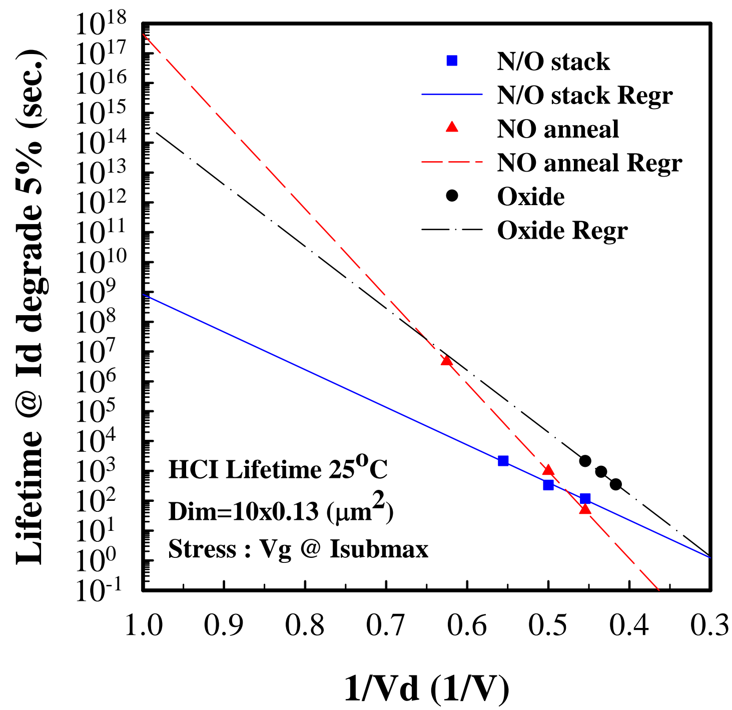

Fig. 3-11(a). HCI lifetime projection at 25°C under Vg @ Isubmax stress condition of three kinds of samples.

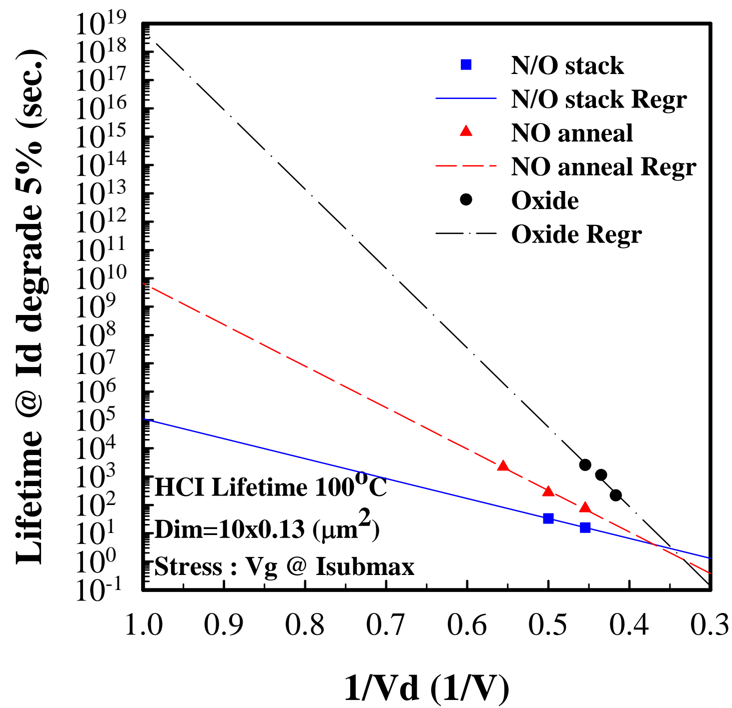

Fig. 3-11(b). HCI lifetime projection at 100°C under Vg @ Isubmax stress condition of three kinds of samples.

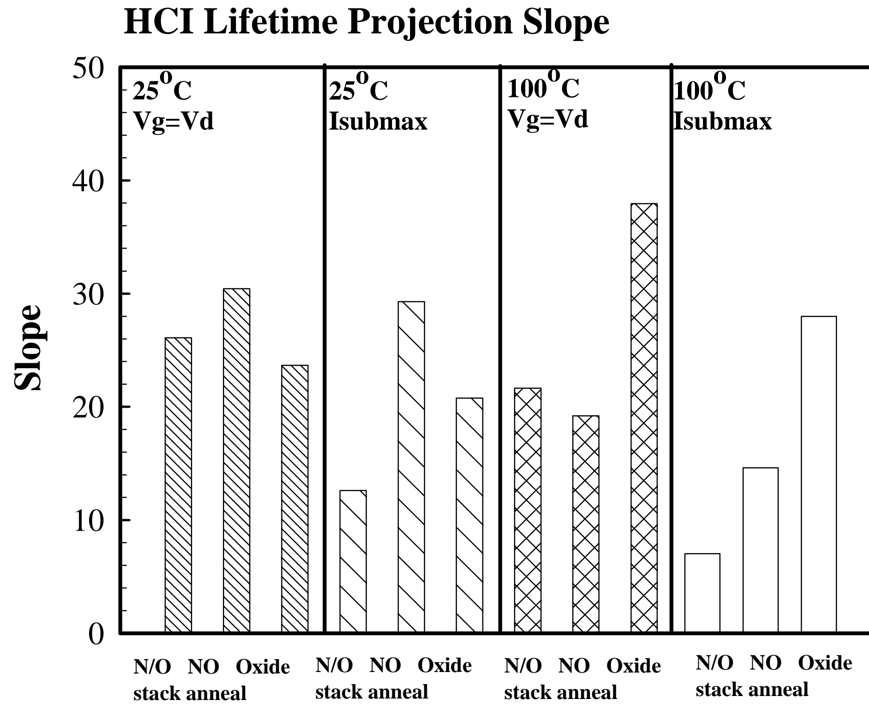

Fig. 3-12. HCI Lifetime Projection Slope at 25°C and 100°C under Vg = Vd and Vg @ Isubmax stress conditions.

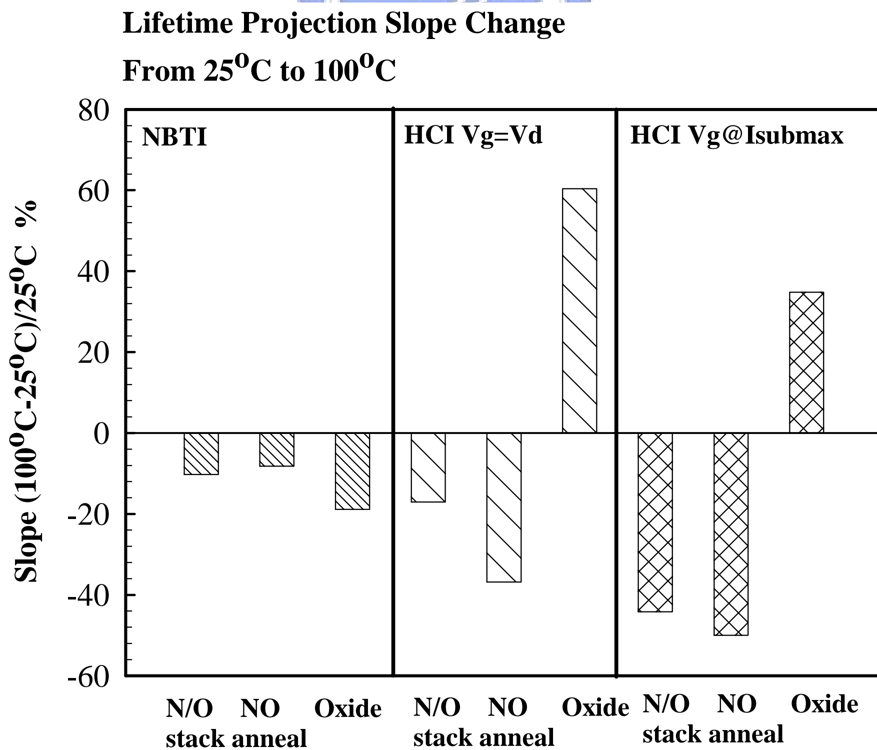

Fig. 3-12. Lifetime Projection Slope Change from 25°C to 100°C of NBTI and two stress conditions of HCI.

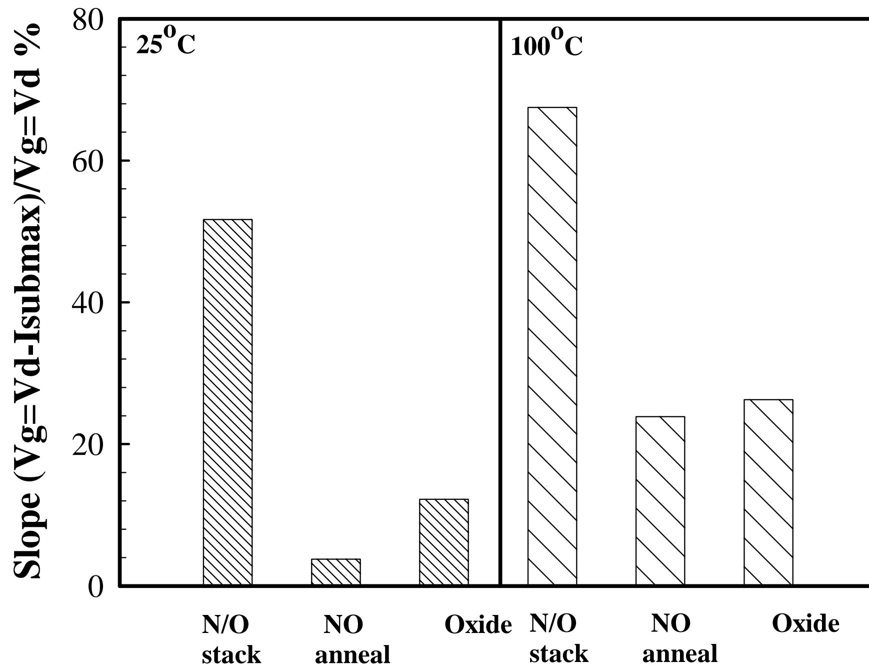

Fig. 3-14. HCI lifetime projection slope change from Vg = Vd to Vg @ Isubmax at 25°C and 100°C.

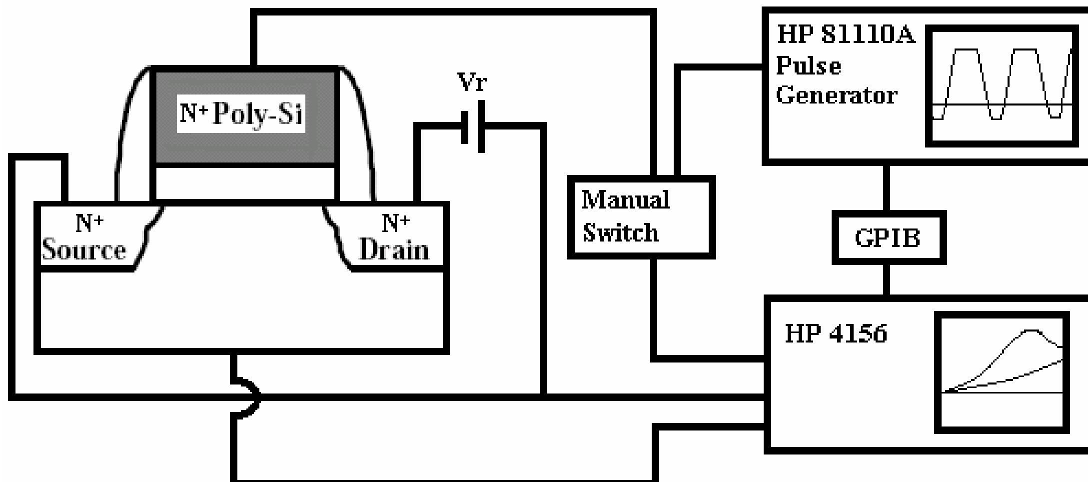

Fig. 4-1. Measurement setup in our charge pumping experiment.

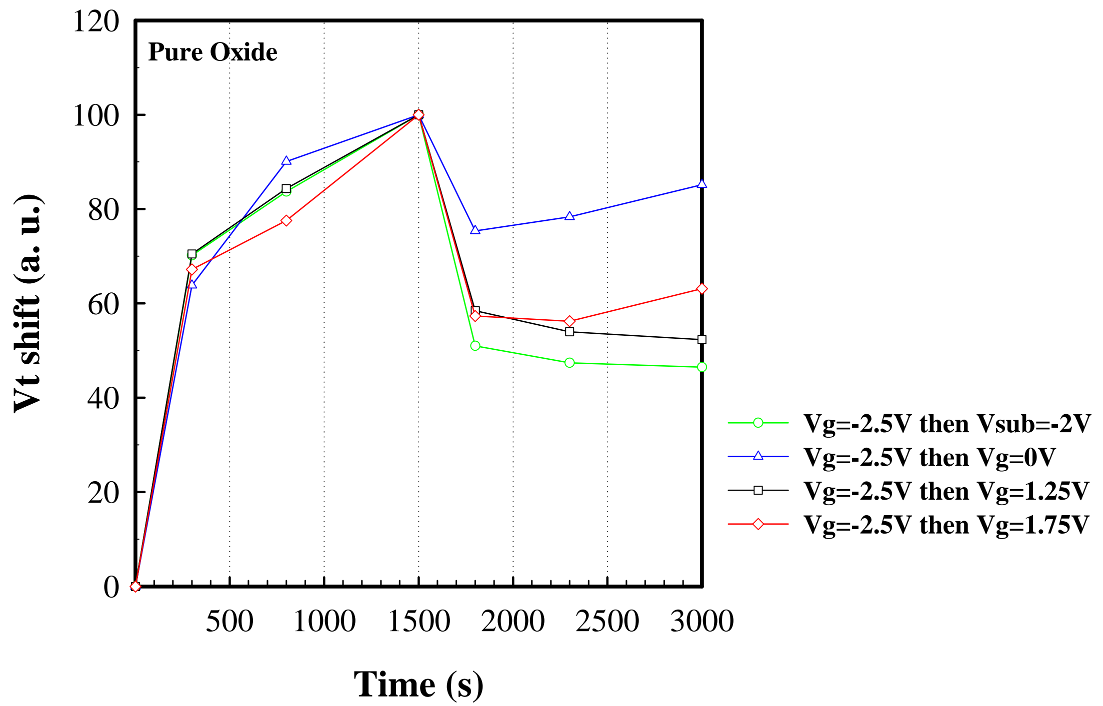

Fig. 4-2(a). Vt shift of pure oxide.

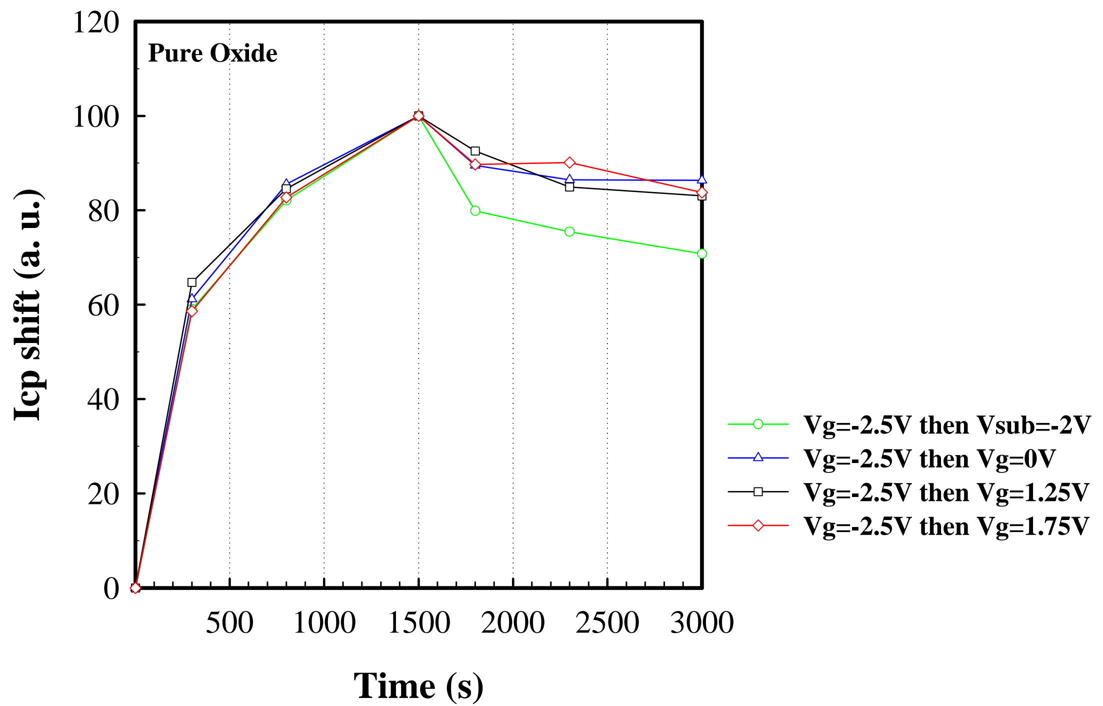

Fig. 4-2(b). Icp shift of pure oxide.

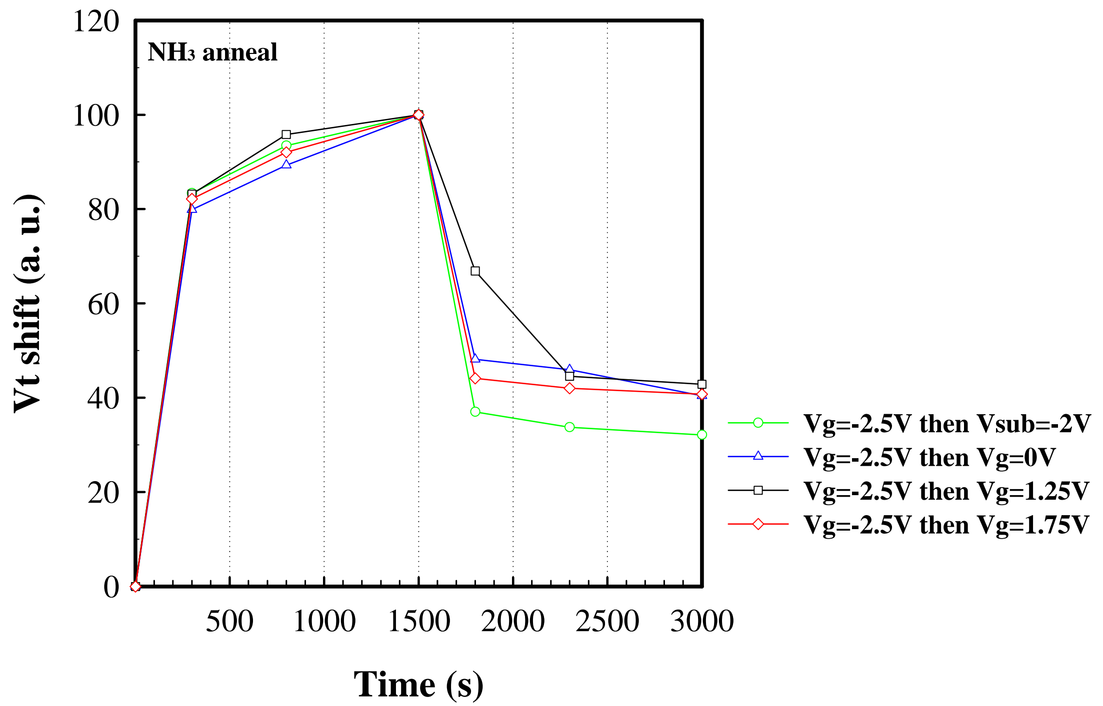

Fig. 4-3(a). Vt shift of NH_3 anneal.

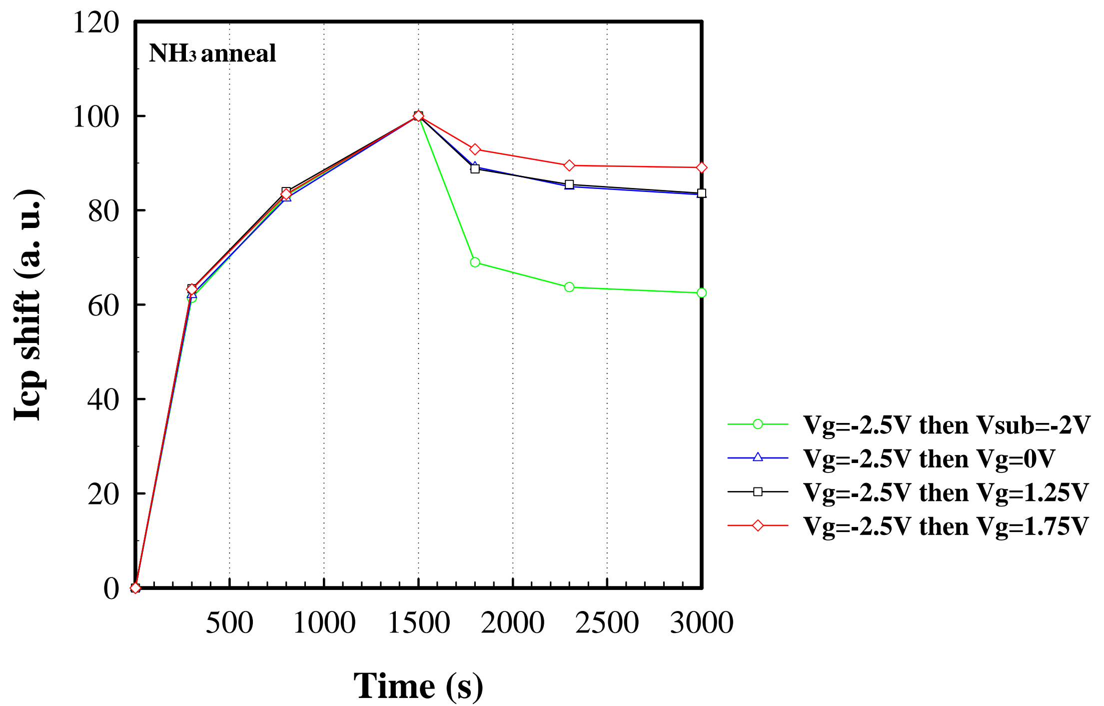

Fig. 4-3(b). Icp shift of NH_3 anneal.

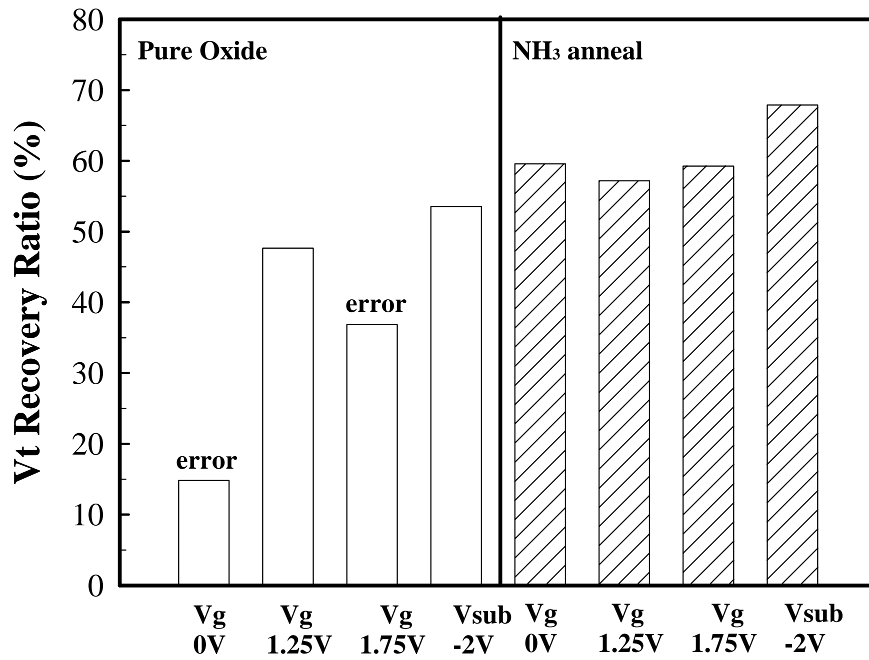

Fig. 4-4. Vt recovery ratio of pure oxide and NH_3 anneal.

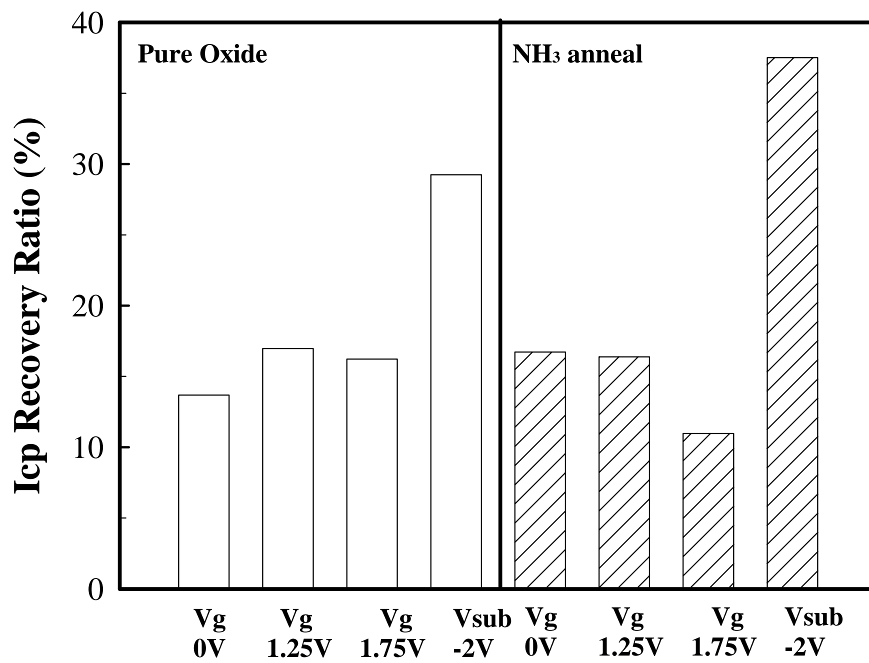

Fig. 4-5. Icp recovery ratio of pure oxide and NH_3 anneal.