國立交通大學

電子工程學系 電子研究所碩士班

碩 士 論 文

應用於無線感測網路之低電壓低功率 5-GHz 射頻前端接收電路設計

Low-Voltage Low-Power 5-GHz Receiver Front-End Circuit Design for Wireless Sensor Networks

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摘要

本篇論文的目的，主要在設計適用於低電壓操作及低功率消耗之前端接收電路，以應用於無線感測網路。共實現兩顆晶片。第一顆晶片為一低功率混頻器，藉由將轉導級與相位分離器整合的方式節省功率消耗，並且採用折疊式架構降低偏壓要求。轉導級之差動相位輸出、輸入匹配條件與雜訊輸出均加以分析。量測結果顯示，設計之混頻器消耗 2mW 功率，在 1V 偏壓下有 10.4dB 之電壓轉換增益，11dB 之輸入返迴損耗及 3.8dBm 之輸入第三階交會點。第二顆晶片為一前端接收電路，包含有低雜訊放大器、混頻器以及將此兩級交流耦合之變壓器。設計之電路如折疊式架構，適用於低偏壓操作。並且，利用變壓器將單端信號轉換為差動信號，進一步省去相位轉換所需之功率消耗。論文中針對放大器之偏壓與穩定度、變壓器操作於共振模式，產生電流耦合增益之條件，均加以分析設計。量測結果顯示，此前端電路在 0.6V 偏壓下有 12dB 的電壓轉換增益，16.9db 之輸入返迴損耗以及-2.8dBm 之輸入第三階交會點，而此電路之功率消耗僅有 0.29mW。

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ABSTRACT

This thesis aims at design of a low-voltage low-power receiver front-end circuit applicable to wireless sensor networks. Two chips are realized. In the first chip, a low-power double-balanced mixer is designed in a folded topology. A transconductance stage with phase splitting function which is composed of a common-gate and common-source transistors is adopted for low power consideration. Output balanced condition, input matching, and noise of the transconductance stage are analyzed. Realized in 0.18-um CMOS technology, the measured input return loss and voltage conversion gain are 11dB and 10.4dB, respectively. The input third-order intercept point (IIP3) is 3.8dBm while consuming 2mW from a 1V supply.

In the second chip, a receiver front-end circuit is designed for low supply voltage as low as 0.6V. The circuit consists of a low noise amplifier, switching stage, and on-chip transformer which provides AC coupling between stages connected to it in a folded structure. The transformer is designed not only to convert single-ended signal

into differential form without excess power consumption, but also to operate in resonant mode to have current transfer gain. The power consumption of the circuit is effectively cut down. Also, a figure of merit for bias consideration and stabilization design for LNA is analyzed for the optimum design condition under low supply voltage case. The measured input return loss and voltage conversion gain are 16.9dB and 12dB, respectively. The input third-order intercept point (IIP3) is -2.8dBm while consuming only 0.29mW from a 0.6V supply.

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Chapter 1

Introduction

1.1 Wireless Sensor Networks

Wireless sensor networks are emerging as an attractive solution for health monitoring, or said personal body area network (BAN) [1]. The network consists of a number of miniature sensor nodes connected wirelessly together, among which a central node collects all the data and then transmits to outside world using a standard telecommunication infrastructure such as Wireless Local Area Network (WLAN) or cellular phone network as shown in Fig. 1-1. To realize widespread adoption of the networks, some critical obstacles have to be conquered. One major bottleneck is lifetime requirement. The wireless nodes must offer reliable data delivery for at least 10m indoor range, while achieving several years lifetime from carried batteries.

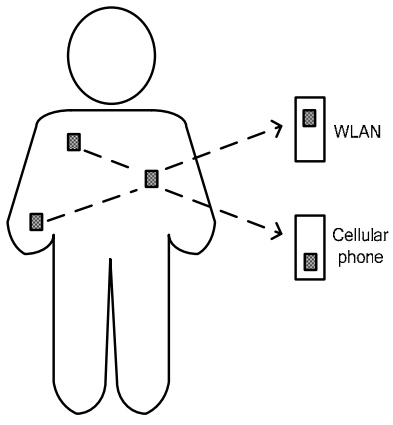


Fig. 1.1 Diagram for personal body area network.

1.2 Motivation

Extremely low power consumption is the key requirements for wireless sensor networks since lifetime measured in years constrains average power consumption to 10uW or so [2]. For low data rate sensors, a duty cycle around 1% limits radio power consumption to approximately 1mW. The supply voltage of button cell batteries is about 1.0-1.5V and that of a single solar cell is 0.4V. Circuits must be designed to suit for the low supply voltage requirement. And the power consumption of the circuits must be as low as possible to allow a long lasting use without battery replacement. As far as power consumption is concerned, RF front-end circuit typically consumes much more than that of the other circuits in the transceiver system. Therefore, a low supply voltage and low power consumption RF front-end circuit is worth of great effort.

When supply voltage goes down, the conventional cascode topology is not suitable for its stacked structure. Folded cascode structure is so selected for low voltage consideration with the form of LC tank and transformer AC coupling. To save power consumption of the phase splitting stage which usually appears in circuit, a transconductance stage merged with phase splitting function and a passive balun, transformer, with current gain are designed. All the efforts in the thesis are to realize a low-voltage and low-power front-end circuit while trade little of the circuit performance.

1.3 Thesis Organization

In Chapter 2, fundamentals about noise theory and stability considerations in RF design will be introduced. In Section 2.1 the basics including the noise model of MOSFET, noise factor, and optimum source impedance are introduced. The stability concept about amplifier design is discussed in Section 2.2.

In Chapter 3, the design of a low-power double-balanced mixer is presented. The output balanced condition and noise analysis are given in Section 3.2. In Section 3.3 and 3.4, described are the design for folded structure and mixing pairs, respectively. In Section 3.5, the implementation and measured result of the mixer is presented. A short conclusion of this mixer is given in Section 3.6.

Chapter 4 presents the design of a low-voltage low-power receiver front-end circuit. In Section 4.2, the design consideration for a LNA is proposed. The I-V curve of MOSFET, a figure of merit for bias design, and stabilization of LNA are included. Section 4.3 discusses the design consideration of mixing stage. Section 4.4 relates to the transformer design. The equivalent model for the transformer, resonant operation derivation and analysis, and the design of physical dimension of the transformer are all discussed. Section 4.5 reports the implementation and measured result of the circuit. Section 4.6 is a conclusion of this front-end circuit. A summary of the thesis and future work on this topic are given in the last chapter, Chapter 5.

Chapter 2

Fundamentals in RF Design

2.1 Noise Basic

2.1.1 Noise Model of MOSFET

Thermal noise is a consequence of Brownian motion: thermally agitated charge carriers in a conductor contribute a randomly varying current that give rise to a random voltage which has a zero average value, but a nonzero mean-square value. The noise of a resistor can be modeled as a noise voltage generator in series with the resistor itself or a noise current source shunting the resistor with value given as $\overline{v_n^2} = 4kTR\Delta f$ and $\overline{i_n^2} = \frac{4kT\Delta f}{R}$, respectively. Because the noise arises from the random agitation of charge in the conductor, the noise does not have a particular constant polarity and the polarity in model is simply a references.

Since MOSFET is essentially a voltage-controlled resistor, it exhibits thermal noise. The dominant noise source in CMOS devices is channel thermal noise. The expression for this drain current noise of MOSFET is given by [3]

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f \tag{2-1}$$

where γ is bias-dependent factor, and g_{d0} is the zero-bias drain conductance of the

device. γ is one for zero V_{DS} and decreases toward 2/3 in saturation in long channel devices.

Another source of drain noise is flicker noise which is usually explained by charge trapping phenomena [3]. The trapping times by some types of defects and certain impurities especially at the surface are distributed in a way that can lead to a 1/f noise spectrum. Larger MOSFETs exhibit less 1/f noise because the large gate capacitance smoothes the fluctuation in channel charge. The 1/f drain noise source is given by [3]

$$\overline{i_{nd}^2} = \frac{K}{f} \cdot \frac{g_m^2}{WLC_{ox}^2} \cdot \Delta f \tag{2-2}$$

where K is a device-specific constant. For PMOS, K is typically about 1/50 times of that of NMOS.

For frequency as high as radio frequencies, the thermal agitation of channel charge leads to a non-negligible amount of noisy gate current to the MOSFET. The gate noise is produced by the fluctuations in the channel charge that induce a physical current in the gate terminal due to capacitive coupling. This source of noise is modeled as a shunt current source between gate and source terminal with a shunt conductance g_g, and may be expressed as [3]

$$\overline{i_{ng}^2} = 4kT\delta g_g \Delta f \tag{2-3}$$

where $g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}}$ and δ is the gate noise coefficient, classically equal to 4/3 for long-channel devices while 4 to 6 in short channel one. Since the gate noise and

channel thermal noise both stem from the thermal fluctuations in the channel, they are correlated with each other. The magnitude of the correlation can be expressed as [4]

$$c \equiv \frac{\overline{i_g \cdot i_d^*}}{\sqrt{\overline{i_g^2} \cdot \overline{i_d^2}}} \approx -0.395\,j \tag{2-4}$$

where the value of -0.395j is exact for long channel devices. The gate noise can then be expressed as the sum of two components, one of which is fully correlated with the drain noise and the second of which is uncorrelated with the drain noise. It is

$$\overline{i_{ng}^2} = \overline{(i_{ngc} + i_{ngu})^2} = 4kT\delta g_g \Delta f \,|\, c \,|^2 + 4kT\delta g_g \Delta f\,(1 - |\, c \,|^2) \tag{2-5}$$

Fig. 2.1 depicts a standard MOSFET noise model. In this model, several noise sources mentioned are included: $\overline{i_{nd}^2}$ is the drain noise source, $\overline{i_{ng}^2}$ is the gate noise source, and $\overline{v_{rg}^2}$ is thermal noise source of gate parasitic resistor r_g.

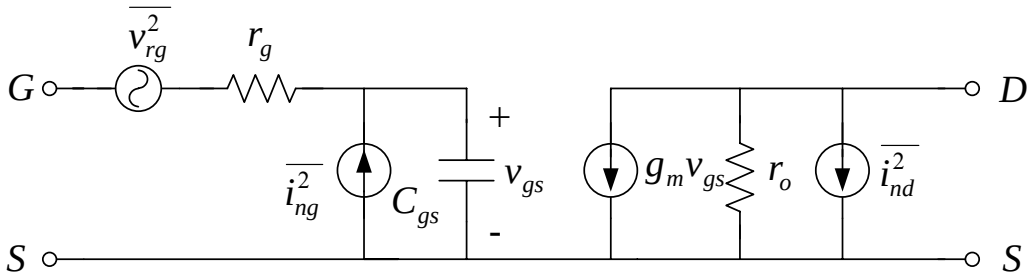


Fig. 2.1 A standard noise model of MOSFET.

2.1.2 Noise Factor of a Tow-Port Network

Noise factor F is a useful measure of the noise performance of a system. It is defined as the ratio of the available noise power P_{no} at its output divided by the product of the available noise power at its input P_{ni} times the networks's numeric gain G or equivalently defined as the ratio of the signal to noise power at the input to the signal to noise power at the output [5]. Thus

$$F = \frac{P_{no}}{P_{ni}G} = \frac{S_i / N_i}{S_o / N_o} \tag{2-6}$$

The noise factor is a measure of the degradation in signal to noise ratio due to the noise from the system itself. Since the noise factor relates to the input noise power, a standardized definition of noise source has been setup: a resistor at 290K. A more general expression of noise factor NF is called noise figure which is just noise factor expressed in decibels:

$$NF = 10\log F \tag{2-7}$$

When several networks are cascaded each having its own gain G_i and noise factor F_i, the total output noise is composed of all the noise from each stage but with different amount of contribution to the noise performance. The noise factor of a cascade networks is given as

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_2} + \ldots \tag{2-8}$$

From (2-8), the noise factor of the first stage is most critical and must be keep as

low as possible and the gain of it should be as large as possible to suppress the noise of the following stage. The result is intuitive since the noise's interference has less effect when the signal level is high.

2.1.3 Optimum Source Impedance for Noise Design

The noise factor of a two port network can be given as [5]

$$F = F_{\min} + \frac{4R_n}{Z_o} \frac{|\Gamma_s - \Gamma_{opt}|}{(1-|\Gamma_s|^2)|1+\Gamma_{opt}|^2} \tag{2-9}$$

where Rn is the correlation resistance which tells us the relative sensitivity of the noise figure to departures from the optimum conditions and Z_o is the characteristic impedance of the system. This equation expresses that there exists an optimum source reflection coefficient, Γ_{opt}, or equivalently an optimum source impedance, Z_{opt}, at the input of the network in order to deliver lowest noise factor, $F_{\min}$. The value of Γ_s that provides a constant noise factor value forms non-overlapping circles on the Smith chart. It is usually the case that the optimum noise performance trades with the maximum power gain.

2.2 Amplifier Stability

The stability of an amplifier, or its resistance to oscillate, is a very important consideration in a design and can be determined from the S parameters, the matching networks, and the terminations [6]. The non-zero S_{12} parameter of a two port networks as shown in Fig. 2.2 provides a feedback path by which the power transferred to the output can be feedback to the input and combined together. Oscillation may occur when the magnitude of reflection coefficient Γ_{IN} or Γ_{OUT}, defined as the ratio of the reflected to the incident wave, exceeds unity. It is expected that a properly designed amplifier will not oscillate no matter what passive source and load impedances are connected to it [5], which is said to be unconditionally stable and the reflection coefficient is given as

$$|\Gamma_{IN}| = |S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}| < 1$$
$$|\Gamma_{OUT}| = |S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s}| < 1 \qquad (2\text{-}10)$$

A network that has $\Gamma_{IN} > 1$ or $\Gamma_{OUT} > 1$ for certain load impedance is said to be conditionally stable. In such a case, input and load stability circles, the contour of $\Gamma_{IN} = 1$ and $\Gamma_{OUT} = 1$ for certain frequencies on the Smith chart, are useful to fine the boundary line for load and source impedances that cause stable and unstable condition. The stability circles can be calculated directly from the S parameters of the two port network, so another convenient parameter, stability factor K, is defined and given as

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{2-11}$$

where

$$|\Delta|^2 = |S_{11}S_{22} - S_{12}S_{21}|^2$$

The amplifier is unconditionally stable provided that

$$K > 1 \quad \text{and} \quad |\Delta|^2 < 1 \tag{2-12}$$

or equivalently

$$K > 1 \quad \text{and} \quad B_1 < 1 \tag{2-13}$$

where $B1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2$.

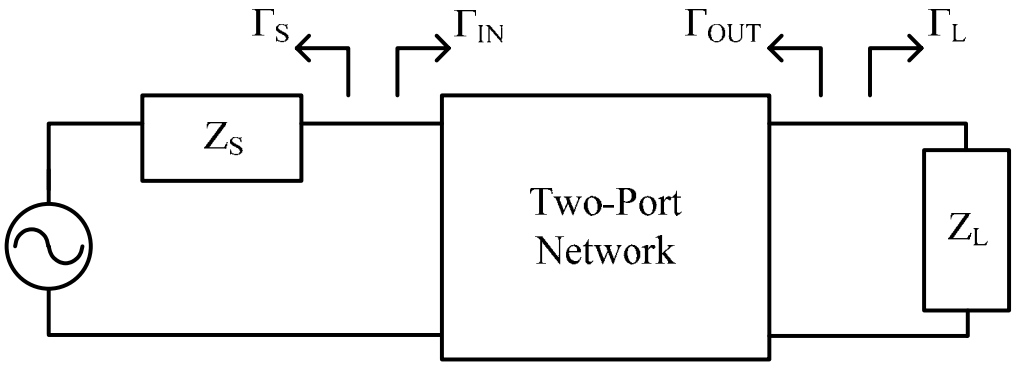


Fig. 2.2 Stability of two-port networks embedded between source and load.

Chapter 3

Low Power Double-Balanced Mixer

3.1 Introduction

Mixer is an essential part of RF front-end circuits. Double balanced type mixer is more desirable than single-ended one for its better port-to-port isolation and even-order terms rejection. The received signal from the antenna is usually single ended. A phase splitter is needed to transform the signal from the proceeding stage, low noise amplifier (LNA), into a differential form to benefit from the double-balanced structure. To avoid unwanted signal loss, an active phase splitter is usually adopted [7][8]. However, the active phase splitter contributes limited gain and consumes lots of power. Therefore, in this work the phase splitter and transconductance stage are combined to a single stage to largely save power consumption. It consists of common gate and common source transistors which is claimed in [9] to have averagely good performance over other inspected types. The output balanced condition, the input matching, and the noise performance of the transconductance stage has been analyzed. PMOS switching stage with large size has bee selected for performance consideration.

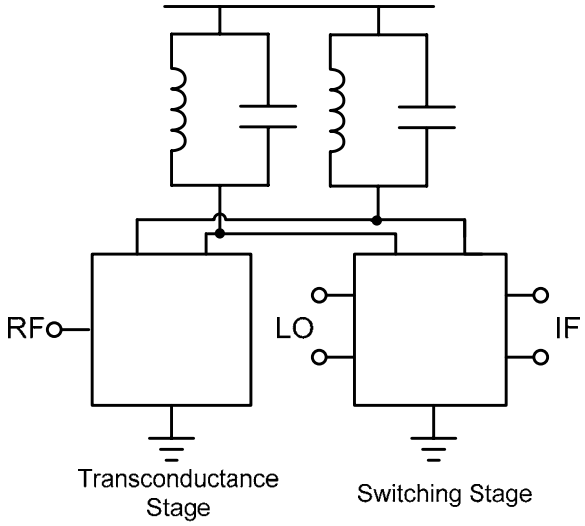


Fig. 3.1 Circuit Architecture of mixer.

The mixer under consideration is composed in an LC folded cascode structure [10] as shown in Fig. 3.1. Folded structure is a good configuration for low supply voltage and provides enough voltage headroom for transistors. The proposed structure of the mixer can not only meet the 1V supply requirement but also allow further reduction in the supply voltage level. Moreover, LC resonating removes unwanted harmonic signals so the linearity can be improved.

3.2 Transconductance Stage

3.2.1 Balanced Output Design

The transconductance stage consists of two transistors, a common gate transistor M_1 and a common source transistor M_2 as shown in Fig. 3.2(a). The RF input signal V_i is transformed into differential current by M_1 and M_2, respectively. The output differential current is then connected to the switching stage for current commutation, which loads the transconductor stage and makes the current into voltage V_{o1} and V_{o2} at drain nodes. In the analysis, the parasitic capacitance C_{gd1} and C_{gd2} are not neglected and r_{o1} and r_{o2} are also taken into consideration.

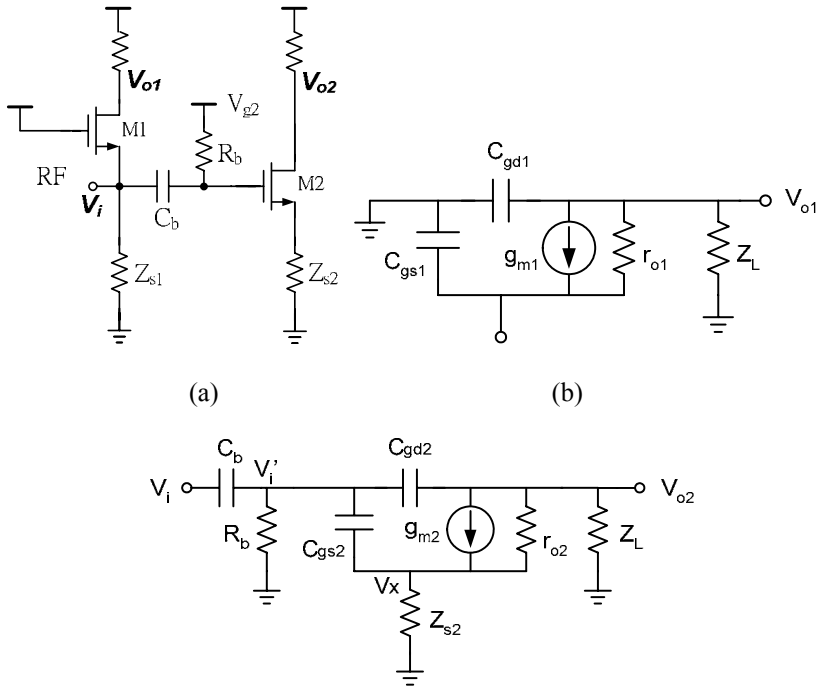


Fig. 3.2 Common-gate common-source transconductance stage (a) schematic (b) small signal model of common gate and (c) common source parts.

Applying KCL to the small signal models shown in Fig. 3.2, the equations of output voltages to input voltage V_i is obtained as:

$$\frac{V_{o1}}{V_i} = \frac{Z_L / r_{o1} + g_{m1} Z_L}{1 + Z_L / r_{o1} + sC_{gd1} Z_L} \tag{3-1}$$

$$\frac{V_{o2}}{V_i} = \frac{-g_{m2} + sC_{gd2} + sZ_{s2}(\frac{C_{gs2} + C_{gd2}}{r_{o2}} + g_{m2} C_{gd2} + sC_{gd2} C_{gs2})}{\frac{1}{r_{o2}} + \frac{1}{Z_L} + sC_{gd2} + \frac{Z_{s2}}{Z_L}(\frac{1}{r_{o2}} + g_{m2}) + sZ_{s2}(\frac{C_{gs2} + C_{gd2}}{r_{o2}} + g_{m2} C_{gd2} + sC_{gd2} C_{gs2} + C_{gs2} / Z_L)} \tag{3-2}$$

Where Z_L models the loading impedance of the switching pairs and V_i' is assumed close to V_i at the operating frequency for the large capacitance C_b which is added to do the dc blocking. The large resistor R_b is used to give dc bias voltage and neglected in the analysis.

Suppose that Z_{s2} is equal to zero in (3-2), then (3-2) would be:

$$\frac{V_{o2}}{V_i} = \frac{-(g_{m2} - sC_{gd2}) Z_L}{1 + Z_L / r_{o2} + sC_{gd2} Z_L} \tag{3-3}$$

(3-1) and (3-3) must be equal in magnitude and out of phase at the operation frequency. Assume a pure resistance loading, Z_L=R_L, and equal size for the two transistors. The magnitude and phase of the two equations is extracted:

$$\begin{aligned} |\frac{V_{o1}}{V_i}| &= \frac{(1/r_{o1} + g_{m1}) R_L}{\sqrt{(1 + R_L / r_{o1})^2 + (wC_{gd1} R_L)^2}} \\ |\frac{V_{o2}}{V_i}| &= \frac{\sqrt{g_{m2}^2 + (wC_{gd2})^2} R_L}{\sqrt{(1 + R_L / r_{o2})^2 + (wC_{gd2} R_L)^2}} \end{aligned} \tag{3-4}$$

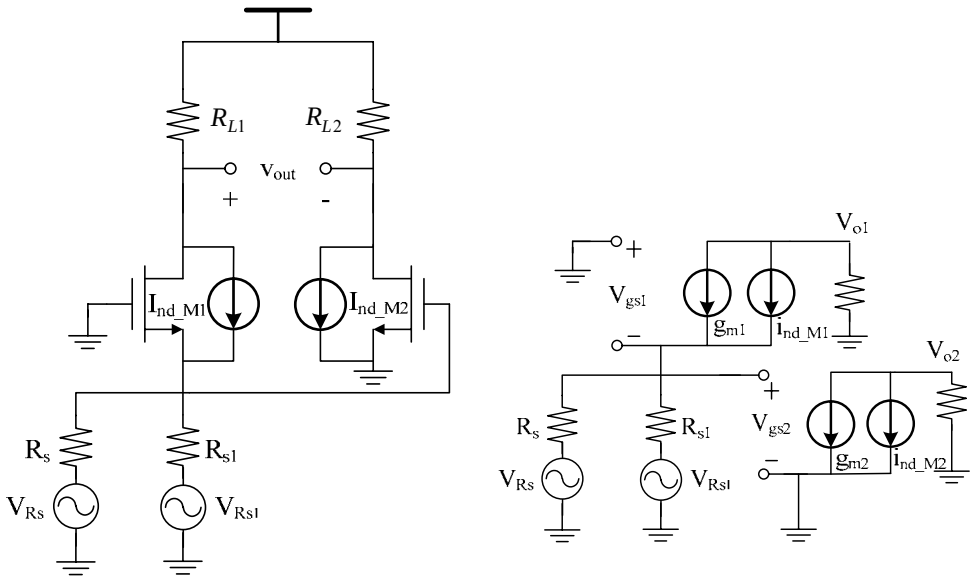
$$Arg(\frac{V_{o1}}{V_i}) = -\angle \tan^{-1} \frac{wC_{gd1}R_L}{1+R_L/r_{o1}}$$
$$Arg(\frac{V_{o2}}{V_i}) = \pi - \angle \tan^{-1} \frac{wC_{gd2}R_L}{1+R_L/r_{o2}} - \angle \tan^{-1} \frac{wC_{gd2}}{g_{m2}} \quad (3\text{-}5)$$

From (3-4) and (3-5), it is found that g_{m1} dose not exist in (3-5) that is g_{m1} could adjust the magnitude balance condition without any impact on the phase difference. Moreover, from (3-5), the phase difference of the two equations could be adjusted by one coefficient C_{gd1} by adding a parallel capacitance C_{ex} to the gate to drain capacitance of M_1. Since C_{gd1} will affect both the phase and gain difference, the C_{ex} is defined to make the phase balanced first, then to adjust g_{m1} to meet the magnitude condition. The bias voltages of CG and CS stage are separated, so g_{m1} can be adjusted by gate voltage independently. The value of g_{m1} and g_{m2} would not be far apart, and the values of r_{o1} and r_{o2} are expected to be almost equal.

The input admittance Y_{in} of the mixer can also be derived from the small signal model shown in Fig. 3.2:

$$Y_{in\_CG} = \frac{1}{Z_{s1}} + g_{m1} + sC_{gs1} + \frac{1}{r_{o1}} - \frac{1/r_{o1}^2 + g_{m1}/r_{o1}}{sC_{gd1} + 1/r_{o1} + 1/Z_L}$$
$$Y_{in\_CS} = sC_{gs2} + sC_{gd2}\frac{g_{m2} + 1/r_{o2} + 1/Z_L}{sC_{gd2} + 1/r_{o2} + 1/Z_L} \quad (3\text{-}6)$$
$$Y_{in} = Y_{in\_CG} + Y_{in\_CS}$$

Where Y_{in_CG} is the input admittance of the common gate transistor M_1 only and Y_{in_CS} is the input admittance seen into the gate of the common source transistor M_2. The real



(a) (b)

Fig. 3.3 Schematic for noise analysis (a) schematic (b) small signal model for (a)

part of the input impedance is mainly the parallel combination of $1/g_{m1}$ and Z_{s1}. By Z_{s1}, the gm value can be much more released, that is the power consumption can be much lower when making the input impedance matches to the source resistance.

3.2.2 Noise Analysis

Noise is analyzed in a simplified model which neglects both C_{gs} and C_{gd}, Z_{s1} is assumed to be R_{s1} to evaluate the noise contribution of every part of the transconductance stage, especially R_{s1} that is used to help input matching and power consumption. Only the drain current noise of the MOSFET and thermal noise of each resistor are taken into consideration. Based on Fig. 3.3, the noise power of each noise source contributes to the output is derived respectively. When calculate the noise output contribution of one noise source, other noise sources are turned off.

Consider for the thermal noise of R_s only:

V_{gs1}=-V_{gs2} (3-7)

$$i_{o1} = g_{m1}V_{gs1} = \frac{-V_{gs1}}{R_{s1}} + \frac{-V_{gs1} - V_{RS}}{R_s} \tag{3-8}$$

$$i_{o2} = g_{m2}V_{gs2} \tag{3-9}$$

From (2), $V_{gs1} = \frac{-V_{RS}}{R_s(g_{m1} + 1/R_{s1} + 1/R_s)}$ (3-10)

From (1) to (4), the output noise current can be derived as:

$$\overline{i_{no\_R_s}^2} = \overline{(i_{no1} - i_{no2})^2} = 4kTR_s(\frac{1}{1 + R_s/R_{s1} + g_{m1}R_s})^2(g_{m1} + g_{m2})^2 \tag{3-11}$$

where i_{o1} and i_{o2} are from the same noise source and are fully correlated to each other.

The output noise current for R_{s1} can be derived with the same procedure, and the equation is able to be written down immediately from (5). It is given as

$$\overline{i_{no\_R_{s1}}^2} = 4kTR_{s1}(\frac{1}{1 + R_{s1}/R_s + g_{m1}R_{s1}})^2(g_{m1} + g_{m2})^2 \tag{3-12}$$

The output noise from M_1 is calculated by equations as follows:

V_{gs1}=-V_{gs2}

$$i_{o1} = g_{m1}V_{gs1} + i_{nd\_M1} = \frac{-V_{gs1}}{R_s \parallel R_{s1}} \tag{3-13}$$

$$i_{o2} = g_{m2}V_{gs2}$$

From (7), $V_{gs1} = \frac{-i_{nd\_M1}}{g_{m1} + 1/(R_{s1} \parallel R_s)}$ (3-14)

From (7) and (8)

$$\overline{i_{no\_indM1}^2} = 4kT\frac{\gamma}{\alpha}g_{m1}(\frac{1 - g_{m2}(R_s \parallel R_{s1})}{1 + g_{m1}(R_s \parallel R_{s1})})^2 \tag{3-15}$$

As to M2, since the simplified model has no feedback path, Cgd1, the noise from M2 contributes directly to the output:

$$\overline{i_{no\_indM2}^2} = 4kT\frac{\gamma}{\alpha}g_{m2} \tag{3-16}$$

The expression for noise figure is

$$F = 1 + \frac{\overline{i_{no\_R_{s1}}^2}}{\overline{i_{no\_R_s}^2}} + \frac{\overline{i_{no\_indM1}^2}}{\overline{i_{no\_R_s}^2}} + \frac{\overline{i_{no\_indM2}^2}}{\overline{i_{no\_R_s}^2}} \tag{3-17}$$

From (11), (12), (15), and (16), the noise contributed by M_1 is much less than M_2 when the parallel combination of R_s and R_{s1} is approaching to $1/gm_2$. Take some values to give an approximate evaluation of each noise contribution. For R_s=50, g_{m1}=g_{m2}=0.015, γ/α=1, and R_{s1}=200, (3-17) would be

$$F \approx 1 + 0.25 + 0.08 + 1.33 = 2.66 = 4.25dB \tag{3-18}$$

The noises contribute by M_2 is the main noise sources. The drain noise of M_1 generates much less output noise as compared to M_2 for its negative feedback function. However, if g_{m2} is increased to make the term be zero, the noise contributes by M_2 is also increased. Moreover, the noise contributed by R_{s1} is much large than that from M_1.

3.3 LC-Folded Structure

The folded topology is a typical structure for low supply voltage consideration. The supply voltage of connected stages could be given respectively. An stacked structure is avoid. Furthermore, the current through the transconductance stage and switching

stage could be set differently. Though their biasing condition is independent, they are fully connected at high frequency for the frequency characteristic of LC tank. The LC tank is designed to resonate at the operation frequency. It is almost short at zero frequency so that DC supply voltage could be added through it. At the operating frequency, it provides very high impedance so that it will not degrade the differential current. Complete current could be transmitted to the switching stage for current commutation. At frequencies higher or lower to the center frequency, the impedance of LC tank is low. Therefore its resonate behavior forms a good filter to unwanted signals.

3.4 Mixing Stage

In this work, the proposed mixer utilizes current commutation for frequency mixing. A mixing stage is constructed to transform the incoming RF signal to a lower frequency. The non-ideal switching character and noise contribution will alleviate the circuit performance. To make the switching behavior more ideal, MOSFET of larger size is chosen and biasing point is set near threshold voltage. As pointed out in the beginning of this paper, the effort to convert signal into differential form is to make mixer in double-balanced structure. The issues of even-order distortion and LO-IF feedthrough are diminished in the double-balanced mixer.

Moreover, PMOSFET is chosen for its lower flicker noise. The flicker noise of MOSFET is appeared in low frequency range around DC, much lower than LO frequency, it can be effectively modeled as interference at the gate terminal of switching component. This slowly varying offset voltage disturbs the switching time, advancing or retarding the time of zero crossing. Mixed with the LO signal, the low frequency noise is up-converted to frequency around the LO frequency which degrades the function of mixing [11]. Therefore, the mixer topology is chosen as PMOS pairs. The complete circuit schematic is shown in Fig. 3.4.

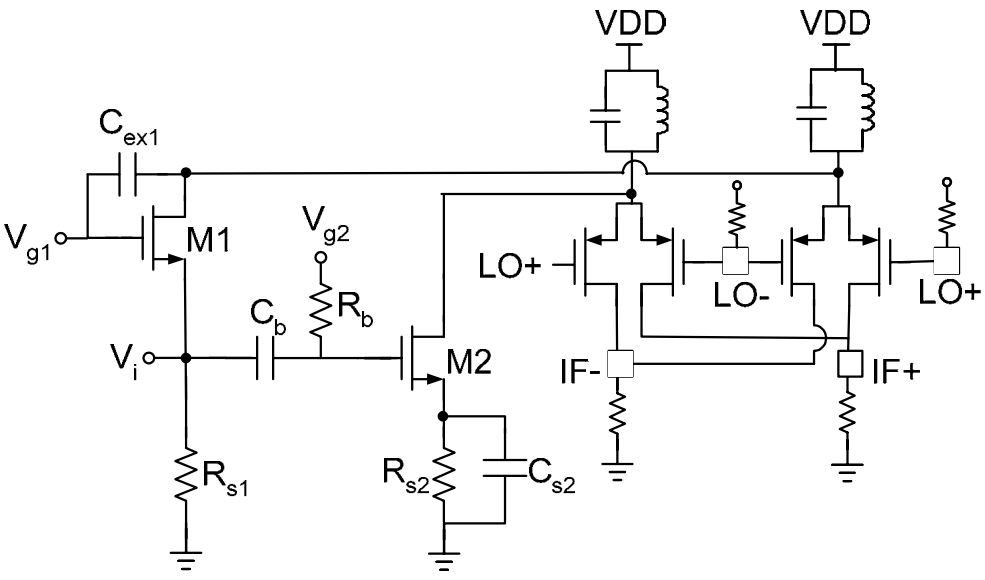


Fig. 3.4 Complete circuit schematic of the mixer.

3.5 Chip Implementation and Measured Result

The die micrograph of the mixer fabricated in 0.18-um RF CMOS technology is shown in Fig. 3.5. The size of the chip is 1.04 x 0.67 mm^2 including bonding pads. Measurements were conducted by chip-on-board setup as shown in Fig. 3.6. RF input and LO signals are applied through on-wafer probing with a GSG probe and GSGSG probes, respectively. A hybrid coupler is utilized to generate the LO differential signal from a single-ended signal. DC pads are wire-bonded on a PCB board, so as the differential IF signal. The output IF signal is buffered by an on-board unit gain operational amplifier circuit to convert to a single-ended form. Not to affect the IF loading condition, the differential input impedance of the OP amplifier is chosen as 16

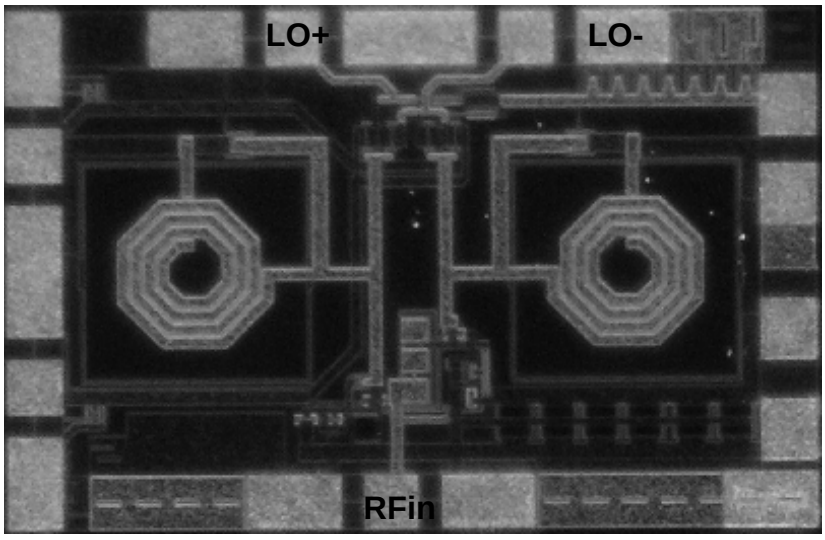


Fig. 3.5 Micrograph of the mixer.

Kohm. A 50-ohm resistor is connected in series at the OP amplifier output for impedance matching to measurement system. Therefore, 6dB voltage gain shall be compensated in all the gain measurement.

The supply voltage Vdd is set as 1V in the measurements. The total DC power consumption is only 2 mW. The measured and the simulated input return loss centered at 5.5 GHz are shown in Fig. 3.7(a). The measured S11 is better than -10 dB within the wanted frequency band but for frequency higher than 4GHz, the measured S11 is worse than the simulated data. If is found on the Smith chart that the impedance is higher than 50Ohm. The input matching condition could be improved with higher bias voltage for larger gm. The RF signal is downconverted to 1 MHz. The measured conversion gain is 10.4 dB and the P1dB point is -6.8 dBm as depicted in Fig. 3.7(b). It is about 3.5 dB short as compared to the simulation. Two-tone test is done for measuring third-order intermodulation distortion. The maximum gain is corresponding to LO power equal to 2dBm as shown in Fig. 3.7(c). Fig. 3.7(d) shows that the measured IIP3 is about 3.8 dBm while the simulated IIP3 is about 0dBm. The noise figure is not tested for now and the simulated result is 9.9 dB.

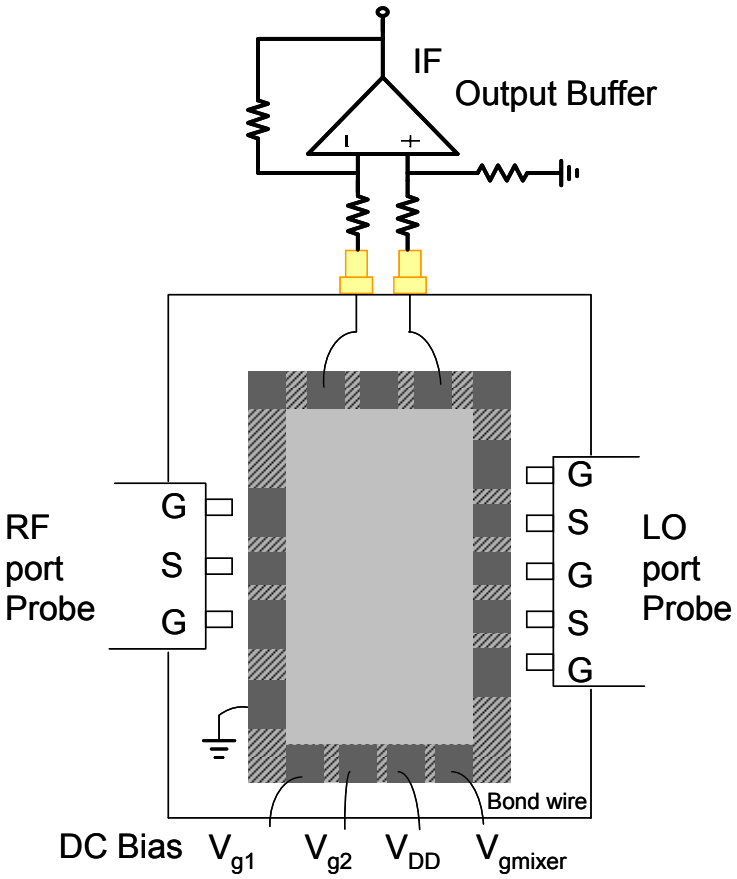
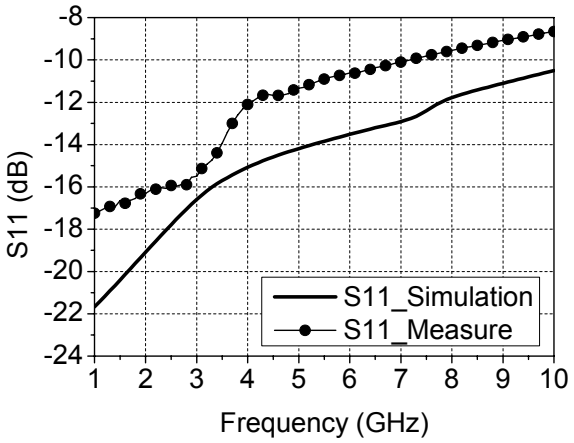
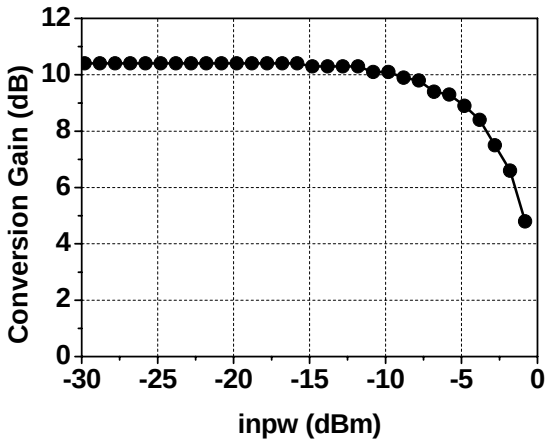


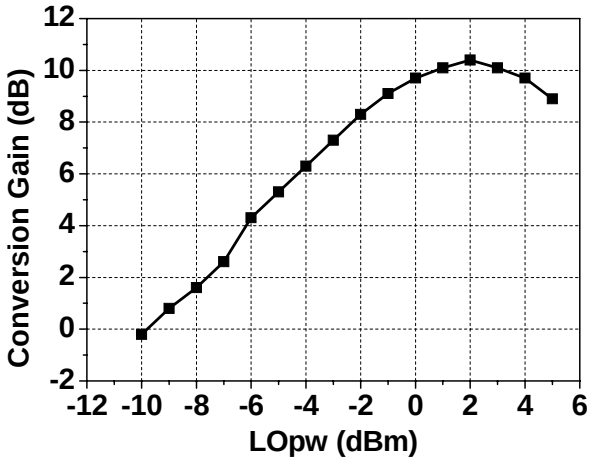
Fig. 3.6 Setup for mixer measurement.



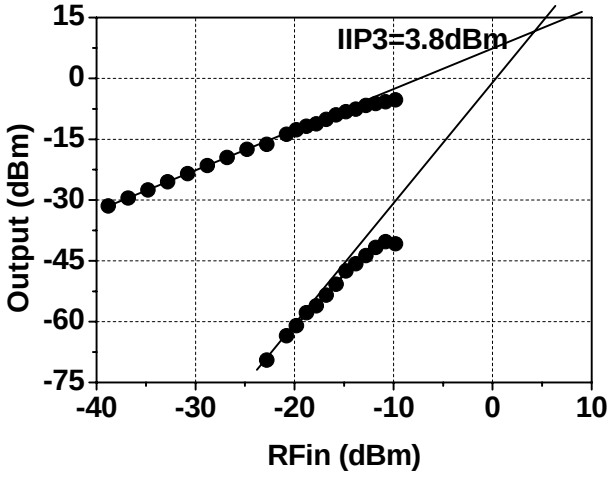
(a)



(b)



(c)



(d)

Fig. 3.7 Mixer measured result (a) Input return loss (b) Conversion Gain (c) Conversion gain versus Lo

3.6 Summary

A 5-GHz double-balanced mixer is designed and fabricated in 0.18 CMOS technology. The circuit architecture is chosen available for the application of low supply voltage and low power consumption. The circuit consists a transconductance stage and PMOS switching pairs in a folded topology. Phase splitting function is integrated in the transconductance stage, which is composed of a common gate and common source transistors to save power consumption and to benefit from the double–balanced topology. Output balanced condition and noise of the transconductance stage are analyzed.

The measured input return loss and voltage conversion gain are 11dB and 10.4dB, respectively. The input third-order intercept point (IIP3) is 3.8dBm while consuming only 2mW from a 1V supply. Table I summaries the measured results of this work and compares the performance with other two circuits. Among these, [12] is a differential input mixer, and the power consumption must be increased since a phase splitting stage has to be added for single-ended input. As compared to the two circuits, this work has comparable gain and linearity while consuming the lowest power and lower supply voltage.

TABLE 3.1

Summary of measured performance and comparison to other mixers.

Item	This Work	Ref[10]	Ref[12]
Technology	CMOS 0.18um	CMOS 0.18um	CMOS 0.18um
RF Frequency (GHz)	5.5	2.4	2.4
DC Supply Voltage (V)	1.0	1.8	1
LO power (dBm)	2	-	0.5 Vp
Conversion Gain (dB)	10.4	16.5	11.9
IIP3 (dBm)	3.8	9	-3
Noise Figure (dB)	9.9 (simulate)	14.2 (DSB)	13.9 (SSB)
Power Dissipation (mW)	2	5.4	3.2

Chapter 4

Low-Power Front-End Circuit

4.1 Introduction

To meet the low supply voltage requirement, the conventional cascode topology is dismissed, a single transistor structure is adopted instead for the LNA. The issue of this structure is the stability problem, and it has been tackled in our design. A figure of merit is also presented to find an optimum biasing point for transistors under low supply voltage as low as 0.6V.

Transformer ac coupling is an effective way to realize a low power front-end circuit. It can not only cut down the supply voltage [13], but also do the phase transformation

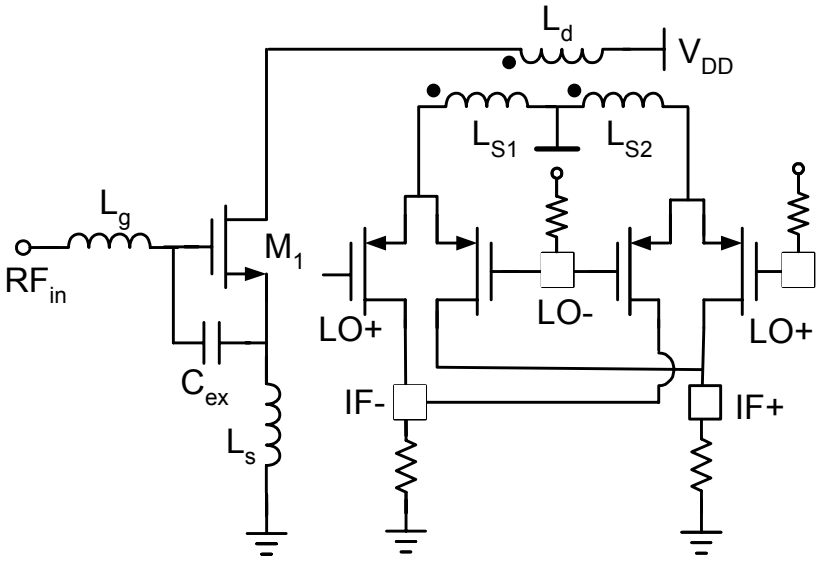


Fig. 4.1 Receiver front-end circuit schematic.

without extra power consumption [14]. The transformer design relates to many design variables, to analyze and design with a quick convergence to the optimum condition is realistic for fabrication. In this work, based on resonant operation idea [15], a transformer is designed to transform single-ended signal from the LNA into differential current with current conversion gain to realize a low power receiver front-end circuit.

Fig. 4.1 shows the circuit schematic of this receiver front-end. The design consideration of each stage is discussed in the following sections.

4.2 Low Noise Amplifier

4.2.1 MOSFET I-V Model

A semi-empirical, single-piece expression that provides good accuracy in moderate inversion and acceptable accuracy in weak and strong inversion is given by [16]

$$I_{ds} = I_{do}\{[\ln(1+e^{\frac{V_{gs}-V_{th}}{2n\phi_t}})]^2 - [\ln(1+e^{\frac{V_{gs}-V_{th}-nV_{ds}}{2n\phi_t}})]^2\} \quad (4\text{-}1)$$

where

$$I_{do} = \mu C_{ox} 2n\phi_t^2 \frac{w}{L}$$

$\phi_t = kT/q$ is the thermal voltage. The parameter n whose value depends on the process describes the rate of exponential incrase of Ids with Vgs in the subthreshold region. Its value varies from 1.1 to 1.9 which is higher for short channel devices.

When MOSFET operates in weak inversion region, the exponential terms in (4-1) are small and with log(1+x)≈x for x<<1, (4-1) reduces to

$$I_{ds} \approx I_{do}(1-e^{\frac{-V_{ds}}{\phi_t}})e^{\frac{V_{gs}-V_{th}}{n\phi_t}} \quad (4\text{-}2)$$

For the strong inversion region, $\log(1+e^y)^2 \approx \log(e^y)^2 = y^2$, (4-1) is reduced to

$$I_{ds} = \mu C_{ox}\frac{w}{L}[(V_{gs}-V_{th})V_{ds} - \frac{1}{2}nV_{ds}^2] \quad (4\text{-}3)$$

for linear region, and it is simplified to

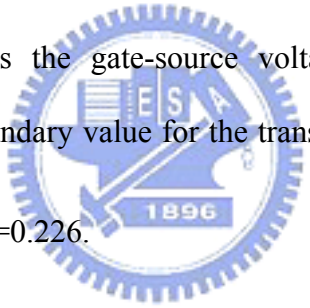
$$I_{ds} = \mu C_{ox}\frac{w}{L}\frac{(V_{gs}-V_{th})^2}{2n} \quad (4\text{-}4)$$

for strong inversion where MOSFET in the linear RF blocks are usually biased. In the

saturation region, the second exponential in (4-1) becomes negligible, and (4-1) reduces to

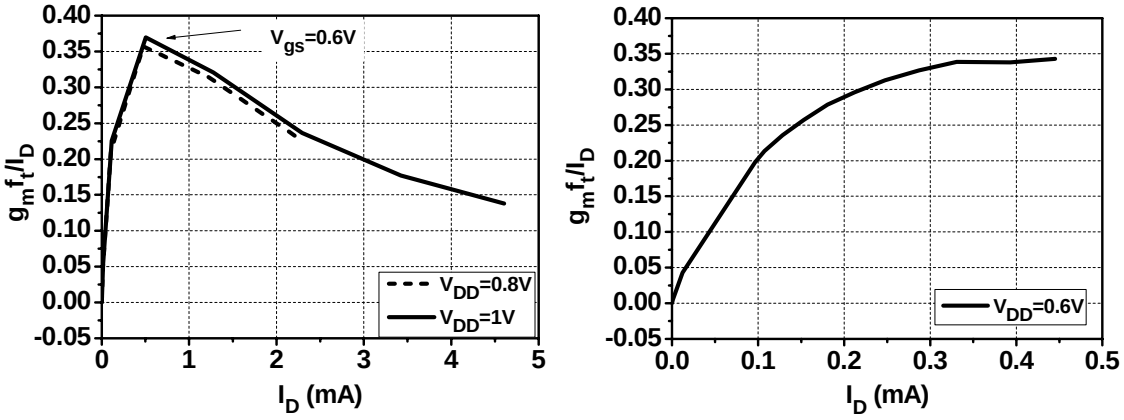
$$I_{ds} = I_{do}\{[\ln(1+e^{\frac{V_{gs}-V_{th}}{2n\phi_t}})]^2 \quad (4\text{-}5)$$

From the semiconductor concept, the MOSFET's operation region makes a transition from weak to moderate inversion region if both the minority and the majority carrier concentrations become equal. To determine the bias transition from the I-V relation of MOSFET, the exponential part of (4-5) is approximated as $(V_{gs}-V_{th})^2$ when $V_{gs}-V_{th} >> 2n\phi_t$. Thus, the upper limit of moderate inversion region is roughly defined as the gate-source voltage at which $e^{\frac{V_{gs}-V_{th}}{2n\phi_t}} = 10$ or V_{gs}-V_{th}=4.6nϕ_t [17]. The boundary value for the transition for n as 1.1 to 1.9 ranges from V_{gs}-V_{th}=0.131 to V_{gs}-V_{th}=0.226.



4.2.2 Optimum Design- New Figure of Merit

LNA typically consumes much more power than that of the other parts to provide enough gain to the receiver front-end circuit. In order to maintain low power consumption, the biasing current of the LNA is desired to be as low as possible. Therefore, there exists a compromise between the current consumption, ID, and the transconductance, gm, of the MOSFET to keep the gain of the circuit. A conventional figure of merit, g_m/I_D, is so presented. However, this kind of definition dose not take



(a) (b)

the frequency response of a device into consideration. Another figure of merit, $g_m f_t/I_D$, [17] which adds unit gain frequency into it to evaluate the frequency response of the MOSFET is therefore defined and an optimum design point is found by using this parameter, which is moderate inversion region of a MOS transistor.

But this figure of merit is not effective as the supply voltage level goes down. As shown in fig. 4.2, where the x axis is the biasing current, I_D, and the y axis is the production of g_m and f_t divided by I_D, both of which are not normalize but it has no effect on the conclusion. Fig. 4.2(a) takes supply voltage, V_{DD}, as 1 V and 0.8 V, respectively. Sweep the bias voltage, V_{gs}, from zero to V_{DD}, a maximum value of the figure of merit is reached when V_{gs} is about 0.6V. But when the supply voltage is lowered further to 0.6V, as shown in fig. 4.2(b), no optimum point would exist. The value of the figure of merit keeps flat when V_{gs} approaches V_{DD}, 0.6V.

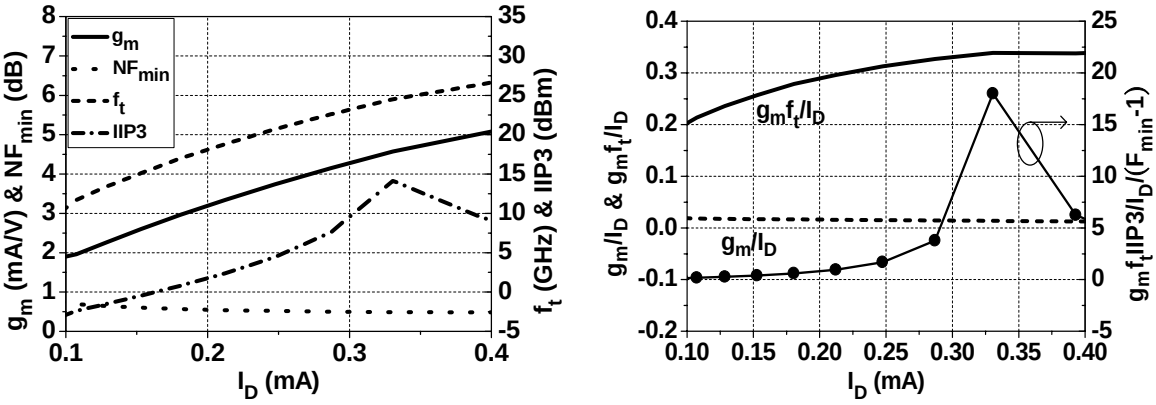
To decide an optimum design point around 0.6V, linearity of the MOS transistor is

added to define a figure of merit for MOSFET:

$$\frac{g_m f_t IIP3}{I_D(F_{\min}-1)} \tag{4-6}$$

which has been used as a figure of merit for LNA. As shown in fig. 4.3(a), IIP3 has an optimum value around that flat region. Fig. 4.3(b) shows the new figure of merit. Therefore, the bias condition of LNA is chose as 0.58V.

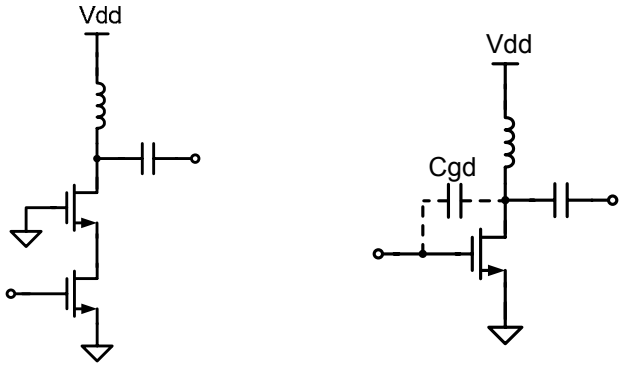
However, the load impedance affects the position of the IIP3 peak and should be taken into consideration as discussed in section 4.4. Therefore, a modified version of this circuit was re-taped out. The second chip of the front-end trades little gain while has better linearity and lower power consumption.



(a) (b)

Fig. 4.3 Character of a transistor (a) Parameters variation of a transistor (b) Several figure of merits for a transistor.

4.2.3 LNA Stabilization



(a) (b)

Fig. 4.4 Topologies of LNA (a) Cascode configuration (b) Single transistor topology.

Cascode configuration shown in Fig. 4.4(a) is conventionally adopted for LNA design. It has good isolation between the input and output port. However, as the supply voltage goes down, cascode configuration is not applicable. A single transistor configuration as shown in Fig. 4.4(b) is preferred. The C_{gd} feedback path causes the circuit isolation become poor. The load inductance connected to the drain of the transistor falls into the unstable region for a common source transistor. Therefore, an effort is needed to make sure the circuit is stable.

Fig. 4.5 is the source and load stability circle of a single transistor from 0.1GHz to 10GHz. As shown in this figure, the load stability circle of a common source transistor typically cuts the upper region of the smith chart. There is no stability issue for the cascode topology since the load of the common source transistor is usually

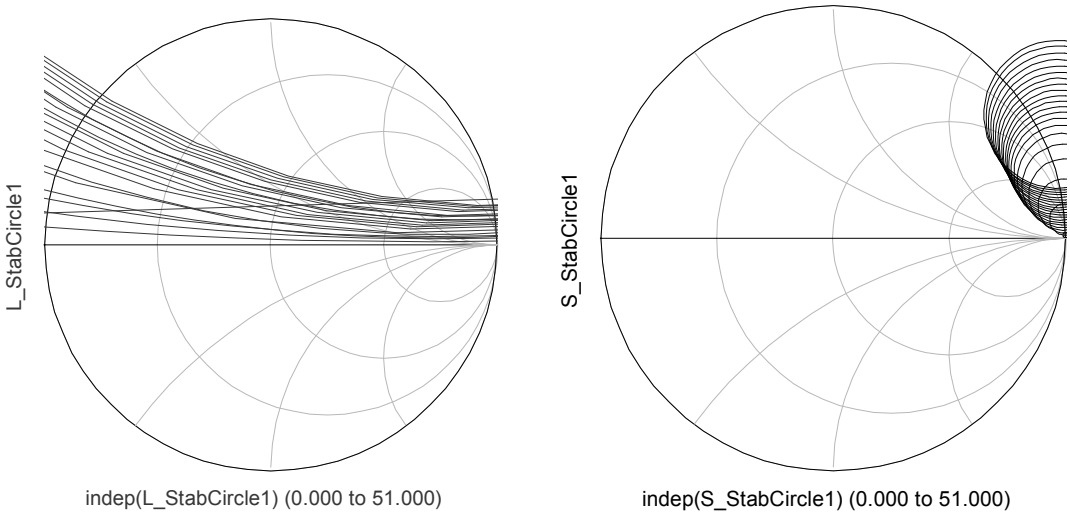


Fig. 4.5 Load and source stability circle of a single transistor

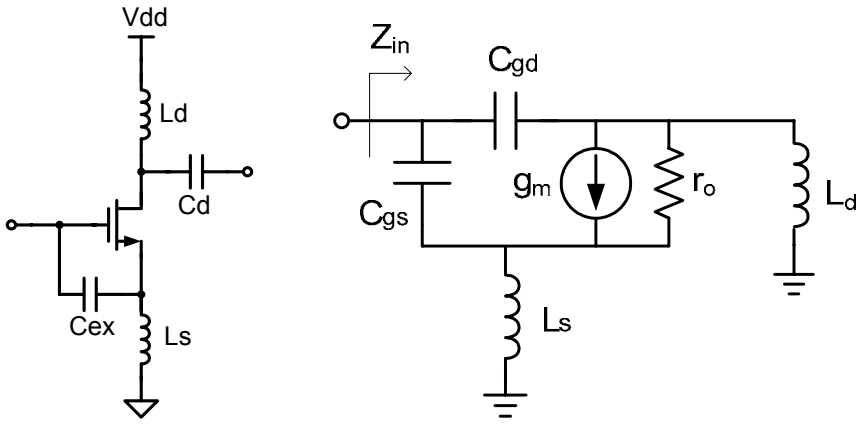
capacitive and locates at the stable region. However, the load in our design is potentially inductive. To improve the stability of the two port network, a small signal model shown in Fig. 4.6(b) is used to calculate the input resistance when an inductor being its load and two passive components added as in Fig. 4.6(a). The input impedance is derived as

$$Zin = \frac{(1 + sg_m L_s + s^2 C_{gs} L_s)(1 + s^2 C_{gd} L_d)}{s[(C_{gs} + C_{gd}) + sg_m C_{gd}(L_s + L_d) + s^2 C_{gs} C_{gd}(L_s + L_d)]} \tag{4-7}$$

Assuem

$$\begin{aligned} Zin &= \frac{c + jd}{a + jb} = \frac{ac + bd}{a^2 + b^2} + j\frac{ad - cb}{a^2 + b^2} \\ a &= -w^2 g_m C_{gd}(L_s + L_d) \\ b &= w[(C_{gs} + C_{gd}) - w^2 C_{gs} C_{gd}(L_s + L_d)] \\ c &= 1 - w^2 C_{gd} L_d - w^2 C_{gs} L_s + w^4 C_{gs} C_{gd} L_s L_d \\ d &= wg_m L_s - w^3 g_m C_{gd} L_s L_d \end{aligned} \tag{4-8}$$

To make sure the real part of the input resistance is positive, ac+bd must be positive.



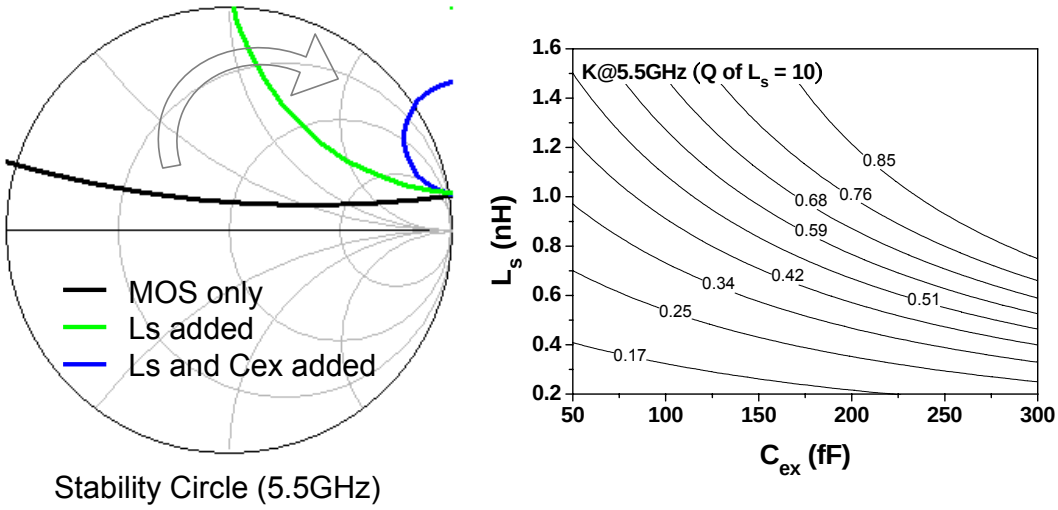
(a) (b)

Fig. 4.6 Schematic and small signal model of proposed LNA (a) The transistor with stabilization elements. (b) small signal model of (a).

After some calculation, the equation is given as

$$(C_{gs}L_s - C_{gd}L_d)(1 - C_{gd}L_d w^2) > 0 \qquad (4\text{-}9)$$

The input resistance might be negative due to the inductive load. The second term in (4-9) would not be negative up to several tens of gigahertz. Therefore, the multiplication of C_{gs} and L_s must be larger than $C_{gd}L_d$ to improve the circuit stability. The result is quite intuitive since the gain of the circuit degrades due to these added components. The above analysis gives a hint to improve stability, though it is not complete. The output port should also be checked. However, as shown in Fig. 4.5, the source stability circle cuts less to the Smith chart and the source impedance is typically 50 Ohms which is far out of the stability circle.



(a) (b)

Fig. 4.7 Stability variation with stabilization (a) Stability circles before and after stabilization (b) K of a transistor with Ls and C_{ex}

Fig. 4.7(a) depicts the simulation result of load stability circle's variation when these two passive components are added to a single transistor. Fig. 4.7(b) shows the variation of K for C_{ex} and L_s. The K does grow high as L_sC_{ex} gets higher. The K is still less than 1, so the circuit is still conditionally stable. But as Fig. 4.7(a) shows, the stability circle does moves more out before stabilization.

Since the higher the C_{ex} and L_s is, the lower the gain and the higher the NF_{min} would be, these values are chosen to be properly large to make sure the load impedance locates outside the stability circle for all the frequencies. As shown in Fig. 4.8, the L_s is 0.9nH and C_{ex} is 100fF.

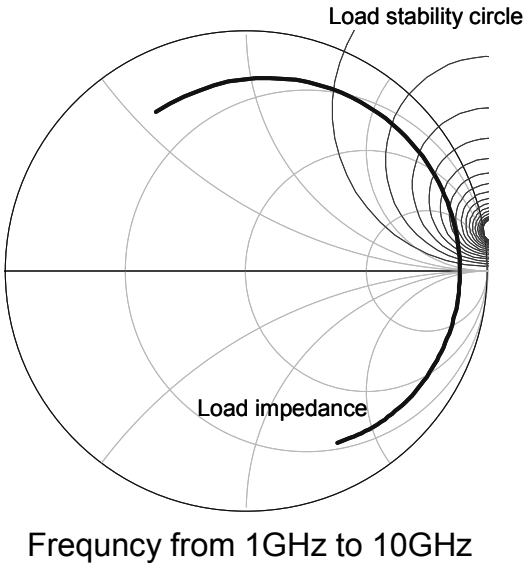


Fig. 4.8 Frequency response of load stability circle and load impedance

4.3 Mixer Consideration

The transconductor of the mixer is the transformer stage. The transformer converts input signal into differential current output and then sends into the mixing stage. The design consideration for the first chip of the front-end circuit is based on the idea discussed in Section 3.4. However, the mixing stage has to be activated by large LO power which dose not conform to the idea of low power consumption. Therefore, the modified version re-considers the design procedure. Gate bias voltage, LO power, and load resistance R_L are the design variables. The conversion gain begins to decrease when the MOSFET operation suffered from compression, which is about 0.2 to 0.3V for drain to source voltage V_{DS}.

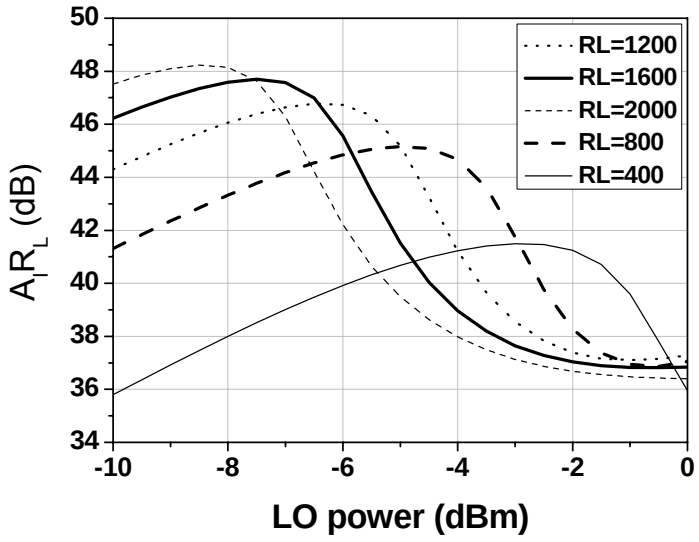


Fig. 4.9 Conversion gain versus LO power for different load resistance.

Therefore, for larger RL, the LO power for highest gain is smaller while the power consumption is smaller. And for lower gate bias voltage, or said larger VSG for PMOS, the LO power for highest gain is also smaller. Fig. 4.9 depicts the current to voltage conversion gain of the mixing stage with different R_L for a given gate bias voltage 0.16V. Since the gain gets saturated when R_L large, the selected R_L is 1600 Ohm and the LO power is -7.5dBm.

4.4 Transformer Design

Transformer is used as the phase splitter stage for this circuit. Differential current has been generated from a single-ended input for the following stage with no extra power consumption. However, the conversion loss of a conventional transformer design trades the benefit of power, since a higher power consumption of LNA is required to overcome the loss. Based on the idea of resonant operation mentioned in [15], two coupled resonant networks, each of which composed of a capacitor and an inductor, have resonant frequency w_1 and w_2, respectively, can result in a high current gain of the transformer. In this way, there is no need to increase the power of the LNA stage and the phase splitting can be done with current conversion gain under no extra power consumption so that low power consumption is achieved. Moreover, the AC coupled DC blocked character makes LNA and Mixer connected in a folded topology. Low supply voltage is therefore realized.

4.3.1 Equivalent Model for the Transformer

There are some main parameters regarding to describe a transformer. One of them is turn ration n:

$$n = \sqrt{\frac{L_1}{L_2}} \tag{4-10}$$

where L_1 and L_2 are the self-inductances of the primary and secondary windings,

respectively.

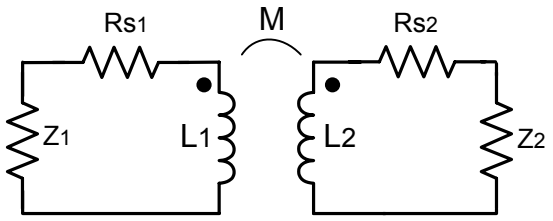
The self-inductance, which is relates the voltage induced in a winding by a time-varying current in the same winding, is extracted at the terminals with other windings open-circuited. For monolithic transformers, the turn ratio value is not equal to the turn ratio of the layout, since the physical length of the inside and outside turns are not equal. Besides, the arrangement of the alternative windings affects the self-inductance of each winding.

Another is the magnetic coupling coefficient k:

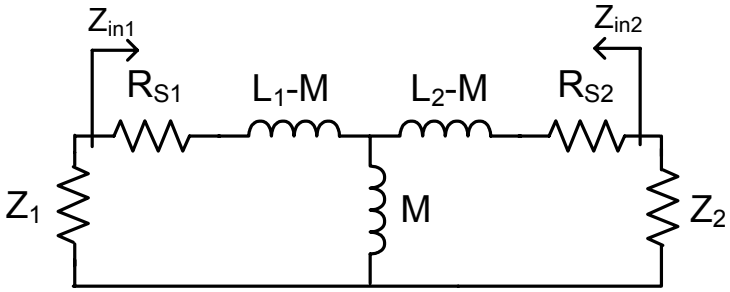
$$k = \frac{M}{\sqrt{L_1 L_2}} \tag{4-11}$$

where M is the mutual inductance, which is the ability of one inductor or segment to induce a voltage across the neighboring inductor or segment when they are close enough.

There are mutual inductance between two inductors and different segments of a single inductor. The mutual inductance linking these two could be positive or negative to the total inductance of each of them. For two segments with current flow in the same direction, the mutual inductances are positive. But for two segments with current flow in opposite direction, the mutual inductances are negative. k is a measure of the magnetic coupling between two windings and ranges from zero, uncoupled condition, to unity, perfect coupling. For passive elements, the magnitude of the



(a)



(b)

Fig. 4.10 Transformer model (a) a figure presents transformer (b) a small signal model of (a)

coupling coefficient may not exceed unity.

Fig. 4.10(a) is a figure of transformer with loads Z_1 and Z_2 and Fig. 4.10(b) is a simple equivalent model for the transformer. L_1 and L_2 are the self-inductances of the windings. M is the mutual inductance between the two windings. R_{s1} and R_{s2} are the ohmic losses of the windings. Z_1 and Z_2 are not only the source and load impedances but also have to include parasitic capacitances of the transformer, as the model adopted later. The input impedance Z_{in1} can be derived as

$$Z_{in1} = R_{s1} + SL_1 + \frac{w^2 M^2}{Z_2 + R_{s2} + SL_2} \tag{4-12}$$

For an ideal transformer, which is defined to has unity coupling coefficient, and infinite self-inductances with no loss, the input impedance is

$$Z_{in1} = Z_2 n^2 \quad (4\text{-}13)$$

which is quite different from the input impedance derived for non-ideal case. Though both of them depict the ability of impedance transformation, the n^2 ratio may not be realistic in reality and depends on the inductances and mutual inductances.

4.3.2 Derivation and Design of Resonant Operation for Current Gain

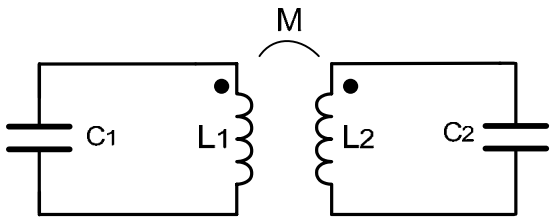


Fig. 4.11 Resonant system

Before calculating for the current transfer equation, let's take a look at resonant network[15] which is composed of two LC resonant circuits with some mutual coupling between them as shown in Fig. 4.11. The resonant frequencies are w_1 and w_2, respectively.

$$\omega_1 = \frac{1}{\sqrt{L_1 C_1}}, \omega_2 = \frac{1}{\sqrt{L_2 C_2}} \quad (4\text{-}14)$$

Let $w_1 = m w_2$. The two resonant frequencies of this system can be derived as

$$w_r = w_2\sqrt{\frac{1+m^2 \pm \sqrt{m^4-2m^2+4k^2m^2+1}}{2(1-k^2)}} \tag{4-15}$$

where

$$w_H = w_2\sqrt{\frac{1+m^2+\sqrt{m^4-2m^2+4k^2m^2+1}}{2(1-k^2)}}$$
$$w_L = w_2\sqrt{\frac{1+m^2-\sqrt{m^4-2m^2+4k^2m^2+1}}{2(1-k^2)}} \tag{4-16}$$

For two resonators of the same frequency w_o, m=1, when there exists some coupling between them, the coupled system's resonant frequency will depart from w_o due to the coupling coefficient. For two resonators of different resonant frequency, the systems resonant frequency will depend not only on k, but also on their separate resonant frequencies. When the resonant system resonant at the desired frequency, no matter it is of the higher resonant frequency or the lower one, the current gain can be relatively high.

Let's consider for the model to calculate for the current transfer equation of the fabricated transformer. Since the signal is differential at the second turn, there exists a virtually short point for the transformer, the center tape, and two of the switching pairs of the front-end circuit are turned on by the LO signal. The simplified equivalent

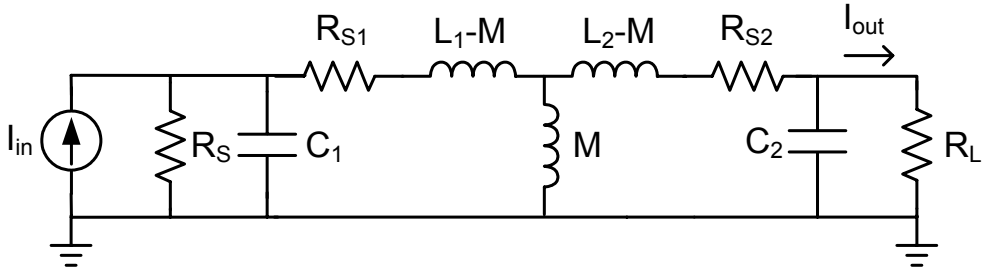


Fig. 4.12 small signal model for current transfer function calculation

circuit for the half path of Fig. 4.1 can be shown as Fig. 4.12. R_s and R_L are the source and load impedances which are extracted from the former stage, LNA, and the following stage, switching stage, respectively. C_1 and C_2 are the parallel combination of the parasitic capacitances of transformer and that of the stages connected to it. With the definition of following coefficients, the transfer function would be a function of five variables, m, k, n, L_1, and C_1 when R_s, R_L, w, and α are defined.

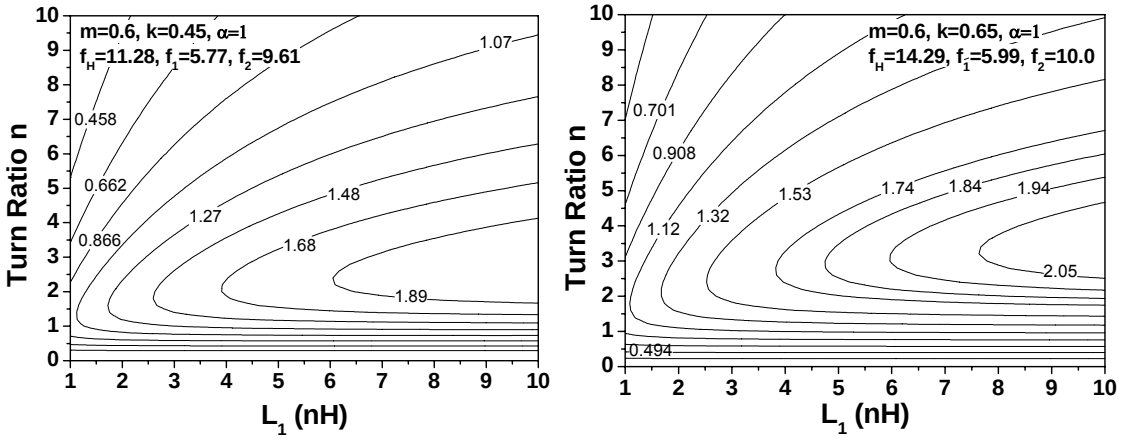
$$
\begin{aligned}
m &= \sqrt{\frac{L_2 C_2}{L_1 C_1}} = \frac{w_1}{w_2} \\
n &= \sqrt{\frac{L_1}{L_2}} \\
k &= \frac{M}{\sqrt{L_1 L_2}} \\
R_1 &= \alpha L_1 \\
R_2 &= \alpha L_2
\end{aligned}
\qquad (4\text{-}17)
$$

The current transfer function is (4-18) which is given as:

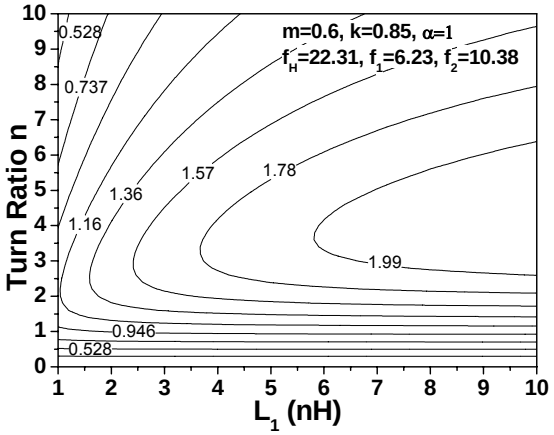
$$
G(s) = \frac{I_{out}}{I_{in}} = \frac{sR_s M}{R_L[R_s + (R_1 + sL_1)(1 + sR_s C_1)] + (1 + sR_L C_2)\{sM\{R_s + (1 + sR_s C_1)[R_1 + s(L_1 - M)]\} + [R_2 + s(L_2 - M)][Rs + (R_1 + sL_1)(1 + sR_s C_1)]\}}
$$

To design the transformer for resonant operation, (4-16) are assumed equal to operation frequency in turn and w_2 is therefore solved for given m and k condition.

Once w_2 is found, w_1 is also known. The remained unknowns are the L_1 and L_2 values, which is equivalent to L_1 and n, and C_1 and C_2, the last two unknowns, can be derived after these two values are defined. There are lots of possible solutions for L_1 and n. All these solutions satisfy the resonant operation condition. But among them, the rules of L_1 and n combination which gives the highest possible gain need to be found out. Since the target of the design is to find high gain solution, (4-18) is calculated for sets of L_1 and n. Fig. 4.13 to Fig. 4.15 are the gain variation condition with solutions of L_1 and n under certain m and k combination. The current gain is calculated for: R_s=7.675kΩ, R_L=276Ω, α=1Ω/nH case. R_s and R_L is the extracted r_o of LNA and operation parallel $1/g_m$ of the switching pair.



(a) (b)



(c)

Fig. 4.13 Current gain relative to n and L_1. Set f_L=5.5GHz, m=0.6 (a) k=0.45 (b) k=0.65 (c) k=0.85

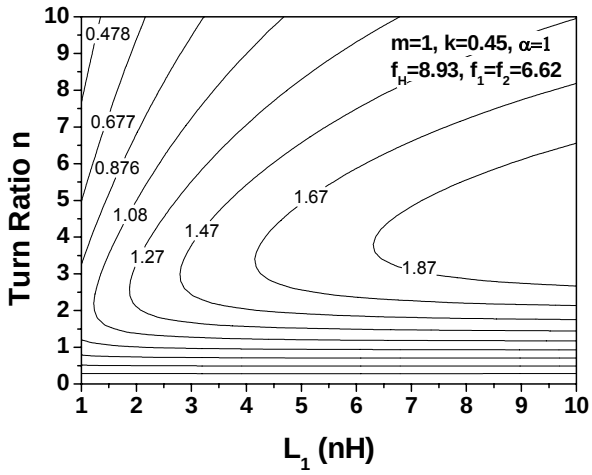


Fig. 4.14 Current gain relative to n and L_1. Set f_L=5.5GHz. m=1, k=0.45

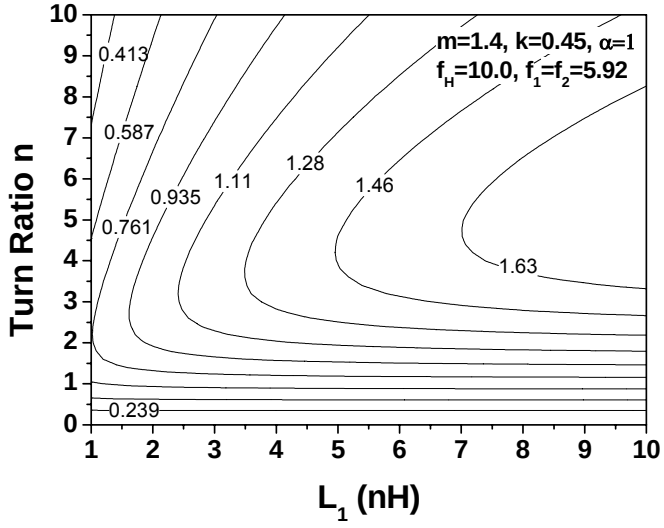


Fig. 4.15 Current gain relative to n and L_1. Set f_L=5.5GHz. m=1.4, k=0.45

Assumed three conditions: m=0.6 (m<1), m=1, m=1.4 (m>1) and set lower resonant frequency f_L as 5.5GHz. The condition for higher gain is limited to certain turn ratio and the calculated gain becomes saturated for that turn ratio as L_1 gets larger. For larger m (w_1 is higher than w_2), the turn ratio for higher gain is moved to larger region than smaller m case. The current gain gets higher as k larger. No matter what the m value is, the current gain has close order of magnitude. But for m<1 and

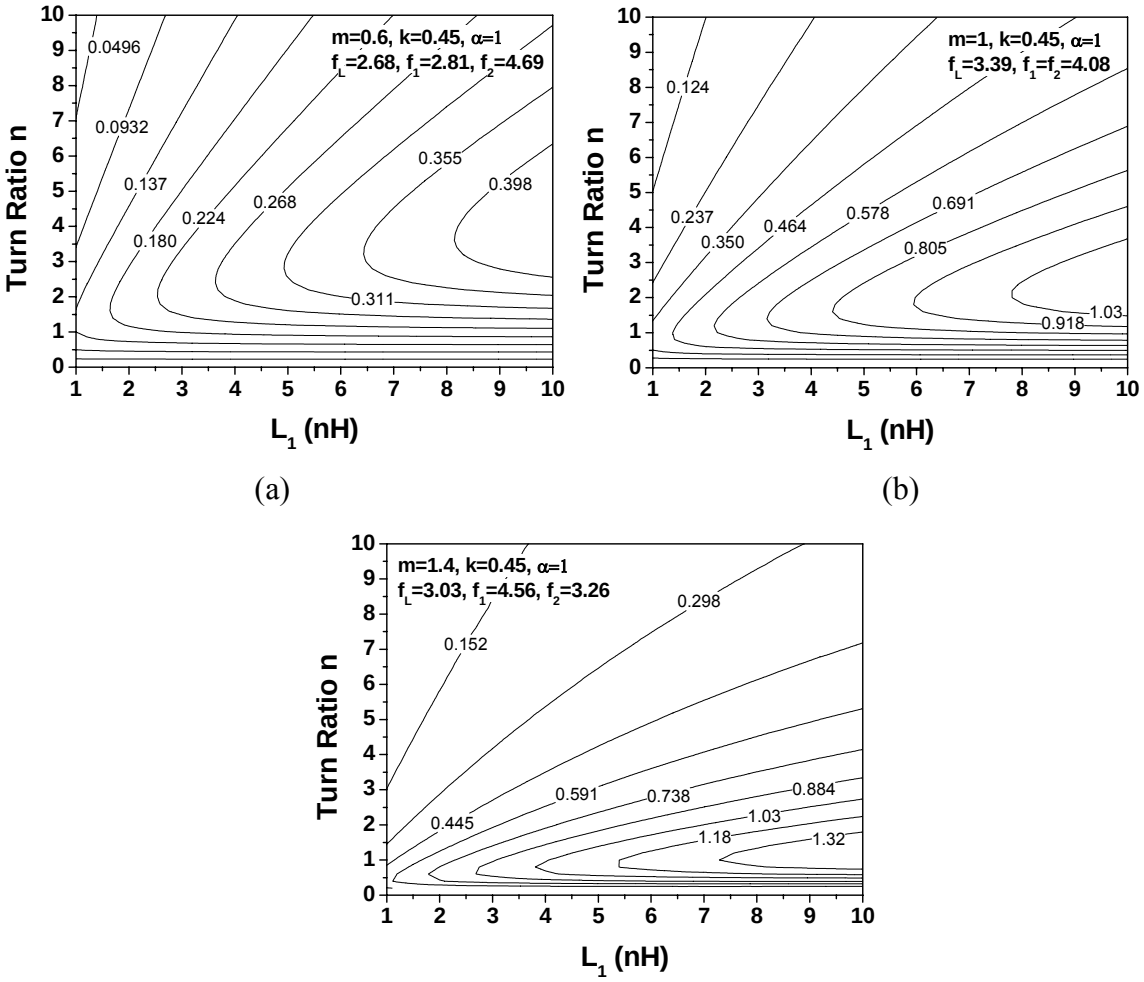
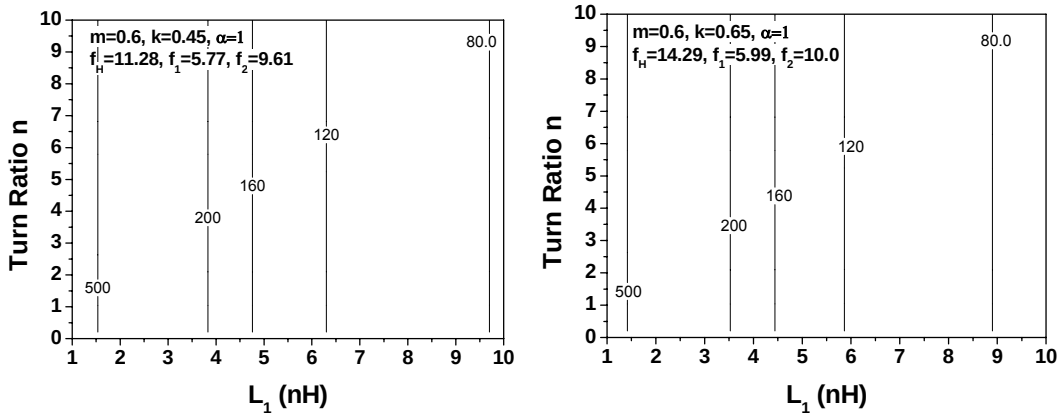


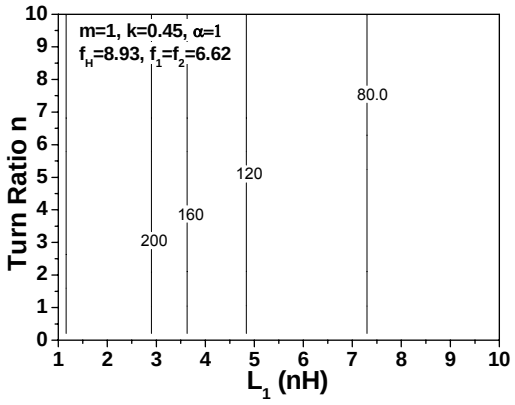
Fig. 4.16 Current gain relative to n and L_1. Set f_H=5.5GHz (a) m=1.4, k=0.45 (b) m=0.6, k=0.45 (c) m=1, k=0.45

f_L=5.5GHz case, the current gain can be larger than the turn ratio due to the resonant operation mode. Moreover, for m>1 and lower resonant frequency f_H=5.5GHz case, the current gain can also be larger than the turn ratio as shown in Fig. 4.16.

For k higher, the current gain is getting lower for f_H equal to 5.5GHz case. Although the current gain larger than turn ratio for m>1 case, the magnitude under this case is much lower than setting f_L to 5.5GHz cases. Therefore, it is better to design f_L as the operation frequency.



(a) (b)



(c)

Fig. 4.17 Calculated C1 for different solutions (a) m=0.6, k=0.45 (b) m=0.6, k=0.65 (c) m=1, k=0.45.

As mentioned in last few paragraphs, for f_L=5.5GHz case, the current gain for different m is quite close and the gain is higher for larger k, how to make decision for these parameters? The constraint is given by the unavoidable parasitic capacitance of the transformer and that of the stages connected to transformer. C_1 is typically the limit since the turn ratio larger than one means smaller L_2, then calculated C_2 is usually quite large. Fig. 4.17 shows the calculated C_1 value for Fig. 4.13 (a) and (b). When the coupling coefficient gets larger, the calculated resonant frequency w_2

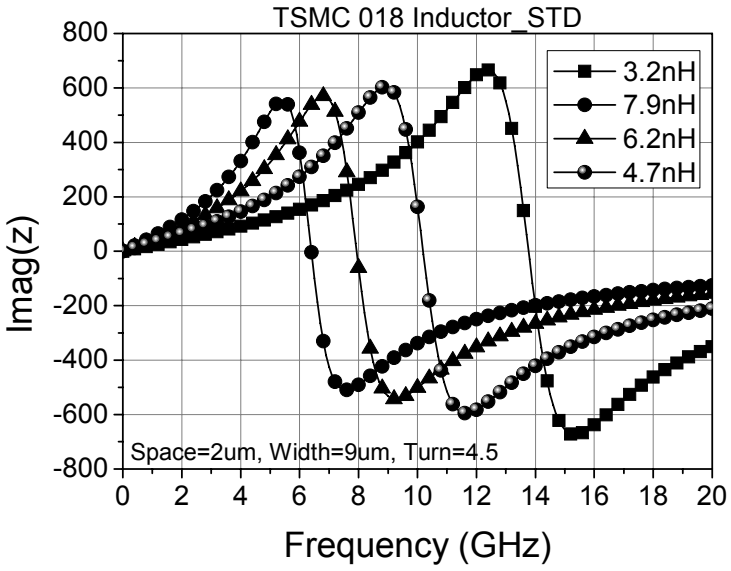
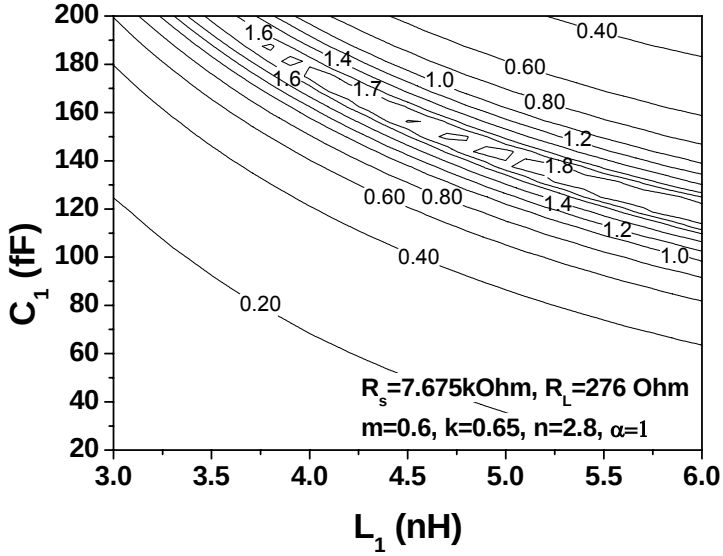


Fig. 4.18 Frequency response of TSMC inductors.

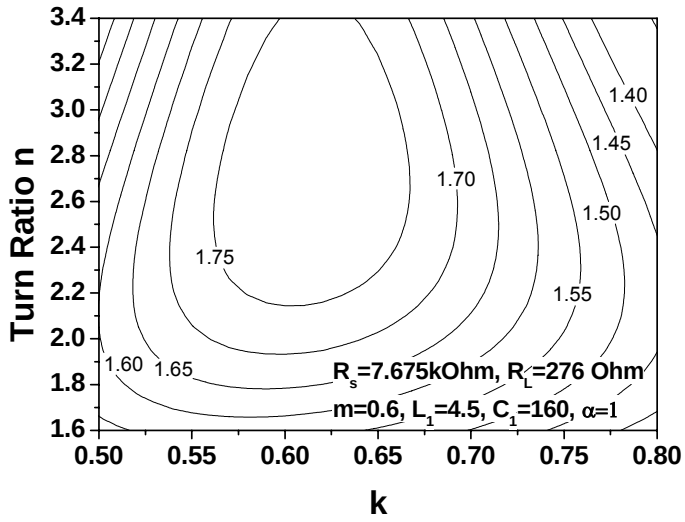
becomes larger which means a larger w_1. Then the C_1 would become smaller as shown in Fig. 4.17(a) and (b). When m is larger, even though w_2 is smaller, $w_1=mw_2$ is not necessary smaller since m increases. The m large case's gain is limited by the C_1 and achievable gain might be low.

By the inductor model of TSMC, one can estimate the parasitic capacitance of the transformer and then decide the parameters. Fig. 4.18 shows the frequency response of several inductors, by the resonant frequency of the inductor, the parasitic capacitance is estimated as 52fF for 4.7nH inductor. The parasitic of the transformer is expected to be larger than that of the inductor. Besides, the capacitance looked back into the LNA also needs to be considered. Then, the C_1 limit is set as 150fF for a 4.5nH inductor. Since the C_1 limit of higher k is smaller, and the gain level of higher k

case is close to smaller k case which is easier to fabricate, the parameters is chosen as m=0.6, k=0.65, L1=4.5nH, n=2.8 from Fig. 4.13(b) and 4.17(b), and correspondingly C_1=160fF, L_2=0.5nH, C_2=1.67pF. The calculated current gain is about 1.8.



(a)



(b)

Fig. 4.19 Gain sensitivity of the design point (a) Gain sensitivity to k and turn ratio of the selected design set (b) Gain sensitivity to L_1 and C_1 of the selected design set.

After the parameters have been decide, the gain variation due to the variation of the parameter values should be observed to find which parameter is more critical. Fig. 4.19 shows the gain variation. The L_1 and C_1 are more critical than n and k. The gain decreases quickly as the values depart from a limited range. Therefore, when design the transformer, the L_1 and C_1 value have to be the first priority.

What limits the current gain magnitude? One is the resistance of the metal line which is modeled by α. As shown in Fig. 4.20, the current gain is higher as the loss is less. Beside, the range of n for high gain is moved to higher region, but it is confined to be less than the square root of R_s/R_L. Therefore, the loss of the inductor is smaller is preferred.

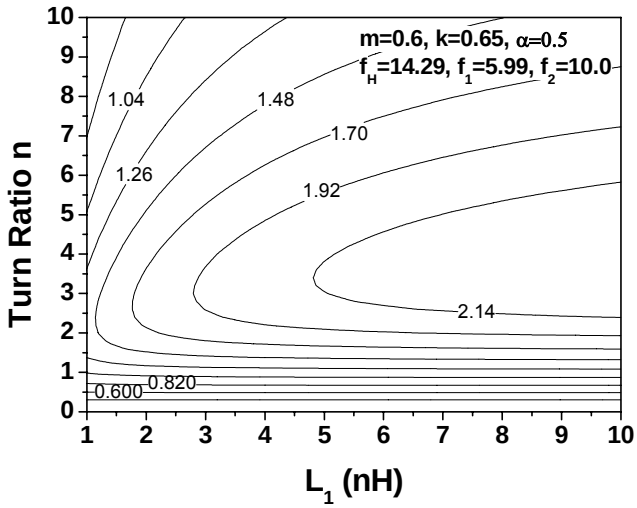


Fig. 4.20 Current gain relative to n and L_1. Solve f_L=5.5GHz with less loss

Another important factor affects gain is the source and load resistance ratio. It is desired that the source resistance is as large as possible and the load resistance is as

small as possible. As shown in Fig. 4.21, it is the current gain plot for R_s=7675 and R_L=50.

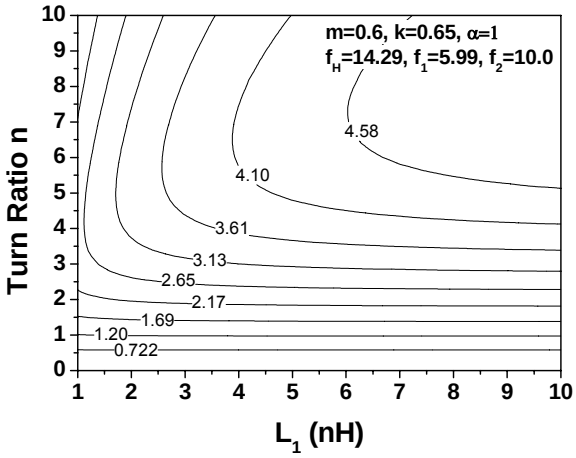


Fig. 4.21 Current gain relative to n and L_1. Set R_s to R_L ratio larger.

The current gain is higher than R_L=276 case, and the high gain region moves to higher n place. Therefore, one should make the source to load resistance ratio larger for better gain performance.

To show that the design according to resonant frequency solutions does gives relative high current gain, a simple program is written to calculate gain for sweep of all the possible combinations of variables: m, k, n, L_1 when C_1 limited to 150fF. TABLE 4.1 lists the highest gain for a given m, and the relative k, n, L_1 values. As shown, the f_L or f_H of these sets is close to 5.5GHz.

TABLE 4.1 Sweep variables to find maximum gain.

m	k	n	L1 (nH)	Gain	f_L (GHz)	f_H (GHz)
0.6	0.75	3	4.5	1.84	5.52	17.13
1	0.85	3.4	3	1.75	5.51	19.35
1.4	0.35	0.6	6.5	1.62	3.46	5.72

4.3.3 Physical Dimension Design of the Transformer

The self-inductance for a straight planar rectangular conductor according to [18] is

$$L = 2\ell[\ln(2\ell / GMD) - 1.25 + AMD/\ell + (\mu/4)T] \quad (4\text{-}19)$$

L is the inductance in nanohenries, ℓ is the conductor length in centimeters, geometric mean distance (GMD) and arithmetic mean distance (AMD) represent the geometric and arithmetic mean distances, respectively of the conductor cross section, μ is the conductor permeability, and T is a frequency-correction parameter which is almost equal to 1 for thin film and microwave frequencies. GMD is the distance between two imaginary filaments normal to the cross section of the conductor, whose mutual inductance is equal to the self-inductance of the conductor. AMD is the average of all possible distance within the cross section. For thin-film inductors with rectangular sections, GMD is 0.2232(a+b) and AMD is (a+b)/3. (4-19) reduces to

$$L = 2\ell[\ln[2\ell/(a+b)] + 0.50049 + [(a+b)/3\ell]] \quad (4\text{-}20)$$

The inductance of a straight line is approximate proportional to the length of it. For a=8um, b=2.34um case, as shown in Fig. 4.22. The calculated (4-20) for this case is shown in Fig. 4.23.

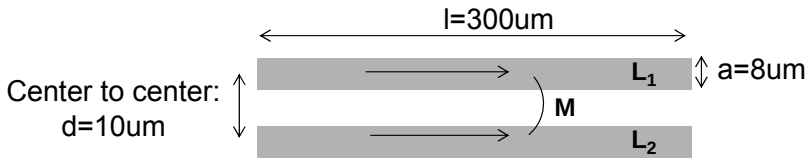


Fig. 4.22 Two parallel straight conductor with coupling between them.

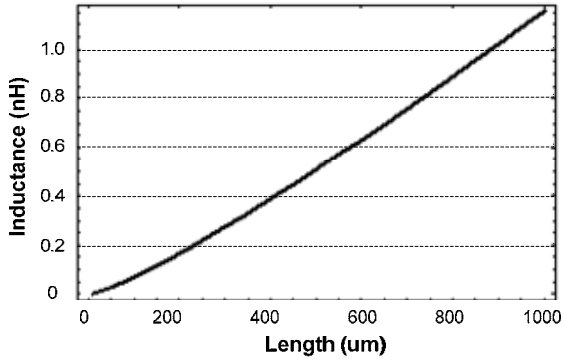


Fig. 4.23 Inductance magnitude varies with length for a straight inductor.

The mutual inductance between two parallel conductors is a function of the length of the conductors and of the geometric mean distance between them. In general, according to [18],

$$M = 2\ell Q \tag{4-21}$$

where M is the mutual inductance in nanohenries, Q is the mutual-inductance parameter,

$$Q = \ln\{(\ell / GMD) + [1 + (\ell^2 / GMD^2)]^{1/2}\} - [1 + (GMD^2 / \ell^2)]^{1/2} + (GMD / \ell) \tag{4-22}$$

GMD is the geometric mean distance between the two conductors, which is approximately equal to the distance d between the track centers. The exact value is

$$\ln GMD = \ln d - \{[1/12(d/w)^2] + [1/12(d/w)^4] + [1/60(d/w)^2] + [1/168(d/w)^6] + [1/360(d/w)^8] + [1/660(d/w)^{10} + ...]\} \tag{4-23}$$

Consider for Fig. 22, take these parameters into equations with 2.34um thickness, the self inductance of one straight inductor is about 0.274nH and the mutual conductance between these two conductors is about 0.191nH. The mutual conductance is positive in this case, since the current flow in each of the pairs is in the same direction. The

coupling coefficient k is about 0.697. This example gives us an idea of the magnitude level of the self-inductance of two inductors separated 10um.

The total inductance L_T of a coil can be written as

$$L_T = L_O + M_+ - M_- \tag{4-24}$$

where L_O is the sum of the self-inductances of all the straight segments, M+ is the positive mutual inductance when current flow in two parallel conductors is in the same direction, and M- is that when opposite direction. For a planar spiral inductor, M- is mainly attributed from the opposite segments which is much far than the nearby segments that have current in the same direction, so the radius of the spiral inductor shouldn't be too small, or the total inductance will degrade due to the negative term. Assume the center to center distance of Fig. increases to 300um from 10um, the

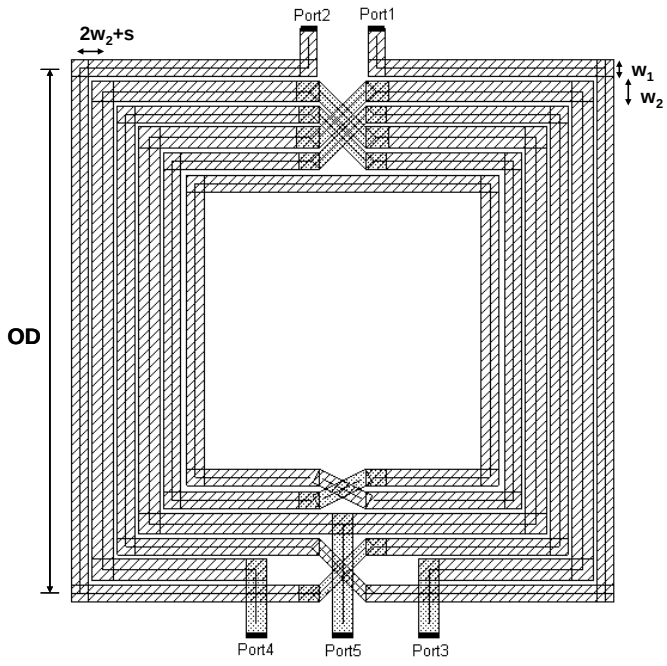


Fig. 4.24 Structure schematic of the transformer.

mutual inductance becomes 0.028nH which is much lower than 0.191nH for 10um separation.

From last section, the transformer should satisfy the following requirements:

k=0.65, L1=4.5nH, n=2.8

Since the self-inductance of a straight line is almost proportional to its length, a transformer with physical turn ratio as 4 to 1 between primary turn and one of the secondary turn is designed as shown in Fig. 24. The square root of the physical turn ratio is only 2, but the width of primary turn can be set larger than the secondary turn. Moreover, when the mutual inductance is taken into consideration, the turn ratio is expected to be closer to what is required. As from the calculation in former paragraphs, the separation between turns is around 10um for k consideration and outside dimension is around 250um from L_1 requirement.

The actual character of the transformer needs to be checked with EM simulation tool. In this design, Ansoft Designer helps the verification and only few times of iterations are required to find optimum physical dimension since it should be close to the estimation. The dimension of the transformer is chosen as:

OD=260um, w_1=8um, w_2=10um, s=1um.

The extracted value for this transistor's model as shown in Fig. 4.12 is:

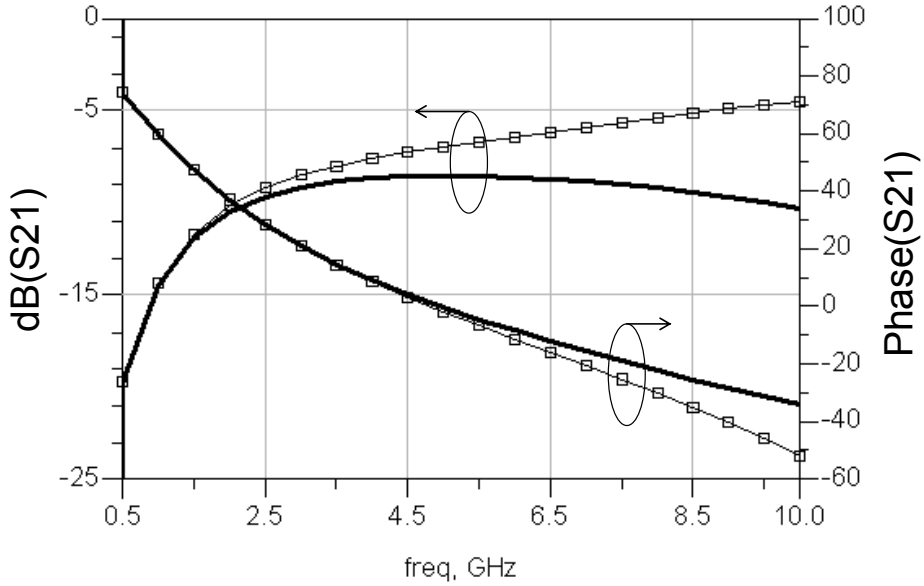


Fig. 4.25 Comparison of the extraction and model's frequency response.

k=0.642, n=2.76, L_1=4.408nH, L_2=0.578nH, R_1=8.043Ω, R_2=2.414Ω

Fig. 4.25 is the comparison of S21 between extracted model's and the simulation of EM tool's frequency response. The simulation current gain of the front-end circuit with S parameter extracted from Designer is about 2.1 while the calculated value is 1.8.

The model for the transformer is very simplified since a complex one is not useful for calculation. Therefore, there exists certain calculation difference between the model and the fabrication result.

4.5 Chip Implementation and Measured Result

The die micrograph of the front-end circuit fabricated in 0.18-um RF CMOS technology is shown in Fig. 4.26. The size of the chip is 1.16×0.75 mm^2 including bonding pads.

Measurements were conducted by the similar approach for mixer. The supply voltage V_{DD} is set as 0.6V in the measurements. The total DC power consumption is

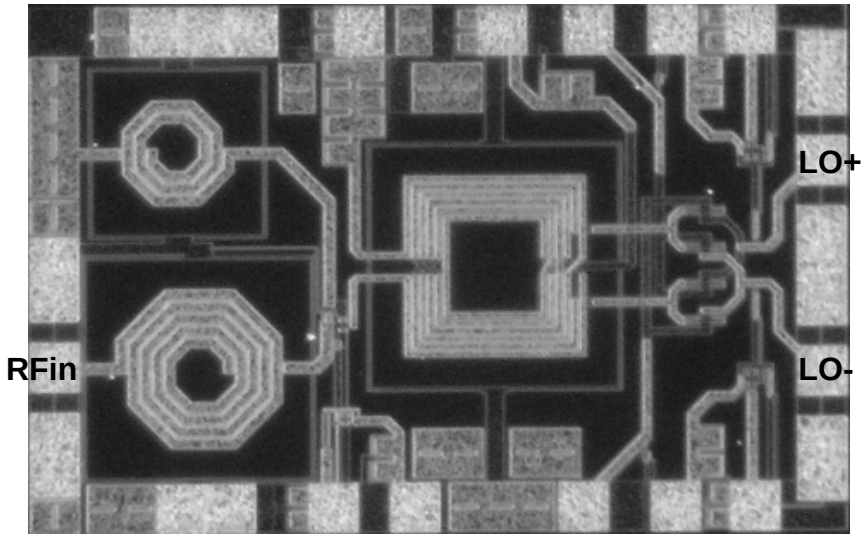


Fig. 4.26 Micrograph of the front-end circuit.

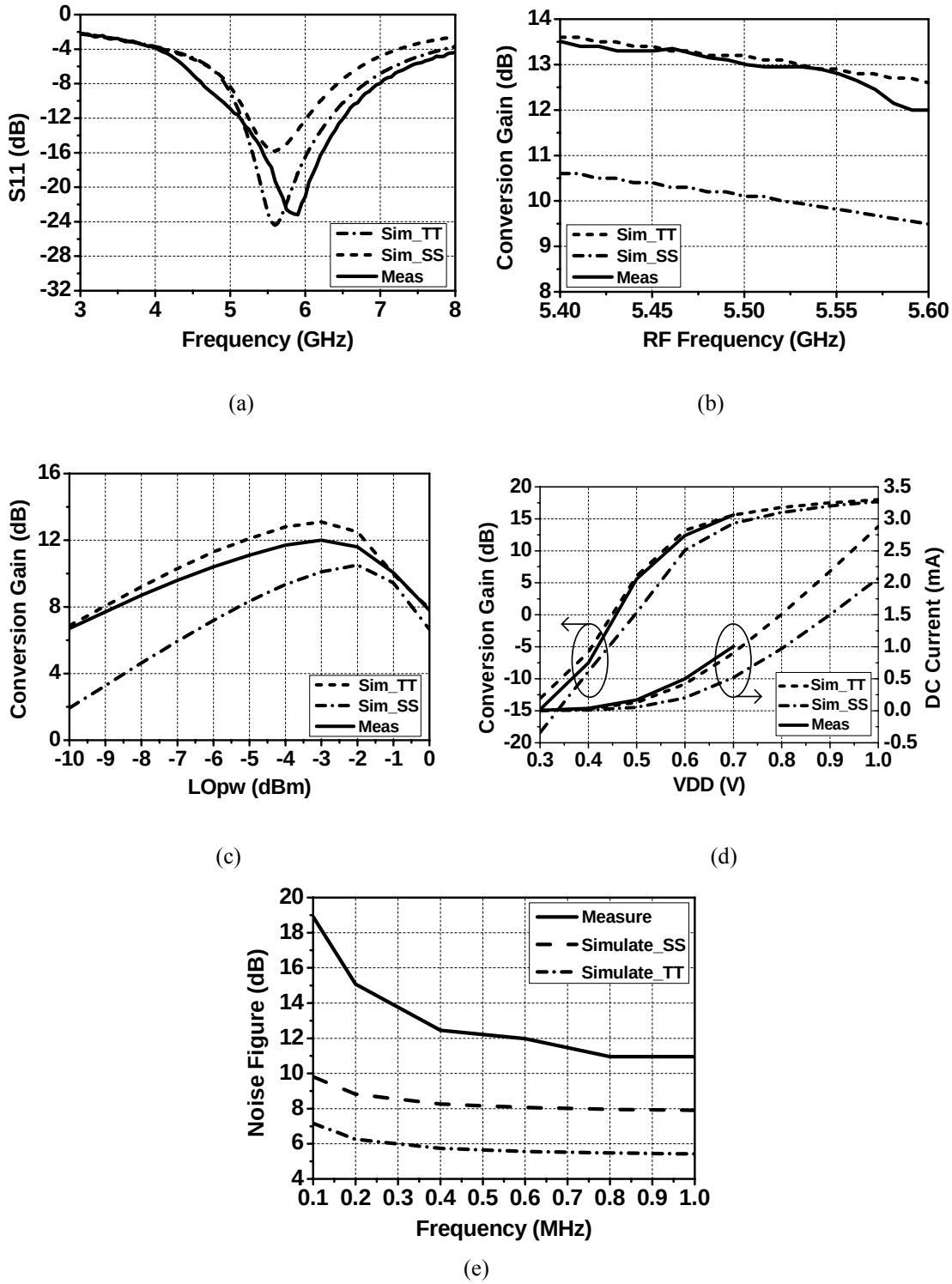


Fig. 4.27 Front-end measured result (a) S11 (b) Conversion gain (c) Conversion gain versus LO power (d) Conversion gain and DC current versus V_{DD} (e) Noise figure (DSB).

only 0.29mW. The measured and the simulated input return loss centered at 5.5 GHz are shown in Fig. 2.27(a). The measured S11 is better than -10 dB within the wanted

frequency band. It is found on the Smith chart that the frequency response is similar to the simulated one, though the impedance is a little higher at the center frequency. The RF signal is down-converted to 1 MHz. The measured conversion gain is 12 dB as depicted in Fig. 4.27(b). It is close to the simulation in Typical-Typical corner case. The maximum gain condition is corresponding to LO power as -3dBm as shown in Fig. 4.27(c). Fig. 4.27(d) shows the conversion gain and DC current with different V_{DD}. Two-tone test is done for measuring third-order intermodulation distortion. The measured IIP3 is about -2.8dBm. In the measurement, LO power is given as -3dBm, and the power consumption of active mode is 0.68mW. The measured noise figure is 11.0dB. Measurement is done through noise floor magnitude read from the instrument. The setup is shown in Fig. 4.28. The gain of the pre-amplifier and circuit under test, the noise figure of pre-amplifier, and the noise contributed by IF amplifier (unit gain buffer) and all the connected devices are measured and used to calculate for the noise figure of the front-end circuit. The measured noise figure is about 3 dB higher than the simulated result under slow-slow corner case.

IIP3 depends on the loading impedance of the MOS as shown in Fig. 4.29(a). The optimum bias point is 0.55V for the chosen MOS size when the load impedance is around 600 Ohm. This bias point chosen is observed to be in the moderate inversion region. The measured and simulation IIP3 versus LNA's gate voltage of the front-end

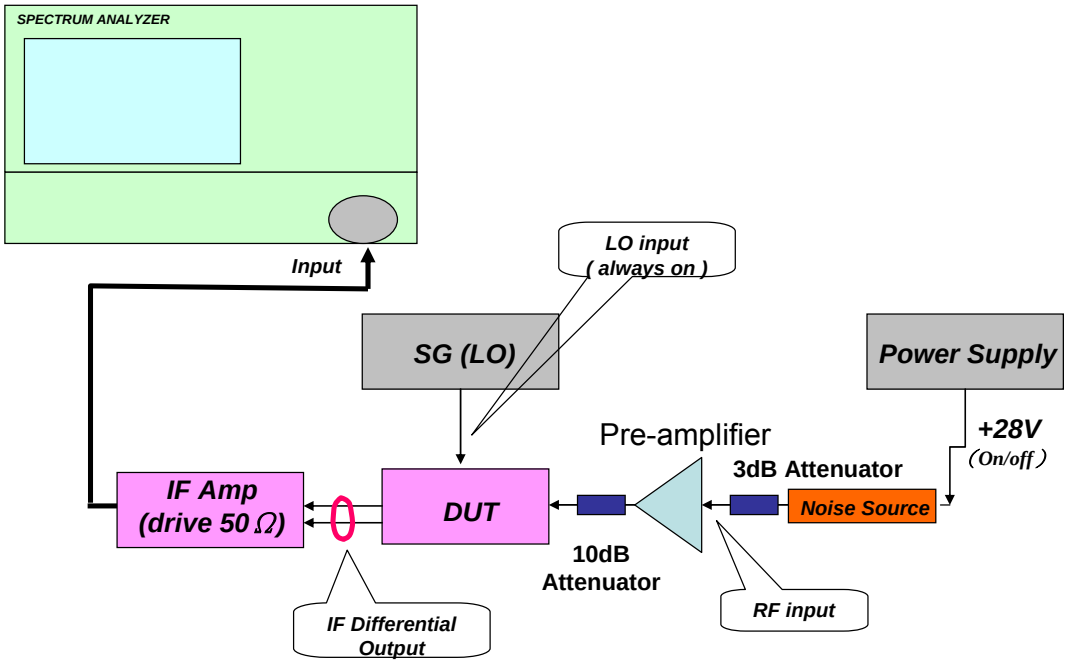
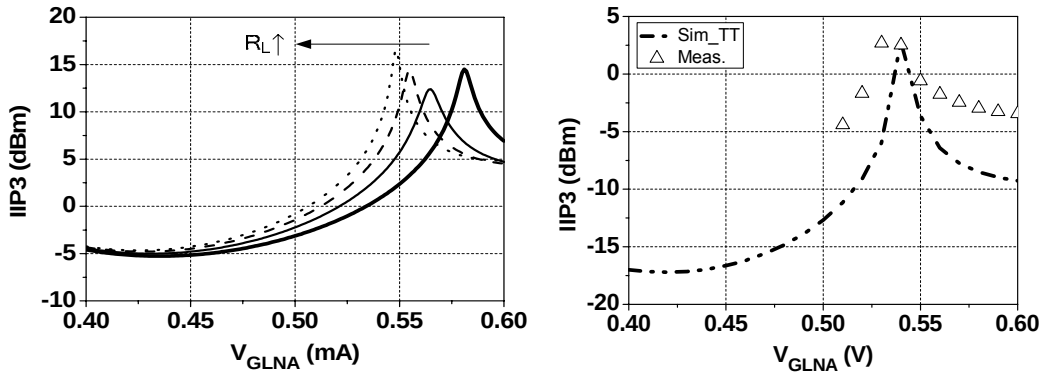


Fig. 4.28 Noise measurement setup.

circuit is shown in Fig. 4.29(b). The highest point is about 0.54V which is around that of a single transistor. The measured IIP3 and conversion gain at 0.54V is 2.5dBm and 10dB, respectively. The linearity is improved about 5dB while trades 2dB conversion gain.

A modified version has taken this into consideration. Moreover, LO power

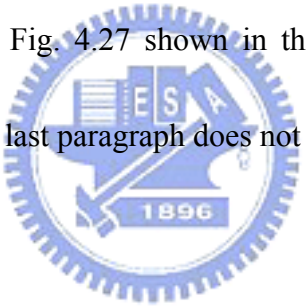


(a) (b)

Fig. 4.29 IIP3 relative to load resistance (a) IIP3 of a transistor for different load resistance. (b)

consumption has also been lowered down. In this circuit, the circuit operates at LO power equal to -3dBm. The LO voltage amplitude at the gate of mixing pair is about 0.25V which is quite high under 0.6V supply. The modified version operates at LO power as low as -7.5dBm. The LO voltage amplitude at the gate of mixing pair is about 0.15V only.

The simulated conversion gain of the circuit in Fig. 4.27 is not high. This is much less than the original result which was used as the fabrication basis. The conversion gain of it was about 19dB. But there was something wrong with the original file when the simulation tool upgraded. Fig. 4.27 shown in the thesis has been redone. The modified version mentioned in last paragraph does not have this issue.



4.6 Summary

In this work a 5-GHz receiver front-end circuit is designed for the application of wireless sensor networks. The circuit topology is chosen available for low supply voltage as low as 0.6V. An On-chip transformer with current conversion gain is analyzed and designed to convert single-ended signal from the single transistor LNA into differential form to benefit from double balanced mixer structure. A figure of merit for LNA is also presented for the optimum design condition under low supply voltage case.

Realized in 0.18-um CMOS technology, the measured input return loss and voltage conversion gain are 16.9dB and 12dB, respectively. The input third-order intercept point (IIP3) is -2.8dBm while consuming only 0.29mW from a 0.6V supply. Table III summaries the measured results of this work and compares the performance with other three circuits. Among these, [19] is composed of a differential LNA and a double balanced mixer designed for low power purpose. [3] also adopts transformer for current conversion. [20] is a single balanced low power receiver front-end. As compared to the three circuits, this work has comparable gain and linearity while consuming the lowest power and lower supply voltage.

TABLE 4.2 also lists the simulation performance of the modified version. The bias condition of the LNA stage is selected at the high figure of merit point. The linearity

is improved and the simulation result is 3dBm. LO power is cut down to -9dBm, 6dB short as compare to the first version. Though the DC power consumption is close to the former work, the operation power consumption is improve, about 1/2 times of that of the original circuit.

TABLE 4.2

Summary of measured performance and comparison to other front-end circuits.

Item	This Work	Modified (sim_TT)	Ref[19]	Ref[3]	Ref[20]
Technology	CMOS 0.18um	CMOS 0.18um	CMOS 0.18um	SiGe-BiCMOS 0.35um	CMOS 0.18um
RF Frequency (GHz)	5.5	5.5	5.8	5.8	5
DC Supply Voltage (V)	0.6	0.6	1.5	1.8	1
Conversion Gain (dB)	12	17.6	15.7	14	25
IIP3 (dBm)	-2.8	3.0	-20.56	-1.6	-6.5
Noise Figure (dB)	11.0	8.8	4.8	-	12
Power Dissipation (mW)	0.29*	0.21**	17.2	13.8	0.87

* Power dissipation for standby mode. The power consumption for active mode is 0.68mW.

** Power dissipation for standby mode. The power consumption for active mode is 0.34mW.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

Two circuits, fabricated in TSMC 0.18um RF CMOS technology, are proposed for the application of wireless sensor networks. One is a low power double-balanced mixer which is composed of a transconductance stage with phase splitting function and PMOS switching pairs in the folded topology. The output balance and noise contribution conditions of the transconductance stage have been analyzed theoretically and designed accordingly. The measured voltage conversion gain is 10.4dB and the total power consumption of it is 2mW from a 1V supply.

Another circuit is a 5-GHz receiver front-end circuit whose topology is chosen to suit the application of low supply voltage and low power consumption. A transformer in resonant operation is designed to have current transformation gain and to convert signal into differential form while consumes zero extra power. Besides, a single transistor low noise amplifier is adopted and carefully designed. The measured result shows the voltage conversion gain is 12dB and the total power consumption of this work is greatly cut down to only 0.29 mw from a 0.6V supply.

5.2 Future Work

About the first circuit, the frequency response of the mixer has a potential to be extended for broadband application since the input matching and output balanced condition has neglected dependence on frequencies when frequencies are low as compare to f_T. The LC tank must be dismissed and replaced by an element that has broader frequency response, an inductor, for example.

For the second circuit, the physical limitation of the fabricated transformer has set a design constraint for the resonant operation current transfer gain or equivalently the total conversion gain of the front-end circuit. MENS transformers that have less parasitic capacitances due to the etched silicon substrate are favored to replace normal planar transformer in the circuit in the future.

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2. Tatao Hsu, Yen-Lin Liu, Shu-Hui Yen, and Chien-Nan Kuo, "Sub-mW 5-GHz Receiver Front-End Circuit Design," *the 18th VLSI Design/CAD Symposium*, Hualien, August 2007.