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碩士論文

以準分子雷射退火製作控制晶界位置之雙閘極複晶矽薄膜電晶體之研究

Study on the Polycrystalline Silicon Thin-Film Transistors with Location-Controlled Grain Boundary and Double Gate Structure Using Excimer Laser Annealing

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指導教授：鄭晃忠 博士　Dr. Huang-Chung Cheng

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以準分子雷射退火製作控制晶界位置之雙閘極

複晶矽薄膜電晶體之研究

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摘要

近年來，複晶矽薄膜電晶體成為顯示技術的關鍵元件，除了可以應用在系統面板(System on a Panel, SOP)上，於三維積體電路的實現具備相當大的應用潛力。雖然透過準分子雷射可有效的提升複晶矽薄膜電晶體複晶矽層的結晶性，但此方法仍有些許缺點，如隨機的晶界分佈、較窄的製程窗口等等。在這篇論文裡，我們將提出一種易於控制的結晶方式，並利用該結晶方式配合雙閘極結構來增進複晶矽薄膜電晶體的特性。

在第一個部分，我們稱為梯台式通道結晶法(Elevated Channel Method)之側向結晶方式將被用於製作控制晶界位置之複晶矽薄膜通道並加以探討，我們將介紹

此種單晶界複晶矽薄膜電晶體成長機制。因為底閘極結構梯台邊緣區域提供了較厚非晶矽層，而在準分子雷射退火時得以扮演晶種的角色。當雷射能量密度控制使得較薄的元件通道區域全融，且接近角落較厚的區域半融，如此一來，由通道兩邊側向成長的晶粒沿著相對的方向往通道中間成長，進而在通道的中心只形成單一晶界，因而得到大型的晶粒以提升元件的效能。各種各樣的分析方法也將用來探討晶界控制之複晶矽薄膜層，由掃描式電子顯微鏡，穿透式電子顯微鏡的分析中可知，我們觀察到大約 0.6μm長的人為控制晶粒。

我們也利用該結晶方式，製作出雙閘極低溫複晶矽薄膜電晶體，並對其電特性加以研究。在沒有任何氫化的處理之下，其N型元件之等效載子移動率更超過1000 cm^2/V-s，而P型元件則超過 340 cm^2/V-s。我們觀察到元件的均勻性也被提升，在量測二十個元件之下，載子移動率的標準差小於 50 cm^2/V-s，臨界電壓的標準差小於 0.16 V，次臨界擺幅之標準差則小於 0.04 V/decade。而透過雙閘極之結構，我們也觀察到較為陡峭之次臨界擺幅以及較小的汲極誘導能障下降(DIBL)。此外，相較於傳統結晶方式之上閘極薄膜電晶體，我們也獲得八倍以上之驅動電流。

儘管雙閘極結構之複晶矽薄膜電晶體表現出良好的電特性，然而在量測中發現部分元件之漏電流的問題卻相當嚴重。我們認為漏電流來自於上下兩個閘極在微影製程造成的不對稱，導致一些隨著梯台式通道結晶法形成的小晶粒在強閘極逆偏壓時被空乏區所覆蓋，導致當汲極端施加強電場時，一些缺陷中被捕捉的電子釋放出來而形成漏電流，因此為了解決此問題，我們提出了低汲極摻雜(Lightly Doped Drain, LDD)之雙閘極薄膜電晶體結構，以降低汲極端之電場，將漏電流抑制下來以提升電流開關比。然而低汲極摻雜也導致轉導衰退與驅動電流減小，因此我們亦引入了上閘極內縮之結構，以避開小晶粒的方式，在不影響轉導與驅動電流等電性情況下，達到抑制漏電流之效果。

Study on the Polycrystalline Silicon Thin-Film Transistors with Location-Controlled Grain Boundary and Double Gate Structure Using Excimer Laser Annealing

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ABSTRACT

In recent years, polycrystalline silicon (poly-Si) thin-film transistors (TFTs) were the key devices in flat-panel displays , System on a panel (SOP), and three dimensional integrated circuits (3D-ICs) applications. Although conventional top-gate poly-Si TFTs by excimer laser crystallization was an effective technology to improve the crystallinity of polycrystalline silicon thin films, there were still some drawbacks such as random grain boundaries, narrow process window, etc. In this thesis, we introduced so called elevated channel method to control the grain growth and the location of grain boundary. With the aid of this method and double gate structure, the high performance double gate poly-Si TFTs had been fabricated to obtain single grain boundary in the channel region.

In the first part, single grain boundary (SGB) double gate (DG) thin-film

transistors fabricated by excimer laser annealing were investigated. The mechanisms of elevated channel thin films were studied. A thick amorphous silicon region was formed in the both sides of elevated channel on the bottom gate which served as the seeds for the lateral grain growth during excimer laser irradiation. As the laser energy density was controlled to completely melt the thin region in the channel and partially melt the thick region near the corner, the lateral grain growth starting from the sides of elevated channel could progress along the direction toward the center of channel region. There was only one longitudinal grain boundary in the center of the channel. Thus, a large-grain polycrystalline silicon thin film which would lead to improved device performance was obtained. Various analyses were also performed to investigate the elevated channel thin films. From the analyses of scanning electron microscope (SEM), transmission electron microscope (TEM), large longitudinal grains artificially grown were observed to be about 0.6 μm.

Electrical characteristics of single grain-boundary double-gate TFTs were also studied. High-performance SGB-DG-TFTs with equivalent field-effect mobility exceeding 1000 $cm^2/V\text{-}s$ for n-channel TFTs and 340 $cm^2/V\text{-}s$ for p-channel TFTs have been fabricated without any hydrogenation treatment. The uniformity was also improved by this method. If twenty SGB-DG-TFTs devices were taken into discussion, the standard deviation of equivalent field-effect mobility was smaller than 50 $cm^2/V\text{-}s$ and the standard deviation of Vth was smaller than 0.16 V, while that of subthreshold swing was smaller than 40 mV/decade. By means of double gate structure, we obtained steeper subthreshold swing and superior drain-induced-barrier-lowering (DIBL). Furthermore, SGB-DG-TFTs provided 8 times higher driving current than conventional TFTs.

Although SGB-DG-TFTs exhibited high performance, leakage current issue was observed in some devices. The mechanism was demonstrated by the penetration of

depletion region to the small grain accompanied with the elevated channel structure. During off-state operation, high drain bias voltage causing strong lateral electric field would release the trap charges and lead to the leakage current. Therefore, we proposed two methods for the purpose of the alleviation of leakage current, lightly doped drain (LDD) structure and shrunk gate engineering. For the LDD, the on/off current ratio was increased while the driving current was sacrificed. Therefore, we developed the shrunk gate engineering to achieve the goal of the suppression of leakage current without any sacrifice of transconductance and driving current.

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Contents

Abstract (in Chinese)……………………………………………………………i

Abstract (in English)…………………………………………………………iii

Acknowledgements (in Chinese)………………..………………………………...vi

Contents…………………………………………………………………………...vii

Table Lists……………………………………………………………………… x

Figure Captions…………………………………………………………………xii

==

Chapter 1 Introduction……..…………………………………………………...1

1.1 Overview of Low-Temperature Polycrystalline Silicon Thin-Film Transistors

(LTPS TFTs)……………….……………………………………………………1

1.2 Overview of Crystallization of Amorphous Silicon Thin Films…………………..2

1.2.1 Solid Phase Crystallization of Amorphous Silicon Thin Films……………..2

1.2.2 Metal Induced Crystallization of Amorphous Silicon Thin Films…………3

1.2.3 Laser Irradiation Crystallization of Amorphous Silicon Thin Films……….4

1.3 Motivation………………………………………………………………………....5

1.3.1 Fabrication of Polycrystalline Silicon Thin Films with Single Grain

Boundary……………………………………………………………………..5

1.3.2 Polycrystalline Silicon TFTs with Double Gate Structure by Elevated

Channel Process…………………………………………………………...6

1.3.3 Suppression of Leakage Current with Lightly Doped Drain Structure…..…7

1.4 Thesis Organization……………………………………………………………..8

Chapter 2 Fabrication of Location-Controlled Single Grain Boundary (SGB) and

Double Gate (DG) Polycrystalline Silicon (Poly-Si) Thin-Film

Transistors (TFTs) by Elevated Channel Methods Using Excimer Laser Annealing (ELA)…………………………………………………….....9

2.1 Introduction……………………………………………………………………..9

2.1.1 Introduction to Elevated Channel Methods………………………………...9

2.1.2 Introduction to Single Grain Boundary and Double Gate Polycrystalline Silicon Thin-Film Transistors Fabricated by Elevated Channel Method….12

2.2 Material Analyses of Single Grain Boundary Polycrystalline Silicon Thin Films Fabricated by Elevated Channel Methods………………………………………. 13

2.2.1 Process Flow of Material Analyses of SGB Poly-Si Thin Film Fabricated by Elevated Channel Method ………………………………………....13

2.2.2 Material Analysis of SGB Poly-Si Thin Film Fabricated by Elevated Channel Method……………………………………………………….....14

2.2.2.1 Scanning Electron Microscope (SEM) Analysis…………………14

2.2.2.2 Transmission Electron Microscope (TEM) Analysis………….....16

2.3 Fabrication and Electrical Characteristics Analyses of Single Grain Boundary (SGB) and Double Gate (DG) Polycrystalline Silicon (Poly-Si) Thin-Film Transistors (TFT) Fabricated by Elevated Channel Method……………………17

2.3.1 Process Flow of SGB-DG-TFTs by Elevated Channel Method…………17

2.3.2 Electrical Characteristics of SGB-DG-TFTs by Elevated Channel Method…………………………………………………………………...18

2.3.2.1 Electrical Characteristics of SGB-DG-TFTs……………………..18

2.3.2.2 Uniformity Investigation on SGB-DG-TFTs ……………………21

2.3.2.3 Dependence of Effective Field Effect Mobility on Applied Laser Energy Density……………………………………………………..22

2.3.2.4 Activation Energy for Carrier from Source to Drain……………23

2.4 Summary………………………………………………………………………24

Chapter 3 Investigation of the Characteristics of Single Grain Boundary Low-Temperature Polycrystalline Silicon Thin-Film Transistors with Double Gate Structure……………………………………………………26

3.1 Introduction………………………………………………………………26

3.2 Comparisons of Electrical Characteristics between Top Gate, Bottom Gate and Double Gate TFTs Fabricated by Elevated Channel Method ……………………27

3.1.1 Process Flow of Top Gate, Bottom Gate and Double Gate TFTs …………27

3.1.2 Electrical Characteristics Analysis and Comparison of Single Gate Devices and Double Gate Devices……………………………………………………..29

3.3 Leakage Current Issue and Suppression…………………………………………30

3.3.1 Leakage Current Mechanism………………………………………………30

3.3.2 Suppression of Leakage Current Using Lightly Doped Drain (LDD) Structure……………………………………………………………………31

3.2.2.1 Introduction…………………………………………………………...31

3.2.2.2 Process Flow of DGTFTs with LDD………………………………32

3.2.2.3 Electrical Characteristics Analysis of DGTFTs with LDD………...33

3.3.3 Suppression of Leakage Current Using Shrunk Gate Engineering………...33

3.2.3.1 Introduction…………………………………………………………...33

3.2.3.2 Process Flow of DGTFTs Using Shrunk Gate Engineering ……….34

3.2.3.3 Electrical Characteristics Analysis of DGTFTs Using Shrunk Gate Engineering……………………………………………………...35

3.4 Summary……………………………………………………………………....36

Chapter 4 Conclusions……………………………………………...…………37

References……………………………………………………………………...89

Vita……………………………………………………………………………..99

Table Lists

Table 2-1 Average of twenty measured electrical characteristics of n-channel SGB-DG-TFTs crystallized with elevated channel method and conventional top gate structure. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping).

Table 2-2 Average of twenty measured electrical characteristics of n-channel SGB-DG-TFTs crystallized with elevated channel method and conventional top gate structure. The thickness of gate oxide was 1000Å. The number of laser shots was 20(ie. 95% overlapping).

Table 2-3 Average of twenty measured electrical characteristics of p-channel SGB-DG-TFTs crystallized with elevated channel method and conventional top gate structure. The thickness of gate oxide was 1000. The number of laser shots was 10(ie. 90% overlapping).

Table 2-4 Electrical characteristics of twenty measured n-channel SGB-DG-TFTs crystallized with elevated channel method and conventional top gate TFTs. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping)

Table 2-5 Electrical characteristics of twenty measured p-channel SGB-DG-TFTs crystallized with elevated channel method and conventional top gate TFTs. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping)

Table 3-1 Electrical characteristics of p-channel top/bottom/double gate poly-crystalline silicon TFTs crystallized by elevated channel method. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping)

Table 3-2 Electrical characteristics of n-channel double gate polycrystalline silicon TFTs with LDD crystallized by elevated channel method. The thickness of gate oxide was 1000Å. The number of laser shots was 20(ie. 95% overlapping)

Table 3-3 Electrical characteristics of n-channel double gate polycrystalline silicon TFTs with shrink gate crystallized by elevated channel method. The thickness of gate oxide was 1000Å. The number of laser shots was 20(ie. 95% overlapping)

Figure Captions

Chapter 2

Fig. 2-1 (a) The schematic illustration of the low energy regime corresponding to energy densities that partially melting the a-Si thin film

Fig. 2-1 (b) The schematic illustration of the high energy regime corresponding to energy densities that completely melting the a-Si thin film

Fig. 2-1(c) The schematic illustration of the super lateral growth regime corresponding to energy densities that nearly completely melting the a-Si thin film

Fig. 2-2 SEM graph of poly-Si by conventional ELA process in SLG regime

Fig. 2-3 Process flow of preparing samples for material characteristics by elevated channel method

Fig. 2-4 The schematic illustration of the excimer laser system.

Fig. 2-5 SEM graphs of excimer laser crystallized polycrystalline silicon by elevated channel method. The channel length was varied from 1μm to 1.5 μm. The bottom poly gate thickness was 1000Å and the gate oxide thickness was 500Å. The laser energy density was 510 mJ/cm^2

Fig. 2-6 SEM graphs of excimer laser crystallized polycrystalline silicon by elevated channel method. The channel length was 1.2 μm. The poly gate thickness was 1000Å and the gate oxide thickness was 500Å. The laser energy density was (a) 470 (b) 490 (c) 510 mJ/cm^2.

Fig. 2-7 SEM graphs of excimer laser crystallized polycrystalline silicon by elevated channel method. The channel length was (a)1 (b)0.8 (c)0.7 μm. The poly gate thickness was 1000Å and the gate oxide thickness was 500Å. The laser energy density was 310 mJ/cm^2.

Fig. 2-8 Cross-section TEM graphs of excimer laser crystallized polycrystalline silicon by elevated channel method.

Fig. 2-9 Cross-section TEM graphs of excimer laser crystallized polycrystalline silicon by elevated channel method.

Fig. 2-10 Process flow for fabrication of SGB-DG-TFTs

Fig. 2-11 Transfer characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 0.8 μm, in which the thickness of gate oxide was 1000 Å. The number of laser shots was 10 (ie. 90% overlapping).

Fig. 2-12 Transfer characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

Fig. 2-13 Transfer characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1.2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

Fig. 2-14 Transfer characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1.5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

Fig. 2-15 Transfer characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

Fig. 2-16 Transfer characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

Fig. 2-17 Transfer characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 0.8 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping).

Fig. 2-18 Transfer characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping).

Fig. 2-19 Transfer characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1.2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping).

Fig. 2-20 Transfer characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1.5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping).

Fig. 2-21 Transfer characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping).

Fig. 2-22 Transfer characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping).

Fig. 2-23 Transfer characteristic of p-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 0.8 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

Fig. 2-24 Transfer characteristic of p-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

Fig. 2-25 Transfer characteristic of p-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1.2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

Fig. 2-26 Transfer characteristic of p-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1.5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

Fig. 2-27 Transfer characteristic of p-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

Fig. 2-28 Transfer characteristic of p-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

Fig. 2-29 Output characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 0.8 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

Fig. 2-30 Output characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

Fig. 2-31 Output characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1.2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

Fig. 2-32 Output characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1.5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

Fig. 2-33 Output characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

Fig. 2-34 Output characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

Fig. 2-35 Output characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 0.8 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping).

Fig. 2-36 Output characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping).

Fig. 2-37 Output characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1.2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping).

Fig. 2-38 Output characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1.5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping).

Fig. 2-39 Output characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping).

Fig. 2-40 Output characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping).

Fig. 2-41 Output characteristic of p-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 0.8 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

Fig. 2-42 Output characteristic of p-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

Fig. 2-43 Output characteristic of p-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1.2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

Fig. 2-44 Output characteristic of p-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1.5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

Fig. 2-45 Output characteristic of p-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

Fig. 2-46 Output characteristic of p-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

Fig. 2-47 Alleviated kink effect by n-channel SGB-DG-TFTs rather than conventional TFTs. The channel length was 0.8 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

Fig. 2-48 Statistics and uniformity of equivalent field effect mobility. Twenty n-channel SGB-DG-TFTs crystallized with elevated channel method and conventional top gate TFTs were measured. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping)

Fig. 2-49 Statistics and uniformity of threshold voltage. Twenty n-channel SGB-DG-TFTs crystallized with elevated channel method and conventional top gate TFTs were measured. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping)

Fig. 2-50 Statistics and uniformity of subthreshold swing. Twenty n-channel SGB-DG-TFTs crystallized with elevated channel method and conventional top gate TFTs were measured. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping)

Fig. 2-51 Statistics and uniformity of equivalent field effect mobility. Twenty p-channel SGB-DG-TFTs crystallized with elevated channel method and conventional top gate TFTs were measured. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping)

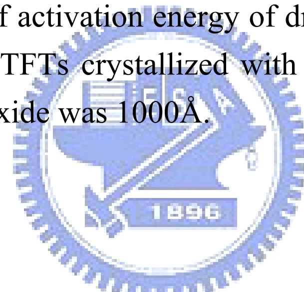
Fig. 2-52 Statistics and uniformity of threshold voltage. Twenty p-channel SGB-DG-TFTs crystallized with elevated channel method and conventional top gate TFTs were measured. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping)

Fig. 2-53 Statistics and uniformity of subthreshold swing. Twenty p-channel SGB-DG-TFTs crystallized with elevated channel method and conventional top gate TFTs were measured. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping)

Fig. 2-54 The dependence of equivalent field effect mobility on laser energy densities for n-channel SGB-DG-TFTs crystallized with elevated channel method and conventional TFTs. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping).

Fig. 2-55 The dependence of activation energy of drain current on gate bias voltage for n-channel SGB-DG-TFTs crystallized with elevated channel method. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping).

Fig. 2-56 The dependence of activation energy of drain current on gate bias voltage for n-channel DG-TFTs crystallized with solid phase crystallization. The thickness of gate oxide was 1000Å.



Chapter 3

Fig. 3-1 Process flows for fabrication of SGB-TG-TFTs

Fig. 3-2 Process flows for fabrication of SGB-BG-TFTs

Fig. 3-3 Transfer characteristic of p-channel top/bottom/double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1 μm, in which the thickness of gate oxide was 1000 Å. The number of laser shots was 10 (ie. 90% overlapping).

Fig. 3-4 Output characteristic of p-channel top/bottom/double gate polycrystalline silicon TFTs crystallized using elevated channel method and conventional TFTs with channel length of 1 μm, in which the thickness of gate oxide was 1000 Å. The number of laser shots was 10 (ie. 90% overlapping).

Fig. 3-5 The leakage current issue of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1 μm, in which the thickness of gate oxide was 1000 Å. The number of laser shots was 20 (ie. 95% overlapping).

Fig. 3-6 TEM observation of double gate polycrystalline silicon TFTs crystallized using elevated channel method, in which the thickness of gate oxide was 1000 Å.

Fig. 3-7 The leakage current issue of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method measured from Vg = -15V to Vg= 15V with channel length of 1 μm, in which the thickness of gate oxide was 1000 Å. The number of laser shots was 20 (ie. 95% overlapping).

Fig. 3-8 The leakage current issue of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method measured from Vg = -20V to Vg= 20V with channel length of 1 μm, in which the thickness of gate oxide was 1000 Å. The number of laser shots was 20 (ie. 95% overlapping).

Fig. 3-9 SEM graphs of excimer laser crystallized polycrystalline silicon by elevated channel method. The channel length was varied from 1μm to 1.5 μm. The bottom poly gate thickness was 1000Å and the gate oxide thickness was 500Å. The laser energy density was 510 mJ/cm^2

Fig. 3-10 Process flows for fabrication of SGB-DG-TFTs with LDD Structure

Fig. 3-11 Transfer characteristic of n-channel double gate polycrystalline silicon LDD TFTs crystallized using elevated channel method with channel length of 1 μm, in which the thickness of gate oxide was 1000 Å. The number of laser shots was 20 (ie. 95% overlapping).

Fig. 3-12 Output characteristic of n-channel double gate polycrystalline silicon LDD TFTs crystallized using elevated channel method with channel length of 1 μm, in which the thickness of gate oxide was 1000 Å. The number of laser shots was 20 (ie. 95% overlapping).

Fig.3-13 Process flows for fabrication of SGB-DG-TFTs with Shrunk Gate Engineering

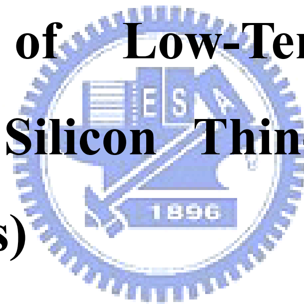
Fig. 3-14 In-line SEM observation of shrunk gate.

Fig. 3-15 Transfer characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with shrunk gate, in which the thickness of gate oxide was 1000 Å. The number of laser shots was 20 (ie. 95% overlapping).

Fig. 3-16 Output characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with shrunk gate, in which the thickness of gate oxide was 1000 Å. The number of laser shots was 20 (ie. 95% overlapping).

Chapter 1
Introduction

1.1 Overview of Low-Temperature Poly-crystalline Silicon Thin-Film Transistors (LTPS TFTs)



Thin-film transistors (TFTs) have become crucial devices of modern Active Matrix Liquid Crystal Displays (AMLCDs) and Active Matrix Organic Light Emitting Diodes (AMOLEDs) applications [1.1]-[1.5].

Generally, amorphous silicon (a-Si:H) TFTs are the pixel switching elements in AMLCD industry. Amorphous silicon TFTs exhibit low leakage current because of their high off-state resistivity. In addition, they are compatible with large glass substrate for low process temperature. However, the electrical characteristics of a-Si TFTs such as carrier mobility (typically below 1 cm^2/V-s) are inadequate for peripheral circuits . That is, additional integrated circuits (ICs) are needed to support the function of gate drivers and source drivers to drive a display panel. This will lead to high cost and poor reliability. On the other hand, low- temperature polycrystalline

silicon (LTPS) TFTs possesses superior carrier mobility [1.6], greater device reliability, CMOS process capability [1.7], and low temperature process compatibility. Therefore, LTPS TFTs have been investigated to achieve the goal of integrating peripheral circuit in a single panel, which is known as system on panel (SOP) [1.8]. Furthermore, LTPS TFTS have the potential to fulfill the 3-dimentional integrated circuits [1.9].

1.2 Overview of Crystallization of Amorphous Silicon Thin Films

The crystallinity of poly-Si thin film has great influence on the performance of poly-Si TFTs. For a poly-Si thin film, the grain boundaries cause a lot of defects, which is so called strained bonds and dangling bonds. These defects act as trap states within the band gap and will degrade the electrical characteristics of poly-Si TFTs, such as carrier mobility, threshold voltage, subthreshold swing, and the leakage current. Moreover, the poly-Si TFTs with many defects may suffer reliability issue. It is generally believed that the defects will be reduced by enlarging the grain size. There are several ways to enlarge the grain size, including solid phase crystallization, metal induced crystallization, and laser irradiation crystallization. These methods could be concluded that the a-Si thin films are recrystallized into poly-Si thin film by additional energy. However, there are some differences between these methods and will be introduced in the following three sections.

1.2.1 Solid Phase Crystallization of Amorphous Silicon Thin Films

The solid phase crystallization (SPC) method is intuitive, with which method the a-Si thin film can be crystallized by thermal annealing. With a view to compatibility with glass substrate, the a-Si thin film is deposited at 550℃ using silane (SiH_4). Then followed the SPC process, and the process temperature is kept at 600℃ in N_2 ambient, whereas the process time is about 24 hours [1.10]-[1.11].

The grain size of solid phase crystallized poly-Si thin film is several times larger than that of as-deposited poly-Si thin film. Besides, the surface morphology is much smoother in SPC poly-Si thin film than in as-doped ones. However, the SPC TFTs suffers a lot of intra-granular defects and result in a bad performance. The most important of all is the fact that the annealing time is too long and this will limit the throughput to fabricate poly-Si thin film.

1.2.2 Metal Induced Crystallization of Amorphous Silicon Thin Films

It has been reported that certain metals can induce the crystallization of a-Si thin film. The basic concept of metal induced crystallization (MIC) is furnace annealing, which is analogous to SPC. Compared to SPC, MIC is able to reduce the annealing temperature (<400℃) and process duration (<5hrs); that is, higher throughput can be obtained.

Several metals have been proposed to be applied to MIC process, such as aluminum (Al), aurum (Au), nickel (Ni), platinum (Pt). Among these metals, Ni is the candidate for mainstream industrial application. Nickel silicide will be formed during process and the crystallization of silicon will start. Owing to the very small mismatch (0.4%) of crystal lattice constant between the <111> orientation faces of nickel silicide and crystalline silicon, the defects in crystal can be minimized [1.12]-[1.15].

However, MIC suffers high leakage current because of the fact that metal residues cannot be avoided after MIC process. The residues act as metal contamination and offer leakage path under carrier transportation.

1.2.3 Laser Irradiation Crystallization of Amorphous Silicon Thin Films

The laser irradiation crystallization process may be the most promising for grain growth, for the glass substrate not being damaged during laser process [1.16]-[1.17]. The laser modes can mainly be divided into two types, pulse type and continuous wave laser type. The excimer laser emits in UV light region with short pulse duration (10-30ns) by the laser source of ArF, KrF, or XeCl (output wavelengths 193, 248, and 308nm, respectively) gas. On the other hand, the continuous wave (CW) laser emits in green light by the diode-pumped solid-state (DPSS) laser source of Nd:YVO_4 (532nm) [1.18].

The benefit of using excimer laser crystallization (ELC) is the strong optical absorption of a-Si thin film to UV lights. During ELC process, a-Si thin films absorb the light, then melt and recrystallize in a short period of time, forming poly-Si grain (~1 μm). For the volume expansion from liquid to solid phase, surface roughness (usually called protrusion) occurs after the ELC process. It has been reported that increasing the laser shots will reduce the protrusion and obtain better crystallinity. The definition of laser shots is the overlaps between each laser shot, i.e., 20 shots correspond to 5% overlap per shot. The poly-Si thin film fabricated by ELC suffers from narrow process window and instability of shot-to-shot laser energy, which lead to non-uniformity issue of grain structure.

Unlike ELC, poly-Si thin film fabricated by CW laser exhibits less protrusion and

better uniformity. The power instability is less than 1%, which is superior to that of excimer laser. The continuous wave characteristic makes it possible for grain to grow in a large longitudinal distance (tens of μm in average). However, the technology has not been well-development and is still under investigation in modern academic research.

1.3 Motivation

In order to fabricate high performance low-temperature polycrystalline silicon thin-film transistor, we introduce several aspects to improve the electrical characteristics of LTPS TFTs: to reduce defects of poly-Si thin film, to raise the gate control ability, and suppress the leakage current. From the view of reducing defects of poly-Si thin film, we introduced a simple method to fabricate high quality poly-Si thin film, which is so called **elevated channel structure**. When it comes to raising the gate control ability, we propose the double gate structure. The leakage current issue is investigated and alleviated by lightly doped drain structure.

1.3.1 Fabrication of Polycrystalline Silicon Thin Film with Single Grain Boundary

Although pulsed excimer laser crystallization (ELC) has been widely applied to recrystallize a-Si, narrow process window and the uniformity of crystallized poly-Si thin film are crucial problems. The excimer laser energy should be kept at a certain threshold value to make sure the a-Si thin film is nearly completely melted, which is so called "super lateral growth" (SLG) region; that is, ELC suffers narrow process window. In addition, the shot-to-shot laser energy of ELC is not stable enough and the seeds of crystallization distribute randomly during recrystallization. Consequently, the

ELC process comes out a non-uniform poly-Si thin film.

For the purpose of the issues mentioned above, many researches have been proposed to solve the problem, such as sequential lateral solidification (SLS), phase-modulated ELC, μ-Czochralski (so called grain filter) method, selectively enlarging laser crystallization (SELAX) technology, etc [1.19]-[1.22]. However, these methods are not compatible with the existing excimer laser annealing system or need complex process flows. Therefore, a simple method to control the direction of grain growth and the location of grain boundary has been developed in this thesis, which is called "**Elevated Channel Method**". In this method, we can artificially control the thermal gradient in selective region, which is the elevated region, (actually the channel region) formed by bottom gate structure. The step at the corner of bottom gate region is thicker than elsewhere of the other region. If the laser energy density is controlled to completely melt the thinner region and partially melt the thicker region, a lateral thermal gradient will determine the grain growth from the un-melting solid phase seeds towards the melting liquid phase region. For the whole thesis, the crystallization is based on this structure.

1.3.2 Polycrystalline Silicon TFTs with Double Gate Structure by Elevated Channel Process

It has been demonstrated that the performance of devices can be enhanced with multi-gate structure. These methods, including double gates, dual gates, tri-gates, Ω-gate, and surrounding gate…etc. [1.23]-[1.26], are concentrated on the extension of the field induced channel in the same area. By means of these methods, we can obtain better gate control ability and higher driving current than that of conventional top gate or bottom gate devices. The short channel effect can be alleviated with the strong gate

control ability if the channel region is fully depleted [1.27].

Among the methods mentioned above, the double gate structure is preferred in this thesis because of the compatibility with the elevated channel process. We use the step of the corner of bottom gate structure to control the grain growth and attain single grain boundary in channel region. Therefore the top gate dielectric and top gate electrode can be deposited in the following process. In the first part of this thesis, the device performance is investigated by the combination of elevated channel process and double gate structure.

1.3.3 Suppression of Leakage Current with Lightly Doped Drain Structure

Low-temperature polycrystalline silicon thin-film transistors suffer storage charge distortion as pixel switches or noise as circuit application if the leakage current is high. Therefore, the suppression of leakage current has become significant issue. The leakage mechanisms of LTPS TFTS have been investigated a lot and are related to the grain boundaries [1.28]-[1.29]. The trap states arisen from grain boundaries act as leakage path at high gate bias and drain bias. Most researches reveal that the lightly doped drain (LDD) or offset structure can eliminate the leakage current [1.30]. Hence, we introduce LDD structure to suppress the leakage current. In this thesis, the LDD structure is formed followed by the gate spacer and then the heavily doped implant. With LDD structure, the electric field near drain can restrain the leakage current from drain to source. In the second part of this thesis, the double gate TFTs with LDD structure are introduced to investigate the leakage current suppression.

1.4 Thesis Organization

In chapter 1, a brief overview of LTPS TFTs technology was given to explain the crystallization process. The motivations of this thesis were subsequently explained to introduce this thesis.

In chapter 2, experimental processes of elevated channel thin films were introduced. The mechanism of lateral growth of elevated channel thin films was proposed by material analysis. The material properties were analyzed by scanning electron microscope (SEM) and transmission electron microscope (TEM). Then experimental procedures of polycrystalline silicon thin-film transistors with double gate structure were introduced. The electrical characteristics, including the field-effect mobility, the subthreshold swing, the threshold voltage, and the uniformity were investigated.

In chapter 3, the double gate devices were compared with the top gate and bottom gate ones. Then the DGTFTs fabricated by elevated channel process were modified with lightly doped drain (LDD) structure and shrunk gate engineering with a view to suppression of leakage current. The process flows and the leakage current lowering mechanism would be discussed in detail.

Finally, conclusions were given in chapter 4.

Chapter 2
Fabrication of Location-Controlled Single Grain Boundary (SGB) and Double Gate (DG) Polycrystalline Silicon (Poly-Si) Thin-Film Transistors (TFTs) by Elevated Channel Methods Using Excimer Laser Annealing (ELA)

2.1 Introduction

2.1.1 Introduction to Elevated Channel Methods

Currently, high current-driving capability, low leakage current, and good uniformity of TFT characteristics are essential for the application of AMLCD, AMOLED, and 3-dimensional ICs [2.1]-[2.6]. Low-temperature polycrystalline silicon (LTPS) technology is the most promising method to fabricate high performance thin-film transistors (TFTs) on glass or plastic substrate [2.7]. In comparison with amorphous silicon (a-Si) TFTs, LTPS TFTs exhibit higher field effect-mobility and better reliability, which lead to higher driving current and better

stress resistance. Therefore, LTPS TFTs acting as pixel switches are allowed in smaller size; that is, higher aperture ratio is obtained. Furthermore, LTPS TFTs are compatible with complementary metal-oxide-semiconductor (CMOS) circuits which results in the alleviation of power consumption [2.8]. Consequently, the scan drivers, the data drivers, and even the processors are allowed to be integrated in a single glass substrate for the next generation of system on panel (SOP) application. As compared to high temperature polycrystalline silicon (HTPS) TFTs, the thermal budget of LTPS TFTs is much lower for the process temperature is below 200℃, which means that LTPS TFTs may open a new field for flexible microelectronics [2.9]. Accordingly, the cost of LTPS TFTs is much lower than that of HTPS TFTs.

In order to prepare LTPS thin films, several ways have been reported to date, including solid phase crystallization (SPC), metal induced lateral crystallization (MILC), and laser annealing [2.10]-[2.13]. Among these methods, the excimer laser annealing (ELA) may be the most promising one. The excimer laser emits in UV light region with short pulse duration (10-30ns) by the laser source of ArF, KrF, or XeCl (output wavelengths 193, 248, and 308nm, respectively) gas source. The strong optical absorption of UV light and small diffusion length during the laser pulse in silicon imply that high temperature can be produced and cause melting of silicon without significant damage of glass substrate [2.14]. In addition, ELA poly-Si films possess good crystallinity and few intra-grain defects due to the melt-regrowth process. During ELA process, the mechanism of grain growth is quite sensitive to the laser energy density. Fig. 2-1 schematically illustrates the grain growth corresponding to the different laser energy densities. As shown in Fig. 2-1 (a), if the laser energy density is too small to melt the whole a-Si thin film, vertical solidification occurs and the un-melted solid layer remains to be a-Si, while the melted Si layer transform into poly-Si with small grain size [2.15]. Refer to Fig. 2-1 (b), if the laser energy density is

large enough to completely melt the a-Si thin film, homogeneous nucleation occurs for deep supercooling, resulting in small grain size [2.16]. Only when the laser energy density is controlled around a certain threshold value will we obtain large grains whose size are as large as 1 μm in diameter, as shown in Fig. 2-1 (c). This is so called *Super Lateral Growth* (SLG) regime [2.17], which vividly illustrates the behavior of melted a-Si to recrystallize from very few un-melted Si residues to each other. For the very few residues as seeds, the lateral growth phenomenon causes large grain size.

However, there are some limits for the ELA process even though we control the laser energy density in SLG regime. First, the seeds of SLG regime appear randomly; that is, the location of grain and grain boundary cannot be controlled and thereafter the large variation of grain size. Fig. 2-2 reveals the non-uniformity of grain size. Second, a lot of process fluctuation factors exist, i.e., the pulse-to-pulse variation of excimer laser energy, the variation of a-Si film thickness, and the narrow process window of ELA process. Therefore, a novel method called *Elevated Channel Process* is proposed to enhance the uniformity of grain crystallinity and the location of grain and grain boundary. Moreover, with elevated channel process, we obtained much larger process window rather than that of conventional ELA process.

In this chapter, the experimental procedures of elevated channel process would be introduced. We studied the mechanism of lateral growth of elevated channel process by material analysis equipments. The material properties of elevated channel thin films were investigated by scanning electron microscope (SEM) and transmission electron microscope (TEM).

2.1.2 Introduction to Single Grain Boundary and Double Gate Polycrystalline Silicon Thin-Film Transistors Fabricated by Elevated Channel Method

High current-driving capability and good uniformity of TFT characteristics over a large area of glass substrate were imperative for devices aiming at AMLCD and AMOLED drivers and matrix [2.18]-[2.22]. Furthermore, they should be produced with low cost and high throughput. It was desired that the growth of high-quality large grain could be controlled in the device channel region from the viewpoint of device performance and uniformity. A novel process for high quality LTPS thin films for producing high-mobility polycrystalline silicon TFTs was described in the section above. We call this novel method, elevated channel method. With this method, single grain boundary (SGB) low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) with double gate (DG) structure were formed. There was only one longitudinal grain boundary in the center of the channel. Besides, it has been reported for integrated circuit (IC) application, a double gate device is expected to obtain ultimate high-performance ideal metal oxide semiconductor field-effect transistors (MOSFETs) [2.23]. Therefore, we can produce silicon-on-insulator-liked (SOI-liked) LTPS TFTs by means of introducing the double gate structure. Furthermore, another advantage of double gate structure is the enhancement of gate controlling ability. With enhanced gate controlling ability, the devices will exhibit high driving current, steeper subthreshold swing, and superior short-channel effect immunity [2.24]-[2.26].

In this section, the detail process flows of SGB-DG- TFTs were introduced. Then the electrical characteristics were measured by electrical parameter analyzer, Agilent 4156. Both the N-type and P-type SGB-DG-TFTs were fabricated in comparison to conventional ones. Moreover, the dependence of laser shots number and electrical

characteristics was investigated. Finally, statistics and uniformity of electrical characteristics exhibited the superiority of SGB-DG-TFTs rather than conventional top gate TFTs.

2.2 Material Analyses of Single Grain Boundary Polycrystalline Silicon Thin Films Fabricated by Elevated Channel Methods

2.2.1 Process Flow of Material Analyses of SGB Poly-Si Thin Films Fabricated by Elevated Channel Method

Detailed process flows of prepared samples were shown in Fig. 2-3. At first, in-situ doping phosphorus polycrystalline silicon thin films with thickness of 1000Å were deposited by pyrolysis of pure SiH4 and PH3 by low-pressure chemical vapor deposition (LPCVD) at 550℃ on oxidized silicon substrates with oxide thickness of 1 μm. Then, the doped polycrystalline silicon layer was defined to form polycrystalline silicon gate by transverse coupled plasma reactive ion etch (TCP-RIE). Next, a 500Å TEOS oxide layer was deposited as gate insulator by LPCVD at 700°C. After the deposition of bottom gate insulator, the 1000Å amorphous silicon layer was deposited as the active layer by LPCVD at 550℃ with SiH4 as gas source. The elevated channel was named after the channel region which is elevated for bottom gate structure. Laser crystallization was performed by KrF excimer laser (λ=248nm). The excimer laser system was shown in Fig. 2-4. During the laser irradiation, the samples were located on a substrate in a vacuum chamber pumped down to 10^{-3} Torr and the substrate was maintained at room temperature. The number of laser shots per

area was 20 (i.e., 95% overlapping) and laser energy density was varied. The grain structure of the crystallized polycrystalline silicon thin film was analyzed using scanning electron microscope (SEM) and transmission electron microscope (TEM). In order to facilitate the SEM observation, all the samples were processed by secco-etch before SEM analysis.

2.2.2 Material Analysis of SGB Poly-Si Thin Film Fabricated by Elevated Channel Method

2.2.2.1 Scanning Electron Microscope (SEM) Analyses

Fig. 2-5 shows SEM graphs of excimer laser crystallized polycrystalline silicon with elevated channel method. The channel length was (a) 1 μm (b) 1.2 μm and (c) 1.5 μm, respectively. The laser energy was 510 mJ/cm^2 and the poly gate thickness was 1000 Å. The longitudinal grains with 0.6 μm in length were formed in the channel region. It has been reported that lateral thermal gradient could arise as a result of the heat generated at moving solid-melting interface [2.27]. When a proper laser energy density irradiated the silicon thin film containing different thicknesses, the thin region in the channel region was completely melted while the thick region in the corner due to the step structures of bottom gate was only partially melted, leaving behind islands of solid material. As a result, grains would grow laterally towards the complete melting region from the retained solid seeds. The lateral growth would start from the still solid amorphous silicon spacer seeds and stretch toward the completely melted region until the solid-melt interface from opposite direction collided. Due to the in-situ design of thin channel region, the grain boundaries perpendicular to the current flow in the channel region could be reduced. Thus the field-effect mobility of

polycrystalline silicon TFTs could be greatly improved with this crystallization technique. When a longer channel length was adopted for crystallization, the laser fluence would have to be increased high enough to make the longitudinal grains collide with those grown from the other side; otherwise, small grains caused by spontaneous homogeneous nucleation would form in the center of the channel region as Fig.2-5 (c).

With a view to investigating the process window of elevated channel method, we altered the laser energy density irradiated on a-Si thin film. Fig.2-6 shows SEM graphs of poly-Si thin films with different laser energy densities while the channel length was kept at 1.2 μm. As the laser energy density was increased from 470 mJ/cm^2 to 510 mJ/cm^2, we obtained analogous gate structure in channel region. Therefore, we could conclude that the process window of elevated channel method is much larger than that of conventional excimer laser annealing on whole flat a-Si thin film.

It has been reported that thinner active layer can achieve the “fully depleted” device operation [2.28]. The electrical characteristics of fully depleted devices are much greater than partially depleted ones, such as alleviated kink effect, low threshold voltage, and more ideal subthreshold swing. In our experiment, thinner a-Si thin film (500Å) was also adopted to the elevated channel method. As shown in Fig.2-7, the laser energy density was controlled at 310 mJ/cm^2 to completely melt thinner region but partially melted thicker region. However, the a-Si thin film was too thin to keep thermal energy retained in the molten Si channel region and the severe supercooling phenomenon occurred which led to homogenous nucleation. In consequence, small grains were observed in the channel region instead of the lateral grain growth. Therefore, we must use a-Si thin film thickness of 1000 Å to prevent the homogenous nucleation for the purpose of enlarging poly-Si grains.

2.2.2.2 Transmission Electron Microscope (TEM) Analysis

Fig. 2-8 shows the cross-section TEM graphs of polycrystalline silicon thin film fabricated by elevated channel method in the channel region. From the Fig. 2-8, it could be found that single grain boundary was controlled artificially at the center of the channel region, and two large grains with very few intra-grain defects were observed. For polycrystalline silicon thin film used as active layer in thin-film transistor, fewer defects were desired. Meanwhile, the cross-section TEM graph of polycrystalline silicon thin film in the corner region the bottom gate shows that the thickness of the corner region became thinner than that in the channel region. From the correlated electron diffraction pattern of polycrystalline silicon thin film, the crystallinity of the polycrystalline silicon was analyzed. It could be found that as the channel region was selected, the diffraction spots become more obvious, which means that the crystallinity was good. When the corner region was selected, the ring was observed, which revealed that the vertical growth in the corner region of the grains exhibit poor crystallinity. But the corner regions would be heavily doped and act as the source/drain region of TFTs. Therefore, the poor crystallinity may not degrade the performance of LTPS-TFTs.

It is notable to keep an eye on the fact that the good crystallinity appeared not only in the channel region but also the regions at both sides away from the corner of bottom gate as shown in Fig. 2-9. This was analogous to the channel region that the thinner a-Si thin films at these sides were completely melted during laser irradiation, resulting in lateral growth of poly-Si grains. That is, we could obtain similar poly-Si grains with fewer defects except the channel. Therefore, elevated channel method has the potential of produce periodic poly-Si grains if the mask is well designed.

2.3 Fabrication and Electrical Characteristics Analyses of Single Grain Boundary (SGB) and Double Gate (DG) Polycrystalline Silicon (Poly-Si) Thin-Film Transistors (TFT) Fabricated by Elevated Channel Method

2.3.1 Process Flow of SGB-DG-TFTs by Elevated Channel Method

Detailed process flows of device fabrication were shown in Fig. 2-10. At first, in-situ doping phosphorus polycrystalline silicon thin films with thickness of 1000Å were deposited by pyrolysis of pure SiH4 and PH3 by low-pressure chemical vapor deposition (LPCVD) at 550˚C on oxidized silicon substrates with oxide thickness of 1μm. Then, the doped polycrystalline silicon layer was defined to form bottom gate by TCP-RIE. Next, a 1000 Å TEOS oxide layer was deposited as bottom gate insulator by LPCVD at 700˚C. After the deposition of bottom gate insulator, the 1000Å amorphous silicon layer was deposition as the active layer by LPCVD at 550 ℃ with SiH4 as gas source. Laser crystallization was performed by KrF excimer laser (λ=248nm). During the laser irradiation, the samples were located on a substrate in a vacuum chamber pumped down to 10^{-3} Torr and the substrate was maintained at room temperature. The number of laser shots per area was 10 or 20 (i.e., 90 or 95% overlapping) and laser energy density was varied. Next, the active region was defined by TCP-RIE. Then, a 1000 Å TEOS oxide layer was deposited as top gate insulator by LPCVD at 700˚C followed by in-situ doping phosphorus polycrystalline silicon

layer as top gate electrode. After the deposition of top polycrystalline silicon gate, the contact hole was defined and etched by TCP-RIE and 1:10 dilute Buffer Oxide Etch (BOE) solvent to interconnect top gate and bottom gate electrode. Next, a phosphorus/BF2 ion implantation with a dosage of 5×10^{15} cm^{-2} and energy of 40keV/70keV was performed to form source and drain regions. A 5500Å TEOS oxide layer was then deposited as passivation layer by LPCVD at 700℃ and the implanted dopants were activated by thermal annealing in furnace at 600°C for 9 hours. Then, contact hole opening by TEL5000-RIE and and metallization with Aluminum were carried out. Finally, Aluminum sintering was carried out at 400 ℃ to reduce the series resistance. No hydrogenation plasma treatment was performed during the device fabrication process. For comparison, conventional top-gate ELC polycrystalline silicon TFTs were also fabricated.

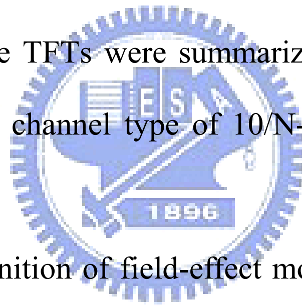
2.3.2 Electrical Characteristics of SGB-DG-TFTs by Elevated Channel Method

2.3.2.1 Electrical Characteristics of SGB-DG-TFTs

It has been demonstrated that large and longitudinal grains could be formed in the channel region by elevated channel method in section 2.1. The grain structure would have a significant influence on the electrical characteristics of the fabricated TFTs. Fig. 2-11~Fig. 2-16 show the typical transfer characteristics of n-channel SGB-DG-TFTs with channel lengths of 0.8 μm ~5 μm, in which the thickness of gate oxide was 1000Å and the number of laser shots per area was 10(i.e., 90% overlapping). Fig. 2-17 ~Fig. 2-22 show the typical transfer characteristics of n-channel SGB-DG-TFTs with channel lengths of 0.8 μm ~5 μm, in which the

thickness of gate oxide was 1000Å and the number of laser shots per area was 20(i.e., 95% overlapping). Fig. 2-23 ~Fig. 2-28 show the typical transfer characteristics of p-channel SGB-DG-TFTs with channel lengths of 0.8 μm ~5 μm, in which the thickness of gate oxide was 1000Å and the number of laser shots per area was 10.

The laser process conditions were optimized and the conventional top gate TFTs were included for comparison. The threshold voltage was defined as the gate voltage required to achieve a normalized drain current of I_d = (W/L)x10^{-8} A at $|V_{ds}|$ =0.1V. The equivalent field-effect mobility was extracted from the maximum transconductance in the linear region of I_d-V_g characteristics at $|V_d|$ = 0.1V (i.e., the formula of $\mu=g_m/[(W/L)V_{ds}Cox]$). The on/off current ratio was defined as the ratio of maximum drain current over minimum drain current at $|V_d|$ =3V. Several important electrical characteristics of the TFTs were summarized in Table 2-1, Table 2-2 and Table 2-3 for laser shots and channel type of 10/N-type, 20/N-type and 10/P-type, respectively.



It is notable that the definition of field-effect mobility of double gate TFTs was analogous to *HARA et al.* [2.29] in this thesis. The definition of field-effect mobility could be approached by two aspects. One was the physical meaning of carrier transport capability of poly-Si layer, which was defined by the following equation:

$$\mu = \frac{g_m}{\left(\frac{2W}{L}\right) \cdot C_{ox} \cdot V_{DS}} \qquad \text{..................(1),}$$

while the channel width was 2W because of the number of field induced channel was two.

The other definition was corresponding to the carrier transport capability in the occupied area of active region, which was defined by the following equation:

$$\mu^* = \frac{g_m}{\left(\frac{W}{L}\right) \cdot C_{ox} \cdot V_{DS}} \quad \text{.................(2),}$$

while the channel width was W because of the occupied width of active region was only W.

In this thesis, the latter definition was adopted; the name of "**equivalent field-effective mobility**" and the symbol of "**μ***" was used to avoid the confusion with the first definition.

According to Fig. 2-11~Fig. 2-28, the SGB-DG-TFTs exhibit superior electrical characteristics to those of conventional top-gate ones, especially in short channel devices. This could be attributed to the longitudinal grain and single grain boundary in the device channel region. Take the dimension of W = L = 1 μm and laser shots of 10 for example, SGB-DG-TFTs with equivalent field-effect mobility of about 720 cm^2/V-s could be achieved by using elevated channel method and double gate structure while the mobility of the conventional counterpart was about 79 cm^2/V-s. Aside from the enhancement of equivalent field-effect mobility, the gate controlling ability of double gate structure could be emphasized by the electrical characteristics of subthreshold swing and drain-induced-barrier-lowering (DIBL, which was defined as the difference of threshold voltage between $|V_d|$ =0.1V and $|V_d|$ =3V). In W = L = 1μm device, we obtained subthreshold swing of SGB-DG-LTPS-TFTs about 0.23V/decade, while that of conventional top gate TFTs was about 0.66V/decade. Similarly, the DIBL of SGB-DG-TFTs was lowered about 200mV rather than that of conventional top gate TFTs. In addition, although the maximum achievable length of lateral grain growth was limited between 0.6 μm as described in the previous section, the electrical characteristics of the TFTs with device dimension up to W = L = 5 μm were still superior to those of conventional ones. This could also ascribed to the long longitudinal grain growth at the channel edge even though many small grains resulted

from spontaneous nucleation exist in the channel center, forming a high series resistance in the middle of channel region as well.

Fig. 2-29 ~Fig. 2-46 display the output characteristics of SGB-DG-TFTs with laser shots and dopant type of 10shots/N-type, 20shots/N-type and 10shots/P-type, respectively. It was demonstrated that SGB-DG-TFTs provide about 8 times higher driving current than conventional ELC polycrystalline silicon TFTs under the same bias condition, especially in short channel devices.

It was reported that the trap center due to grain boundaries enhance kink effect [2.30]-[2.32]. The good crystallinity at the drain edge due to the artificial controlled grain also reduced the kink effect, especially in short channel devices. Fig. 2-47 elaborated more serious kink effect in conventional top gate TFTs than SGB-DG-TFTs.

2.3.2.2 Uniformity Investigation on SGB-DG-TFTs

In the previous section the superior performance of SGB-DG-TFTs than conventional top gate TFTs was highlighted. The uniformity issue of SGB-DG-TFTs would be discussed in this section.

Take the dimension of W = L = 1 and laser shots of for example, Fig. 2-48 ~Fig. 2-50 and Fig. 2-51~Fig. 2-53 show the comparison of equivalent field-effect mobility, threshold voltage, and subthreshold swing for the N-type and P-type devices respectively. Twenty-two TFTs were measured to investigate the device-to-device variation for each dimension, then twenty of which were chosen for the exclusion of unexpected extreme value under statistics. Table 2-4 and Table 2-5 list the average and standard deviation of electrical characteristics. For the accuracy to investigate the precise variation from the mean value, we introduced a parameter from statistics which is called coefficient of variance (C.V) and defined by the ratio of standard

deviation over mean value in percentage.

Referring to Fig. 2-48~ Fig. 2-53, the values of standard deviation of threshold voltage and subthreshold swing of SGB-DG-TFTs were smaller than those of conventional top gate TFTs, whether N-type devices or P-type devices. However, the value standard deviation of equivalent field-effect mobility seemed to reveal the worse uniformity of SGB-DG-TFTs rather than conventional ones. This illusion might have been reversed with the C.V. When it came to the C.V, we obtained about 7% mobility variation for SGB-DG-TFTs and about 17% mobility variation for conventional top gate devices. Therefore, we concluded that high performance SGB-DG-TFTs with good uniformity could be fabricated easily using elevated channel method with the number of laser shots 10. Therefore, the number of laser shots was reduced and the throughput and the yield could be increased.

2.3.2.3 Dependence of Equivalent Field-Effect Mobility on Applied Laser Energy Density

Fig. 2-54 displays the dependence of equivalent field effect mobility on laser energy densities for SGB-DG-TFTs and conventional ones. Compared to the conventional top gate TFTs, the SGB-DG-TFTs possessed wide process window by the investigation of mobility. We obtained high equivalent field effect mobility of SGB-DG-TFTs with laser energy densities varying from 470 to 530 mJ/cm^2, while high mobility of conventional ones was obtained only at 490 mJ/cm^2 in contrast. This result corresponded to the material analysis in this chapter that the seed at the corner of step remained partially melted if the laser energy ranged from 470 to 530 mJ/cm^2. Besides, the conventional TFTs exhibited good electrical characteristics only at 490mJ/cm^2 corresponding to the SLG regime.

2.3.2.4 Activation Energy for Carrier from Source to Drain

It has been reported that the leakage current mechanism of poly-Si TFTs at high negative gate and positive drain field is the carrier emission from source to drain in the depletion region [2.33]. With regard to the carrier emission, additional insight could be obtained from the temperature dependence of the drain current in the off state (i.e., V_g smaller than threshold voltage). The leakage current might be attributed to the carrier generation and recombination at the trap levels from the grain boundaries in depletion region. The temperature dependence of the carrier in equilibrium with the trapped charge could be given by the equation below:

$$I = I_0 \exp(-\frac{E_a}{kT}) \quad \text{..........(3),}$$

where I_o was constant independent of temperature, E_a was the drain current activation energy defined by the difference between conduction band and trap levels generated by grain boundaries within Fermi level. These trap levels were generally uniformly distributed around the midgap ($E_g/2$). In the off-state, the Fermi level would be swept to states within the trap further away from conduction band. On the contrary, the Fermi level would be closer to the conduction band in the on-state. Therefore, the measurement of the drain current as a function of temperature, drain bias and gate bias yielded the height of the potential barrier the carriers must overcome.

The activation energy was extracted from the equation (3). With the logarithmic scale of this model and the measurement of different temperature, the activation energy dependent on gate voltage could be extracted. Fig. 2-55 and Fig. 2-56 show the activation energy of SGB-DG-TFTs fabricated by elevated channel method and DG-LTPS-TFTs fabricated by solid phase crystallization (SPC), respectively. For low drain bias (V_d = 0.1V), the activation energy had a value of about 0.5eV for SGB-DG-TFTs and about 0.6eV for SPC-DG-LTPS-TFTs under negative gate bias.

The comparable potential barrier for drain current was intuitive for the electric field along the channel to be small so that the effect of trap states was not obvious. If the drain bias was 3V, the activation energy of SGB-DG-TFTs was about 0.4eV, while that of SPC-DG-LTPS-TFTs dropped to about 0.25eV when gate bias equaled -10V. The worse crystallinity of SPC poly-Si thin films exhibited lower potential barrier at off-state than poly-Si thin film fabricated by elevated channel method because of the aid of trap states attributed to more grain boundaries, which enhanced the leakage current in off-state.

2.4 Summary

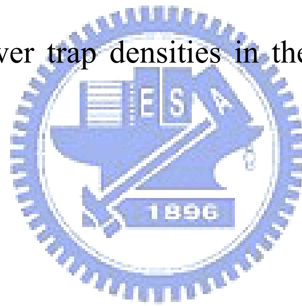
In this chapter, we successfully fabricated poly-Si thin-film transistors by elevated channel method. The material analyses of elevated channel thin films and the electrical analysis of SGB-DG-TFTs were carried out by SEM, TEM, and Agilent 4156 system.

In the first part, we introduce the mechanisms of elevated channel thin films. After that, various analyses were performed to investigate elevated channel thin films. From the analysis of SEM and TEM, large longitudinal grains about 0.6 μm were artificially grown in the channel region. Furthermore, the lateral grain growth starting from the seeds of corner region could progress until the opposite grain direction impinged and single grain boundary was controlled in the center of the channel region artificially.

In the second part, high-performance SGB-DG-TFTs with equivalent field-effect mobility exceeding 1000 $cm^2/V\text{-}s$ for N-type devices and 340 $cm^2/V\text{-}s$ for P-type devices had been fabricated with elevated channel method proposed in the first part. With the aid of artificial controlled grain by elevated channel method, alleviated kink effect and better uniformity were also observed. The standard deviation of mobility

was 45.8 cm^2/V-s, the standard deviation of V_{th} was 0.16V, and the standard deviation of subthreshold swing was 0.039V/decade for N-type devices; while those of P-type devices were 25.3cm^2/V-s, 0.16V, 0.03V/decade, respectively. The excellent uniformity with high performance could be attained even though the number of laser shots is 10. Therefore, the throughput and the yield could be increased.

The steeper subthreshold swing is also observed in double gate devices rather than conventional top gate ones. Furthermore, the DIBL of double gate devices was lower than conventional ones about 200mV. The conspicuous improvement of driving current (8 times higher driving current than conventional TFTs) attributed to double gate structure was also demonstrated. Finally, the activation energy from source to drain was investigated and revealed the poly-Si thin films fabricated by elevated channel method exhibited fewer trap densities in the channel region than SPC thin films.



Chapter 3
Investigation of the Characteristics of Single Grain Boundary Low-Temperature Polycrystalline Silicon Thin-Film Transistors with Double Gate Structure

3.1 Introduction

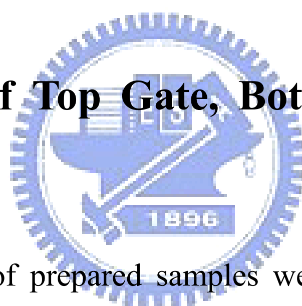
In last chapter, SGB-DG-LTPS-TFTs were fabricated by elevated channel method and the electrical characteristics were briefly investigated and compared to conventional top gate TFTs. In this chapter, we would introduce the elevated channel structure to the fabrication of top gate TFTs and bottom gate TFTs. It had been reported that the double gate structure would enhance the electrical characteristics rather than single gate devices [3.1]-[3.3]. By means of the fabrication of top gate, bottom gate, and double gate devices crystallized with elevated channel method, we would compare the electrical characteristics of this three different gate structures in the first part of this chapter.

In the second part of this chapter, we would investigate the leakage current of double gate devices. The enormous lateral electric field might enhance the leakage

current of short channel double gated TFTs. The detail of leakage current mechanism would be demonstrated. After the ascertainment of leakage current mechanism, we proposed two ways to suppress the leakage current of double gate devices. One was the lightly doped drain structure, the other was the shrunk gate engineering.

3.2 Comparisons of Electrical Characteristics between Top Gate, Bottom Gate and Double Gate TFTs Fabricated by Elevated Channel Method

3.1.1 Process Flow of Top Gate, Bottom Gate and Double Gate TFTs



Detailed process flows of prepared samples were shown in Fig. 3-1 and 3-2, which correspond to top gate devices and bottom gate devices respectively. The crystallization of polycrystalline silicon was carried out by elevated channel method. The process flows of double gate devices were demonstrated in chapter 2.

For the top gate devices, at first in-situ doping phosphorus polycrystalline silicon thin films with thickness of 1000 Å were deposited by pyrolysis of pure SiH4 and PH3 by low-pressure chemical vapor deposition (LPCVD) at 550℃ on oxidized silicon substrates with oxide thickness of 1μm. Then, the doped polycrystalline silicon layer was defined to form bottom dummy gate by TCP-RIE. Next, a 1000 Å TEOS oxide layer was deposited as dummy gate insulator by LPCVD at 700°C. After the deposition of gate insulator, the 1000Å amorphous silicon layer was deposition as the active layer by LPCVD at 550℃ with SiH4 as gas source. The elevated channel

structure was formed and then laser crystallization was performed by KrF excimer laser (λ=248nm). During the laser irradiation, the samples were located on a substrate in a vacuum chamber pumped down to 10^{-3} Torr and the substrate was maintained at room temperature. The number of laser shots per area was 10 (i.e., 90% overlapping) and laser energy density was varied. Next, the active region was defined by TCP-RIE. Then, a 1000 Å TEOS oxide layer was deposited as top gate insulator by LPCVD at 700°C followed by in-situ doping phosphorus polycrystalline silicon layer as top gate electrode. After the top gate electrode been defined, a BF2 ion implantation with a dosage of 5×10^{15} cm^{-2} and energy of 45keV was performed to form source and drain regions. A 5500Å TEOS oxide layer was then deposited as passivation layer by LPCVD at 700℃ and the implanted dopants were activated by thermal annealing in furnace at 600°C for 9 hours. Then, contact hole opening by RIE and metallization with Aluminum were carried out. Finally, Aluminum sintering was carried out at 400 ℃ to reduce the series resistance. No hydrogenation plasma treatment was performed during the device fabrication process. It should be mentioned that the top gate and bottom gate was not interconnected for the fabrication of top gate devices; the bottom gate acted as a dummy gate to achieve the crystallization of elevated channel method.

For fabrication of bottom gate devices, the process flows were analogous to that of top gate devices demonstrated above. The bottom polycrystalline gate was deposited by LPCVD at 550℃ with the in-situ doped phosphorus poly-Si layer on 1 μm oxidized silicon wafer and then defined by TCP-RIE, followed by 1000 Å TEOS oxide at 700℃. Then, 1000Å amorphous silicon layer was deposited as the active layer by LPCVD at 550℃ and annealed by KrF excimer laser irradiation at 10^{-3} Torr and room temperature. The number of laser shots per area was 10 (i.e., 90% overlapping) and laser energy density was varied. After the active region was defined by TCP-RIE, the source and drain regions were formed by BF2 ion implantation with

a dosage of 5×10^{15} cm^{-2} and energy of 45keV. A 5500Å TEOS oxide layer was then deposited as passivation layer by LPCVD at 700℃ and the implanted dopants were activated by thermal annealing in furnace at 600°C for 9 hours. Then, contact hole opening by dilute Buffered Oxide Etch (DBOE) and metallization with Aluminum were carried out. Finally, Aluminum sintering was carried out at 400 ℃ to reduce the seriess resistance. No hydrogenation plasma treatment was performed during the device fabrication process.

3.1.2 Electrical Characteristics Analyses and Comparisons of Single Gate Devices and Double Gate Devices

Fig. 3-3 shows the transfer characteristics of top gate, bottom gate and double gate devices crystallized by elevated channel method with channel length of 1μm and P-type carrier. For the comparison of bottom gate and top gate devices, the top gate TFTs exhibited higher leakage current than bottom gate ones. This might arise from the fact that the peak, or so called protrusion, occurred at the single grain boundary during the excimer laser irradiation. Two opposite lateral growth of liquid silicon collided with each other and the solidification with the expansion of volume would cause the protrusion with the height of several hundred angstroms [3.4]. Therefore, the gate insulator deposited near the protrusion region would not as thick as we imagined. The thinner oxide with the aid of the enhancement of electric field by protrusion eventually lead to the surface roughness issue, causing the higher leakage current in top gate devices. On the contrary, the bottom gate devices obtained lower leakage current attributed to smoother interface between active region and gate insulator.

For the comparison of double gate devices and top/bottom gate devices, we

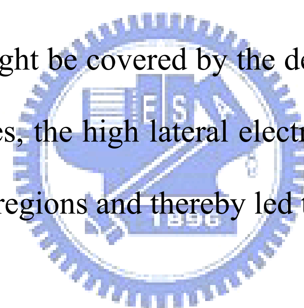
could refer to the extracted electrical characteristics listed in Table 3-1. The steeper subthreshold swing and superior DIBL revealed the enhanced gate controlling ability of double gate structure. The equivalent field-effect mobility of double gate TFTs was 352cm^2/V-s, while that of top gate TFTs and bottom gate TFTs was 197cm^2/V-s and 137cm^2/V-s, respectively. The driving current of double gate devices was almost the sum of top gate and bottom gate devices, as shown in Fig. 3-4. The output characteristic of conventional TFTs was also included in Fig. 3-4 for comparison. We found the driving current could be enhanced more than two times if the crystallization of elevated channel method was used.

3.3 Leakage Current Issue and Suppression

3.3.1 Leakage Current Mechanism

During the measurement of SGB-DG-LTPS-TFTs, we found there was serious leakage current issue in some devices. Fig. 3-5 indicates the leakage current issue at high drain bias and negative gate bias voltage. Many researches investigated the mechanism of leakage current [3.5]-[3.7]. In order to clarify it in a simple way, we demonstrated the mechanism of leakage current by the aspect of electric field. During device off-state operation, there were two direction of electric field applied in active region. One was the vertical field cause by gate electrode, while the other was lateral field along the direction of current transport. With the aid of TEM graph as Fig. 3-6, the leakage paths could be divided into vertical and lateral, which were correspond to the vertical and lateral electric field respectively. If we obtained a vertical leakage path, the gate current might be as large as the order of leakage current. However, by means of the measurement of gate current at high drain bias (i.e., V_d = 3V), we found

the gate current was on the order of PA, while the leakage current was on the order of nA as Fig. 3-7 and Fig. 3-8. Therefore, we excluded the hypotheses of the leakage path along with the vertical electric field by gate electrode. Therefore, the leakage current might be mainly on account of the lateral electric field. Referring to Fig. 3-6, the top gate electrode and bottom gate electrode were not completely aligned. Therefore, the heavily doped region which was implanted to form source and drain sides was not symmetric. From the SEM graph of Fig. 3-9, it could be observed that there were a lot of small grains near the step of the corner. Therefore, there might be some small grains in the channel region because of asymmetry of source and drain region. When the devices were operated in off-state region, the negative gate bias would generate depletion region in channel. Therefore, the small grain regions with many defects as trap states might be covered by the depletion region. If the high drain bias was applied to the devices, the high lateral electric field would cause the release of trap charges in small grain regions and thereby led to leakage current.



3.3.2 Suppression of Leakage Current Using Lightly Doped Drain (LDD) Structure

3.2.2.1 Introduction

It had been clarified that the leakage current of SGB-DG-LTPS-TFTs was attributed to the lateral electric field. Therefore, the reduction of electric field in drain junction might be a solution of leakage current reduction. A lot of methods have been proposed to reduce leakage current in TFTs, such as offset-gate structure [3.8], light doped drain (LDD) [3.9], and field-induced drain (FID) [3.10], gate overlapped LDD (GOLDD) [3.11] and so on. The LDD structure seemed to be a rather simple process

and the number of mask would not be increased. Therefore, the lightly doped drain structure was introduced to SGB-DG-LTPS-TFTs.

3.2.2.2 Process Flow of DGTFTs with LDD

Detailed process flows of prepared samples were shown in Fig. 3-10. At first, in-situ doping phosphorus polycrystalline silicon thin films with thickness of 1000 Å were deposited by pyrolysis of pure SiH4 and PH3 by low-pressure chemical vapor deposition (LPCVD) at 550°C on oxidized silicon substrates with oxide thickness of 1μm. Then, the doped polycrystalline silicon layer was defined to form bottom gate by TCP-RIE. Next, a 1000Å TEOS oxide layer was deposited as bottom gate insulator by LPCVD at 700°C. After the deposition of bottom gate insulator, the 1000Å amorphous silicon layer was deposition as the active layer by LPCVD at 550℃ with SiH4 as gas source. Laser crystallization was performed by KrF excimer laser (λ=248nm). During the laser irradiation, the samples were located on a substrate in a vacuum chamber pumped down to 10^{-3} Torr and the substrate was maintained at room temperature. The number of laser shots per area was 20 (i.e., 95% overlapping) and laser energy density was varied. Next, the active region was defined by TCP-RIE. Then, a 1000 Å TEOS oxide layer was deposited as top gate insulator by LPCVD at 700°C followed by 2500 Å in-situ doping phosphorus polycrystalline silicon layer as top gate electrode. After the deposition of top gate, the contact hole was defined and etched by TCP-RIE and 1:10 dilute Buffered Oxide Etch (DBOE) solvent to interconnect top gate and bottom gate electrode. Next, a phosphorus ion implantation with a dosage of 1×10^{13} cm^{-2} and energy of 30keV was performed to form LDD regions. Then 2500 Å TEOS oxide layer was deposited by PECVD at 385℃. After RIE etch back to form gate spacer, a phosphorus ion implantation with a dosage of 5×10^{15} cm^{-2} and energy of 30keV was performed to form source and drain regions. A

5500Å TEOS oxide layer was then deposited as passivation layer by LPCVD at 700℃ and the implanted dopants were activated by thermal annealing in furnace at 600°C for 9 hours. Then, contact hole opening by DBOE and and metallization with Aluminum were carried out. Finally, Aluminum sintering was carried out at 400 ℃ to reduce the series resistance. No hydrogenation plasma treatment was performed during the device fabrication process.

3.2.2.3 Electrical Characteristics Analyses of DGTFTs with LDD Structure

Fig. 3-11 exhibits the transfer characteristic of SGB-DG-LTPS-TFTs with LDD and without LDD, while Fig. 3-12 exhibits the output characteristic of which, and the summary of electrical characteristics were listed in Table 3-2. From the transfer characteristic we observed the leakage current was suppressed by slightly larger than an order of magnitude. However, the equivalent field-effect mobility of DGTFTs with LDD was also degraded to smaller than half that of DGTFTs without LDD. Therefore, the on/off current ratio was not increased too much. The sacrifice of driving current could be attributed to the large series resistance. Therefore, we would like to develop another method to reduce the leakage current without the degradation of on current. This method would be discussed in the next section.

3.3.3 Suppression of Leakage Current Using Shrunk Gate Engineering

3.2.3.1 Introduction

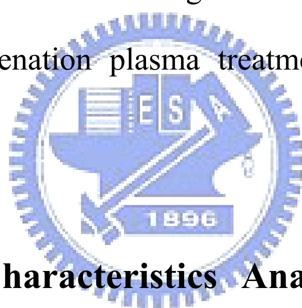
From the investigation of leakage current mechanism, the leakage current was

due to the penetration of depletion region into small grain region near the corner of bottom gate, which was inventible in elevated channel method. With a view to evading the gate coupling to the small grain region, we introduced the shrunk gate engineering. By means of lateral etching of top gate electrode, the shrunk gate could be achieved without any additional mask.

3.2.3.2 Process Flow of DGTFTs Using Shrunk Gate Engineering

Detailed process flows of prepared samples were shown in Fig. 3-13. At first, in-situ doping phosphorus polycrystalline silicon thin films with thickness of 1000 Å were deposited by pyrolysis of pure SiH4 and PH3 by low-pressure chemical vapor deposition (LPCVD) at 550°C on oxidized silicon substrates with oxide thickness of 1μm. Then, the doped polycrystalline silicon layer was defined to form bottom gate by TCP-RIE. Next, a 1000Å TEOS oxide layer was deposited as bottom gate insulator by LPCVD at 700°C. After the deposition of bottom gate insulator, the 1000Å amorphous silicon layer was deposited as the active layer by LPCVD at 550℃ with SiH4 as gas source. Laser crystallization was performed by KrF excimer laser (λ=248nm). During the laser irradiation, the samples were located on a substrate in a vacuum chamber pumped down to 10^{-3} Torr and the substrate was maintained at room temperature. The number of laser shots per area was 20 (i.e., 95% overlapping) and laser energy density was varied. Next, the active region was defined by TCP-RIE. Then, a 1000 Å TEOS oxide layer was deposited as top gate insulator by LPCVD at 700°C followed by 2500 Å in-situ doping phosphorus polycrystalline silicon layer as top gate electrode. After the deposition of top polycrystalline silicon gate, a 1000 Å TEOS oxide layer was deposited as hard mask layer for the gate shrinking engineering by LPCVD at 700°C. Then, the hard mask layer was defined by the mask of gate electrode by RIE, and the hard mask layer was over-etched by 1:10 dilute

Buffer Oxide Etch (DBOE) to form a lateral etch of about 0.15μm. After the strip of photo resistor, the top polycrystalline gate electrode was defined by TCP-RIE with the pre-patterned hard mask, and top gate insulator was then etched by DBOE with the in-situ strip of hard mask. Next, the contact hole was defined and etched by TCP-RIE and 1:10 dilute Buffer Oxide Etch (DBOE) solvent to interconnect top gate and bottom gate electrode. Then, a phosphorus ion implantation with a dosage of 5×10^{15} cm^{-2} and energy of 30keV was performed to form source and drain region. A 5500Å TEOS oxide layer was then deposited as passivation layer by LPCVD at 700℃ and the implanted dopants were activated by thermal annealing in furnace at 600°C for 9 hours. Then, contact hole opening by DBOE and and metallization with Aluminum were carried out. Finally, Aluminum sintering was carried out at 400 ℃ to reduce the series resistance. No hydrogenation plasma treatment was performed during the device fabrication process.



3.2.3.3 Electrical Characteristics Analyses of DGTFTs Using Shrunk Gate Engineering

Fig. 3-14 shows the in-line SEM observation of DGTFTs after the shrunk gate engineering. With the measurement of top gate length, the gate length defined to be 1μm was about 0.668μm, which corresponded to the lateral etch of 0.15μm shrinkage at each side along top gate.

Fig. 3-15 displays the transfer characteristic of SGB-DG-LTPS-TFTs with shrunk gate and without shrunk gate and the electrical characteristics were listed in Table 3-3, while the output characteristic was displayed in Fig. 3-16. We obtained an order suppression of leakage current without any sacrifice of transconductance and driving current. It should be noted that the equivalent mobility was not defined here because of the difference of top and bottom channel length.

3.4 Summary

In this chapter, we carry out the comparisons of single gate TFTs and double gate TFTs crystallized by elevated channel method. The leakage current issue of double gate devices was found and the mechanism was investigated, followed by the two solutions, lightly-doped-drain structure and shrunk gate engineering.

In the first part, top gate and bottom gate poly-Si TFTs was fabricated by elevated channel method. With the high field-effect mobility of 137 cm^2/V-s for P-type BG-TFTs and 197 cm^2/V-s for P-type TG-TFTs, we obtained high performance of single gate devices and thereby proved the application of elevated channel method to the top gate TFTs and bottom gate TFTs. Furthermore, the superior DIBL and subthreshold swing of double gate devices also certified the enhancement of gate controlling ability of double gate structure.

In the second part, the leakage current mechanism was demonstrated by the penetration of depletion region to the small grain accompanied with elevated channel structure. During off-state operation, high drain bias voltage causing strong lateral electric field would release the trap charges and led to leakage current. The leakage current was alleviated about an order by LDD structure. We found the series resistance degraded the driving current in on-state for LDD devices; therefore, shrunk gate engineering was introduced. With the analogous effect of LDD, the leakage current was also suppressed one order while the transconductance and driving current were not sacrificed.

Chapter 4
Conclusions

In this thesis, we had demonstrated the high performance double-gate polycrystalline silicon thin-film transistors fabricated by elevated channel method with excimer laser irradiation. The results and discussions were summarized in the chapter.

In chapter 2, material analyses were performed to investigate the poly-Si thin films fabricated by elevated channel method. The location-controlled grain boundary mechanism of elevated channel method was introduced at first. Then, from the analysis of scanning electron microscope (SEM) and transmission electron microscope (TEM), large longitudinal grains laterally grown in the channel regions measured to be about 0.6 μm were observed. Furthermore, the lateral growth starting from the both side regions of the elevated channel could progress along the opposite direction and single grain boundary was controlled in the center of the channel region artificially. This crystallization technique could be applied to the fabrication of short channel poly-Si TFTs. Then, the electrical characteristics of SGB-DG-TFTs fabricated by excimer laser annealing were studied. High-performance

SGB-DG-TFTs with equivalent field-effect mobility exceeding 1000 cm^2/V-s for the n-channel devices and 340 cm^2/V-s for the p-channel ones have been fabricated. Low kink current, wide process window, and improved throughput were obtained. The SGB-DG-TFTs exhibited better electrical characteristics than the conventional top gate ones, especially in the short channel devices owing to the artificially controlled lateral grain growth. In addition to the enhancement of TFT performance, TFTs crystallized with elevated channel method also demonstrated excellent uniformity. The standard deviation of mobility was smaller than 50 cm^2/V-s and the standard deviation of threshold voltage was smaller than 0.16V, while that of subthreshold swing was smaller than 40 mV/decade. By means of double gate structure, we obtained steeper subthreshold swing and superior drain-induced-barrier-lowering (DIBL) rather than conventional ones. Furthermore, SGB-DG-TFTs provided 8 times higher driving current than conventional TFTs.

In chapter 3, the elevated channel method was applied to the fabrication of top gate and bottom gate devices with a view to the comparison of double gate devices. We also obtained high performance single gate devices for the artificially controlled lateral grain growth. The double gate structure was proven again to exhibit superior gate controlling ability. Besides, we investigated the mechanism of leakage current, which was observed in some DG devices during measurement. During off-state operation, high drain bias voltage causing strong lateral electric field would release the trap charges of small grains near bottom gate corner and lead to leakage current. With a view to the alleviation of leakage current, we introduced the LDD structure at first. The leakage current was suppressed by an order of magnitude, but unfortunately the driving current was degraded due to the large series resistance. Therefore, we introduced another method, the shrunk gate, to avoid the couple of top gate electric field with small grain regions. We succeeded to suppress the leakage current by an

order of magnitude without any sacrifice of transconductance and driving current.

To sum up, the elevated channel method was attractive to fabricate the high performance TFTs, especially in the short channel devices. The electrical characteristics of TFTs fabricated by elevated channel methods exhibited high performance and good uniformity, whether in single gate or double gate structure. Furthermore, the double gate structure was proven to have steeper subthreshold swing, superior DIBL, large driving current, and high equivalent field-effect mobility. It is very promising to the future SOP and 3D-IC applications.

Table

10 shots Gate Oxide: 1000A	Mobility* (cm^2/V-s)	Subthreshold swing (V/dec)	Vth (V)	On/Off current ratio at Vds = 3 V
Conventional TFT (W/L = 0.8/0.8μm)	90	0.633	1.197	1.76E+07
DG-TFT (W/L = 0.8/0.8μm)	857	0.259	-0.491	4.57E+07
Conventional TFT (W/L = 1/1μm)	89	0.686	1.427	1.75E+07
DG-TFT (W/L =1/1μm)	660	0.264	-0.501	3.09E+07
Conventional TFT (W/L = 1.2/1.2μm)	92	0.659	1.275	2.20E+07
DG-TFT (W/L = 1.2/1.2μm)	668	0.304	-0.423	8.88E+08
Conventional TFT (W/L = 1.5/1.5μm)	78	0.702	0.895	3.78E+07
DG-TFT (W/L = 1.5/1.5μm)	414	0.359	-0.235	8.27E+06
Conventional TFT (W/L = 2/2μm)	76	0.731	2.38	2.94E+07
DG-TFT (W/L = 2/2μm)	288	0.486	1.038	2.15E+07
Conventional TFT (W/L = 5/5μm)	55	0.906	4.352	1.72E+07
DG-TFT (W/L = 5/5μm)	191	0.654	1.987	4.55E+05

Table 2-1 Average of twenty measured electrical characteristics of n-channel SGB-DG-TFTs crystallized with elevated channel method and conventional top gate structure. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping).

20 shots Gate Oxide: 1000A	Mobility* (cm^2/V-s)	Subthreshold swing (V/dec)	Vth (V)	On/Off current ratio at Vds = 3 V
Conventional TFT (W/L = 0.8/0.8μm)	178	0.514	-0.369	4.32E+06
DG-TFT (W/L = 0.8/0.8μm)	1004	0.374	1.024	1.99E+07
Conventional TFT (W/L = 1/1μm)	141	0.572	0.098	5.15E+06
DG-TFT (W/L =1/1μm)	970	0.327	0.996	2.26E+07
Conventional TFT (W/L = 1.2/1.2μm)	155	0.619	-0.042	8.84E+06
DG-TFT (W/L = 1.2/1.2μm)	944	0.362	0.597	4.08E+07
Conventional TFT (W/L = 1.5/1.5μm)	111	0.636	0.765	1.38E+07
DG-TFT (W/L = 1.5/1.5μm)	463	0.422	1.012	1.83E+07
Conventional TFT (W/L = 2/2μm)	86	0.706	1.482	1.52E+07
DG-TFT (W/L = 2/2μm)	365	0.448	0.919	2.07E+07
Conventional TFT (W/L = 5/5μm)	93	0.813	2.494	2.97E+07
DG-TFT (W/L = 5/5μm)	346	0.515	0.949	4.44E+05

Table 2-2 Average of twenty measured electrical characteristics of n-channel SGB-DG-TFTs crystallized with elevated channel method and conventional top gate structure. The thickness of gate oxide was 1000Å. The number of laser shots was 20(ie. 95% overlapping).

10 shots Gate Oxide: 1000A	Mobility* (cm^2/V-s)	Subthreshold swing (V/dec)	Vth (V)	On/Off current ratio at Vds = 3 V
Conventional TFT (W/L = 0.8/0.8μm)	50	0.41	-6.41	1.33E+07
DG-TFT (W/L = 0.8/0.8μm)	338	0.181	-2.308	1.35E+08
Conventional TFT (W/L = 1/1μm)	46	0.411	-6.43	1.33E+07
DG-TFT (W/L =1/1μm)	316	0.197	-2.435	3.02E+08
Conventional TFT (W/L = 1.2/1.2μm)	44	0.513	-6.57	9.20E+06
DG-TFT (W/L = 1.2/1.2μm)	318	0.216	-2.622	5.06E+08
Conventional TFT (W/L = 1.5/1.5μm)	41	0.546	-7.18	9.18E+06
DG-TFT (W/L = 1.5/1.5μm)	244	0.219	-2.877	7.78E+08
Conventional TFT (W/L = 2/2μm)	39	0.691	-7.656	1.91E+07
DG-TFT (W/L = 2/2μm)	206	0.227	-2.723	5.88E+08
Conventional TFT (W/L = 5/5μm)	39	0.486	-8.417	1.01E+07
DG-TFT (W/L = 5/5μm)	77	0.412	-6.038	4.40E+07

Table 2-3 Average of twenty measured electrical characteristics of p-channel SGB-DG-TFTs crystallized with elevated channel method and conventional top gate structure. The thickness of gate oxide was 1000. The number of laser shots was 10(ie. 90% overlapping).

	Mobility* (cm2/V-s)		Vth (V)		SS (V/decade)	
	AVG±STDEV	C.V.	AVG±STDEV	C.V.	AVG±STDEV	C.V.
Con. TFT	89±43.7	17.3%	1.43±1.36	95.1%	0.686±0.124	18.1%
DGTFT	660±45.8	6.9%	-0.5±0.16	32.0%	0.264±0.039	14.8%

Table 2-4 Electrical characteristics of twenty measured n-channel SGB-DG-TFTs crystallized with elevated channel method and conventional top gate TFTs. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping)

	Mobility* (cm2/V-s)		Vth (V)		SS (V/decade)	
	AVG±STDEV	C.V.	AVG±STDEV	C.V.	AVG±STDEV	C.V.
Con. TFT	46±16.1	35%	-6.430±0.97	15.10%	0.411±0.148	36%
DGTFT	316±25.3	8%	-2.435±0.16	6.60%	0.197±0.030	15%

Table 2-5 Electrical characteristics of twenty measured p-channel SGB-DG-TFTs crystallized with elevated channel method and conventional top gate TFTs. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping)

	Mobility* (cm2/V-s)	SS (V/dec)	Vth (V)	Ion/Ioff @ Vds = 3V	DIBL (mV)
TGTFT	197	0.320	-3.89	2.63E+07	452
BGTFT	137	0.286	-4.88	1.44E+07	753
DGTFT	352	0.185	-2.35	4.39E+08	351

Table 3-1 Electrical characteristics of p-channel top/bottom/double gate polycrystalline silicon TFTs crystallized by elevated channel method. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping)

	Gm (μS)	Mobility* (cm^2/V-s)	SS (V/dec)	Vth (V)	Ion/Ioff @ Vds = 3V
DGTFT	2.92	847	0.524	1.006	2.34E+06
DGTFT with LDD	1.25	362	0.536	0.015	2.23E+07

Table 3-2 Electrical characteristics of n-channel double gate polycrystalline silicon TFTs with LDD crystallized by elevated channel method. The thickness of gate oxide was 1000Å. The number of laser shots was 20(ie. 95% overlapping)

	Gm (μS)	SS (V/dec)	Vth (V)	Ion/Ioff @ Vds = 3V
DGTFT	2.92	0.524	1.006	2.34E+06
Shrunk Gate TFT	2.95	0.380	-0.608	3.20E+07

Table 3-3 Electrical characteristics of n-channel double gate polycrystalline silicon TFTs with shrink gate crystallized by elevated channel method. The thickness of gate oxide was 1000Å. The number of laser shots was 20(ie. 95% overlapping)

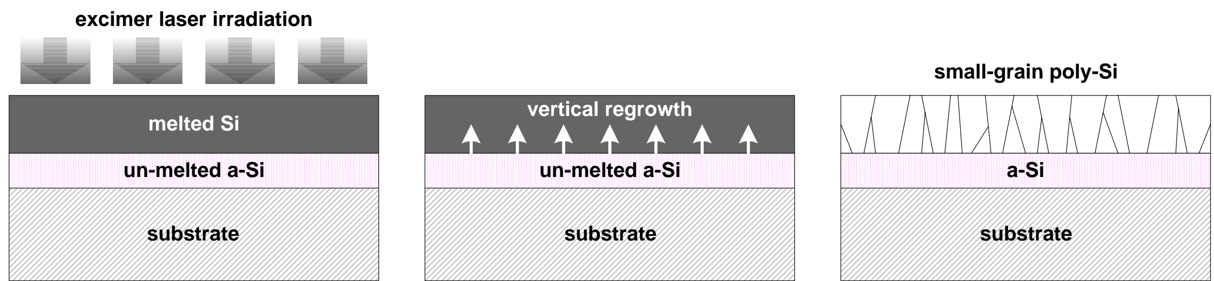


Fig. 2-1 (a) The schematic illustration of the low energy regime corresponding to energy densities that partially melting the a-Si thin film

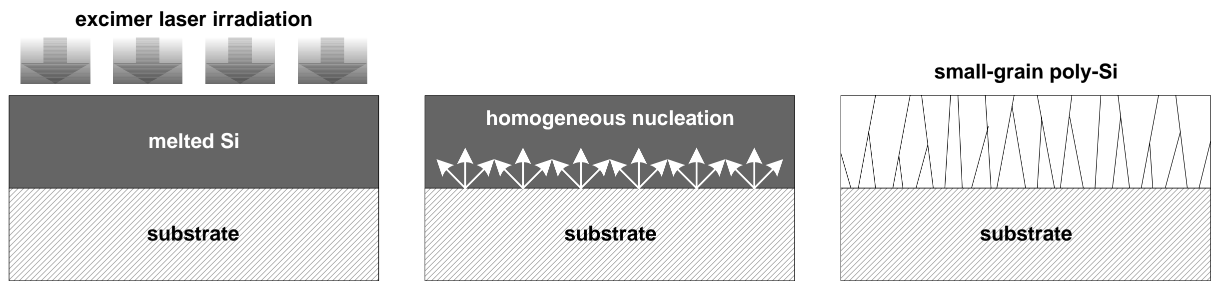


Fig. 2-1 (b) The schematic illustration of the high energy regime corresponding to energy densities that completely melting the a-Si thin film

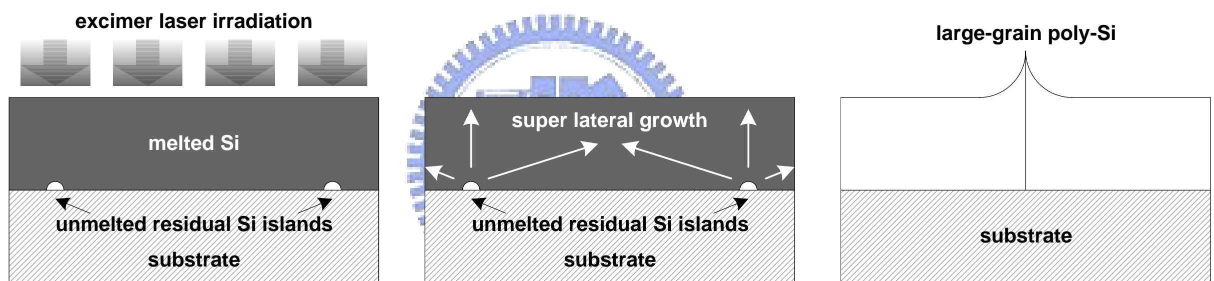


Fig. 2-1 (c) The schematic illustration of the super lateral growth regime corresponding to energy densities that nearly completely melting the a-Si thin film

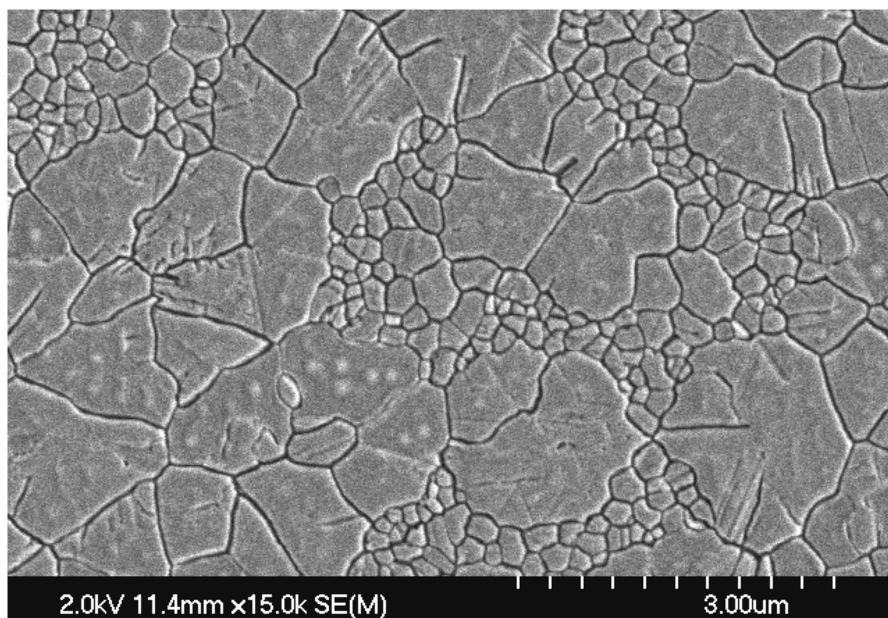
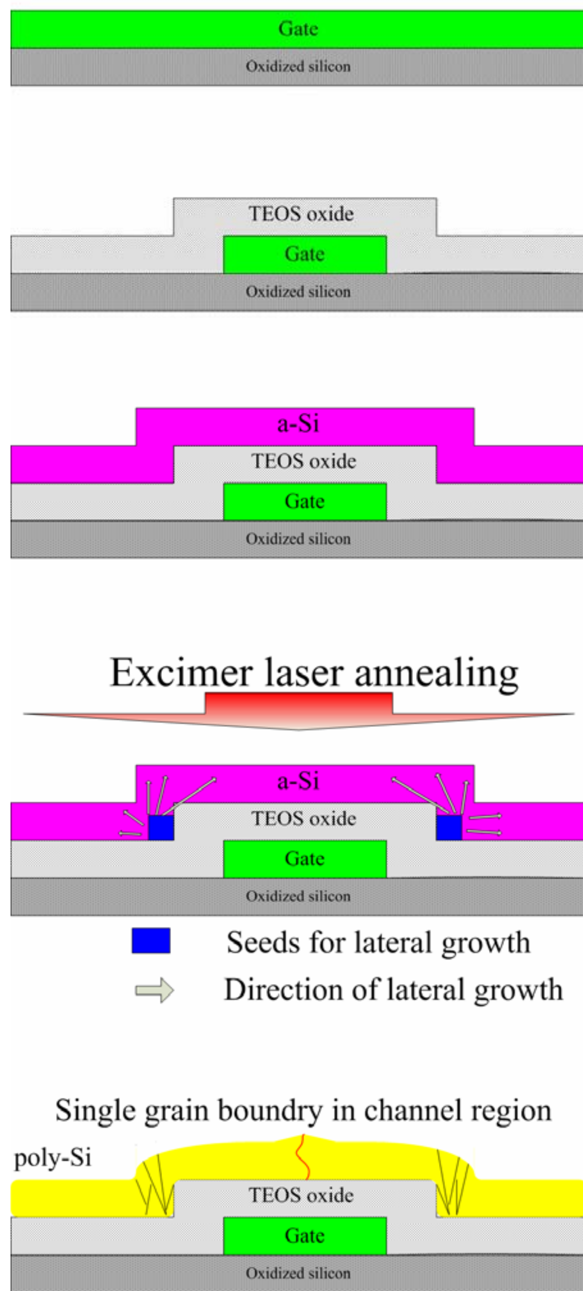


Fig. 2-2 SEM graph of poly-Si by conventional ELA process in SLG regime



1000A in-situ doping phosphorous polycrystalline silicon was deposited by LPCVD at 550℃.

1. Poly gate patterned by TCP-RIE.
2. 500A TEOS oxide was deposited by LPCVD at 700℃.

1000A amorphous silicon was deposited by LPCVD at 550℃.

The a-Si thin film was subjected to excimer laser irradiation at room temperature and the number of laser shots was 20 shots.

After excimer laser irradiation the single grain boundary polycrystalline silicon thin film was formed.

Fig. 2-3 Process flow of preparing samples for material characteristics by elevated channel method

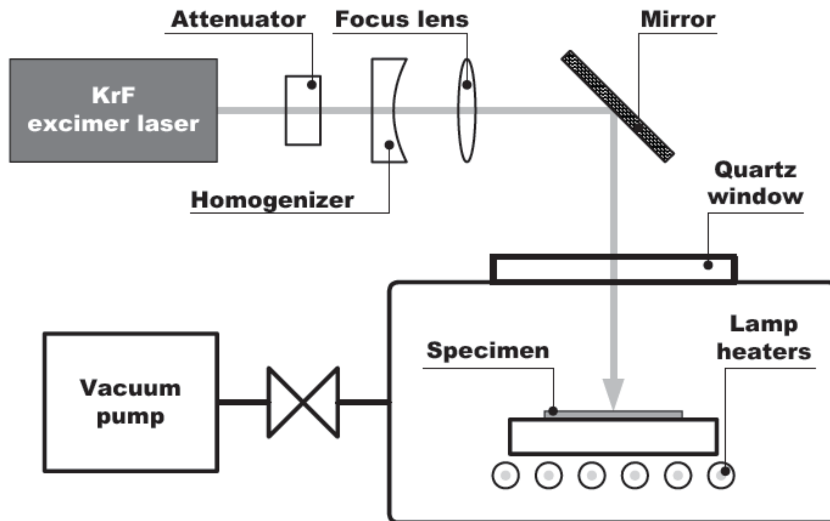
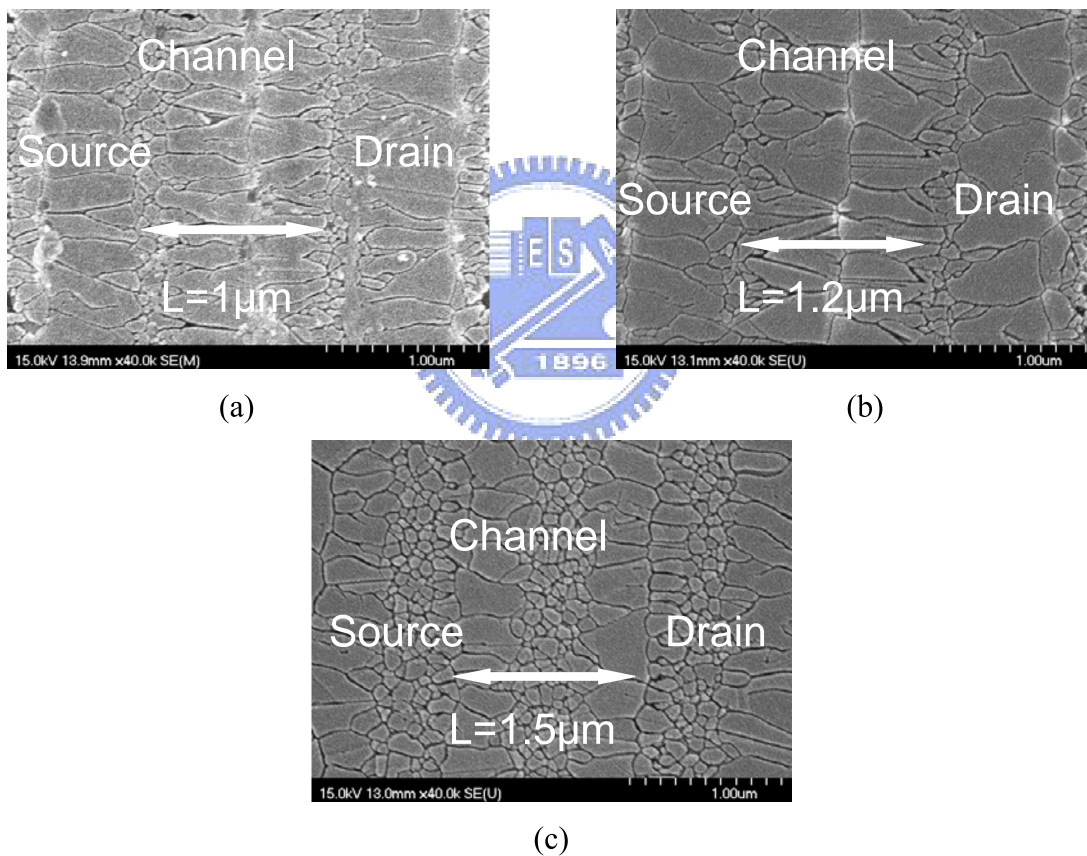


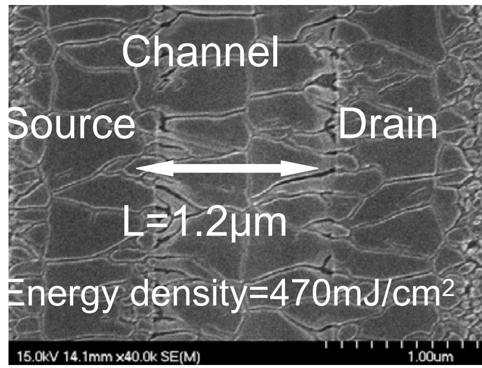
Fig. 2-4 The schematic illustration of the excimer laser system.



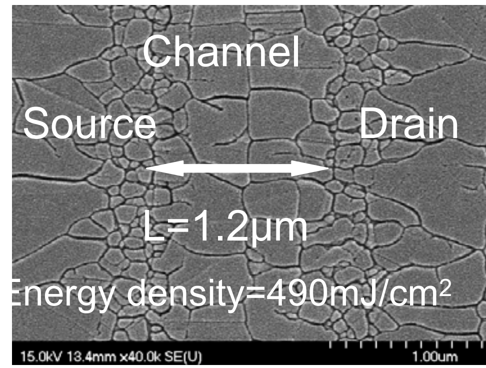
Channel
Source
Drain
L=1.5μm
15.0kV 13.0mm x40.0k SE(U)
1.00um

(c)

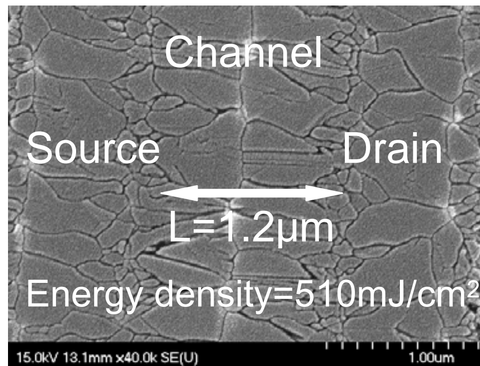
Fig. 2-5 SEM graphs of excimer laser crystallized polycrystalline silicon by elevated channel method. The channel length was varied from 1μm to 1.5 μm. The bottom poly gate thickness was 1000Å and the gate oxide thickness was 500Å. The laser energy density was 510 mJ/cm^2



(a)

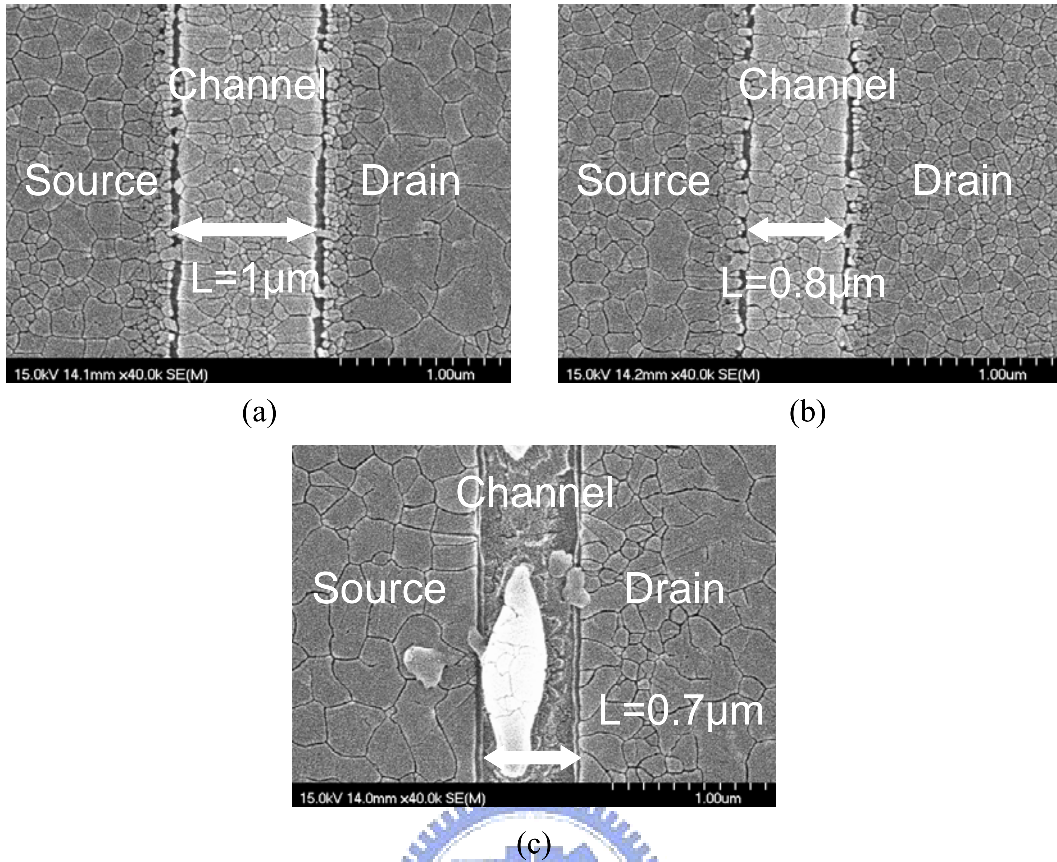


(b)



(c)

Fig. 2-6 SEM graphs of excimer laser crystallized polycrystalline silicon by elevated channel method. The channel length was 1.2 μm. The poly gate thickness was 1000Å and the gate oxide thickness was 500Å. The laser energy density was (a) 470 (b) 490 (c) 510 mJ/cm^2.



(a) (b)

(c)

Fig. 2-7 SEM graphs of excimer laser crystallized polycrystalline silicon by elevated channel method. The channel length was (a)1 (b)0.8 (c)0.7 μm. The poly gate thickness was 1000Å and the gate oxide thickness was 500Å. The laser energy density was 310 mJ/cm^2.

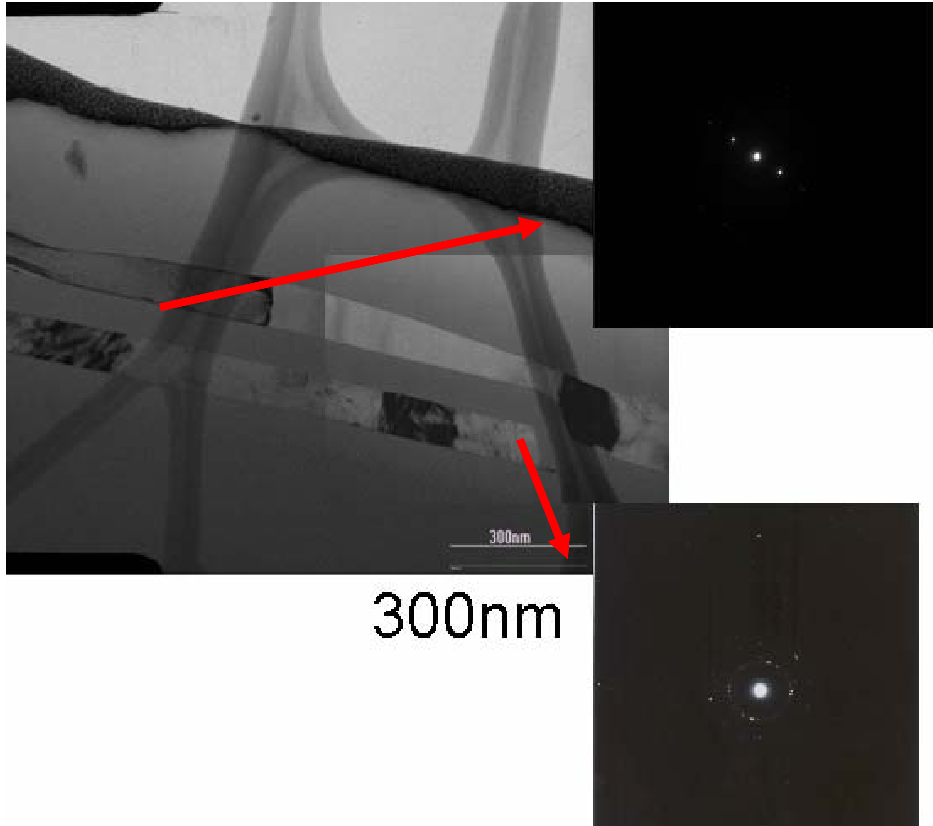


Fig. 2-8 Cross-section TEM graphs of excimer laser crystallized polycrystalline silicon by elevated channel method.

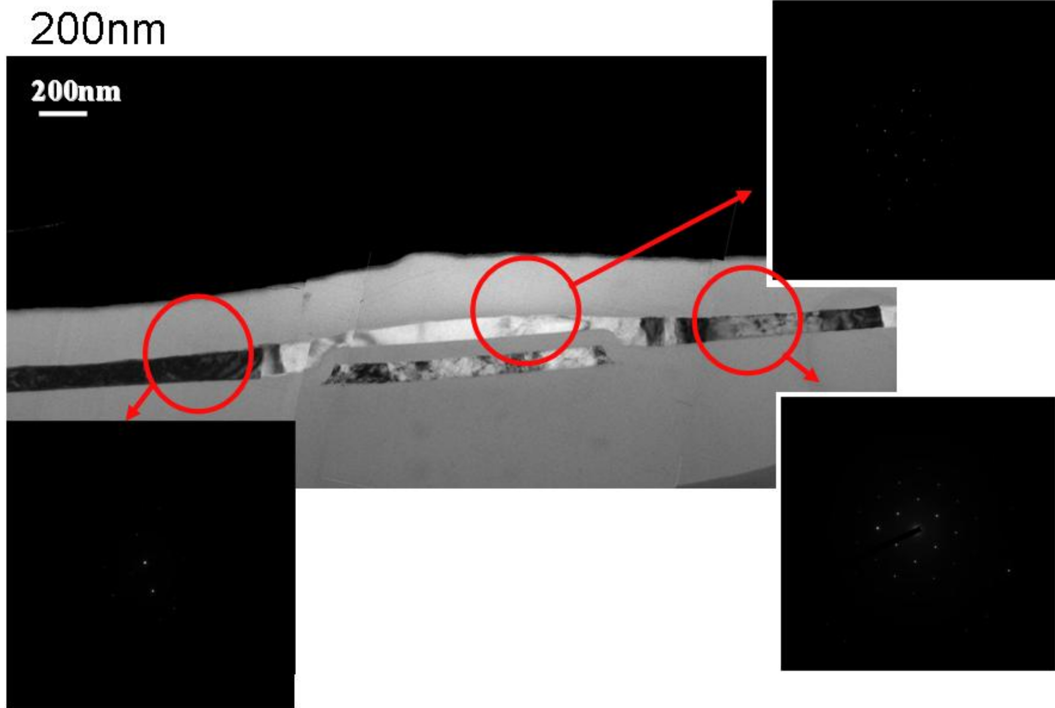
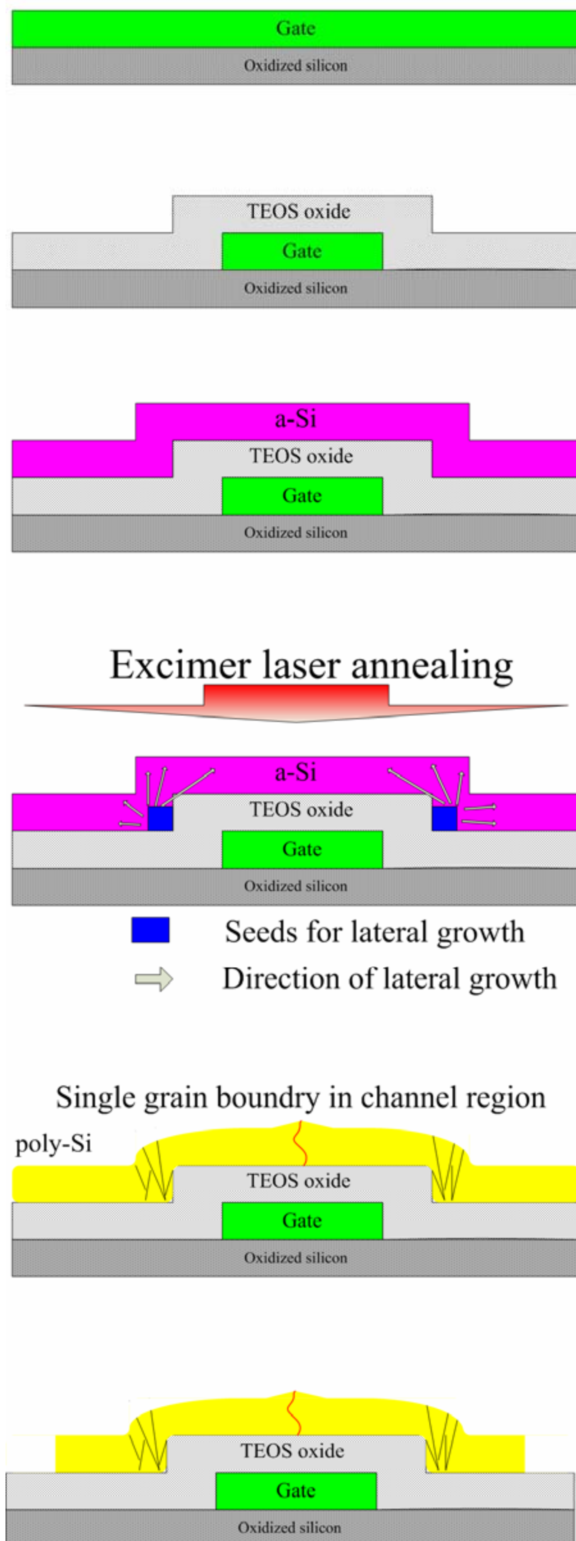


Fig. 2-9 Cross-section TEM graphs of excimer laser crystallized polycrystalline silicon by elevated channel method.



1000A in-situ doping phosphorous polycrystalline silicon was deposited by LPCVD at 550℃.

1. Poly gate patterned by TCP-RIE.
2. 1000A TEOS oxide was deposited by LPCVD at 700℃.

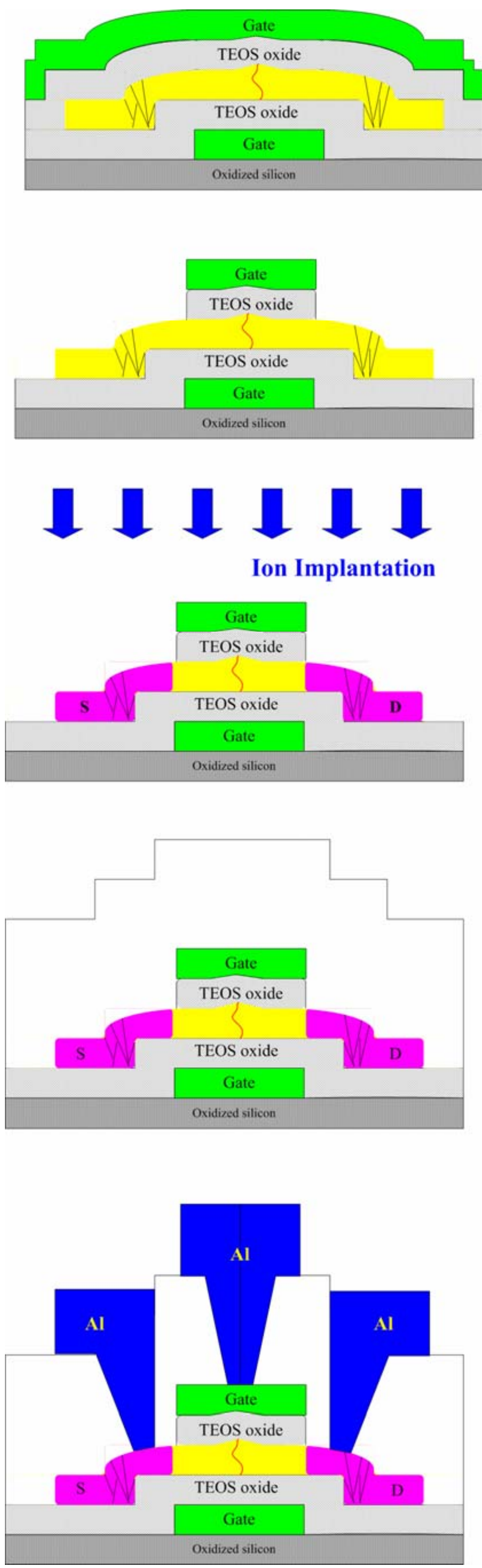
1000A amorphous silicon was deposited by LPCVD at 550℃.

The a-Si thin film was subjected to excimer laser irradiation at room temperature and the number of laser shots was 10/20 shots.

After excimer laser irradiation the single grain boundary polycrystalline silicon thin film was formed.

Active region define by TCP-RIE.

Fig. 2-10 Process flow for fabrication of SGB-DG-TFTs (I)



1. 1000A TEOS oxide was deposited by LPCVD at 700°C.
2. 1000A in-situ doping phosphorous polycrystalline silicon was deposited by LPCVD at 550°C.

1. Gate electrode define by TCP-RIE.
2. Gate oxide define by DBOE.
3. Top gate and bottom gate contact hole etching.

Ion implantation with dose of 5E15cm^{-2} was carried out to form source and drain regions.
(Phosphorous: 40keV / BF2: 70keV)

5500A TEOS oxide was deposited by LPCVD at 700°C followed by thermal annealing for 9 hours to activate the dopants.

Contact hole formation by RIE and metallization was carried out by PVD and dry etching.
Finally Al sintering at 400°C was carried out.

Fig. 2-10 Process flow for fabrication of SGB-DG-TFTs (II)

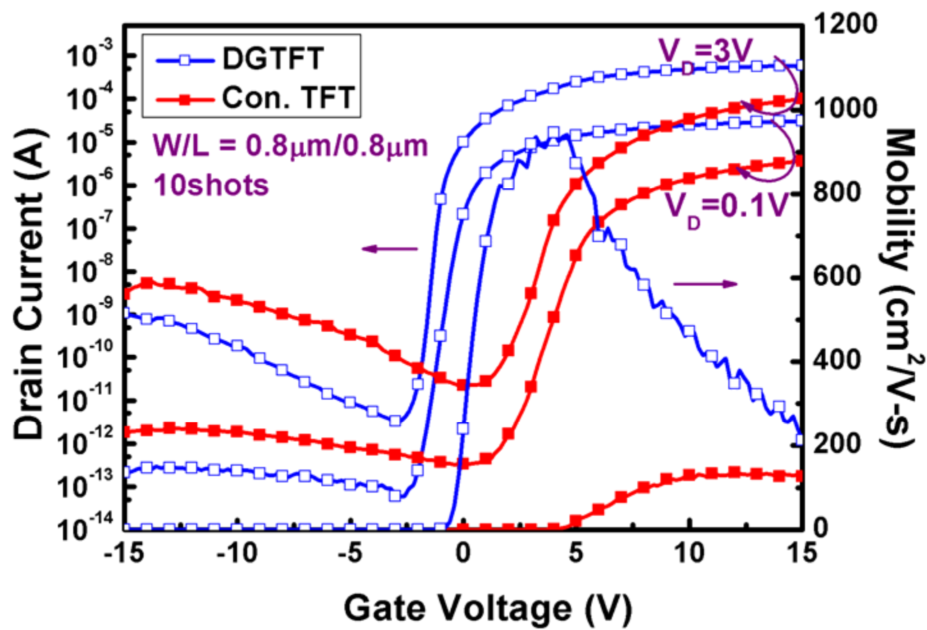


Fig. 2-11 Transfer characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 0.8 μm, in which the thickness of gate oxide was 1000 Å. The number of laser shots was 10 (ie. 90% overlapping).

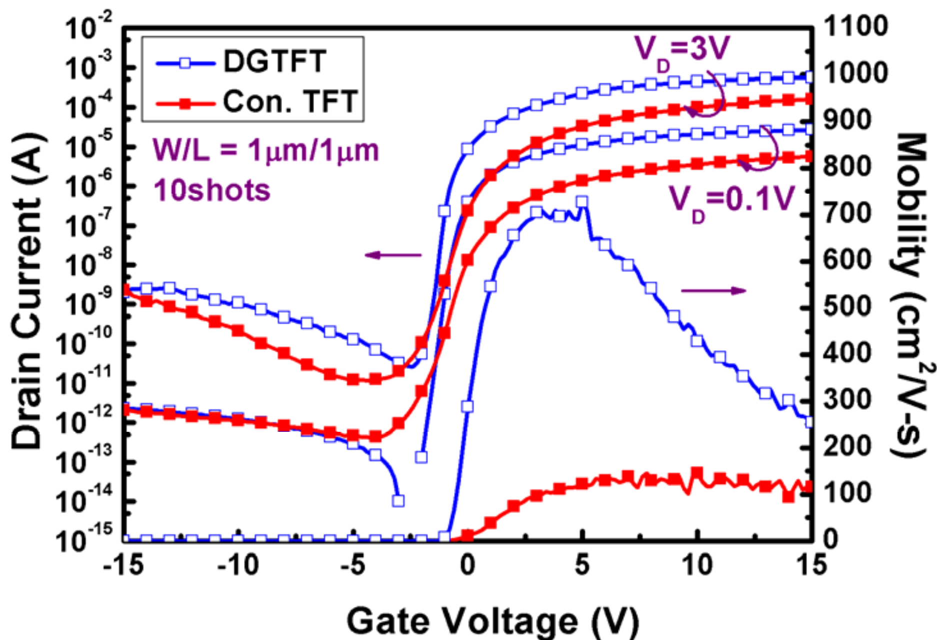


Fig. 2-12 Transfer characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

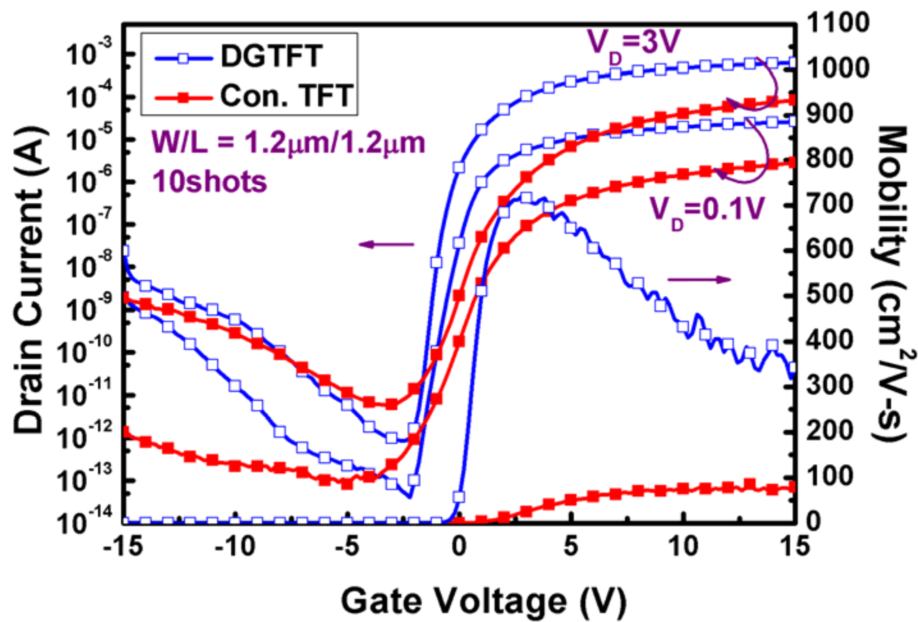


Fig. 2-13 Transfer characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1.2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

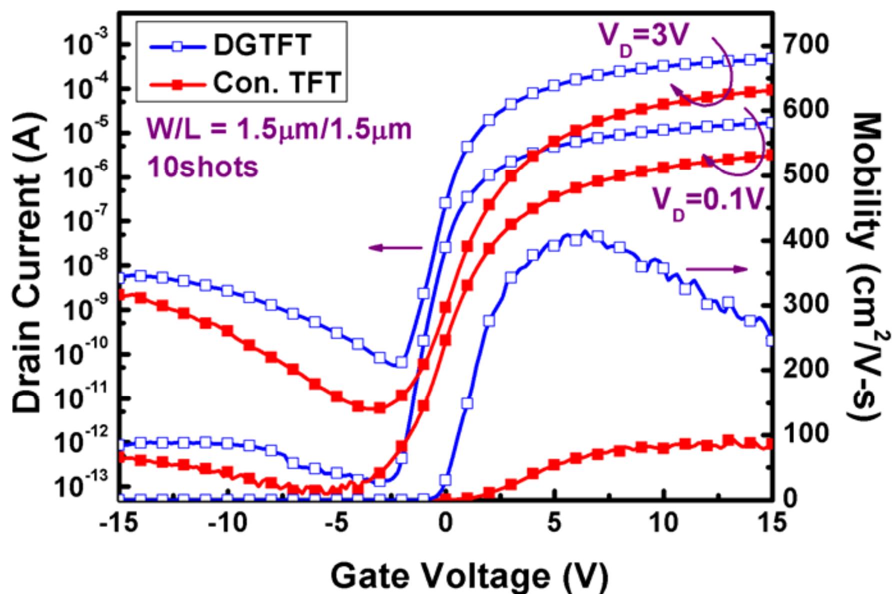


Fig. 2-14 Transfer characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1.5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

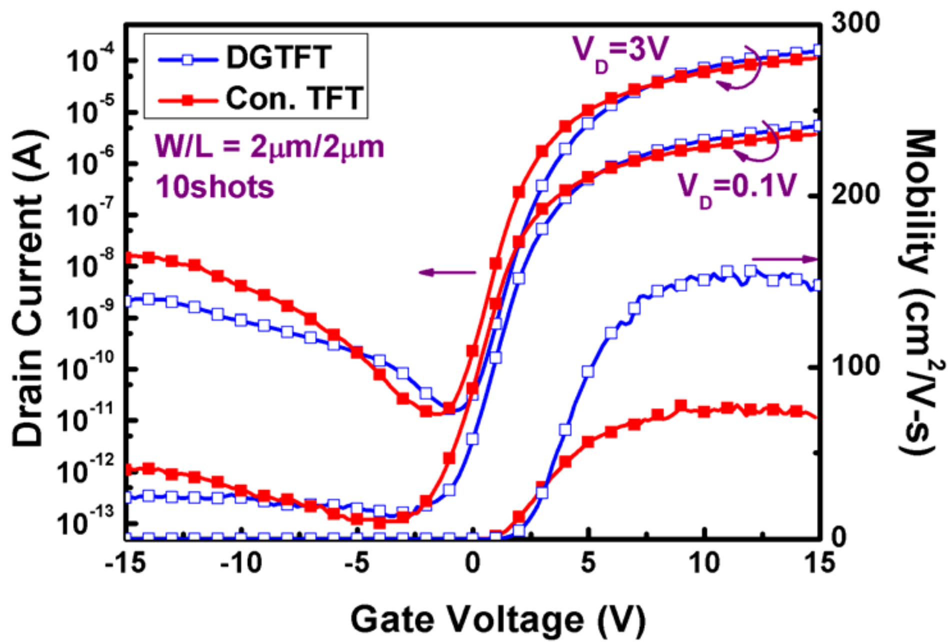


Fig. 2-15 Transfer characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

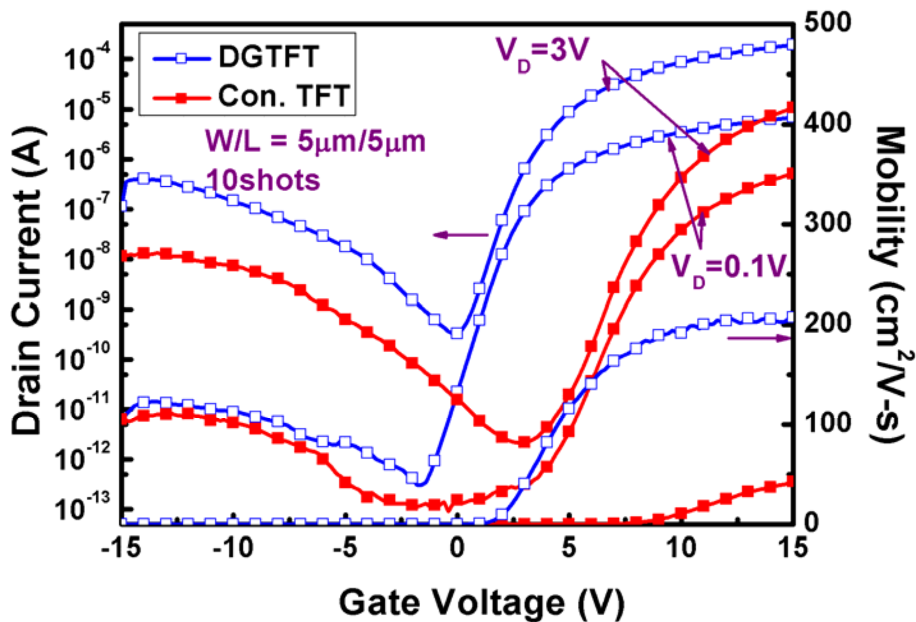


Fig. 2-16 Transfer characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

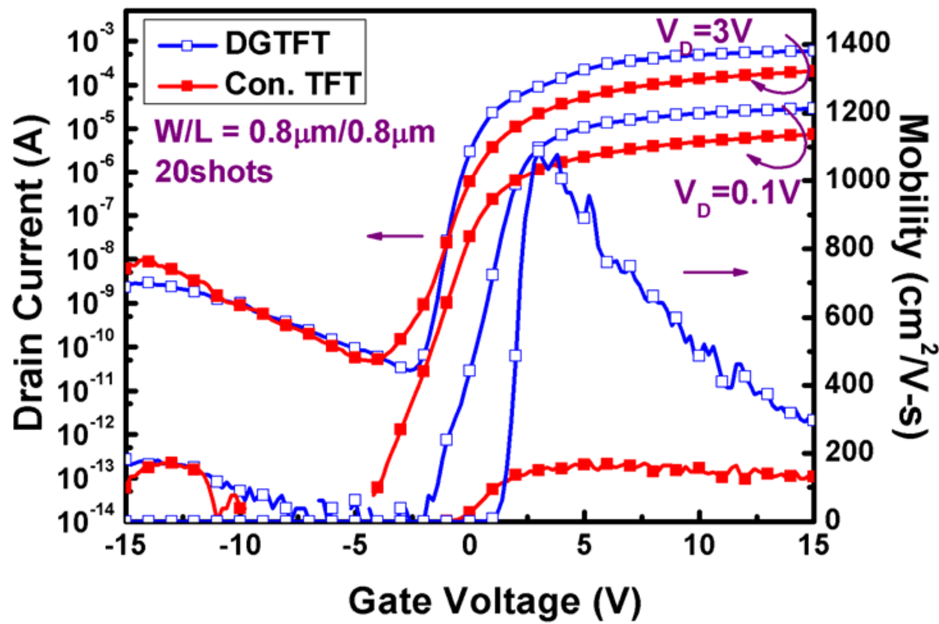


Fig. 2-17 Transfer characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 0.8 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping).

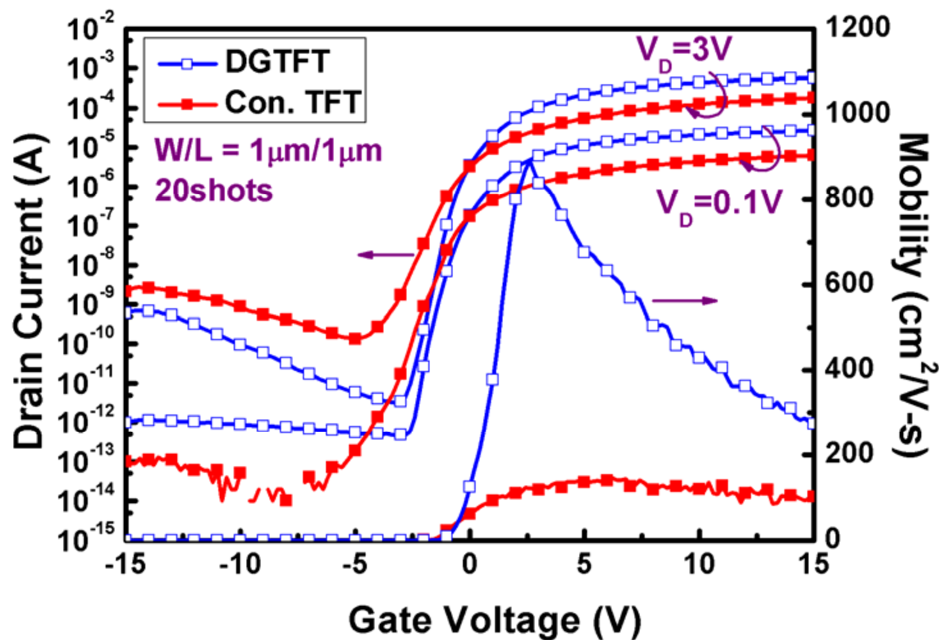


Fig. 2-18 Transfer characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping).

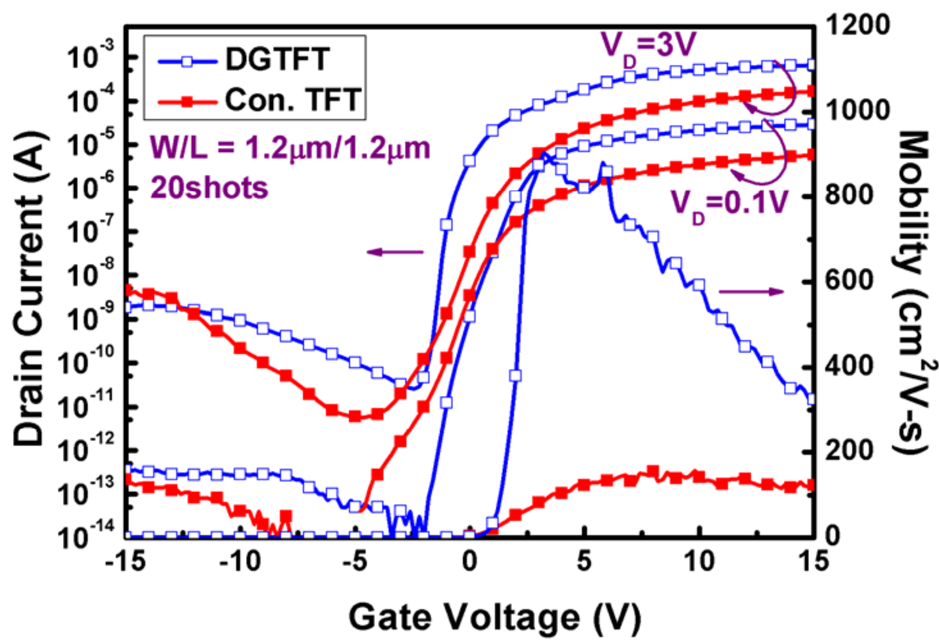


Fig. 2-19 Transfer characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1.2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping).

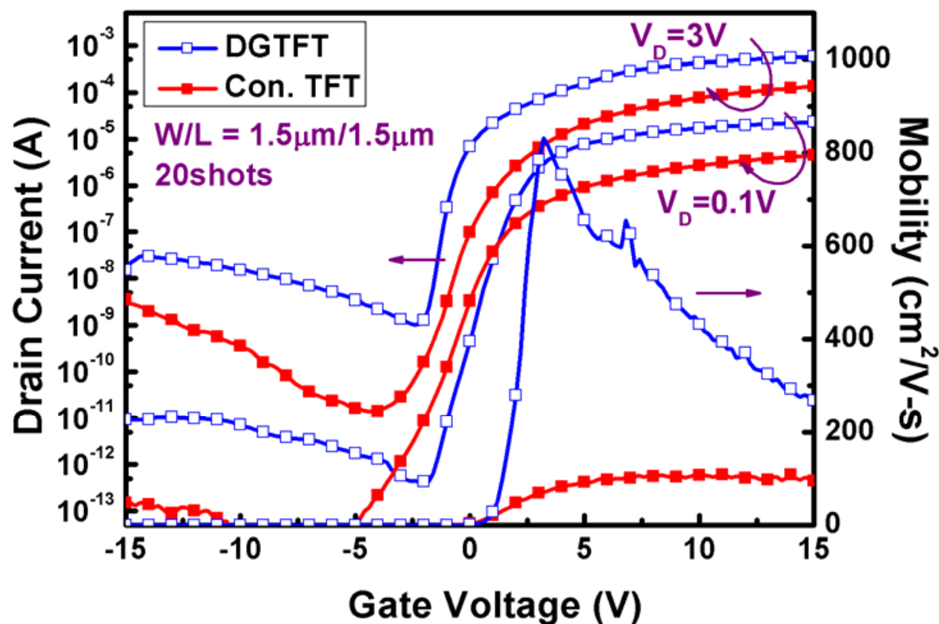


Fig. 2-20 Transfer characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1.5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping).

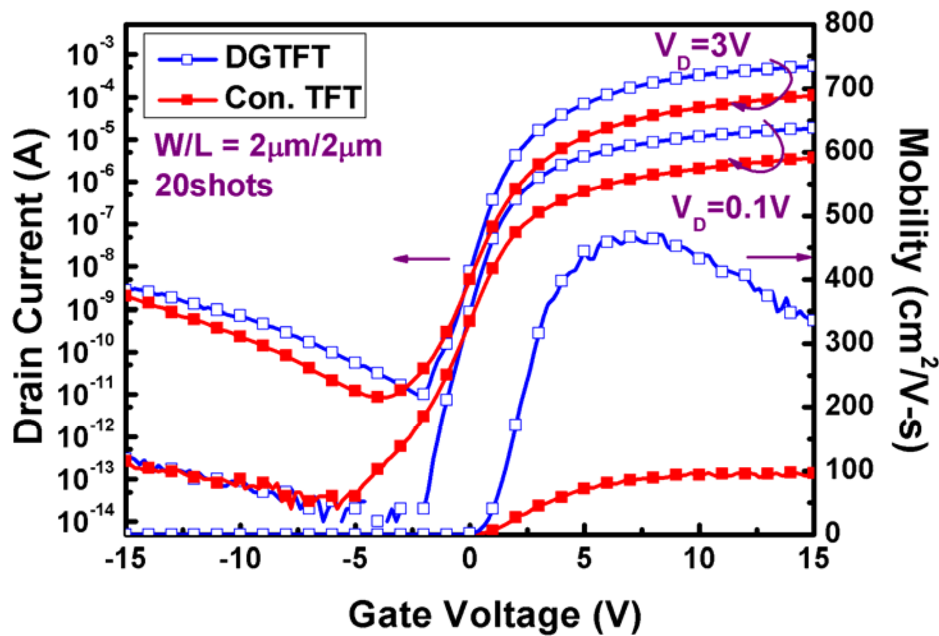


Fig. 2-21 Transfer characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping).

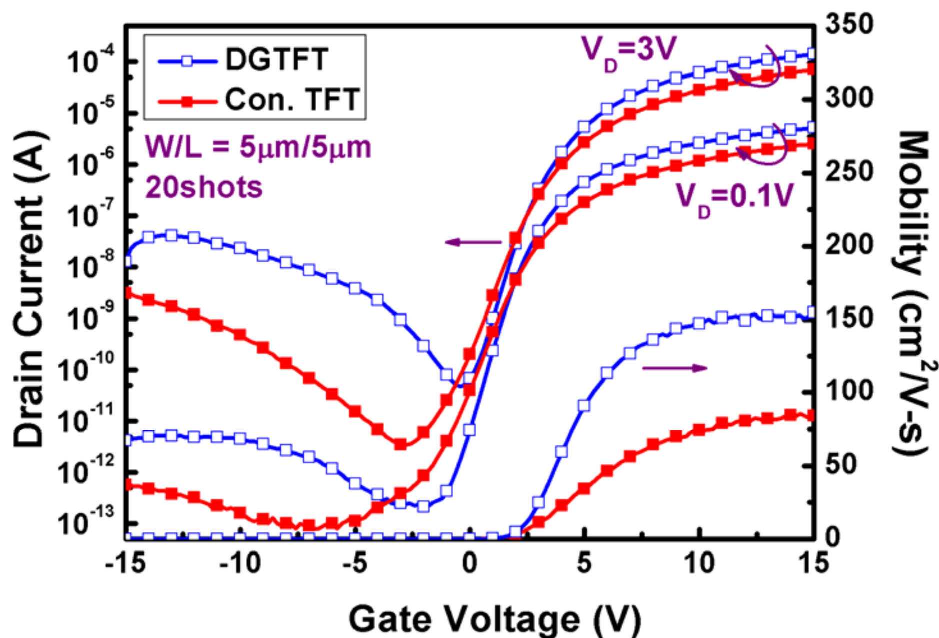


Fig. 2-22 Transfer characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping).

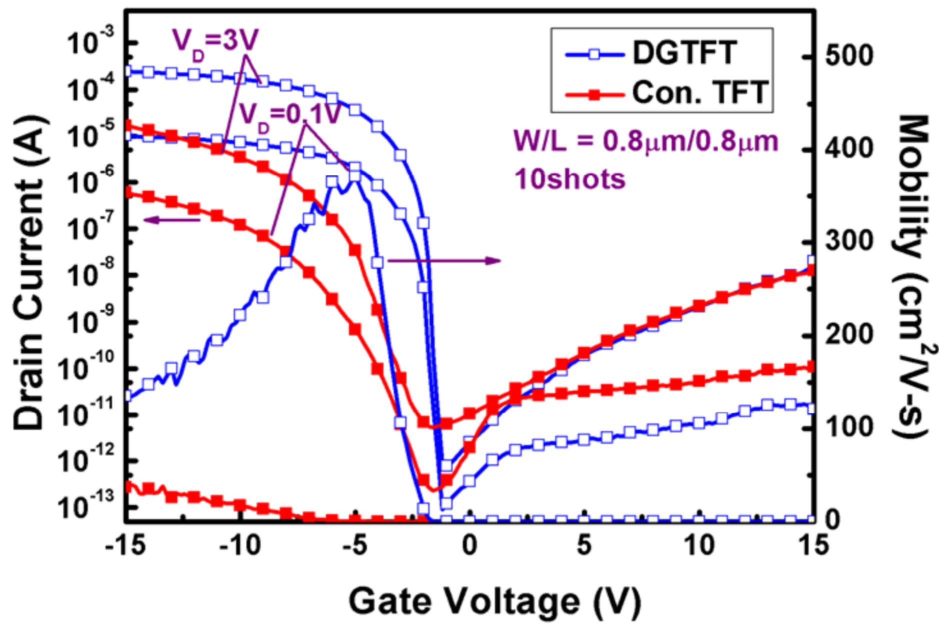


Fig. 2-23 Transfer characteristic of p-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 0.8 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

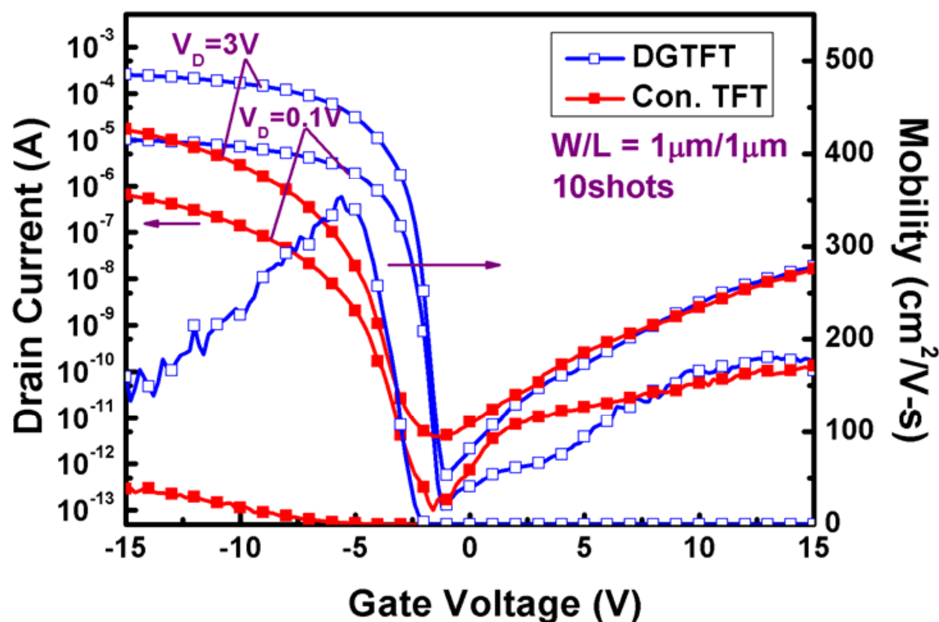


Fig. 2-24 Transfer characteristic of p-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

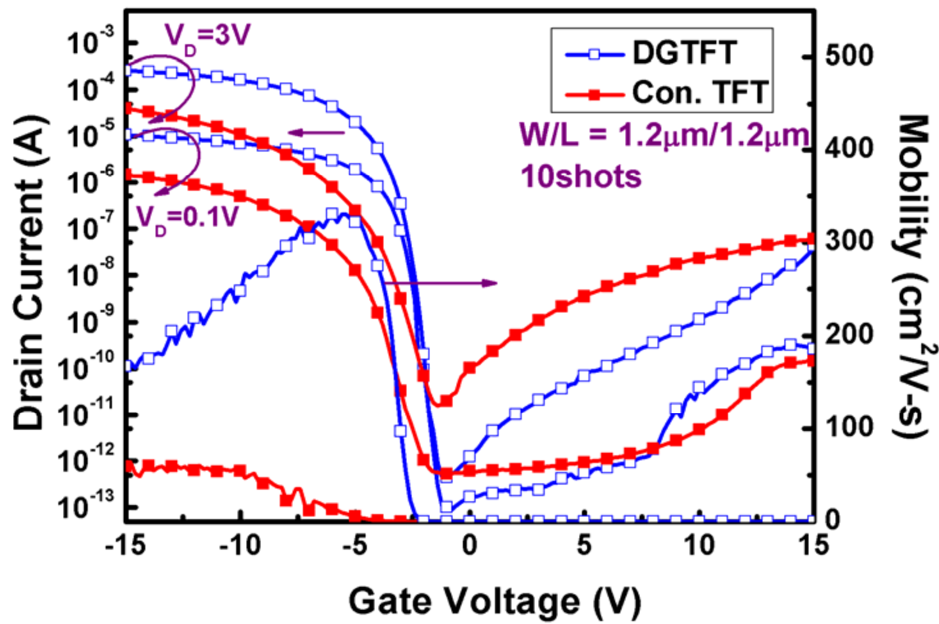


Fig. 2-25 Transfer characteristic of p-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1.2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

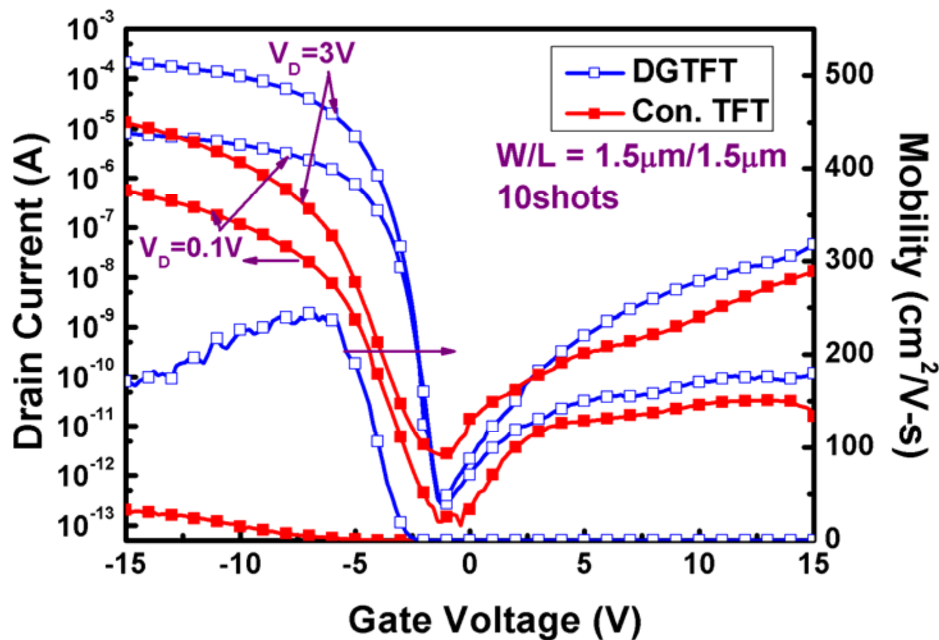


Fig. 2-26 Transfer characteristic of p-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1.5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

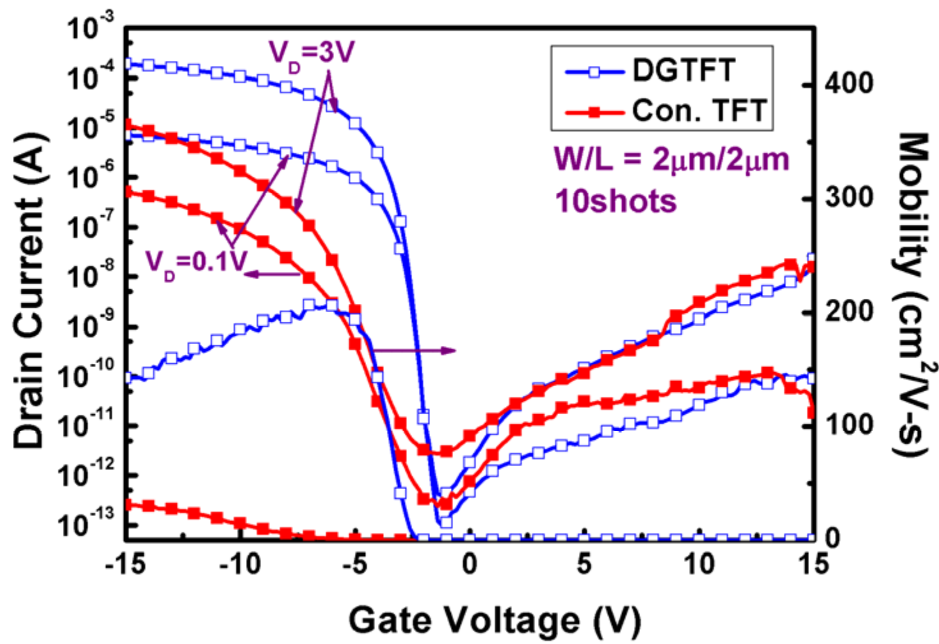


Fig. 2-27 Transfer characteristic of p-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

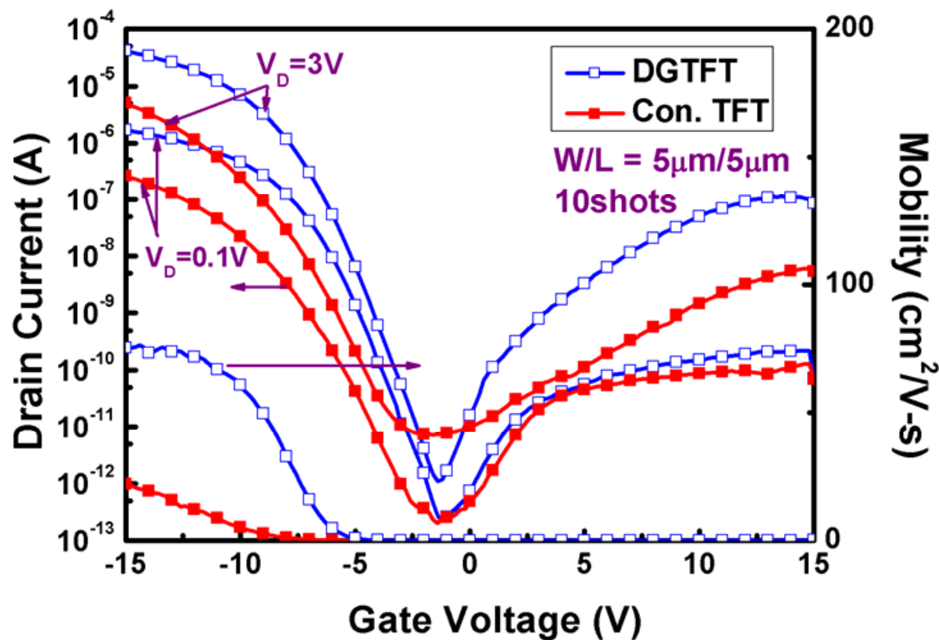


Fig. 2-28 Transfer characteristic of p-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

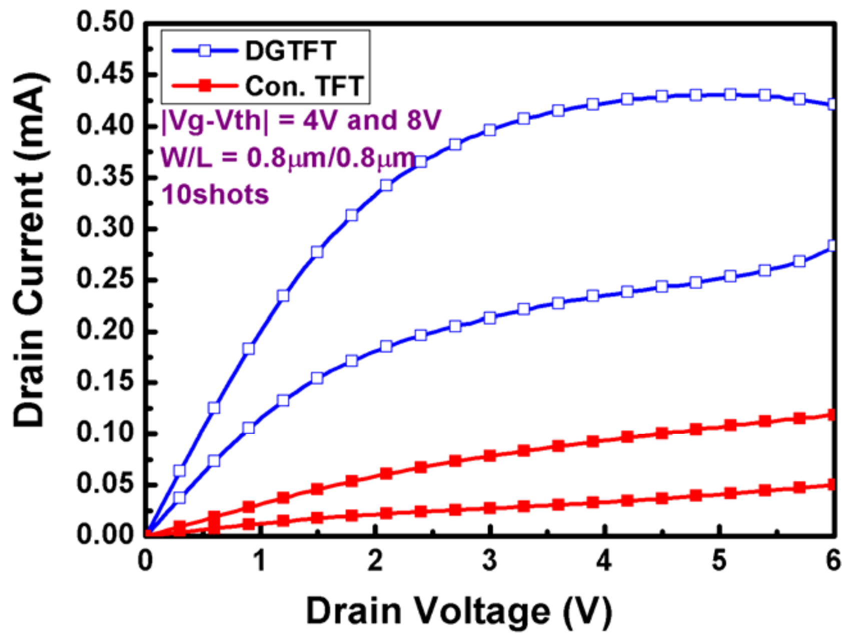


Fig. 2-29 Output characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 0.8 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

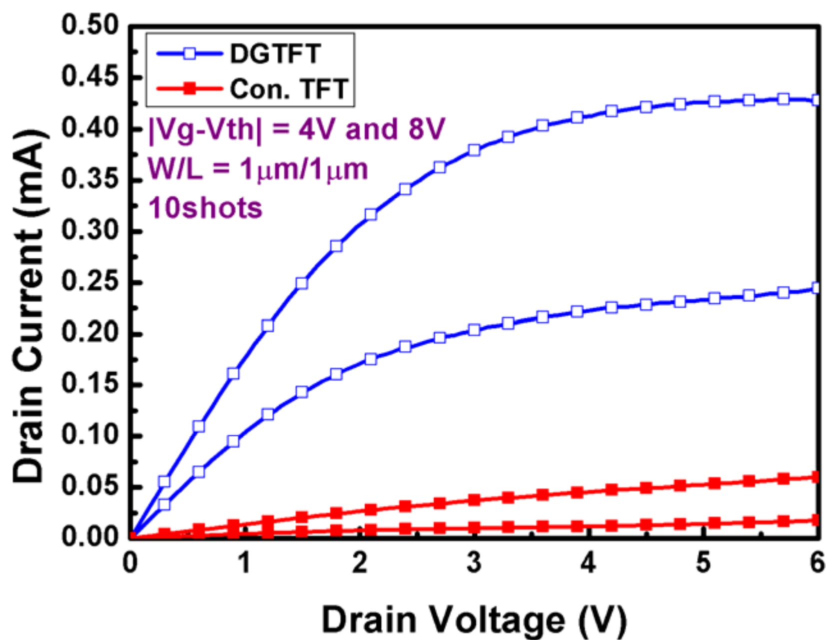


Fig. 2-30 Output characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

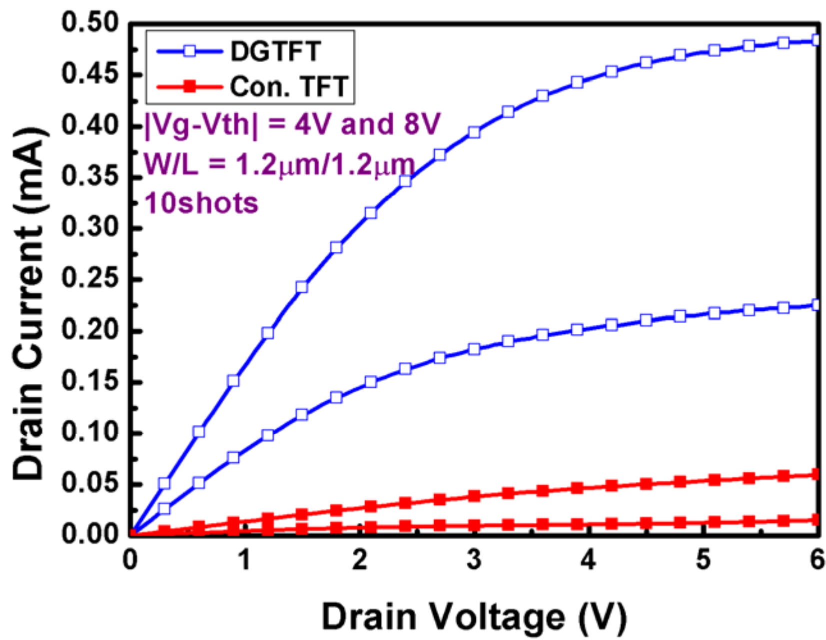


Fig. 2-31 Output characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1.2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

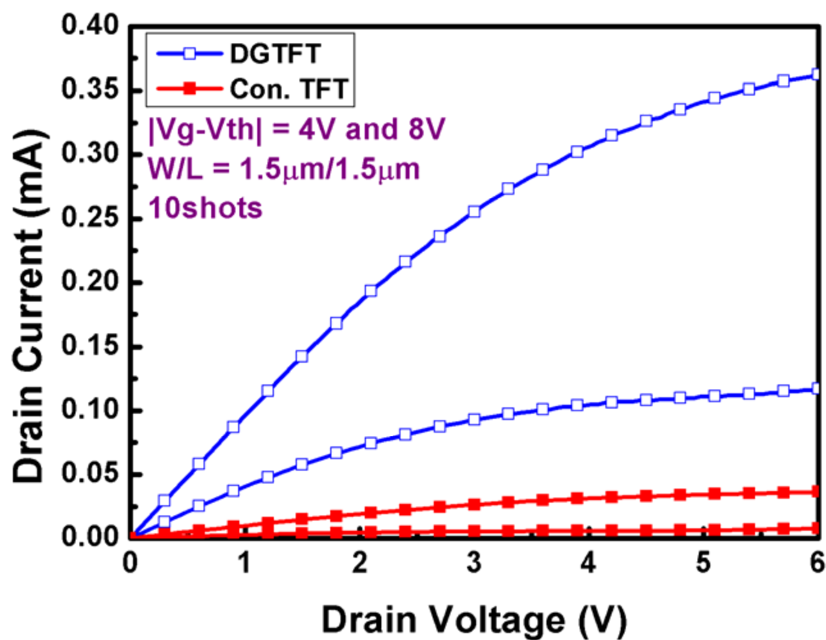


Fig. 2-32 Output characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1.5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

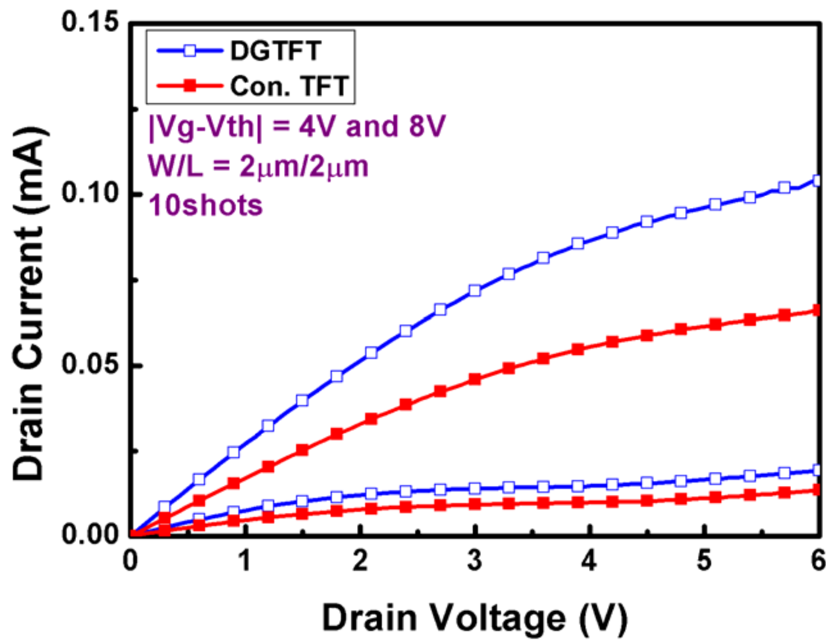


Fig. 2-33 Output characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

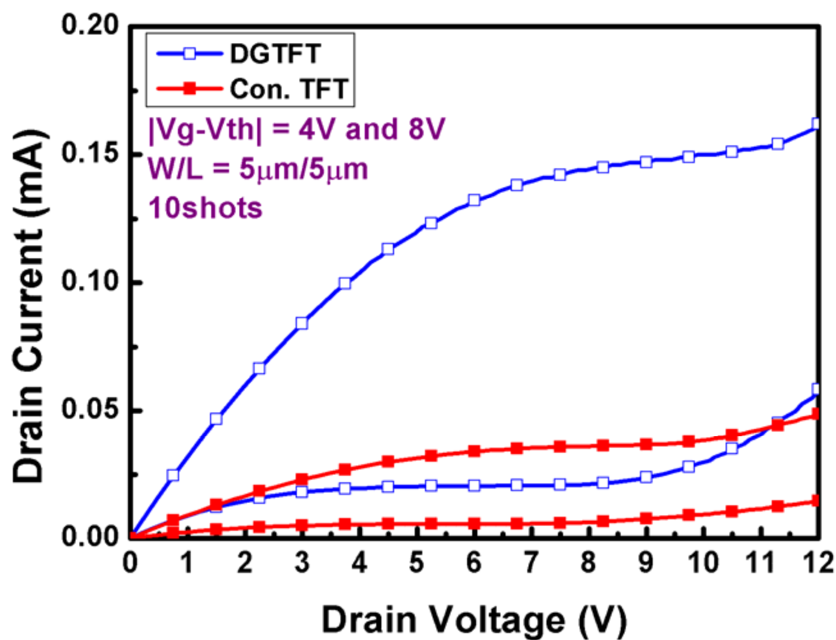


Fig. 2-34 Output characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

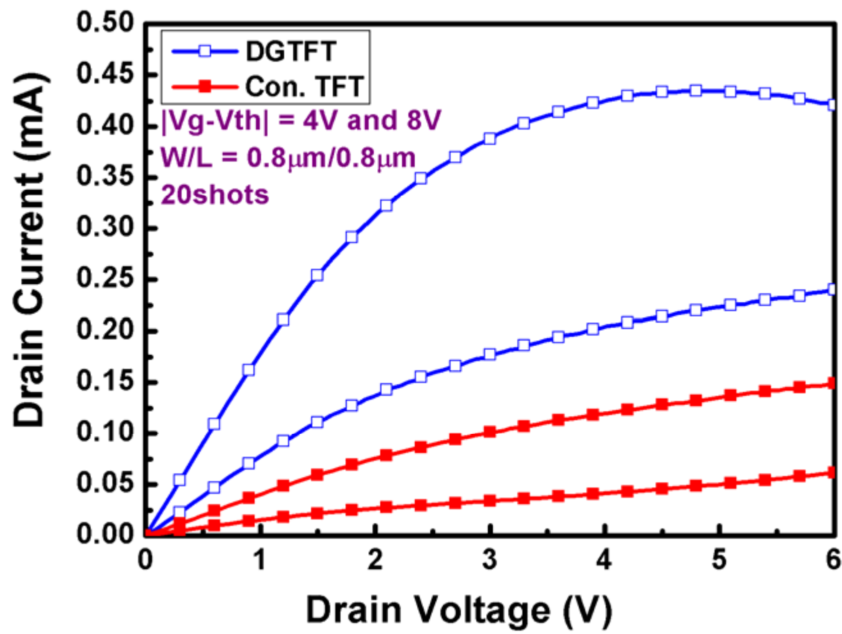


Fig. 2-35 Output characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 0.8 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping).

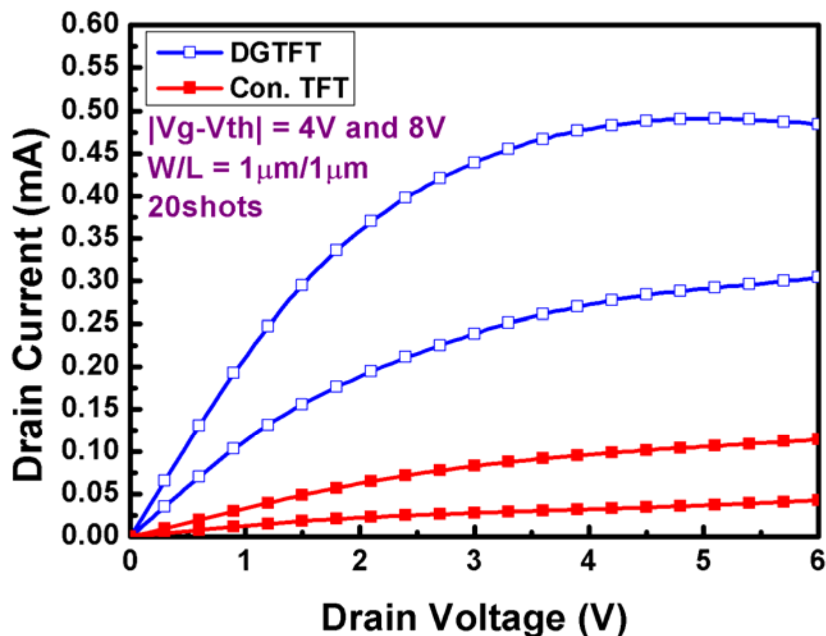


Fig. 2-36 Output characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping).

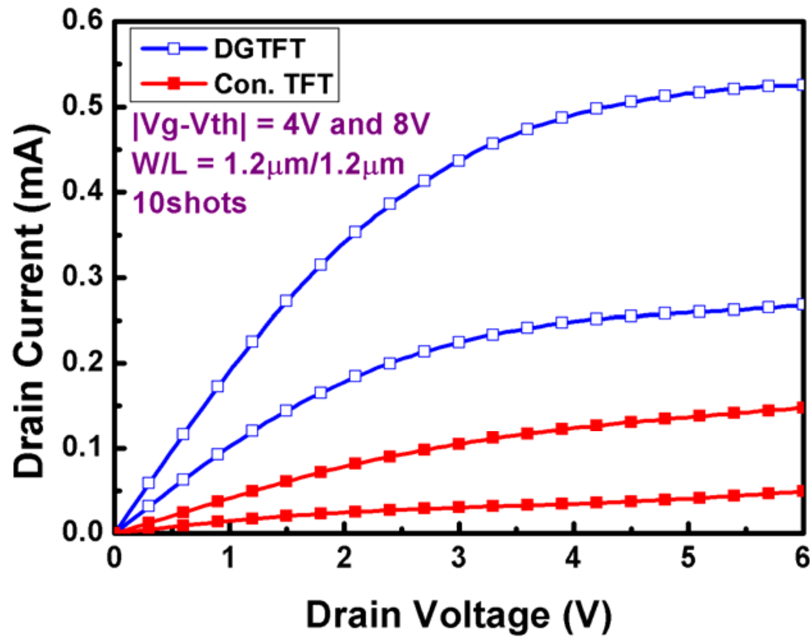


Fig. 2-37 Output characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1.2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping).

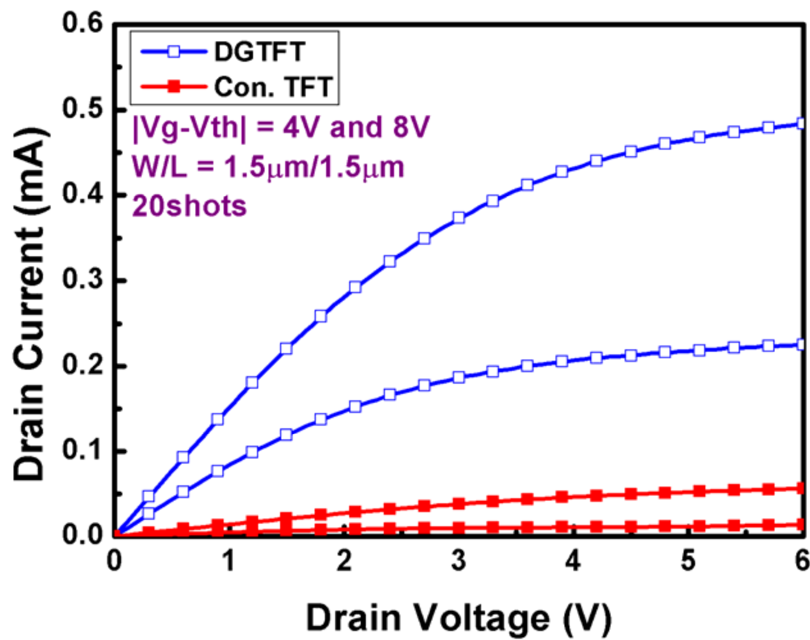


Fig. 2-38 Output characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1.5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping).

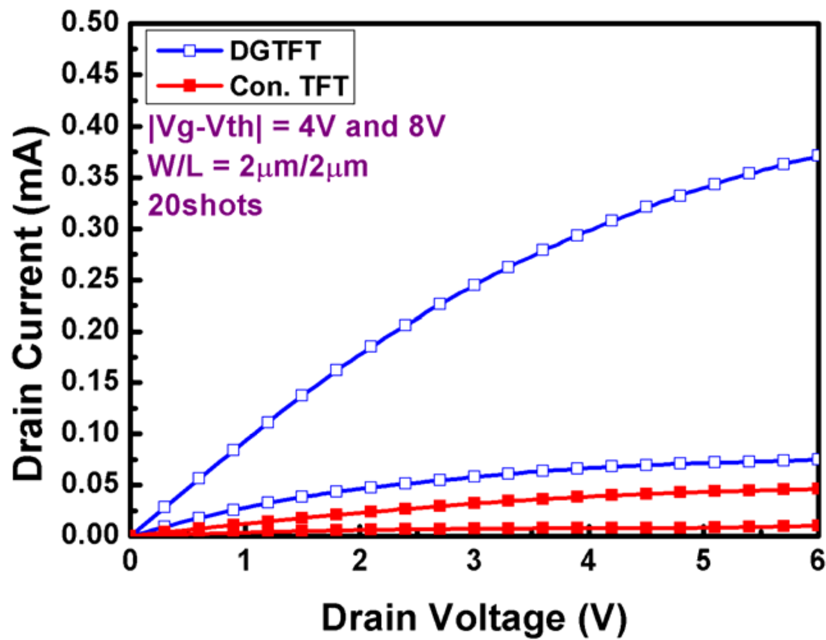


Fig. 2-39 Output characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping).

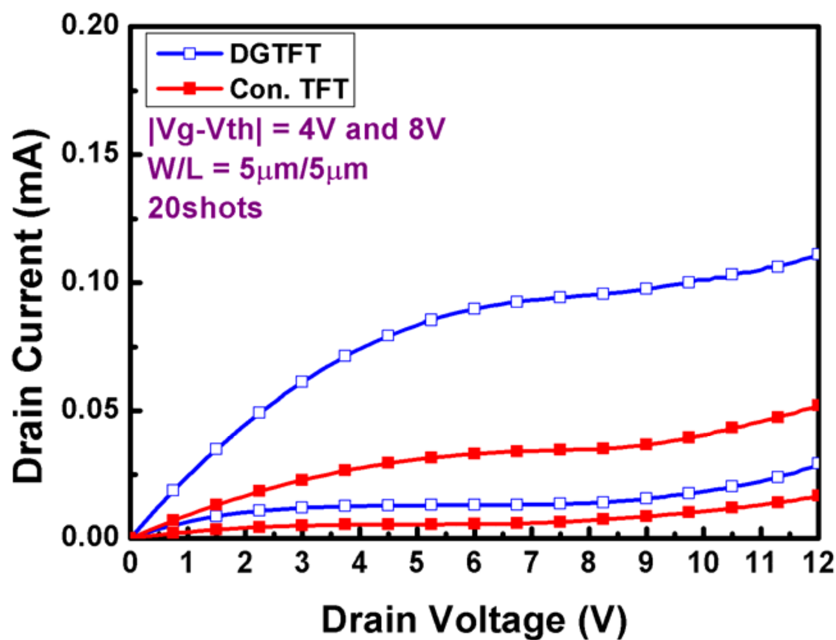


Fig. 2-40 Output characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping).

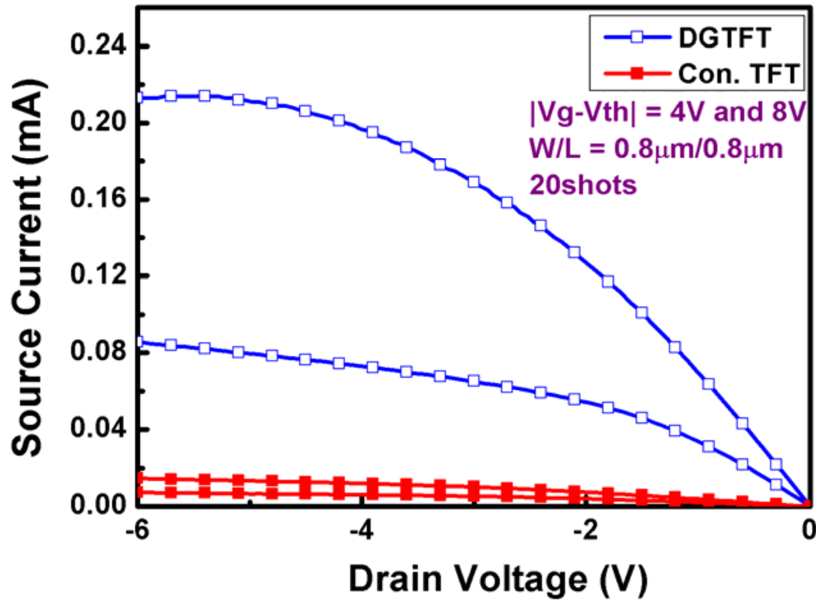


Fig. 2-41 Output characteristic of p-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 0.8 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

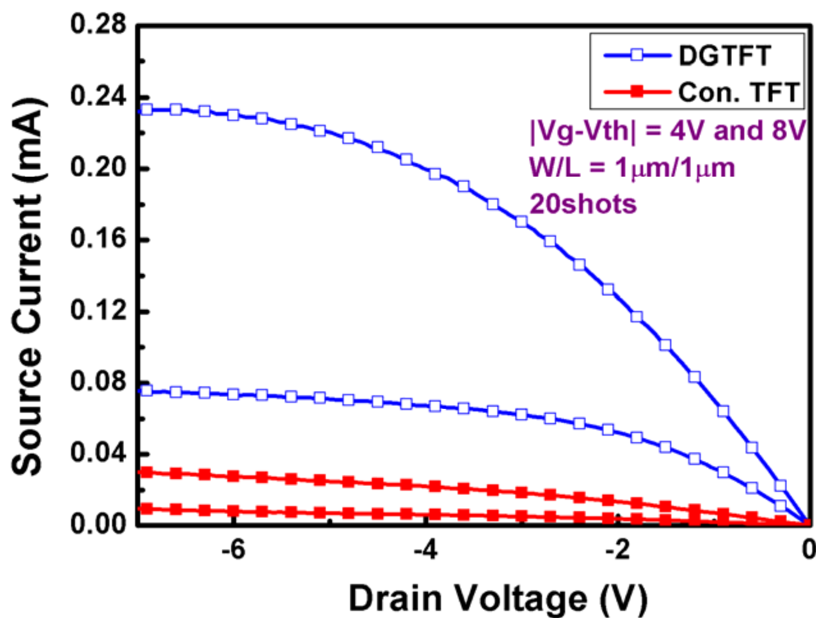


Fig. 2-42 Output characteristic of p-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

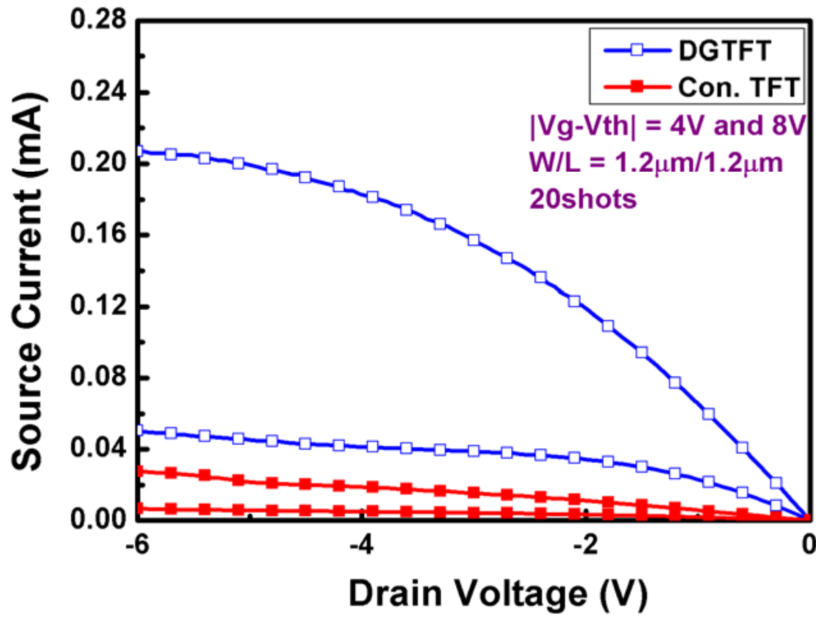


Fig. 2-43 Output characteristic of p-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1.2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

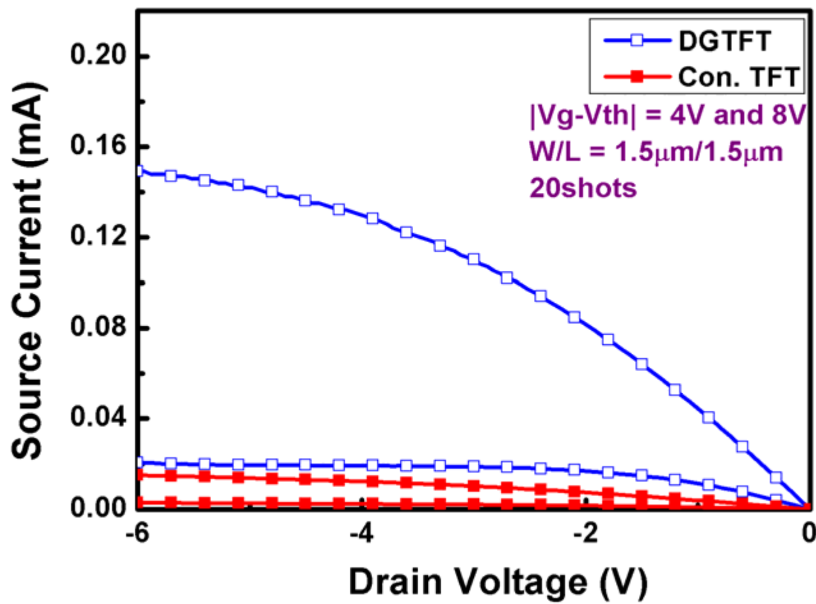


Fig. 2-44 Output characteristic of p-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1.5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

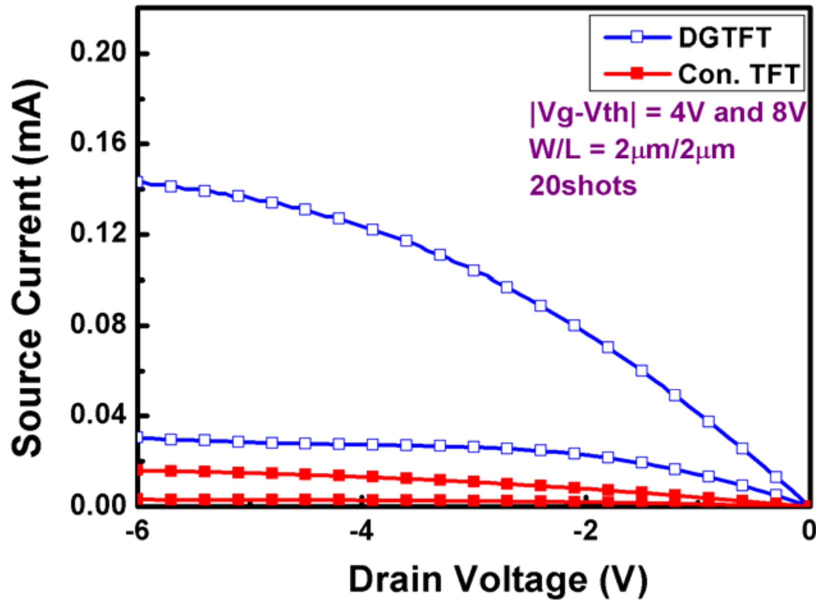


Fig. 2-45 Output characteristic of p-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

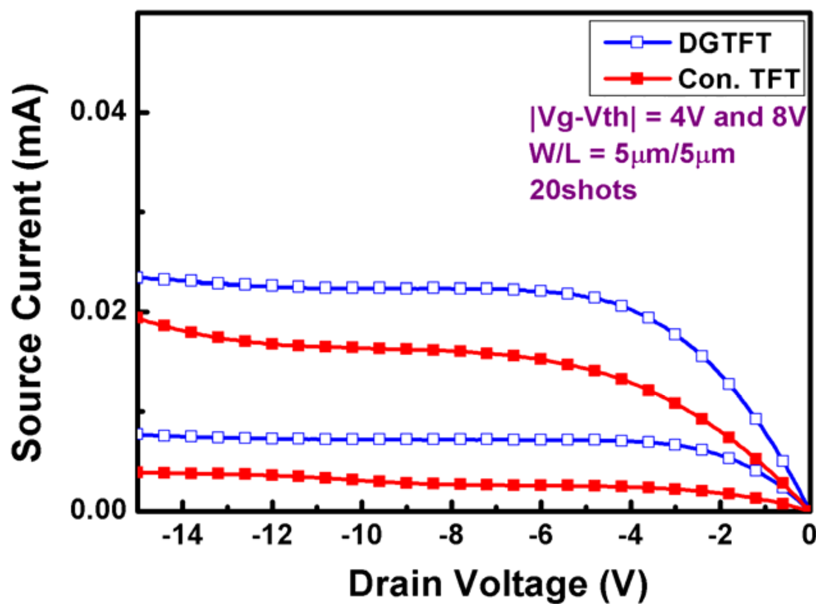


Fig. 2-46 Output characteristic of p-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

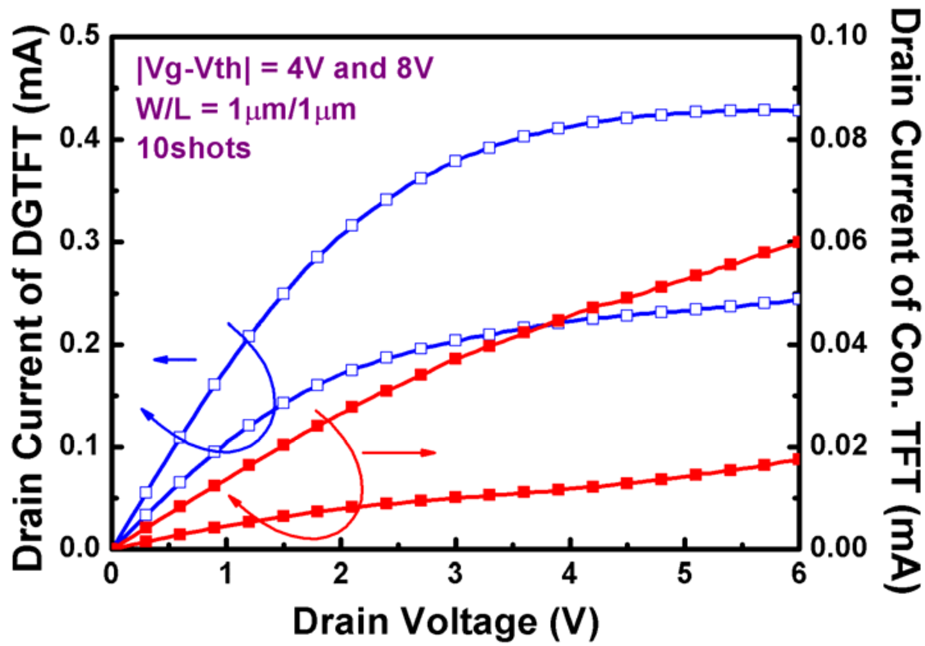


Fig. 2-47 Alleviated kink effect by n-channel SGB-DG-TFTs rather than conventional TFTs. The channel length was 0.8 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping).

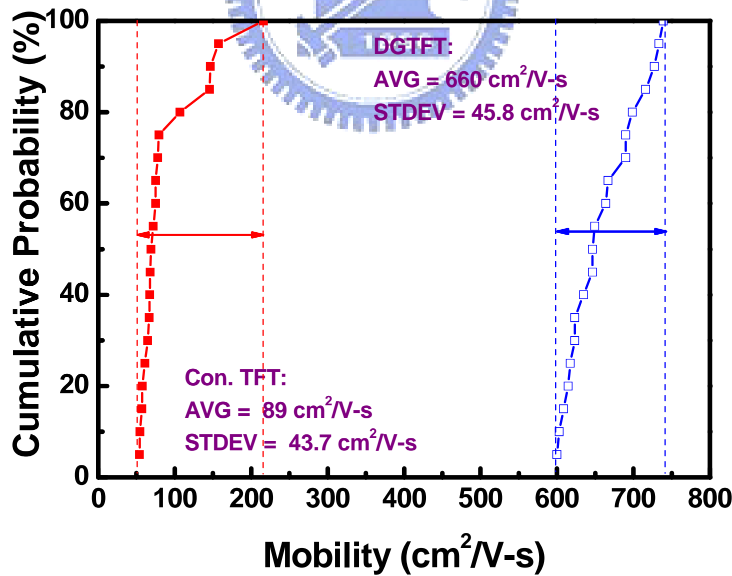


Fig. 2-48 Statistics and uniformity of equivalent field effect mobility. Twenty n-channel SGB-DG-TFTs crystallized with elevated channel method and conventional top gate TFTs were measured. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping)

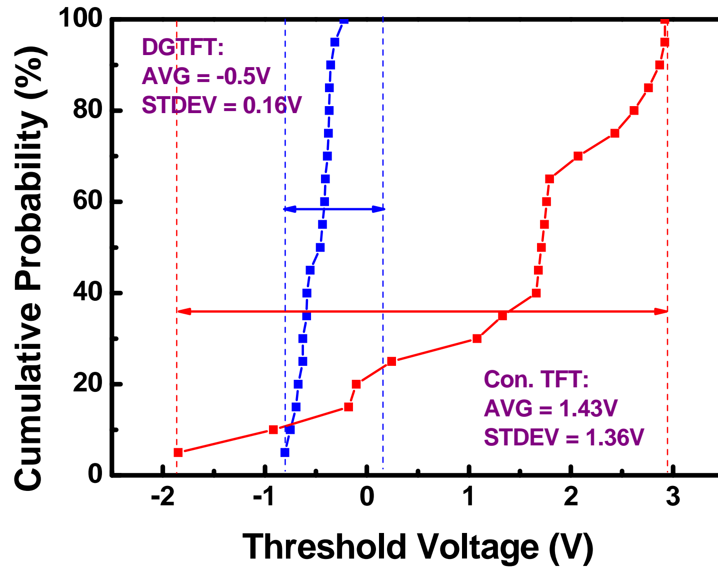


Fig. 2-49 Statistics and uniformity of threshold voltage. Twenty n-channel SGB-DG-TFTs crystallized with elevated channel method and conventional top gate TFTs were measured. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping)

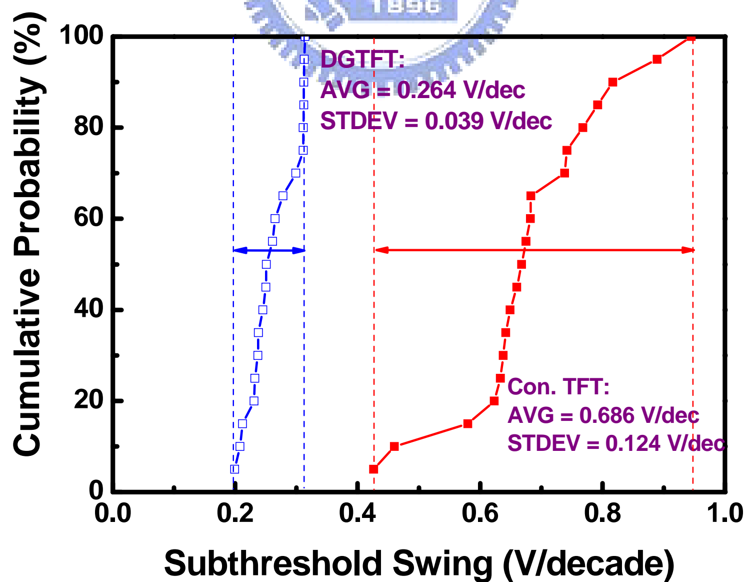


Fig. 2-50 Statistics and uniformity of subthreshold swing. Twenty n-channel SGB-DG-TFTs crystallized with elevated channel method and conventional top gate TFTs were measured. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping)

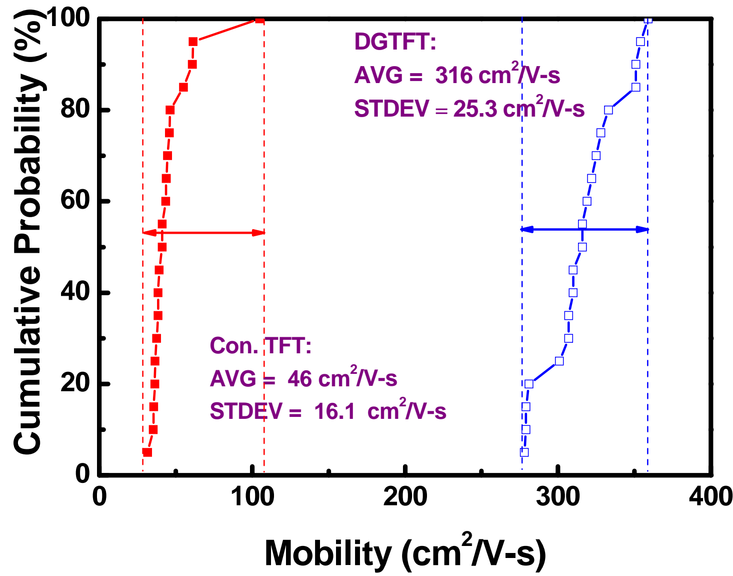


Fig. 2-51 Statistics and uniformity of equivalent field effect mobility. Twenty p-channel SGB-DG-TFTs crystallized with elevated channel method and conventional top gate TFTs were measured. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping)

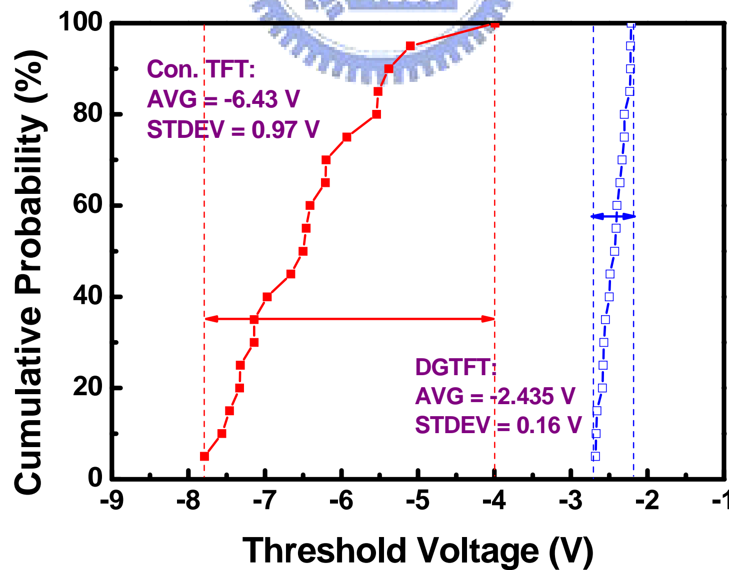


Fig. 2-52 Statistics and uniformity of threshold voltage. Twenty p-channel SGB-DG-TFTs crystallized with elevated channel method and conventional top gate TFTs were measured. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping)

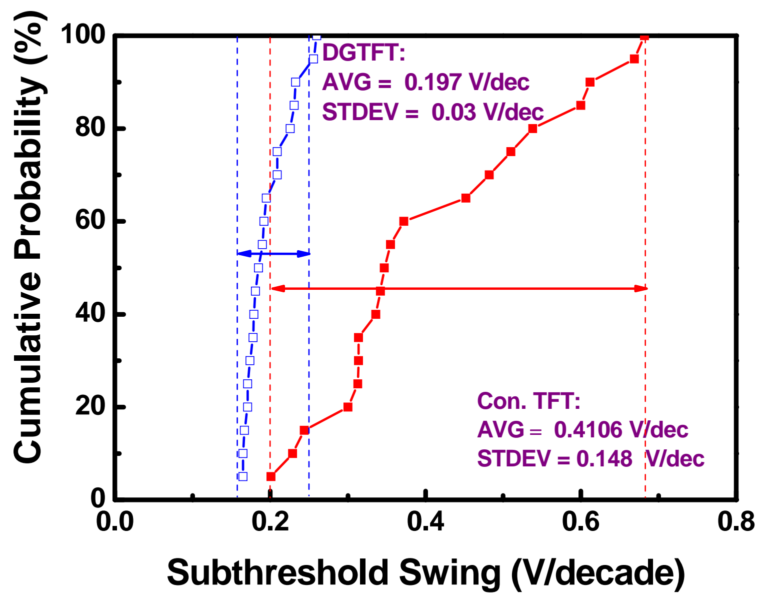


Fig. 2-53 Statistics and uniformity of subthreshold swing. Twenty p-channel SGB-DG-TFTs crystallized with elevated channel method and conventional top gate TFTs were measured. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping)

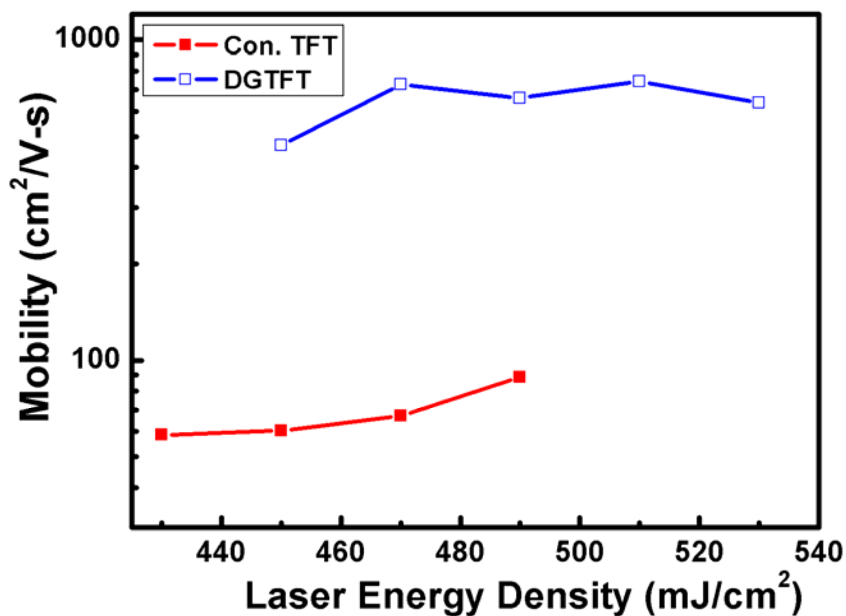


Fig. 2-54 The dependence of equivalent field effect mobility on laser energy densities for n-channel SGB-DG-TFTs crystallized with elevated channel method and conventional TFTs. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping).

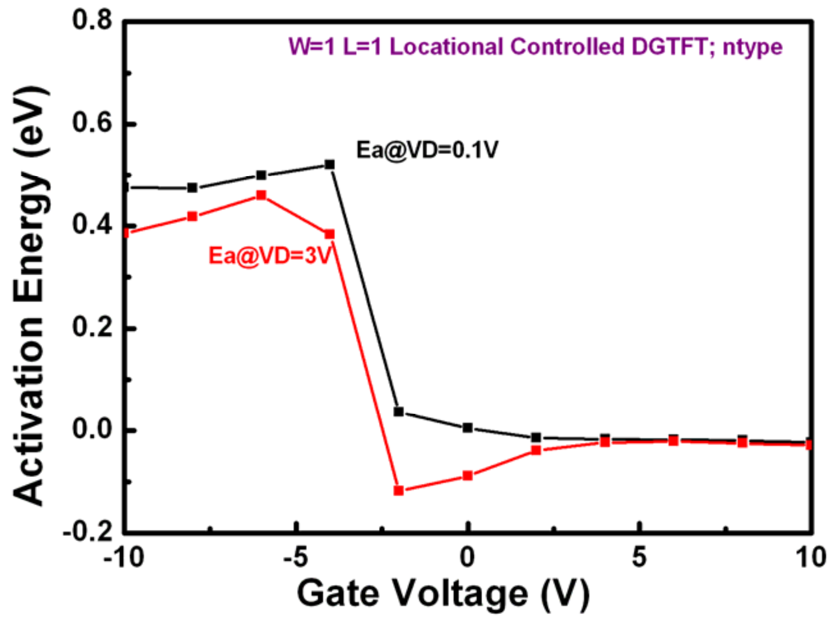


Fig. 2-55 The dependence of activation energy of drain current on gate bias voltage for n-channel SGB-DG-TFTs crystallized with elevated channel method. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping).

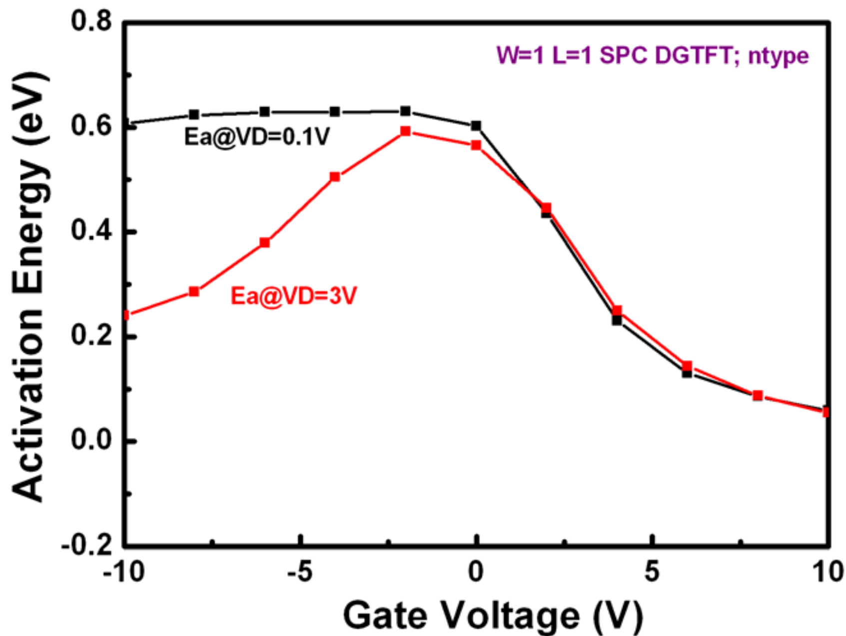
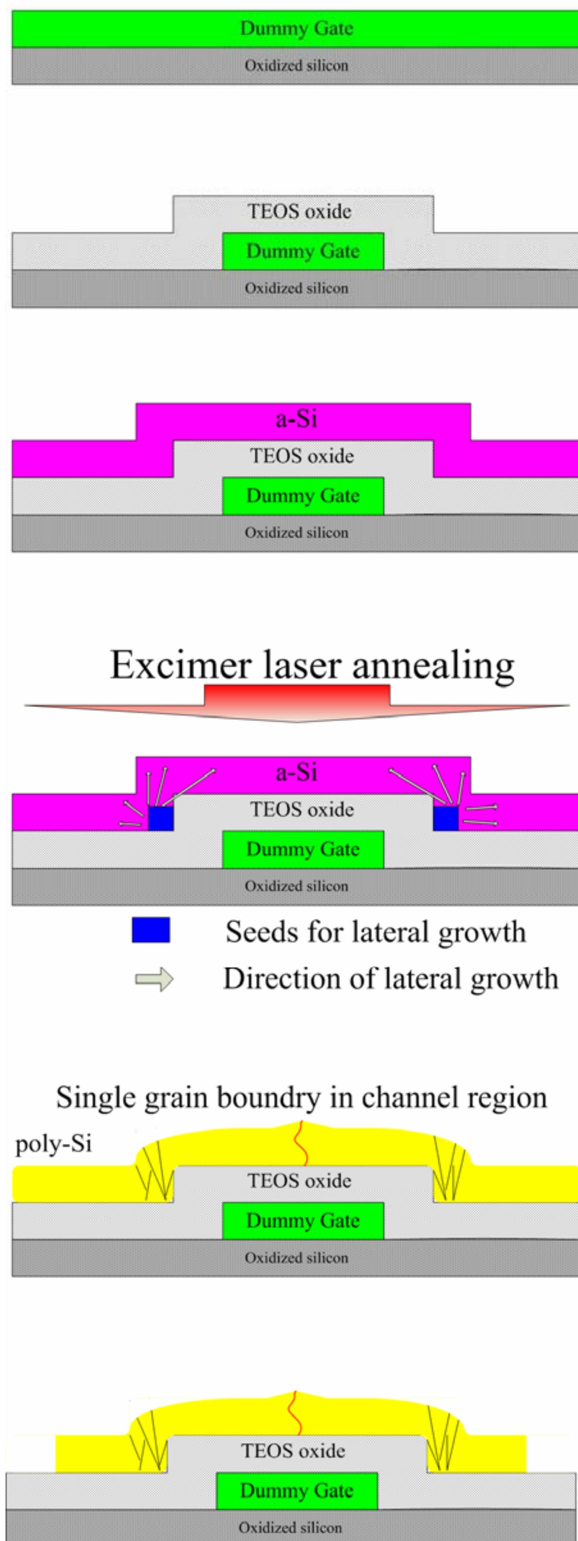


Fig. 2-56 The dependence of activation energy of drain current on gate bias voltage for n-channel DG-TFTs crystallized with solid phase crystallization. The thickness of gate oxide was 1000Å.



1000A in-situ doping phosphorous polycrystalline silicon was deposited by LPCVD at 550°C.

1. Poly gate patterned by TCP-RIE.
2. 1000A TEOS oxide was deposited by LPCVD at 700°C.

1000A amorphous silicon was deposited by LPCVD at 550°C.

The a-Si thin film was subjected to excimer laser irradiation at room temperature and the number of laser shots was 10/20 shots.

After excimer laser irradiation the single grain boundary polycrystalline silicon thin film was formed.

Active region define by TCP-RIE.

Fig. 3-1 Process flows for fabrication of SGB-TG-TFTs (I)

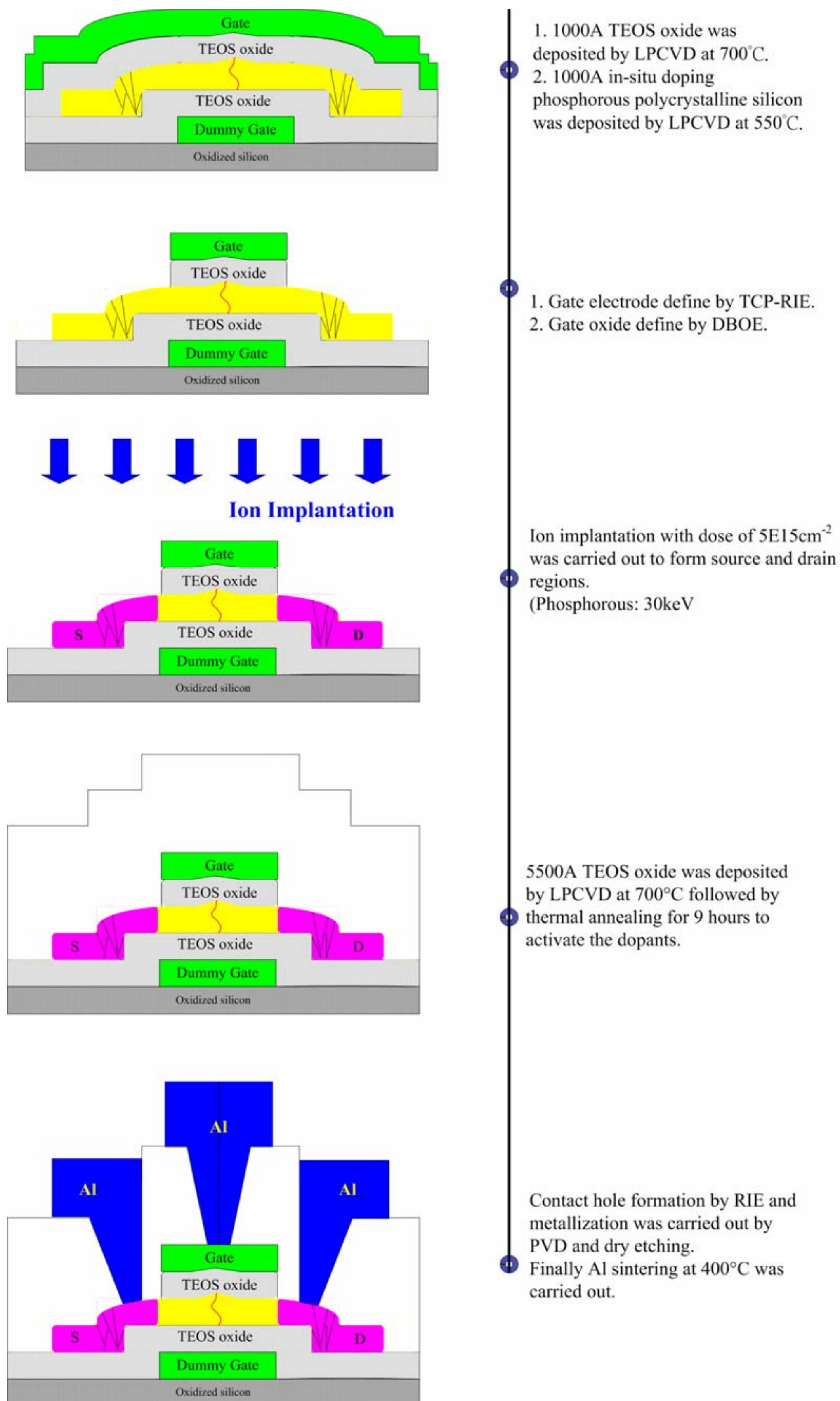


Fig. 3-1 Process flows for fabrication of SGB-TG-TFTs (II)

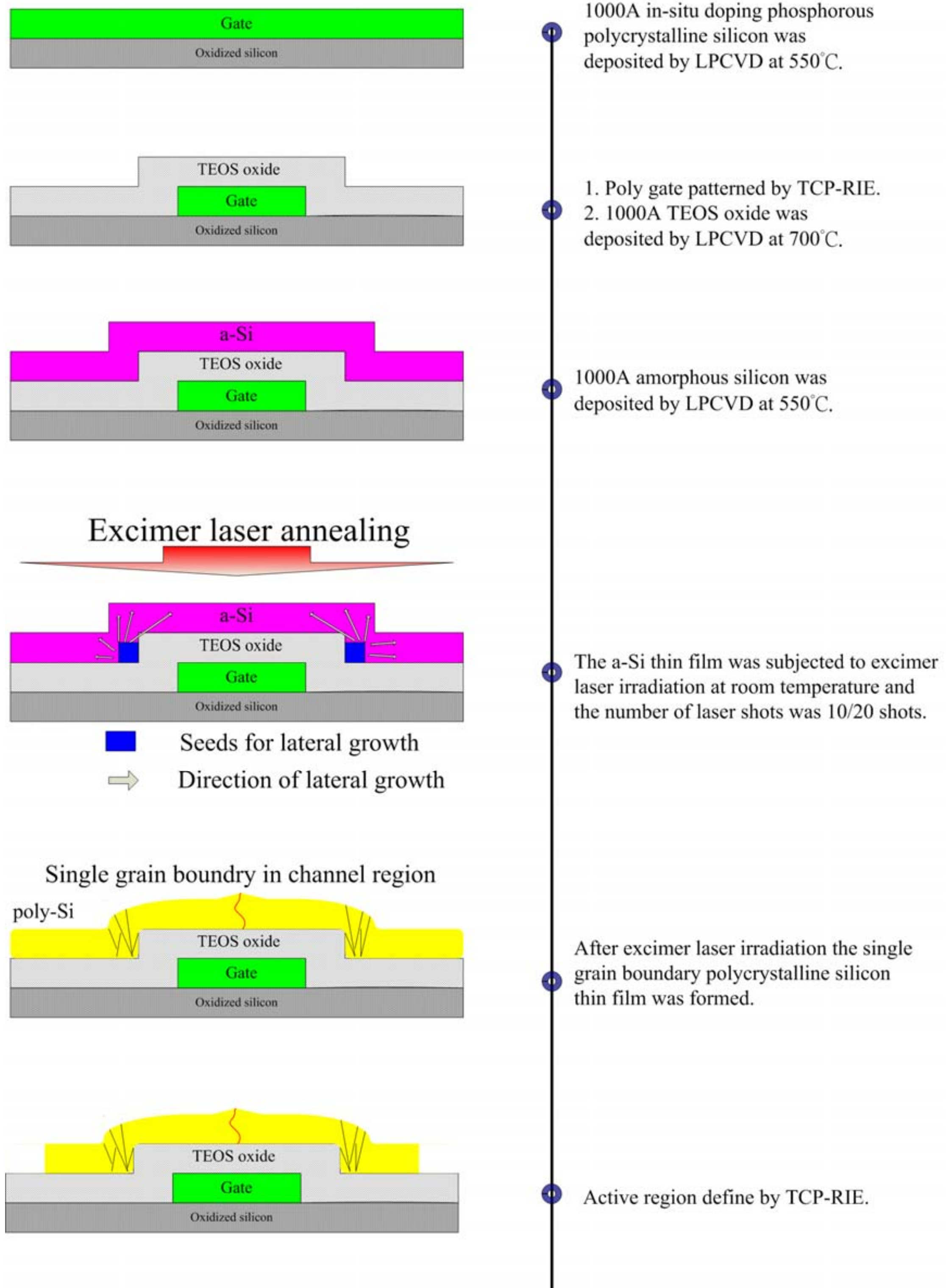
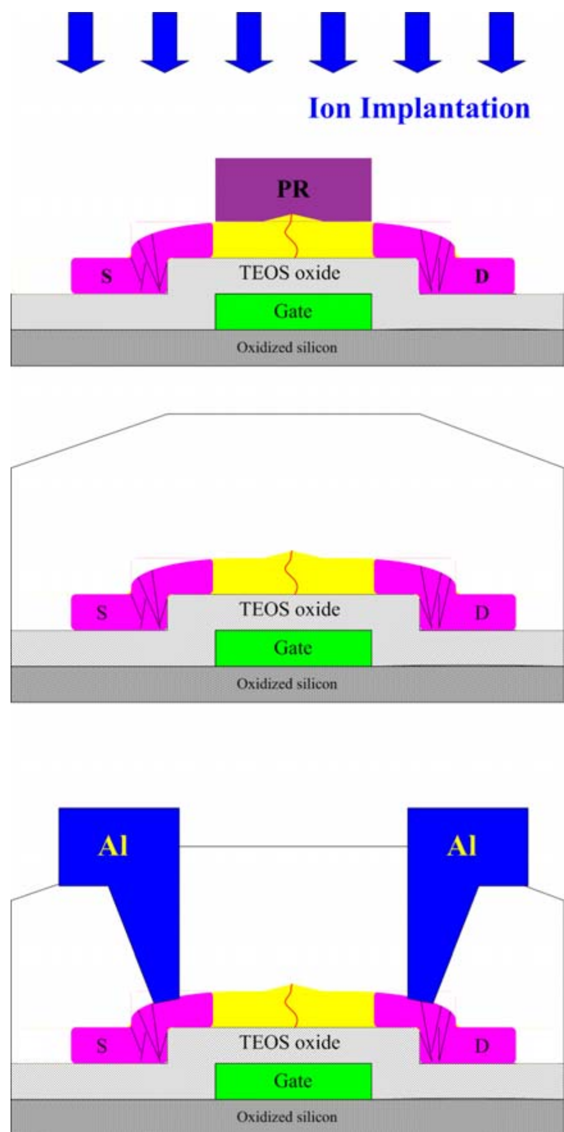


Fig. 3-2 Process flows for fabrication of SGB-BG-TFTs (I)



Ion implantation with dose of 5E15cm^{-2} was carried out to form source and drain regions.
(BF2: 45keV)

5500A TEOS oxide was deposited by LPCVD at 700°C followed by thermal annealing for 9 hours to activate the dopants.

Contact hole formation by RIE and metallization was carried out by PVD and dry etching.
Finally Al sintering at 400°C was carried out.

Fig. 3-2 Process flows for fabrication of SGB-BG-TFTs (II)

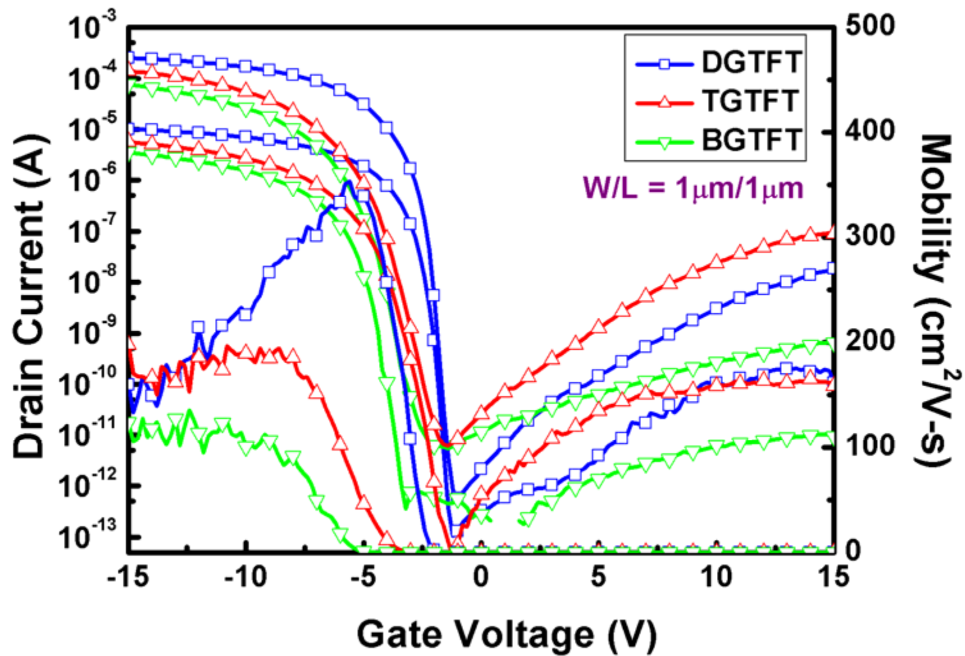


Fig. 3-3 Transfer characteristic of p-channel top/bottom/double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1 μm, in which the thickness of gate oxide was 1000 Å. The number of laser shots was 10 (ie. 90% overlapping).

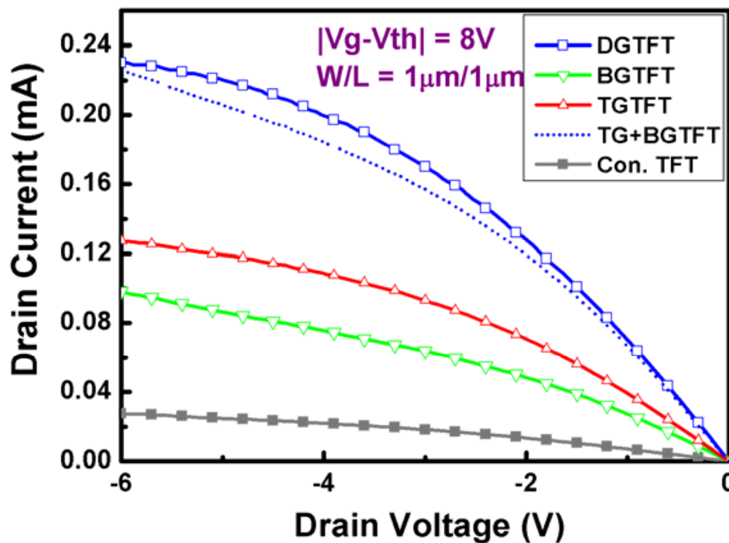


Fig. 3-4 Output characteristic of p-channel top/bottom/double gate polycrystalline silicon TFTs crystallized using elevated channel method and conventional TFTs with channel length of 1 μm, in which the thickness of gate oxide was 1000 Å. The number of laser shots was 10 (ie. 90% overlapping).

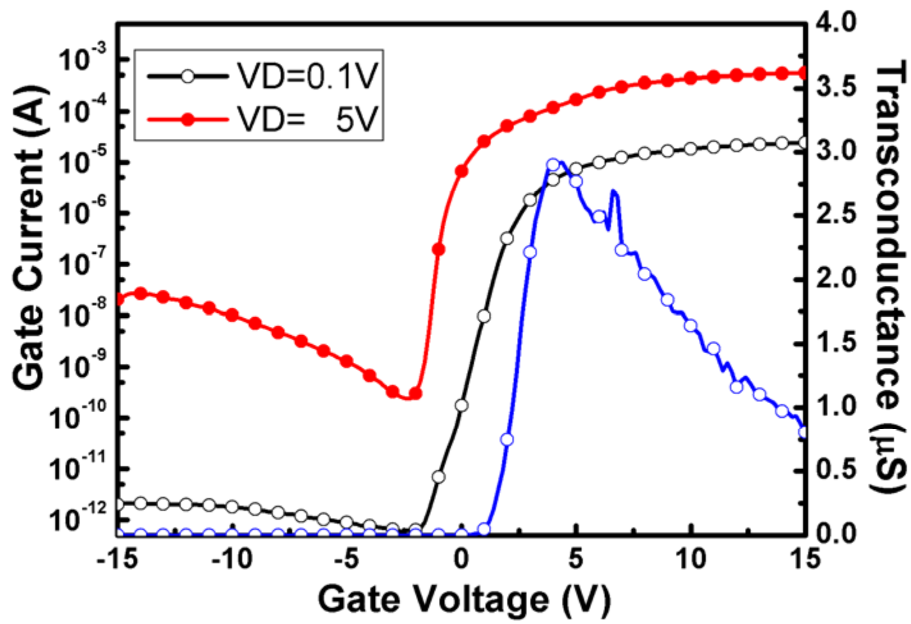


Fig. 3-5 The leakage current issue of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1 μm, in which the thickness of gate oxide was 1000 Å. The number of laser shots was 20 (ie. 95% overlapping).

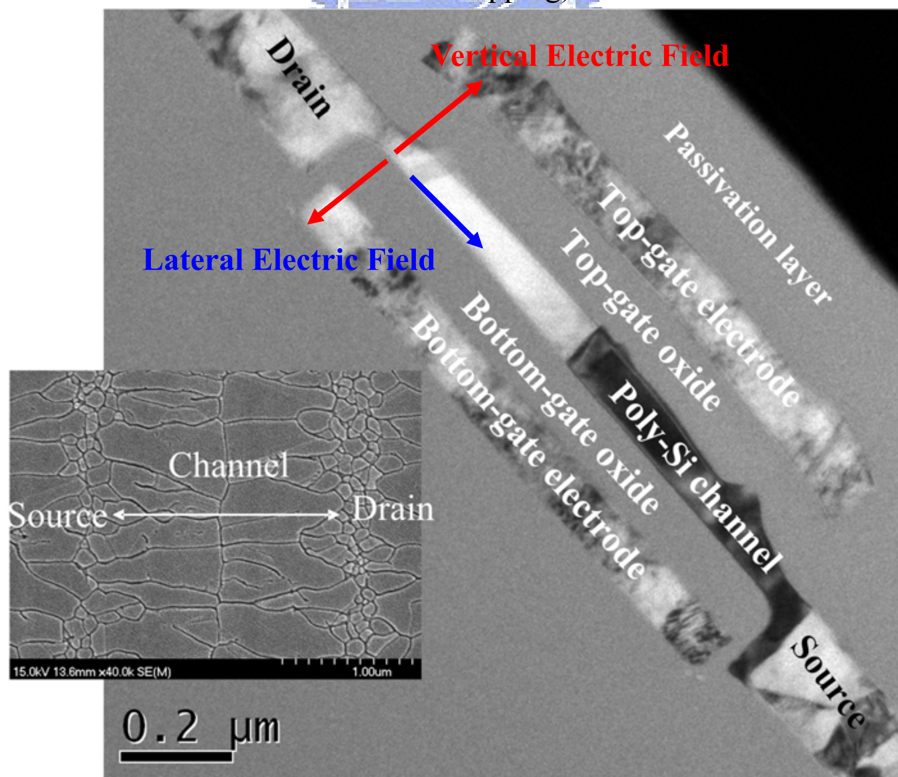


Fig. 3-6 TEM observation of double gate polycrystalline silicon TFTs crystallized using elevated channel method, in which the thickness of gate oxide was 1000 Å.

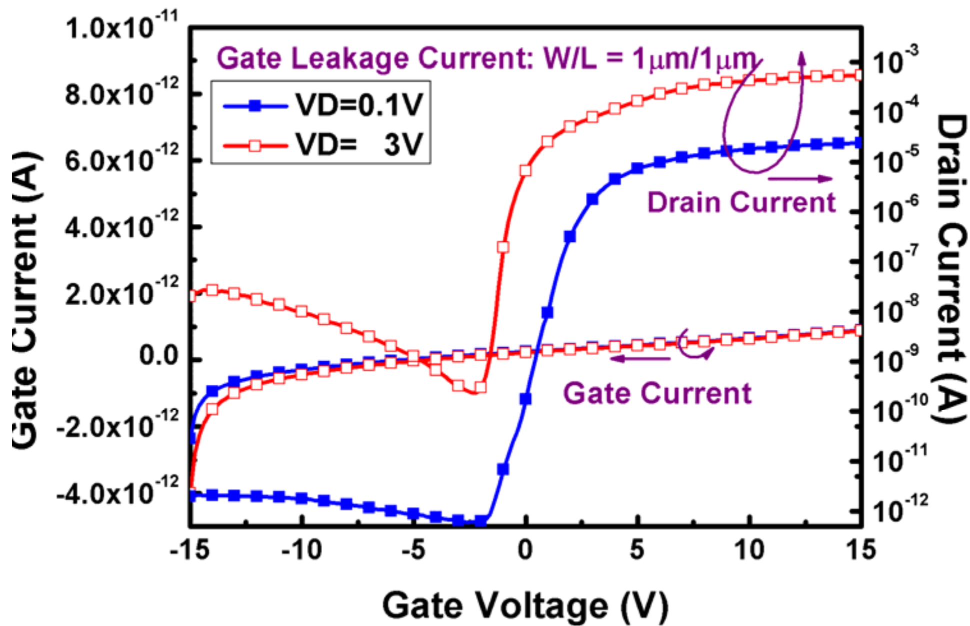


Fig. 3-7 The leakage current issue of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with channel length of 1 μm, in which the thickness of gate oxide was 1000 Å. The number of laser shots was 20 (ie. 95% overlapping).

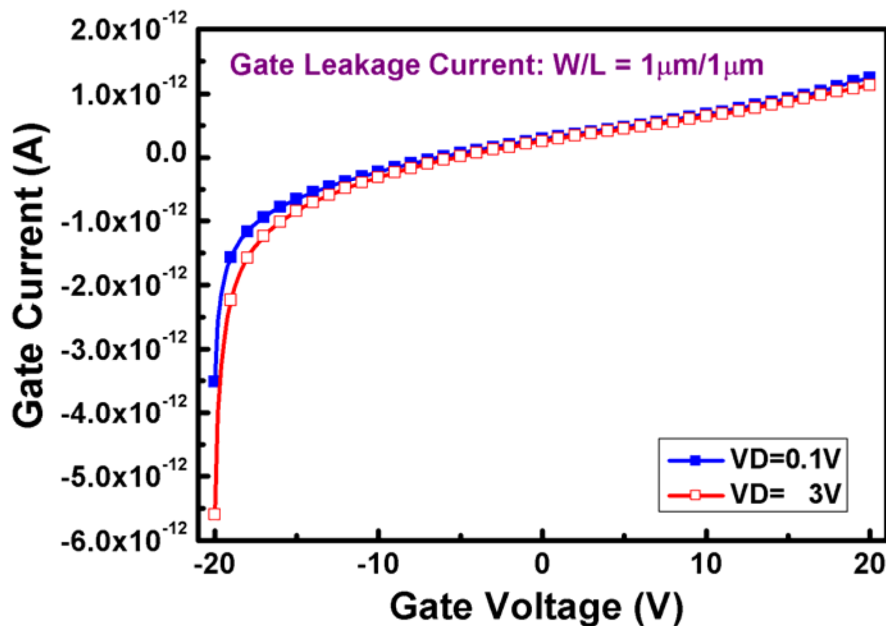


Fig. 3-8 The leakage current issue of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method measured from Vg = -20V to Vg= 20V with channel length of 1 μm, in which the thickness of gate oxide was 1000 Å. The number of laser shots was 20 (ie. 95% overlapping).

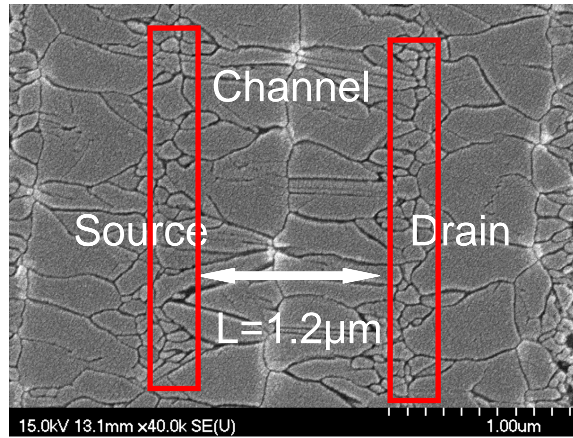


Fig. 3-9 SEM graphs of excimer laser crystallized polycrystalline silicon by elevated channel method. The channel length was varied from 1.2 μm. The bottom poly gate thickness was 1000Å and the gate oxide thickness was 500Å. The laser energy density was 510 mJ/cm^2

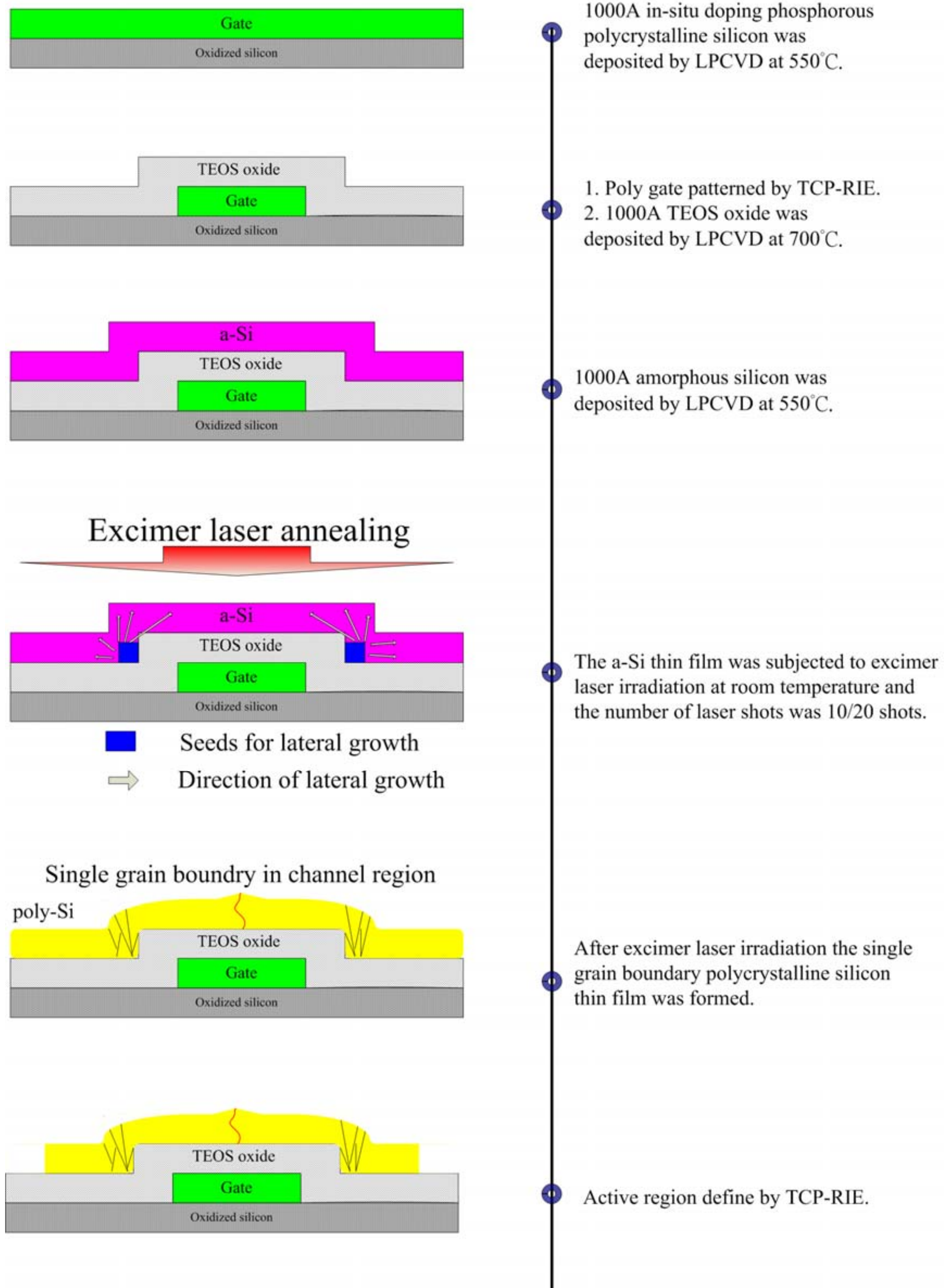
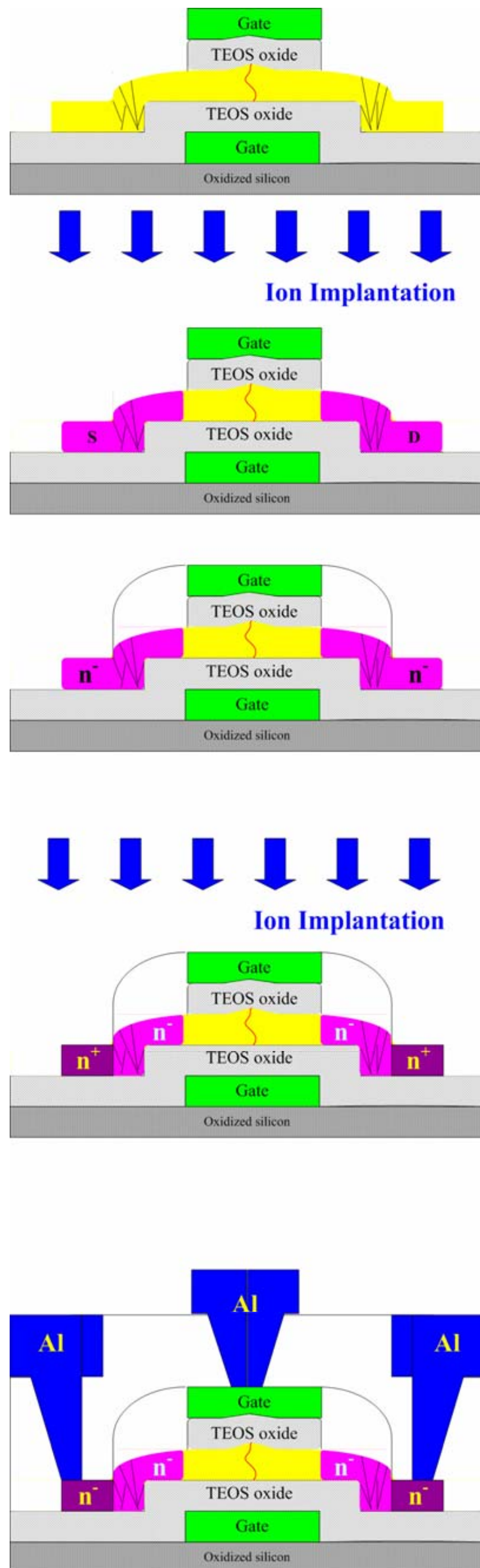


Fig. 3-10 Process flows for fabrication of SGB-DG-TFTs with LDD Structure (I)



1. 1000A TEOS oxide was deposited by LPCVD at 700°C.
2. 1000A in-situ doping phosphorous polycrystalline silicon was deposited by LPCVD at 550°C.
3.Gate electrode define by TCP-RIE.
4. Gate oxide define by DBOE.
5. Top gate and bottom gate contact hole etching.

Ion implantation with dose of 1E13cm^{-2} was carried out to form source and drain regions.
(Phosphorous: 30keV)

2500A TEOS oxide was deposited by PECVD at 385°C and patterned by RIE.

Ion implantation with dose of 5E15cm^{-2} was carried out to form source and drain regions.
(Phosphorous: 30keV)

1. 5500A TEOS oxide was deposited by LPCVD at 700°C followed by thermal annealing for 9 hours to activate the dopants.
2. Contact hole formation by RIE and metallization was carried out by PVD and dry etching.
Finally Al sintering at 400°C was carried out.

Fig. 3-10 Process flows for fabrication of SGB-DG-TFTs with LDD Structure (II)

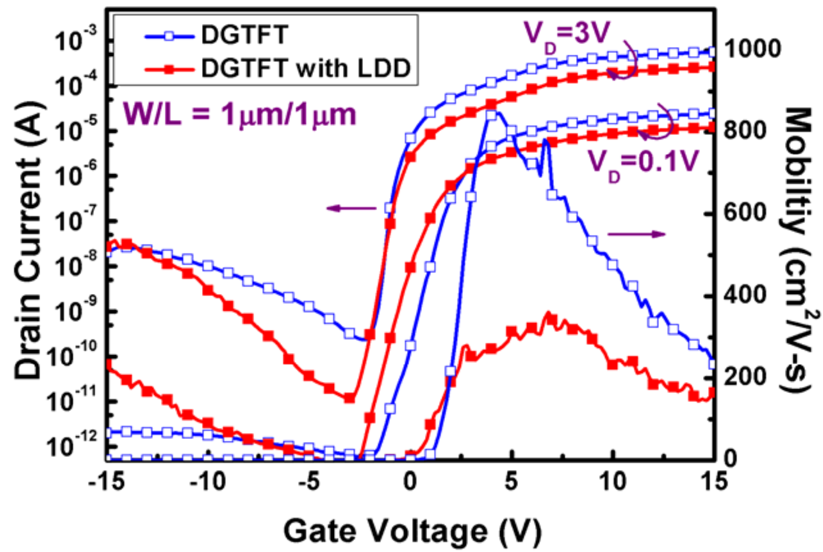


Fig. 3-11 Transfer characteristic of n-channel double gate polycrystalline silicon LDD TFTs crystallized using elevated channel method with channel length of 1 μm, in which the thickness of gate oxide was 1000 Å. The number of laser shots was 20 (ie. 95% overlapping).

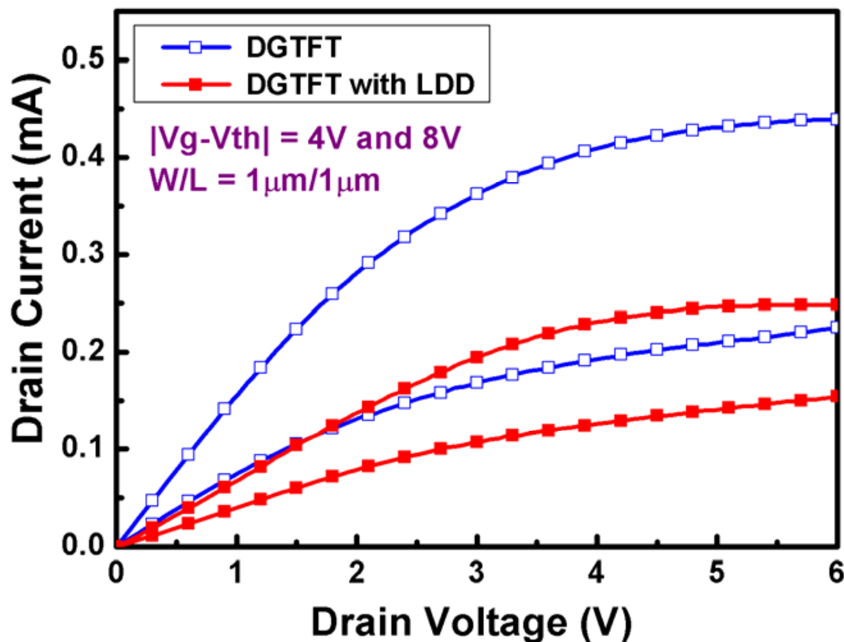
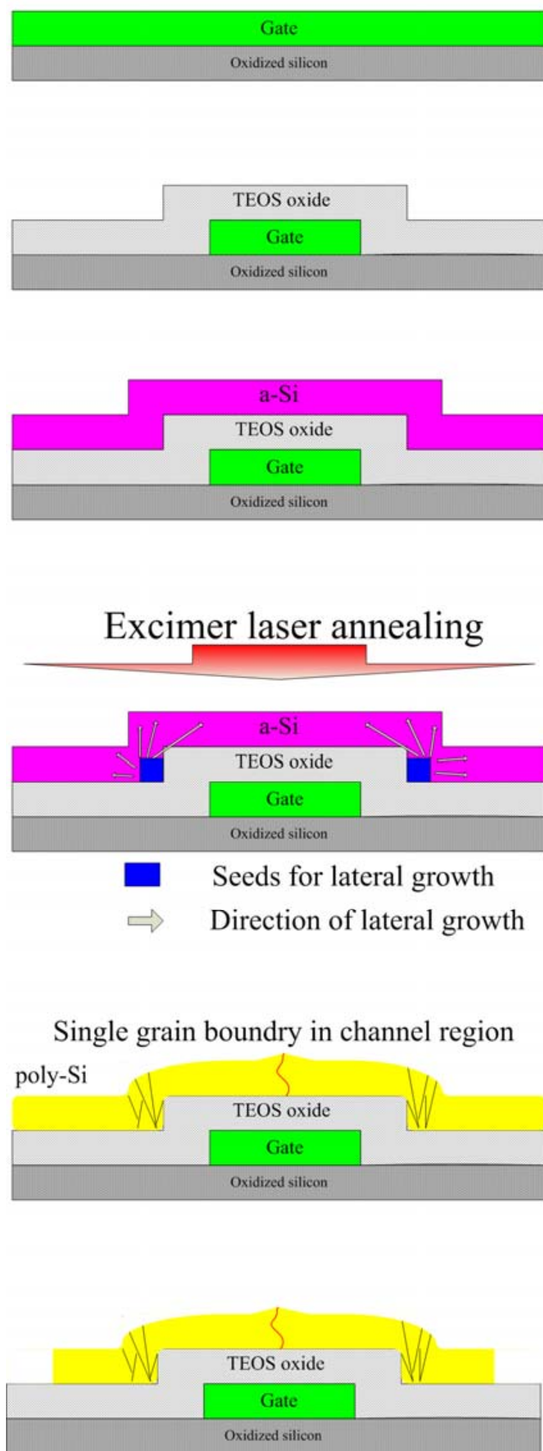


Fig. 3-12 Output characteristic of n-channel double gate polycrystalline silicon LDD TFTs crystallized using elevated channel method with channel length of 1 μm, in which the thickness of gate oxide was 1000 Å. The number of laser shots was 20 (ie. 95% overlapping).



1000A in-situ doping phosphorous polycrystalline silicon was deposited by LPCVD at 550℃.

1. Poly gate patterned by TCP-RIE.
2. 1000A TEOS oxide was deposited by LPCVD at 700℃.

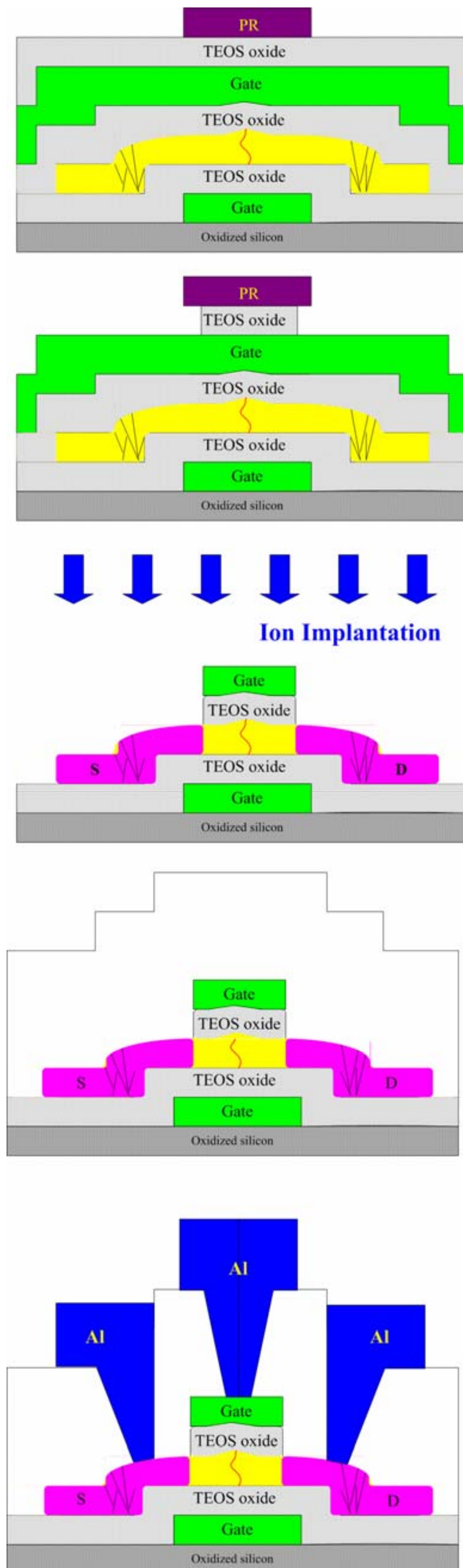
1000A amorphous silicon was deposited by LPCVD at 550℃.

The a-Si thin film was subjected to excimer laser irradiation at room temperature and the number of laser shots was 10/20 shots.

After excimer laser irradiation the single grain boundary polycrystalline silicon thin film was formed.

Active region define by TCP-RIE.

Fig. 3-13 Process flows for fabrication of SGB-DG-TFTs with Shrunk Gate Engineering (I)



1. 1000A TEOS oxide was deposited by LPCVD at 700°C.
2. 1000A in-situ doping phosphorous polycrystalline silicon was deposited by LPCVD at 550°C.
3. 1000A TEOS oxide was deposited by PECVD at 385°C as hard mask layer.

1. Gate definition
2. Hard mask define by RIE and side etch of DBOE
3. Strip of PR
4. Top gate defined by TCP-RIE
5. Top gate insulator etch by DBOE

Ion implantation with dose of 5E15cm^{-2} was carried out to form source and drain regions.
(Phosphorous: 30keV)

5500A TEOS oxide was deposited by LPCVD at 700°C followed by thermal annealing for 9 hours to activate the dopants.

Contact hole formation by RIE and metallization was carried out by PVD and dry etching.
Finally Al sintering at 400°C was carried out.

Fig. 3-13 Process flows for fabrication of SGB-DG-TFTs with Shrunk Gate Engineering (II)

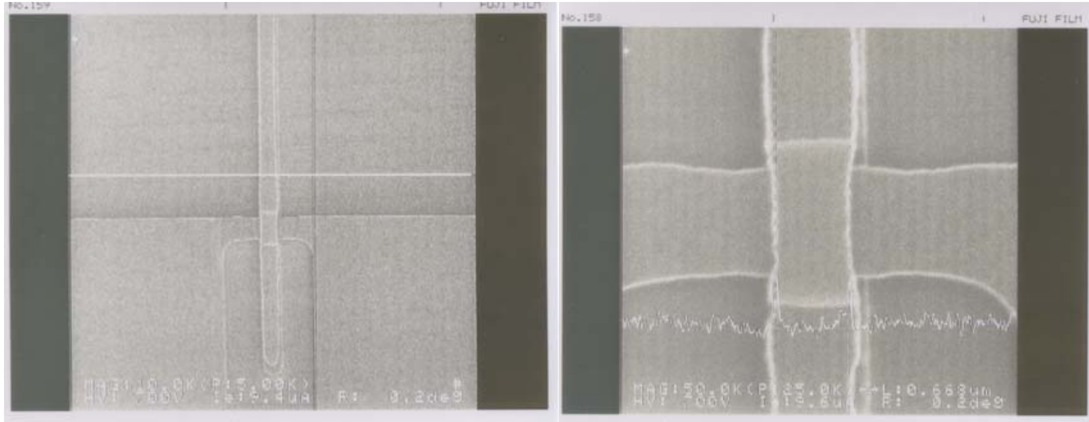


Fig. 3-14 In-line SEM observation of shrunk gate.

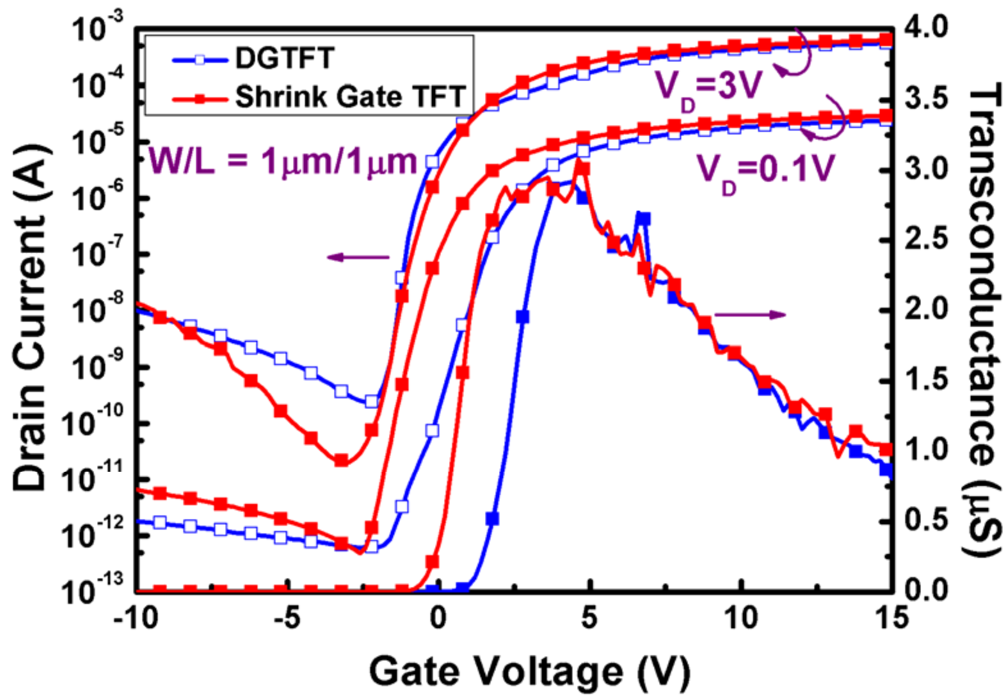


Fig. 3-15 Transfer characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with shrunk gate, in which the thickness of gate oxide was 1000 Å. The number of laser shots was 20 (ie. 95% overlapping).

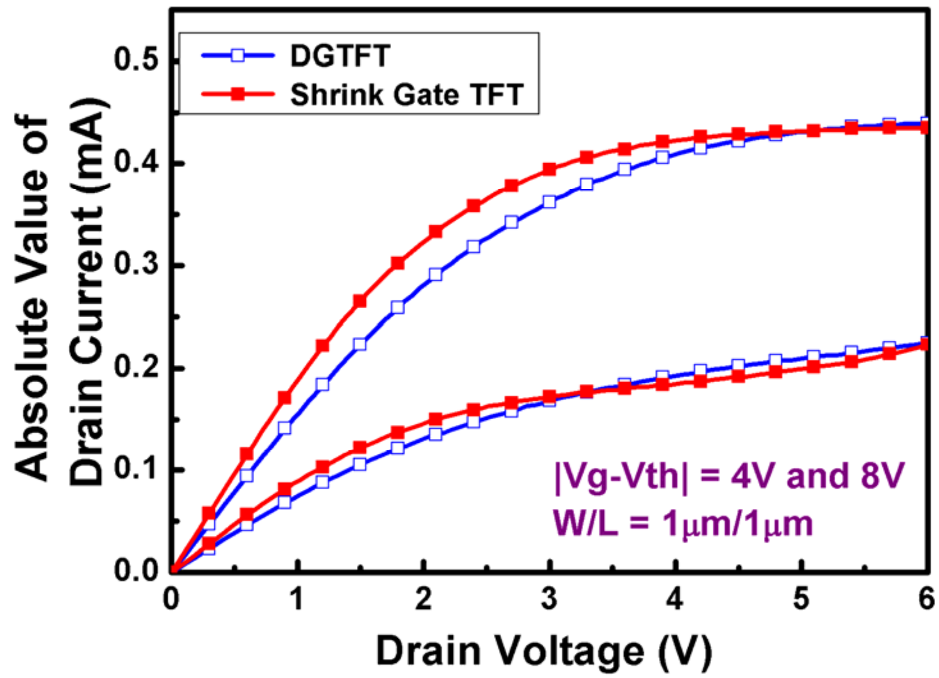


Fig. 3-16 Output characteristic of n-channel double gate polycrystalline silicon TFTs crystallized using elevated channel method with shrunk gate, in which the thickness of gate oxide was 1000 Å. The number of laser shots was 20 (ie. 95% overlapping).

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Chapter 1

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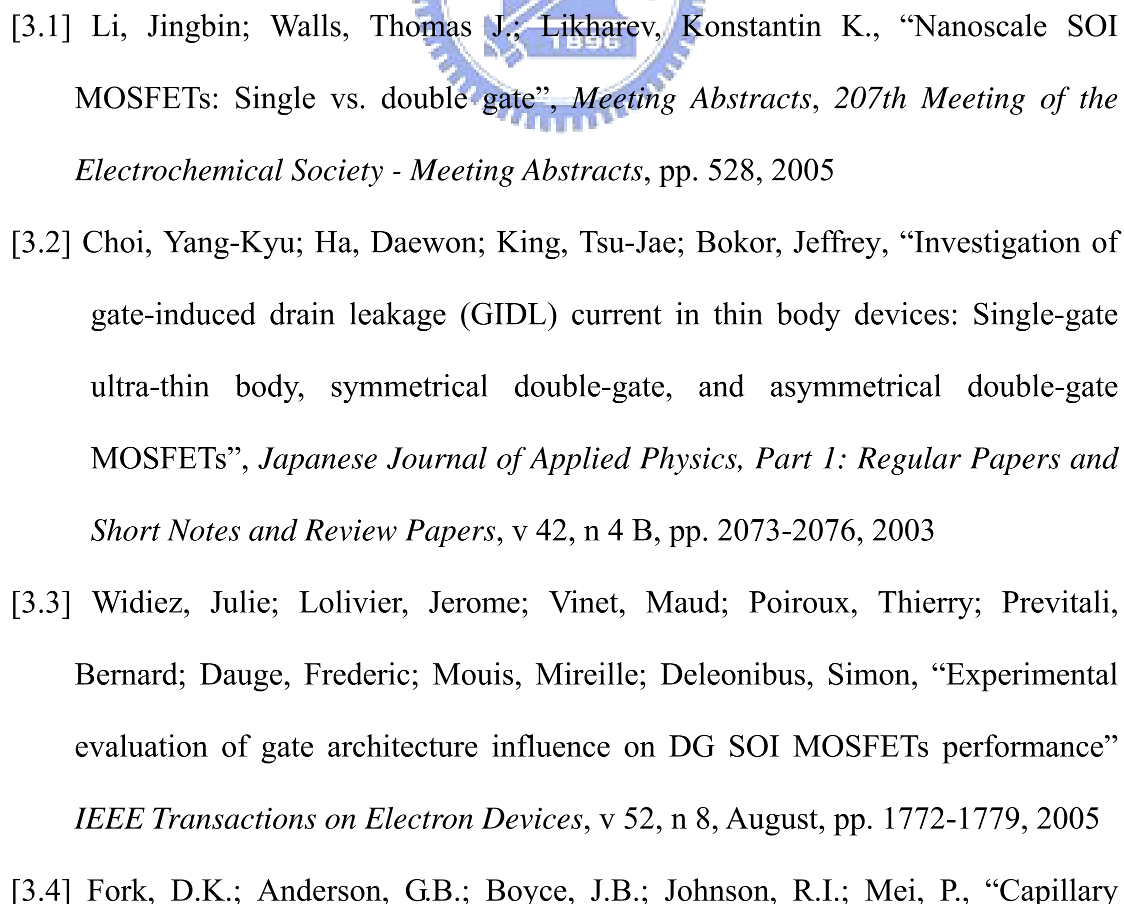

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論文題目：Study on the Polycrystalline Silicon Thin-Film Transistors with Location-Controlled Grain Boundary and Double Gate Structure Using Excimer Laser Annealing

以準分子雷射退火製作控制晶界位置之雙閘極複晶矽薄膜電晶體之研究