國立交通大學

電子工程學系 電子研究所碩士班

碩 士 論 文

SONOS 記憶體陣列中因二次熱電子引致寫入干擾之蒙地卡羅分析

Monte Carlo Analysis of Secondary Hot Electrons Induced Program Disturb in SONOS Memory Array

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中華民國 九十六 年 六 月

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A Thesis

Submitted to Department of Electronics Engineering & Institute of Electronics

College of Electrical Engineering and Computer Science

National Chiao Tung University

in partial Fulfillment of the Requirements

for the Degree of Master

in

Electronic Engineering

June 2006

Hsinchu, Taiwan, Republic of China

中華民國九十六年六月

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摘要

本篇論文之重點在於利用蒙地卡羅模擬，來分析一種新產生的寫入干擾模式。為了節省元件面積，近年 NOR 型態的 SONOS 元件採用潛擴散式的位元線技術(Buried Diffusion Bit-lines)製作，其操作方式為熱電子寫入(CHEI)與熱電洞抹除(BTBHH)。而在元件尺寸越來越縮小之後，在此種元件寫入的過程中，發現鄰近的元件也同時會被寫入，形成干擾。此一干擾的原因為熱電子寫入的同時產生的二次熱電子，透過蒙地卡羅模擬，也得到了與實驗趨勢相符的結果。最後，針對元件尺寸繼續縮小對此一寫入干擾的影響也有所評估。

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Abstract

This thesis is focused on a new program disturb in a two-bit storage buried diffusion bit-line SONOS flash memory. In a NOR-type SONOS flash memory, channel hot electron program and band-to-band hot hole erase are usually employed. In channel hot electron program operation, channel hot electrons will cause impact ionizations. Generated holes from impact ionizations will be accelerated by the drain-to-substrate voltage and cause second impact ionization. The second impact ionization generated electrons, referred to as secondary electrons, may flow to a neighboring cell and cause a program disturb. In this thesis, a multi-step Monte Carlo simulation is used to explore this mechanism for it can accurately obtain the high energy tail of the secondary electron distribution function. Both electron and hole Monte Carlo simulations in this thesis include a full-band structure. In addition, the effects of substrate bias, bit-line dimension and pocket implant on the program disturb will be characterized and evaluated by a Monte Carlo simulation.

Acknowledgements

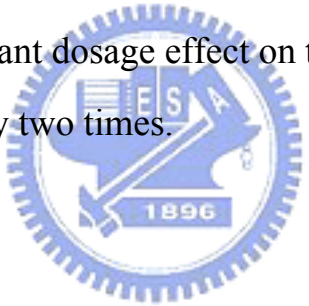
The author wishes to express his deep feeling of gratitude to his advisor, Professor Tahui Wang, for his patient guidance, encouragement, supports and insight during the course of this study. Moreover, the author wants to thank the members of the DSML; Little Rabbit, David, Little Cheng, Little Ma, Dada Tang, Shedd, Ilv, Sunfan, Big Bear, Small Duck, Afo, and Markwu for their useful discussions and teaching, it's them who make his life colorful in these days.

In addition, the author sincerely appreciates T. C. Lu, Y. W. Chang and many colleagues from MXIC. Without their supporting for the advanced devices and the precious experiences, this thesis will not be easily accomplished.

Finally, the author gives the greatest appreciation to his family for their love and care during growing and developing, which makes the author become a mature and brave person.

Contents

Figure Captions



Chapter 1

Introduction

Nonvolatile memories play an important role in our VLSI industry. For their wide applications, you can find them in mobile phones, personal computers, digital cameras and many hi-tech products. Recently, nitride-based trapping layer flash memories (SONOS) [1–4] have received great interest due to their smaller bit size [5], simpler fabrication process [6] and better charge retention [7] for locally stored charges. In a NOR-type SONOS memory, a virtual ground array with buried diffusion (BD) bit-lines is implemented [5] to achieve a higher package density. For two-bit per cell operation, Channel Hot Electron Injection (CHEI) and Band-to-Band Hot Hole Injection are used for programming and erasing, respectively. Previous studies have shown that, in channel hot electron programming, channel initiated secondary electrons play an important role in charge injection [8]. However, as the width of a BD bit-line in a SONOS array is further reduced, impact ionization-generated secondary electrons may flow to a neighboring cell and cause a program disturb. To explore this new failure mode, a SONOS mini-array is used. Thus, the evolution of the threshold voltages of both programmed bit and disturbed bit can be monitored simultaneously. Extensive characterization and a multi-step Monte Carlo simulation were performed to study this failure mode.

In chapter 2, the structure of NOR-type SONOS array will be illustrated, and the operation mechanisms including programming and erasing will be introduced. Recently, CHEI was taken as the major mechanism of programming. However, the extra gate current contributed from secondary hot electrons is compatible to the primary one when the programming window is high, which is called CHannel Initiated Secondary ELectron (CHISEL) [9]. As device gate length continues to scale down, CHISEL is becoming more and

more important mechanism for programming.

When a SONOS array is under programming, a positive voltage is applied to the word line (e.g., VG = 9V) and bit line (e.g., VD = 4.2V), respectively. In this bias condition, a new program disturb mode is induced by secondary hot electrons. In addition to the programmed bit, the neighboring bits are also programmed. The ratio of V_T shift between primary bit and neighboring bits can be up to 5, which seriously degrades the SONOS array reliability. The detailed experimental measurement will be shown in chapter 3.

In chapter 4, a Monte Carlo simulation is used to analyze program disturb induced from secondary hot electrons, and the simulation results show good agreement with experiments. Moreover, the dependence of the program disturb on bit-line geometry, substrate bias and pocket dosages will be evaluated, which gives us a guideline to improve device performance.

Conclusions are finally given in chapter 5.

Chapter 2

Array Structure and Operations of SONOS Flash Memory

2.1 Introduction

Due to the limited scalability of the traditional floating gate flash memory, SONOS flash memory with SiN traps as charge storage media was invented. A recent report [10] also revealed that the revenues of nonvolatile memory had reached more than 19 billion dollars in a single year, which was attributed to the rapid growth of many new applications. According to their functions, the nonvolatile memories are divided into two types. For code storage, it needs fast and random access capabilities provided by the NOR architecture; on the other hand, data storage needs page access by NAND architecture. The different operation modes are shown in [10]. In this thesis, we will focus on the NOR-type flash memory.

2.2 Buried Diffusion Bit-Line SONOS Memory

For a conventional SONOS memory, the cell was fabricated by standard CMOS process, and the gate dielectric was replaced by an ONO layer. Furthermore, a novel process, the buried diffusion bit-line structure, was introduced to increase the density of the array. Unlike the Shallow Trench Isolation (STI) structure, the junction is diffused under the bit-line oxide, so it saves the space of two junctions in a cell. The cell can be processed in a virtual ground array, where word lines (WLs) and buried diffusion bit lines (BLs) are crisscrossed, as indicated in Fig. 2.1. It's flat and contactless because there is no filed isolation, and a very tight BL pitch is allowable in such a structure. In a typical 0.25μm technology process, the cell area of each bit is $0.188\mu m^2$ [5].

2.3 Operation Modes

For a NOR-type SONOS array, it is utilized for code storage, so the operation modes is different from the NAND-type array. The erasing and programming are performed by Band-to-Band Hot Hole (BBHH) and Channel Hot Electron Injection (CHEI), respectively [11]. The erase and program state behaviors of the cell are shown in Fig. 2.2. Due to the CHEI programming, two-bit per cell operation is allowed by placing programmed charges locally in the nitride layer above the junction of source or drain. To read the programmed bit, a "reverse read" method is used [5]. For example, when we want to read the bit in drain side, a bias is applied at source to sense the V_t. Moreover, the applied voltage must be sufficiently large to cover the charges in source side (e.g., V_s>1.6V). However, in CHEI programming a large lateral field will accelerate the electrons to high energy state in order to cross the oxide barrier. In the meanwhile, some of the high energy electrons will cause first impact ionization which generates new electron-hole pairs, and then the generated holes accelerated by vertical field will cause second impact ionization, which generates the substrate electrons to result in disturbance. The detailed mechanisms will be discussed in the next chapter.

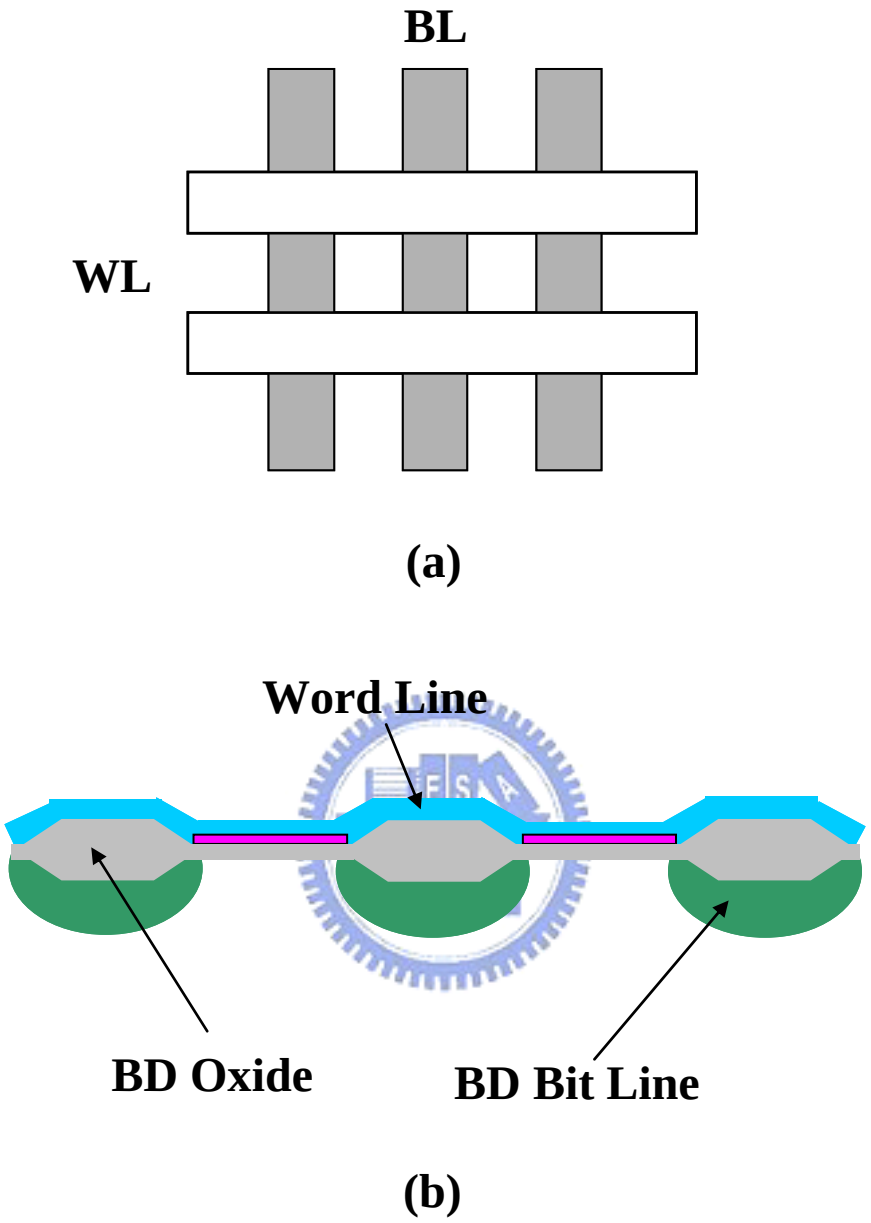


Fig. 2.1 Illustration of buried diffusion bit-line SONOS array

(a) Top view (b) Cross-section view

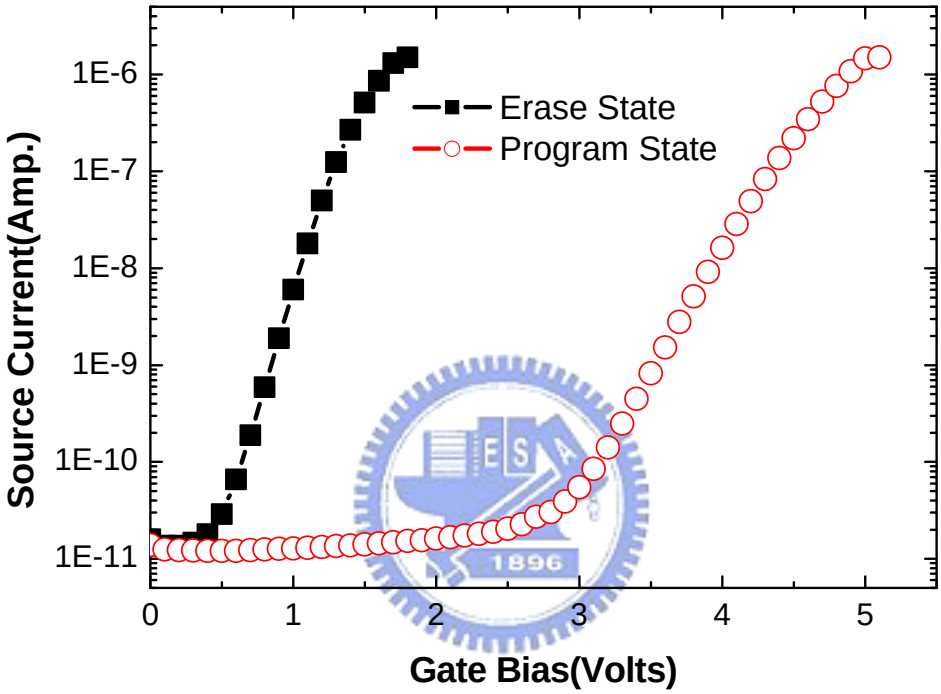


Fig. 2.2 Source current versus gate bias in erase state and in program state.

Chapter 3

New Program Disturb in a SONOS Array

3.1 Introduction

In a NOR-type SONOS flash memory utilizing CHEI programming, the threshold voltage shift still exists even the drain bias is less than 3V. And it reveals that some electrons may gain energy above 3eV to cross the oxide barrier (~3.1eV). Thus, there must be some additional programming mechanisms in SONOS memory. Moreover, it is believed that CHannel Initiated Secondary ELectron (CHISEL) is another important mechanism during programming [9]. Due to the high energy and broad distribution of CHISEL, they can cause further disturbance during programming in deep submicron devices. During cell programming, CHISEL will cause broadening of the injected charge in the programmed bit. The consequence is a degraded second bit effect [12, 13]. Besides, CHISEL may flow to a neighboring cell and cause a new mode of disturbance.

3.2 Channel Initiated Secondary Electron Programming

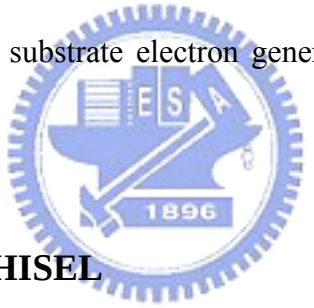
Fig. 3.1 illustrates the concept of CHISEL in a NOR-type flash memory. The channel electrons are accelerated by the drain field and electron-hole pairs are generated through first impact ionization (II). The generated electrons flow to the drain while the generated holes diffuse to the substrate. The generated holes will be accelerated by the drain-substrate potential drop and gain enough energy to cause second II. The electrons generated by second II flow back and are accelerated by the drain-substrate potential drop to gain sufficient energy at the SiO_2/Si interface. The secondary electron induced gate current can be expressed as [9]

$$I_G = I_D M_1 M_2 T \tag{1}$$

where M_1 and M_2 are multiplication factors of first and second II, respectively and T is

tunneling probability for the electrons to inject into the gate dielectric.

In previous studies, the energy and space distributions of CHISEL have been investigated. The energy of some secondary II generated electrons can be as great as $qV_D + qV_{bi} + q\delta\varepsilon_{sec}$, where qV_{bi} is the build-in potential energy and $q\delta\varepsilon_{sec}$ is the residual energy after twice II [8, 9]. Compared to primary electrons, though the number of secondary electrons is much smaller than that of primary electrons, their higher energy makes them become more efficient for programming. On the other hand, the space distribution of CHISEL is broader than that of CHEI [14, 15]. As a result, the secondary hot electrons will dominate the programming gate current. Moreover, as program time increase, the effective oxide barrier height increases due to charge build-up in the nitride layer. Thus, the injection efficiency is reduced. I would like to remark that although substrate electron generation via re-absorption of hot electrons emitted light is possible, the dominant substrate electron generation mechanism in this case is still second impact ionization.



3.3 Disturbance due to CHISEL

3.3.1 Second Bit Effect

For two-bit per cell operation in SONOS flash memory, the programming window is limited by second bit effect. The “reverse read” method is used by applying a bias at the opposite side of the reading side. If the charges distribution in the first bit is too broad to be screened by the read bias, it will become the noise when reading the second bit (Fig. 3.2). This phenomenon is called “second bit effect”. The measurement data is shown in Fig. 3.3. Obviously, in low program-state, bit-A is almost unaffected by bit B. However, when the ΔV_t of bit B is larger than 3V, ΔV_t of bit-A increases with the ΔV_t of bit-B. In other words, the subsequently programmed electrons affect the V_t of both sides, and CHISEL is responsible for it due to the wide injection region. This neighboring bit disturb is observed in NOR-type, two-bit per cell operation SONOS memory.

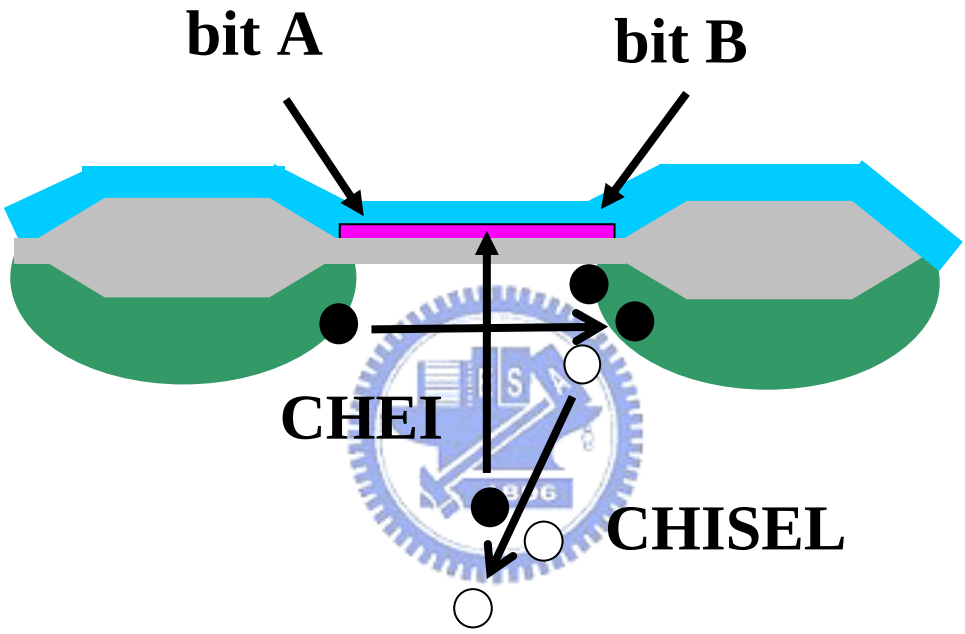


Fig. 3.1 Illustration of CHannel Initiated Secondary ELectrons (CHISEL)

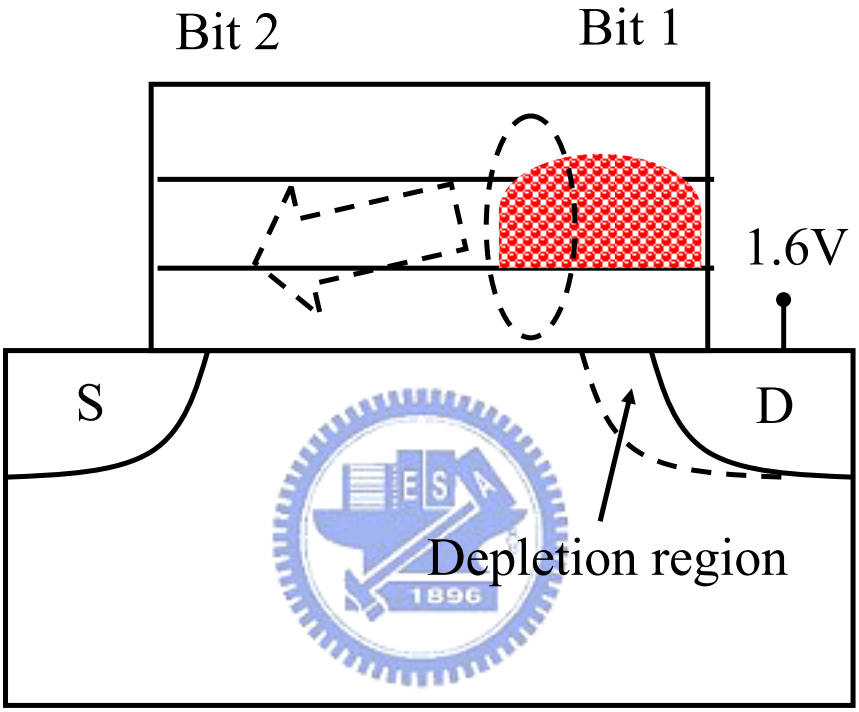


Fig. 3.2 Illustration of second bit effect due to the spread of bit 1 programmed charges.

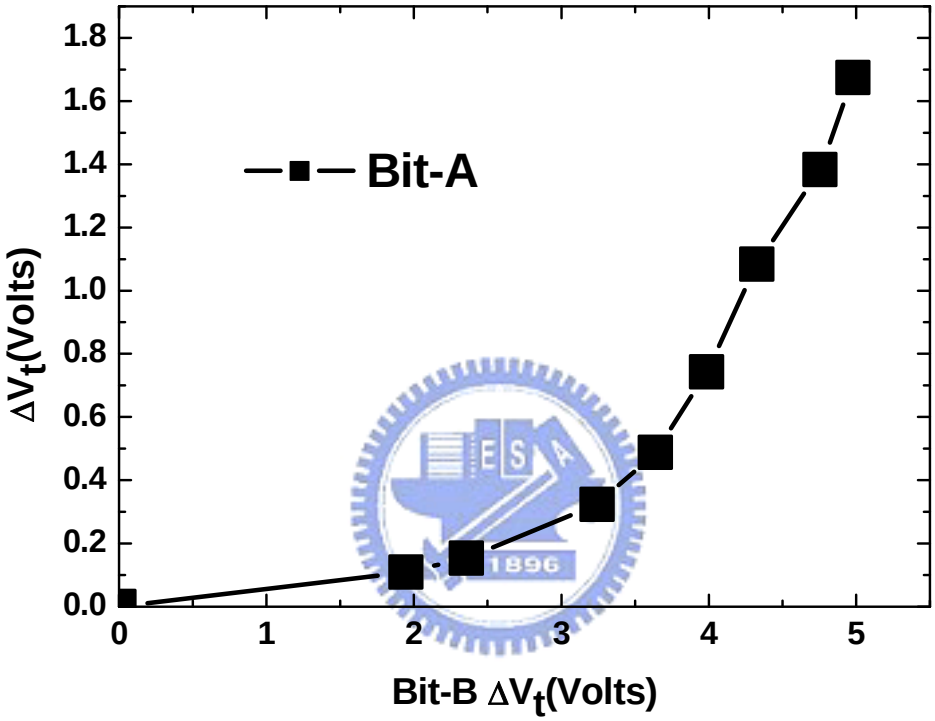


Fig. 3.3 ΔV_t of bit B and bit A during programming

3.3.2 Disturbance in Neighboring Cell

In a NOR-type SONOS array with buried diffusion (BD) bit-line structure, as the width of a BD bit-line is further reduced, impact ionization-generated secondary electrons may flow to a neighboring cell and cause a program disturb, as illustrated in Fig. 3.4. Bit B in cell 1 is a programmed bit and bit C and bit D in cell 2 are disturbed bits. The V_t evolutions of two neighboring cells in programming operation are measured (Fig. 3.5). The program disturb is more serious as the program window increases (Fig. 3.6). Similar to second bit effect, the new program disturb mode shows a two-region behavior in Fig. 3.3. For bit B being at a low program level, the slope of ΔVt(bit C) versus ΔVt(Bit B) is almost zero, which implies that the program speed in programmed bit is much faster than the disturbed one. As the program level of bit B increases (>3V), ΔVt of bit C and bit D increase with bit B. The reason is that programmed charges in bit B greatly increase the effective barrier height and hinders subsequent charge injection in bit B. Thus the charge injection rate in the disturbed bit becomes more significant, as compared to the programmed bit. To analyze such program disturb induced by secondary hot electrons, Monte Carlo simulation is required for it can correctly simulate carrier transport behavior of high energy carriers, and it will be demonstrated in chapter 4.

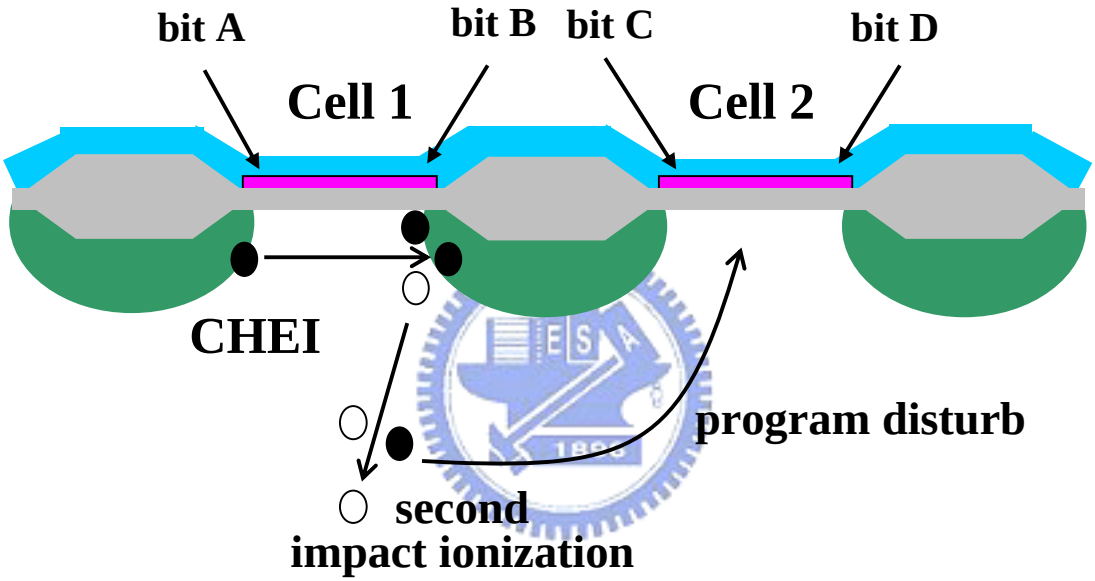


Fig. 3.4 Illustration of generation of secondary electrons which cause program disturb in neighboring cell.

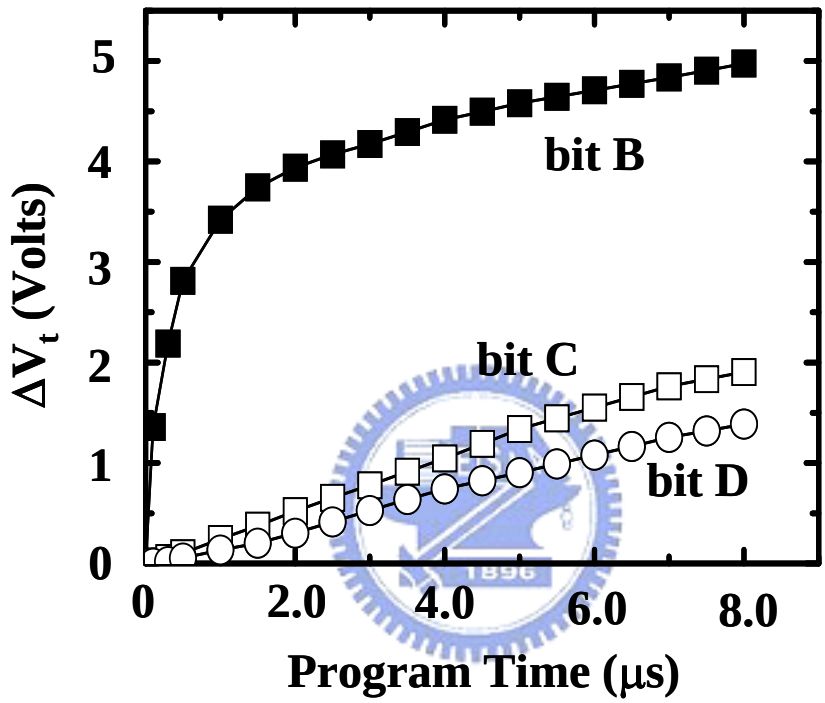


Fig. 3.5 Threshold voltage shift versus programming time. Bit B in cell 1 is a programmed bit and bits C and D in cell 2 are disturbed bits.

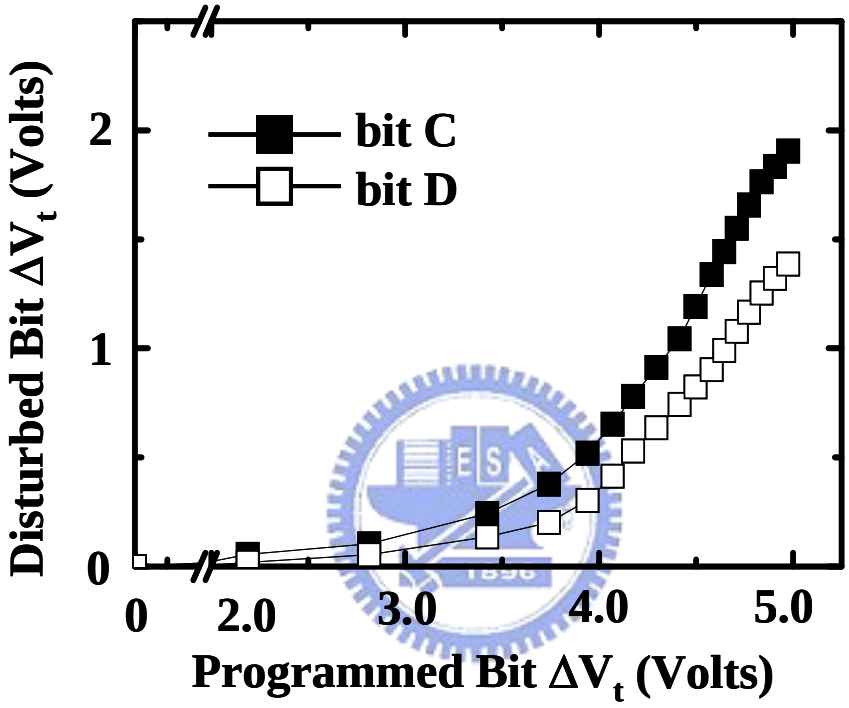


Fig. 3.6 Disturbed bit ΔV_t versus programmed bit ΔV_t.

Chapter 4

Monte Carlo Analysis of Program Disturb

4.1 Introduction

Monte Carlo (MC) methods are widely used for simulating the behaviors of physical and mathematical systems, especially for systems with a large number of coupled degrees of freedom. In particle transport of semiconductors, it is used to solve the Boltzmann Transport Equation (BTE). The Monte Carlo method can easily include all the scattering mechanisms, allow the inclusion of many realistic energy bands and simulate both steady and transient state phenomena. So far, it has been recognized the most successful approach for the carrier transport simulation in semiconductors.

The commercial simulation tool, MEDICI [18], which solves the coupled the Poisson's equation, continuity equation and energy transport equation, can not simulate the high energy carriers correctly. Therefore, the Monte Carlo method is employed to simulate the program disturb induced by high energy carries in this thesis [19-22].

4.2 Procedure of Monte Carlo Device Simulation

There are two important components in Monte Carlo simulation, the band structure and the scattering rates. First, under a very high field where impact ionization is an important scattering mechanism, electron energy can be above 2 eV that interband transitions may occur; as illustrated in Fig. 4.1. Therefore, two conduction bands are considered in our Monte Carlo simulation program [23]. Second, the scattering rates are calculated according to the Fermi-Golden rule, and the impact ionization is treated as another scattering mechanism [24]. Band-structure and scattering parameters used in Monte Carlo simulation were calibrated in our previous studies [25, 26].

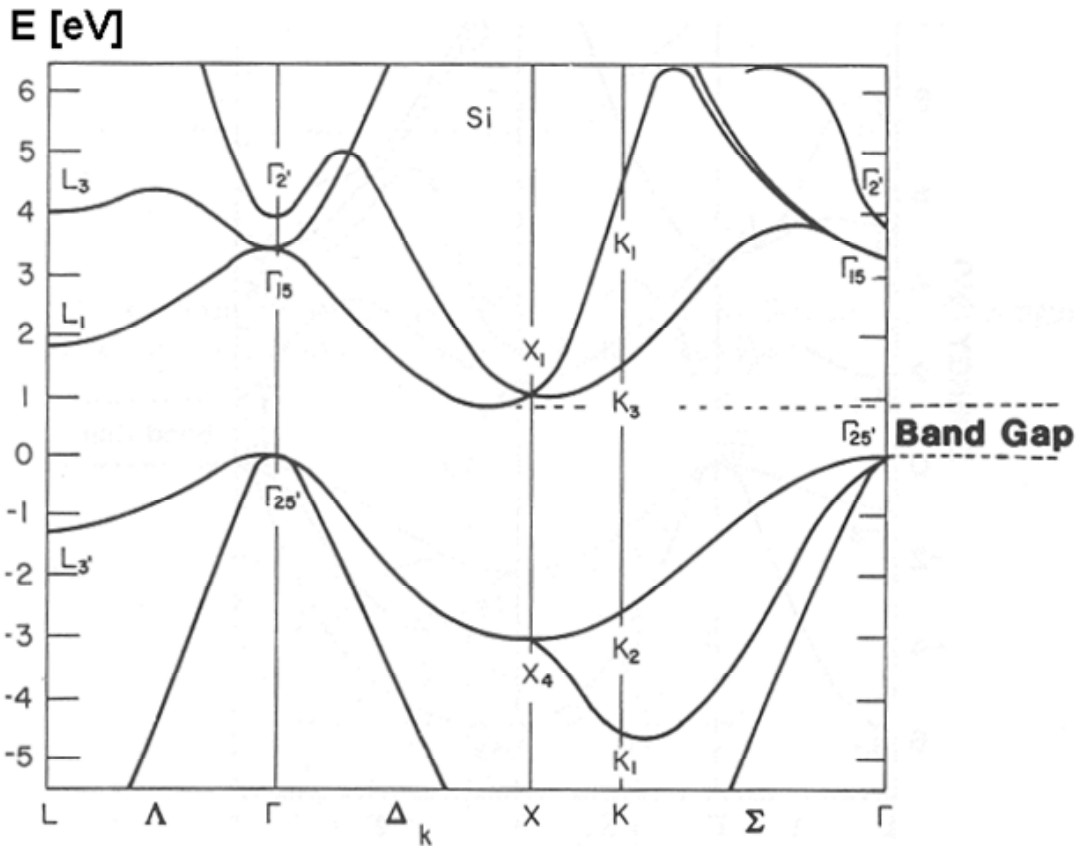


Fig. 4.1 The band structure of silicon.

The basic Monte Carlo flow is shown in Fig. 4.2. To start with, a particle is simulated under an external electric field. It travels freely between two successive scatterings. The free-flight time is determined by using a fixed time technique. During the free flight, the particle is accelerated by the field and its momentum and energy are updated according to the tabular form of the E-k relationship. The new state *k'* of the free flight under the applied field *F* is calculated by the equation below

$$k' = k + \frac{eF}{\hbar}\Delta t \tag{2}$$

Next, whether the scattering events will occur in the end of free flight is determined by a random number between 0 and 1 and the scattering rate at the new energy. If a scattering happens, another random number is generated to decide the responsible scattering mechanism and the new final state is chosen according to the tabular form of the E-k relationship. However, if there is no scattering, the electron goes to the free flight step again. This procedure is continued until the fluctuation due to the statistical uncertainty is less than 1%. This is the basic flow of Monte Carlo simulation.

To extend bulk simulation to device simulation, a buried diffusion bit-line structure is simulated by MEDICI and the electric field distribution is obtained by solving the coupled drift-diffusion and continuity equations. Afterwards, a Monte Carlo window is illustrated, as in Fig. 4.3. All the possible carrier trajectories are included within the simulation window. Some surfaces are treated as reflective boundaries while the others are treated as absorptive ones, depending on realistic physical concepts. Then, a multi-step Monte Carlo simulation similar to [27] (Fig. 4.4) is used to investigate the new program disturb. In the third step where charge injection is taken into account, the tunneling probability is given by using a WKB approximation [28]

$$T(E) = \exp\left\{-\frac{4m^*}{\hbar}\left[\frac{2}{3q|F|}\right]\left[\left(\phi_{\max} - E\right)^{3/2} - \left(\phi_{\min} - E\right)^{3/2}\right]\right\} \tag{3}$$

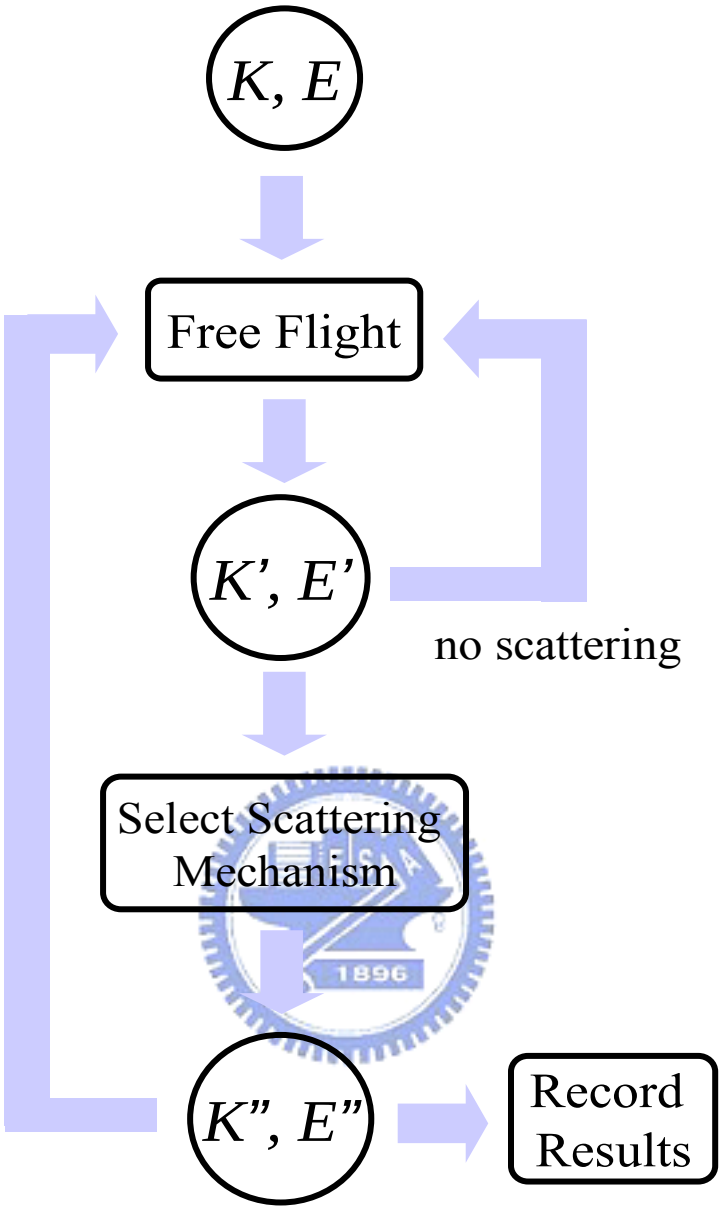


Fig. 4.2 Flow chart of a Monte Carlo simulation.

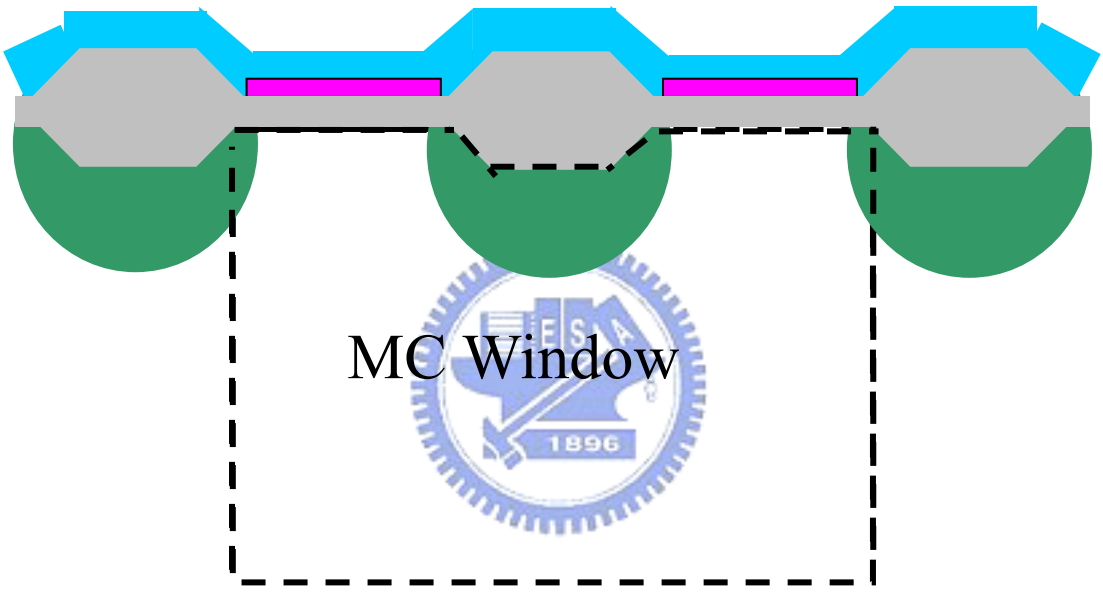


Fig. 4.3 Monte Carlo window in device simulation

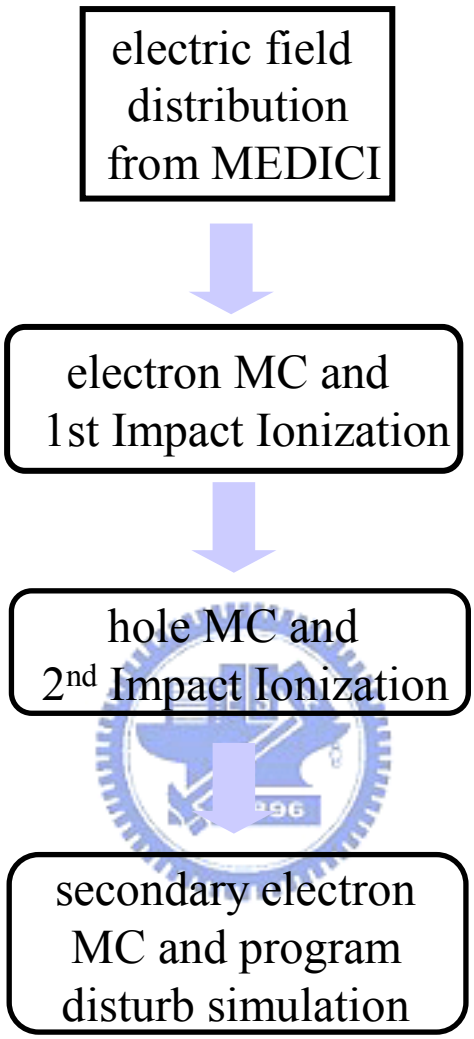


Fig. 4.4 Three-step Monte Carlo simulation flow for the program disturb analysis.

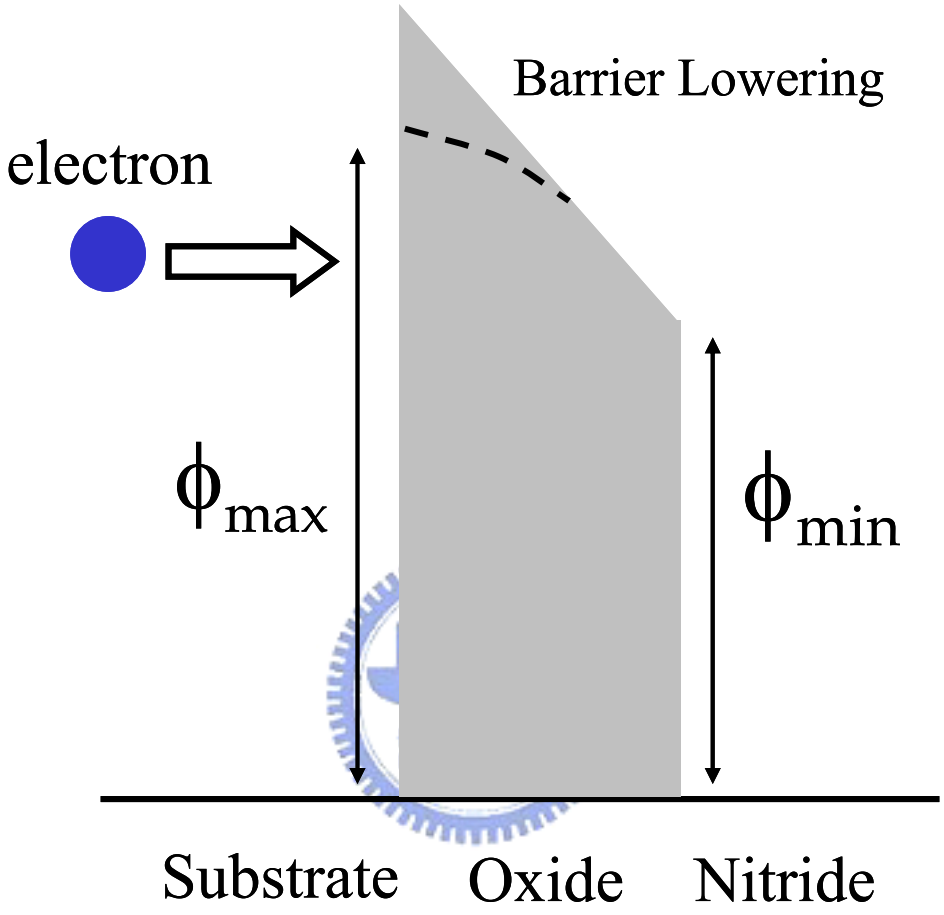


Fig. 4.5 Illustration of barrier lowering for tunneling probability calculation.

where E is electron energy, F is vertical electric field, ϕ_{max} and ϕ_{min} are oxide barriers as illustrated in Fig. 4.5. Furthermore, the oxide barrier height ϕ_{max} is modified by taking into account tunneling and image force [29].

$$\phi_{max} = 3.1V - \alpha E^{2/3} - \beta E^{1/2} \quad (4)$$

where α and β are given coefficients, and E is the perpendicular oxide field.

4.3 Results and Discussions

4.3.1 Analysis of Impact Ionization

The MC simulated distributions of primary and secondary impact ionization (II) events in the programming condition, are plotted in Fig. 4.6(a) and Fig. 4.6(b), respectively. Most of the primary impact ionization events take place in drain junction where lateral electric field is at maximum. However, the distribution of secondary impact ionization events spreads into the substrate [27]. Then, a random sample of secondary electrons with energy above 2.5eV is shown in Fig. 4.7. In Fig. 4.7, it is confirmed that some high energy secondary electrons (2.5eV) may flow to cell 2 and have a chance to inject into the trapping layer and cause a program disturb.

4.3.2 Energy and Space Distributions of Injected Charges

Fig. 4.8 shows the MC simulated energy distributions in cell 1 and cell 2. For energy distribution of bit B, it is a superimposed result of primary and secondary electrons where the high energy hump is dominated by secondary electrons [9]. In cell 2, electrons of entire channel are accumulated. Compared to the bit B, the energy distribution of bit C is dominated by secondary electrons.

The distributions of injected electrons (N_{inj}) along the channel in cell 1 and cell 2 are shown in Fig. 4.9, at a program window of 3V. In cell 1, the injected charges have a very tight

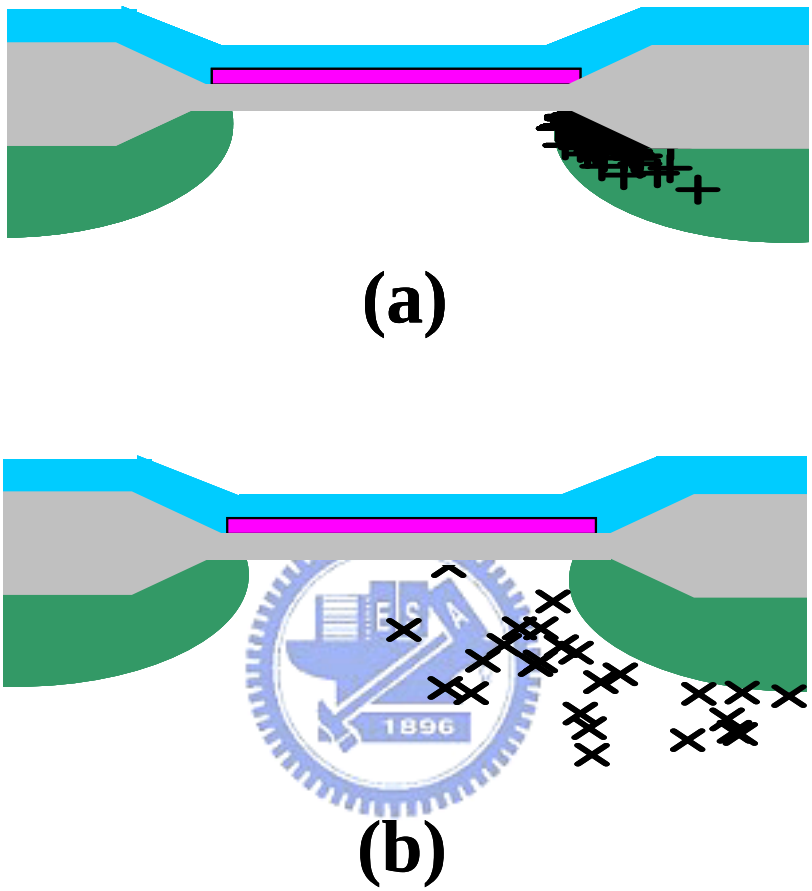


Fig. 4.6 Monte Carlo simulated distribution of primary (a) and secondary (b) impact ionization events.

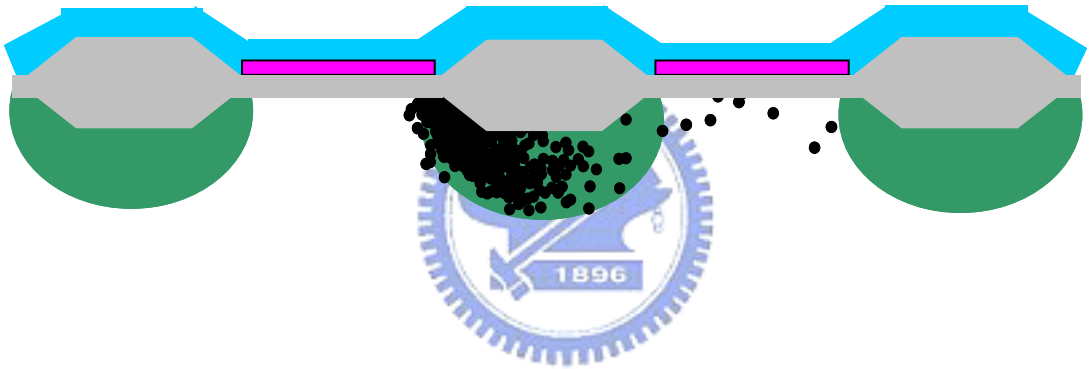


Fig. 4.7 Monte Carlo simulated distribution of secondary electrons whose energy is above 2.5 eV.

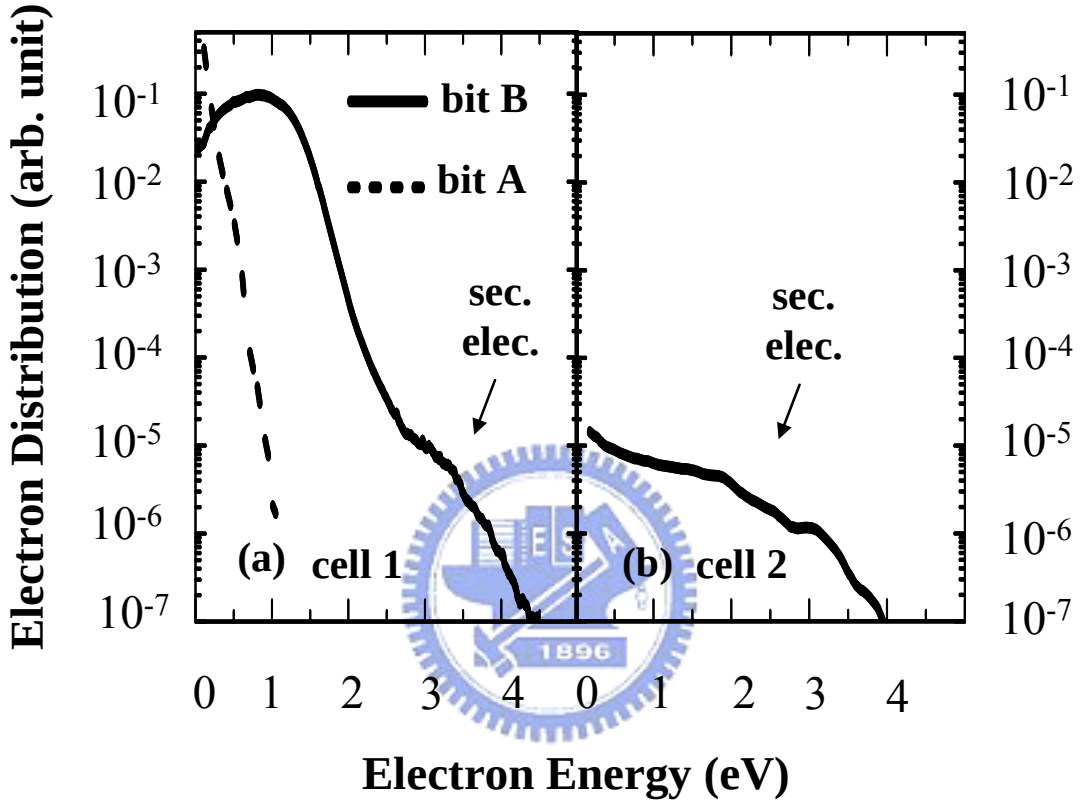


Fig. 4.8 Relative electron energy distributions in cell 1 (a) and cell 2 (b).

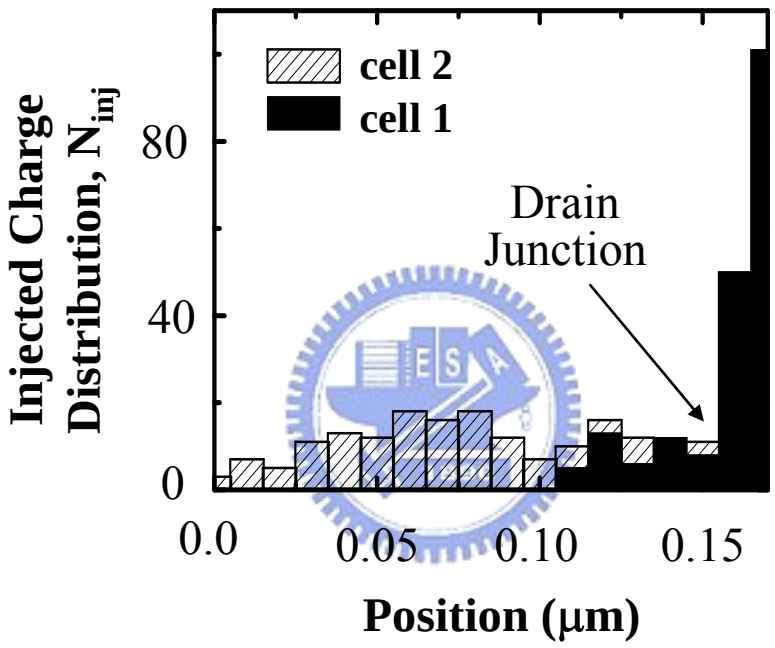


Fig. 4.9 Relative injected charge distribution along channel in cell 1 and cell 2.

distribution near the drain. Unlike cell 1, the injected charges in cell 2 spread over the entire channel that the V_t of bit C and bit D are both affected. In addition, the larger ΔV_t in bit C than in bit D (Fig. 3.5) can be realized due to an asymmetrical injected charge distribution toward bit C.

4.3.3 Relative Charge Injection Rate

The relative charge injection rate in a disturbed bit to a programmed bit is shown in Fig. 4.10. In the beginning of programming, the charge injection rate in cell 2 is negligible compared to cell 1. As program window increases, the charge injection rate in bit B is reduced, due to the programmed charges which raise the effective barrier height and thus slow down the programming. As a consequence, the relative charge injection rate in disturbed bit increases with program window of bit B. A similar trend is also observed in measurement (Fig. 4.10).

4.3.4 Substrate Bias Effect

Then, the substrate bias effect on the program disturb is characterized in Fig. 4.11. A negative substrate bias enhances the program disturb, indicating again that the disturbance is related to substrate impact ionization. In Fig. 4.12, the relative charge injection rates from MC simulation and measurement are shown. The trend matches well. In addition, the MC simulation shows the broader charge distribution in bit B with a negative substrate bias (Fig. 4.13), resulting in an adverse influence on the second bit effect [12].

4.3.5 Scaling Issues

In the last section, some important factors for device scaling are evaluated. First, the dependence of program disturb on bit-line width and depth is shown in Fig. 4.14 and Fig. 4.15, respectively. The MC simulation shows a strong dependence on a bit-line width. The N_{inj} in a

disturbed cell increases by more than 20 times as the bit-line width shrinks from 0.25μm to 0.1μm. A shallower BD junction also aggravates the disturbance. Second, the effect on pocket dosages is compared in Fig. 4.16. It is found that secondary impact ionization region moves deeper into the substrate as the pocket dosage increases, due to a larger electric field. As a result, secondary electrons have a better chance to go around the buried diffusion junction and inject into cell 2, leading to a more serious disturbance.

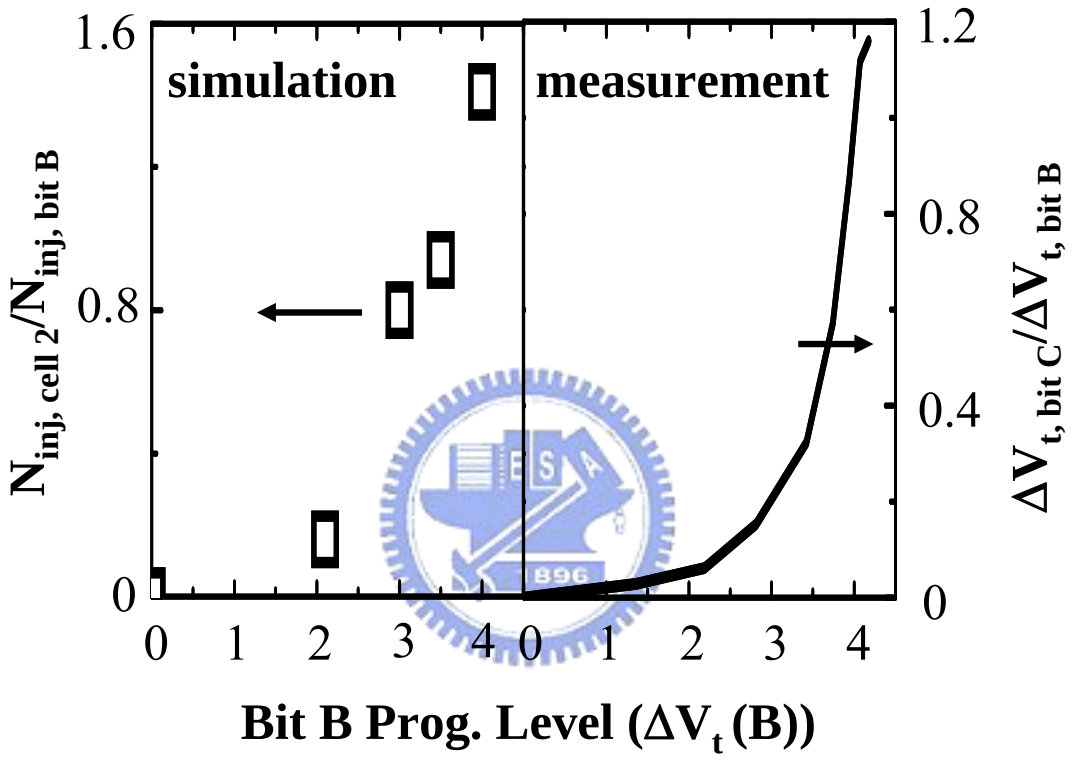


Fig. 4.10 Relative electron injection rates in a disturbed bit from MC simulation (a) and measurement (b).

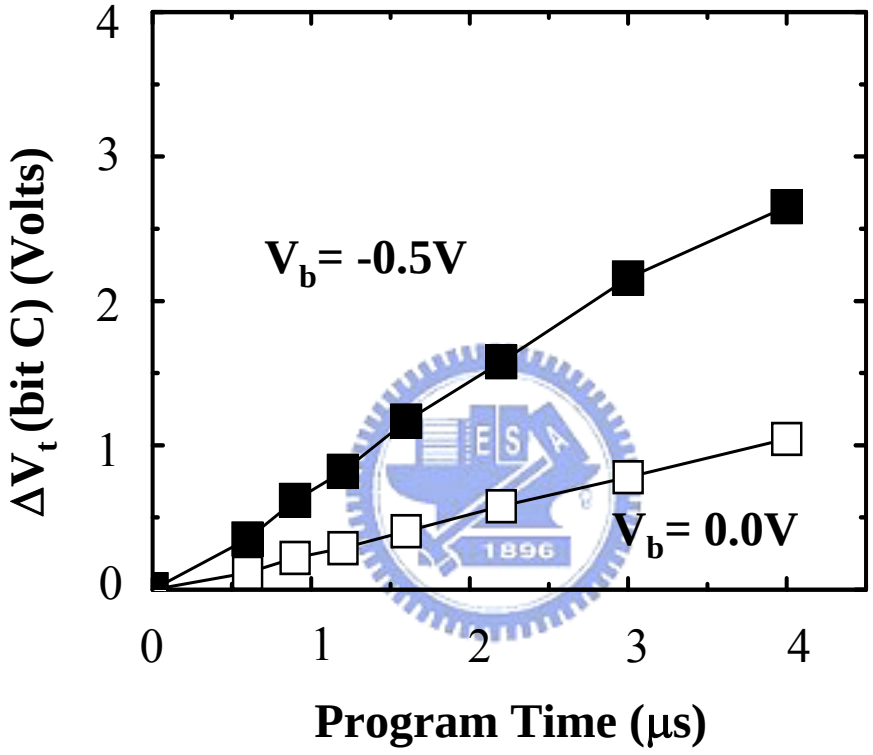


Fig. 4.11 Measured substrate bias effect on the program disturb.

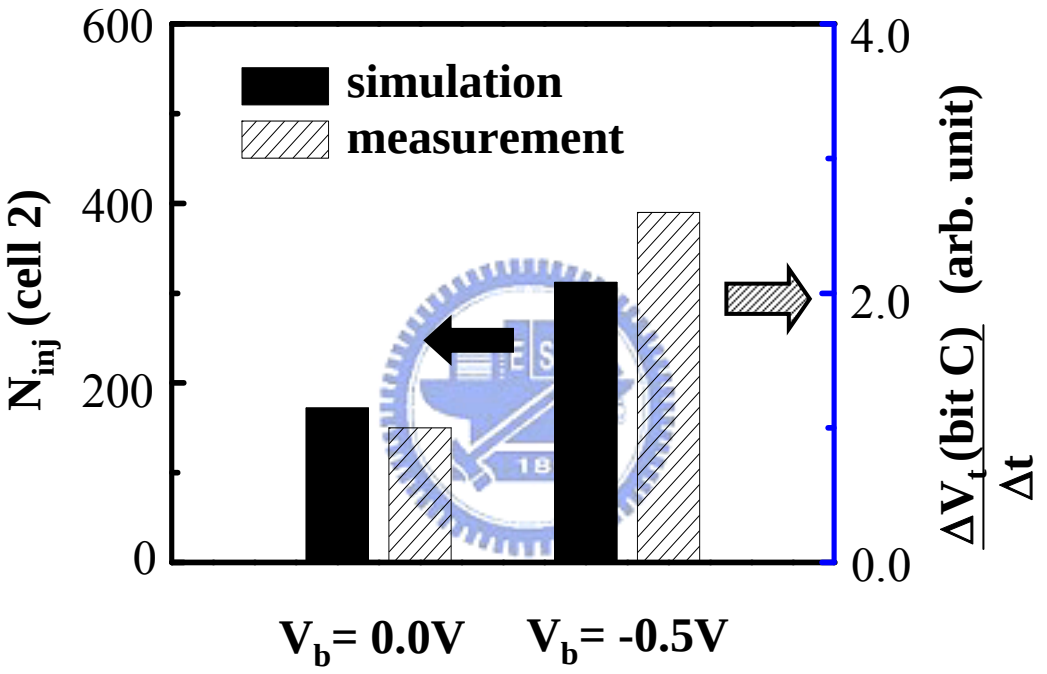


Fig. 4.12 Simulated and measured program disturb rate for different substrate bias.

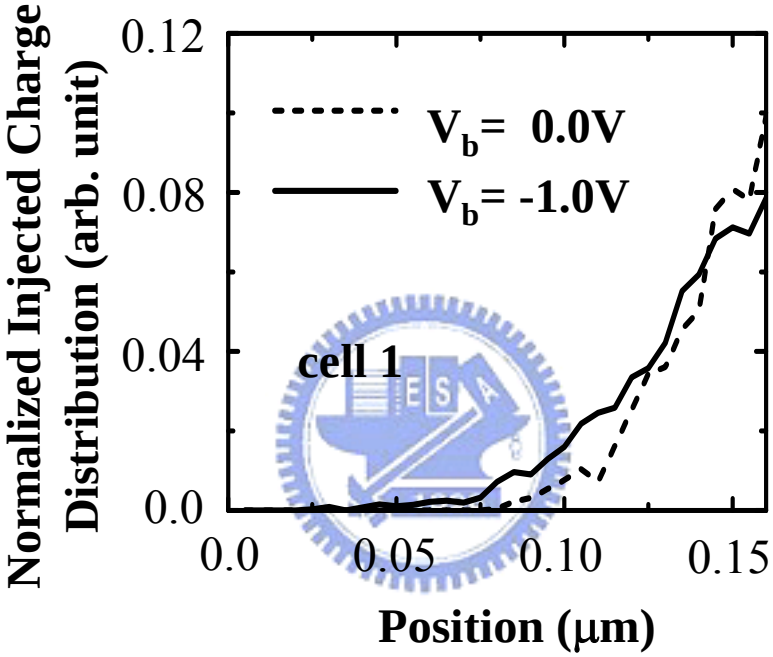


Fig. 4.13 Normalized injected charge distributions in the channel with different substrate bias.

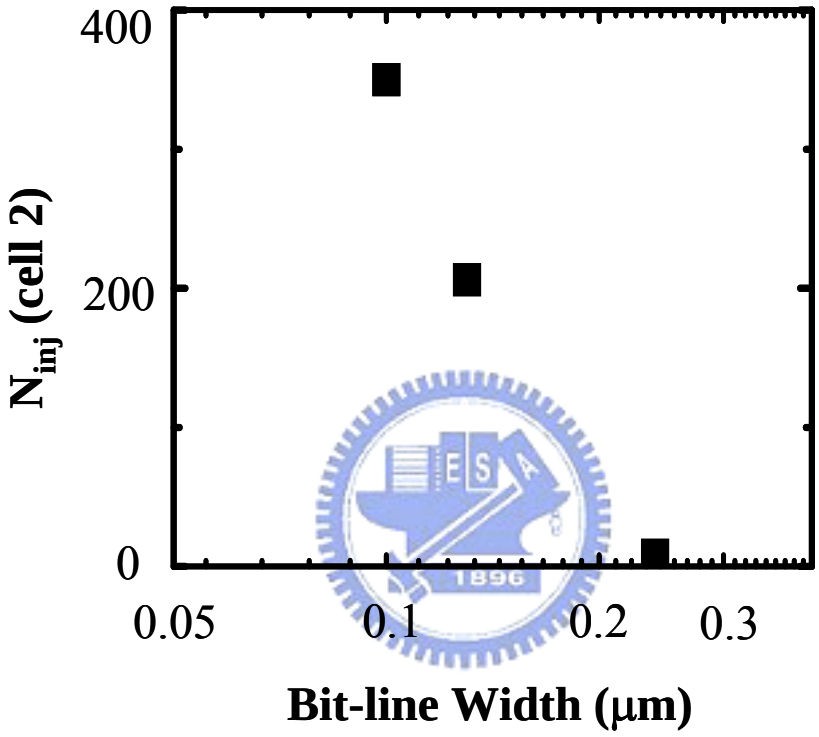


Fig. 4.14 Dependence of program disturb on bit-line width.

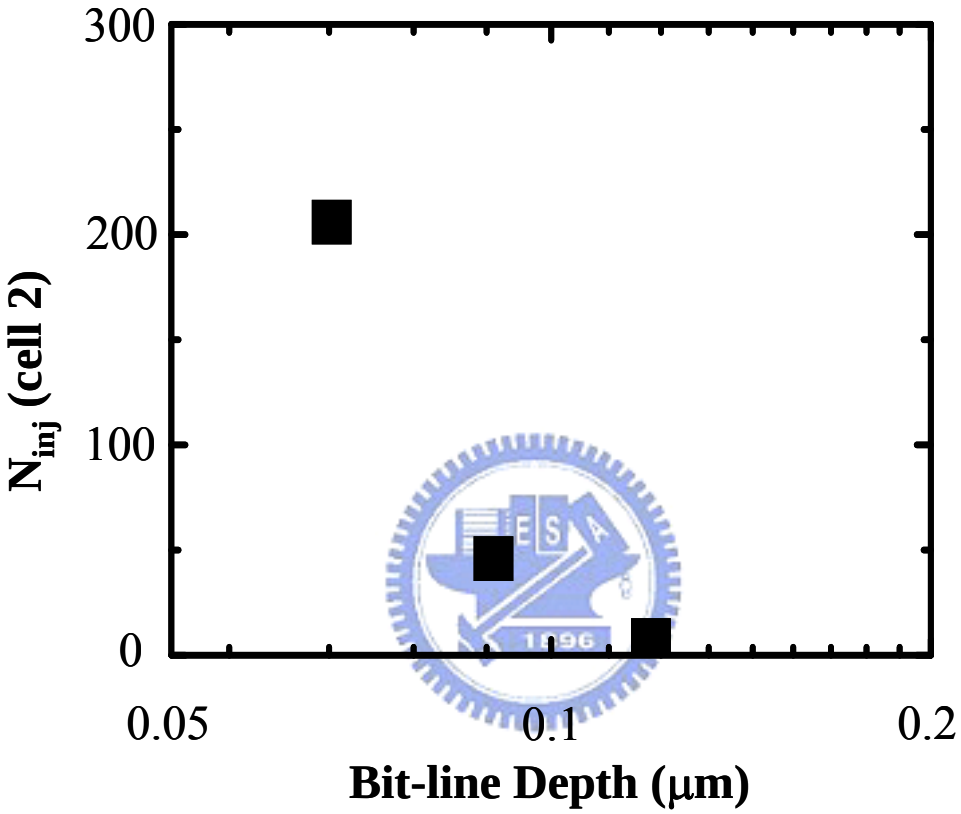


Fig. 4.15 Dependence of program disturb on bit-line junction depth.

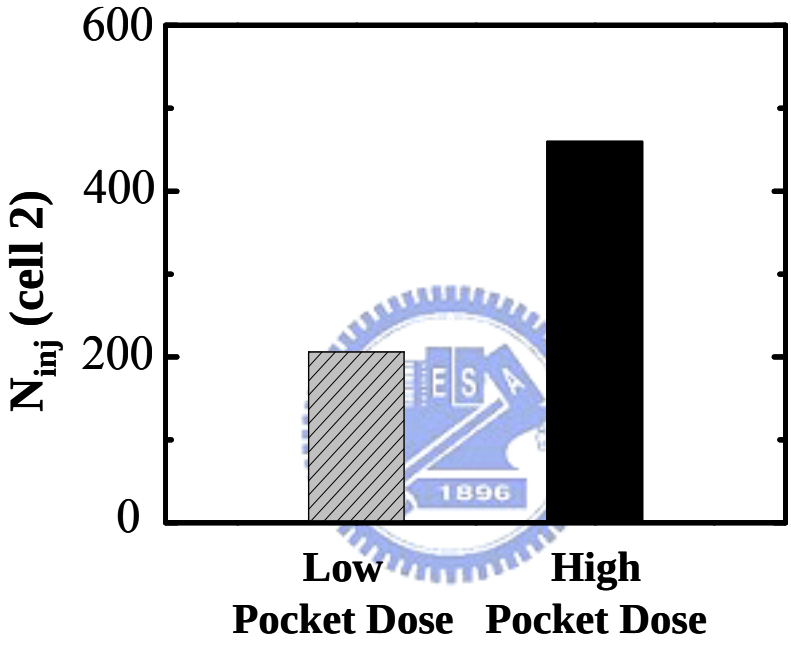


Fig. 4.16 The pocket implant dosage effect on the program disturb. The two dosages differ by two times.

Chapter 5

Conclusions

In this thesis, a multi-step Monte Carlo program is developed to study the new program disturb mode successfully. It is revealed that channel initiated secondary electrons during hot electron programming may flow to a neighboring cell in a buried diffusion bit-line array and cause a program disturb. This disturb mode is more serious as the bit-line width and the junction depth are reduced, and they will become new constraints in bit-line scaling. Optimizations of pocket implant, bit-line geometry and operation condition can help alleviate this new program disturb.

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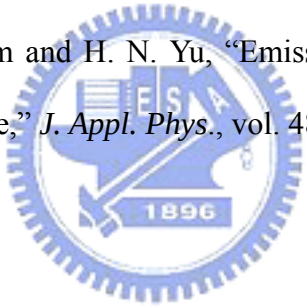

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碩士論文題目：

SONOS 記憶體陣列中因二次熱電子引致寫入干擾之蒙地卡羅分析

Monte Carlo Analysis of Secondary Hot Electrons Induced Program Disturb in SONOS Memory Array