結構化高分子薄膜電晶體之
製程開發與電特性分析之研究

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摘要

近年來，隨著有機半導體材料的開發，利用旋轉塗佈的方式，可以有效降低在塑膠基板表面製作半導體元件的成本。我們選擇聚(3-己基噻吩)作為高分子薄膜電晶體主動層材料，利用氯仿為溶劑，聚(3-己基噻吩)在重量百分濃度為 0.5%，旋轉塗佈速率為 1000 rpm 時，有機薄膜電晶體可擁有最高的開關電流比，移動率亦可達 0.02 $cm^2/V\text{-}s$。我們藉由縮減附著層鉻的厚度亦可降低鉻/聚-(3-己基噻吩)界面的接觸電阻值。除此之外，我們也在沉積有機半導體層之前，於二氧化矽介電層上面進行化學表面處理，使有機半導體能夠在二氧化矽上整齊排列，藉以控制電晶體的特性，增進元件的載子移動率。

理論上，高分子薄膜電晶體的漏電流主要來自兩條路徑，第一條是來自材料本身，另一條則是經由閘極氧化層產生。傳統的高分子有機薄膜電晶體製作，為了簡

化製程，結構上皆使用共閘極以及整面未結構化的主動層，導致漏電途徑大增，也使得電晶體的開關電流比大為下降。因此我們致力於製作結構化高分子聚(3-己基噻吩)薄膜電晶體之元件結構與製程開發，利用微影製程以及乾式蝕刻技術，定義出高分子主動層的區域，並成功製作出高開關電流彼之結構化有機薄膜電晶體。跟未結構化的聚(3-己基噻吩)薄膜電晶體相比，雖然載子移動率衰退約百分之四十，但開關電流比提升了 1000 倍之多，且獲得與一般非晶矽薄膜電晶體相近的次臨界擺幅(~1.5 V/decade)。

另一方面，為了達成在塑膠基板上製作有機薄膜電晶體的目標，我們必須進一步降低整個製程的溫度，因此利用旋佈塗抹方式製作高分子閘極介電層來取代二氧化矽介電層是個非常重要的議題。本論文將對於利用高分子材料作為閘極介電層的有機薄膜電晶體元件製作加以研究探討。要利用高分子作為閘極介電層，必須擁有低製程溫度，強韌的機械性質以及與其他有機材料互相匹配等特性。我們成功製作出可利用旋轉塗抹方式成長且擁有良好絕緣特性的交鏈高分子介電層。利用此交鏈高分子作為閘極介電層來製作為非結構化的高分子有機薄膜電晶體，能夠得到與傳統利用二氧化矽作為介電層之非結構化高分子電晶體相近的電特性，開關電流比達 1.58×10^4，次臨界擺幅甚至達到與結構化有機薄膜電晶體相近的水準(~1.66 V/decade)。

Study on the Process Development and Electrical Characterization of the Patterned Polymer Thin-Film Transistors

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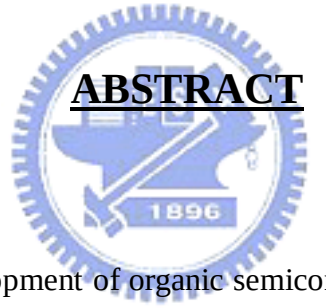

ABSTRACT

Recently, with the development of organic semiconductor materials, the devices can be fabricated easily on the plastic substrates by spin coating process with extremely low temperature and production costs. In this work, we chose poly(3-hexylthiophene) or called P3HT as the active layer of polymer TFTs (P-TFTs). At a 0.5 wt% P3HT in chloroform with spin-coating rate of 1000 rpm, we demonstrated that both high field-effect mobility (up to 0.02 cm^2/V-s), and high I_{ON}/I_{OFF} ratios (~10^4) could be achieved. We found that reducing the thickness of the adhesion layer, Cr, can decrease the contact resistance. Besides, the characteristics of polymer thin-film transistors can also be enhanced by chemically modifying the surface of the gate dielectric prior to the

deposition of the organic semiconductor because of better arrangement of the polymer films when they was spun-coating on the gate dielectric.

In principle, there are two primary leakage paths of P-TFTs; one is the conductive bulk of P3HT, and the other is through the gate insulator. Conventional P-TFTs share a common gate, in which case the leakage through the gate dielectric is much more significant. Therefore, we had efforts on defining the active layer via the photolithographic technique for improving device performances. We successfully proposed a patterned P3HT thin-film transistor. Although there was 40% degradation in mobility as compared with those non-patterned P-TFTs, however, the I_{ON}/I_{OFF} ratio of the patterned devices was significantly improved by over three orders of magnitude and even the subthreshold swing was compatible with the amorphous Si TFTs (~1.5 V/decade).

On the other hand, in order to make the P-TFTs on the plastic substrate, we had to further lower the process temperature. Therefore, using spin-coatable polymer gate dielectric instead of SiO_2 one was also a very important issue. In this thesis, we still discussed the process development and electrical characterization of P-TFTs with polymer gate dielectric. The quest for high-performance polymer gate dielectrics is of intense current interest. Beyond having excellent insulating properties, such materials must meet other stringent requirements for optimum P-TFT function: efficient low-temperature solution fabrication, mechanical flexibility, and compatibility with

diverse gate materials and organic semiconductors. We reported the realization of spin-coatable and cross-linked polymer blends exhibiting excellent insulating properties. Moreover, the non-patterned P-TFTs with cross-linked polymer as the gate dielectric in this work performed a high I_{ON}/I_{OFF} ratio (1.58×10^4), which was similar to the conventional P-TFTs with a thermal oxide as the gate dielectric. Furthermore, the subthreshold swing was even as good as the patterned P-TFTs (~1.66 V/decade).

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畢業，是另一段旅程的開始，希望大家在未來都可以發揮所長，一路順風。

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