Chapter 1
Introduction

1.1 Overview of Organic Thin-Film Transistors

Organic semiconductors, as we know, have huge potential to create some revolutionary products and applications in our daily life. However, due to their poor performance, organic devices could not compete with inorganic ones until new structures and materials were adopted in resent years. Light-emitting diodes [1.2], solar cells [3], and thin film transistors [4-6] using organic semiconductor have been reported and there are also many new organic-electronics products in the market. Nowadays, organic electronics is not only the research in the labs but also in use in our life.

Inorganic semiconductors such as silicon, germanium and gallium arsenide have been used for centuries. However, the electronic devices based on these materials usually need complex processing steps by costly production facilities. In recent years, organic thin film transistors (OTFTs) have attracted much attention because most organic semiconductor materials can be easily deposited by spin coating at room temperature with low costs. Because of these unique processing characteristics, they can be quite suitable for novel thin-film transistor applications or disposable electronics on flexible substrates requiring large area coverage, structural flexibility and low temperature

processing. It has been proved to be used for some low end electronics such as chemical vapor sensors [7], smart card, and radio-frequency identification (RFID) tags. Additionally, prototypes of all-polymer integrated circuits have also been demonstrated. [8]

Integration of organic TFTs with AMOLED has a great potential to make the dream of fully-organic flexible display with totally roll-to-roll technology come true. For this purpose, more understanding about the electrical properties and reliability behaviors of organic devices is necessary.

1.2 Solution-Processed Organic Semiconductor Films

There are two methods have been usually used to fabricate organic TFT devices. The first method involves the use of a soluble material, either a conjugated polymer such as poly(3-alkylthiophene) (P3AT) [9] or precursor materials that can undergo subsequent chemical reactions to give the desired compounds, such as pentacene and poly(thienylene vinylene) [10-11]. In this method, low field effect mobility has been reported due to poor ordering and the amorphous nature of the semiconductor thin films. The second one involves the use of vacuum deposition system to form the films of oligomers and organic materials with low molecular weights. Mobility of higher than 0.01 cm^2/V s can be obtained with materials such as oligothiophenes,[12-15] copper phthalocyanine,[16] bis(benzodithiophene)[17], and pentacene[18.19], which are with highly ordered and

self-assembled films. It is clear that good ordering is necessary to achieve better transistor performance.

However, the technology that is believed to have the potential to produce the highest impact on manufacturing costs is the use of soluble organic semiconductors, both polymers and oligomers, combined with large area spin-coating or printing techniques that could eliminate lithography. For this reason, we choose P3HT as the semiconducting layer material in our research because P3HT has many merits to act as the semiconducting layer in thin film transistors: (1) P3HT could be solution processed by spin coating. (2) The addition of alkyl side-chains of P3HT enhanced the solubility of the polymer chains [20], so that we can use different solvent such as toluene, xylene, and chloroform to fabricate our device. (3) P3HT is a well-known polymer as an organic semiconductor and has shown the field-effect mobility from 10^{-4} cm^2/Vs in 1988 to 0.2 cm^2/Vs in 2003 [21-23].

1.3 Introduction to Poly-3-hexylthiophene, P3HT

The chemical structure of the P3HT had been shown in Fig.1-1. In this figure, R stands for the alkyl side chain (C_6H_{13} for P3HT), which allows P3HT to be dissolved in many kinds of solvents such as chloroform. The 3-alkyl substituents can be incorporated into a polymer chain with two different regioregularities: head to tail (HT) and head to

head (HH) [24]. If the P3HT consists of both HH and HT 3-hexylthiophenes in a random pattern, we call it a regiorandom P3HT. In contrast, a regioregular P3HT has only one kind of 3-hexylthiophene backbone, either HH or HT-P3HT.

A regioregular P3HT, with a higher ordering, can be obtained higher mobility than regiorandom one. More interestingly, P3HT with regioregular molecular structure exhibit very different properties from their regiorandom counterpart including a better ordering, smaller band-gap, superior crystallinity in solid states and substantially improved electroconductivities

1.4 Motivation

Although significant progress has been made to improve the performance of solution-deposited small molecules, semiconducting polymers offer significant advantages in terms of solution rheology and mechanical properties. The polymers, however, currently have lower performance than a-Si, limiting their applications. Due to this reason, we need to optimize the parameters of bottom gate/bottom contact P3HT-TFTs including coating speed, S/D contact metal, and modification layer at the beginning of our research to enhance the mobility of our devices.

We all know that the degree of mobility is superiorly limited by the active-layer material so that the two major issues of structural polymer thin-film transistors (P-TFTs) is to enhance the on/off ratio & switching speeds. Therefore, we need to fabricate

patterned P3HT-TFTs to suppress leakage current and reduce subthreshold swing.

Besides, another vital key of P-TFT is that we have to make the devices compatible with plastic substrate to realize the flexible electronics so that we should apply organic dielectrics which could lower the process temperature to make sure that the P-TFTs can be fabricated on plastic substrate.

1.5 Organization of This Thesis

In chapter 1, described background and motivation of our research.

In chapter 2, showed experimental procedures to fabricate several kinds of structures of polymer TFTs (P-TFTs) with one of the most commonly used polymer material, ex. poly(3-hexylthiophene); the structures included non-patterned P-TFTs, patterned active region P-TFTs, and patterned both gate and active layer P-TFT. Besides, we did some researches with cross-linked PVP as organic dielectrics in order to realize a full-organic TFT.

In chapter 3, proposed the experimental results and discussed the correlates explanations and some issues of P-TFTs which were described above.

In chapter 4, we made the summary and conclusions to this thesis.

Chapter 2
Experimental Procedures

2.1 Introduction

There are many parameters will impact the performance of P-TFTs. In this chapter, we will discuss each part of P-TFTs and try to optimize the process parameters.

We need to consider about the structure of P-TFTs and optimize the spin-on conditions for P3HT include the concentration of P3HT solution, spin-coating rate and thermal curing time etc. Source/drain metals for ohmic contact with P3HT are also an important issue in our devices due to the contact resistance between the source/drain electrodes and the semiconductor becomes increasingly important to device performance as the channel length decreases. Pt is a well know material applied in P3HT TFTs as the contact material because it is pretty stable in the air and its work function is also match with P3HT. Therefore, we just change the material of adhesion layer and adjust its thickness to examine its effect to the contact resistance and the ON current.

Oxide surfaces treated with some modification chemicals is also a significant step to improve the adhesion between the organic semiconductor and oxide surface. The modification of the substrate surface prior to the deposition of regioregular P3HT has also been found to influence the film morphology so that we use different kinds of surface treatments to investigate their effect.

2.2 Device Fabrication of Non-Patterned Polymer Thin-Film Transistors

2.2.1 Device Structure

P3HT TFTs are usually fabricated in either the coplanar or staggered geometry, with bottom gate. The staggered geometry, as shown in Fig.2-1, so-called top contact device, is generally less susceptible to high contact resistance than the coplanar one (bottom contact device), because of the larger effective contact area. However, there might be some physical damage when using sputtering system to deposit metal contacts, or even some metal–semiconductor reactions to influence the contact resistance. The coplanar structure, as shown in Fig.2-2, is desirable for its ease of fabrication and compatible with conventional lithography technique.

Due to the reason mentioned above, we fabricated our devices with the coplanar structure. The schematic diagram of non-patterned P-TFT is shown in Fig 2-3. First, a thermal oxide layer with a thickness of 1200 nm was grown in a furnace on an N++ type low-resistance wafer which acts as a common gate electrode. Afterwards, source/drain regions were defined using the photolithography process. The finger type for source/drain electrode was shown in Fig.2-4. Finger geometry for the source/drain contacts is to minimize the TFT device area and the associated gate to source/drain leakage current. Finally, the device is finisfed after spinning-coating the P3HT for the active layer.

2.2.2 Process Flow of Non-Patterned P-TFTs

1. Initial RCA cleaning
2. 120 nm field-oxide layer: furnace wet oxidation at 980 ^{o}C
3. Mask #1: Source/Drain electrodes definition
4. Ti or Cr / Pt = 5 nm / 50 nm as the adhesion/electrode layer: Sputter system at base pressure = 2×10^{-6} torr; metals were deposited continuously without breaking vacuum
5. P. R. lift-off in ACE with ultrasonic agitation and then the residual Pt metals form the source/drain electrodes.
6. ACE + IPA cleaning
7. Surface modification layer deposition
8. Spin-on P3HT: 0.5 wt% P3HT in chloroform, 500 ~ 2000 rpm for 40 seconds, and then baking in a vacuum chamber under 120^{o}C for 45 minutes.

The descriptions above are shown in Fig.2-5.

2.2.3 Bi-Layer Electrode

Materials and structures of the source/drain electrodes both affect the contact characteristics between the source/drain electrode and the organic semiconductor. Unlike the FET of single-crystalline silicon, polycrystalline silicon, or hydrogenated amorphous silicon, the P3HT material cannot be optimized easily by semiconductor doping or silicide formation. Such properties of organic semiconductors deteriorate the performance of devices; moreover, the chemical compound always increase the contact

resistance between the source/drain electrode and the organic semiconductor [25],[26]. It is a straightforward method to find a suitable electrode material which forms ohmic contact with the organic active layer and thus to improve the performance of OTFTs. Pt is a well know material applied in OTFTs as the contact material. It is stable and the work function is match with P3HT, however, Pt is hard to deposit on SiO_2 so that we needed to add an adhesion layer between Pt and SiO_2 – Cr layer or Ti layer because these two kinds of metal are not only noted for good adhesion to SiO_2 but have similar work function.

2.2.4 Modification of Oxide Surface

The self-assembled monolayer (SAM) modification of a SiO_2 gate dielectric surface improved the molecular ordering of semiconducting layer in P-TFTs, leading to a significant improvement in transistor performance. Similarly, the mobility of P3HT TFTs has also been reported to improve by orders of magnitude upon modification of the SiO_2 gate dielectric substrate by hydrophobic SAM, possibly through lowering of the surface energy of the gate dielectric and removal of residual surface water and other polar groups prior to deposition of the polymer[27], or by inducing microstructural changes through specific interactions with functional groups of the polymer[28]. Molecular ordering in semiconductors can be manipulated to varying degrees through controlled solvent evaporation[29], postdeposition annealing[30], and substrate surface chemistry[31–34]. For example, modification of the gate dielectric surface with HMDS, as shown in Fig.2-6(a), led to improved P3HT-TFT

performance[35]. Similarly, a significantly higher mobility of F8T2-TFTs was obtained using a dielectric surface modified with octadecyltrichlorosilane (OTs), as shown in Fig.2-6(b)[36]. Because of these reasons, in our research, we discuss several condition of different modification layers as below: 1. none (O_2 plasma treatment); 2. HMDS layer; 3. O_2 plasma treatment+ OTs layer; 4. HMDS layer + OTs layer. There are HMDS layer on oxide surface after S/D deposition due to the process of lithography in NCTU NFC so the purpose of O_2 plasma treatment is to destroy the HMDS layer and remove other chemicals on the oxide surface.

The detail experimental method was described below: HMDS molecules were chemically bonded with the hydroxyl groups on the oxide surface in a high temperature (150^{o}C) and low pressure (lower than 20 torr) oven which was full of HMDS steam. In order to remove the HMDS from the process of lithography, we employed O_2 plasma for ten minutes to make the surface of SiO_2 clean and without any organic chemicals. To grow OTs modification layer, we put the sample and 1 ml OTs liquid in a negative-pressure box in R.T for 45 mins and then baking in vacuum chamber (100^{o}C for 30mins).

2.3 Device Fabrication of Patterned Polymer Thin-Film Transistors

2.3.1 Introduction

How to pattern the organic semiconductor active layer in organic devices is a

really critical issue. It is required in applications such as color or backlit polymer/organic light emitting diode displays[37] [38]. Patterning the active layer is required in order to reduce leakage currents, crosstalk between individual devices, unwanted parasitic capacitance, and to increase the much-needed operational speed. As a result, the devices have better performance characteristics (I_{ON}/I_{OFF} ratio, for instance). Patterning is even more important when P-TFTs share a common gate, in which case the leakage through the gate dielectric is significant [39].

Several methods of patterning small molecules can be found in the literature, ex, deposition through a shadow mask[40], integrated shadow mask[41], or patterned growth[42]. However, these kinds of convenience methods could not be applied to P-TFTs because we usually use the spin-coating technique to deposit the active layer of P-TFT instead of vacuum deposition which was compatible with the patterned technology through shadow mask. Therefore, one of the most common methods for patterning P-TFT consists of either a water-soluble resist or a protective parylene layer followed by a regular photoresist on top of the polymer, which is acted as an etch mask. Subsequently the polymer layer is etched by oxygen plasma. [43] [44]

In this thesis, we clarify a photolithographic patterning process for P3HT TFTs. The process described in this thesis could apply to other organic semiconductors as well (F8T2, PQT-12, for example). One of the handicaps of this process is the observed degradation of the transistor performance. Recent reports show a mobility of 6.1×10^{-3} $cm^2/V\ s$ and 10^{-5} $cm^2/V\ s$ for photolithographically patterned pentacene and

P3HT OTFTs, respectively [45][46]. Considering a typical mobility of 0.1 cm^2/V s and 0.01 cm^2/V s for unpatterned pentacene and P3HT, respectively [47–50], there is more than two orders of magnitude performance degradation after patterning. Therefore, we focus on not only how to develop a process that is compatible with inexpensive plastic substrates but the electrical characteristic enhancement of P3HT-TFT devices such as mobility, I_{ON}/I_{OFF} ratio, and switching speeds etc.

One of the most vital parts of this kind of patterned method is the passivation layer which is use to protect the active layer. We employ cross linked PVP as the passivation layer to prevent the damage from coming process. (ex: PR spin-coating, HDP-RIE) because it is not only insoluble in common solvents but with a pretty good mechanical strength and flexibility to act as a great passivation layer.

2.2.2 Process Flow of P-TFTs with Non-Patterned Gate and Patterned Active Region

1. Initial RCA cleaning
2. 120 nm field-oxide layer: furnace wet oxidation at 980 ^oC
3. Mask #1: Source/Drain electrodes definition
4. Cr / Pt = 3~8 nm / 50 nm as the adhesion/electrode layer: Sputter system at base pressure = 2×10^{-6} torr; metals were deposited continuously without breaking vacuum
5. P. R. lift-off in ACE with ultrasonic agitation and then the residual Pt metal

forms the source/drain electrodes.

6. ACE + IPA cleaning
7. HMDS layer growth
8. Spin-on P3HT: 0.5 wt. % P3HT in chloroform, 1000 rpm for 40 seconds, and then baking in a vacuum chamber under 120^{o}C for 45 minutes.
9. Spin-on passivation layer (PVP liquid : 2.67 wt% PVP, 1.33 wt% PMF, 0.8 wt% PAG in three kinds of solvent: PGMEA, BuOH, and IPA), 1500 rpm for 30 seconds, exposing under 365nm UV light for 1 minute and then baking in a vacuum chamber under 120^{o}C for 10 minutes to make PVP cross linked.
10. Spin-on thick PR (AZ-4620) and patterned the active region as a hard mask.
11. HDP-RIE in an O_2 plasma etcher for the dry etching of PR, PVP and P3HT.

The descriptions above are shown in Fig.2-7.

2.2.3 Process Flow of P-TFTs with Patterned Gate and Patterned Active Region

1. Si-Wafer with 400nm thermal oxide as buffer oxide
2. Using E-gun system to deposit Cr gate for 100nm. (use the lift-off technique to pattern)
3. Depositing 120nm PECVD oxide.
4. Cr / Pt = 3 nm / 50 nm as the adhesion/electrode layer: Sputter system at base pressure = 2×10^{-6} torr; metals were deposited continuously without breaking

vacuum

5. P. R. lift-off in ACE with ultrasonic agitation and then the residual Pt metal forms the source/drain electrodes.
6. ACE + IPA cleaning
7. HMDS layer growth
8. Spin-on P3HT: 0.5 wt. % P3HT in chloroform, 1000 rpm for 40 seconds, and then baking in a vacuum chamber under 120^{o}C for 45 minutes.
9. Spin-on passivation layer (PVP liquid : 2.67 wt% PVP, 1.33wt% PMF, 0.8wt% PAG in BuOH), 1500 rpm for 30 seconds, exposing under 365nm UV light for 1 minute and then baking in a vacuum chamber under 120^{o}C for 10 minutes to make PVP cross linked.
10. Spin-on thick PR (AZ-4620) and patterned the active region as a mask.
11. HDP-RIE in an O_2 plasma etcher for the dry etching of PR, PVP and P3HT.

The schematic diagram of patterned gate and patterned active region P-TFTs is shown in Fig.2-8.

2.4 Polymer Thin-Film Transistors using Organic Dielectric

2.4.1 Introduction

The dielectric systems discussed above have all been part of bottom gate devices. The deposition of inorganic dielectrics would be difficult on top of the organic active

layer. The surface treatments employed on inorganics would be practically impossible to use in top gate devices. Organic dielectrics, however, offer the freedom to build both top and bottom gate devices more easily by the use of solution coating techniques and printing.

Solution-processable materials are very attractive for applications in electronics, in part because films exhibiting good characteristics can often formed simply by spin-coating, printing, or casting at room temperature under ambient conditions. Of course, gate dielectrics are not an exception. Furthermore, this capability has practical merits when coupled with low-cost patterning techniques for dielectric and for other materials needed for TFT fabrication. From this point of view, polymer dielectrics really have great potential.

However polymer TFTs in which both the semiconductor and the insulator are polymers have shown limited success in contrast. An inherent problem in the fabrication of these polymer TFTs is that the polymer semiconductor layer on an insulating layer can get damaged when the other layer is spin-coated onto the existing, underlying layer for the fabrication of the transistor.

2.4.2 Cross-Linked PVP Gate Dielectrics

Poly(4-vinylphenol) (PVP), as shown in Fig.2-9, is one of the most popular gate materials. OTFTs with PVP gate dielectric and opaque noble-metal S/D contacts showed a pretty good performance. However, the organic dielectric capacities of the

polymer gate dielectric are still inferior to those of inorganic dielectric materials. Moreover, sensitivity to gate bias stress in OTFTs with the polymer dielectric, resulting in threshold voltage shift depending on the direction of gate voltage sweeping, has been often found and reported[51]. Cross-linked PVP is that PVP blends with some cross-linking agent and then treat with UV light or thermal curing to make PVP cross-linked. Cross-linked PVP is insoluble in common solvents, and it could be patterned using standard microelectronic etching methodologies, moreover, it has a pretty good mechanical strength and flexibility so that it is one of the prospective materials as gate dielectric. Few studies reported the reasons of the threshold voltage shift and the unreliable behavior of P-TFTs with organic dielectrics [52]. Hence, no report has mentioned about optimum PVP curing conditions for crosslinking of polymer chains, which may substantially influence the electrical properties of polymer gate dielectric films and further influence the reliability of the OTFTs with polymer gates

2.4.3 Process Flow of P-TFT with Cross-Linked PVP as Gate Dielectric.

Cross-linked PVP films were prepared from a solution of 8 wt% poly-4-vinylphenol, 4 wt% poly(melamineco-formaldehyde) (PMF, as shown in Fig.2-10), and 0,0.1, 0.5, 2.4 wt% photo acid (PAG, as shown in Fig.2-11) in propylene glycol monomethyl ether acetate (PGMEA), deposited by spin coating, and then curing in vacuum chamber, (120^{o}C,30 minutes) followed by exposing under 365nm UV light

for 1 minute to make PVP cross linked, as shown in Fig.2-12.(If we did not add PAG in the solution, we needed to make PVP cross-linked at 200 ^{o}C for 30 minutes)

The process in detail is described as below:

1. Initial RCA cleaning
2. Spin–coating PVP solution (1000 rpm for 40 seconds) on Si-wafer
3. Thermal curing in vacuum chamber, (120^{o}C for 30mins) followed by exposing unde 365nm UV light for 1 minute to make PVP cross linked
4. OTs layer growth
5. Mask #1: Source/Drain electrodes definition (abridge the step of HMDS deposition)
6. Cr / Pt = 3 nm / 50 nm as the adhesion/electrode layer: Sputter system at base pressure = 2×10^{-6} torr; metals were deposited continuously without breaking vacuum
7. P. R. lift-off in ACE with ultrasonic agitation and then the residual Pt metal forms the source/drain electrodes.
8. ACE + IPA cleaning
9. Spin-on P3HT: 0.5 wt. % P3HT in chloroform, 1000 rpm for 40 seconds, and then baking in a vacuum chamber under 120^{o}C for 45 minutes.

Chapter 3
Process Development and Electrical Characterization of the P-TFTs

3.1 Electrical Characteristics of P-TFTs

3.1.1 Measurement

Current-voltage characteristics of P-TFTs were measured in atmospheric pressure with a semiconductor parameter analyzer HP4156C. All measurements were carried out in an electrically shielded box. The drain-source current, I_{DS}, was measured as a function of the drain-source voltage, V_{DS}, to observe FET-like characteristics. I_{DS} was also measured as a function of the gate voltage at V_{DS} = -40V, which was constructed to determine the gate bias modulation of the TFT conductive channel. Four primary parameters were extracted from the experimental I-V curves: (1) the transistor threshold voltage (V_{th}), (2) ON/OFF current ratio, (3) the field effect mobility (μ) (4) subthreshold swing (SS). The detailed extraction method will be discussed in the following section.

3.1.2 Extractions of Mobility and Threshold Voltage

Mobility is an important parameter for carrier transport because it describes how

strongly the motion of an electron or hole is influenced by an applied electric field. P3HT-TFTs are adequately modeled by standard field-effect transistor equations and the P3HT used in the present devices behaved as a p-type semiconductor. When the gate electrode is biased negatively with respect to the source electrode (ground), P3HT-TFTs operate in the accumulation mode and the accumulated charges are holes. Mobility could be extracted from the maximum transconductance (g_m) at V_D = -40V in our experiment

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=const} = \frac{WC_i}{L} mV_D \qquad \text{(equation 3-1)}$$

where L is the channel length, W is the channel width, C_i is the capacitance per unit area of the insulating layer, and μ is the field effect mobility.

. The threshold voltage of an organic thin film transistor is also a very vital device parameter, since it is directly related to the power supply requirements. The interface between the dielectric and organic-semiconductor strongly affects the transistor I-V characteristics. The density of charges trapped in the bulk and at the interface, as well as the mobile and fixed charges in the dielectric directly affects the threshold voltage. For a given dielectric thickness, the presence of higher charge results in a higher threshold voltage because the charge carriers get trapped and larger voltage is required to invert the semiconductor surface. Threshold voltage V_t can be extracted from the following equation

$$I_D^{1/2} = \sqrt{\frac{1}{2} m C_i \frac{W}{L}} (V_G - V_t) \qquad \text{(equation 3-2)}$$

Use linear fitting of the plot $I_D^{1/2}$ vs. V_G in saturation region to abtain the slope and the horizontal axis intercept at point A, which was the extracted threshold voltage (V_t = V_G at $I_D^{1/2}$ =0)

3.2 Non-Patterned P-TFTs

3.2.1 Material Purification

Poly(3-hexylthiophene) (regioregular, >98.5% head-to-tail) was purchased from Aldrich company. The P3HT had a wide range of molecular weight, so we needed to purify it and make separation with different Mw molecules so that we can collect the higher Mw molecule together and it might result in the performance enhancement of our devices. The polymer was separated into narrow molecular weight fractions with the method similar to the paper of Trzandel et al[53]. The illustration of Soxhlet extraction for purification of P3HT was shown in Fig.3-1. Put the P3HT in the filter glass and the solvent in the extraction pot, by means of the different solubility with different molecular weight of P3HT in the solvent, we can make molecule with unfamiliar molecular weight separated to reach the purpose of purification. The as-received material was subjected to a series of Soxhlet extractions with hexane and dichloromethane. In the end we used chloroform to extract the P3HT we wanted. The

Soxhlet apparatus was kept under a nitrogen purge to avoid unintentional doping of P3HT. Each solvent was refluxed until the filtrate was colorless (~12 h). The collected fractions were concentrated by rotor evaporation and then dried until reaching constant mass.

The results of the separation of Aldrich P3HT into narrow molecular weight fractions are shown in Table.3-1. The starting material from Aldrich had a large polydispersity distribution as can be seen from the GPC results.

We use P3HT both before purification and after purification to be active layers in our devices. The I_D-V_G curves of these transistors were shown in Fig.3-2. Both transistors are fabricated under the parameter as below: 0.5% weight percentages of P3HT in chloroform, and spin-coating 1000 rpm for 40 seconds. We found that the mobility was eight times and the on/off ratio was forty times enhancement because the lower molecular weight had been wiped out to make the P3HT purer so that the electrical characteristic of our P-TFT had been improved.

3.2.2 Effects of Films Thickness

In this section, we prepared 0.5 wt% of P3HT in chloroform. And then the P3HT solution was filtered by a 0.2-μm pore-size PTFE filter and then spun onto the wafer surface with different coating rate: 250, 500, 1000, 2000rpm. Next, we investigated the electrical characteristics of P3HT-TFTs, such as mobility, threshold voltage,

subthreshold swing and on/off ratio, with different spin-coating rate of P3HT layer.

3.2.2.1 Physical Properties of Spin-On P3HT Film

We employed scanning electron microscope to observe the thickness of deposited P3HT film. Fig.3-3 exhibits the thickness of the deposited P3HT in chloroform film with different coating rates: 250, 500, 1000, 2000rpm. We found that the faster of coating rate, the thinner the films deposited.

3.2.2.2 The Bulk Current Effect of P3HT Film

There are two current paths in organic semiconductor layer [54]. One is the channel current (I_{ch}), it comes from source electrode (Pt) and goes through the accumulation holes and into drain electrode (Pt). Using established metal-oxide-field effect transistor (MOSFET) current-voltage relationships, the channel current can be written as:

$$I_{ch} = \frac{W}{L} mC_i (V_G - V_{th} - V_D/2) V_D \qquad \text{as } V_D << V_G - V_{th} \qquad \text{(equation 3-3)}$$

for the linear regime, where L is the channel length, W is the channel width, Ci is the capacitance per unit area of the insulating layer, V_{th} is the threshold voltage, and μ is the field effect mobility. Another leakage path is the bulk current (I_{bk}). It comes from source electrode (Pt) and goes through conductive layer which is above the accumulation holes and into drain electrode. The bulk current (I_{bk}) can be represented as

$$I_{bk} = m \times \frac{W}{L} \times l \times V_{DS} \qquad \text{(equation 3-4)}$$

where l is the organic semiconductor layer thickness [54].

The I_D-V_G curves of these transistors with different coating rate were shown in Fig.3-4. We found that the devices which were fabricated by coating rate of 250, 500 rpm can not be turned off. It can be shown that the current is the bulk current from the aspects of that as the organic semiconductor layer thickness increases, the drain current increases. These conclusions are consistent with Equation 3-4.

It is believed that the conducting channel in P-TFTs is confined to a few monolayers at the organic dielectric interface[55]. Studies on pentacene-based devices show 0.9 and 2–3 nm accumulation layers depending on the dielectric and the applied gate bias[56][57]. Even though working P-TFTs have been made with a monolayer of P3HT, the semiconductor layer in most P-TFTs has a thickness ranging from a few tens of nanometers to hundreds of nanometers which is much lager than the accumulation layer thickness [58]. In Fig.3-4, we observed that the on current decreased obviously when the spin-coating rate was up to 2000 rpm. We suggested that the P3HT solution evaporated so soon under this condition that the P3HT film could not be formed with a good order. It resulted in a lower driving current and lower mobility.

In this work, P3HT-TFTs with film thickness of 59–164 nm were made. The

mobility and on/off ratio up to 0.02 cm^2 /V s and 8 x 10^4, respectively, have been obtained, which are similar to best P3HT-TFTs reported in the literature. The effects of P3HT film thickness on the electrical properties of P3HT-TFTs were studied. The drain current and the mobility increase with thickness. The results provide useful information and guidelines for circuit design of organic devices for different application requirements.

3.2.3 Effects of Surface Treatments

The P3HT (regioregular, >98.5% head-to-tail) used in coming chapter and section was purchased from Reike Metal company. The steps of purification were the same as we described above.

The characteristics of polymer thin-film transistors can be controlled by chemically modifying the surface of the gate dielectric prior to the deposition of the organic semiconductor. The chemical treatment consists of derivatizing the silicon oxide surface with organic trichlorosilanes to form self-assembled monolayers (SAMs).

In this section, we will discuss several condition of different modification layers as below: 1. none of SAMs (O_2 plasma treatment); 2. HMDS layer; 3. O_2 plasma treatment before OTs was deposited; 4. HMDS layer deposition before OTs was deposited.

Fig.3-5 showed that the I_D-V_G curves of P3HT-TFT with different modification

layer. We found that if we treated the surface with O_2 plasma, V_{th} shifted to positive apparently. We thought that if we did with O_2 plasma treatment, P3HT not only arranged well on the channel region but on the top of source and drain, leading to larger leakage current from the bulk. In order to get lower leakage current, we only treated with HMDS to improve adhesion and regioregularity between the polymer chain and the oxide surface[59]. After treating SiO_2 surface with HMDS, the hydroxyl groups at the oxide surface would be replaced by methyl groups and the apolar nature of these groups apparently attract the hexyl side chains of P3HT, favoring lamellae with an edge-on orientation.

The OTs molecules with long alkane chains as the modification layer provided the highest driving current[60], which allowed them to interact with similar features in the structure of P3HT via induceddipole dispersion forces. The alkane chains in OTS extend perpendicularly to the SiO_2 surface. The mobility increases clearly on the devices with OTs layer; either O_2 plasma treatment or HMDS layer deposition before OTs layer was deposited. The effect of dielectric surface treatment on carrier mobility in the polymer is still not well understood. Replacing siloxyl groups on the SiO_2 surface with methyl groups by treating the dielectric with HMDS or OTs might lead to a mobility increase in P3HT. The increase was attributed to the presence of apolar groups at the surface leading to phase segregation of the polymer at the interface [61].

This mechanism is not consistent with the mobility increase observed on OTS-treated surfaces. If the mobility depended only on the presence of methyl groups on the surface, the devices fabricated on the HMDS-treated surface would have characteristics comparable to those fabricated on the OTs-treated surface.

However, there must be HMDS layer on oxide surface after S/D deposition due to the process of lithography in NCTU NFC so the OTs layer had to be deposited after O_2 plasma treatment to destroy the HMDS layer. This process causes higher leakage current and also suppresses the on/off ratio. If we deposit OTs layer on HMDS layer, the I_D-V_G curves showed two steps of increasing current because of the different modification layer on the oxide surface.

3.2.3.1 Electrical Stability of P3HT-TFTs with Different Modification Layers

As shown in Fig.3-6, a negative V_{th} shift was observed after a constant gate bias stress of -40 V, especially on the devices with O_2 plasma treatment. Several mechanisms are responsible for the above observation. One is the charge trapping/relaxing near the semiconductor-insulator interface, mobile ions/trap-states in the gate dielectric, or polarization effect. It was also reported that the electro-negativity of the molecule's functional group, such as self-assembly monolayer at the interface, influences the charge distribution within the organic active

layer and can lead to the formation of an electric dipole[62]. The devices with O_2 plasma treatment created more defects on the surface of dielectric and this is why a larger negative V_{th} shift be observed.

The other is that when the gate electrode was applied a constant negative bias, the dipoles from the polar part of P3HT molecules would rearrange and induce a polarization electric field as shown in Fig.3-7. The polarization electric field enhances the free holes to be depleted, and thus the device is easily turned off and the threshold voltage would decrease as we observed in the experiments.

3.2.4 Adhesion Layer

Pt is a well know material applied in OTFTs as the contact material. It is stable and the work function is match with P3HT, however, Pt is hard to deposit on SiO_2 so that we needed to add an adhesion layer between Pt and SiO_2 – Cr layer or Ti layer because these two kinds of metal are not only noted for good adhesion to SiO_2 but have similar work function.

Fig.3-8 and Fig.3-9 showed the I_D - V_G and I_D -V_D curves of P-TFT with different adhesion layers. We found the curves are very similar to each other. Due to this, we think the thin Ti & Cr (5nm) both acts as good adhesion layers.

3.3 Patterned P-TFTs

3.3.1 Subthreshold Slope and On/Off Current Ratio

Subthreshold slope is also important characteristics for device application. To take advantage of a large on/off current ratio it is necessary to swing the TFT gate bias over small range. But the TFTs don't turn off abruptly at the threshold voltage as the saturation current equation would suggest. Instead there is a subthreshold region where the drain current varies approximately exponentially with gate voltage. For single crystal silicon TFTs the subthreshold region is well-behaved and ideally the subthreshold slope comes from the exponential activation of current with voltage compared to the thermal voltage; at room temperature this gives a subthreshold slope for drain current of about 60 mV/decade. Due to tail and midgap states, a-Si TFTs have a larger subthreshold slope, typically 0.3-1.5 V/decade. The subthreshold slope for the P3HT TFTs discussed is about 8-10 V/decade. This is a significant problem since to achieve a low off current it is necessary to swing the TFT gate voltage a large range. We must reduce the subthreshold slope to improve the TFTs performance. The subthreshold slope of transistors can be defined by the equation:

$$SS = \frac{\partial V_G}{\partial(\log I_D)}\Big|_{V_D=\text{comstant}} \quad \text{, when } V_G > V_t \text{ for p-type.}$$

If we want to have the TFTs with good performance, a small subthreshold slope of transistors is indeed.

For active matrix liquid crystal displays (AMLCD's) application, TFTs must have a sufficiently large on current to charge the pixel capacitance during a line access time and a sufficiently low off current that the charge remains stable during the much longer frame time so that the high on/off current ratio is really a vital target to the P-TFTs.

Amorphous Si TFTs have excellent on/off current ratio, typically near 10^8, and this is one of the reasons they have found wide application in AMLCD's. The on/off current ratio is more strongly affected by film purity effects. Using commercially available P3HT we had been able to achieve TFT mobility greater than 0.01 cm^2/V-s, however the on/off current ratio is typically only 10^3-10^4. It is really a fatal problem for P3HT-TFTs because if we want to apply P-TFT as a simple switch, on/off ratio higher than 10^4 is necessary at least. In this study, we will try to solve this problem by patterning the polymer active layer and will be shown in coming section.

3.3.2 Contact Resistance

Because of the driving current after patterning the active region layer would decrease apparently, contact resistance effect might be observed easily. We had to do some research to investigate the effect of the thickness of the adhesion layer.

We adjusted three kinds of thickness of adhesion layer in this experiment including 3nm, 5nm, and 8nm. The I_D -V_D curves are shown in Fig.3-10. We found that thicker

adhesion layer (~8nm) results in linear current increment at low V_D contract to the thinner adhesion layer (3~5nm) which displays a traditional curves. The accumulation region formed a low resistance channel and current will flow through this path, the current flow path is shown in Fig.3-11. This might suggest that the conducting channel in a P3HT layer should be 5 to 8 nm thick.

3.3.3 P-TFTs with Non-Patterned Gate and Patterned Active Layer

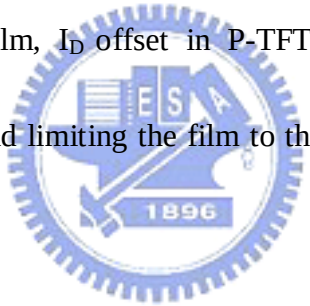
3.3.3.1 Gate Induced Leakage in the Polymer Thin-Film Transistors

Fig.3-12 (a) shows the I_D–V_D characteristics of our standard P3HT device. The P3HT film is approximately 70 nm thick and was not patterned for these devices. The distortion of the I–V curves in the linear region because of the I_D offset can be clearly seen. The gate induced leakage (i.e. the gate current) (I_G) increases with gate bias and is much higher at lower V_{DS} and peaks at V_{DS} = 0 V (Fig. 3-12(b)). These kinds of P-TFTs share a common gate and a common active layer so that there were many current paths from drain to gate and result in large gate leakage current.

The I_D -V_D curve of patterned active layer P-TFT was shown in Fig.3-12(c)(d). The electrical characteristics of the patterned P3HT device represented in the Figure show a P-TFT with low gate induced leakage current. While the I_D offset is reduced

significantly, the drive current for the transistor is comparable to the non-patterned devices.

In this section, we studied the I_D offset in P-TFTs with a bottom contact configuration. I_D offset is closely related to gate leakage and can be used to monitor the leakage of OTFTs. I_D offset changes with film thickness and doping density of P3HT films. Thicker films and higher doping densities result in higher I_D offset. We suggest that the major source of I_D offset is the effective expansion of drain/source electrodes from the conducting accumulation layer when unpatterned P-TFTs are on. By patterning the P3HT film, I_D offset in P-TFTs can be reduced significantly. Patterning the P3HT film and limiting the film to the channel area eliminates a large source of I_D offset.



3.3.3.2 Cross-Linked PVP as the Passivation Layer with Different Solvents

The I_D-V_G curves of patterned P-TFT using PVP solution as the passivation layer with different solvent was shown in Fig.3-13. BuOH as solvent exhibits the best characteristic among these three solvent apparently. Using BuOH has much better coverage than using PGMEA and smoother film than using IPA as solvent. When doing the experiment of using PGMEA as solvent, we found that it was hard to spin the

solution on the P3HT film because the polarity of these two material was repulsive; obviously, it lost its function as passivation layer and only few devices were protected during PR coating and dry etching. The film of PVP solution with IPA as solvent after coating on P3HT, we found a pretty rough surface, might result in unbalanced energy when proceeding dry etching which leading to damage of the devices. Fig. 3.14 to Fig. 3.16 shows the SEM graphs of P-TFTs with patterned P3HT. From these graph, we found that the position of channel is so far away from the edge of the residual polymer (P3HT, PVP and thick PR) so we could be sure that the active region was well protected by the passivation layer and avoided the plasma damage from the process of HDP-RIE.

Fig. 3-17 shows the transfer characteristics of two P-TFTs, one without and the other with the patterned P3HT. Non-patterned the P3HT film, the on/off ratio and SS of the device was about 10^3 and 4.5 V/decade. After patterning the active region, the on/off ratio was dramatically improved from 10^3 to about 10^6 and SS also drops to 1.3 V/decade because of the reduction of the P3HT film coverage, which was confined only between the source and drain electrodes. The mobility of patterned P-TFT was slightly decrease from 0.0022 to 0.0013 (cm2/V-s) compared with non-patterned one. The characteristic of these two P-TFTs was listed in Table 3-2.

3.3.4 P-TFTs with Patterned Gate and Patterned Active Layer

The OM graph, I_D - V_G curve, and I_D -V_D curve of Patterned Gate & Patterned Active Layer P-TFTs were shown in Fig.3-18~Fig.3-20. We found that all electrical characteristics were degraded compared to the non-patterned gate with patterned active layer one. The possible reason was that there was very rough surface (Fig.2-8) before P3HT coating, leading to the fact that the P3HT could not arrange well on the surface. The surface morphology of the P-TFTs with patterned-gate and patterned-P3HT before active layer deposition is different to others, so we have to do more study about spin-coating rate of P3HT for optimizing the film condition. However, this patterned device still has the on/off ratio more than 10^4 and small SS as 2.25 V/decade. The I_D-V_G curves of non-patterned and patterned P-TFTs with PECVD oxide was shown in Fig.3-21

We note that previous non-patterned P3HT-TFTs that were fabricated and measured in air generally showed low on/off ratio. Doping in ambient environments was often regarded as a key reason. Our results suggest that the main cause could actually be the high gate-leakage current if the device was not patterned. By using proper photolithography to define the P3HT channel, we show that high-performance P-TFTs can be fabricated and measured in ambient conditions owning to the

cross-linked PVP as passivation layer.

The characteristic and the OM graphs of these three kinds of P-TFTs were listed in Table.3-3.

3.4 Organic Dielectric for P-TFTs

3.4.1 Material Analysis

3.4.1.1 Scanning Electron Microscope (SEM) Analyses

Fig.3-22 exhibits the thickness of the deposited cross-linked PVP film with different weight percentage of PAG: 0, 0.1, 0.5, 2.4 wt%. We found that the more PAG, the thicker films which were deposited and might result in lower leakage current.

3.4.1.2 Atomic Force Microscope (AFM) Analyses

Fig.3-23 is the AFM graph of the deposited cross-linked PVP film with different weight percentage of PAG: 0, 0.1, 0.5, 2.4 wt%. It is obviously to be observed that only the material without PAG but curing at higher temperature caused a rougher film and the roughness of other weight percentage of PAG are almost the same. We could conclude that the factor to affect the roughness is curing temperature but not the weight percentage of PAG

3.3.2 Device Characterization

We found that PR can adhere well on cross-linked PVP with OTs layer as adhesion layer, but not on SiO_2 so that we can use the OTs as modification layer instead of HMDS to fabricate a higher mobility device without O_2 plasma treatment. The I_D- V_G curve of the P-TFT using Cross-Linked PVP as dielectric was shown in Fig.3-24. The mobility of P-TFT using Cross-Linked PVP as dielectric was up to 0.005 cm^2/V-s, which is four times higher than SiO_2-HMDS-P3HT TFTs. Beside, low SS (1.66 V/decade) and high on/off ratio (1.58×10^4) are almost compatible with patterned P-TFT.

These films are readily deposited from solution, adhere strongly to a variety of rigid and flexible conducting substrates, can be patterned, and are compatible with a broad range of organic semiconductors.

Chapter 4
Summary and Conclusions

Material is still the most vital factor to the polymer TFTs. The same materials from different companies resulted in different performances although we treated them with a totally the same method.

It had been proven that the purification technique has been proven to make molecules with different Mw separated so that we could collect the higher Mw molecule together and improve device performance.

Modification layer really plays a vital role in P-TFTs device. HMDS is the most suitable material for our processes; OTs can increase the driving current and enhance the mobility of P-TFTs; O_2 plasma treatment will lead the device to a serious degradation under stressing.

After optimizing the parameters of P3HT-TFTs, we demonstrated that both high field-effect mobility (0.02 cm^2/V-s) and high on/off current ratios (greater than 10^4) could be achieved. We found that the film quality and field-effect mobility were strongly dependent on the spin coating rate and self assembly monolayers (SAMs). In addition, reducing the thickness of the adhesion layer, Cr, can decrease the contact resistance.

We successfully proposed a patterning process with P3HT as the organic

semiconductor. In this process, cross-linked PVP was used as a passivation layer. We patterned the active region after spinning-coating the thick photo-resist to be etching block and then unwanted PVP/P3HT was etched using O_2 plasma reactive ion etching (RIE). There was 40% degradation in mobility as compared with P-TFTs whose P3HT channels are not patterned; however, the on/off ratio of the patterned devices is improved from about 10^3 to 10^6, because of the dramatically reduction of leakage current.

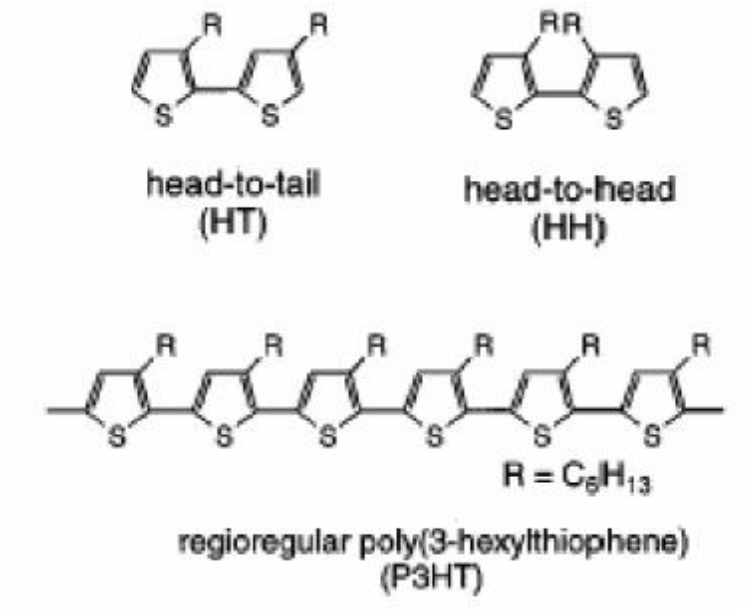
The surface morphology of P-TFTs with patterned gate and patterned active layer is rougher and different to the others, so we still have to optimize the spin-coating rate of P3HT for better film condition.

A direct method to pattern P3HT has been demonstrated using standard high-throughput photolithography technique with high yield. The method could be applied generally to both small molecules and conducting polymer materials. This technique can be extended to use the optical phase-shifting masks to manufacture the structures down to 100 nm in dimension, which may significantly increase the speed of plastic electronic devices and circuits into the MHz range, which is crucial in practical applications.

We also had presented a cross-linked hygroscopic insulator P-TFTs with a performance, when operated in air, superior to the traditional organic devices in terms of higher mobility (0.005 cm^2/V-s), low SS (1.66 V/decade) and high on/off ratio (1.58×10^4).

Also, using cross-linked technique with PAG for the fabrication of organic dielectric could not only lower the process temperature as low as 120^{o}C but also achieve the full-organic TFTs. These cross-linked hygroscopic insulators were readily deposited from the solution with strong adhesion to a variety of rigid and flexible conducting substrates, and compatible with a broad range of organic semiconductors.

Figures



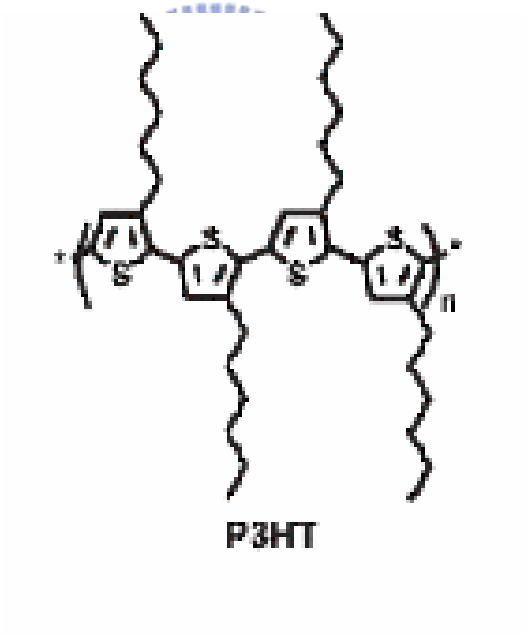


Fig. 1-1 chemical structure of P3HT

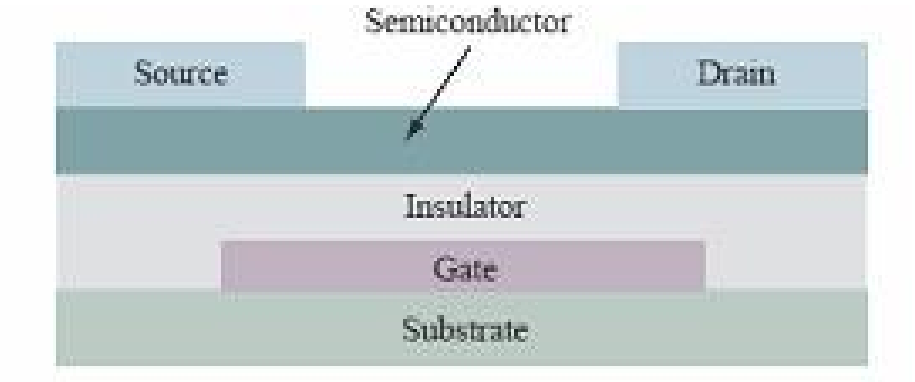


Fig.2-1 structure of bottom gate/top contact P-TFTs

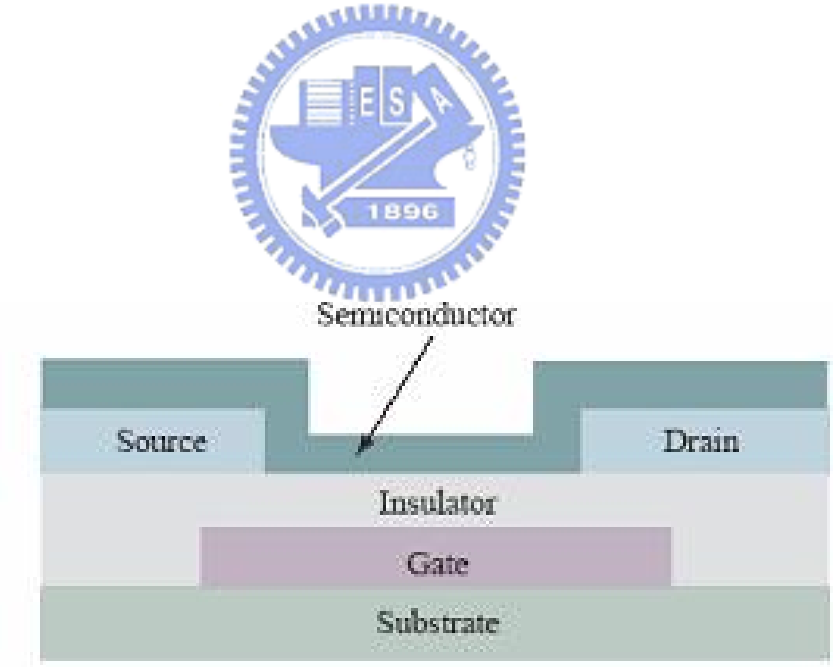


Fig. 2-2 structure of bottom gate/bottom contact P-TFTs

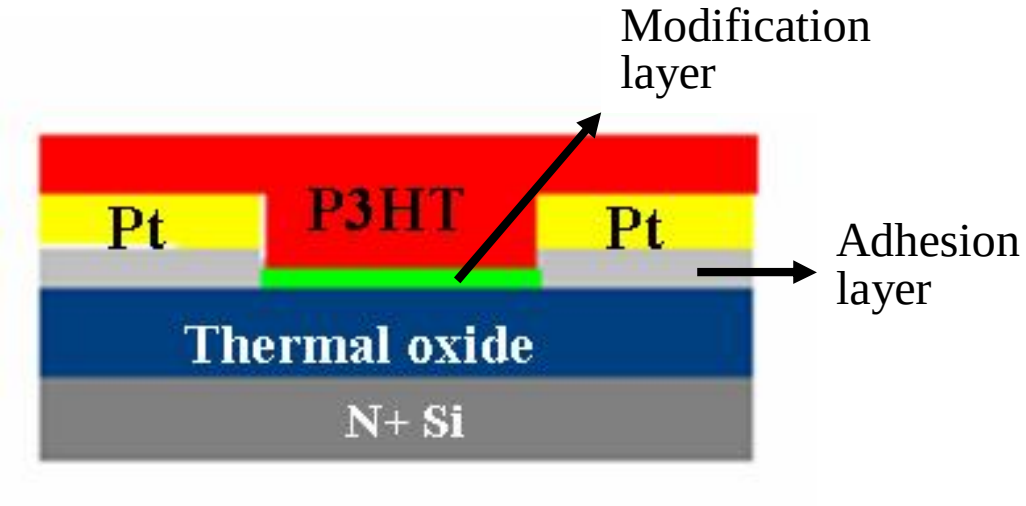


Fig.2-3 the schematic diagram of non-patterned P-TFT

Fig.2-4 the comb structures for source/drain electrodes

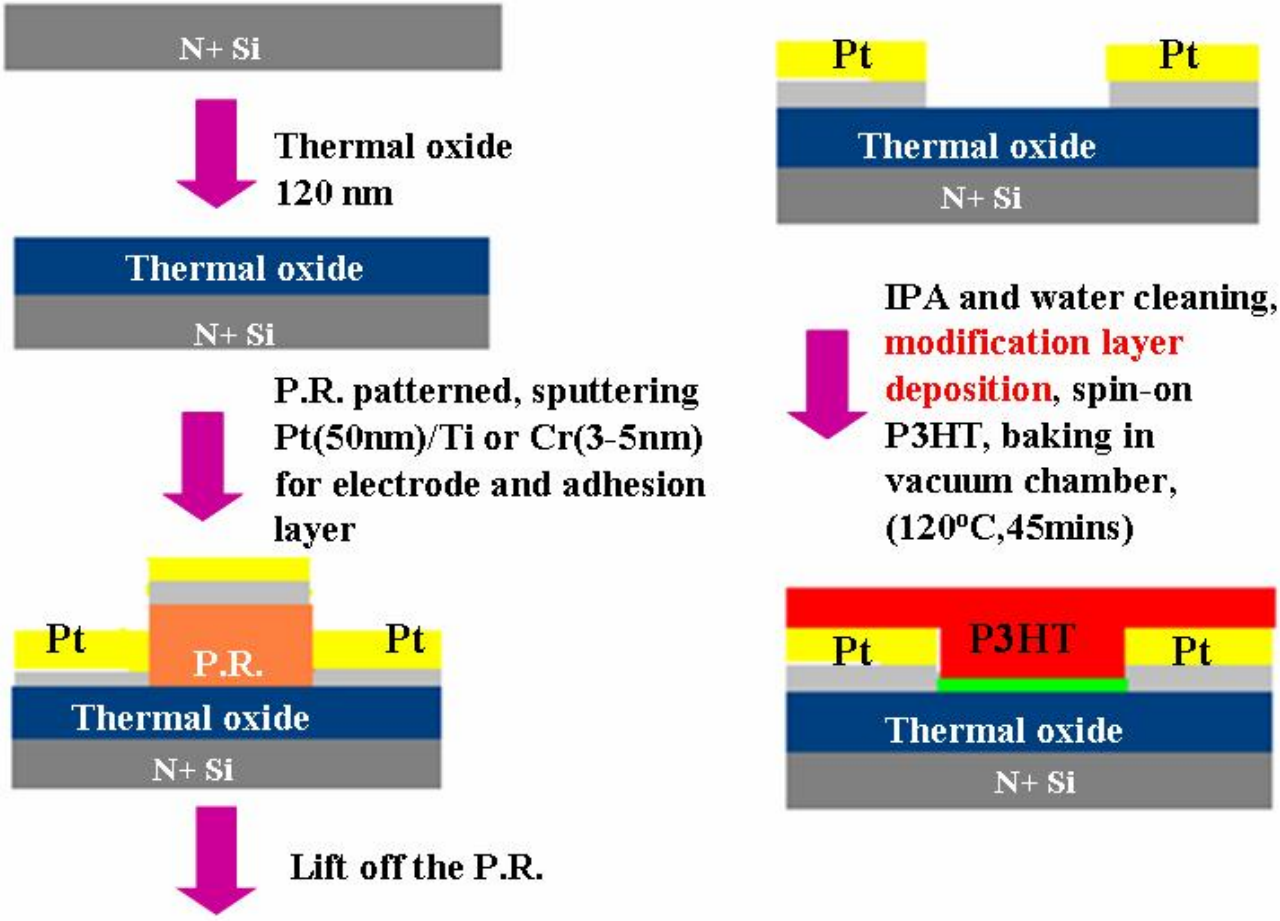
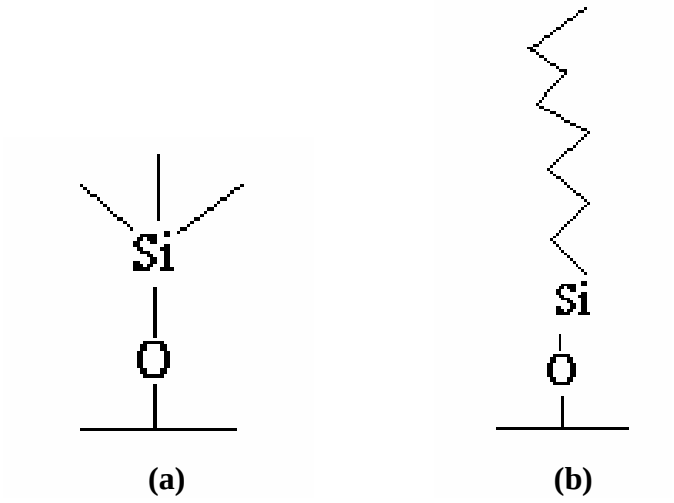


Fig.2-5 process flow of non-patterned P-TFTs



(a) **(b)**

Fig.2-6 (a) the structure of HMDS (b)the structure of OTs

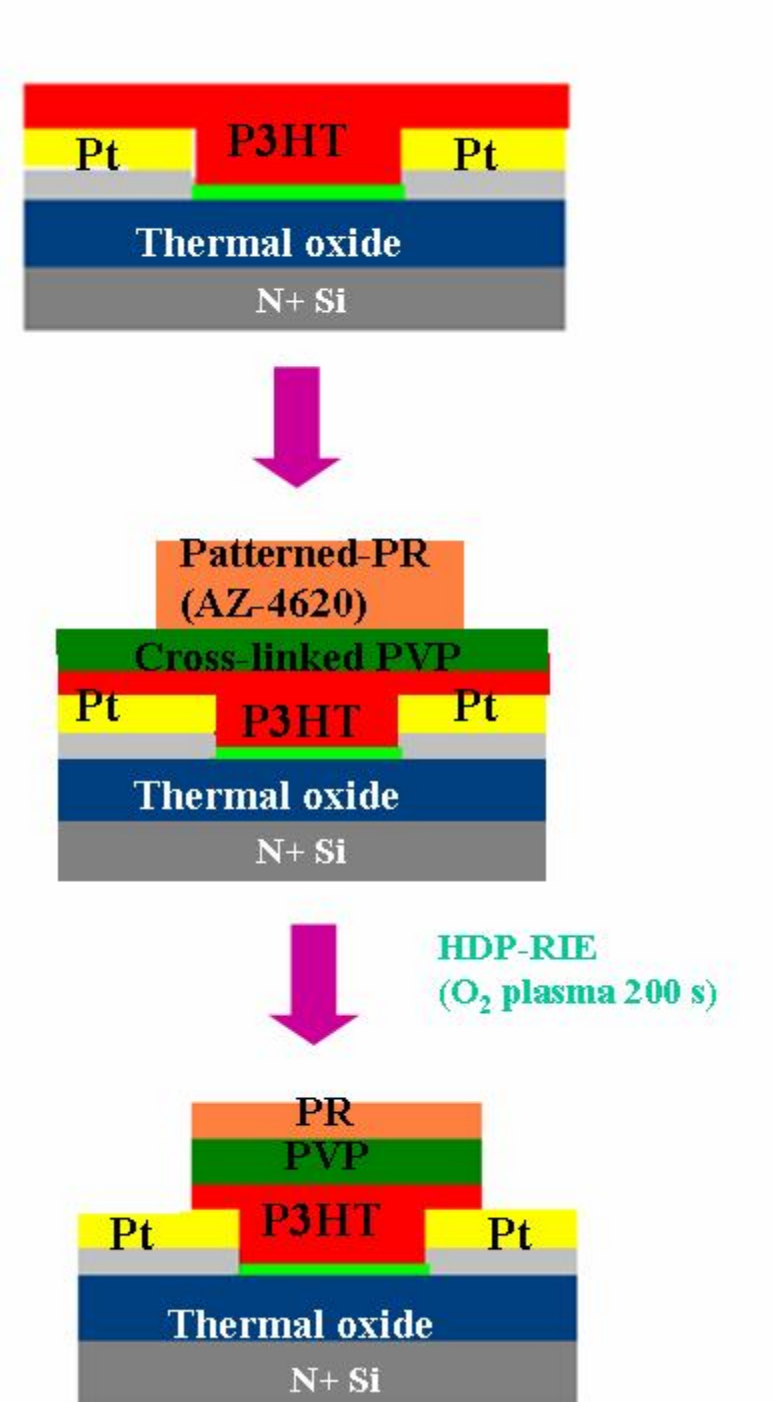


Fig.2-7 process flow of non-patterned gate and patterned active region P-TFTs

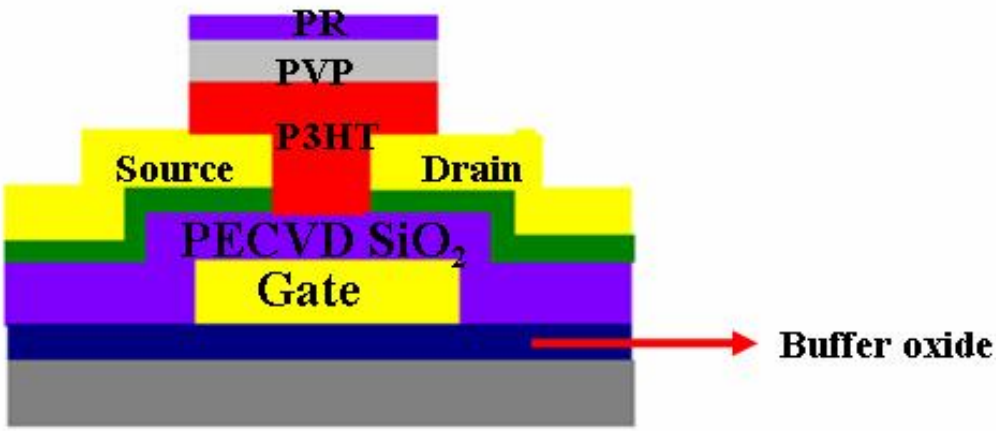


Fig.2-8 schematic diagram of patterned gate and patterned active region P-TFTs

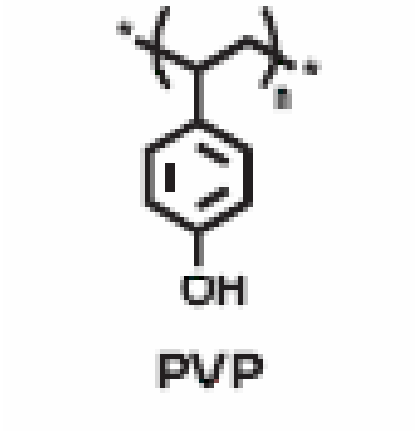


Fig.2-9 chemical structure of PVP

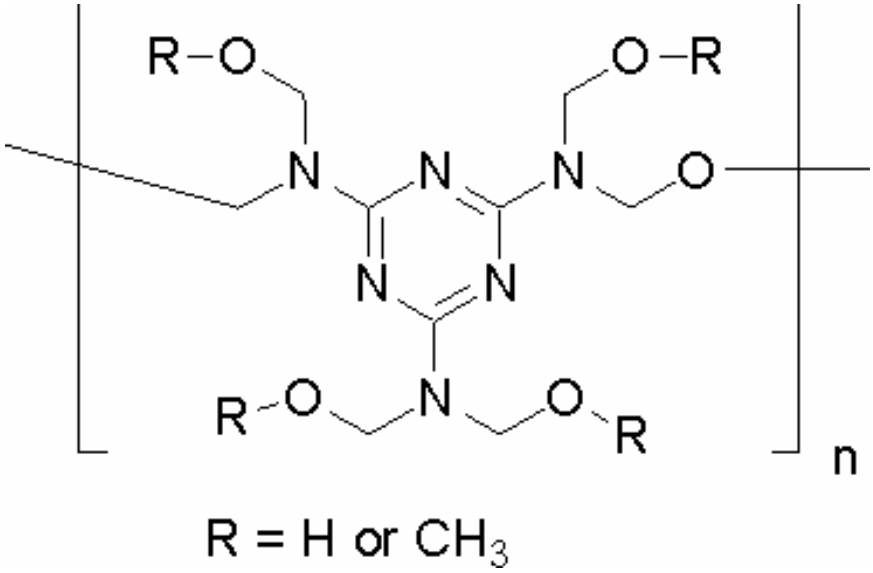


Fig.2-10 chemical structure of PMF

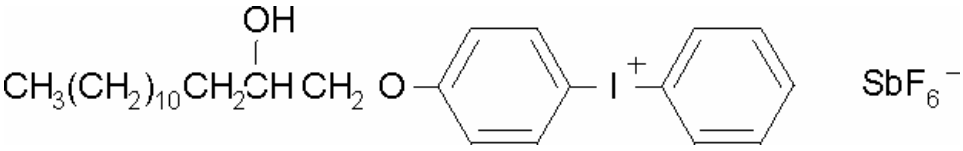


Fig.2-11 chemical structure of PAG

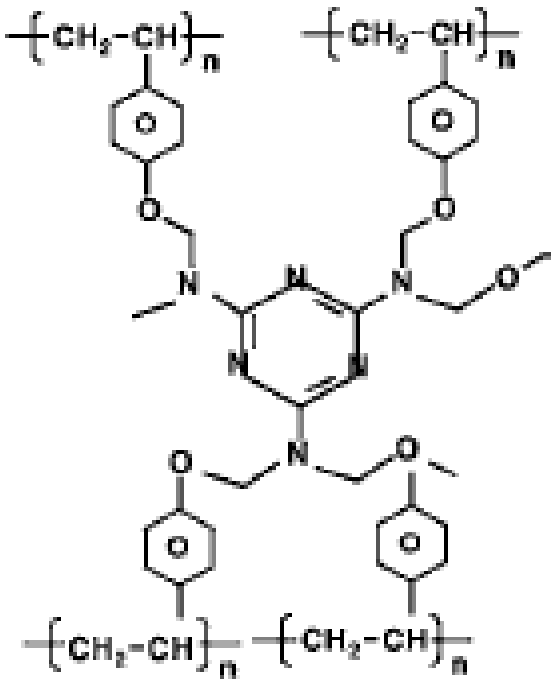
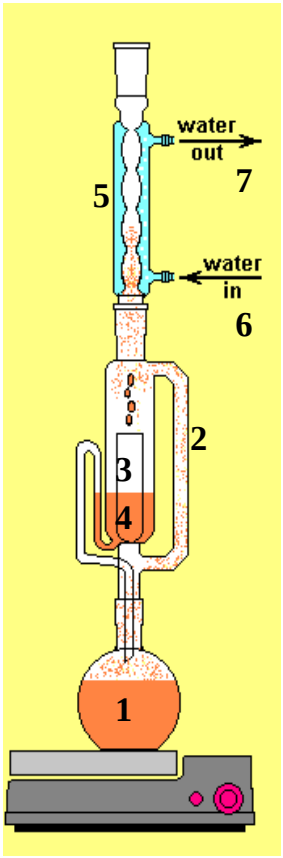


Fig.2-12 chemical structure of cross-linked PVP with PMF as cross-link agents



1: Still pot (extraction pot)

2: Distillation path

3: Soxhlet Thimble

4: Extraction solid (residue solid)

5: Condenser

6: Cooling water in

7: Cooling water out

Fig.3-1 the illustration of Soxhlet extraction to purify the P3HT

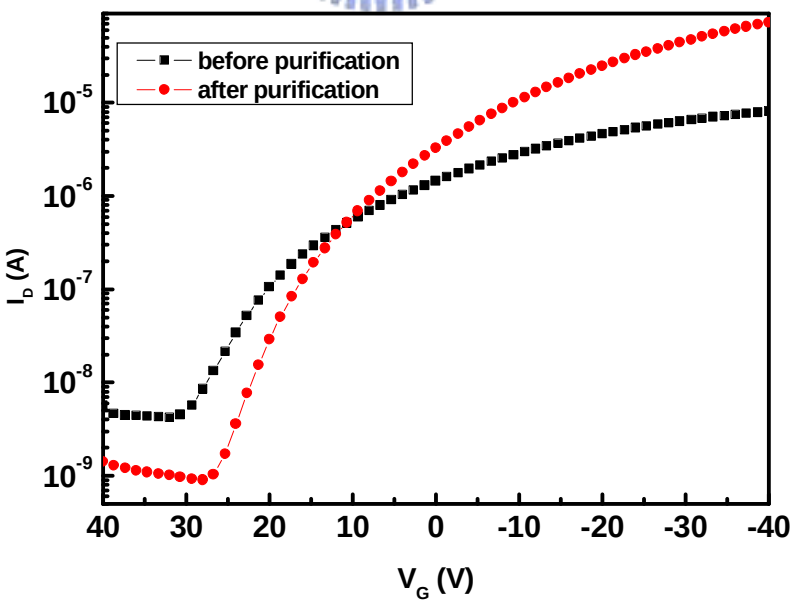


Fig.3-2 the I_D-V_G curves of P-TFT before and after purification of P3HT

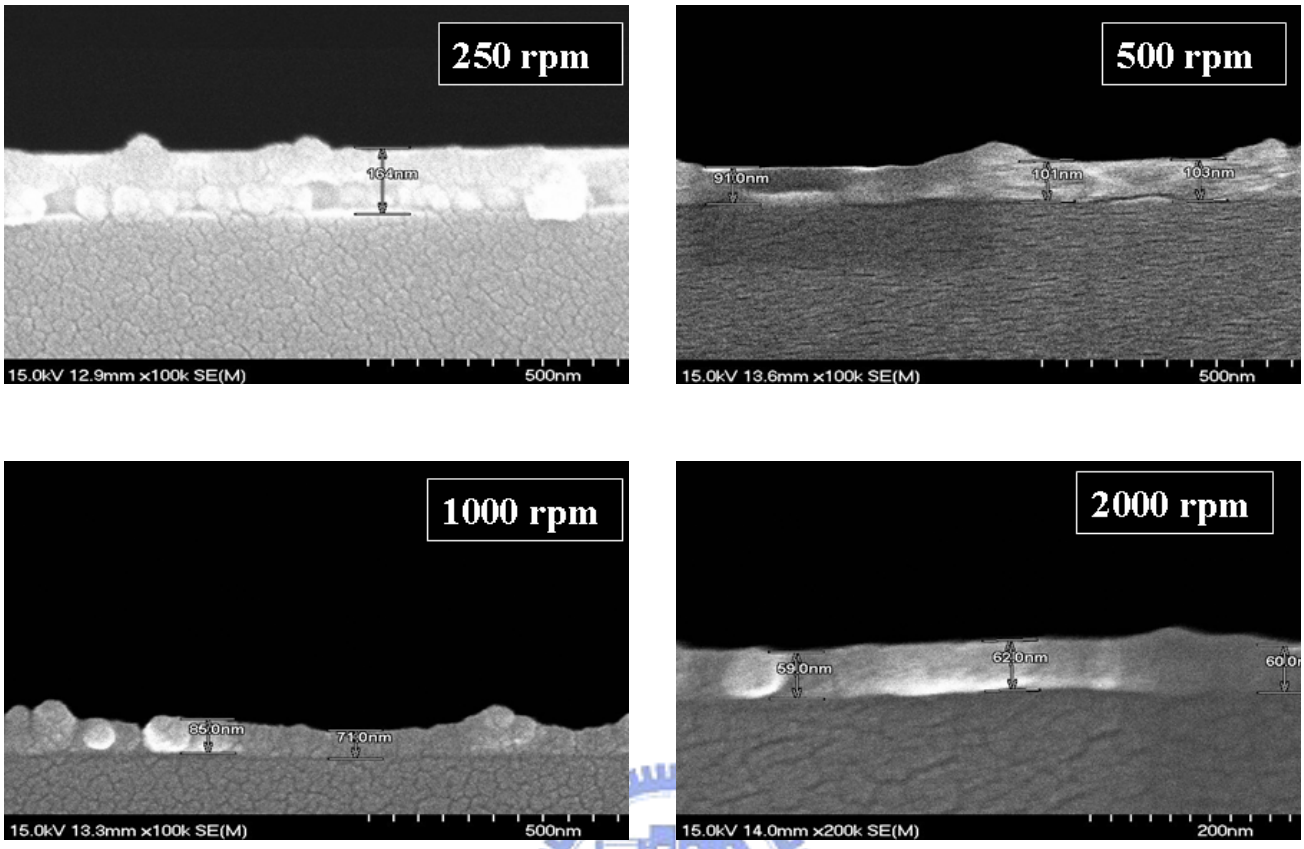


Fig.3-3 the thickness of the deposited P3HT in chloroform film with different coating rate: 250, 500, 1000, 2000rpm

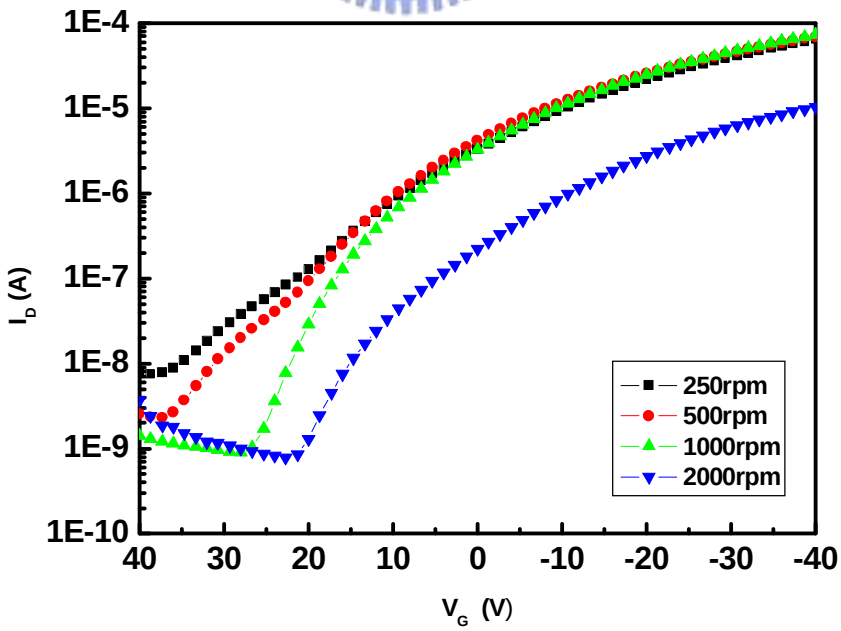


Fig.3-4 I_D-V_G curves of transistors with different coating rate

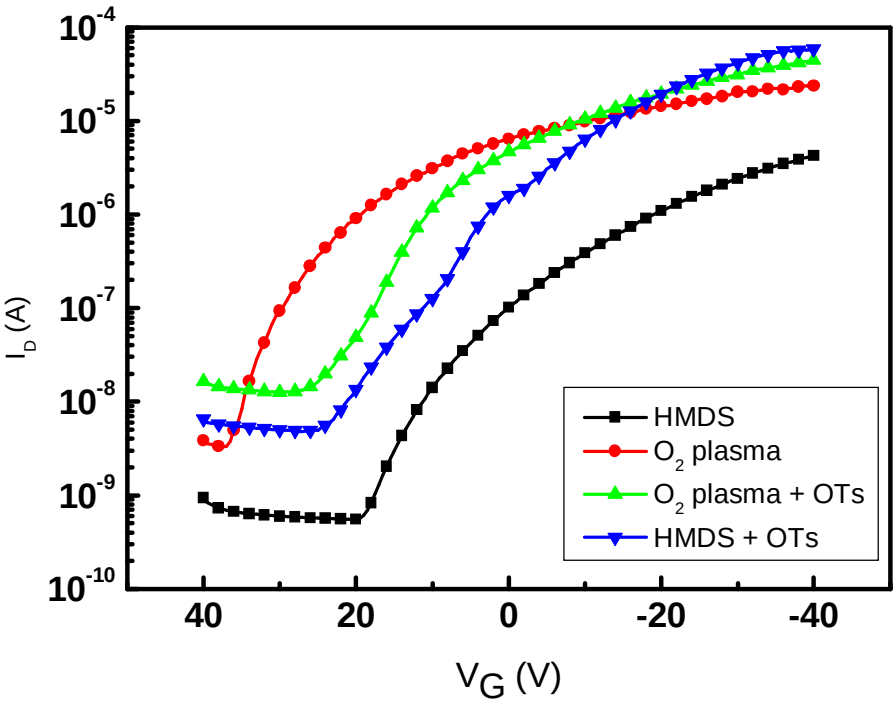


Fig.3-5 the I_D-V_G curves of P3HT-TFT with different modification layer.

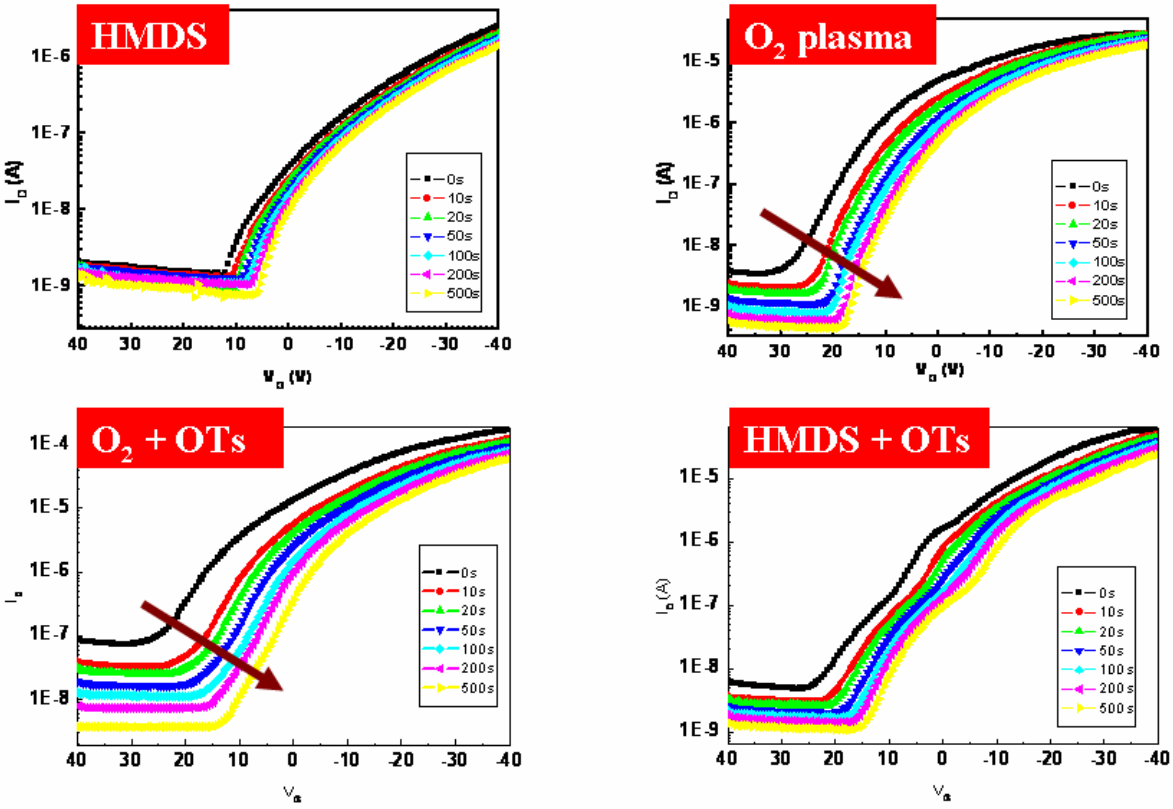


Fig. 3-6 a constant gate bias of -40 V was applied for 500 seconds with different modification layer.

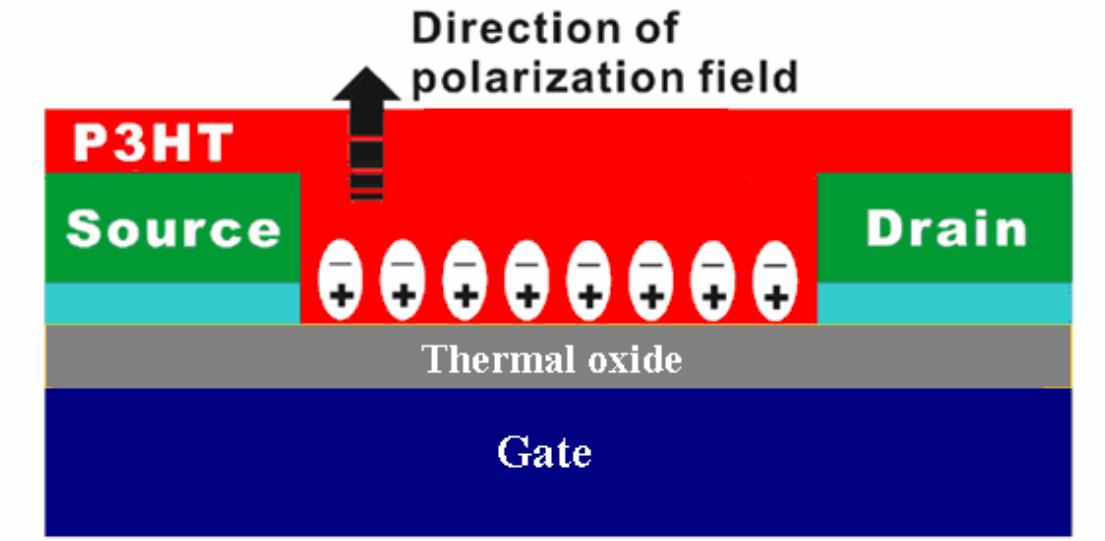


Fig.3-7 direction of polarization electric field under a constant gate bias stress of -40 V

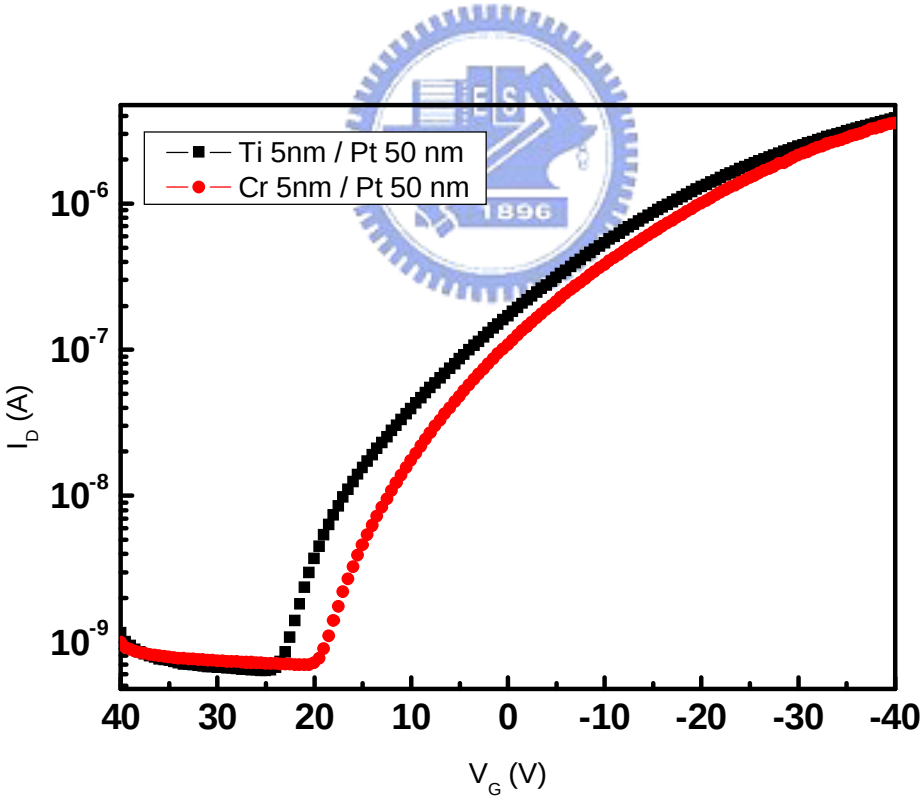


Fig.3-8 I_D-V_G curves of P-TFT with different adhesion layers.

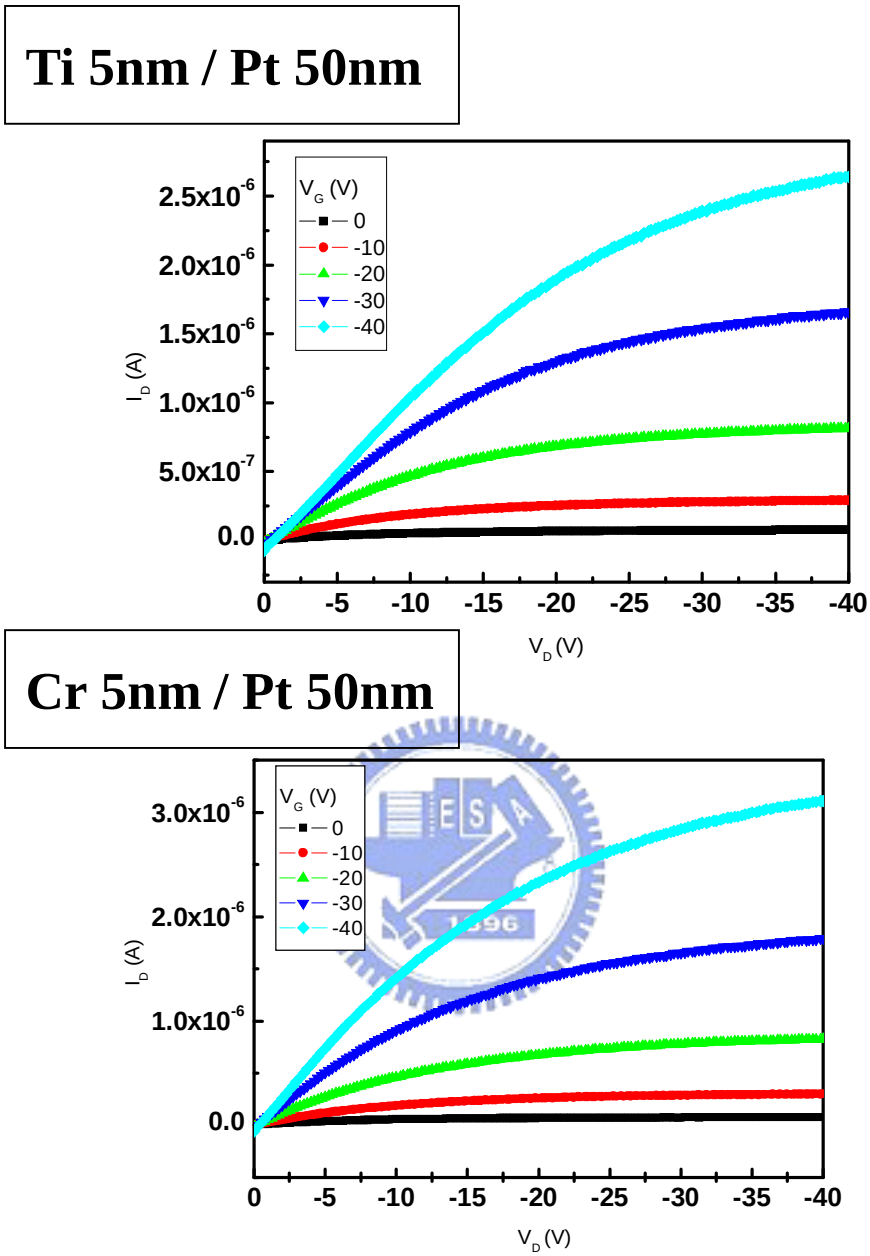


Fig.3-9 I_D-V_D curves of P-TFT with different adhesion layers.

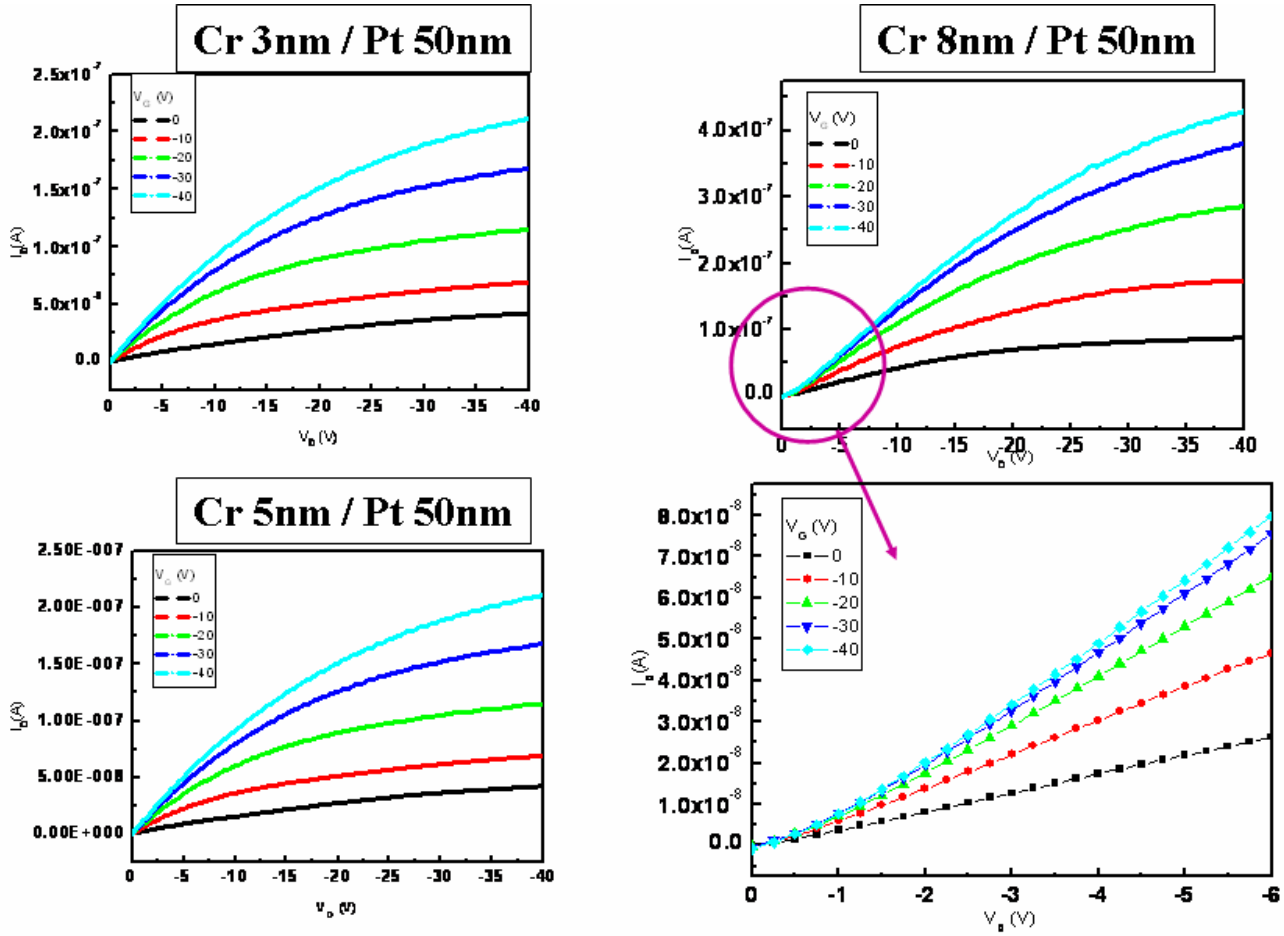
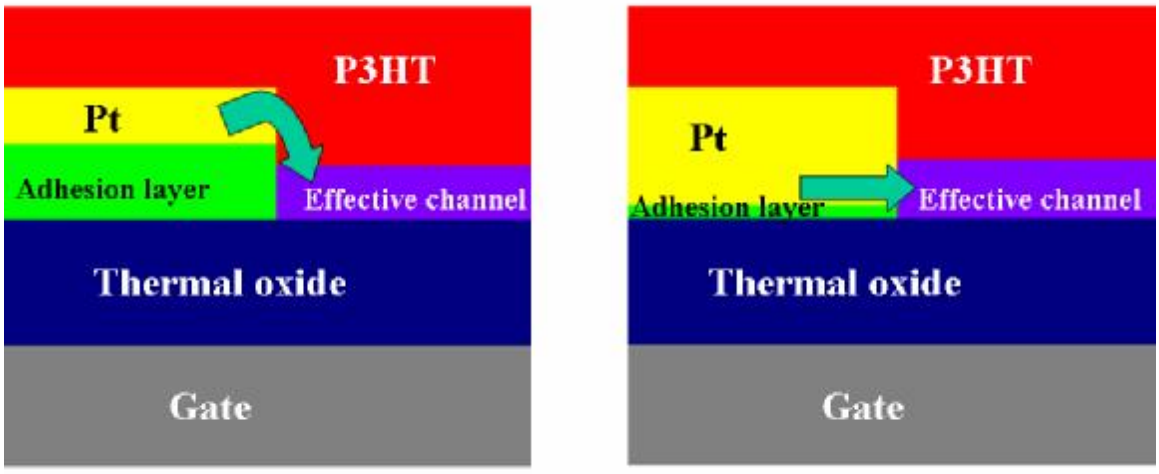


Fig.3-10 I_D-V_D curves of adhesion layer with different thickness including 3nm, 5nm, and 8nm.



(a) **(b)**

Fig.3-11 model of carrier injection into the effective channel from S/D electrodes when the adhesion layer is (a) thicker or (b) thinner than the conducting channel layer.

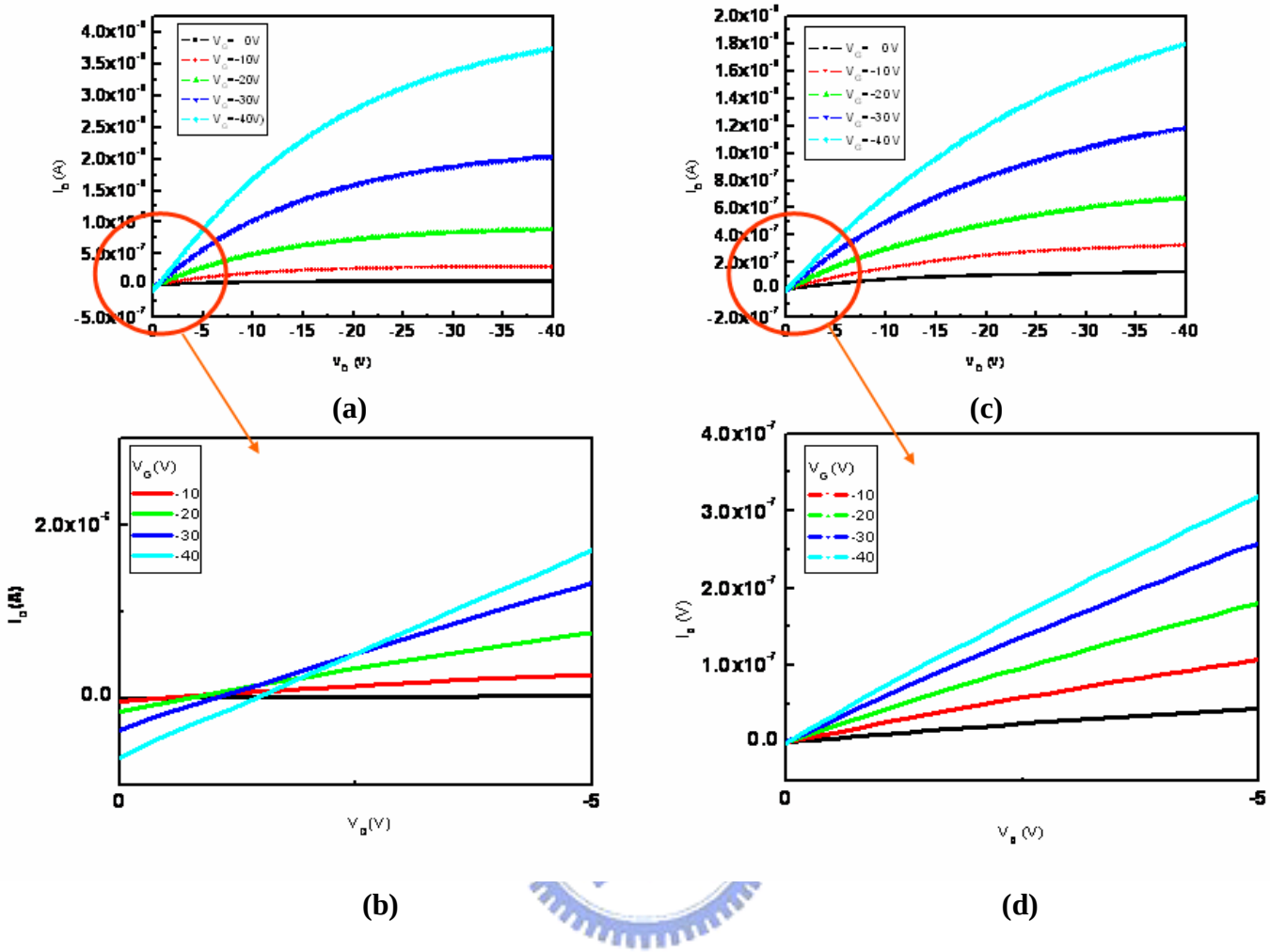


Fig.3-12 I_D–V_D characteristics of (a) (b) non-patterned P-TFT
(c) (d) non-patterned gate & patterned active layer P-TFTs

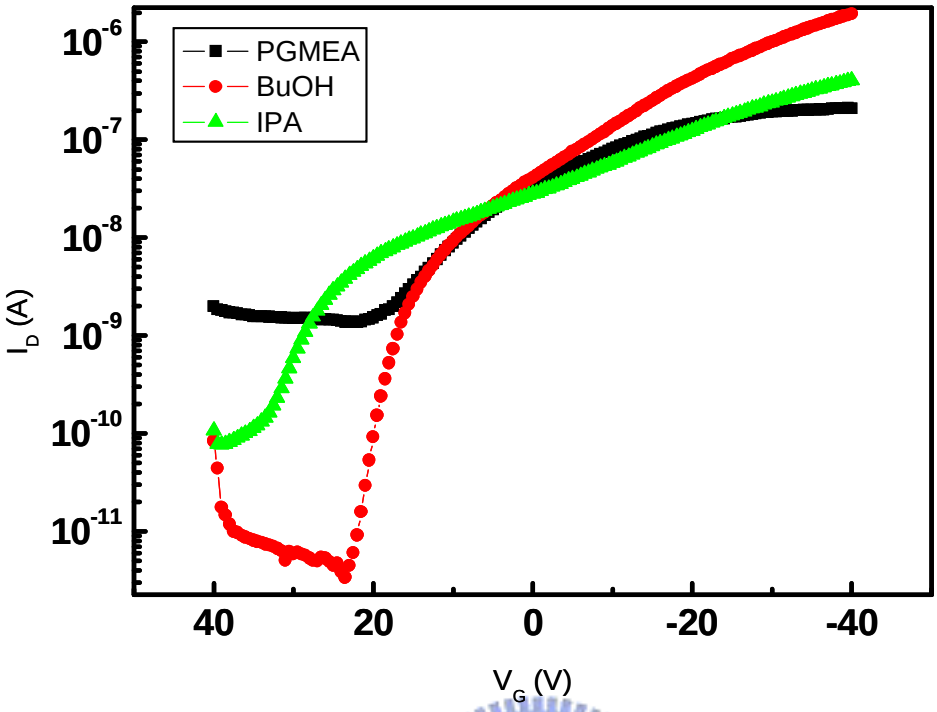


Fig.3-13 I_D-V_G curves of patterned P-TFT using PVP solution as passivation layer with different solvent

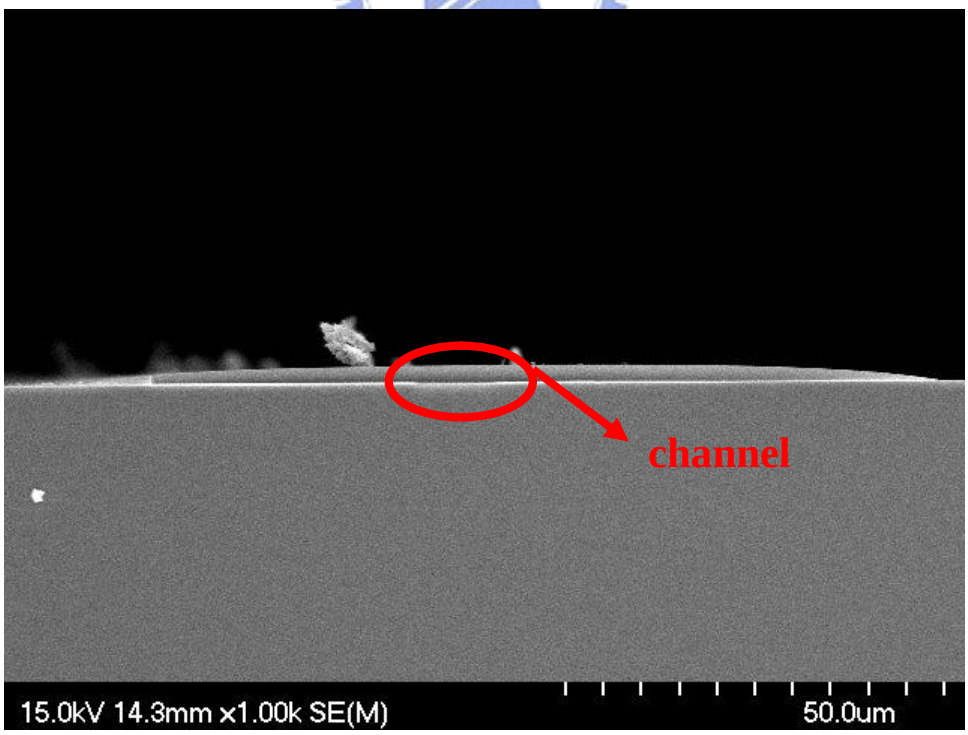


Fig.3-14 SEM graph: cross-section of P-TFTs with patterned P3HT

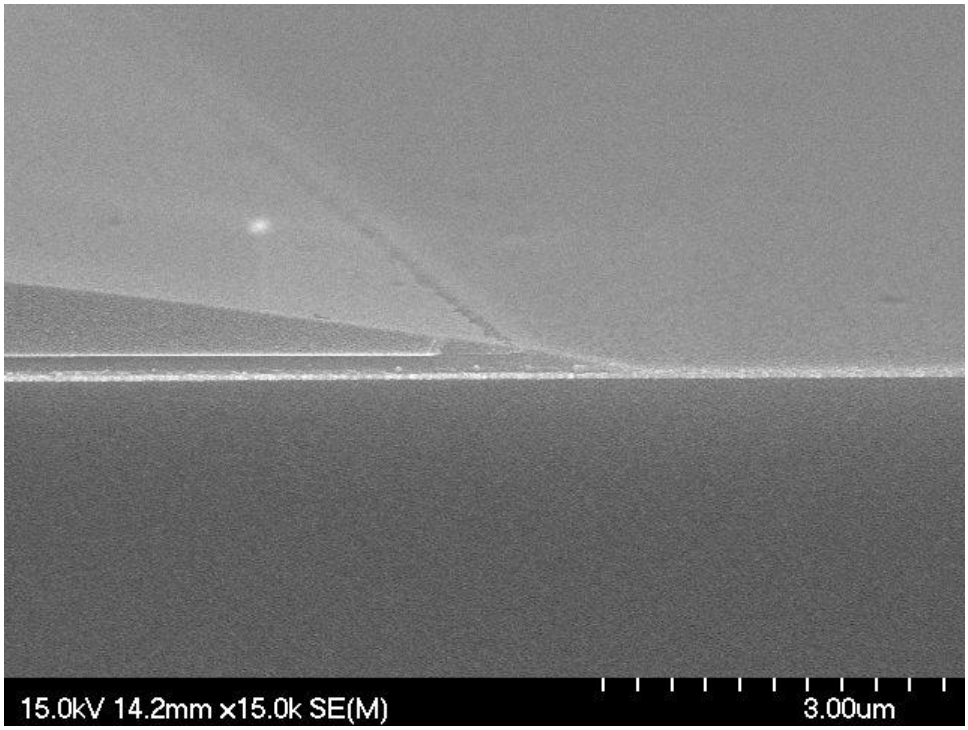


Fig. 3-15 SEM graph: the etching edge of P-TFTs with patterned P3HT

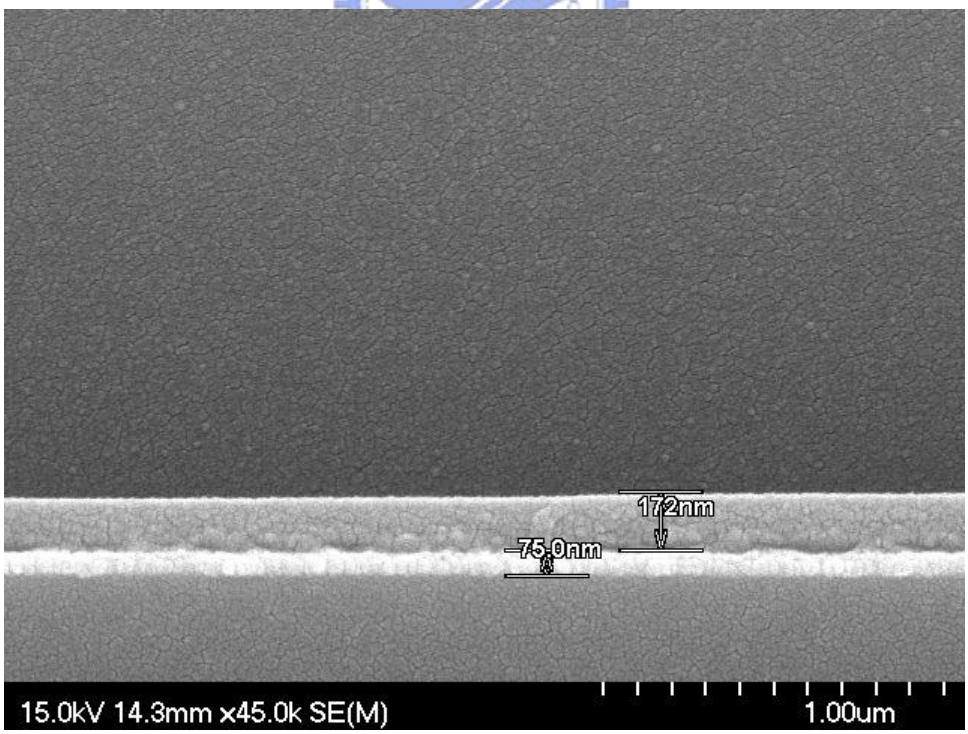


Fig. 3-16 SEM graph: P3HT (75 nm), PVP(172 nm) and thick PR

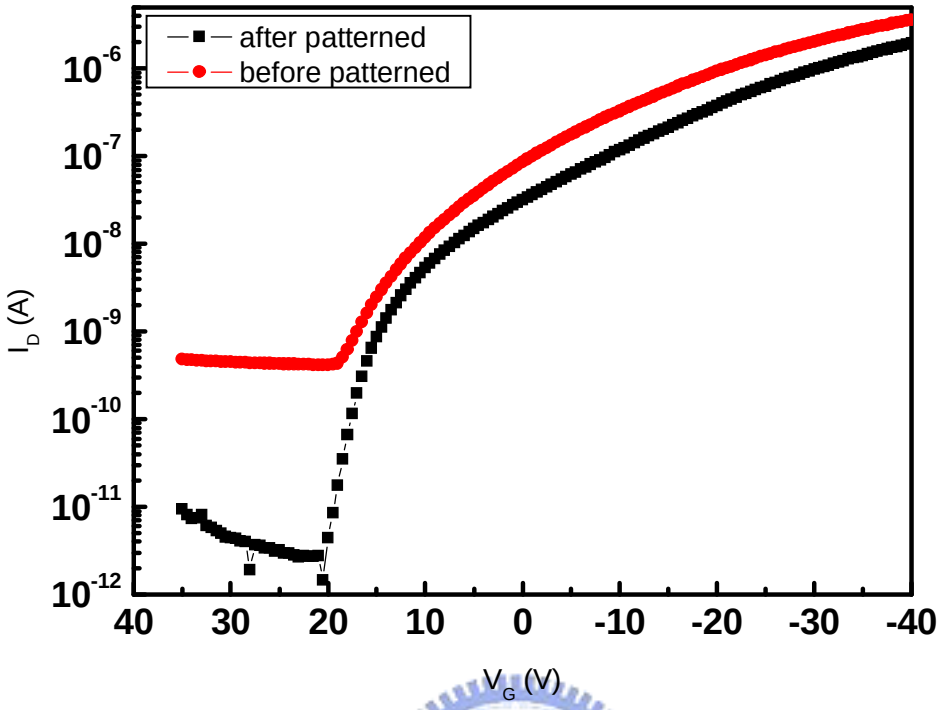


Fig.3-17 I_D-V_G curves of non-patterned and patterned active layer P-TFTs.

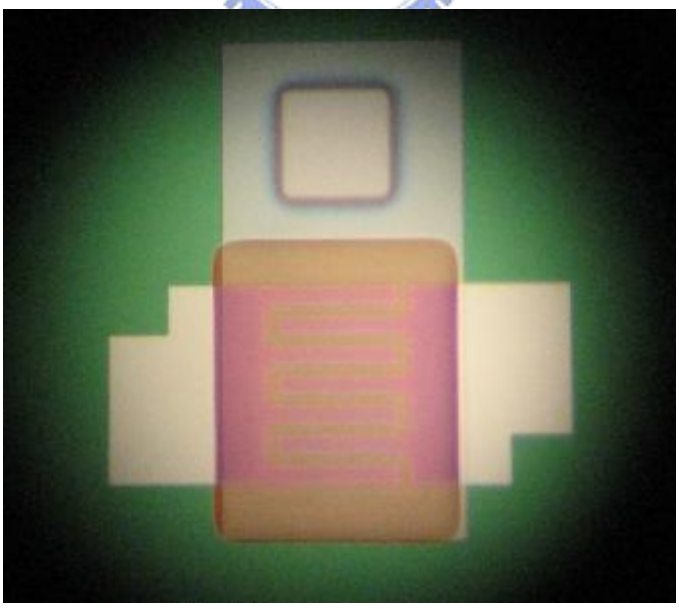


Fig.3-18 OM graph of patterned gate and patterned active layer P-TFTs

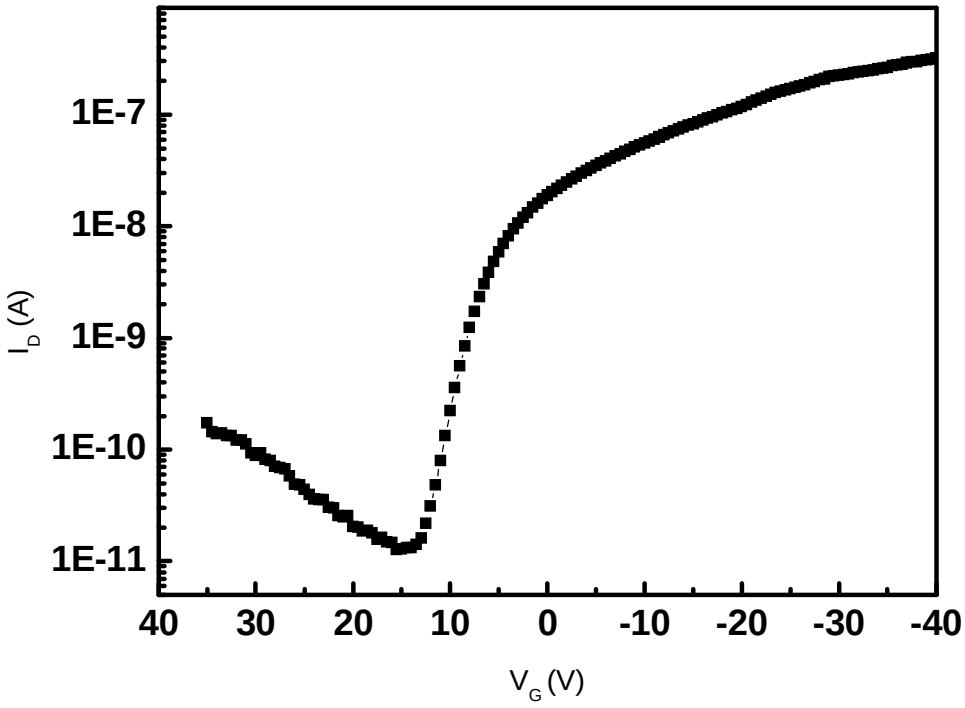


Fig.3-19 I_D-V_G curves of patterned gate and patterned active layer P-TFTs

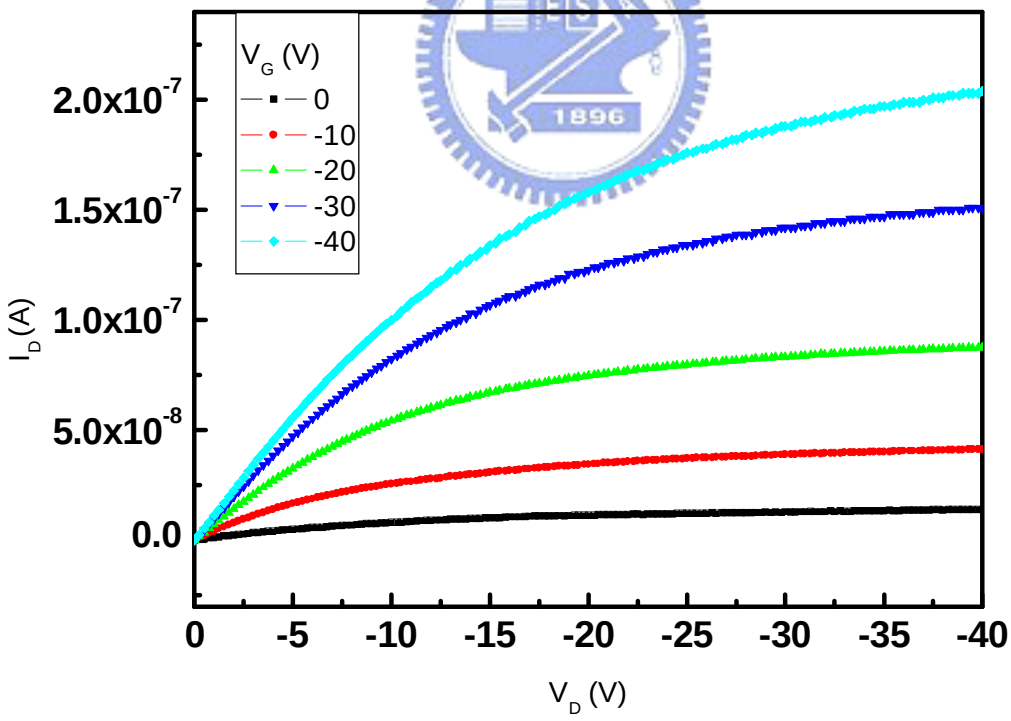


Fig.3-20 I_D-V_D curve of patterned gate and patterned active layer P-TFTs

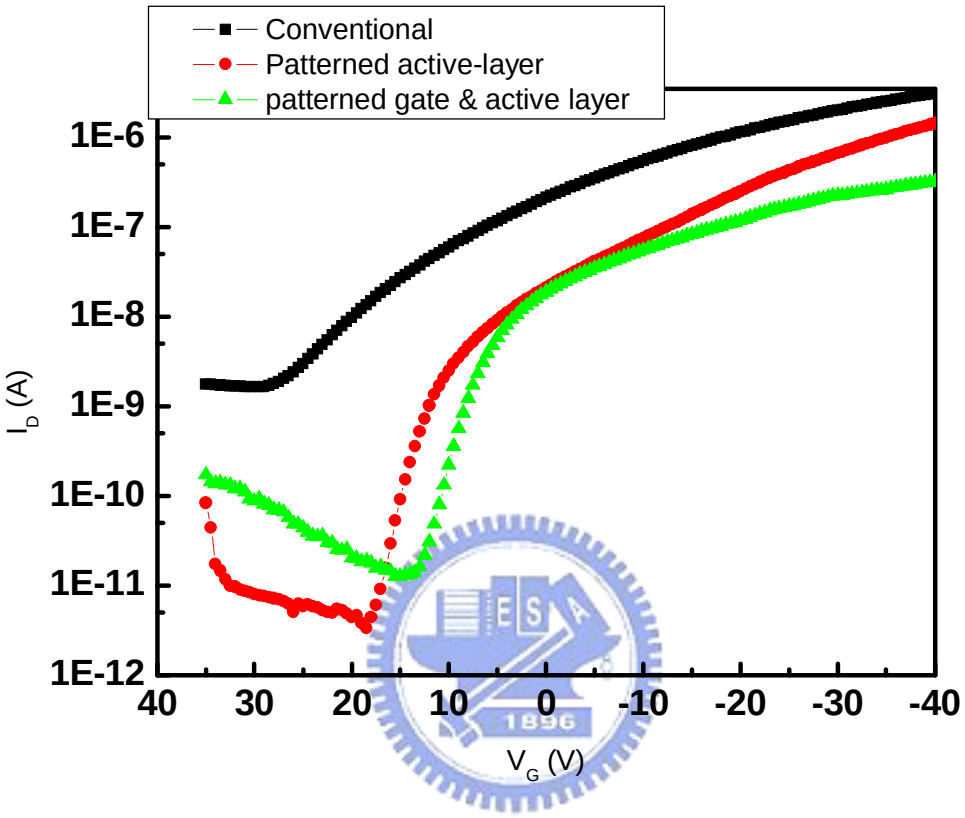


Fig.3-21 I_D-V_G curves of non-patterned and patterned P-TFTs with PECVD oxide

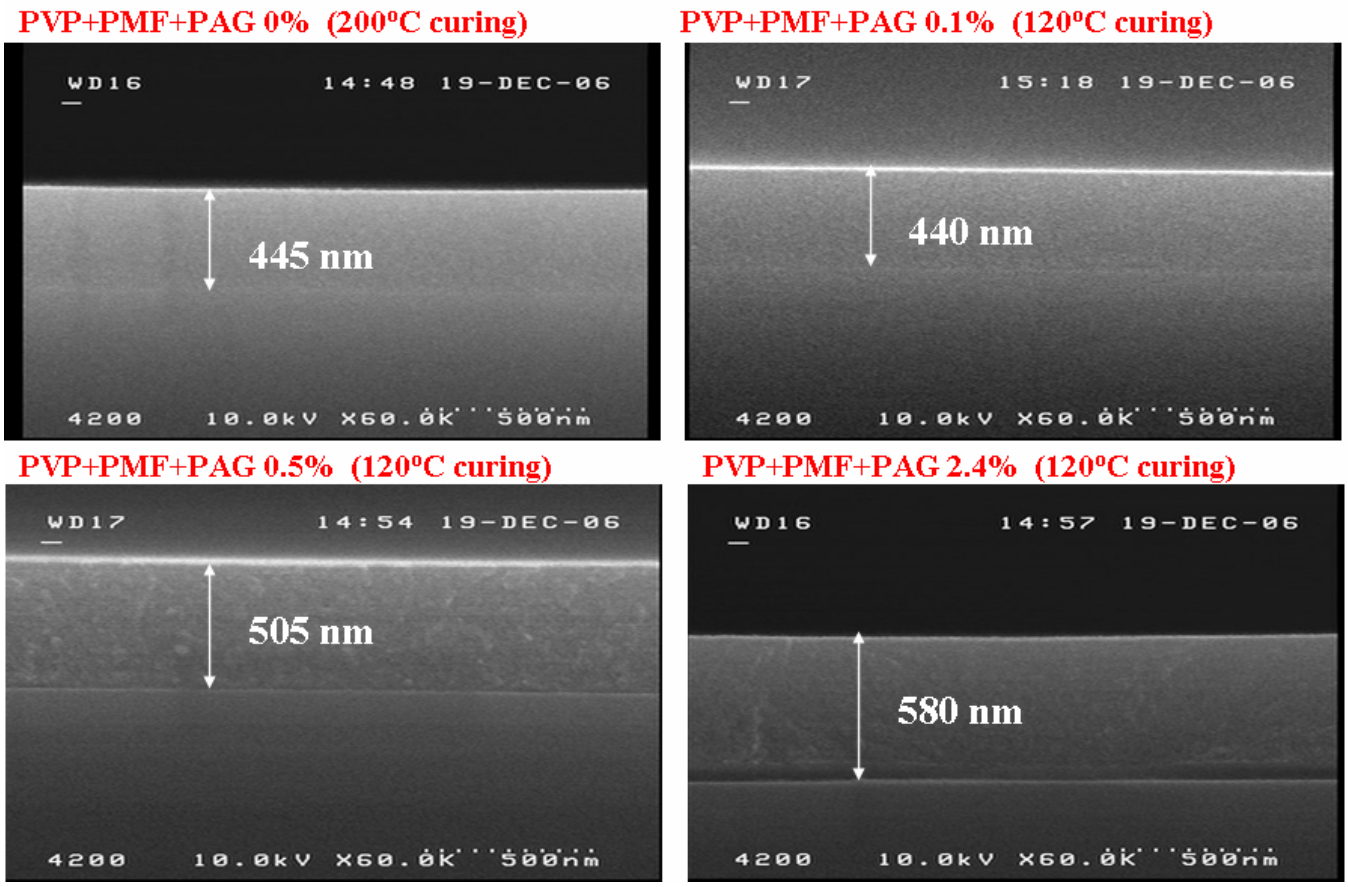


Fig.3-22 SEM of the deposited cross-linked PVP film with different weight percentage of PAG: 0, 0.1, 0.5, 2.4 wt%

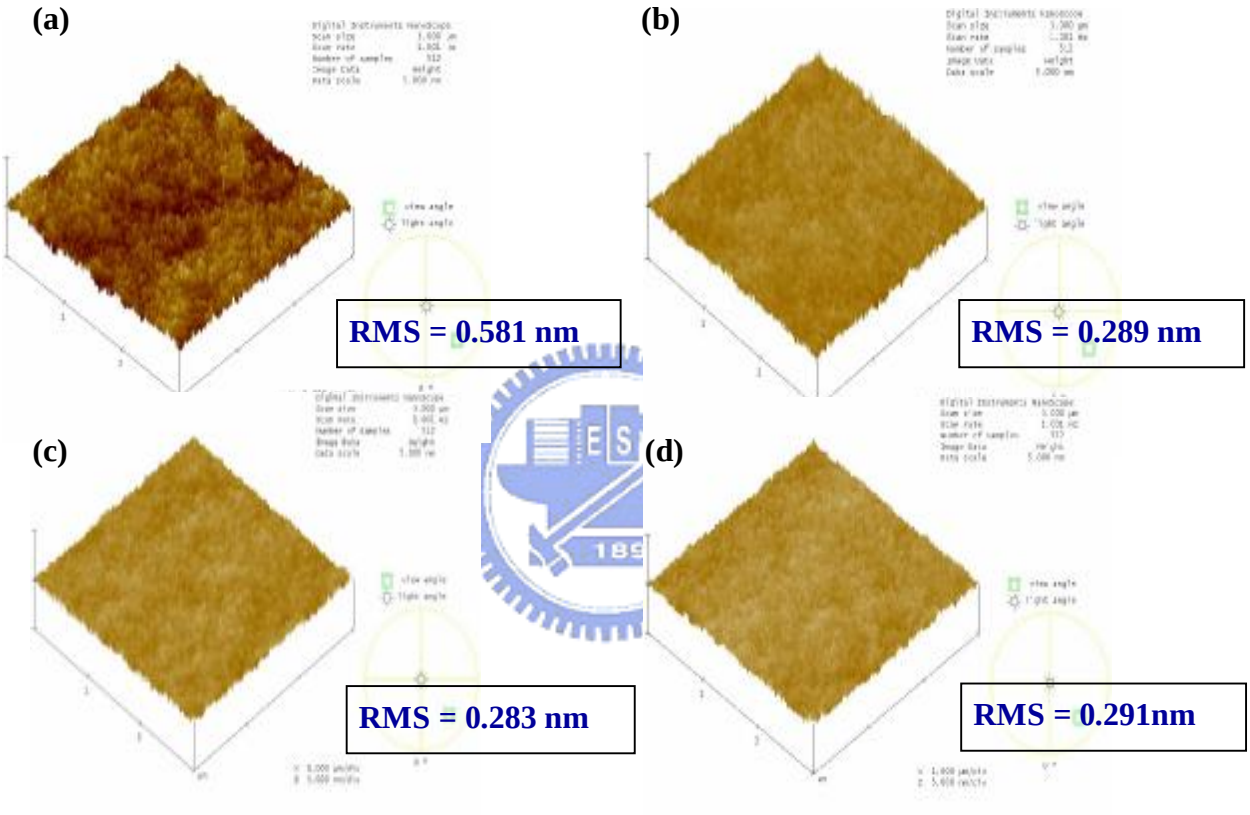


Fig.3-23 AFM of the deposited cross-linked PVP film with different weight percentage of PAG: (a)0 (b)0.1 (c)0.5 (d)2.4 wt%

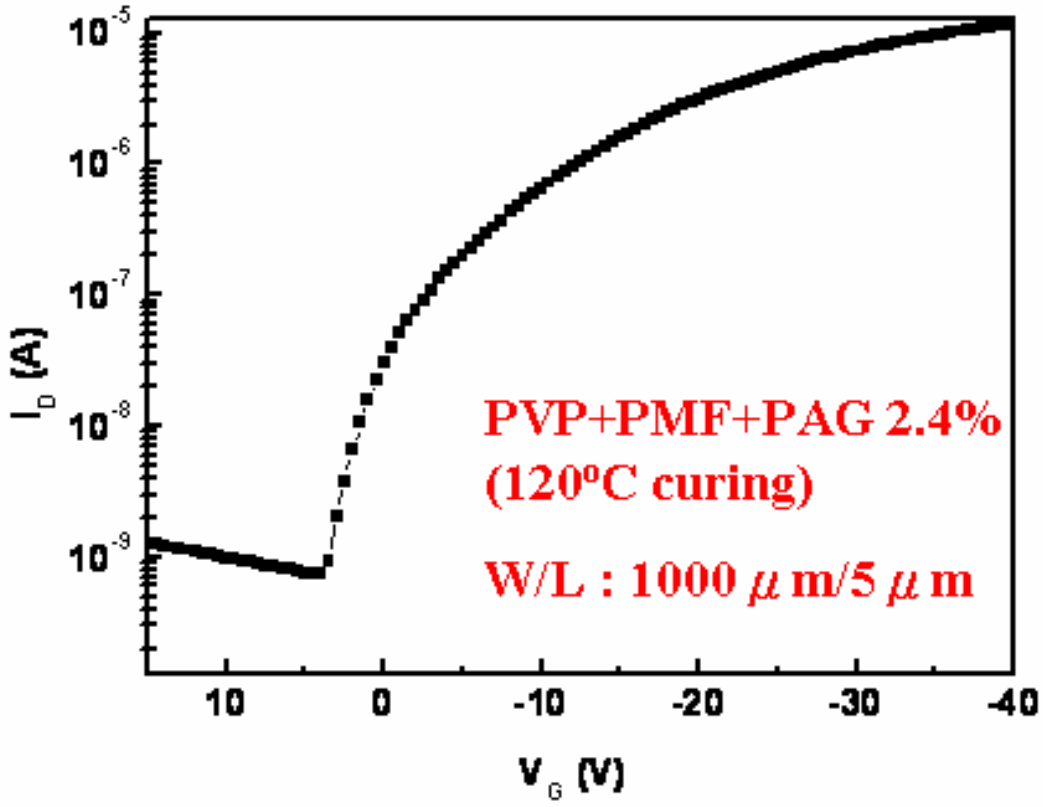


Fig.3-24 I_D-V_G curve of the P-TFT using cross-linked PVP as dielectric

Tables

Aldrich	Mn	Mw	PDI
As received	18496	45368	2.45
P3HT-hexane	5054	6907	1.37
P3HT-CH_2Cl_2	14415	25559	1.77
P3HT-3 (77%)	35928	63661	1.77

$$\bar{M}_w = \frac{\sum_i N_i M_i^2}{\sum_i N_i M_i}$$ **Weight average molecular weight**

$$\bar{M}_n = \frac{\sum_i N_i M_i}{\sum_i N_i}$$ **Number average molecular weight**

Table 3-1 the results of the separation of P3HT into narrow molecular weight fractions

	Before patterned	After patterned
mobility (cm^2/V-s)	0.0022	0.0013
on/off	10^3	10^6
V_{th}	1.94	-0.43
swing (V/decade)	4.5	1.3

Table 3-2 characteristic of non-patterned and patterned active layer P-TFTs with thermal oxide

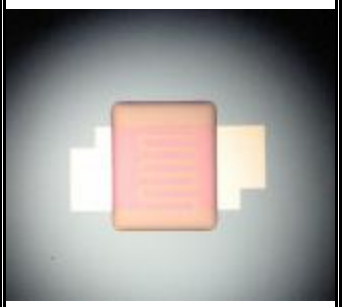
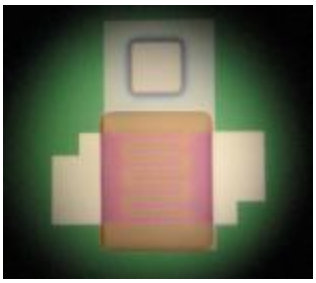
	Conventional	Patterned-P3HT	Patterned-P3HT & Patterned-Gate
			
Mobility (cm^2/V-s)	**0.0012**	**0.0010**	**0.00014**
on/off	**10^3**	**5×10^5**	**2×10^4**
V_{th} (V)	**11**	**-0.12**	**7**
swing (V/decade)	**4.5**	**1.9**	**2.25**

Table 3-3 characteristic and the OM graph of non-patterned and two kinds of patterned P-TFTs with PECVD oxide.

References

[1] J. H. Burroughes, D. C. C. Bradley, A. R. Brown, R. N. Marks, K. McKay, R. H. Friend, P. N. Burns and R. B. Holmes,” Light-emitting diodes based on conjugated polymers” *Nature*, 335, 539, 1990.

[2] J. Gmeiner, S. Karg, M. Meier, W. Reiû, P. Strohriegl and M. Schwoerer, **“** Synthesis, electrical conductivity and electroluminescence of poly(p-phenylene vinylene) prepared by the precursor route**“** *Acta Polymerica*.,44, 201, 1993.

[3] H. Antoniadis, B. R. Hsieh, M. A. Abkowitz, S. A. Jenekhe and M. Stolka, “Photovoltaic and photoconductive properties of aluminum/poly(p-phenylene vinylene) interfaces “ *Synth. Met.*, 62, 265, 1994.

[4] A. Tsumura, H. Koezuka and T. Ando, ” FIELD-EFFECT TRANSISTOR WITH POLYTHIOPHENE THIN FILM.” *Appl. Phys. Lett.*, 49, 1210, 1986.

[5] F. Garnier, R. Hajlaoui, A. Yassar and P. Srivastava, “All-polymer field-effect transistor realized by printing techniques” *Science*, 265, 1684, 1994.

[6] L. Torsi, A. Dodabalapur, L. J. Rothberg, A. W. P. Fung and H. E. Katz, “Intrinsic transport properties and performance limits of organic field-effect transistors.” *Science*, 272, 1462, 1996.

[7] B. Crone, A. Dodabalapur, A. Gelperin, L. Torsi, H. E. Katz, A. J. Lovinger, Z. Bao, “Electronic sensing of vapors with organic transistors” *Appl. Phys. Lett.*, 78, 2229,

2001.

[8] C. J. Drury, C. M. J. Mutsaers, C. M. Hart, M. Matters, D. M. de Leeuw, “Low-cost all-polymer integrated circuits” *Appl. Phys. Lett.*, 73, 108, 1998.

[9] J. Paloheimo, P. Kuivalainen, H. Stubb, E. Vuorimaa, and P. Y. Lahti, “Mobility in conducting polymer transistors” *Appl. Phys. Lett.* 56, 157, 1990.

[10] H. Fuchigami, A. Tsumura, and H. Koezuka, “Polythienylenevinylene thin-film transistor with high carrier mobility” *Appl. Phys. Lett.* 63, 1372, 1993.

[11] J. H. Burroughes, C. A. Jones, and R. H. Friend, “NEW SEMICONDUCTOR DEVICE PHYSICS IN POLYMER DIODES AND TRANSISTORS” *Nature (London)* 335, 137, 1988

[12] F. Garnier, A. Yassar, R. Hajlaoui, G. Horowitz, F. Deloffre, B. Servet, S. Ries, and P. Alnot, “Molecular engineering of organic semiconductors. Design of self-assembly properties in conjugated thiophene oligomers” *J. Am. Chem. Soc.* 115, 8716, 1993.

[13] G. Horowitz, D. Fichou, X. Peng, Z. Xu, and F. Garnier, “Field-effect transistor based on conjugated alpha-sexithienyl” *Solid State Commun.* 72, 381, 1989.

[14] A. Dodabalapur, L. Torsi, and H. E. Katz, “Organic transistors: two-dimensional transport and improved electrical characteristics” *Science* 268, 270, 1995.

[15] H. Akimichi, K. Waragai, S. Hotta, H. Yano, and H. Sasaki, “Field-effect transistors using alkyl substituted oligothiophenes” *Appl. Phys. Lett.* 58, 1500, 1991

[16] Z. Bao, A. J. Lovinger, and A. Dobabalapur, “Organic field-effect transistors with high mobility based on copper phthalocyanine” *Appl. Phys. Lett.* 69, 3066, 1996

[17] J. G. Laquindanum, H. E. Katz, A. J. Lovinger, and A. Dodabalapur, “Benzodithiophene rings as semiconductor building blocks” *Adv. Mater.* 9, 36, 1997

[18] J. G. Laquindanum, H. E. Katz, A. J. Lovinger, and A. Dodabalapur, “Morphological Origin of High Mobility in Pentacene Thin-Film Transistors” *Chem. Mater.* 8, 2542, 1996

[19] Y. Lin, T. Gundlach, and T. N. Jackson, “Contact dependence of α-sexithienyl thin film transistor characteristics” *Materials Research Society Symposium - Proceedings, v 413, Electrical, Optical, and Magnetic Properties of Organic Solid State Materials III*, 413-418, 1996

[20] A. Assadi, C. Svensson, M. Willander, O. Inganäs, “Field-effect mobility of poly(3-hexylthiophene)” *Appl. Phys. Lett.*, 53, 195, 1988.

[21] Christos D. Dimitrakopoulos, D. J Mascaro, “Organic thin film transistors : A review of recent advances ” *IBM J. RES. & DEV.* 45(1), 11, 2001

[22] Christos D. Dimitrakopoulos, Parick R. Malenfant, “Organic thin film transistorsfor large area electronics” *Adv. Mater*. 14, No2, January 16, 2002.

[23] A. Assadi, C. Svensson, M. Willander, O. Inganas, “Field-effect mobility of poly(3-hexylthiophene)” *Appl. Phys. Lett*. 53(3), 18 July, 1988

[24] Zhenon Bao, Ananth Dodabalapur, and Andrew J. Lovinger, “Soluble and processable regioregular poly(3-hyxelthiophene) for thin film field-effect transistor applications with high mobility,” Appl. Phys. Lett., vol. 69, No. 26, Dec. 1996.

[25] J. H. Lin ”The Analysis of Process Improvement and Reliability Characteristic of Spin-On Organic TFT”, Graduate thesis.

[26] Y. Chen, I. Shih and S. Xiao, “Effects of $FeCl_3$ doping on polymer-based thin film transistors” *Journal of Applied Physics*, 96, 454, 2004.

[27] H. Sirringhaus, N. Tessler, R. H. Friend, “Integrated optoelectronic devices based on conjugated polymers” *Science*, 280, 1741, 1998

[28] D. H. Kim, Y. D. Park, Y. S. Jang, H. C. Yang, Y. H. Kim, J. I. Han, D. G. Moon, S. J. Park, T. Y. Chang, C. W. Chang, M. K. Joo, C. Y. Ryu, K. W. Cho, **“**Enhancement of Field-Effect Mobility Due to Surface-Mediated Molecular Ordering in Regioregular Polythiophene Thin Film Transistors**”** *Adv. Funct. Mater.*, 15, 77, 2005.

[29] Z. Bao, A. Dodabapur, and A. J. Lovinger, “Soluble and processable regioregular poly(3-hexylthiophene) for thin film field-effect transistor applications with high mobility”*Appl. Phys. Lett.* 69, 4108, 1996.

[30] H. Sirringhaus, R. J. Wilson, R. H. Friend, M. Inbasekaran, W. Wu, E. P. Woo, M. Grell, and D. D. C. Bradley, “Mobility enhancement in conjugated polymer field-effect transistors through chain alignment in a liquid-crystalline phase” *Appl. Phys. Lett.* 77, 406, 2000.

[31] H. Sirringhaus, N. Tessler, and R. H. Friend, “Integrated optoelectronic devices

based on conjugated polymers" *Science* 280, 1741, 1998.

[32] A. Salleo, M. L. Chabinyc, M. S. Yang, and R. A. Street, "Polymer thin-film transistors with chemically modified dielectric interfaces" *Appl. Phys. Lett*. 81, 4383 , 2002.

[33] T. W. Kelley, L. D. Boardman, T. D. Dunbar, D. V. Muyres, M. J. Pellerite, and T. P. Smith, "High-performance OTFTs using surface-modified alumina dielectrics" *J. Phys. Chem*. B 107, 5877, 2003.

[34] Y. Y. Lin, D. J. Gundlach, S. F. Nelson, and T. N. Jackson, "Stacked pentacene layer organic thin-film transistors with improved characteristics" *IEEE Trans. Electron Devices* 44, 1325,1997.

[35] D.G. Lidzey, M. Voigt, C. Giebeler, A. Buckley, J. Wright, K. Bo¨hlen, J. Fieret, R. Allott, "Laser-assisted patterning of conjugated polymer light emitting diodes" *Org. Electr*. 6 221, 2005.

[36] I. Kymissis, C.D. Dimitrakopoulos, S. Purushothanman, "Patterning pentacene organic thin film transistors" *J. Vac. Sci. Technol*. B 20 (3) 956, 2002.

[37] H. Jia, G.K. Pant, E.K. Gross, E.M. Wallace, B.E. Bruce, "Gate induced leakage and drain current offset in organic thin film transistors" *Org. Electr.* 7,16, 2006.

[38] T. W. Kelley, D. V. Muyres, P. F. Baude, T. P. Smith, and T. D. Jones, "High Performance Organic Thin Film Transistors" *Mater. Res. Soc. Symp. Proc*. 771, L.6.5.1, 2003.

[39] S. De Vusser, S. Steudel, K. Myny, J. Genoe, and P. Heremans, "Integrated shadow

mask method for patterning small molecule organic semiconductors" *Appl. Phys. Lett.* 88, 103501, 2006.

[40] S. Steudel, D. Janssen, S. Verlaak, J. Genoe, and P. Heremans, " Patterned growth of pentacene" *Appl. Phys. Lett.* 85, 5550, 2004.

[41] C. Balocco, L.A. Majewski, A.M. Song, "Non-destructive patterning of conducting-polymer devices using subtractive photolithography" *Organic Electronics* 7 500–507, 2006

[42] Huiping Jia, Gaurang K. Pant, Erich K. Gross, Robert M. Wallace, Bruce E. Gnade, "Gate induced leakage and drain current offset in organic thin film transistors" *Organic Electronics* 7 16–21, 2006.

[43] J.A. DeFranco, B.S. Schmidt, M. Lipson, G.G. Malliaras, "Photolithographic patterning of organic electronic materials" *Org. Electr*. 7, 22, 2006.

[44] F.M. Li, Y. Vygranenko, S. Koul, A. Nathan, "Photolithographically defined polythiophene organic thin-film transistors" *J. Vac. Sci. Technol*. A 24 (3),657, 2006.

[45] M.L. Chabinyc, A. Salleo, "Materials requirements and fabrication of active matrix arrays of organic thin-film transistors for displays" *Chem. Mater*. 16, 4509, 2004.

[46] C. Reese, M. Roberts, M. Ling, Z. Bao, "Organic thin film transistors" *Mater. Today* 7, 20, 2004.

[47] M. Ling, Z. Bao, "Thin film deposition, patterning, and printing in organic thin film transistors" *Chem. Mater*. 16, 4824 2004.

[48] H.E. Katz, “Recent advances in semiconductor performance and printing processes for organic transistor-based electronics” *Chem. Mater*. 16, 4748, 2004.

[49] J. A. Rogers, Z. Bao, A. Makhija, and P. Braun, “Printing process suitable for reel-to-reel production of high-performance organic transistors and circuits” *Adv. Mater*. 11, 741, 1999.

[50] H. Sirringhaus, T. Kawase, R. H. Friend, T. Shimoda, M. Inbasekaran, W.Wu, and E. P. Woo, “High-resolution inkjet printing of all-polymer transistor circuits” *Science* 290, 2123, 2000.

[51] H. Klauk, M. Halik, U. Zschieschang, G. Schmid, and W. Radlik, “High-mobility polymer gate dielectric pentacene thin film transistors” *J. Appl. Phys.*, 92, 5259, 2002.

[52] S. J. Zilker, C. Detcheverry, E. Cantatore, and D. M. de Leeuw, “Bias stress in organic thin-film transistors and logic gates” *Appl. Phys. Lett.*, 79, 1124, 2001.

[53] Trznadel, M.; Pron, A.; Zagorska, M.; Chrzaszcz, R.; Pielichowski, “Effect of molecular weight on spectroscopic and spectroelectrochemical properties of regioregular poly(3-hexylthiophene)” *J. Macromolecules*, 31, 5051, 1998.

[54] Mohamed S. A. Abdou, Francesco P. Orfino, Yongkeun Son, and Steven Holdcroft; “Interaction of Oxygen with Conjugated Polymers: Charge Transfer Complex Formation with Poly(3-alkylthiophenes) ” ; J. Am. Chem. Soc., 119, 4518-4524, 1997

[55] A. Dodabalapur, L. Torsi, and H. E. Katz, “Organic transistors: two-dimensional transport and improved electrical characteristics” *Science* 268, 270, 1995

[56] J. Lee, K. Kim, J. H. Kim, and S. Im, " Optimum channel thickness in pentacene-based thin-film transistors" *Appl. Phys. Lett.* 82, 4169, 2003.

[57] M. Kiguchi, M. Nakayama, K. Fujiwara, K. Ueno, T. Shimada, and K. Saiki, "Accumulation and depletion layer thicknesses in organic field effect transistors" *Jpn. J. Appl. Phys.*, Part 2 42, L1408 ,2003.

[58] H. G. O. Sandberg, G. L. Frey, M. N. Shkunov, H. Sirringhaus, and R. H. Friend, "Ultrathin regioregular poly(3-hexyl thiophene) field-effect transistors" *Langmuir* 18, 10176 , 2002.

[59] H. Sirringhaus, N. Tessler, and R. H. Friend, "Integrated optoelectronic devices based on conjugated polymers" *Science* 280, 1741, 1998.

[60] A.Salleo, M. L. Chabinyc, M. S. Yang, and R. A. Street, "Polymer thin-film transistors with chemically modified dielectric interfaces" *Appl. Phys. Lett.* 81, 4383 , 2002.

[61] H. Sirringhaus, N. Tessler, and R. H. Friend, "Integrated optoelectronic devices based on conjugated polymers" *Science* 280, 1741, 1998.

[62] K. P. Pernstich, S. Haas, D. Oberhoff, C. Goldmann, D. J. Gundlch, and B. Batlogg, A. N. Rashid, and G. Schitter, "Threshold voltage shift in organic field effect Transistors by dipole monolayers on the gate insulator," *J. Appl. Phys.*, vol. 96, No. 11, pp. 6431-6438, Dec., 2004.

簡歷

姓　　名：王祐圻

性　　別：男

出生年月日：民國七十二年六月二十七日

住　　址：台北市士林區中山北路七段 114 巷 33 弄 10-1 號三樓

學　　歷：台北市立建國中學　(87 年 9 月~90 年 6 月)

國立交通大學電子工程學系

(90 年 9 月~94 年 6 月)

國立交通大學電子研究所碩士班

(94 年 9 月~96 年 7 月)

論文題目　：結構化高分子薄膜電晶體之製程開發與電特性分析之研究

Study on the Process Development and Electrical Characterization of the Patterned Polymer Thin-Film Transistors