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碩 士 論 文

寬頻矽基板覆晶片結構及低功率基底趨動混頻器之設計

Design of Broadband Si Carrier Flip-Chip Structure and Low-Power Bulk-Driven Mixer

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寬頻矽基板覆晶片結構及低功率基底趨動混頻器之設計

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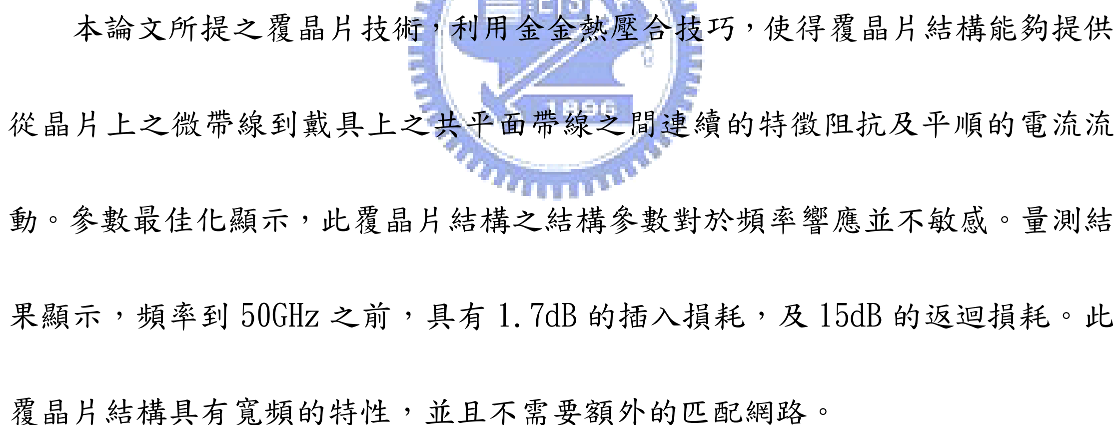
摘要

本篇論文提出一個適用於毫微米波頻段之無凸塊覆晶片結構，以及高效能、低功率射頻積體電路之設計。



本論文所提之覆晶片技術，利用金金熱壓合技巧，使得覆晶片結構能夠提供從晶片上之微帶線到戴具上之共平面帶線之間連續的特徵阻抗及平順的電流流動。參數最佳化顯示，此覆晶片結構之結構參數對於頻率響應並不敏感。量測結果顯示，頻率到 50GHz 之前，具有 1.7dB 的插入損耗，及 15dB 的返迴損耗。此覆晶片結構具有寬頻的特性，並且不需要額外的匹配網路。

電壓控制振盪器之設計，乃利用該覆晶片技術，整合微機電之高品質因素電感，及 CMOS 晶片，分別設計二個操作於 5GHz 之電壓控制振盪器，以達成低功率，高效能的目的。其中一個電壓控制振盪器，設計為具有高的優劣評比，在功率消耗僅 1.03mW 情況下，其優劣評比為 191.2dB，頻率調整範圍為 7.9%；另一個電壓控制振盪器，設計為具有寬的頻率調整範圍，在功率消耗僅為 1.08mW 情況下，

其頻率調整範圍為 20.2%，優劣評比為 188dB。操作電壓皆為 1V。

混頻器之設計，應用於無線近身網路，乃利用 LO 基底趨動之電路架構，結合切換級及轉導級於單一顆電晶體，以達成低電壓，電功率之目的。並且利用變形之 Volterra 級數進行基底趨動混頻器之最佳化設計，發現電壓轉換增益和三階互調乘積的本質來源分別源自於二階和四階非線性電流。量測結果顯示，當基底趨動混頻器操作於 1.4 GHz 及 1V 之操作電壓下，具有 16dB 的電壓轉換增益，-0.5dBm 的第三階交會點，18.1dB 的返迴損耗，及 19.65dB 的雜訊指數，其等待功率消耗為 0.25mW，操作功率消耗為 0.69mW。

Design of Broadband Si Carrier Flip-Chip Structure and Low-Power Bulk-Driven Mixer

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ABSTRACT

This thesis proposes designs of a bump-less flip-chip structure applicable to millimeter-wave frequency, and radio frequency (RF) integrated circuit with low power and high performance.

The proposed flip-chip structure using Au-Au thermo-compression technique to make the flip-chip structure provides continuity of characteristic impedance from the on-carrier CPW line to the on-chip microstrip line, as well as smooth current flow. Parameter optimization further indicates that the structural parameters in transition are insensitive to the frequency response. Measurement results show that return loss is better than 15dB and insertion loss smaller than 1.7dB up to 50GHz. The transition structure has broadband performance without any external matching network.

Flip-chip technique is employed to integrate with high-quality (Q) MEMS inductor and CMOS chip to design two VCOs operating in 5 GHz for the purpose of high performance and low power consumption. One of the two VCOs is designed with high figure-of-merit (FOM). Under power consumption of 1.03mW, the VCO has FOM of 191.2dB and tuning range of 7.9 %. The other is designed in wide tuning range. The VCO has tuning range of 20.2% and FOM of 188dB consuming only

1.08mW. The supply voltage is 1V in these two VCOs.

As for mixer design at the application of wireless body area network (WBAN), a bulk-driven architecture is adopted to merge switching stage and transconductance stage into a single transistor for the objectives of low voltage and low power operation. Variant Volterra series is also used for the optimization of bulk-driven mixer. The insight of nonlinear operation of bulk-driven mixer is gained that the intrinsic conversion gain and the third-order inter-modulation product (IM3) originate from the second-order and fourth-order nonlinear currents, respectively. The bulk-driven mixer operates in 1.4 GHz under supply voltage of 1V. The measurement results show that the voltage conversion gain is 16dB, the input return loss is 18.1dB, the IIP3 is -0.5dBm, and the NF (DSB) is 19.65dB. The power consumption is 0.25mW in standby mode and 0.69mW in operating mode.

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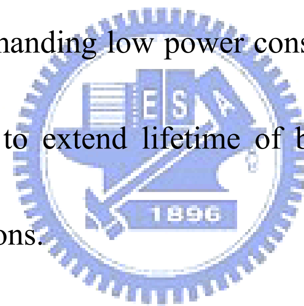
Chapter 1

Introduction

1.1 Motivation

The growing demand of wireless communications has driven many emergent commercial applications. The trend of RF front-end circuit design for these applications is leading to Silicon (Si) CMOS technology for low cost. Much attention is paid to the applications demanding low power consumption, such as wireless body area networks (WBAN) [1], to extend lifetime of battery. Besides, supply voltage shall be low in these applications.



Although CMOS technology has an advantage of low cost, its silicon substrate is very lossy so that it is hard to build on-chip passive components with high-quality. To tackle the issue of Si lossy substrate, the System-on-Package (SoP) technique has been very attractive [2]. Fig. 1.1 demonstrates the SoP technique. Instead of building everything on a single chip, modules of RF transceiver components are designed and fabricated in separate dies, and then fully integrated onto a single carrier as a multi-chip module. SoP also integrates high-quality passive components, such as high Q MEMS inductor, filter, and antenna, onto the carrier. Using Si substrate can low

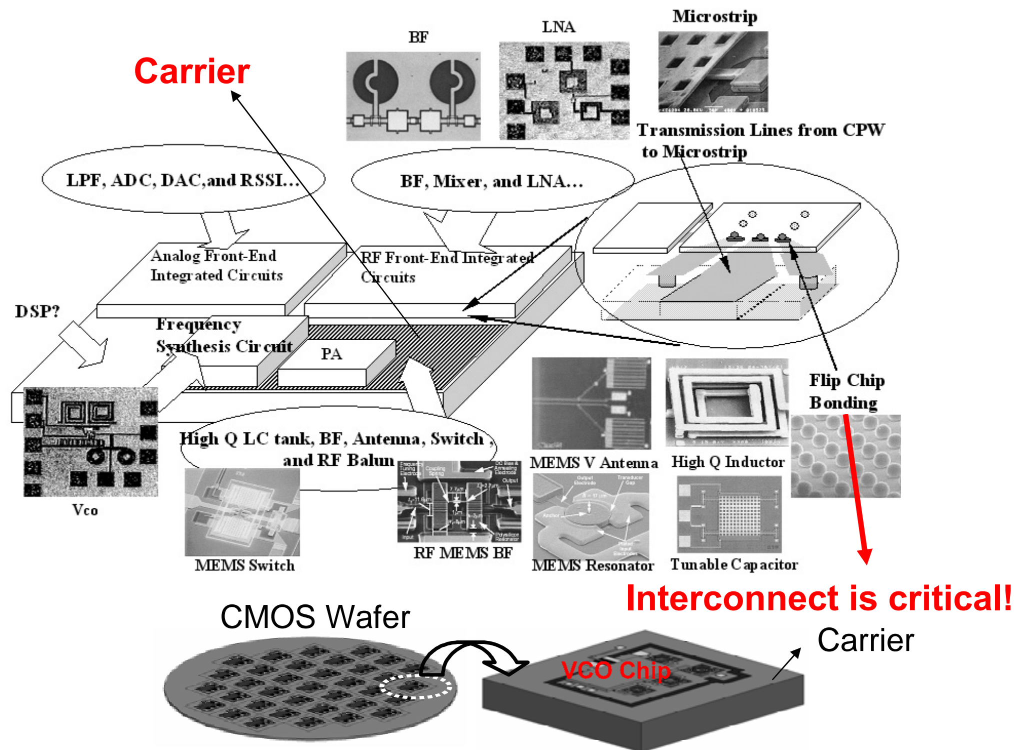


Fig. 1.1. SoP solution.

down the cost and increase the circuit integration.

The most essential part of SoP is the flip-chip interconnection between the CMOS chip and the carrier. This transition structure shall have good return loss and low insertion loss covering a wide-frequency range so that it does not influence CMOS chip performance. This thesis proposes the design of a bump-less broadband flip-chip transition structure for high frequency applications. Its electrical performance is tested by connecting transmission lines on a Si carrier and on a chip circuit fabricated in a standard 0.18μm CMOS process. Chip-carrier assembly is realized by Au-Au thermal compression bonding. With near zero bump height, the impedance variation is so small that the structure provides very good interconnection of good return loss and

low insertion loss.

On-chip inductor is a key passive component in VCO design. However, the lossy substrate degrades the quality factor (Q) of an on-chip inductor. Hence VCO using an on-chip inductor usually consumes large power to compensate the loss from LC tank. To conquer the lossy substrate, we use the SoP technique to integrate CMOS technology with high-Q MEMS inductors to design two VCOs operating in 5GHz. Thanks to the high-Q MEMS inductor, the VCOs feature in high performance under low power consumption.

Gilbert mixer is usually used to down-convert RF signal to intermediate frequency (IF) in low-IF receiver. However, with the fast development of CMOS technology, the supply voltage is reduced to lower level. This reduction of supply voltage makes the Gilbert mixer hard to realize because of stack-up of two transistors. In order to operate in low supply voltage, mixer with cascode topology should be avoided. A good candidate for low voltage operation is the bulk-driven mixer which takes the advantage of MOSFET with inherent four terminals [3]. The bulk-driven mixer can then be used at the application of WBAN, which demands low supply voltage and low power consumption.

The thesis proposes a low power and low voltage bulk-driven mixer demonstrating high conversion gain and good linearity for the application of wireless body area

network (WBAN). Volterra series is used to analyze the nonlinearity of bulk-driven mixer. The insight of nonlinear operation of bulk-driven mixer is gained that the mixer belongs to the type of weakly nonlinear mixer. This insight is different from the prior arts claiming that bulk-driven mixer is a type of switching mixer [4-6]. The individual contribution from each nonlinear source to conversion gain and linearity is obtained to decide the optimal bias condition while the trade-off between conversion gain and linearity is taken into account.

1.2 Thesis Organization

In Chapter 2 we discuss the design of broadband flip-chip interconnect for millimeter-wave Si carrier system-on-package. This discussion includes transmission line design, transition structure design, calibration method, and the measurement results.

In Chapter 3 two VCOs are designed by using the SoP technique to integrate a CMOS chip with a high-Q MEMS inductor. The design procedure of MEMS inductor and VCOs, simulation result, and measurement consideration are discussed.

In Chapter 4 low power and low voltage bulk-driven mixer is designed. This chapter includes the overview of the fundamental of nonlinearity analysis using variant Volterra series, comparison of simulation results and calculation results, individual nonlinear contribution, how to decide the optimal bias condition, input

matching mechanism, bias circuit, and measurement results.

Finally Chapter 5 is the conclusion and future work.

Chapter 2

Broadband Flip-Chip Interconnect for Millimeter-Wave Silicon Carrier System-on-Package

2.1 Introduction

In the development of advanced microwave and millimeter-wave systems, the interconnect design is an essential part of the system electrical performance. As far as circuit design is concerned, the interconnection shall provide good return loss and low insertion loss over the signal frequency range. Of the available multi-chip packaging techniques, the flip-chip technique appears better than the wire-bonding technique for microwave and millimeter-wave packaging due to less and more reproducible parasitic effects [7]. It has been shown in numerous articles that the electrical performance of the conventional wire bond leads to an increase in return loss and insertion loss as the frequency or interconnection distance is increased. The flip-chip interconnect is often employed for connection because of the advantages of low parasitic element since the short interconnection length, the low assembly cost, and

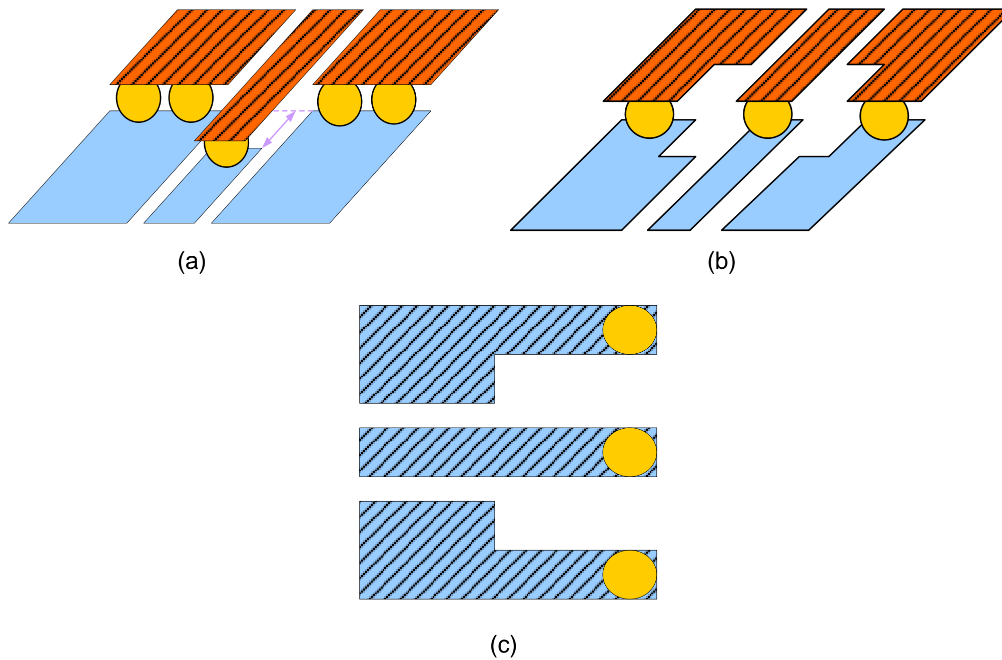


Fig. 2.1. The transition structures: (a) staggered bumps. (b) locally matching technique. (c) high impedance compensation.

the high reproducibility, as compared to the conventional wire bond. When the flip-chip technology is used, there are two main issues that determine the characteristics of a flip-chip monolithic microwave integrated circuit (MMIC): detuning of the circuit on chip due to its proximity to the motherboard and the reflection at the bump interconnect.

Most flip-chip technology adopts a soldering bump structure [8, 9]. Signal propagation inevitably encounters discontinuity. Operated at low frequencies, the flip-chip interconnect can be still considered as a simple transition of no significant impact on electrical performance in terms of return loss and insertion loss. This gives great freedom to circuit design and system integration. As to the millimeter-wave spectrum, it occurs that any discontinuity must be well taken into account with careful

modeling on parasitic and incorporated into circuit design.

Many transition structures have been proposed for the design at millimeter-wave frequency, like those as shown in Fig. 2.1[9-11]. The basic idea is that of compensation, i.e., reducing parasitic capacitance at the transition by adding an inductive counterpart. Three approaches are investigated here: staggered bumps, a locally matching technique, and an on-carrier solution employing a high-impedance line section. As to the staggered bumps in Fig. 2.1(a), compensation is achieved by staggering center conductor and ground bumps. The center conductor of the chip is elevated and the field concentrated in the air region, which leads to a decrease in capacitance. The clear disadvantage, however, is that the interconnection now consumes additional expensive chip area. Moreover, this approach is not compatible with common chip layouts, but requires a customized chip design. In brief, this approach is effective, but not generally recommendable.

Fig. 2.1(b) shows the locally matching technique. The ground conductor is retreat by Δ to reduce the parasitic capacitance. The typical value of Δ for good return loss is around 100um which increase the chip area, and thus raise the cost.

In the case of the high impedance compensation technique as indicated in Fig. 2.1(c), it is clear that the return loss is improved at low frequency band only. The high impedance line which contributes more parasitic inductance will degrade the high

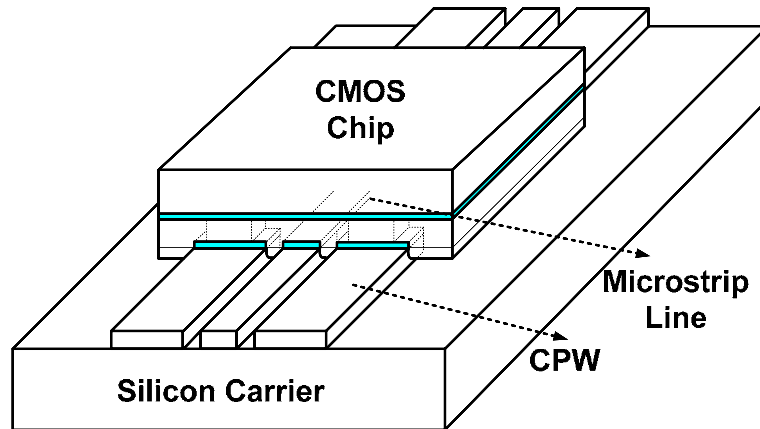


Fig. 2.2. The test structure for characterization of the proposed bump-less flip-chip transition from CPW line on the Si carrier to microstrip line on the chip fabricated in a standard 0.18 um CMOS process.

frequency performance, that is, it is usually narrow band in principle.

These three compensation techniques require impedance matching to compensate the parasitic inductance and capacitance due to the soldering bump and the bumping pad, respectively. Nevertheless, matching optimization causes much time consumption and very often limited bandwidth. In this chapter, bump-less flip-chip interconnect by using Au-Au thermo-compression technique for the applications at millimeter-wave frequency band is discussed. This flip-chip interconnect has the advantages of easy design, no external matching network, small area, and broadband performance.

2.2 CPW to Microstrip Line Transition Structure Design

Transition of CPW to microstrip line is widely used in packages, on wafer measurement of microstrip based MMIC, and it also interconnects in hybrid circuits

including both microstrip and CPW. So CPW to microstrip line transition is adopted to test the bump-less flip-chip technology up to millimeter-wave frequency. The test structure as shown in Fig. 2.2 is designed connecting transmission lines, a microstrip line fabricated in a 0.18 μm CMOS chip and two CPW lines built on a silicon carrier. Bump-less contacts apply Ni/Au deposited layers for chip bonding. In this design, EM signal will be transmitted from one CPW line on the silicon carrier to the other via two flip-chip interconnects and the microstrip line. Essentially this might be considered as the worst scenario of possible transitions. As signal loss through the microstrip line is very low, the symmetric structure design provides a full investigation on the electrical performance of the flip-chip interconnects.

2.2.1 Transmission Line Design

The design target of a transmission line is to decide the physical dimension corresponding to 50Ω characteristic impedance for the measurement purpose.

(i) Microstrip Line

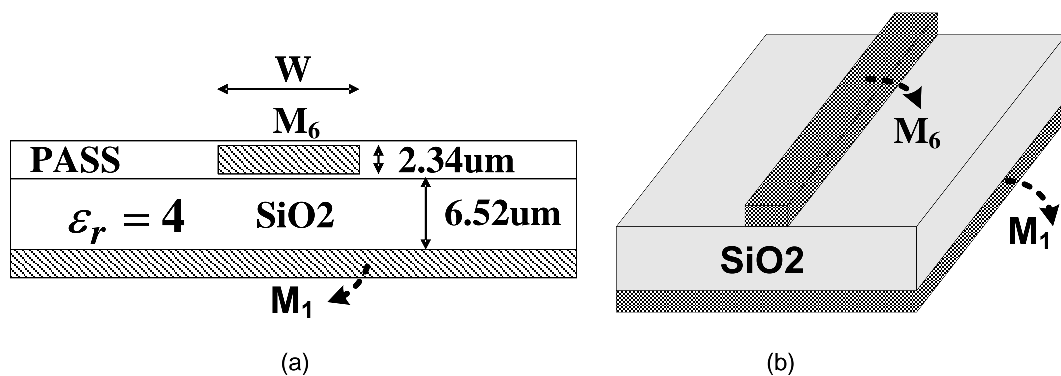


Fig. 2.3. The microstrip line structure in standard 0.18um CMOS technology, (a) cross-section view. (b) top view.

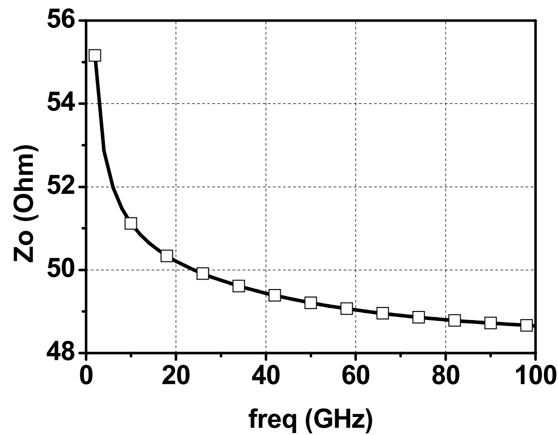
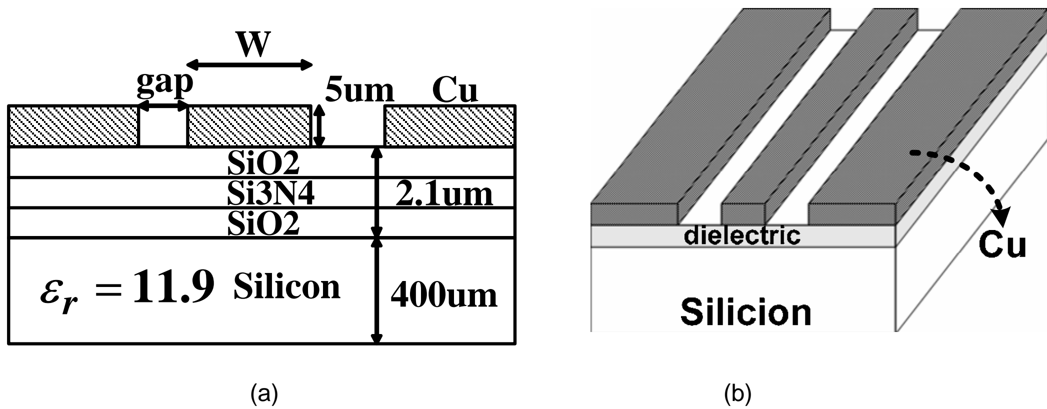


Fig. 2.4. Frequency response of characteristic impedance of the microstrip line.

Fig. 2.3 shows the cross-section view and top view of a microstrip line fabricated in standard 0.18um 1P6M CMOS technology. The microstrip line consists of the top metal layer (M_6) as the signal line and the bottom metal layer (M_1) as the ground plane. The only adjustable parameter is the center width of signal line which is set as 10.5um to obtain 50Ω characteristic impedance. The EM simulation result of Zo versus frequency is shown in Fig. 2.4. As indicated from the plot, Zo is dispersive at low frequency range. This phenomenon can be understood from the equation of characteristic impedance, (2-1). It is found that dispersion in low frequency is caused by the existent dielectric loss and the conductor loss. If the dielectric and conductor is perfect, i.e. no loss, the characteristic impedance will remain constant over the signal frequency. Although Zo deviates from 50Ω at low frequency, this does not mean that return loss degrades too. Keep in mind that the S parameter is defined for an infinite transmission line.



(a) (b)

Fig. 2.5. The CPW structure in carrier. (a) cross-section view (b) top view.

$$Z_o = \sqrt{\frac{R + jwL}{G + jwC}} \tag{2-1}$$

(ii) Coplanar Waveguide (CPW)

The cross-section view and top view of a CPW are shown in Fig. 2.5. The CPW consists of three conductors which center metal is signal line and the other two are ground layer. The CPW metal is made of electroplated Cu of 5um thickness. The design parameters for 50Ω line impedance are the width of center metal and the gap between signal line and ground line. The signal width is set as 10.5 um, the same as the signal width of microstrip line, to have continuous line impedance at the transition. Hence the only changeable parameter is the dimension of the gap. “gap” is set as 7.2um to have 50Ω characteristic impedance. The simulation result of Zo is shown in Fig. 2.6 which indicates that Zo at high frequency is not close to 50Ω. It is since an error in simulation setup, but this does not affect the return loss too much. After removing the error in setup, the gap ought to be 8um to own 50Ω line impedance.

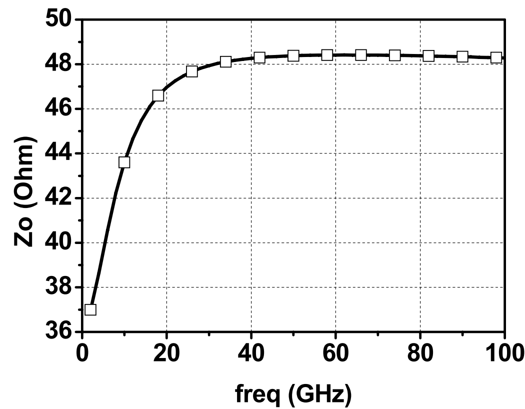


Fig. 2.6. Frequency response of characteristic impedance of the CPW.

The frequency dependence at low frequency is different from the case in the microstrip line. This is since that the conductor loss is greater than the dielectric loss at low frequency in microstrip line; however, in the CPW, the loss from silicon substrate is larger than the conductor loss. Consequently, from (2-1), the Zo of the microstrip line and the CPW will approach infinity and zero, respectively, at zero frequency.

2.2.2 Transition Structure Design

After decision of the physical structure of the microstrip line and the CPW, the transition of CPW to microstrip line needs to be carefully designed to have continuous electromagnetic filed and smooth current flow. The grounds are designed in the shape as shown in Fig. 2.7. The connection of ground references also goes through the M6 metal as the chip is flipped. Vias are therefore required to connect the M6 ground pads to the M1 ground layer in the microstrip line on the CMOS chip. Those ground pads

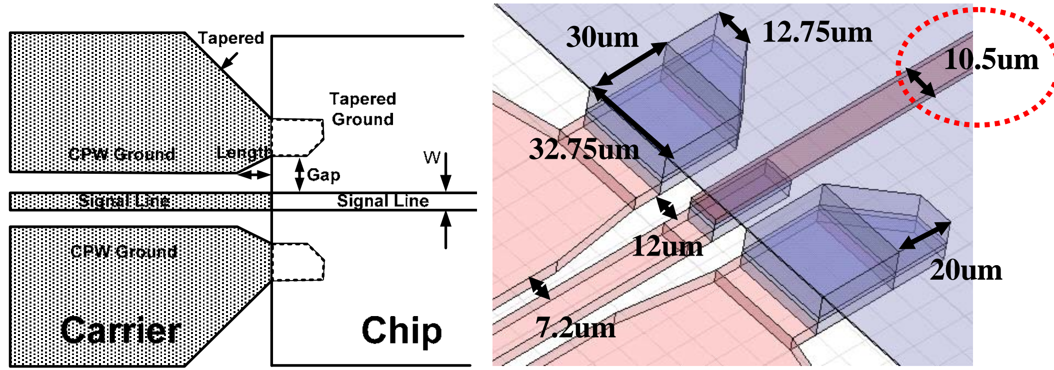


Fig. 2.7. Top view of the transition structure from CPW to the microstrip line. The electrical performance is evaluated by sweeping the parameters, Gap and Length, by an EM simulator.

not only provide the connection but also strengthen mechanical joint. Although near-zero bump height provides smooth transition between two transmission signal lines, inevitable structural discontinuity still exists which would result in extra power loss due to the formation of different propagation modes. Furthermore, the physical discontinuity in the transition between the microstrip and the CPW lines would also raise leading reactive effects which will increase the return loss and insertion loss of signal transmission at high frequencies.

In order to mitigate the problem, the M6 ground pads are selected in a tapered trapezoidal shape and placed in some distance from the signal line to avoid extra capacitive coupling between the microstrip line and the reference ground. The shape of CPW grounds is also tapered near the interface to have better smooth current and continuous filed distributions in order to reduce signal power loss. The parasitic inductances due to current crowding in the ground pads help compensate the parasitic capacitance so that the overall line impedance can still keep on the 50Ω. It is

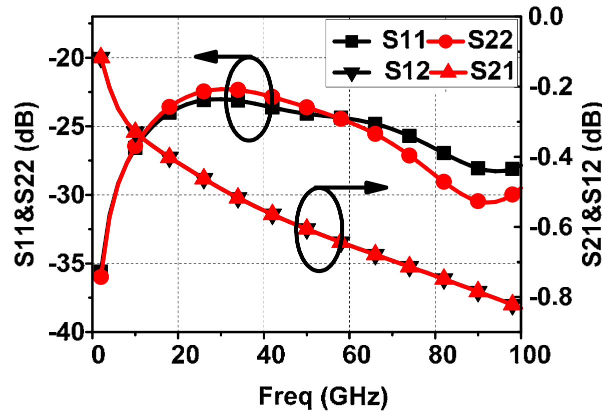
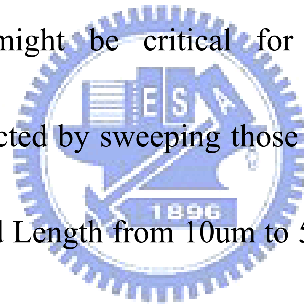


Fig. 2.8. HFSS simulation results of the test structure. The reference plane is de-embedded to the location as shown in Fig. 2.20, the same as that in TRL measurements.

understood that those two parameters of the distance between the signal line and the M6 ground pads of the microstrip line, Gap, and the distance from the tapered corner to the interface, Length, might be critical for good transition performance. Simulations have been conducted by sweeping those two parameters for the value of Gap from 7.2um to 12um, and Length from 10um to 50um. It turns out that the return loss under all conditions varies only within a limited level over the frequency up to 80GHz. This indicates the great advantage of the proposed chip assembly technique that it provides easy transition design for very high-frequency applications. In this design, the Gap and Length geometric parameters are chosen as 12um and 40um, respectively, such that the return loss is the best result of the simulated cases. The tapered angle is therefore around 6.8 degrees. Fig. 2.8 is the plot of the simulation results by HFSS EM simulator, showing the transition structure including two transitions and one microstrip line can provide better than 23dB return loss and 0.9 dB



insertion loss up to 100GHz.

2.2.3 Detuning Effect

Although the bum-less flip-chip interconnect can provide good electric performance, the detuning effect should be carefully concerned if there are reactive components in the CMOS chip. The detuning effect that any circuit on the chip might be affected by the additional lossy substrate or metal on the Si carrier in close vicinity after the chip is flipped and mounted. Since the bump height is near zero in this technique, there exists only thin passivation and air between the chip circuit and the substrate. The circuit electrical performance might be detuned significantly. As to the microstrip line in the flipped condition as shown in Fig. 2.9, the carrier substrate causes extra distributed capacitance and the line impedance is expected to be lower. EM simulations help characterize the detuning effect and the results are shown in Fig.

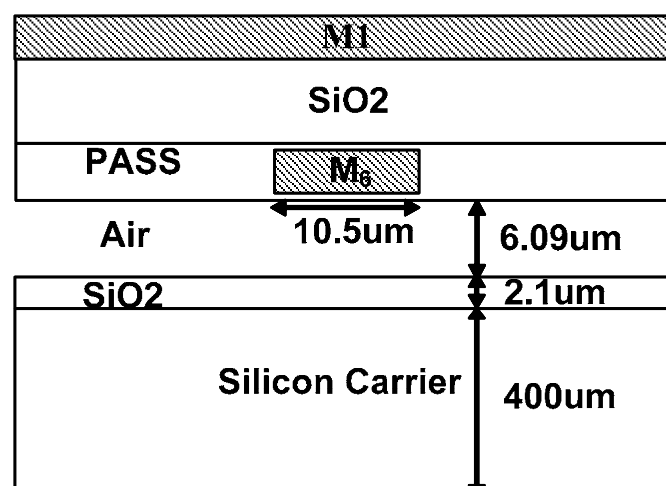


Fig. 2.9. The microstrip line in flipped condition. The silicon carrier detunes the characteristic of the microstrip line.

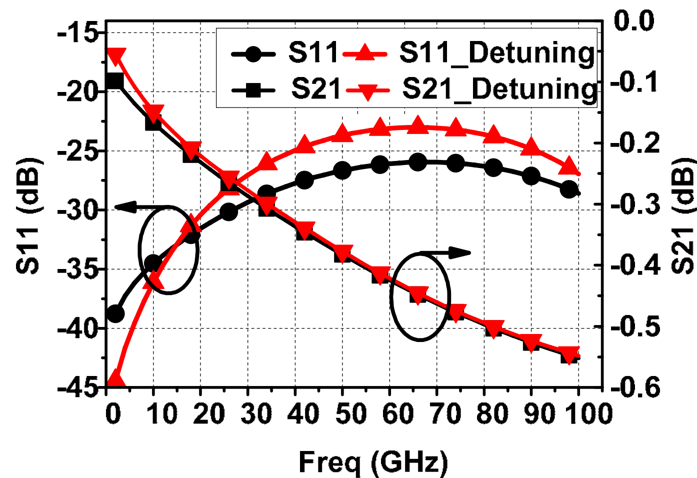


Fig. 2.10. Analysis of detuning effect of the microstrip line under consideration indicates that the line impedance is deviated around 2-Ω.

2.10. The simulation results tell that although the return loss is somewhat degraded, it is still better than 23dB up to 100 GHz. Further study indicates that the line impedance deviates about 2-Ω.

2.2.4 Calibration Method

To measure the device under test (DUT), cables and high frequency probes are inevitably used to link the DUT to equipment. Besides, the Ground-Signal-Ground (GSG) pad is placed to connect the DUT so that it is possible to make an on-wafer measurement. These interconnections and pads contribute undesired loss and phase delay so they will impact the accuracy of DUT measurement. Consequently, calibration is required to remove these non-ideal effects. THRU-RELECT-LINE (TRL) calibration and multi-line de-embedding method are used to characterize the flip-chip interconnection. The major difference of these two methods is the system

characteristic impedance for measurement which is frequency dependent in TRL and fixed to 50Ω for multi-line de-embedding method.

(i) TRL Calibration Method [12, 13]

TRL calibration is most often performed when a high level of accuracy is demanded. It does not have calibration standards in the same connector type as the DUT and the standards are easy to manufacture and characterize. Block diagram shown in Fig. 2.11 represents general measurement setup. These non-ideal effects are lumped together in a two-port error box in Fig. 2.11. So a calibration procedure is needed to characterize the error box. The TRL calibration does not rely on known standard loads, but uses three simple connections to characterize the error box

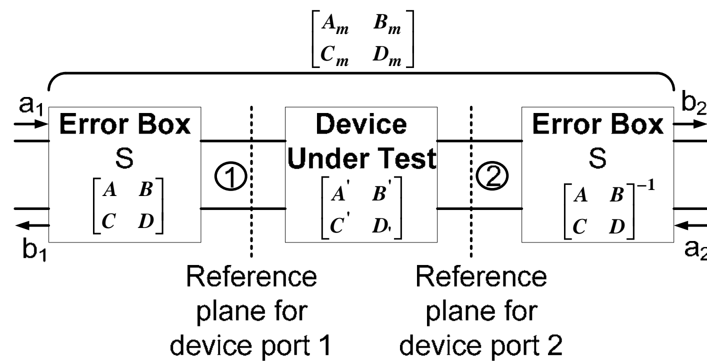


Fig. 2.11. Block diagram of a general measurement setup.

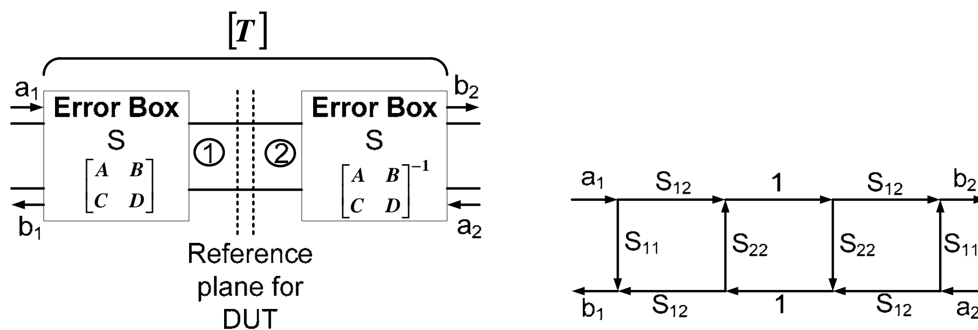


Fig. 2.12. Block diagram and signal flow graph for the THRU connection.

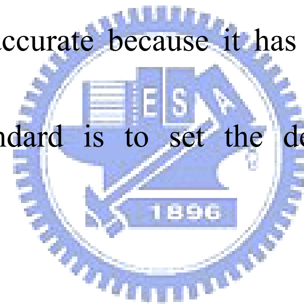
completely. These standards are THRU, REFLECT, and LINE.

Fig. 2.12 shows the block diagram and signal flow graph for THRU connection. Using basic decomposition rules we can get the S-parameters at the measurement plane in terms of S-parameter of the error box, as indicated in (2-2) and (2-3).

$$T_{11}=\left.\frac{b_1}{a_1}\right|_{a_2=0}=\frac{S_{11}(1-S_{22}^2)+S_{12}^2S_{22}}{1-S_{22}^2}=S_{11}+\frac{S_{12}^2S_{22}}{1-S_{22}^2}=T_{22} \tag{2-2}$$

$$T_{12}=\left.\frac{b_1}{a_2}\right|_{a_1=0}=\frac{S_{12}^2}{1-S_{22}^2}=T_{12} \tag{2-3}$$

By symmetry and reciprocity, we have $T_{22}=T_{11}$ and $T_{21}=T_{12}$, respectively. A zero-length THRU is more accurate because it has zero loss and no characteristic impedance. The THRU standard is to set the desired reference plane for the measurement.



The reflect connection is shown in Fig. 2.13. The arrangement effectively isolate the two measurement ports, so that $R_{12}=R_{21}=0$. The signal graph can be easily reduced to show that

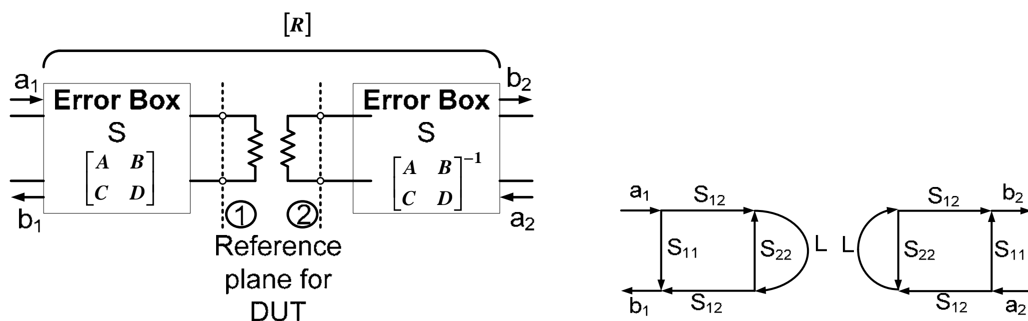


Fig. 2.13. Block diagram and signal flow graph for the REFLECT connection.

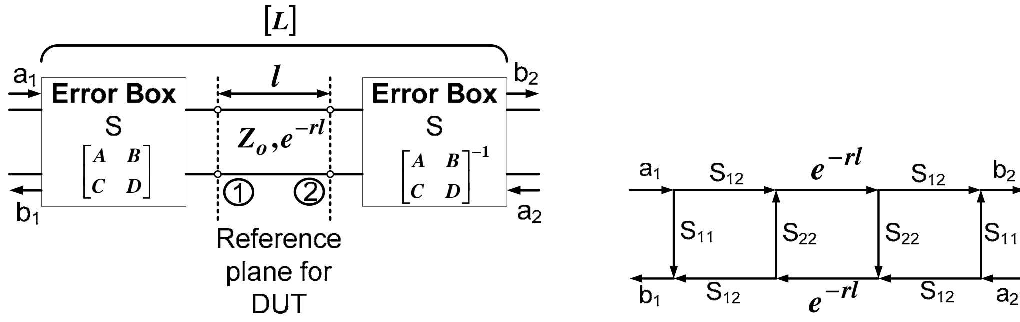


Fig. 2.14. Block diagram and signal flow graph for the LINE connection.

$$R_{11}=\frac{b_1}{a_1}\bigg|_{a_2=0}=S_{11}+\frac{S_{12}^2\Gamma_L}{1-S_{22}\Gamma_L}=R_{22} \tag{2-4}$$

By symmetry we have R_{22}=R_{11}. The Reflect standard can be anything with a high reflection, such as open or short. However, the Reflect standards must have same Γ, reflection coefficient, on both test ports.

Fig. 2.14 shows the Line connection. The signal graph can show that

$$L_{11}=\frac{b_1}{a_1}\bigg|_{a_2=0}=S_{11}+\frac{S_{22}S_{12}^2e^{-2\gamma l}}{1-S_{22}^2e^{-\gamma l}}=L_{22} \tag{2-5}$$

$$L_{12}=\frac{b_1}{a_2}\bigg|_{a_1=0}=\frac{S_{12}^2e^{-2\gamma l}}{1-S_{22}^2e^{-\gamma l}}=L_{21} \tag{2-6}$$

By symmetry and reciprocity we have L_{22}=L_{11} and L_{21}=L_{12}, respectively. The characteristic impedance of line must be of the same impedance as the THRU standard and its length cannot be the same as the THRU standard. The disadvantage of TRL calibration is the limited bandwidth. The LINE standard must be an appropriate electrical length for the frequency range, that is, at each frequency, the phase difference between the THRU and the LINE should be greater than 20 degrees

and less than 160 degrees. This means in practice that a single LINE standard is only usable over an 8:1 frequency range (Frequency Span/Start Frequency). Therefore, for broad frequency coverage, multiple lines are required.

With equations, (2-2 to 2-6), the S-parameter of the error boxes can be derived, as well as unknown reflection coefficient, Γ_L, and the propagation factor, $e^{-\gamma L}$. After the S-parameter of the error box is acquired, the S-parameter is transformed into the transmission matrix so we are able to get the transmission matrix of DUT by (2-7).

$$\begin{bmatrix} A' & B' \\ C' & D' \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}^{-1} \begin{bmatrix} A_m & B_m \\ C_m & D_m \end{bmatrix} \begin{bmatrix} A & B \\ C & D \end{bmatrix}^{-1} \tag{2-7}$$

(ii) Multi-Line De-embedding Method [14]

Any measurement is limited by an inherent flaw due to the test pads and interconnect are required to access the DUT. Multi-line de-embedding method uses two transmission line with different length and its symmetric property to remove the effect of test pad discontinuity.

Consider two transmission line test structure of length l_1 and l_2, where $l_1 < l_2$ (Fig. 2.15). If properly designed, the structures will be symmetric about y axis. Symmetric property means that swapping port 1 and port 2 will not change the resulting S, Z, or Y matrices.

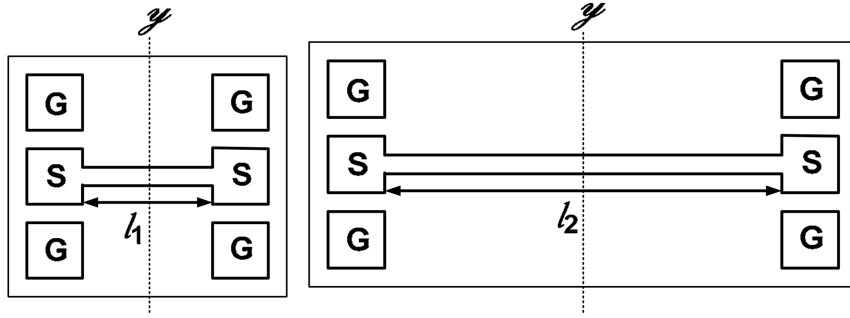


Fig. 2.15. Multi-line for de-embedding.

Swap function swaps port 1 and port 2 as indicated in (2-8).

$$Swap\left(\begin{bmatrix} a_{11} & a_{21} \\ a_{12} & a_{22} \end{bmatrix}\right) = \begin{bmatrix} a_{22} & a_{12} \\ a_{21} & a_{11} \end{bmatrix} \tag{2-8}$$

Transmission line can be decomposed into a cascade of 3 two port network, two pads and intrinsic device. Consequently the transmission matrix of test structure l_i, M^t_{li}, can be represented by the following product:

$$M^t_{li} = M_{P1} M_{li} M_{P2} \tag{2-9}$$

where M_{P1} represents the intrinsic line segment of structure, M_{li} represents the left pad, and M_{P2} represents the right pad. First, multiply M^t_{l2} with the inverse of M^t_{l1}

$$M^h_{l2-l1} \equiv M^t_{l2} \times [M^t_{l2}]^{-1} = M_{P1} M_{l2} M^{-1}_{l1} M^{-1}_{P1} \equiv M_{P1} M_{l2-l1} M^{-1}_{P1} \tag{2-10}$$

where we define M^h_{l2-l1} as the hybrid "structure" and M_{l2-l1} as a line segment of length l_2-l_1. Assuming that the left pad can be modeled as a lumped admittance Y_L, we have

$$M_{P1} = \begin{bmatrix} 1 & 0 \\ Y_L & 1 \end{bmatrix} \tag{2-11}$$

This is referred as a lumped pad assumption. The hybrid structure can be expressed in terms of Y parameters, as a parallel combination of intrinsic transmission line and the parasitic lumped pad.

$$Y^{h}_{l2-l1} = Y_{l2-l1} + \begin{bmatrix} Y_L & 0 \\ 0 & -Y_L \end{bmatrix} \quad (2\text{-}12)$$

Because of symmetry of test structure, we can swap the Y parameters of hybrid structure to remove the contribution from test pad so that we can get the intrinsic Y parameters of transmission line with length l_2-l_1.

$$Y_{l2-l1} = \frac{Y^{h}_{l2-l1} + Swap(Y^{h}_{l2-l1})}{2} \quad (2\text{-}13)$$

Assume the transmission matrix of lossy transmission line can be modeled as

$$M_{l_2-l_1} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}$$

$$= \begin{bmatrix} \cosh\gamma(l_2 - l_1) & Z_C \sinh\gamma(l_2 - l_1) \\ Z_C^{-1} \sinh\gamma(l_2 - l_1) & \cosh\gamma(l_2 - l_1) \end{bmatrix} \quad (2\text{-}14)$$

We can extract the characteristic impedance (Zo) and propagation constant (γ) of the transmission line using

$$Z_C = \sqrt{\frac{B}{C}} \quad (2\text{-}15)$$

$$\gamma = \frac{\cosh^{-1} A}{l_2 - l_1} \quad (2\text{-}16)$$

ABCD parameters of transmission line can be gained by transforming the Y_{l2-l1} into its transmission matrix counterpart. From equation (2-12), the Y_L parameter of

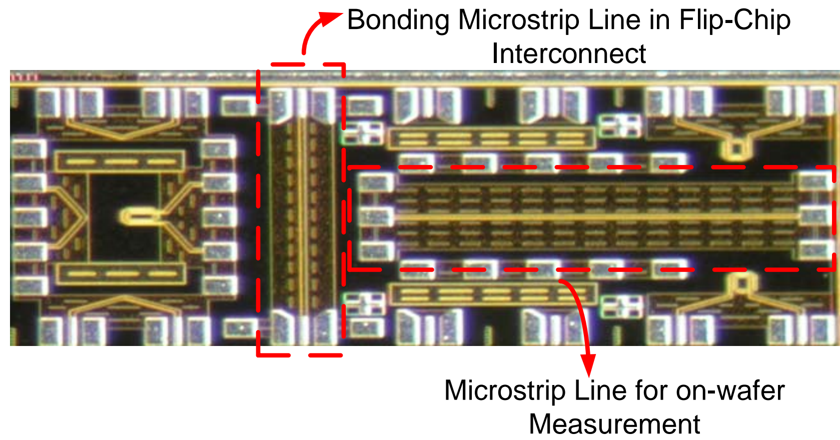


Fig. 2.16. Micrograph of the microstrip line fabricated by standard CMOS 0.18um technology

pad is also easily derived, so is its transmission matrix.

After getting the ABCD matrices of transmission line and pads, ABCD of DUT is then acquired by the following equations where $M_{DUT}^{Measured}$ is obtained after SOLT calibration.

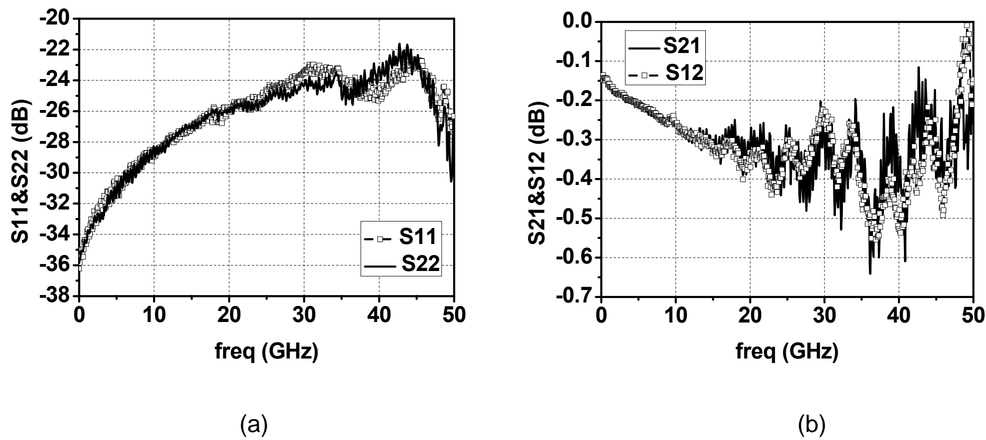
$$M_{DUT} = M_{CPW}^{-1} \times M_{PAD}^{-1} \times M_{DUT}^{Measured} \times M_{PAD}^{-1} \times M_{CPW}^{-1} \qquad (2\text{-}17)$$

2.3 Measurement Results and Discussion

The chip micrograph is shown in Fig. 2.16, including the bonding microstrip line in flip-chip interconnect, a microstrip line for an on-wafer measurement, and other test structure.

2.3.1 Measurement Results of the Microstrip Line

The measurement results of the on-chip microstrip line are shown in Fig. 2.17. The return loss of the microstrip line is kept low over the frequency band. The insertion



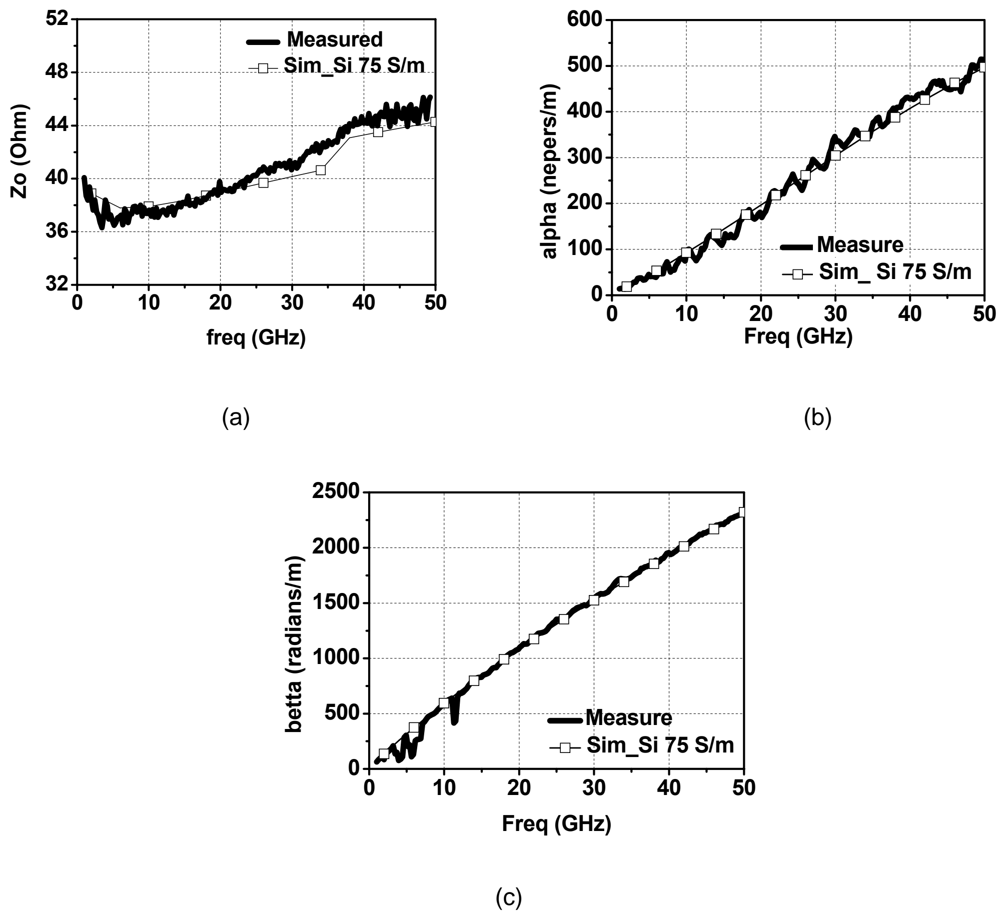
(a) (b)

Fig. 2.17. Measurement results of the microstrip line: (a) return loss. (b) insertion loss.

loss is around -0.4dB up to 50 GHz. The measurement results include the effects of the GSG test pad. This measurement results show that the line impedance of the microstrip line is closed to 50Ω and the line loss is small.

2.3.2 Measurement Results of the CPW

Multi-line de-embedding method is adopted to extract the characteristic impedance and propagation constant of the CPW. The measurement results including characteristic impedance and propagation constant are shown in Fig. 2.18 indicating that the Zo is deviated from 50Ω and more dependent on frequency than the simulation results. This is due to under-estimate the conductivity of silicon substrate. In the initial design, the substrate conductivity is set as 10 S/m. However, if the conductivity is adjusted to around 75 S/m, the simulation results agree well with the measurement results. The deviation of Zo in the CPW will cause serious effects on the TRL measurement because Zo in the measurement system is defined by the line



(a) (b)

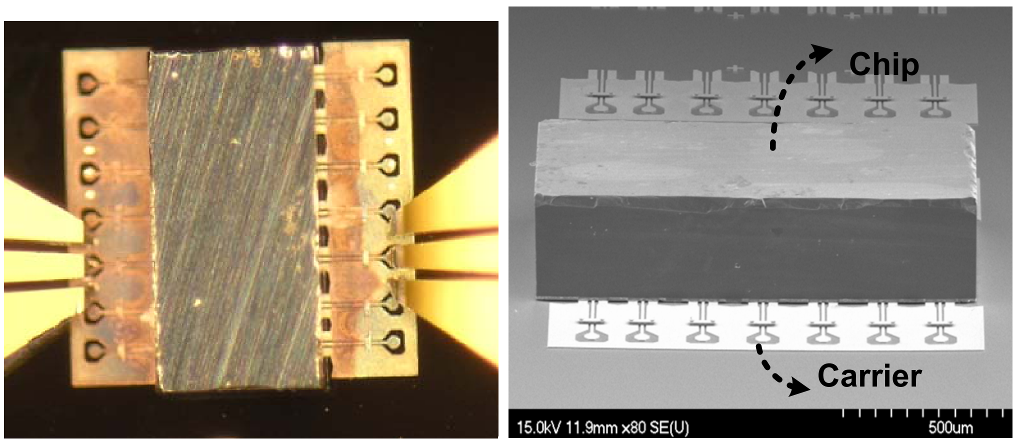
(c)

Fig. 2.18. Measurement results of the CPW: (a) characteristic impedance. (b) alpha (c) beta.

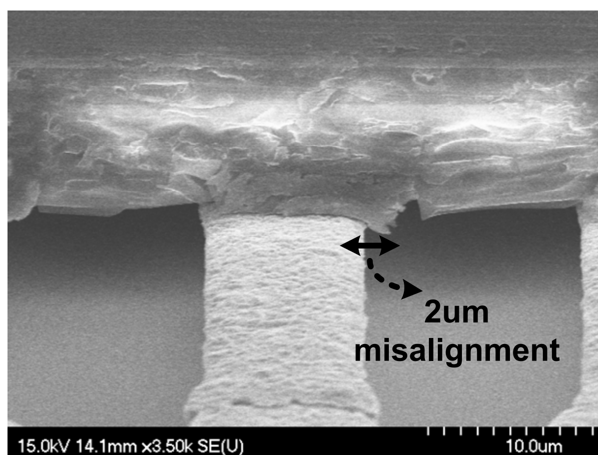
impedance of the CPW. And the higher conductivity of silicon substrate will increase more insertion loss in the flip-chip interconnect.

2.3.3 Measurement Results Using TRL Calibration

Fig. 2.19 shows the SEM pictures of the entire flip-chip structure and the bonding interface. The enlarged SEM picture of Fig. 2.19(c) shows 2μm misalignment in the bonding interface at the transition. It is due to the function loss of interlocking in this case since Zn/Ni/Au layers on the Al pad were over-plated to make its surface above the passivation. The issue can be further resolved with better process control.



(a) (b)



(c)

Fig. 2.19. Pictures of flip-chip structure. (a) on-wafer probing. (b) SEM photo of flip-chip structure. (c) Bonding interface in transition structure shows 2um misalignment.

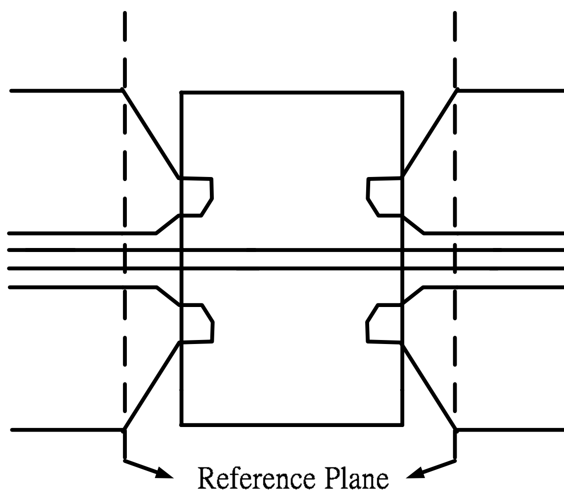


Fig. 2.20. Reference planes of the flip-chip test structure by TRL measurements and EM simulations.

Misalignment may cause some effects in return loss and insertion loss due to local refection in the discontinuity.

On-wafer probing measurements are conducted to characterize the electrical performance of the flip-chip test structure. The TRL calibration technique is applied to move the reference plane of measurement to the location close to the transition interface, as shown in Fig. 2.20. The chip is measured only up to 50GHz due to the equipment limit. The measured data is plotted in Fig. 2.21 showing that the flip-chip interconnects exhibits an insertion loss less than 1.7 dB and a return loss better than 15dB up to 50GHz, including the transmission loss of CPW and microstrip line. The contact resistance of the flip-chip bonding is verified by DC measurement of the test structure. It is as low as 0.7Ω including two CPW lines with the length of 200um, two contact resistances, and one THRU line on the chip. Discrepancy from the simulation results and the measurement results mainly come from the under-estimation of silicon

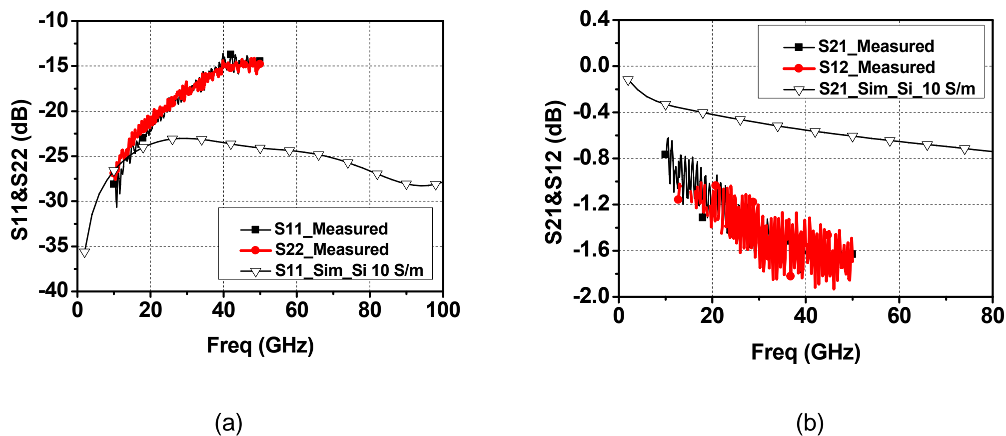


Fig. 2.21. Comparison between simulation and measurement data, (a) return loss and (b) insertion loss. Simulation is based on initial assumption of silicon conductivity of 10S/m.

conductivity in the carrier. The misalignment and the contact resistance in the transition interface may contribute additional insertion loss, which is not included in EM simulation.

2.3.4 Trouble Shooting

As seen in Fig. 2.21, simulation and measurement data appear different levels. After investigations, the difference might be due to two factors, process variation of CPW line and underestimation of its substrate conductivity.

(i) Process Variation

Process variation causes the CPW line width become wider as 11.7um so that the gap size changes to 6.75um which causes Zo deviate from 50Ω. Smaller gap width means higher capacitive coupling between the signal line and the ground line resulting in a lower characteristic impedance. The dependence of Zo on the frequency under

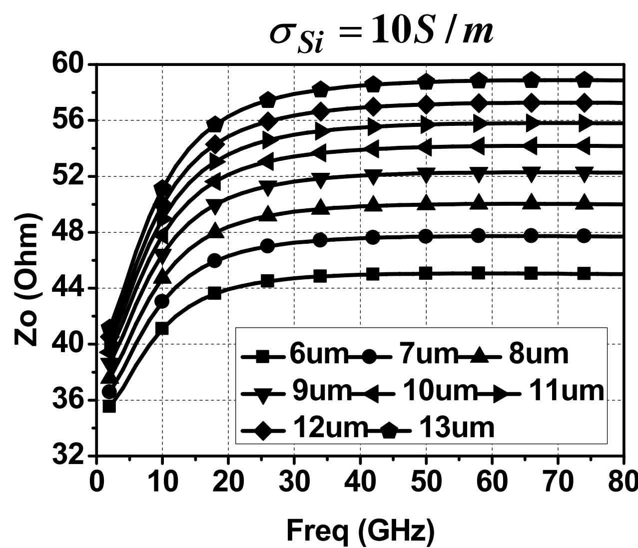


Fig. 2.22. Variation of characteristic impedance of CPW with different gap width.

different gap size as signal width is fixed to 10.5um is shown in Fig. 2.22. This process variation may cause 2~3Ω variation in Zo. This small variation does not affect the return loss too much if the level of Zo is still closed to 50Ω.

(ii) Silicon Conductivity Issue

2~3Ω variation in Zo does not affect the overall response of the flip-chip interconnection very much. The main reason for the discrepancy in Fig. 2.21 is because we under-estimate the silicon conductivity. From the previous discussion of the measurement results of the CPW, the conductivity of the Si substrate is extracted as 75 S/m, much higher than the initial assumption of 10 S/m. This higher silicon conductivity will cause Zo change a lot and become more dispersive. And it also contribute more signal loss to flip-chip interconnect due to the EM fields on the lossy substrate. Zo of the measurement system in TRL calibration is set by the standard of

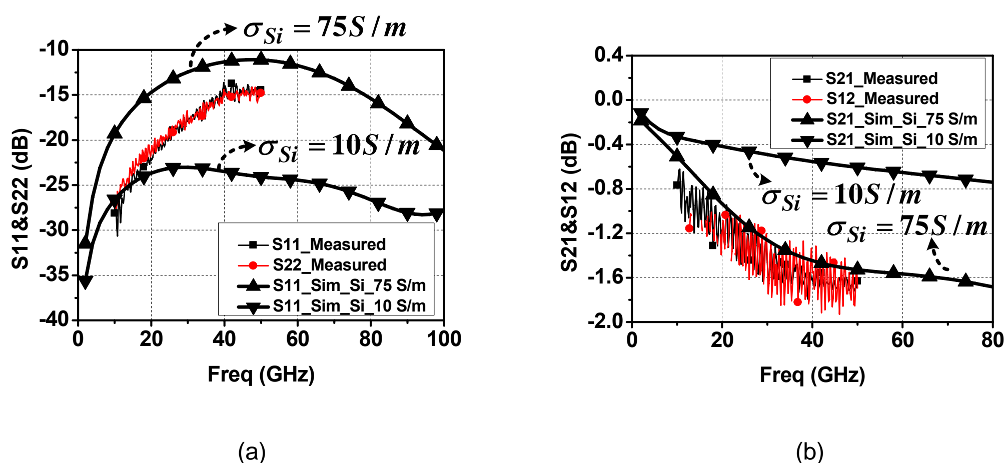


Fig. 2.23. Comparison between simulation and measurement data, (a) return loss and (b) insertion loss. Simulation data with revised the CPW line dimensions and the substrate conductivity (Sx1_Sim_75 S/m Si) agree well with measurement data.

CPW line so that this higher silicon conductivity will cause the TRL measurement results worse. This is because Zo of the CPW is deviated from 50Ω very much, but Zo of the microstrip line is kept around 50Ω. Fig. 2.23 shows the revised simulation results with the silicon conductivity set to 75 S/m. Given the new dimensions and the substrate conductivity, revised simulation data of the insertion loss agree well with measured data. The return loss curves appear in a better similar trend. Nevertheless, the return loss is worse and the insertion loss is higher than the original design.

2.3.5 Measurement Result Using Multi-Line De-embedding Method

Multi-line de-embedding method is also adopted to test the transition structure. The system characteristic impedance is set to 50Ω over the signal frequency, common condition in the S-parameter measurement. The measured data is plotted in Fig. 2.24 showing that the flip-chip interconnects exhibits an insertion loss less than 3 dB and a return loss better than 16dB up to 50GHz, including the transmission loss of

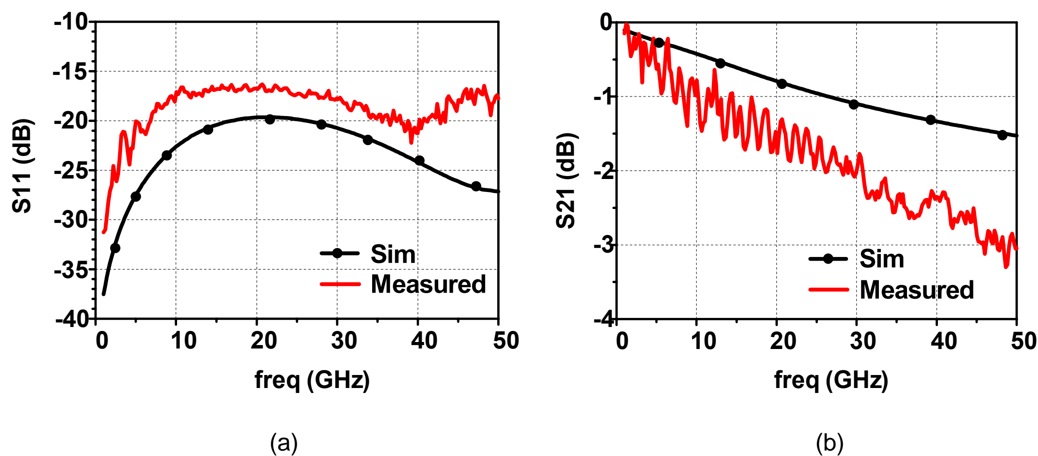
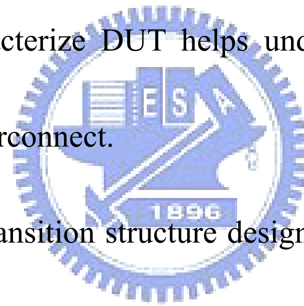


Fig. 2.24. Measurement results using multi-line de-embedding method. (a) return loss. (b) insertion loss.

CPW and microstrip line. The measured insertion loss by multi-line de-embedding method is different from that using TRL calibration. The result using TRL calibration is more reliable than that using multi-line de-embedding method because the reference plane is specifically defined to the place we desired and any non-ideal effect, such as discontinuity of pad, and any interconnects for measurement, can be removed. As for the multi-line de-embedding method, there may be a concern to make a lumped pad assumption in (2-11), especially at high frequency. And the process of calculation may contain numeric errors to impact the final results. However, using more calculation methods to characterize DUT helps understand more on the electrical properties of the flip-chip interconnect.



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In other words, as to the transition structure designed in this chapter, it indeed has good broadband performance for low return loss and low insertion loss suitable for high frequency applications. This structure is easily realized without any external matching network. With good process control and accurate modeling, it is believed that the return loss could be better than 15 dB and the insertion loss could be lower than 2dB up to 100GHz, applicable to millimeter-wave circuits.

Chapter 3

A Low Power 5GHz Voltage-Controlled Oscillator Utilizing SoP Technique

3.1 Introduction

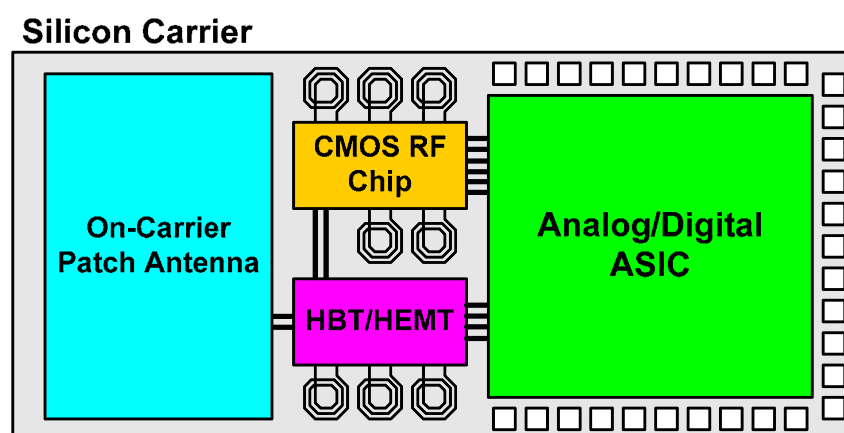


Fig. 3.1. Block diagram demonstrates the integration by SoP technique.

The SoP (System-on-Package) has been attractive for RF circuit and system integration in recent years. As shown in Fig. 3.1, instead of building everything on a single chip, modules of RF transceiver components are designed and fabricated in separate chips, and then fully integrated onto a chip-carrier. Inasmuch as the implementation of high performance active and passive components without having any material and fabrication limitations, a miniaturized RF system can be realized with more design flexibility for better circuit performance.

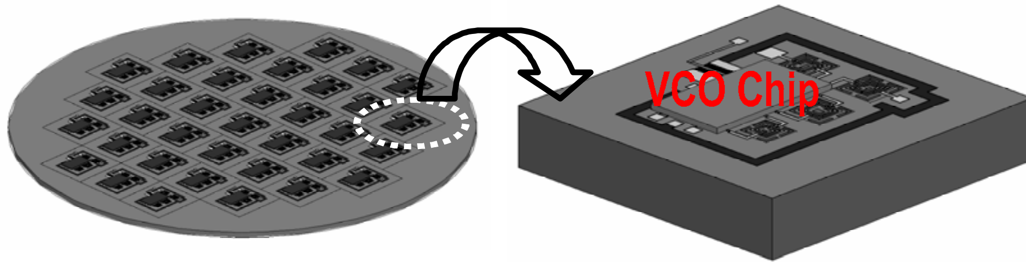


Fig. 3.2. VCO using the flip-chip technique.

This chapter introduces the development of a wafer-level SoP solution for 5GHz VCO using the combination of MEMS and flip-chip packaging technologies as shown in Fig. 3.2. The flip-chip interconnect has been designed and verified by the measurement as discussed in Chapter 2. The core circuit is fabricated in a standard 0.18μm CMOS process. High-performance micromachined inductors are designed, modeled, and fabricated on a silicon substrate, which also acts as a chip-carrier. Chip-carrier integration is realized by Au-Au thermal compression flip-chip bonding, introduce in chapter 3, which provides very good interconnection. On-chip circuit and on-carrier components are co-developed to achieve the required performance. More detailed information about the process and MEMS inductor can be read at [15]. The discussion in this chapter focuses on the VCO circuit design.

3.2 VCO Circuit Design

In the conventional VCO design using on-chip inductor, the VCO usually consumes larger power to compensate the high low from the LC tank. The one the benefits of using MEMS inductor is that we can design the VCO to have the same circuit

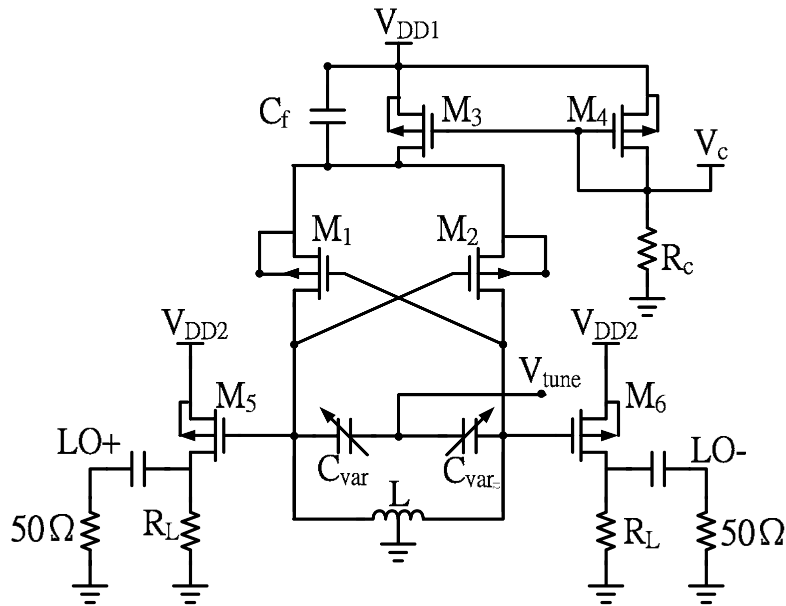


Fig. 3.3. VCO topology using a conventional LC cross-coupled pair. All CMOS transistors are to make VCO have lower flicker noise and thermal noise contributed to the phase noise.

performance under lower power consumption as compared to the VCO using a low-Q inductor. This is because, as shown in Fig. 3.4, the required transconductance can be small to compensate the loss from the MEMS inductor. Besides, the MEMS inductor

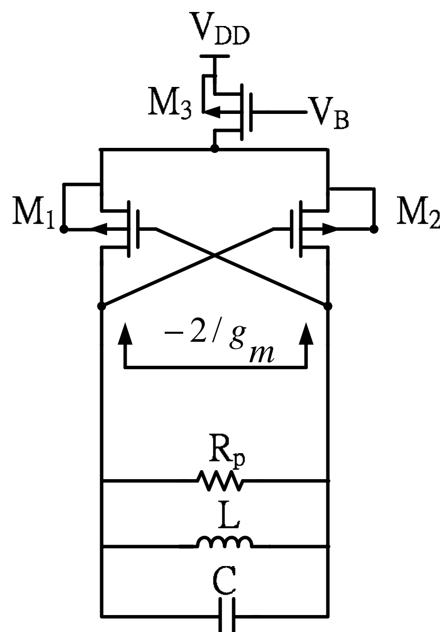


Fig. 3.4. VCO topology using a conventional LC cross-coupled pair.

can still have a high Q even if its inductance value is low. This property of low inductance but still high Q can make us design a width tuning range VCO under low power consumption. So we design two VCOs in this thesis to catch the two benefits discussed above.

One of the two VCOs is designed to feature in high FOM. The FOM is defined in (3-1) where P is the VCO's core power consumption, w_o is the oscillation frequency, Δw is the offset frequency, and $L(\Delta w)$ is the phase noise at the offset frequency of Δw. The fundamental of the phase noise can be seen from Appendix A.

$$FOM = 10\log[(\frac{w_o}{\Delta w})^2 \frac{1}{L(\Delta w)P}] \quad (3\text{-}1)$$

The other is designed to have a high tuning range. All the power consumption of the two VCOs shall be kept low. The VCO topology used to integrate with the MEMS inductor is shown in Fig. 3.3 which is a conventional LC VCO. M_1 and M_2 provide the negative impedance to compensate the energy loss from the LC tank. We adopt a single switching pair to make the VCO be enable to operate at low supply voltage. Choosing PMOS topology is to have lower flicker noise and thermal noise contributing to the output phase noise [16]. M_3 and M_4 compose a current mirror to bias the VCO circuit. Using current mirror for the bias is to make the VCO more robust to process variation. We also add an additional V_c pad if we want to investigate the VCO performance under changes of bias current. M_5 and M_6 are common-source

output buffer used for the measurement purpose.

3.2.1 MEMS Inductor Design Flow

In the first place, we discuss how to design and simulate a MEMS inductor. We make use of Ansoft Designer and HFSS to layout the MENS inductor. Designer and HFSS can export the layout to a gds file. Spectre RF is for the circuit simulation. As shown in Fig. 3.5, the simulation results of inductor are exported as touch stone files (SNp files) which are import to Spectre RF by using an N-port Data item. As to the packaging issue, the package inevitably contributes some parasitic effect which should be included into the simulation. The designed flip-chip interconnect in Chapter2 shows a good return loss at 5GHz. Hence the parasitic effect of the interconnect is small such that the interconnect is likely transparent. We only need to take the contact resistance (~0.3Ω) into account to observe the degradation of Q in the MEMS inductor.

A symmetric inductor with center tap is adopted to give a higher Q and save the chip area. The required inductance value is roughly estimated according to the

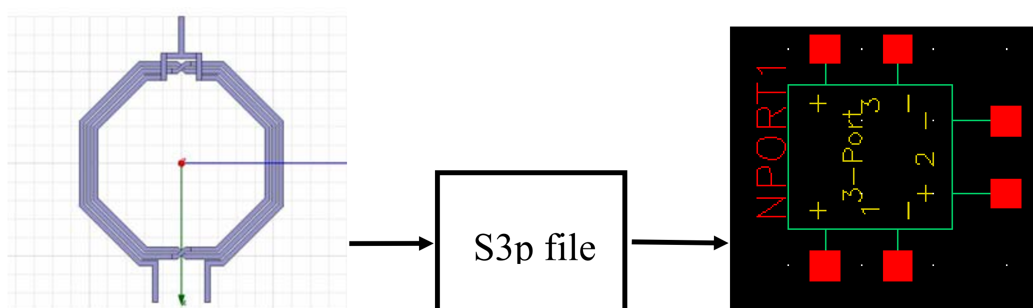


Fig. 3.5. Co-simulation of Spectre RF and the MENS inductor from HFSS and Designer.

oscillation frequency of 5GHz and the available MOS varactor in the foundry. After investigation of MOS varactor, the inductance value for the 5GHz VCO is within the range from 1nH to 6 nH. The structure of the inductor is parameterized so that we can do a parametric sweep in HFSS and Designer. The VCO with a high Q inductor can low down the power consumption under same circuit performance as compared to the VCO using a low Q inductor. So the Q_{peak} of the inductor is designed to as close to the desired oscillation frequency as possible.

The required inductance of the VCO featured in high FOM is chosen as large as possible under a constraint of an acceptable tuning range. The Qpeak of the inductor is also moved close to the oscillation frequency. The inductor has an inductance of 5.07nH at 5GHz with the Q of 37. As for the VCO with a wide tuning range, the inductance is chosen smaller, but still high Q, to make the tuning of the varactor more

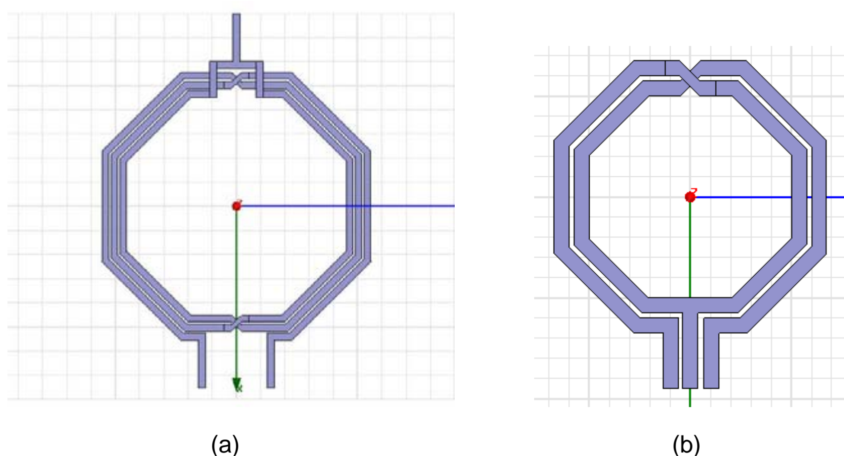


Fig. 3.6. The layout of the MENS inductors. (a) inductance of 5nH at 5GHz with differential Q of 43 used in the VCO with a high FOM. (b) inductance of 1.5nH at 5GHz with differential Q of 37 used in the VCO with a wide tuning range..

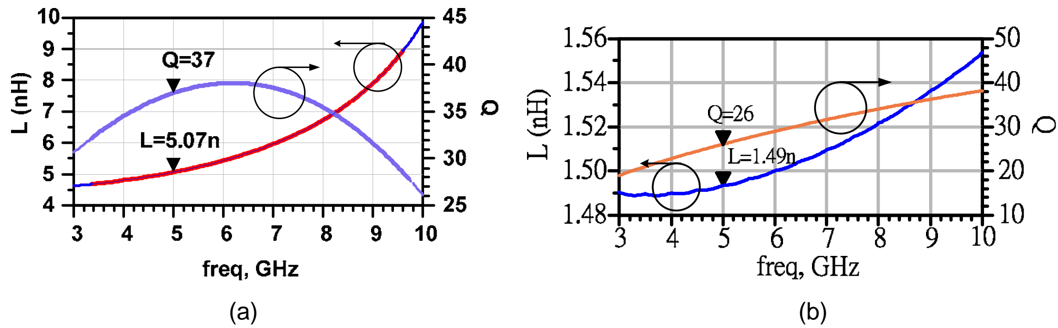


Fig. 3.7. The inductance value and the Q of the MENS inductors (a) used in the VCO with a high FOM. (b) used in the VCO with a wide tuning range.

effective. The inductor has an inductance value of 1.49nH at 5GHz with a Q of 26. The layout of these two inductors is shown in Fig. 3.6 where (a) is for the VCO with a high FOM and (b) is used in the VCO with a wide tuning range. The inductance value and the Q of the two inductors versus frequency are also plotted in Fig. 3.7. The simulation results of the Q include the contact resistance of 0.3Ω at each bonding pad.

3.2.2 The Design of VCO with a High FOM

For the VCO with a high FOM, the inductor with a high inductance value to reduce the power consumption and increase the output power level is chosen so that the phase noise can be improved. As we goes back to the Fig. 3.3, C_f connecting the source nodes of the cross-coupled pair to the V_{DD} is used to filter out the phase noise contribution from the current source. Using current mirror for the bias of the VCO core circuit is more immune to the process variation. The device size of current source is chosen the largest to have lower flicker noise contributing to the output phase noise. Choice of the varactor and the inductor is to have a high loaded Q.

(i) LC Tank Design

Goal of the oscillation frequency is around 5GHz. Taking the inductance and the parasitic capacitance (from the switching pair, the output buffer, and the interconnect in the layout) into account, the residue capacitance is around 75fF. The varactor group fitting the requirement is group 1 and group 2 with finger number of 15~25 and 10~20, respectively. The characteristics of the varactor are summarized in Table 3.1. Finally the varactor of group 1 with finger 20 is chosen because the LC tank can have a high parallel resistance (R_p) at the resonance so that the power consumption can be lowed down. The Q of the LC tank and the R_p are shown in Fig. 3.8 where the parasitic capacitance from the active device is not included into the simulation.

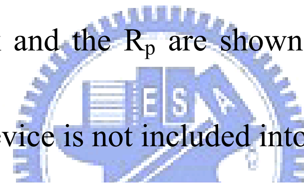


Table 3.1. The summary of MOS varactor of group 1 and group 2.

Vtune:0~1V Freq=5GHz	finger	Cmin(fF)	Cmax(fF)	Q
group1	10	23.5	46.92	76.8~153.2
	20	47	94.69	58.8~118.7
group2	10	47.06	93.92	54.6~109
	20	94.48	191.8	39.5~80.3

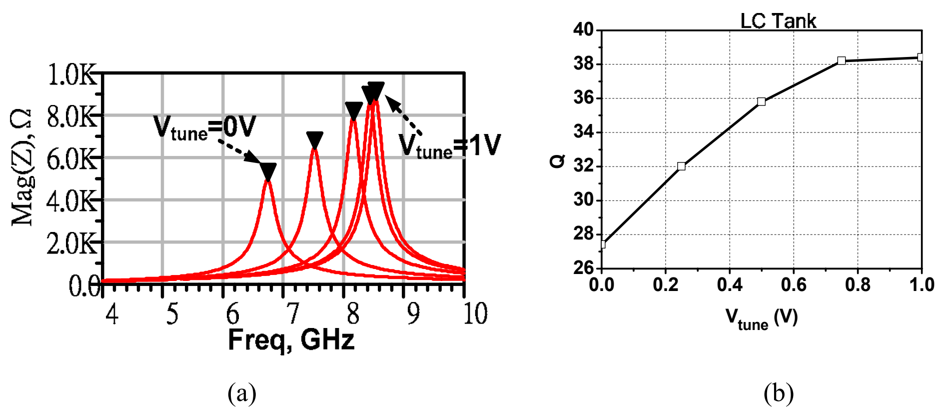


Fig. 3.8. The impedance and the Q of the LC tank under different tuning voltages. (a) the impedance (b) the Q.

(ii) Design of Switching Pair

The PMOS switching pair provides the energy for the VCO to maintain lasting oscillation. However, inevitably, it will contribute parasitic capacitance to degrade the tuning range of the VCO. Small size of transistor in the switching pair can give a small parasitic capacitance, but it also provides small energy to the tank of the VCO. So the trade-off between the tuning range and the FOM are taken into consideration. We do a sweep on the finger number of the transistors. The finger number is changed from 2 to 30 as the width of the transistor is fixed to 1.5um. The simulation results are shown in Fig. 3.9 where the simulation is done as V_{tune} is 0.5V. Due to the high-Q

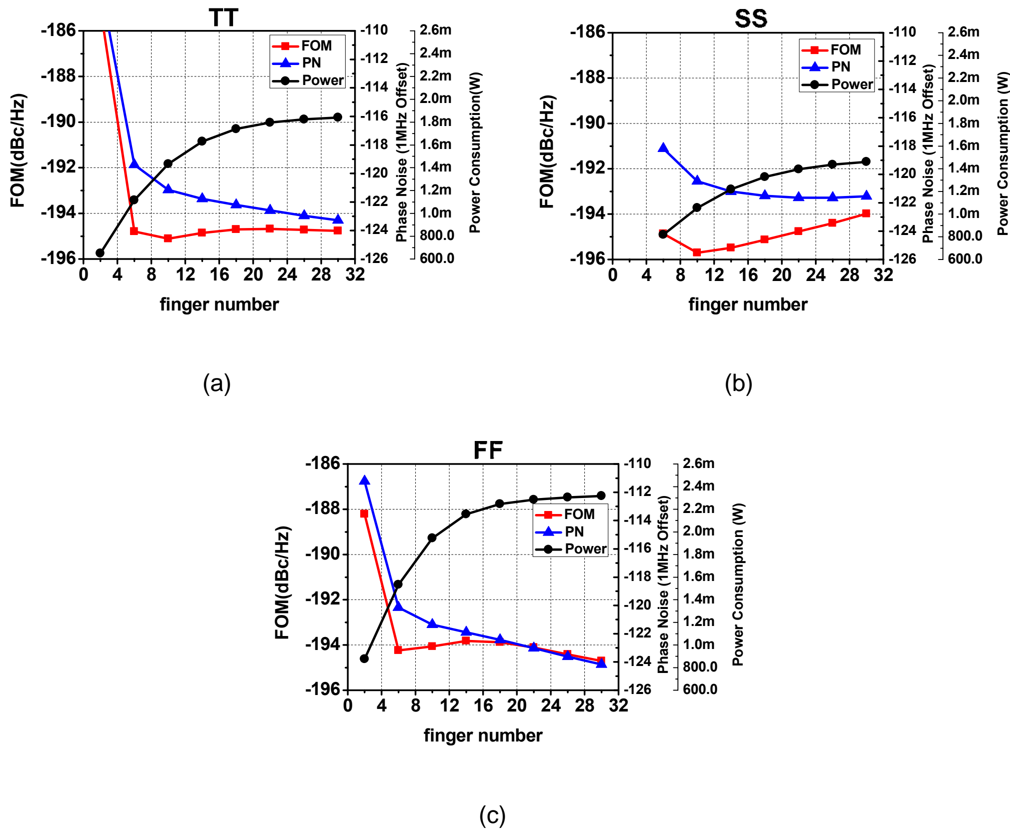
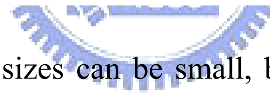


Fig. 3.9. The FOM of the VCO with a high FOM versus the finger number of the switching transistors at different corner cases. (a) TT. (b) SS. (c) FF.



MENS inductor, the transistor sizes can be small, but still provide enough negative transconductances to sustain the oscillation. Final width of the switching transistors are chosen to be 1.5um*25=37.5um. The finger number is set as 25 in order to have flat phase noise response as V_{tune} is changed from 0V to 1V.

(iii) The C_f Effects on the Phase Noise

In general, C_f is added to filter out the flicker noise from the current source so that the phase noise can be improved. However, the phase noise response is insensitive to the value of C_f as shown in Fig. 3.10 in the designed VCO with a high FOM. The reason is that the size of the switching transistors is small in the designed VCO. The

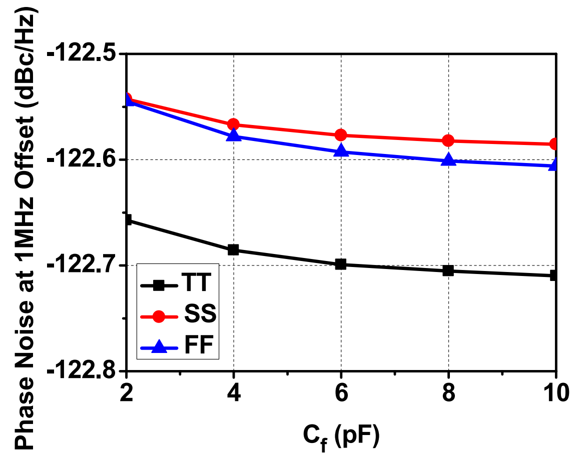


Fig. 3.10. The dependence of the output phase noise on C_f under different corner cases.

contribution of the current source to the output phase noise is function of the transistor size of the switching pair [Ref]. The low frequency noise from the current source causes the amplitude variation of the carrier. And then the amplitude variation modulates the harmonics of the carrier, resulting in the modulation of the phase shift. Variability in the phase shift results in variability in wo, or phase noise. Small transistor size in the switching pair corresponds to low harmonic distortion so that the amplitude modulation (AM) to phase modulation (PM) conversion can be reduced. So the phase noise can be improved and insensitive to the filtering capacitance C_f [16]. However, reduction of the device width is limited by two constraints, sufficient loop gain and voltage headroom. We still add capacitance of 4pF to stabilize the current of tail current source.

(iv) Pre-Simulation Results

Pre-simulation results are done by SpectreRF. The core power consumption is only

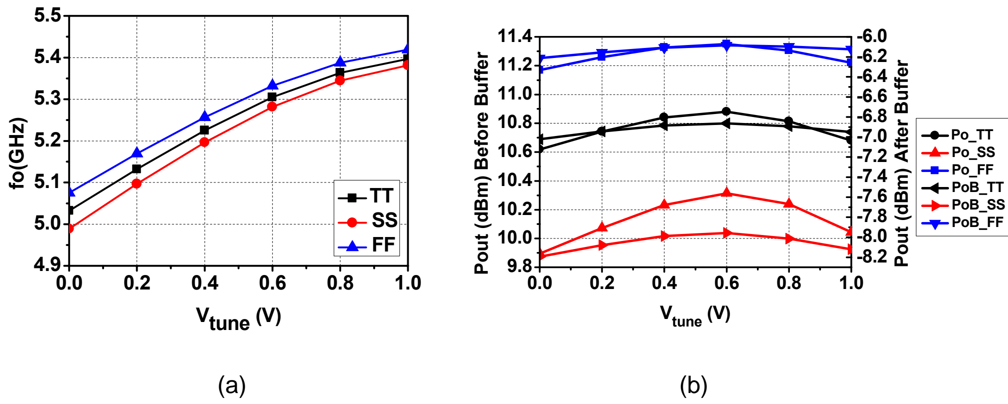


Fig. 3.11. (a) The oscillation frequency. (b) The output power of the high FOM VCO before and after the output buffer.

about 1mW under a supply voltage of 1V. The oscillation frequency as shown in Fig. 3.11(a) is in the range from 5GHz to 5.4GHz corresponds to 8% tuning range. The output power of the high FOM VCO is shown in Fig. 3.11(b) where the right axis denotes the output power before the buffer referred to 50Ω and the left axis is the output power after the buffer stage. The figure shows that the output power referred to 50Ω before the buffer is very large. This is due to the used high-Q MEMS inductor so that the parallel resistance at the resonance is large to produce the large output voltage

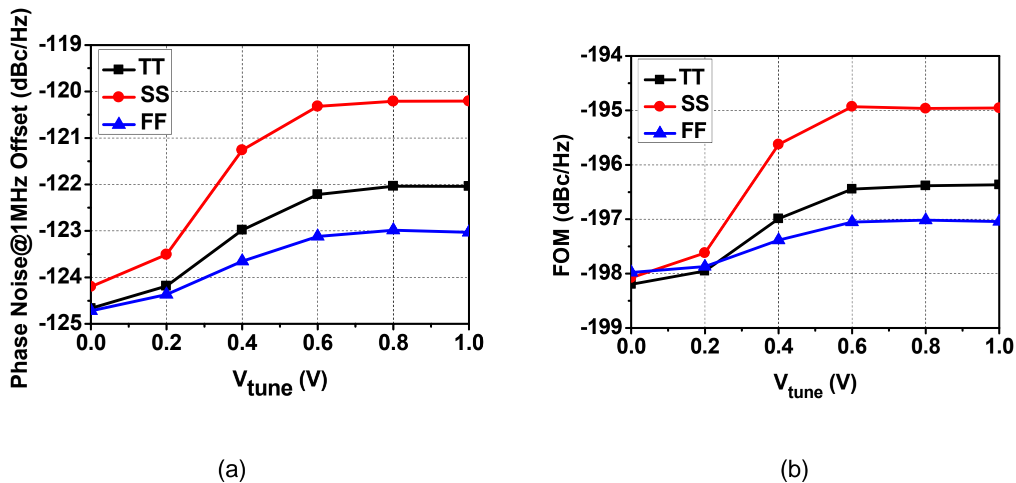


Fig. 3.12. (a) the phase noise at 1MHz offset. (b) The FOM versus the tuning voltage.

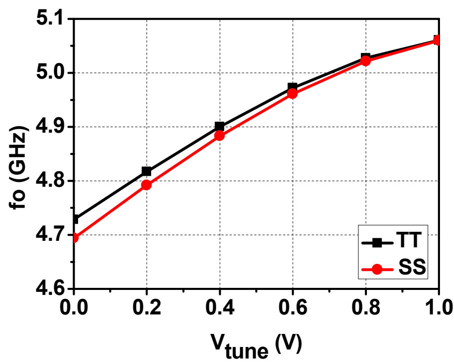
swing even the power consumption is low.

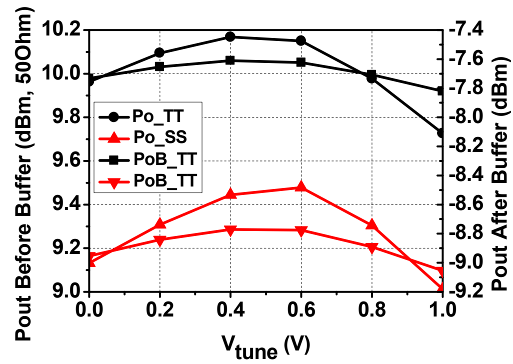
Fig. 3.12 plots the phase noise at 1MHz offset and the FOM. The worse case for the phase noise at 1MHz offset is around -120dBc/Hz in the SS corner. The worse case in FOM is about -195dBc/Hz.

(v) Post-Simulation Results

The layout of VCO is imported to Ansoft Designer for the post-simulation to include the parasitic from the interconnections into the circuit simulation. Because the VCO chip will be flipped and then bonded to the carrier, the substrate in the carrier is involved in the simulation to include the detuning effect. The simulation result is exported as a touch stone file with 85 ports and we use a data item to include the touch stone file into the SpectreRF. However, the simulation cannot converge due to too many ports in SpectreRF. So we can only change the simulation tool to other one. We change the simulation tool to Angilent ADS to post-simulate the VCO. Nevertheless, there are some problems to the design kit regarding to the fast-fast (FF) corner in the MOS varactor so the post-simulation results just show the typical-typical (TT) and slow-slow (SS) corner cases.

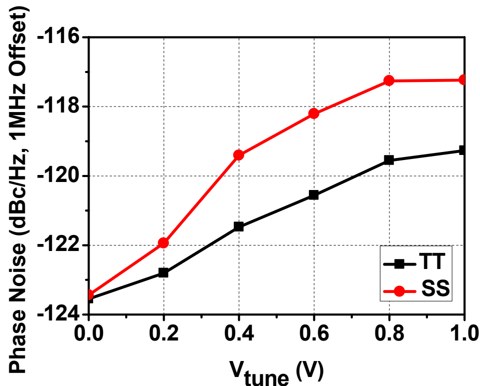
The post-simulation results are shown in Fig. 3.13 and Fig. 3.14. The circuit performance is degraded due to the interconnections and the carrier substrate resulting in larger parasitic effects. The output power is degraded about 1dBm. The frequency

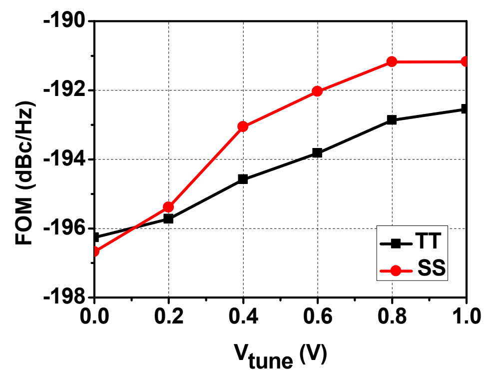




(a) (b)

Fig. 3.13. The oscillation frequency and the output power versus the tuning voltage. (a) The oscillation frequency. (b) The output power.





(a) (b)

Fig. 3.14. The phase noise and the FOM versus the tuning voltage, (a) the phase noise at 1MHz offset. (b) the FOM.

tuning range is shrunk to about 300MHz.The phase noise at the higher tuning voltage degrades the most , so does the FOM. Table 3.2 summarizes the post-simulation results of the high FOM VCO in the worse cases.

Table 3.2. Summary of post-simulation result of high performance VCO.

VDD=1V, Vtune=1V (Worse Case)	TT	SS
Operation Current (mA)	1.2(core)	1.03(core)
Phase noise @ 1 MHz offset (dBc/Hz)	-119.27	-117.23
Tuning Range (GHz)	4.73 ~ 5.06 (5.4-5.03)/5.03=7%	4.69 ~ 5.06 (5.38-4.99)/4.99=7.9%
FOM	-192.6	-191.2

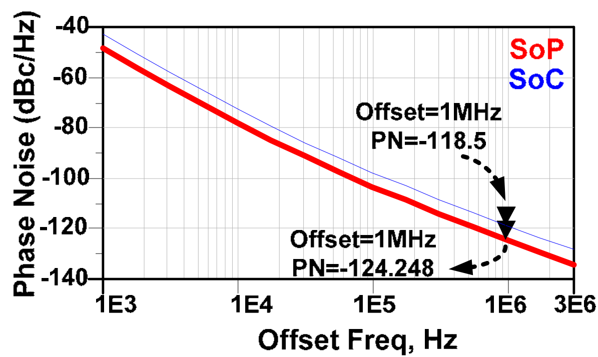


Fig. 3.15. Phase noise. SoP versus SoC.

(vi) SoP V.S. SoC

Fig. 3.15 shows the comparison between SoP and SoC solutions for the VCO design. The tuning range and the LC cross-coupled pair are the same in these two solutions. The only difference is the inductors. It indicates that the phase noise improvement is around 6dB by using SoP technique. The operational power consumption of the SoP case is just 1.08mW, lower than the SoC solution which the power consumption is 1.38mW. This simulation results are the pre-simulation results to compare the two solutions impartially.

3.2.3 The VCO with a Wide Tuning Range

In order to have a wide tuning range, the VCO needs smaller inductance value to make the varactor more effective. Because of using the MEMS inductor, the Q of the inductor is still high even the inductance is small. The residue capacitance is about 200fF for the LC tank to oscillate at 5GHz using a 1.5nH MEMS inductor. The choice of the varactor is group 2 with the finger number of 40, and group 3 with the finger number of 30. However, the Q of these two varactors are about 25 to 50 which are too low to degrade the loaded Q of the LC tank. In order to mitigate the problem, we use three parallel varactors of the group 1 with the finger number of 30. The Q of this varactor is 47.5~96.5, much higher than the varactor of group 2 and group3. Table 3.3 summarizes the parameters of these three varactors. Fig. 3.16 plots the impedance and the loaded Q of the LC tank versus the tuning voltage. The design procedure to decide the transistor size in the switching pair is the same as the high FOM VCO. So we do

Table 3.3. The summary of the characteristic of the varactors.

Vtune:0~1V Freq=5GHz	finger	Cmin(fF)	Cmax(fF)	Q
group1	30	211.8	430	47.5~96.5
group2	40	191.7	398	25~51.9
group3	30	216.6	450.5	23.39~48.7

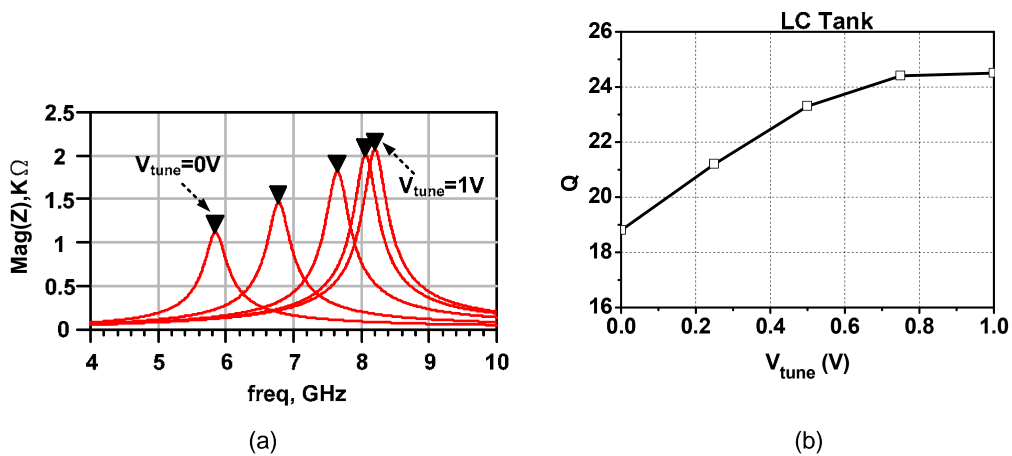


Fig. 3.16. The impedance and the Q of the LC tank under different tuning voltages. (a) the impedance (b) the Q.

not repeat it here. The transistor size is decided to be 2um*50=100um.

(i) Pre-Simulation Results

The power consumption of the designed VCO is 1.33mW and 1.08mW at the TT and SS corners, respectively, under a supply voltage of 1V. The pre-simulation results including the oscillation frequency, output power, phase noise, and the FOM are shown in Fig. 3.17 and Fig. 3.18. The oscillation frequency of the VCO can change from 4.8 GHz to 5.8 GHz. The tuning range is about 20%. The phase noise in the

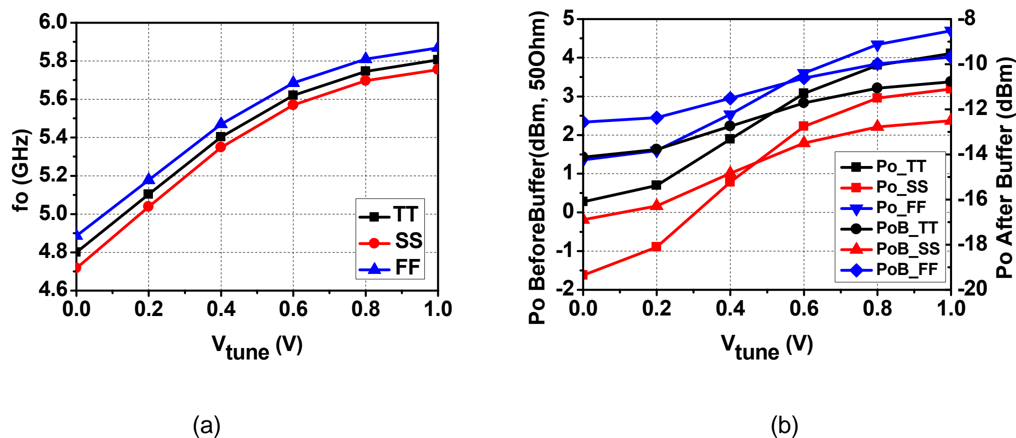
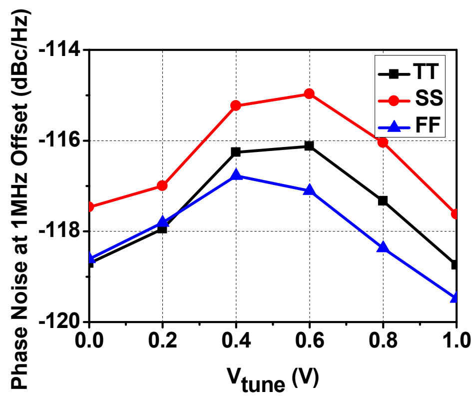
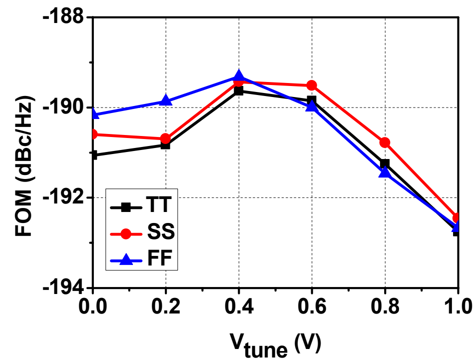


Fig. 3.17. (a) the oscillation frequency (b) the output power, versus the tuning voltage.



(a)



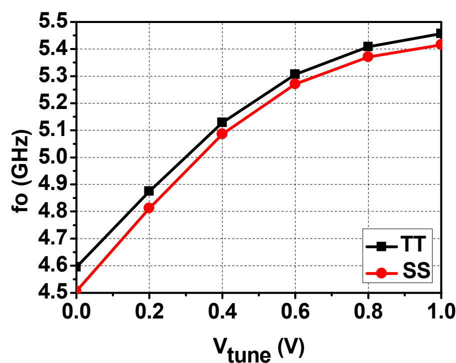
(b)

Fig. 3.18. The phase noise and the FOM versus the tuning voltage, (a) phase noise at 1MHz offset. (b) the FOM.

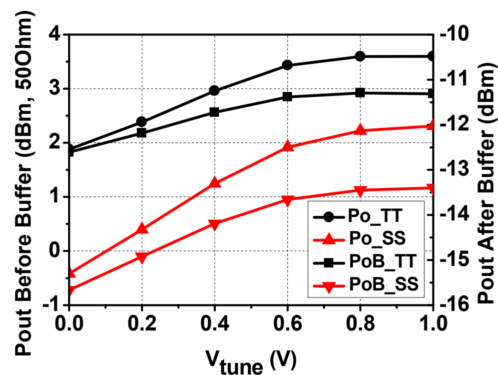
worse case is about -115dBc/Hz. The worse FOM is around -189dBc/Hz.

(ii) Post-Simulation Results

Fig. 3.19 and Fig. 3.20 plot the post-simulation results. The tuning range of the oscillation frequency is reduced to about 900MHz. The worse case of the FOM is about -188dB, a little degraded compared to the pre-simulation results. Table 3.4 summarizes the performance in the worse cases of the VCO.



(a)



(b)

Fig. 3.19. (a) The oscillation frequency. (b) The output power.

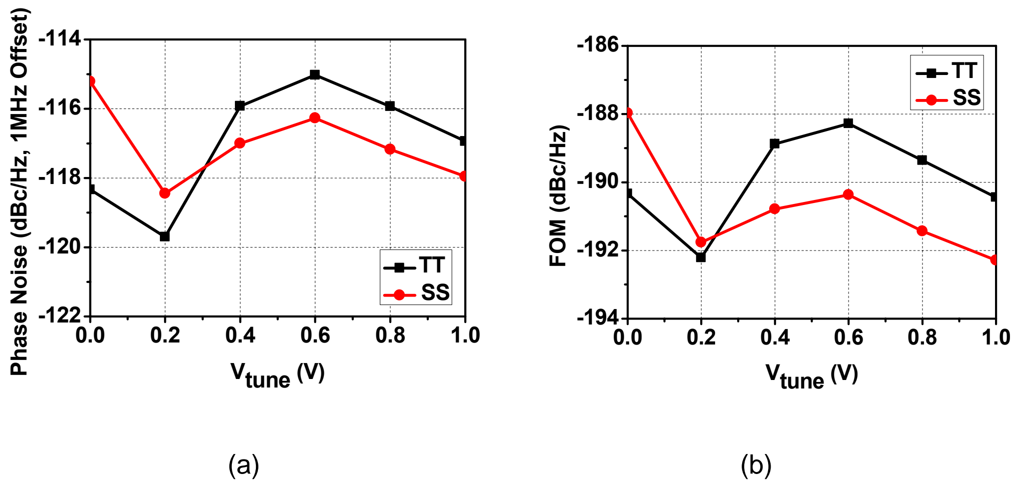


Fig. 3.20. The phase noise and the FOM versus the tuning voltage. (a) the phase noise at 1MHz offset. (b) the FOM.

Table 3.4. Performance summary of the wide tuning range VCO.

VDD=1V	TT V_{tune}=0.6V (Worse Case)	SS V_{tune}=0V (Worse Case)
Operation Current (mA)	1.33(core)	1.08(core)
Phase noise @ 1 MHz offset (dBc/Hz)	-115.03	-115.2
Tuning Range (GHz)	4.59 ~ 5.46 (17.6%)	4.51 ~ 5.42 (20.2%)
FOM	-188.3	-188

(iii) SoP V.S. SoC

The VCOs using SoP and SoC solutions are shown in Fig. 3.21. It indicates the SoP solution has smaller phase noise than the SoC solution.

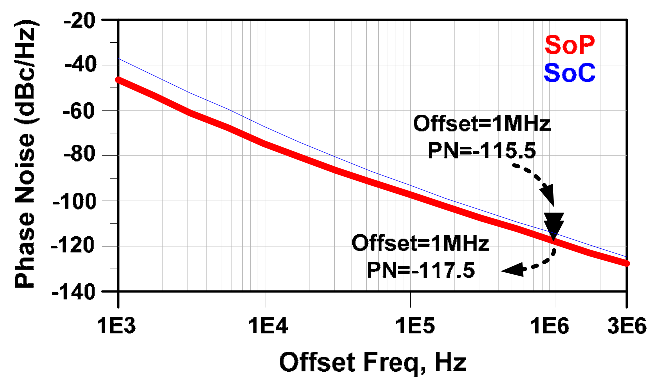


Fig. 3.21. Phase noise. SoP versus SoC.

The comparison of the two VCOs by using SoP and SoC are summarized in Table.3.5.

Table 3.5. Summary of SoP versus SoC.

		VCO with a high FOM		VCO with a wide tuning range	
VDD=1V		SoP	SoC	SoP	SoC
Power Consumption (mW)		1.08	1.38	1.34	1.33
Phase noise (dBc/Hz)	1KHz	-48.3	-42.84	-46.4	-37.2
	600KHz	-119.2	-113.4	-112.5	-110.3
	1MHz	-124.2	-118.5	-117.5	-115.5
	3MHz	-134.3	-128.5	-127.4	-124.6
Tuning Range		5.03 ~ 5.4 (7.36%)	5.02 ~ 5.37 (6.8%)	4.81~5.81 (20%)	4.83 ~ 5.79 (19.2%)
FOM (dBc/Hz)	1KHz	-182	-175.5	-178.8	-169.6
	600KHz	-197	-190.5	-189.3	-187.2
	1MHz	-197.9	-191.1	-189.9	-187.9
	3MHz	-198.5	-191.6	-190.2	-187.5

3.3 The Layout of the Chip and the Carrier

The chip and the carrier layout of the two VCOs are shown in Fig. 3.22. On the top of the chip layout is the high FOM VCO and on the opposite side is the VCO with a wide tuning range. The chip size is 1*1mm^2. Outside the red square is the carrier layout. Because the interconnection of the DC bias is very long, we add a lot of bypass capacitors on the chip to make the DC line ac short to ground. The distance between the DC line and the MEMS inductor is kept far to avoid an impact on the performance of the inductors. The signal line and the DC line needed to bond are put

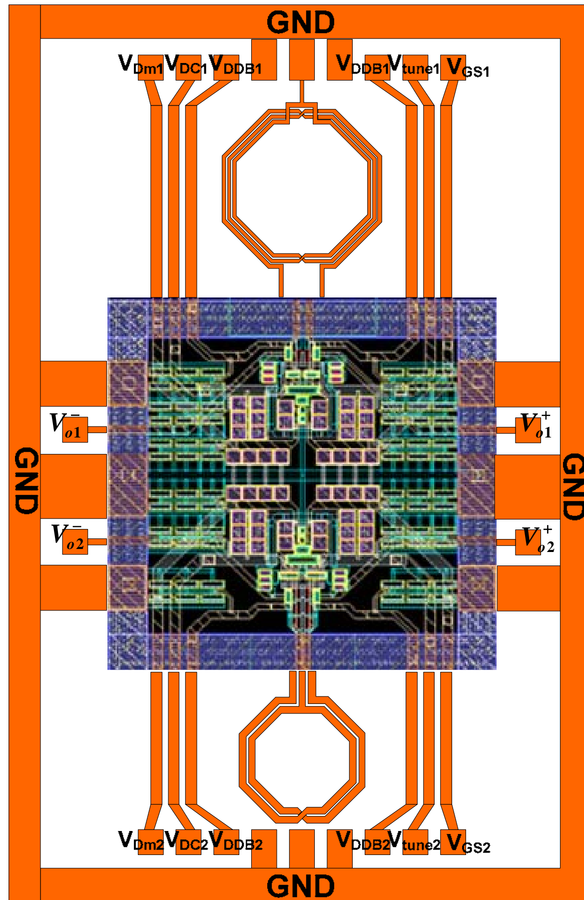


Fig. 3.22. The chip and the carrier layout. The layout outside the red square is the carrier layout.

100um pads on them. The 100um includes the margin of 50um for the chip dicing. The distance between adjacent pads is set as 20um.

The measurement will be conducted by the on-wafer probing as shown in Fig. 3.23. The outputs of VCO are connected to 50Ω termination and spectrum analyzer, individually. The DC bias is given by a 9-pin DC probe with a pitch 100um. So we will use the spectrum analyzer to measure the phase noise, the oscillation frequency, and the output power.

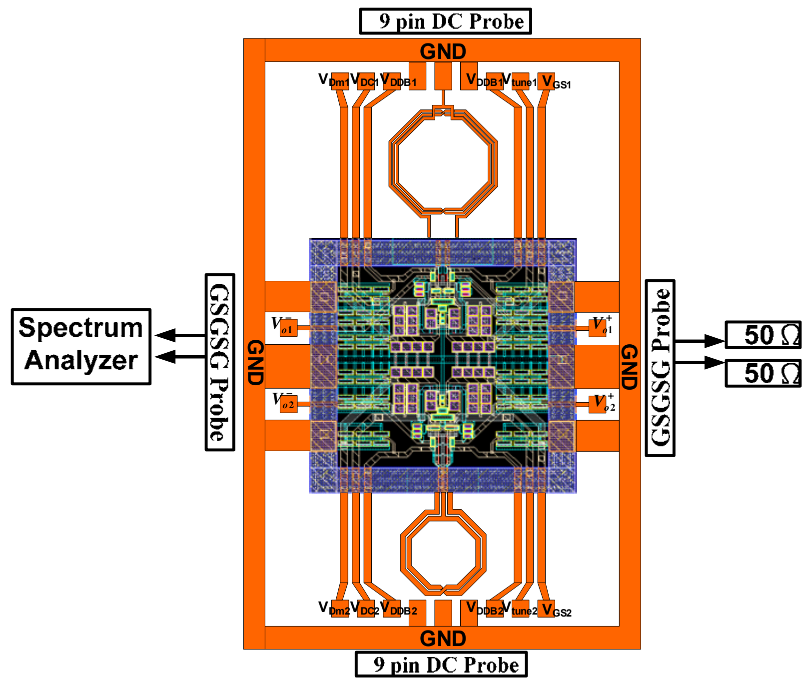


Fig. 3.23.　Measurement setup for the on-wafer measurement.

Chapter 4 Design of the Low Power and Low Voltage Bulk-Driven Mixer

4.1 Introduction

A mixer performs a frequency translation either from a high-frequency input signal to a low-frequency signal or vice versa. A mixer has two inputs: a RF signal and a local oscillator (LO) input. Usually the two inputs are at different ports. The output signal of the mixer is at the frequency that is equal to difference between RF signal frequency and LO signal frequency. Mixer with this kind of frequency translation is used in receiver circuits. It is referred to as down-conversion.

In the case of a frequency translation to a higher frequency, the input signal is at low frequency, while the frequency of LO is again high. The output signal of the mixer is at the frequency which is the sum or difference of the two frequencies. Mixer with this kind of frequency translation is used in transmitter circuits. It is referred to as up-conversion mixer.

We can generally classify the mixer into two types: switching mixer and weakly nonlinear mixer. For a switching mixer, the LO signal is usually large to switch on and off the transistor. The LO signal is like a square-wave signal. This square-wave

signal is modulated by the input signal, and the resulting waveform contains a frequency component at the sum or difference of input signal and LO signal. For the weakly nonlinear mixer, the amplitude of input signal and LO signal is usually kept small so that the mixer behavior in the weakly nonlinear way. The output signal at the sum of difference of input signal and LO signal is due to the second-order nonlinearity of the mixer circuit. The input signal and LO signal at weakly nonlinear mixer are usually applied at different ports sot that the analysis becomes more complex.

Gilbert Mixer as shown in Fig. 4.1 is generally used in the RF front-end circuit. Input RF signal is translated into a current by the transconductance stage formed by the M_1 transistor. The switching pair formed by the transistors of M_2 and M_3 samples the transformed current to realize the function of the frequency conversion. The downconversion or upconversion current flows through the resistor R_L to produce the

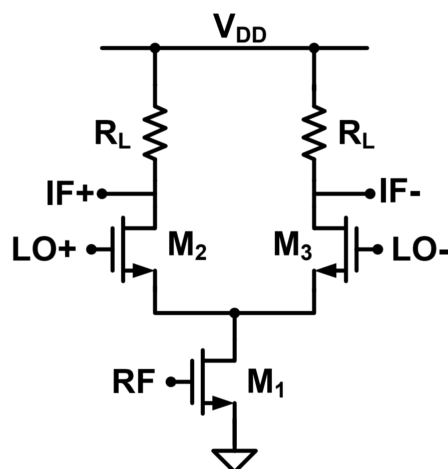


Fig. 4.1. Single-balanced Gilbert Mixer.

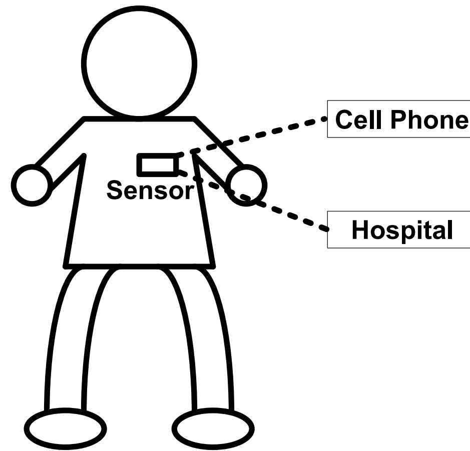


Fig. 4.2. Applications of WBAN on the medical service.

IF output voltage.

For the application of WBAN on the medical service as shown in Fig. 4.2, many sensor nodes are installed on the human body to detect the biological condition of the human body. The sensor nodes translate the biological signal into the electrical signal, and then transmit to the receiver so that the healthy condition of the human beings can be well controlled. Because the sensor nodes are put on the human body, it needs to consume as low power as possible to prolong the battery lifetime. The supply voltage shall be kept to low level too. Gilbert mixer can not be realized at the low voltage operation due to the fact that it stacks two transistors. The supply voltage must be high enough to make the Gilbert mixer features in high circuit performance.

The good candidate of the mixer for the low voltage operation is the bulk-driven mixer as shown in Fig. 4.3. RF signal and LO signal are applied to the gate and the bulk, respectively, to merge the transconductance stage and the switching stage into

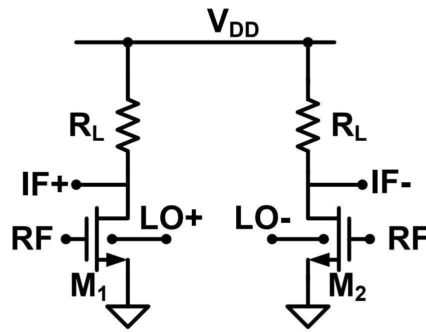


Fig. 4.3. Single-balanced bulk-driven mixer.

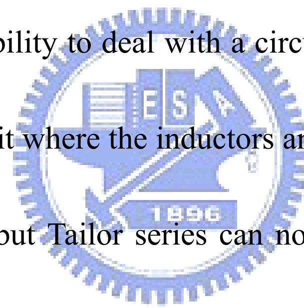
single one. The bulk-driven mixer just needs one transistor to realize the function of the frequency conversion so it can operate in a low supply voltage.

This chapter will discuss the design and analysis of a low power and low voltage bulk-driven mixer for the application of WBAN. The carrier frequency is at the frequency band of the wireless medical telemetry system (WMTS) which is 1.395~1.4 GHz. The bandwidth is 6 MHz. The supply voltage is set as 1V. First we will introduce the variant Volterra series which is used to analyze the nonlinearity of the bulk-driven mixer.

4.2 Fundamental of Nonlinearity Analysis

In this chapter it is investigated how weakly nonlinear behavior of analog integrated circuit can be computed. As we use simulation tool to get the response of distortion, simulation results can not present information from which designers can derive which circuit parameters or circuit elements should be modified to meet the required specifications. Volterra series can help us get such information [17].

Volterra series describe the output of a nonlinear system as the sum of the response of a first-order operator, a second-order one, a third-order one and so on. Every operator is described either in the time domain or in the frequency domain with a kind of transfer function, called Volterra kernel. Actually, Volterra series describes a nonlinear system in a way which is equivalent to the way Taylor series approximate an analytic function. The higher input amplitude, the more terms of that series need to be taken into account in order to describe the system behavior properly. For very high amplitude, the series diverges, just as Taylor series. The most difference from Taylor series and Volterra series is ability to deal with a circuit with memory. Volterra series can analyze the memory circuit where the inductors and capacitors play a role because it retains phase information, but Tailor series can not. Taylor series can deal with a memory-less circuit only.



For a one-port system, such as low noise amplifier (LNA), Volterra kernel can be computed to get the output response for any input signal. However, for multiple-input circuits, Volterra kernel becomes tensors. Calculations with tensors are quite cumbersome in a multiple-input system. It is called a direct calculation method (DCM), variant Volterra series approach, which directly calculates the required response repeatedly so that it does not make use of tensors. Briefly, the DCM calculates the nonlinear response at specific frequency directly and if you want to

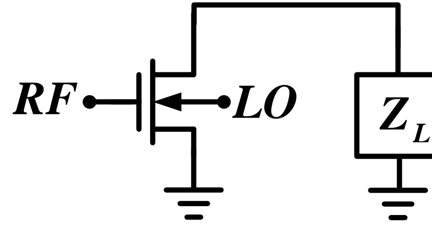


Fig. 4.4. The half circuit of the bulk-driven mixer for the nonlinearity analysis.

obtain another response at other frequency, you need to calculate repeatedly. Using DCM or Volterra kernels will get the same nonlinear response. For mixer circuits, such as Gilbert mixer and the bulk-driven mixer, they are a two-port system with two inputs of RF signal and LO signal. Therefore, the DCM is more appropriate for the nonlinearity analysis. Consequently, we focus on the DCM in this section.

The DCM is explained with the circuit shown in Fig. 4.4. This is a half circuit of the proposed bulk-driven mixer in this chapter later. Fig. 4.5 shows its equivalent circuit for nonlinear analysis.

The circuits is excited at two different input ports by two sinusoidal signals, $v_{RF}(t)$ and $v_{LO}(t)$ at frequencies w_{RF} and $w_{LO,}$ respectively.

$$v_{RF}(t) = \mathrm{Re}(V_{RF} e^{jw_{RF}t}) \tag{4-1}$$

$$v_{LO}(t) = \mathrm{Re}(V_{LO} e^{jw_{LO}t}) \tag{4-2}$$

Under steady-state conditions, every node voltage $v_x(t)$ consists of a sum of harmonics and intermodulation of RF signal and LO signal as indicated in (4-3). RF port has two RF signals at frequencies w_{RF1} and w_{RF2}, respectively, with little frequency offset for a two test in an IIP3 calculation.

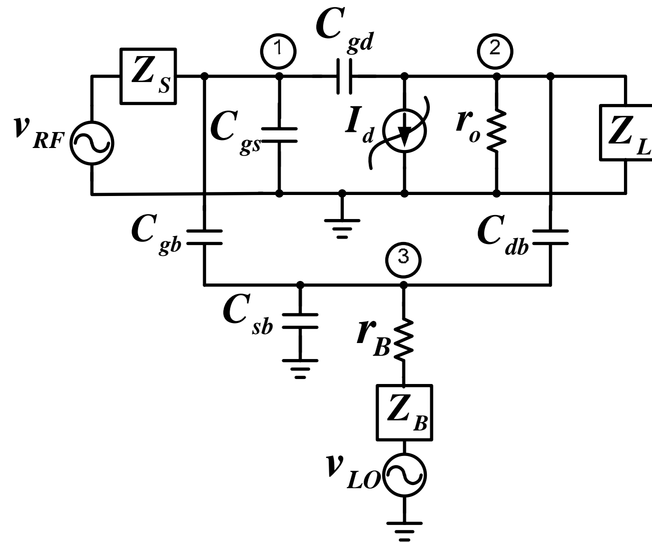


Fig. 4.5. The equivalent circuit for the nonlinear analysis.

$$v_x(t) = \mathrm{Re}(V_{x,1,0,0}e^{jw_{RF1}t}) + \mathrm{Re}(V_{x,0,1,0}e^{jw_{RF2}t}) + \mathrm{Re}(V_{x,0,0,1}e^{jw_{LO}t})$$

$$+ \mathrm{Re}(V_{x,1,1,0}e^{j(w_{RF1}+w_{RF2})t}) + \mathrm{Re}(V_{x,1,-1,0}e^{j(w_{RF1}-w_{RF2})t}) + \ldots\ldots\ldots\ldots$$

$$= \frac{1}{2}\sum_{m,n,k=-\infty}^{\infty} V_{x,m,n,k}e^{j(mw_{RF1}+nw_{RF2}++kw_{LO})t}).. \tag{4-3}$$

where $V_{x,m,n,k}$ denotes the voltage at the node x at the frequency of $mw_{RF1} + nw_{RF2} + kw_{LO}$. The goal of this section is to explain the method to compute the complex phasor $V_{x,m,n,k.}$

The drain current is a function of V_{GS}, V_{DS}, and V_{BS} where source node is the voltage reference so that it can be expanded by a three dimensional power series as shown in equation of (4-4). This power series will take nonlinearities of g_m , g_{mb} , and g_o into account.

$$I_D = g_m v_{gs} + K_{2_{gm}} v_{gs}^2 + g_{mb} v_{bs} + K_{2_{gmb}} v_{bs}^2 + g_o v_{ds} + K_{2_{go}} v_{ds}^2$$

$$+ K_{2_{gm\&gmb}} v_{gs} v_{bs} + K_{2_{2gm\&gmb}} v_{gs}^2 v_{bs} + \ldots. \tag{4-4}$$

where the nonlinear parameters are defined in the following equations:

$$K_{n_{g1}} = \frac{1}{n!}\frac{\partial^n I_D(u)}{\partial u^n}, K_{n_{jg1\&(n-j)g2}} = \frac{1}{j!}\frac{1}{(n-j)!}\frac{\partial^n I_D(u,v)}{\partial u^j \partial v^{(n-j)}}$$

and $K_{n_{jg1\&kg2\&(n-j-k)g3}} = \frac{1}{j!}\frac{1}{k!}\frac{1}{(n-j-k)!}\frac{\partial^n I_D(u,v,w)}{\partial u^j \partial v^k \partial w^{(n-j-k)}}$

(i) First-Order Response

Fist-order response is a linear response which can be obtained by Kirchoff's laws. We use a technique of superposition to get the individual linear response to the inputs of v_{RF1}, v_{RF2}, and v_{LO}, that is, as we calculate the response to the v_{RF1} input, we set v_{RF2}, and v_{LO} to zero. Take the first-order response to the v_{RF1} input for instance. The ac equivalent circuit is then in Fig. 4.6. We can get three equations at the nodes marked ①,②, and ③ by using Kirchoff's current and voltage laws,

$$\frac{v_{RF} - v_1}{Z_s} = sC_{gb}(v_1 - v_3) + sC_{gs}v_1 + sC_{gd}(v_1 - v_2) \tag{4-5}$$

$$sC_{gb}(v_1 - v_3) = sC_{sb}v_3 + \frac{1}{Z_B + r_B}v_3 + sC_{db}(v_3 - v_2) \tag{4-6}$$

$$sC_{gd}(v_1 - v_2) = g_m v_1 + g_{mb}v_3 + sC_{db}(v_2 - v_3) + \frac{1}{Z_L}v_2 \tag{4-7}$$

After making an arrangement into matrix, we can write down a matrix equation:

$$\begin{bmatrix} jw_{RF1}C_g + \frac{1}{Z_S} & -jw_{RF1}C_{gd} & -jw_{RF1}C_{gb} \\ g_m - jw_{RF1}C_{gd} & jw_{RF1}(C_{gs} + C_{db}) + \frac{1}{Z_L \parallel r_o} & g_{mb} - jw_{RF1}C_{db} \\ -jw_{RF1}C_{gb} & -jw_{RF1}C_{db} & jw_{RF1}C_b + \frac{1}{Z_B + r_B} \end{bmatrix} \begin{pmatrix} V_{1,1,0,0} \\ V_{2,1,0,0} \\ V_{3,1,0,0} \end{pmatrix} = \begin{pmatrix} \frac{V_{RF1}}{Z_S} \\ 0 \\ 0 \end{pmatrix}$$

where $C_g = C_{gs} + C_{gd}$ and $C_b = C_{gb} + C_{db} + C_{sb}$.

We can the above equation in a general form

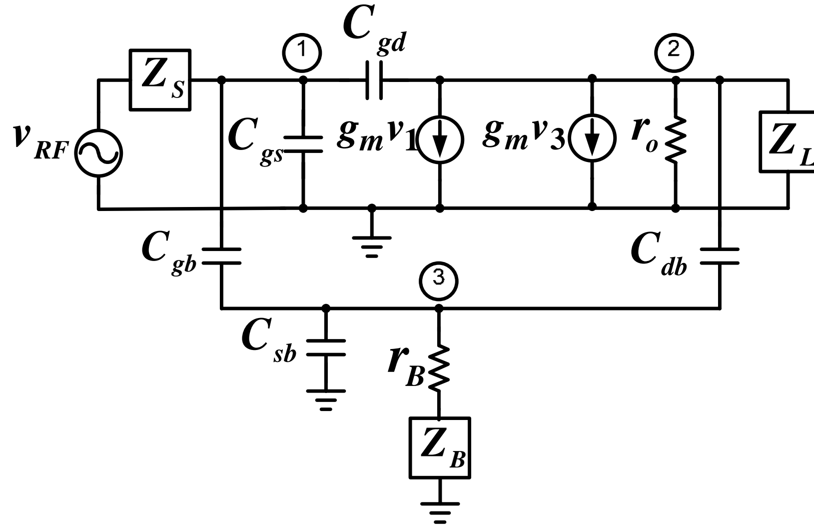


Fig. 4.6. The equivalent circuit for the first-order response.

$$Y(jw_{RF1}).U_{1,0,0} = IN_{1,1,0,0} \tag{4-8}$$

where

$$Y(w) = \begin{bmatrix} jwC_g + \dfrac{1}{Z_S} & -jwC_{gd} & -jwC_{gb} \\ g_m - jwC_{gd} & jw(C_{gs} + C_{db}) + \dfrac{1}{Z_L \| r_o} & g_{mb} - jwC_{db} \\ -jwC_{gb} & -jwC_{db} & jwC_b + \dfrac{1}{Z_B + r_B} \end{bmatrix},$$

$$U_{1,0,0} = \begin{pmatrix} V_{1,1,0,0} \\ V_{2,1,0,0} \\ V_{3,1,0,0} \end{pmatrix} \text{ and } IN_{1,1,0,0} \begin{pmatrix} \dfrac{V_{RF1}}{Z_S} \\ 0 \\ 0 \end{pmatrix}$$

Y(w) is a transconductance matrix and $U_{1,0,0}$ is a matrix of the voltage response. $IN_{1,1,0,0}$ is a vector whose only nonzero components are terms in the network equations that contain V_{RF1}. Then the linear response can be gained by the inverse operation.

Based on the same principle, the fist-order response to the inputs of v_{RF2}, and v_{LO}

can be found by the following equations:

$$Y(jw_{RF2}).U_{1,0,0} = \begin{pmatrix} \frac{V_{RF2}}{Z_S} \\ 0 \\ 0 \end{pmatrix} = U_{0,1,0} \tag{4-9}$$

$$Y(jw_{LO}).U_{1,0,0} = \begin{pmatrix} 0 \\ 0 \\ \frac{-V_{LO}}{Z_B + r_B} \end{pmatrix} = U_{1,0,0} \tag{4-10}$$

(ii) Second-Order Nonlinear Response

With the information from the previous step the second-order response can be computed. Again the same linearized network must be solved as the one that has been used to compute the first-order response. However, the inputs are different now: instead of the external excitation, so-called nonlinear current source of order two must be applied. There is one nonlinear current source for each nonlinearity in the circuit and the source is applied in parallel with the linear current source. This nonlinear current source of order two can be obtained by the following method. We simplify our question by considering only one nonlinear current source, related to K_{2gm} nonlinear parameter. The equivalent circuit for the analysis of the second-order response is shown in Fig. 4.7. We write the nodal equation at node 2 and get the following equation.

$$sC_{gd}(v_1 - v_2) = g_m v_1 + K_{2_{gm}} v_1^2 + g_{mb} v_3 + sC_{db}(v_2 - v_3) + \frac{1}{Z_L} v_2 \tag{4-11}$$

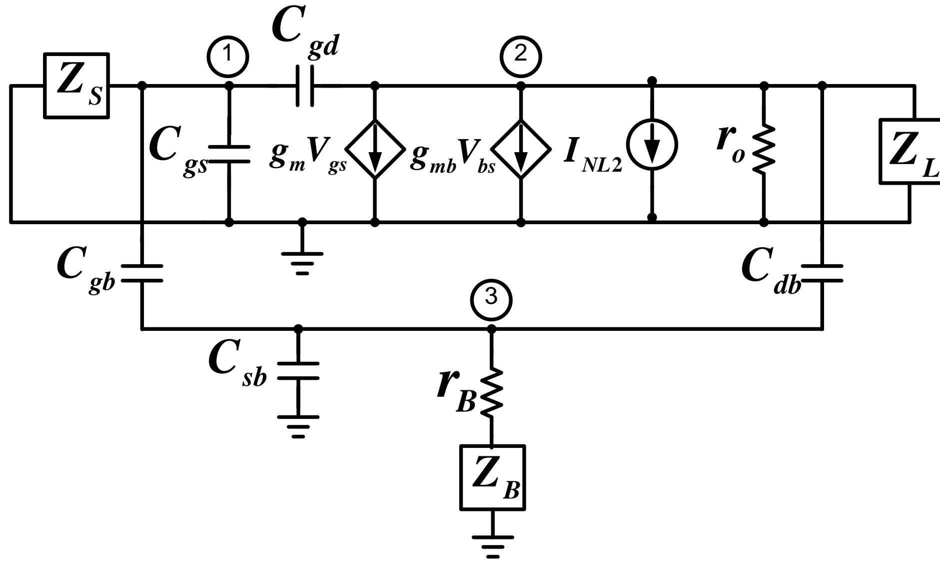


Fig. 4.7. The equivalent circuit for the second-order nonlinear response.

And from the equation (4-3), v_1 can be written as:

$$v_1^2 = (\frac{1}{2} v_{1,1,0,0} e^{jw_{RF1}t} + \frac{1}{2} v_{1,0,1,0} e^{jw_{RF2}t} + \frac{1}{2} v_{1,0,0,1} e^{jw_{LO}t} + ...)^2$$

$$= (\frac{1}{2} v_{1,1,0,0} v_{1,0,1,0} e^{j(w_{RF1}+w_{RF2})t} + ... \qquad (4\text{-}12)$$

Because we consider the second-order nonlinear response now, we only see the response at the frequency which is the sum of frequencies of w_{RF1} and w_{RF2}. The responses at the frequencies of the combination of w_{RF1} and w_{RF2} frequencies can be found by the same method. After substituting (4-12) into (4-11) we can get the following equation:

$$-\frac{1}{2} K_{2_{gm}} V_{1,1,0,0} V_{1,0,1,0} e^{j(w_{RF1}+w_{RF2})t} + ... = \frac{1}{2}(g_m - sC_{gd}) V_{1,1,1,0} e^{j(w_{RF1}+w_{RF2})t}$$

$$+ \frac{1}{2} s(C_{gd} + C_{db} + \frac{1}{Z_L}) V_{2,1,1,0} e^{j(w_{RF1}+w_{RF2})t} + \frac{1}{2}(g_{mb} - sC_{db}) V_{3,1,1,0} e^{j(w_{RF1}+w_{RF2})t} + ...$$

Together with nodal equation (4-5) and (4-6), we can arrange the three equations in the matrix form.

$$\begin{bmatrix} jw_{RF1}C_g + \frac{1}{Z_S} & -jw_{RF1}C_{gd} & -jw_{RF1}C_{gb} \\ g_m - jw_{RF1}C_{gd} & jw_{RF1}(C_{gs}+C_{db}) + \frac{1}{Z_L \| r_o} & g_{mb} - jw_{RF1}C_{db} \\ -jw_{RF1}C_{gb} & -jw_{RF1}C_{db} & jw_{RF1}C_b + \frac{1}{Z_B + r_B} \end{bmatrix} \begin{pmatrix} V_{1,1,1,0} \\ V_{2,1,1,0} \\ V_{3,1,1,0} \end{pmatrix} = \begin{pmatrix} 0 \\ -K_{2_{gm}} V_{1,1,0,0} V_{1,0,1,0} \\ 0 \end{pmatrix}$$

$$= Y(j(w_{RF1} + w_{RF2})).U_{1,1,0} = IN_{2,1,1,0} \tag{4-13}$$

Hence, we get the second-order nonlinear current source related to K_{2gm}. The contribution of the nonlinear current source related to K_{2gm} to the second-order nonlinear response can be calculated by the (4-13). Other nonlinear current sources can be gotten by the same method. Therefore, the matrix equation related to the second-order response is summarized in the following equation.

$$\begin{pmatrix} V_{1,1,1,0} \\ V_{2,1,1,0} \\ V_{3,1,1,0} \end{pmatrix} = Y^{-1}(j(w_{RF1} + w_{RF2}) \begin{pmatrix} 0 \\ -i_{NL2} \\ 0 \end{pmatrix} \begin{pmatrix} V_{1,1,-1,0} \\ V_{2,1,-1,0} \\ V_{3,1,-1,0} \end{pmatrix} = Y^{-1}(j(w_{RF1} - w_{RF2}) \begin{pmatrix} 0 \\ -i_{NL2} \\ 0 \end{pmatrix}$$

$$\begin{pmatrix} V_{1,1,0,-1} \\ V_{2,1,0,-1} \\ V_{3,1,0,-1} \end{pmatrix} = Y^{-1}(j(w_{RF1} - w_{LO}) \begin{pmatrix} 0 \\ -i_{NL2} \\ 0 \end{pmatrix} \ldots\ldots\ldots\ldots$$

where iNL2 is the total second-order nonlinear current sources. It is written as:

$$i_{NL2} = i_{NL2,gm} + i_{NL2,go} + i_{NL2,gm\&go} + i_{NL2,gm\&gmb} + i_{NL2,gmb\&go} + \ldots.$$

We summarize the nonlinear current source at Table 4.1 for the responses at the frequencies of $2w_1$ and $|w_1 \pm w_2|$ where w_1 and w_2 can be w_{RF1}, w_{RF2}, or w_{LO}. The interpretation of the values of the nonlinear current sources from Table 4.1 is as follows: the second-order nonlinearity of every one-dimensional conductance or capacitance combines the first-order response of its controlling voltage due to V_{RF1} only, with the first-order response of its controlling voltage due to V_{RF2} only, to a

second-order signal. This signal, at frequency $|w_1 \pm w_2|$, then propagates through the rest of the circuit. When considering this propagation, only the linearized elements need to be taken into account. Indeed, any interaction of the second-order signal with another one yields a response of order higher than two.

$$\frac{1}{2}K_{2_{g1\&g2}}V_{i,1,0,0}V_{j,0,\pm1,0}\frac{1}{2}K_{2_{g1\&g2}}V_{i,0,\pm1,0}V_{j,1,0,0}\frac{1}{2}K_{2_{g1\&g2}}V_{i,1,0,0}V_{j,1,0,0}$$

Table 4.1. Second-order nonlinear current at $w_1 \pm w_2$ and $2w_2$.

Type of nonlinearity	Nonlinear current source for response at $\|w_1 \pm w_2\|$.	Nonlinear current source for response at $2w_1$
(trans)conductance	$K_{2_{g1}}V_{i,1,0,0}V_{i,0,\pm1,0}$	$\frac{1}{2}K_{2_{g1}}(V_{i,1,0,0})^2$
Capacitor	$j(w_1 \pm w_2)K_{2_{g1}}V_{i,1,0,0}V_{i,0,\pm1,0}$	$jw_1K_{2_{C1}}(V_{i,1,0,0})^2$
Two-dimensional conductance (one cross-terms)	$\frac{1}{2}K_{2_{g1\&g2}}V_{i,1,0,0}V_{j,0,\pm1,0}$ $+\frac{1}{2}K_{2_{g1\&g2}}V_{i,0,\pm1,0}V_{j,1,0,0}$	$\frac{1}{2}K_{2_{g1\&g2}}V_{i,1,0,0}V_{j,1,0,0}$

(iii) Third-Order Nonlinear Response

We can obtain the third-order nonlinear response by the same procedure. The third-order nonlinear current sources are summarized in Table 4.2 and 4.3. The matrices for the third-order nonlinear response are as followed:

$$\begin{pmatrix} V_{1,3,0,0} \\ V_{2,3,0,0} \\ V_{3,3,0,0} \end{pmatrix} = Y^{-1}(j(3w_{RF1})\begin{pmatrix} 0 \\ -i_{NL3} \\ 0 \end{pmatrix} \qquad \begin{pmatrix} V_{1,2,-1,0} \\ V_{2,2,-1,0} \\ V_{3,2,-1,0} \end{pmatrix} = Y^{-1}(j(2w_{RF1} - w_{RF2})\begin{pmatrix} 0 \\ -i_{NL3} \\ 0 \end{pmatrix}$$

$$\begin{pmatrix} V_{1,2,1,0} \\ V_{2,2,1,0} \\ V_{3,2,1,0} \end{pmatrix} = Y^{-1}(j(2w_{RF1} + w_{RF2})\begin{pmatrix} 0 \\ -i_{NL3} \\ 0 \end{pmatrix} \quad \begin{pmatrix} V_{1,2,0,-1} \\ V_{2,2,0,-1} \\ V_{3,2,0,-1} \end{pmatrix} = Y^{-1}(j(2w_{RF1} - w_{LO})\begin{pmatrix} 0 \\ -i_{NL3} \\ 0 \end{pmatrix} \cdots\cdots\cdots\cdots$$

Table 4.2. Third-order nonlinear current for response at $2w_1 \pm w_2$.

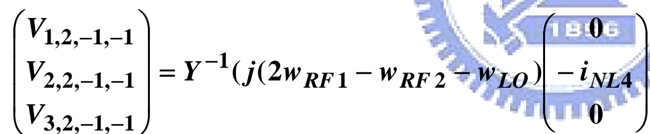
Type of nonlinearity	Nonlinear current source for response at $\lvert 2w_1 \pm w_2 \rvert$.
(trans)conductance	$K_{2_{g1}} V_{i,1,0,0} V_{i,1,\pm1,0} + K_{2_{g1}} V_{i,0,\pm1,0} V_{i,2,0,0} + \frac{3}{4} K_{3_{g1}} V_{i,1,o}^2 V_{i,0,\pm1,0}$
Capacitor	$j(2w_1 \pm w_2)[K_{2_{C1}} V_{i,1,0,0} V_{i,1,\pm1,0} + K_{2_{C1}} V_{i,0,\pm1,0} V_{i,2,0,0} + \frac{3}{4} K_{3_{g1}} V_{i,1,o}^2 V_{i,0,\pm1,0}]$
Two-dimensional conductance (one cross-terms)	$\frac{1}{2} K_{2_{g1\&g2}} [V_{i,0,\pm1,0} V_{j,2,0,0} + V_{i,1,0,0} V_{j,1,\pm1,0} + V_{i,1,\pm1,0} V_{j,1,0,0} + V_{i,2,0,0} V_{j,0,\pm1,0}]$ $+ \frac{1}{4} K_{3_{2g1\&g2}} [2V_{i,0,\pm1,0} V_{i,1,0,0} V_{j,1,0,0} + V_{i,1,0,0}^2 V_{j,0,\pm1,0}]$ $+ \frac{1}{4} K_{3_{g1\&2g2}} [2V_{i,1,0,0} V_{j,0,\pm1,0} V_{j,1,0,0} + V_{i,0,\pm1,0} V_{j,1,0,0}^2]$
Three-dimensional conductance (only cross terms)	$\frac{1}{4} K_{3_{g1\&g2\&g3}} [V_{i,0,\pm1,0} V_{j,1,0,0} V_{k,1,0,0} + V_{i,1,0,0} V_{j,0,\pm1,0} V_{k,1,0,0}$ $+ V_{i,1,0,0} V_{j,1,0,0} V_{k,0,\pm1,0}]$

Table 4.3. Third-order nonlinear current for response at $3w_2$

Type of nonlinearity	Nonlinear current source for response at $3w_2$.
(trans)conductance	$K_{2_{g1}} V_{i,0,1,0} V_{i,0,2,0} + \frac{1}{4} K_{3_{g1}} V_{i,0,1,0}^3$
Capacitor	$3jw_2 [K_{2_{C1}} V_{i,0,1,0} V_{i,0,2,0} + \frac{1}{4} K_{3_{g1}} V_{i,0,1,0}^3]$
Two-dimensional conductance (one cross-terms)	$\frac{1}{2} K_{2_{g1\&g2}} [V_{i,0,1,0} V_{j,0,2,0} + V_{i,0,2,0} V_{j,0,1,0}] + \frac{1}{4} K_{3_{2g1\&g2}} V_{i,0,1,0}^2 V_{j,0,1,0}]$ $+ \frac{1}{4} K_{3_{g1\&2g2}} V_{i,0,1,0} V_{j,0,1,0}^2]$
Three-dimensional conductance (only cross terms)	$\frac{1}{4} K_{3_{g1\&g2\&g3}} V_{i,0,1,0} V_{j,0,1,0} V_{k,0,1,0}$

(iv) Fourth-Order Response

In general, nonlinear current sources are calculated up to third-order because it is enough to obtain the desired information. These nonlinear currents sources up to third-order can be found at the textbook. However, for the bulk-driven mixer circuit, we should make efforts to obtain the fourth-order nonlinear current sources. The details why we need to calculate up to the fourth-order will be discussed in the next section. The fourth-order nonlinear current sources can not be found in the text. We can use a mathematic tool to help us find out the fourth-order nonlinear current source. These fourth-order nonlinear current sources are summarized in Table 4.4 and 4.5. The matrix for the IM3 response is as followed.



$$\begin{pmatrix} V_{1,2,-1,-1} \\ V_{2,2,-1,-1} \\ V_{3,2,-1,-1} \end{pmatrix} = Y^{-1}(j(2w_{RF1} - w_{RF2} - w_{LO})\begin{pmatrix} 0 \\ -i_{NL4} \\ 0 \end{pmatrix}$$

(v) Calculation

Before we start to calculate the nonlinear response, those nonlinear parameters need to be known. We extract these parameters from the DC simulation of the circuit shown in Fig. 4.4 using Angilent ADS. With the above equations and the extracted parameters we can calculate the each order nonlinear response directly.

Table 4.4. Fourth-order nonlinear current for response at $|2w_1+w_2+w_3|$

Type of nonlinearity	Nonlinear current source for response at $\|2w_1+w_2+w_3\|$
(trans)conductance	$K_{2_{g1}}(V_{i,1,0,1}V_{i,1,1,0}+V_{i,0,1,1}V_{i,2,0,0}+V_{i,0,1,0}V_{i,2,0,1}+V_{i,0,0,1}V_{i,2,1,0})$ $+\frac{3}{4}K_{3_{g1}}(V_{i,0,1,1}V_{i,1,0,0}^2+2V_{i,0,1,0}V_{i,1,0,0}V_{i,1,0,1}+2V_{i,0,0,1}V_{i,1,0,0}V_{i,1,1,0}$ $+2V_{i,0,0,1}V_{i,0,1,0}V_{i,2,0,0})$ $+\frac{3}{2}K_{4_{g1}}V_{i,0,0,1}V_{i,0,1,0}V_{i,1,0,0}^2$
Two-dimensional conductance (one cross-terms)	$\frac{1}{2}K_{2_{g1\&g2}}(V_{i,2,1,0}V_{j,0,0,1}+V_{i,2,0,1}V_{j,0,1,0}+V_{i,2,0,0}V_{j,0,1,1}+V_{i,1,1,0}V_{j,1,0,1}$ $+V_{i,1,0,1}V_{j,1,1,0}+V_{i,0,1,1}V_{j,2,0,0}+V_{i,0,1,0}V_{j,2,0,1}+V_{i,0,0,1}V_{j,2,1,0})$ $\frac{1}{2}K_{3_{2g1\&g2}}(V_{i,1,0,0}V_{i,1,1,0}V_{j,0,0,1}+V_{i,0,1,0}V_{i,2,0,0}V_{j,0,0,1}+V_{i,1,0,0}V_{i,1,0,1}V_{j,0,1,0}$ $+V_{i,0,0,1}V_{i,2,0,0}V_{j,0,1,0}+\frac{1}{2}V_{i,1,0,0}^2V_{j,0,1,1}+V_{i,0,1,1}V_{i,1,0,0}V_{j,1,0,0}$ $++V_{i,0,1,0}V_{i,1,0,1}V_{j,1,0,0}+V_{i,0,0,1}V_{i,1,1,0}V_{j,1,0,0}+V_{i,0,1,0}V_{i,1,0,0}V_{j,1,0,1}$ $+V_{i,0,0,1}V_{i,1,0,0}V_{j,1,1,0}+V_{i,0,0,1}V_{i,0,1,0}V_{j,2,0,0})$ $+\frac{3}{8}K_{4_{3g1\&g2}}(V_{i,0,1,0}V_{i,1,0,0}^2V_{j,0,0,1}+V_{i,0,0,1}V_{i,1,0,0}^2V_{j,0,1,0}+2V_{i,0,0,1}V_{i,0,1,0}V_{i,1,0,0}V_{j,1,0,0})$ $+\frac{1}{4}K_{4_{2g1\&2g2}}(V_{i,1,0,0}^2V_{j,0,0,1}V_{j,0,1,0}+2V_{i,0,1,0}V_{i,1,0,0}V_{j,0,0,1}V_{j,1,0,0}$ $+2V_{i,0,0,1}V_{i,1,0,0}V_{j,0,1,0}V_{j,1,0,0}+V_{i,0,0,1}V_{i,0,1,0}V_{j,1,0,0}^2)$
Three-dimensional conductance (only cross terms)	$\frac{1}{4}K_{3_{g1\&g2\&g3}}(V_{i,2,0,0}V_{i,0,1,0}V_{k,0,0,1}+V_{i,1,1,0}V_{j,1,0,0}V_{k,0,0,1}+V_{i,1,0,0}V_{j,1,1,0}V_{k,0,0,1}$ $+V_{i,0,1,0}V_{j,2,0,0}V_{k,0,0,1}+V_{i,2,0,0}V_{j,0,0,1}V_{k,0,1,0}+V_{i,1,0,1}V_{j,1,0,0}V_{k,0,1,0}+V_{i,1,0,0}V_{j,1,0,1}V_{k,0,1,0}$ $+V_{i,0,0,1}V_{j,2,0,0}V_{k,0,1,0}+V_{i,1,0,0}V_{j,1,0,0}V_{k,0,1,1}+V_{i,1,1,0}V_{j,0,0,1}V_{k,1,0,0}+V_{i,1,0,1}V_{j,0,1,0}V_{k,1,0,0}$ $+V_{i,1,0,0}V_{j,0,1,1}V_{k,1,0,0}+V_{i,0,1,1}V_{j,1,0,0}V_{k,1,0,0}+V_{i,0,1,0}V_{j,1,0,1}V_{k,1,0,0}+V_{i,0,0,1}V_{j,1,1,0}V_{k,1,0,0}$

	$+V_{i,1,0,0}V_{j,0,1,0}V_{k,1,0,1}+V_{i,0,1,0}V_{j,1,0,0}V_{k,1,0,1}+V_{i,1,0,0}V_{j,0,0,1}V_{k,1,1,0}+V_{i,0,0,1}V_{j,1,0,0}V_{k,1,1,0}$ $+V_{i,0,1,0}V_{j,0,0,1}V_{k,2,0,0}+V_{i,0,0,1}V_{j,0,1,0}V_{k,2,0,0})$ $+\frac{1}{8}K_{4_{2g1\&g2\&g3}}(V_{i,1,0,0}^{2}V_{j,0,1,0}V_{k,0,0,1}+2V_{i,0,1,0}V_{i,1,0,0}V_{j,1,0,0}V_{k,0,0,1}+V_{i,1,0,0}^{2}V_{j,0,0,1}V_{k,0,1,0}$ $+2V_{i,1,0,0}^{2}V_{j,1,0,0}V_{k,0,1,0}+2V_{i,0,1,0}V_{i,1,0,0}V_{j,0,0,1}V_{k,1,0,0}+2V_{i,0,0,1}V_{i,1,0,0}V_{j,0,1,0}V_{k,1,0,0}$ $2V_{i,0,0,1}V_{i,0,1,0}V_{j,1,0,0}V_{k,1,0,0})$

Table 4.5. Fourth-order nonlinear current for response at $3w_2 \pm w_2$|

Type of nonlinearity	Nonlinear current source for response at $3w_2 \pm w_2$|
(trans)conductance	$K_{2_{g1}}V_{i,0,1,0}V_{i,0,2,0}+\frac{1}{4}K_{3_{g1}}V_{i,0,1,0}^{3}$
Capacitor	$3jw_2[K_{2_{C1}}V_{i,0,1,0}V_{i,0,2,0}+\frac{1}{4}K_{3_{C1}}V_{i,0,1,0}^{3}]$
Two-dimensional conductance (one cross-terms)	$\frac{1}{2}K_{2_{g1\&g2}}[V_{i,0,1,0}V_{j,0,2,0}+V_{i,0,2,0}V_{j,0,1,0}]+\frac{1}{4}K_{3_{2g1\&g2}}V_{i,0,1,0}^{2}V_{j,0,1,0}$ $+\frac{1}{4}K_{3_{g1\&2g2}}V_{i,0,1,0}V_{j,0,1,0}^{2}$
Three-dimensional conductance (only cross terms)	$\frac{1}{4}K_{3_{g1\&g2\&g3}}[V_{i,0,1,0}V_{j,0,1,0}V_{k,0,1,0}]$

4.3 Low Power Bulk-Driven Mixer Design

The proposed low power bulk-driven mixer is as shown in Fig. 4.8. RF signal and LO signal are applied to the gate and the bulk of the MOS, respectively, to merge the LO and RF stage into a single one. There has been lot of papers using the bulk-driven method to implement a low power and low voltage mixer. Reference [3] is the earliest paper demonstrating the idea, but it doesn't make an explicit analysis. Reference [4] applies the LO signal at the gate of the MOS, not at the bulk, which degrades the conversion gain. Reference [5] and [6] consider that the bulk-driven mixer is analogous to Gilbert mixer which the conversion gain basically depends on the linear transconductance g_m. And they usually bias the circuit around the threshold voltage to have a good switching behavior of the LO stage. In this section, nonlinearity analysis using variant Volterra series introduced in the section 4.2 shows that the conversion gain actually comes from the second-order nonlinear current. Furthermore, biasing the

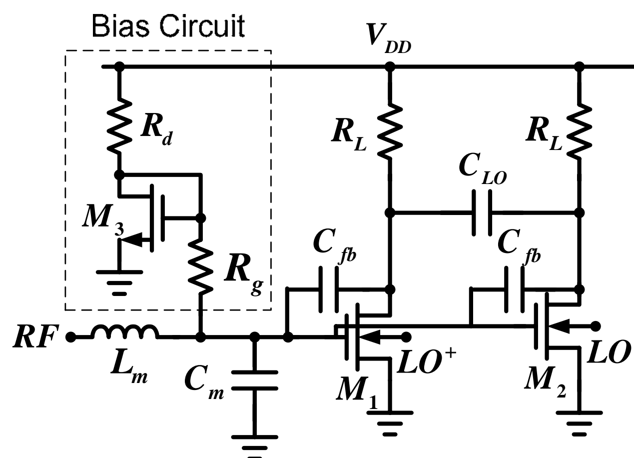


Fig. 4.8. The proposed low power and low voltage bulk-driven mixer.

circuit around the threshold voltage is not a good trade-off between the conversion gain and the linearity.

4.3.1 Large Signal Analysis

In order to understand the operation mechanism of the bulk-driven mixer, a large-signal analysis is done to evaluate the nonlinear response. The LO signal on the bulk periodically modulate the threshold voltage V_T, which is a function of the bulk applied voltage and can be approximated by the equation (4-14) using Taylor series expansion.

$$V_t = V_{to} + r(\sqrt{2\phi_f - V_{BS}} - \sqrt{2\phi_f}) - \frac{1}{2}\frac{r}{\sqrt{2\phi_f - V_{BS}}} v_{LO} = V_{t,DC} - A v_{LO} \tag{4-14}$$

where Φ_f is the surface potential, γ is the body-effect factor, V_{BS} is the bulk bias, $V_{t,DC} = V_{to} + r(\sqrt{2\phi_f - V_{BS}} - \sqrt{2\phi_f})$, and $A \equiv \frac{1}{2}\frac{r}{\sqrt{2\phi_f - V_{BS}}}$.

The bulk-driven mixer is designed to operate in the subthreshold region for the purpose of low power consumption. The drain current in the subthreshold region [6] is written as the equation (4-15) where $V_{DS} >> U_T$ is assumed.

$$I_D = \frac{W}{L} I_t e^{\frac{V_{GS}-V_t}{nU_T}} (1 - e^{-\frac{V_{DS}}{U_T}}) \approx \frac{W}{L} I_t e^{\frac{V_{GS}-V_t}{nU_T}} \tag{4-15}$$

where $V_B = V_{GS} - V_{t,DC}$.

After a few steps of derivation by substituting (4-14) into (4-15), the output voltage at the IF port can be obtained:

$$V_{out} = (I_{D1} - I_{D2})R_L$$

$$= \frac{W}{L} I_t e^{\frac{V_B}{nU_T}} [\frac{AR_L}{(nU_T)^2} v_{RF}(v_{LO^+} - v_{LO^-}) + \frac{AR_L}{2(nU_T)^3} v_{RF}^2 (v_{LO^+} - v_{LO^-})$$

$$+ \frac{A^2 R_L}{6(nU_T)^4} v_{RF}(v_{LO^+}^3 - v_{LO^-}^3) + \frac{AR_L}{6(nU_T)^4} v_{RF}^3 (v_{LO^+} - v_{LO^-}) + ...]. \quad (4\text{-}16)$$

From the equation (4-16), there is a multiplication term of $v_{RF}v_{LO}$ which makes the bulk-driven mixer have the function of the frequency conversion. The voltage conversion gain can also be obtained from the equation (4-16) and is shown in (4-17).

$$\frac{W}{L} I_t e^{\frac{V_B}{nU_T}} \frac{AR_L}{(nU_T)^2} V_{RF} V_{LO} [Cos(w_{RF} - w_{LO})t + Cos(w_{RF} + w_{LO})t] \quad (4\text{-}17)$$

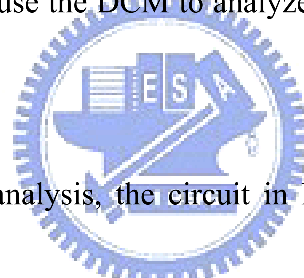
In the first place we consider the g_m nonlinearity only. The drain current can be expanded by Taylor series as shown in (4-18). It can be found by the compare of (4-16) and (4-18) that the conversion gain and the IM3 term in (4-16) correspond to the g'_m and g'''_m term in (4-18), respectively. Thus, it is known that the conversion gain and linearity of the bulk-driven mixer depend on the second-order and the fourth-order nonlinear currents, respectively. This is why we need to know the second-order and fourth-order nonlinear currents. This observation is quite different from the Gilbert Mixer which the first-order and third-order are mostly concerned. This is also the case even the circuit is operated in saturation region. In addition, from equation (4-17), we can understand that voltage conversion gain depends on LO voltage swing, load resistance R_L, I_S and V_B. Bias condition can be decided by

the trade-off between the power consumption, the conversion gain, and the linearity. A large R_L value with a high current corresponds to a higher gain, but there is a limit to the value of the R_L due to the reduction of the drain to source voltage as the current is increased to a certain value. Furthermore, large R_L will worsen the linearity due to the nonlinear effect from the conductance g_o.

$$I_D = g_m v_{gs} + \frac{1}{2!} g_m^{'} v_{gs}^2 + \frac{1}{3!} g_m^{''} v_{gs}^3 + \frac{1}{4!} g_m^{'''} v_{gs}^4 + \ldots \quad (4\text{-}18)$$

4.3.2 AC Response

Above analysis is based on the large signal analysis, it cannot take the frequency effect into consideration. We use the DCM to analyze the bulk-driven mixer which is a two-port system.



In order to simplify the analysis, the circuit in Fig. 4.8 is divided into its half circuit shown in Fig. 4.9 without losing the whole story. The nonlinearity of g_m , g_{mb} , and g_o are taken into account here, but the nonlinearity of the capacitances, such as C_{gs}, are not included into calculation because the analysis later in this section shows that they can be ignored. The matching network is not taken into consideration here.

The required nonlinear parameters for the calculation are extracted by DC simulation of a single transistor at each V_{GS} and V_{DS} bias as V_{BS} is fixed to zero. The calculation results followed are based on the application of WBAN. The RF signal, the LO signal, and the IF signal are locating at 1.4 GHz, 1.39GHz, and 10 MHz,

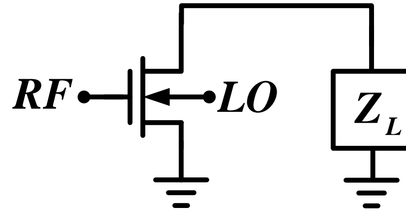


Fig. 4.9. The half circuit of the bulk-driven mixer for the nonlinearity analysis.

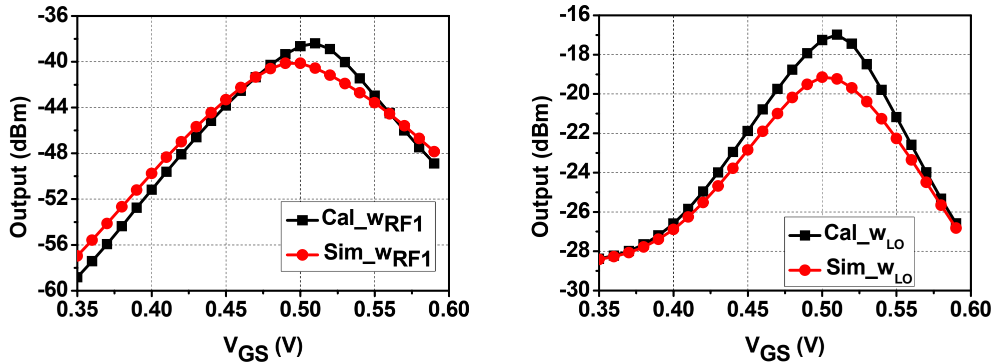


Fig. 4.10. The comparison of the simulation and the calculation results of the first-order response at the frequencies of w_{RF1} and w_{LO}.

respectively. The power of the RF signal and the LO signal are -40dBm and -6dBm, respectively.

The comparison of the calculation and the simulation results of the first-order response are show in Fig. 5-2-4~Fig.5-2-8 under LO power of -6dBm. The frequencies we calculate the response are shown in the figure. The simulation results are conducted by using harmonic balance (HB) in ADS. Two curves are followed well at different V_{GS} except some voltage offset around 0.1V. This voltage off will be discussed later in this section.

Calculation results of the second-order nonlinear responses are shown in Fig. 4.11 and 4.12. As indicated from the Fig. 4.12, the highest voltage conversion gain is about

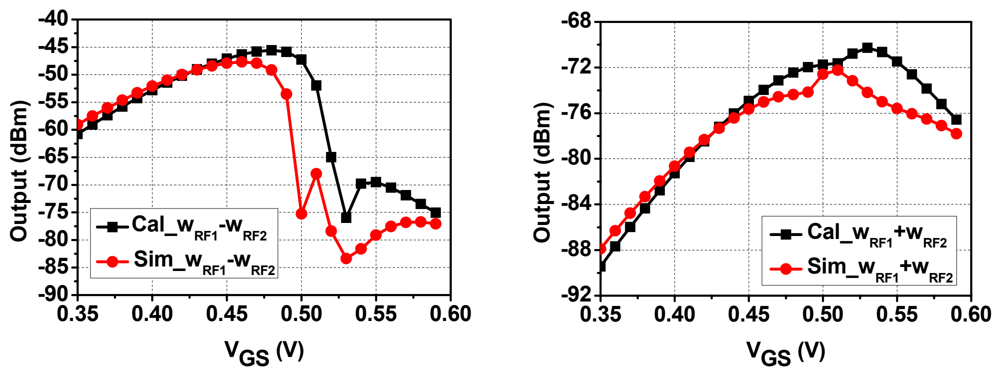


Fig. 4.11. The comparison of the simulation and the calculation results of the second-order nonlinear response at the frequencies of w_{RF1}-w_{RF2} and w_{RF1}+w_{RF2}.

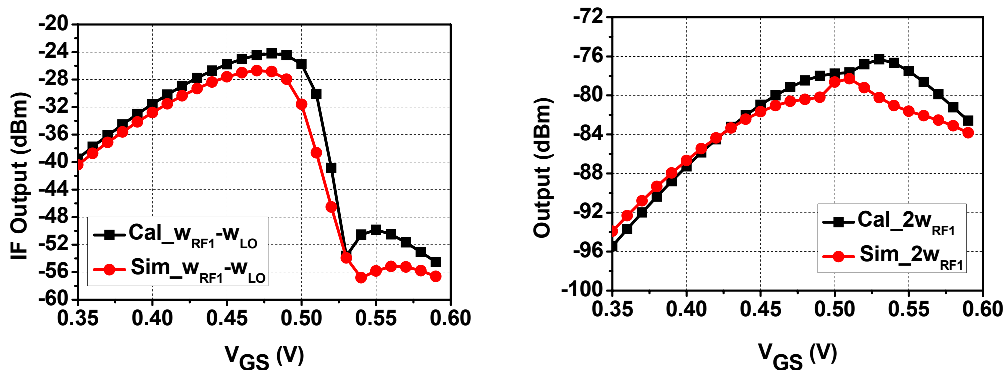


Fig. 4.12. The comparison of the simulation and the calculation results of the second-order nonlinear response at the frequencies of w_{RF1}-w_{LO} and $2w_{RF1}$.

10dB at the V_{GS} of 0.5V which is near the threshold voltage. So bias the bulk-driven mixer can feature in high voltage conversion gain.

The third-order and fourth-order nonlinear response are plotted in the Fig. 4.13 and 4.14. The IM3 response as shown in the Fig. 4.14 tell us that the highest IM3 is at the VGS of 0.5V which happens to the voltage corresponds to the highest voltage conversion. So a higher voltage conversion gain corresponds to a worse linearity. So biasing V_{GS} of the bulk-driven mixer at the voltage near the threshold voltage is not a

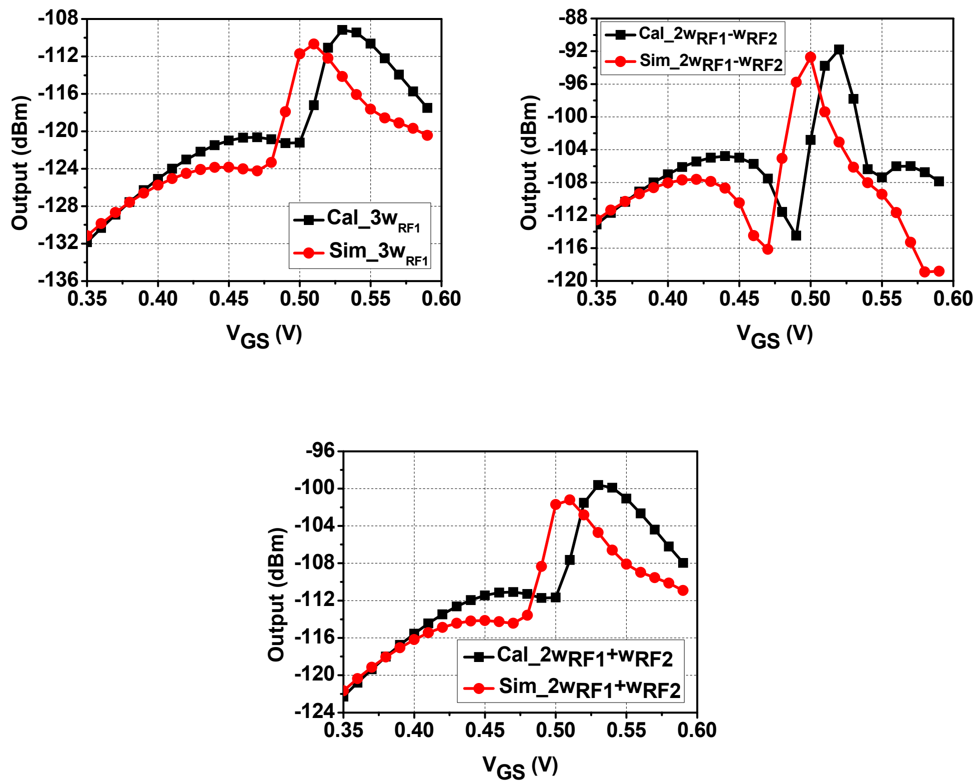


Fig. 4.13. The comparison of the simulation and the calculation results of the third-order nonlinear response.

good trade-off between the conversion gain and the linearity. However, if we carefully investigated the IF and the IM3 responses, we can find that the optimal VGS bias is at the voltage of about 0.43. The IM3 has its minimum at this voltage and the IF output

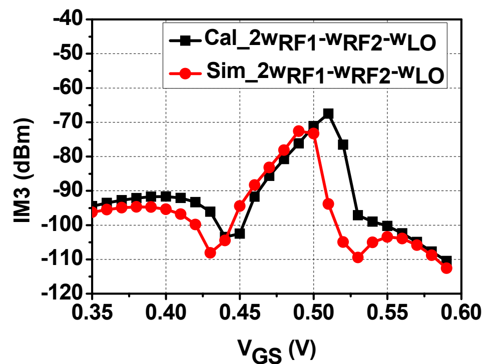


Fig. 4.14. The comparison of the simulation and the calculation results of the fourth-order nonlinear response at the frequency of the IM3.

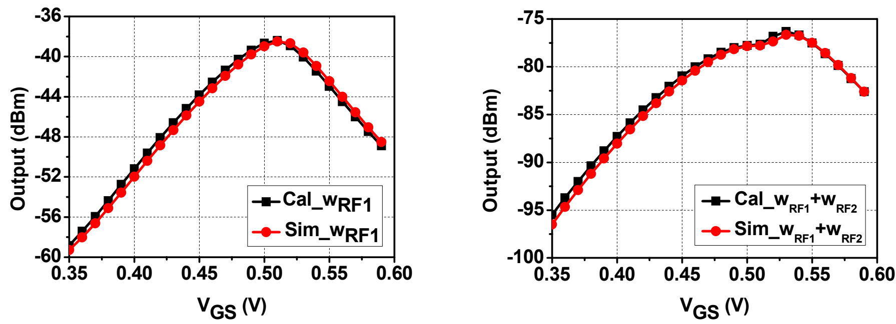


Fig. 4.15. Comparison of the simulation and the calculation results of the first-order response.

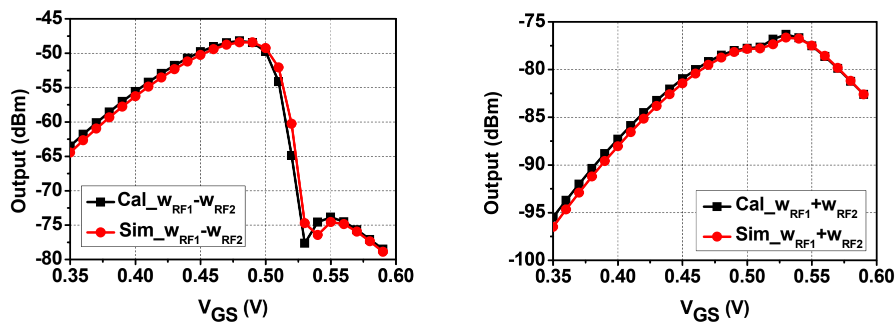


Fig. 4.16. Comparison of the simulation and the calculation results of the second-order response.

not degraded too much as compared to the voltage with the highest IF output. Consequently, the conversion gain can be reserved and the linearity can be improved tremendously.

Actually as the LO voltage swing is small the voltage offset between the simulation and the calculation results is around zero. The comparison of simulation and calculation results with LO power of -30dBm is shown in Fig. 4.15 to Fig. 4.19. This is because that the quantity of the nonlinear mixing to dc is very small so that it does not change the original dc bias condition, that is, it is still in the small signal condition.

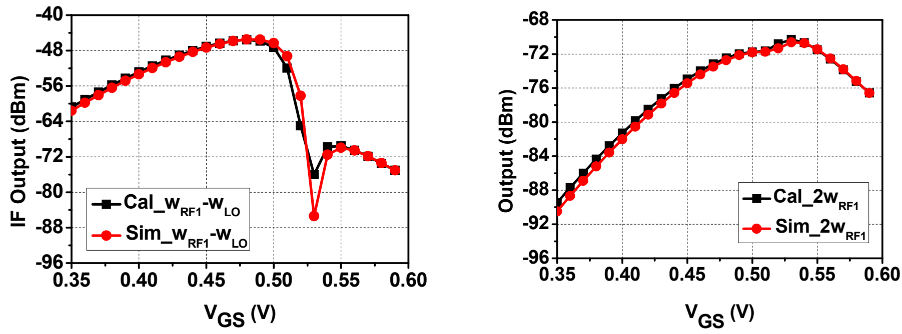


Fig. 4.17. Comparison of the simulation and the calculation results of the second-order response.

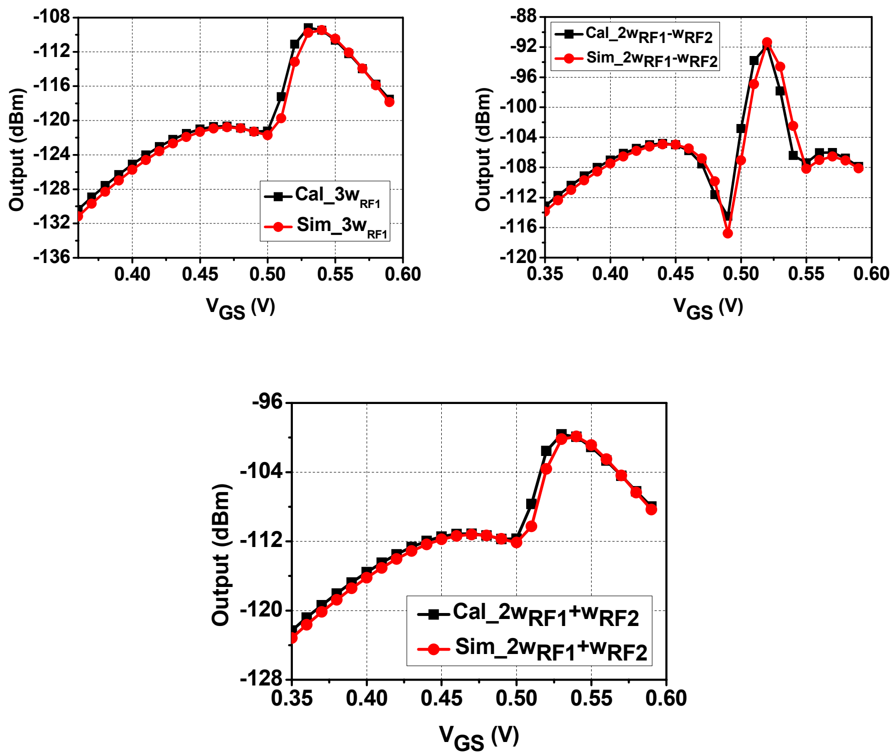


Fig. 4.18. Comparison of the simulation and the calculation results of the third-order response.

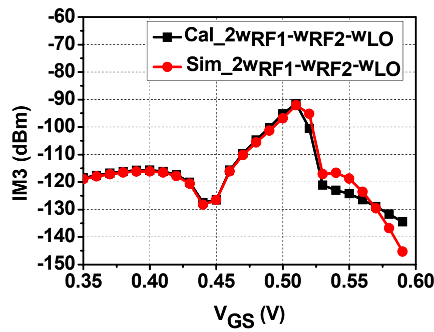


Fig. 4.19. Comparison of the simulation and the calculation results of the fourth-order response.

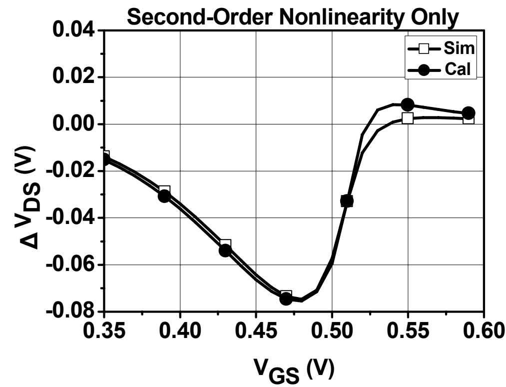


Fig. 4.20. Nonlinear mixing to the DC at the drain node. This DC offset at the VDS will increase the consumed drain current.

The reason for the voltage offset between the simulation and the calculation results as the LO power is -6dBm is due to the high frequency nonlinear current mixing to DC at drain node which alters the DC bias condition. This decrease in the drain to source voltage called ΔV_{DS} can be easily obtained by taking the second-order nonlinearity into consideration only. The calculation result of ΔV_{DS} is plotted in Fig. 4.20 which agrees well with the simulation result. If we take the ΔV_{DS} into consideration, we can make the calculation results approach simulation results very well even the LO power is large.

Furthermore, this ΔV_{DS} can predict the true drain current as the LO signal is going to drive the bulk-driven mixer. This operation current can be obtained by add ΔV_{DS} into the nodal equation as shown in the equation (4-19) where $V_{DS,HB}$ is simulation results at drain node at zero frequency using harmonic balance. The calculation and simulation results of the operation current match very well as shown in Fig. 4.21. So

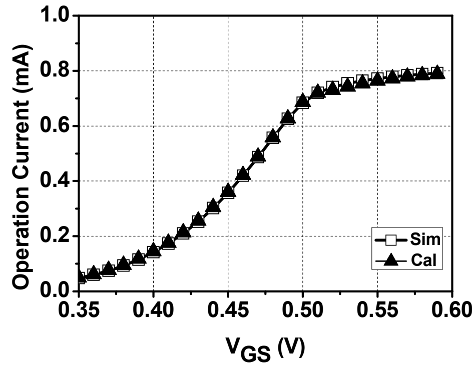


Fig. 4.21. Comparison of calculation and simulation results in operation current.

even the Volterra series is generally applied to a weakly nonlinear circuit, we can modify the changed bias condition due to nonlinear mixing and iterate the calculation to get the final converged result.

$$I_D = \frac{V_{DD} - V_{DS \cdot HB}}{R_L} = \frac{V_{DD} - (V_{DS \cdot DC} + \Delta V_{DS})}{R_L}$$

$$= I_{DC} - \frac{\Delta V_{DS}}{R_L} \tag{4-19}$$

4.3.3 Individual Response

The most important benefit of the direct calculation method is that we can find out the individual contribution of the nonlinear parameters to the conversion gain and IM3, respectively. The individual contribution to the voltage conversion gain and the IM3 under RF power of -40dBm and LO power of -6dBm are shown in Fig. 4.22, and Fig. 4.23, respectively. Fig. 4.22 indicates that the most important source to the conversion gain comes from the second-order nonlinear parameter $K_{2_{gm\&gmb}}$ which depends on g_m and g_{mb} simultaneously. This observation is different from the previous

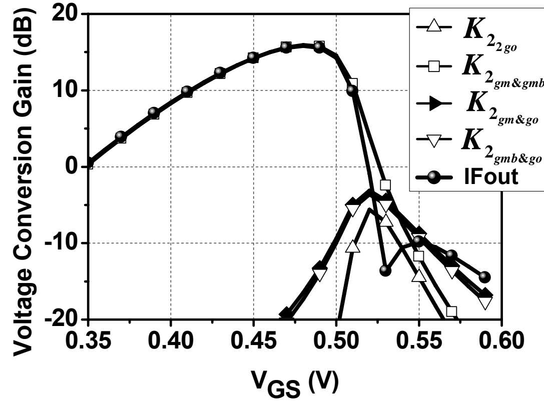


Fig. 4.22. The individual contribution to the voltage conversion gain.

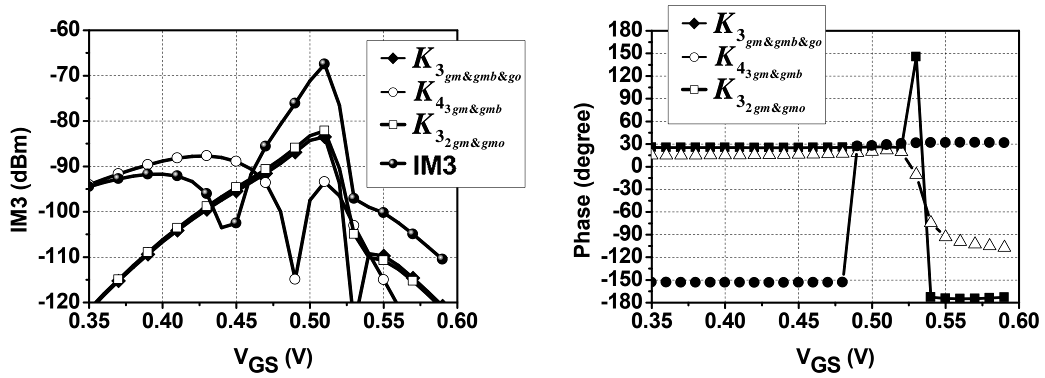


Fig. 4.23. The individual contribution to the IM3.

papers which claim the voltage conversion gain is from g_m only. There is a sweep spot behavior [8] around 0.45V meaning that the linearity of this circuit is very sensitive to the V_{GS} bias and so to the process variation. This sweet spot is due to the cancellation of the $K_{4_{3gm\&gmb}}$ contribution by those of $K_{3_{2gm\&gmo}}$ and $K_{3_{gm\&gmb\&go}}$. The V_{GS} corresponding to the minimal IM3 will move to a smaller value with the increase of the R_L, but the value of the minimal IM3 will also raise due to the larger nonlinear effect. Besides, the minimal IM3 also depends on the device size, too. Thus, we can decide the R_L value, the bias condition, and the device size, by

making a trade-off between the conversion gain and the linearity. In our design, the sweet spot behavior is mitigated by adding a feedback capacitance C_{fb} to have a high IIP3 over a wide V_{GS} range. Furthermore, we adjust the optimal gate bias to 0.4V for the purpose of low power consumption.

4.3.4 Current Mirror Bias Circuit

As shown in Fig. 4.24(a) the bias voltages for the optimal IIP3 at different corner case in the bulk-driven mixer are changed a lot if using voltage bias. Current mirror bias circuit as show in Fig. 4.25, can make the circuit more robust to process variation. The IIP3 versus the finger numbers of the transistors in the current mirror bias circuit is shown in Fig. 4.24(b). The voltage bias for the optimal IIP3 is almost the same now.

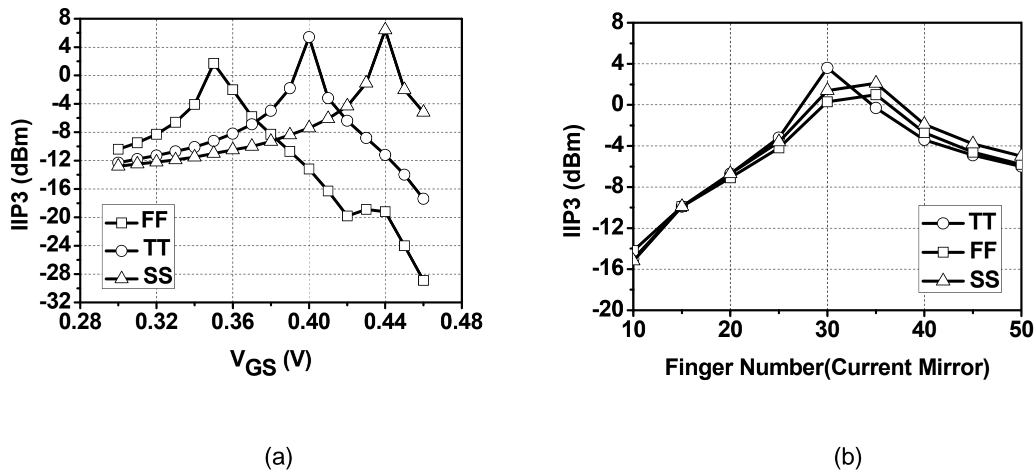


Fig. 4.24. IIP3 versus V_{GS} under different corner cases. (a) use voltage to bias. (b) use current mirror to bias.

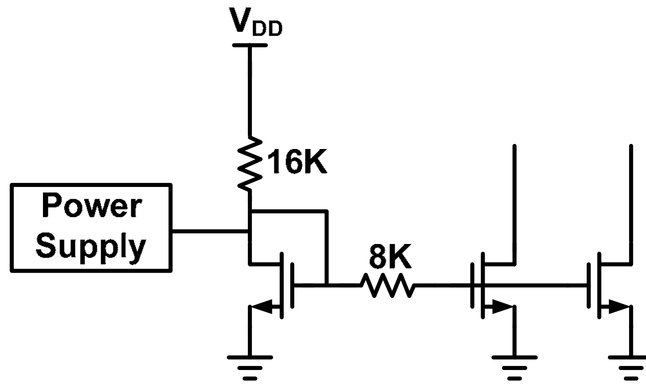


Fig. 4.25. The diagram of the current mirror bias circuit.

4.3.5 Matching Circuit

In general, input impedance of a common source is capacitive. Due to the feedback capacitance Cgd, R_L causes the input impedance to have a large real part. Small signal equivalent is still valid as the MOS operates in the subthreshold region. The input impedance can be computed as:

$$Z_{in} = \frac{v_{gs}}{i} = \frac{w^2 R C_{gd}^2 (1 + g_m R) - jw[w^2 R^2 C_{gd}^2 C_{gs} - (C_{gs} + C_{gd} + g_m R C_{gd})]}{w^2 [w^2 R^2 C_{gd}^2 C_{gs}^2 + (C_{gs} + C_{gd} + g_m R C_{gd})^2]}$$

$$\mathrm{Re}[Z_{in}] = \frac{R C_{gd}^2 (1 + g_m R)}{w^2 R^2 C_{gd}^2 C_{gs}^2 + (C_{gs} + C_{gd} + g_m R C_{gd})^2} \tag{4-20}$$

As seen from the equation (4-20), the real part is zero if the C_{gd} is zero, that is, no feedback path. So we use an L-match technique to make the input impedance match in 50Ω in the 1.4GHz. Actually the bulk-driven mixer has the potential to merge the LNA and the mixer into a single stage so that the power consumption can be low.

4.4 Measurement Results

4.4.1 On-Wafer Measurement Setup

Fig. 4.26 shows the measurement setup where RF and LO signals are given by probes, and DC bias pads are bonding to the FR4 board through bond-wires. The PCB layout is shown in Fig. 4.27. LO signal goes through a balun to transform to differential signals. IF outputs are connected to the output buffer with a unit gain. The micrograph of the chip is shown in Fig. 4.28.

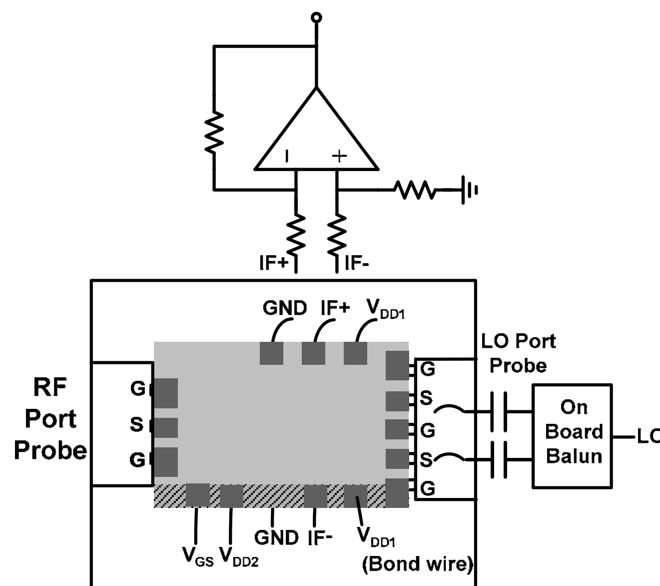


Fig. 4.26. Measurement setup for the on wafer measurement.

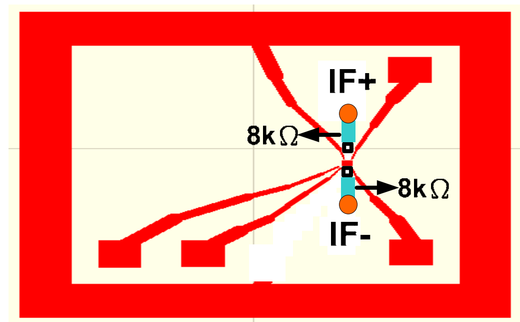


Fig. 4.27. PCB Layout.

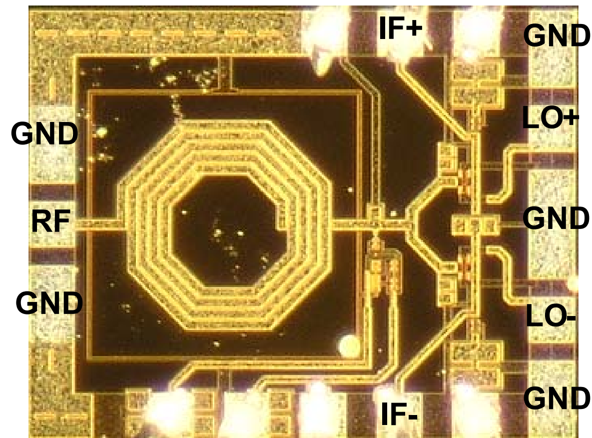
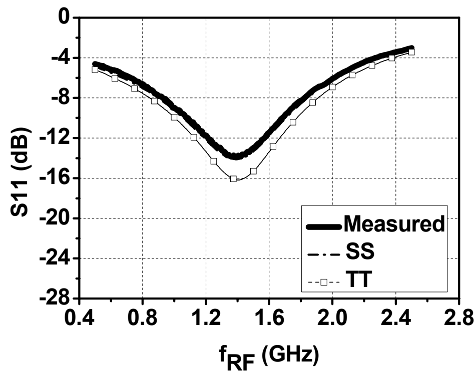
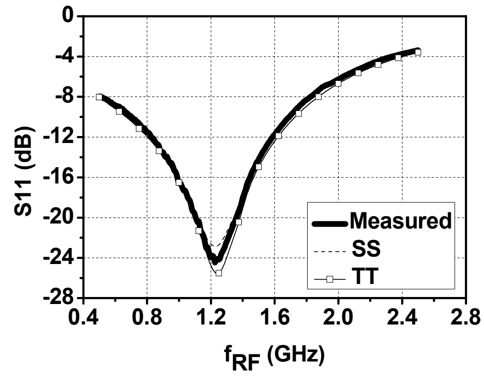


Fig. 4.28. Micrograph of the bulk-driven mixer.

4.4.2 Measurement Results

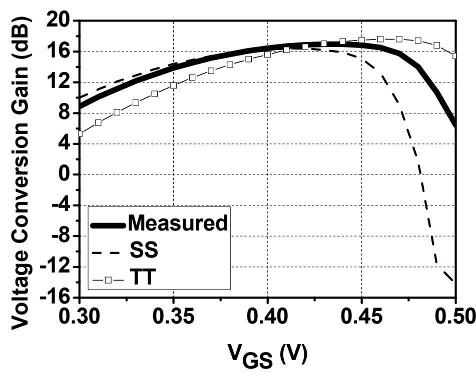
The frequencies of two RF signals and the LO signal in the measurement are 1.391 GHz, 1.392GHz, and 1.39 GHz, respectively. The power of the two RF signals is about -27dBm and the LO power is about -0.55dBm in the measurement. The circuit is still in the linear region as the RF power is -27dBm. So we can make the measurements on IIP3 accurately. The supply voltage is 1V and the standby power consumption is 0.25mW. The operation power is about 0.69mW. Fig. 4.29 shows the S11 measurement results under different LO power. As seen from the figure, the S11 is closed to simulation result. The Minimum of S11 moves to lower frequency as the LO power is increased. In our measurement that we set the LO power to -0.55dBm, nearly the same as simulation. The S11 is -18.1dB at 1.4GHz. The bandwidth is about 1GHz.

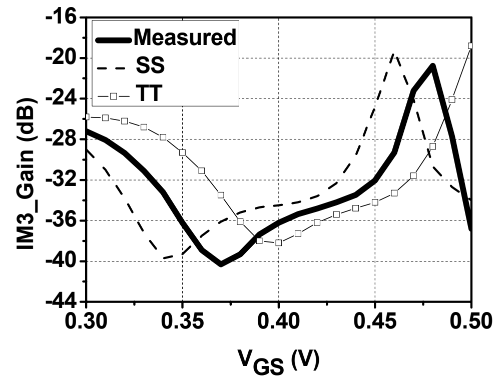




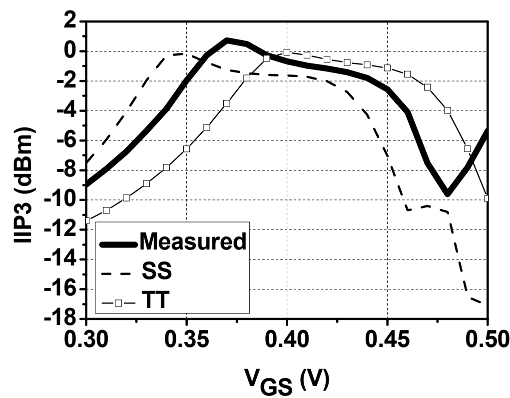
(a) (b)

Fig. 4.29. S11 measurement results. (a) LO is off. (b) LO is applied.



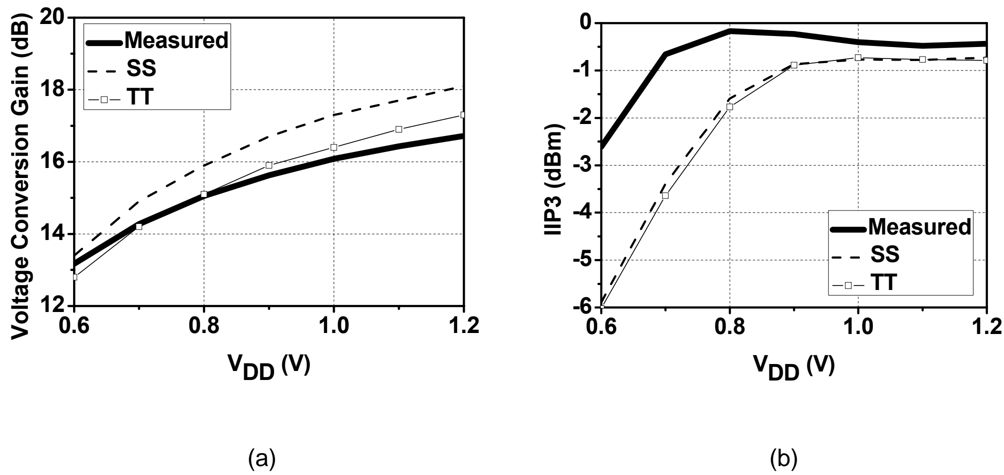


(a) (b)



(c)

Fig. 4.30. The measurements of the conversion gain, the IM3 gain, and the IIP3 versus V_{GS}. (a) voltage conversion gain. (b) the IM3 gain. (c) the IIP3.



(a) (b)

Fig. 4.31. The measurements of the conversion gain, and the IIP3 versus V_{GS}. (a) voltage conversion gain. (b)IIP3.

Fig. 4.30 shows the measurement results of the voltage conversion gain, IM3 gain, and the IIP3 versus V_{GS}. The VGS using the current mirror biasing is 0.39V. The measured data is between the SS and TT corner cases. The measured response is closed to the simulation.

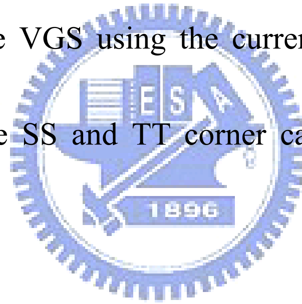


Fig. 4.31 shows the gain and the IIP3 versus supply voltage V_{DD}. In our design, the supply is set to 1V. As seen from Fig. 4.31, the bulk-driven mixer can operate at the supply voltage of 0.6V. The operation current at 0.6V is only 0.3mA corresponding to 0.18mW operation power. The voltage conversion gain is 13.2dB and the IIP3 is -2dBm.

The voltage conversion gain and the linearity versus the LO power is plotted in Fig. 4.32. Larger LO power has larger conversion gain and linearity, but the operation power is increased too. We are also interested in the LO power of -6dBm which is

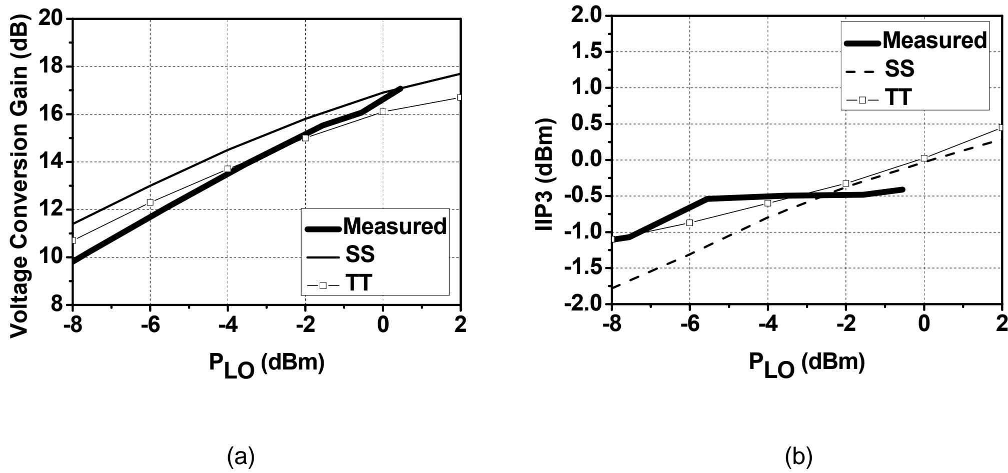


Fig. 4.32. The measurements of the conversion gain, and the IIP3 versus the LO power. (a) voltage conversion gain. (b)IIP3.

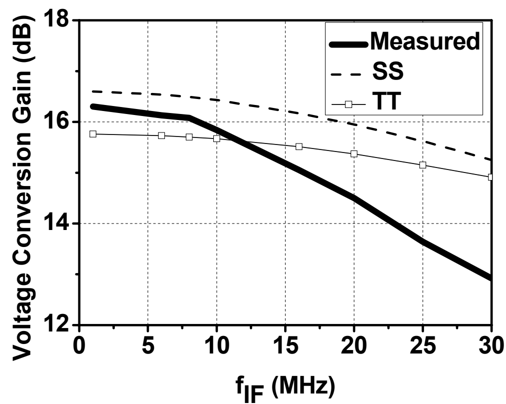


Fig. 4.33. The measurements of the conversion gain versus the IF frequency.

closed to the power level in the nonlinearity calculation. With LO power of -6dBm, the voltage conversion gain and the linearity are 12dB and 0.1dBm, respectively. Small LO power means the power consumption of the VCO can be low. So as integration of the mixer and the VCO, the whole circuit can really feature in the low power consumption.

Fig. 4.33 shows the voltage conversion gain versus the IF bandwidth. The RF

frequency is fixed to 1.4GHz and the frequency of the LO signal is swept from 1.37 GHz to 1.399GHz. The measured IF bandwidth is narrower than that of the simulation. This may come from the unknown factors in measurement setup associated with the PCB board and the external output buffer. Although the bandwidth is narrower, it still satisfies the required bandwidth of of 6 MHz in the WBAN application.

Fig. 4.34 shows the voltage conversion gain versus the RF bandwidth. The frequencies of the RF signal and LO signal change simultaneously to fix the IF frequency to 1MHz. The bandwidth is around 1.8 GHz. The voltage conversion gain is reduced as the high frequency because we have a low pass filter in the IF port.

Fig. 4.35 indicates the measurement results of the double sideband (DSB) noise figure(NF) of the bulk-driven mixer. The DSB NF is 19.65dB at the IF frequency of 10MHz. The measured DSB NF is around 3dB higher than the simulation results. This

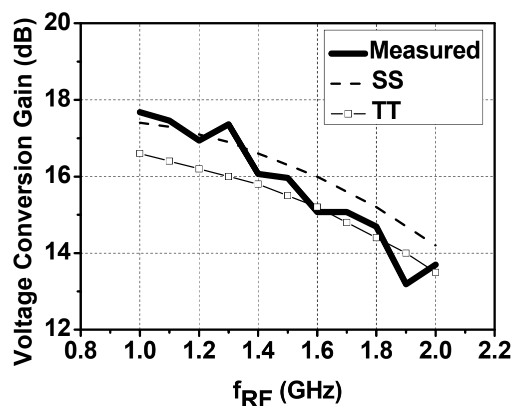


Fig. 4.34. The measurements of the conversion gain versus the IF frequency.

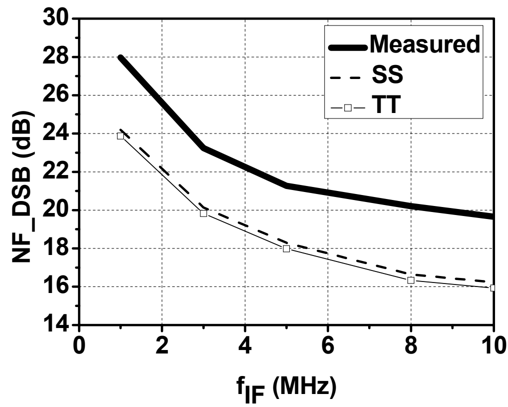


Fig. 4.35. The measurements of the DSB NF versus the IF frequency.

may due to the external parasitic effects coming from the measurement setup. In the application of WBAN, the noise figure is not important because the transmission distance is usually short.

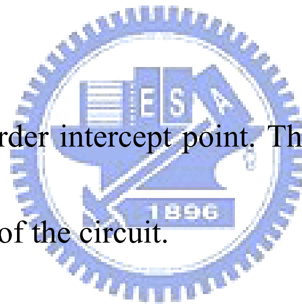


Fig. 4.36 shows the third-order intercept point. The IIP3 is around -0.5dBm using the current mirror for the bias of the circuit.

Table 4.6 summarizes the circuit performance and makes a comparison with the prior arts.

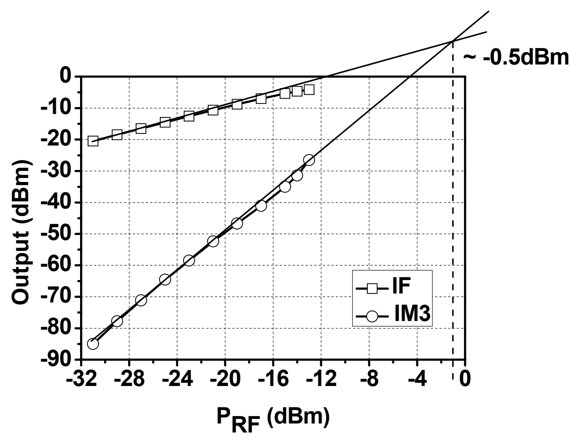


Fig. 4.36. The measurements of the IF and the IM3 versus the RF power.

Table 4.6 Comparison of the proposed bulk-driven mixer with the prior arts.

RF=1.4GHz LO= 1.399GHz	[3] Measured	[3] Measured	[4] Sim	[5] Measured	[6] Measured	This Work Measured		
RF (GHz)	2.1	6.9	0.9	12	1.9	**1.4**	**1.4**	**1.4**
Vdd (V)	1	1	1	1.2	0.8	**1**	**0.6**	**1**
Gain (dB)	6	6	2.1	3.2	1	**16**	**13.2**	**12.11**
LO (dBm)	2	7	N/A	9	0	**-0.55**	**-0.55**	**-5.55**
S11 (dB)	N/A	N/A	N/A	N/A	N/A	**-18.06**	**N/A**	**N/A**
NF (dB)	9.6 (DSB)	18 (DSB)	19.8 (DSB)	17.4 (DSB)	11 (SSB)	**19.65dB (DSB)**	**14.5dB* (DSB)**	**15dB* (DSB)**
IIP3 (dBm)	10	-2	16.65	-2.1	-9	**-0.5**	**-2.61**	**-0.54**
Power (mW)	0.14	0.18	1.6	1.8	0.4	**0.25 0.69****	**0.11 0.18****	**0.25 0.46****
Mixer Type	Switching mixer	Switching mixer	Switching mixer	Switching mixer	Switching mixer	**Nonlinear Mixer**	**Nonlinear Mixer**	**Nonlinear Mixer**
Technology	0.5um	0.5um	0.8um	90nm	0.18um	**0.18um**	**0.18um**	**0.18um**

*simulation. **Operation Power

4.5 Re-Tapeout of the Bulk-Driven Mixer

The measured IF bandwidth is narrower than that of the simulation. We find that the interconnections from the IF output to the measurement FR4 board affects the circuit performance a lot because the bulk-driven mixer has only one transistor, that is, the isolation between the IF output and the RF input is low. We believe that the issue of the narrow IF bandwidth comes from the unknown factors originated from the inevitable interconnections for the measurement purpose at the IF output. Thus, we

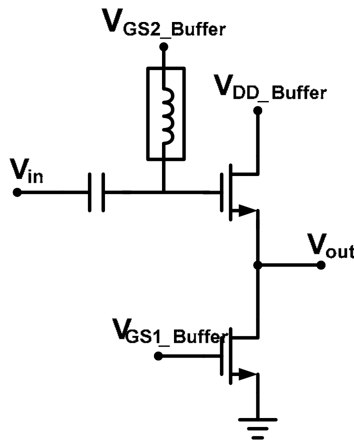


Fig. 4.37. The output buffer.

re-designed the bulk-driven mixer with an output buffer in the architecture of the source follower as shown in Fig. 4.37. The output buffer can help block out the influence of the undesired effect in the board. V_{GS1_Buffer}, V_{GS2_Buffer}, and V_{DD_Buffer} are 0.6V, 1.6V, and 1.8V, respectively. The additional bias voltage of V_{GS2_Buffer} is to keep a good linearity of the output buffer as the VGS of the core bulk-driven mixer is changed.

The simulation results are shown in Fig. 4.38 to Fig. 4.41. The circuit performance is summarized in Table 4.7.

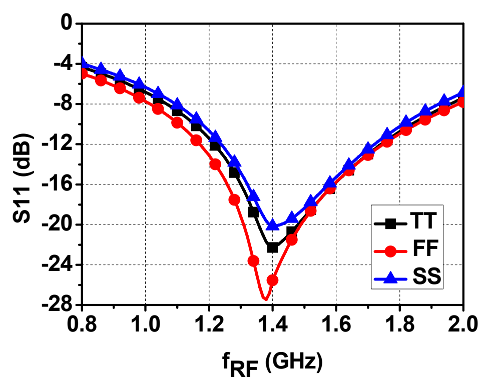


Fig. 4.38. The simulation results.

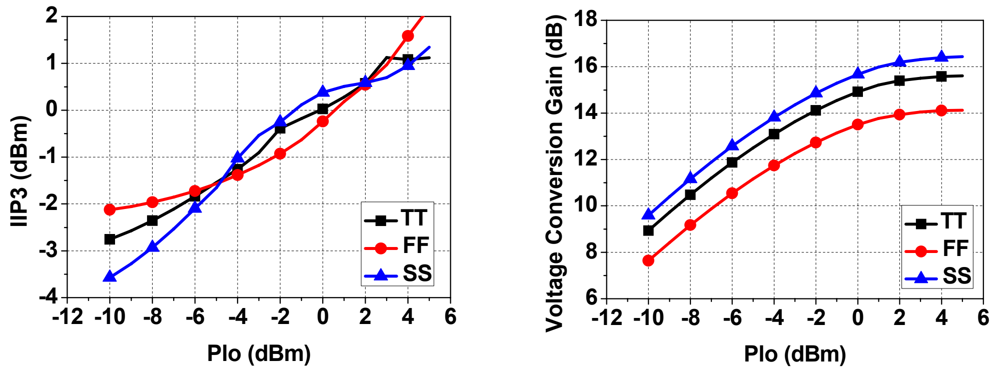


Fig. 4.39. The simulation results

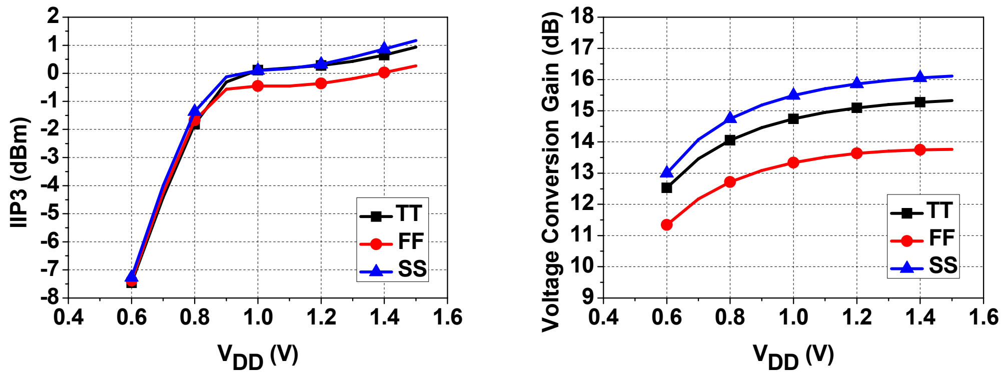


Fig. 4.40. The simulation results.

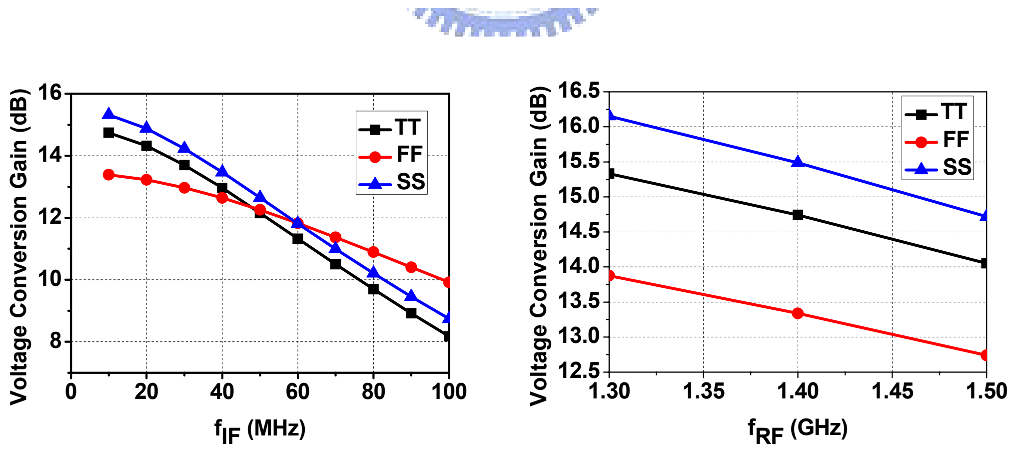


Fig. 4.41. The simulation results.

Table 4.7 Summary of the circuit performance of the re-tapeout bulk-driven mixer

RF：1.4GHz，LO：1.39GHz，LO：-0.5dBm VDD=1V，IF=10MHz	SS	FF	SF	FS	TT
Voltage Conversion Gain (dB)	15.5	13.3	14.8	14.2	14.7
IIP3 (dBm)	0.1	-0.4	0.19	-0.8	0.11
P-1dB (dBm)	-12.8	-13	-12.6	-13.2	-12.7
NF,DSB(dB)	16.4	15.4	16.7	15	16
S11 (dB)@1.4GHz	-19.7	-26.7	-23	-26	-24
LO to IF Isolation (dB)	-24.5	-22.6	-24	-24.5	-23.7
LO to RF Isolation (dB)	-70	-70	-70.8	-70.8	-70
RF to LO Isolation (dB)	-25	-25.6	-25.3	-25.4	-25
RF to IF Isolation (dB)	-36	-35.5	-36	-35.7	-35
Standby Power (mW)	0.24	0.33	0.28	0.28	0.27
Operation Power (mW)	0.59	0.6	0.66	0.52	0.58

Chapter 5 Summary and Future Work

5.1 Summary

In Chpater2, we designed a flip-chip interconnect for millimeter-wave application. The measurement results of the flip-chip structure shows return loss of 15dB and insertion loss of 1.7dB up to 50 GHz.

In Chapter 3 we design two VCOs using SoP technique. One of the two VCOs features in a high FOM. The other is designed to have a wide tuning range. The simulation results shows that the high FOM VCO has worse FOM of 191.2 dB, tuning range of 7% under power consumption of 1.03mW. For the wide tuning range VCO, its worse FOM and tuning range is 188dB and 17.6%, respectively. The power consumption is 1.08mW.

In Chapter 4 use variant Volterra series to analyze the nonlinearity of the bulk-driven mixer. The nonlinearity analysis results help us how to trade off between the gain and the linearity. The measurement results of the bulk-driven mixer hve the voltage conversion gain of 16dB, third-order intercept point of 3.5dBm, input return loss of 18.1dB, and the power consumption is only 0.24mW (0.69mW) in standby mode (operation mode). The bulk-driven mixer can further operate in a supply voltage of 0,6V. The voltage conversion gain is 13.2dB and the IIP3 is -2dBb under a power

consumption (operation) of 0.18mW.

5.2 Future Work

The flip-chip technology makes it possible to realize the system building on the package. We can integrate more RF modules to complete a single IC with high integration.

Bulk-driven mixer uses only one transistor to down-convert the RF signal. As shown in Fig. 5.1, it is possible to down-convert the RF signal twice in one stage by stacking the bulk-driven mixer with an additional switching pair to increase the flexibility in the receiver design.

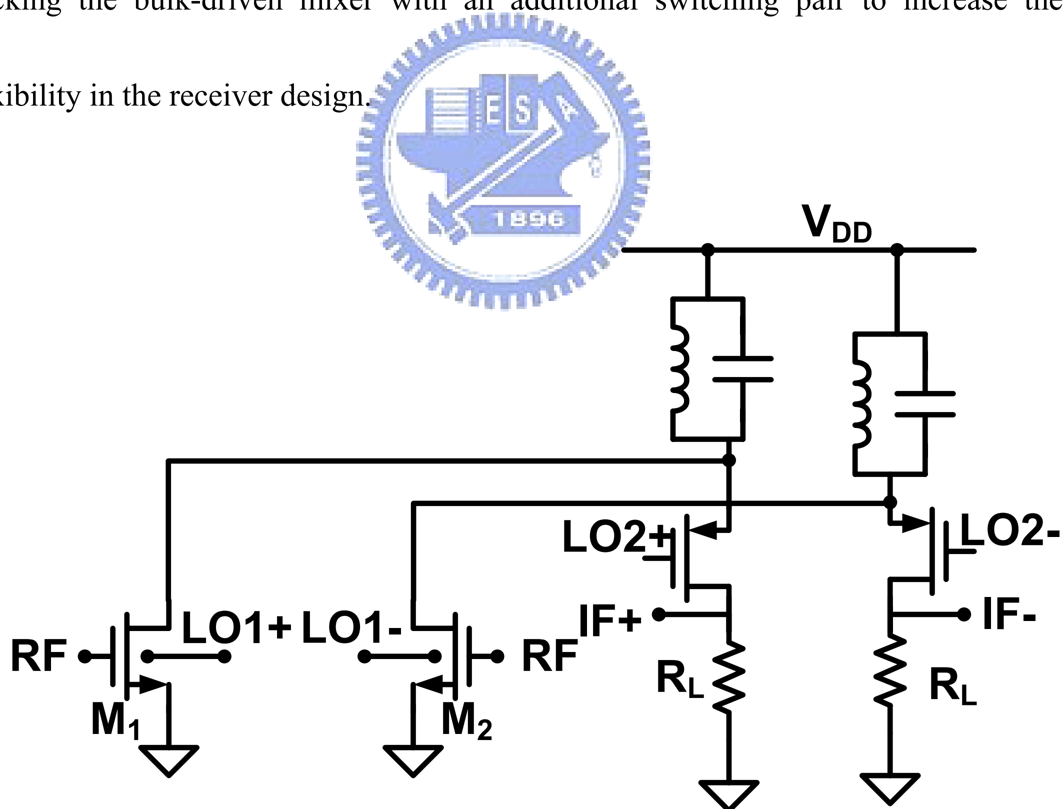


Fig. 5.1. Mixer topology for twice downconversion.

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Appendix A Fundamental of Phase Noise

Phase noise is one of the most important parameters in the VCO. The output of an ideal oscillator in the frequency domain consists of an impulse at the oscillation frequency w_o. However, in practical oscillator, the output spectrum has power around harmonics of w_o and, as a consequence of the fluctuations represented by ϕ(t) and A(t) in equation (A-1), the spectrum is not a impulse, but a shape of skirt as shown in Fig. A.1(b). These sidebands are generally referred to as phase noise sidebands.

$$V_{out}(t) = V_o \cdot [1 + A(t)] \cdot f[w_o t + \phi(t)] \tag{A-1}$$

For a radio receiver, suppose there is a strong interference in an adjacent channel, as shown in Fig. A.1(a). If the LO has large phase noise, some down-conversion of

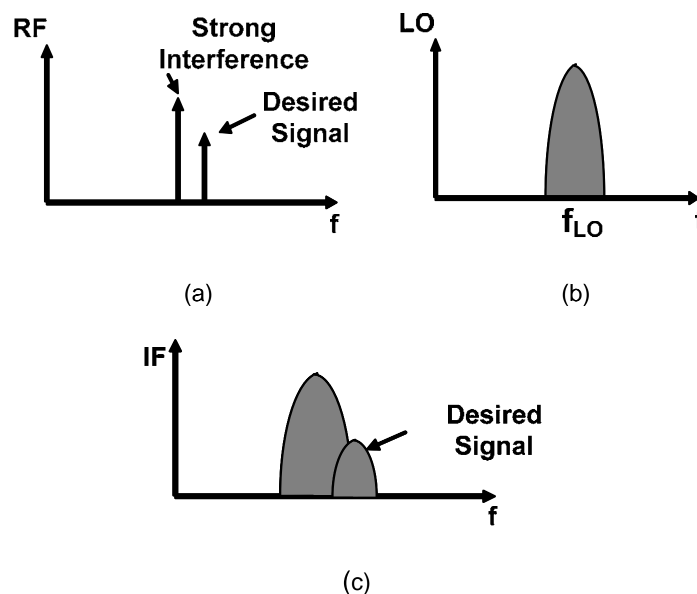


Fig. A.1. Influence of strong interference on dynamic range of receiver, (a) a strong interference adjacent to desired signal (b) practical spectrum in VCO output (c) impact of interference on the desired signal.

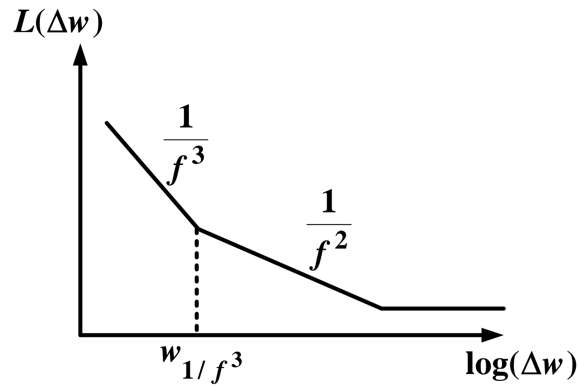
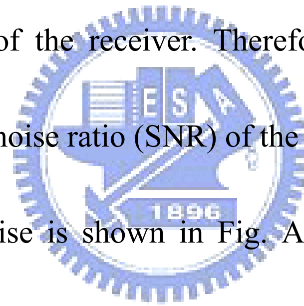


Fig. A.2. The spectrum of the phase noise. The $1/f^3$ region is mainly contributed by the flicker noise and the $1/f^2$ region is dominated by thermal noise.

the interfering signal into the same intermediate frequency (IF) as that of the desired signal will occur as shown in Fig. A.1(c). The resulting interference will significantly degrade the dynamic range of the receiver. Therefore, improving the phase noise clearly improve the signal-to-noise ratio (SNR) of the desired signal.



The spectrum of phase noise is shown in Fig. A.2. The phase noise in the $1/f^3$ region and the $1/f^2$ region are dominated by the flicker noise and the thermal noise, respectively. The most widely used phase noise model is Leeson's model based on a linear time-invariant (LTI) approach. It predicts the following behavior for the phase noise, L(Δ w) [18]:

$$L(\Delta w) = 10 \cdot \log[\frac{2FkT}{P_s} \cdot [1 + (\frac{w_o}{2Q_L \Delta w})^2] \cdot (1 + \frac{w_{1/f^3}}{|\Delta w|})] \qquad \text{(A-2)}$$

where F is an fitting parameter, often called a device excess noise number, and Q_L is the loaded Q of the tank. The drawback of Leeson's model is that it cannot predict the phase noise spectrum because of the fitting parameter "F" which is decided after

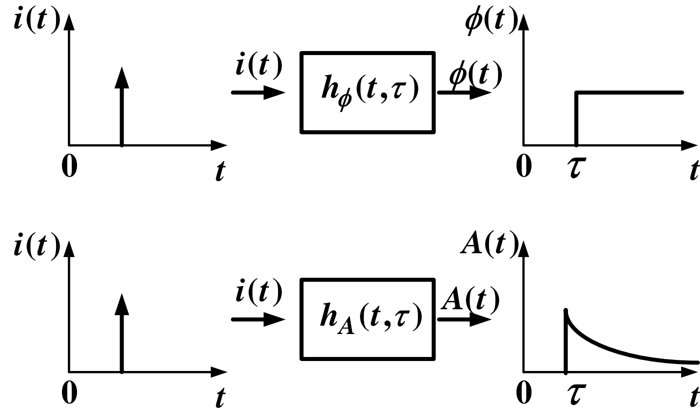


Fig. A.3. An equivalent systems for excess amplitude and phase response in phase noise analysis.

measurement.

Hajimiri and Thomas Lee propose the time-variant model to predict the response of the phase noise [18]. Since each input noise source generally affects both amplitude and phase, a pair of equivalent systems, one each for amplitude and phase, can be defined. The input of each system in Fig. A.3 is a perturbation current (or voltage) and the outputs are the excess phase ϕ(t), and amplitude, A(t), as defined by (A-1). In response to a current impulse, like a noise, the excess amplitude undergoes some transient behavior but finally converges to zero. However, fluctuations in the excess phase are not quenched by any restoring mechanism and therefore persist indefinitely so that the unit phase impulse response can be easily written as

$$h_{\phi}(t,\tau)=\frac{\Gamma(w_{o}\tau)}{q_{\max}}u(t,\tau) \tag{A-3}$$

where $q_{\max}=C\cdot V_{\max}$, u(t) is a unit step function, and $\Gamma(w_{o}\tau)$ is an impulse sensitivity function (ISF). Because the injected charge is linear to excess phase if the amount of injected chare is small, the output excess phase ϕ(t) can be calculated

using the superposition integral:

$$\phi(t) = \int_{-\infty}^{t} h_{\phi}(t,\tau) i(\tau) d\tau = \int_{-\infty}^{t} \frac{\Gamma(w_o \tau)}{q_{\max}} i(\tau) d\tau \tag{A-4}$$

Since ISF is periodic, it can be expanded in a Fourier series

$$\Gamma(w_o \tau) = c_0 + \sum_{n=1}^{\infty} c_n \cos(n w_o \tau + \theta_n) \tag{A-5}$$

Consider a white input noise current with power spectral density $i_n^2 / \Delta f$. ϕ(t) can be known from (A-4) and note by (A-6) that ϕ(t) makes a convolution with fundamental tone in the frequency domain to produce the phase noise sideband adjacent to the signal at w_o. Hence total single-sideband phase noise spectral density due to one noise source at an offset frequency Δw is given by (A-7).

$$Cos(w_o t + \phi(t)) = Cos(w_o t) Cos(\phi(t)) - Sin(w_o t) Sin(\phi(t))$$

$\approx Cos(w_o t) - \phi Sin(w_o t)$ if ϕ(t) is small. (A-6)

$$L(\Delta w) = 10 \cdot \log\left(\frac{\frac{\overline{i_n^2}}{\Delta f} \sum_{n=0}^{\infty} c_n^2}{4 q_{\max}^2 \Delta w^2}\right) \tag{A-7}$$

Equation (A-7) implys both upward and down ward frequency translations of noise into the noise near the carrier, as illustrated in Fig. A.4. This figure summarizes what the (A-7) tell us: Components of noise near integer multiples of the carrier frequency all fold into noise near the carrier itself. Noise near DC is upconverted, with relative weight given by coefficient c_o, so 1/f noise ultimately becomes $1/f^3$ noise near the carrier; noise near the carrier stays there, weighted by c_1.; and white noise near higher

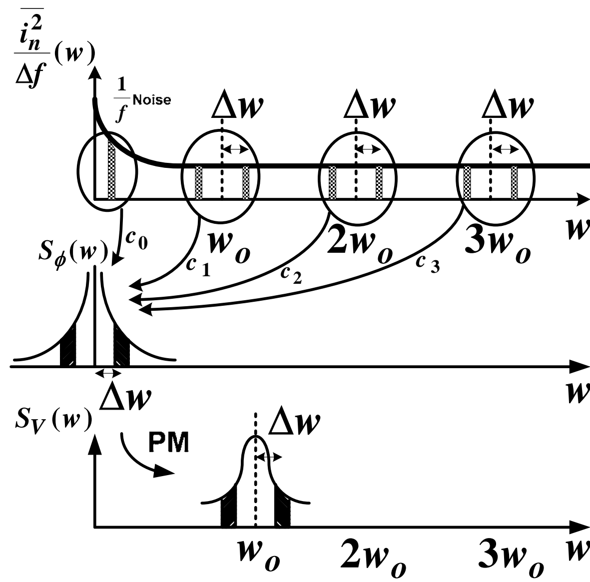


Fig. A.4. Evolution of circuit noise into phase noise.

harmonic of carrier undergoes downconversion into the $1/f^2$ region.

And according to Parseval's theorem,

$$\sum_{n=0}^{\infty} c_n^2 = \frac{1}{\pi}\int_0^{2\pi} |\Gamma(x)|^2\, dx = 2\Gamma_{rms}^2 \quad \text{(A-8)}$$

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where Γ_{rms} is the rms value of $\Gamma(x)$. So the phase noise in the $1/f^2$ region can be re-written as:

$$L(\Delta w) = 10 \cdot \log\left(\frac{\Gamma_{rms}^2}{q_{\max}^2} \frac{\frac{\overline{i_n^2}}{\Delta f}}{2\Delta w^2}\right) \quad \text{(A-9)}$$

So minimizing the Γ_{rms} will minimize the phase noise.

For the $1/f^3$ region, the flicker noise can be written as

$$\overline{i_{n,1/f}^2} = \overline{i_n^2} \cdot \frac{w_{1/f}}{\Delta w} \quad \text{(A-10)}$$

Hence the phase noise in the $1/f^3$ region can be obtained:

$$L(\Delta w) = 10 \cdot \log(\frac{c_o}{q_{\max}^2} \frac{\frac{\overline{i_n^2}}{\Delta f}}{2\Delta w^2} \cdot \frac{w_{1/f}}{\Delta w}) \tag{A-11}$$

The equation (A-11) tells us that VCO with a symmetric waveform can feature in low phase noise at low offset frequency due to less flicker noise contribution because of small c_0. So for a VCO design, we shall carefully design the circuit and make a symmetric layout to have a symmetric waveform.

In practical oscillators, the statistical properties of some of the random noise sources may change with time in a periodic manner. These sources are referred to as cyclostationary. A white cyclostationary noise current $i_n(t)$ can always be decompose as

$$i_n(t) = i_{no}(t) \cdot \alpha(w_o t) \tag{A-12}$$

where $i_{no}(t)$ is a white stationary process and $\alpha(w_o t)$ is a deterministic periodic function describing the noise amplitude modulation and therefore is referred to as the noise modulation function (NMF). So $\phi(t)$ may be re-written as:

$$\phi(t) == \int_{-\infty}^{t} \frac{\Gamma(w_o\tau)}{q_{\max}} i(\tau) d\tau = \int_{-\infty}^{t} i_{no}(\tau) \frac{\alpha(w_o\tau)\Gamma(w_o\tau)}{q_{\max}} d\tau \tag{A-13}$$

As can be seen, cyclostationary noise can be treated as a stationary noise applied to a system with a new ISF given by

$$\Gamma_{NMF}(x) = \Gamma(x) \cdot \alpha(x) \tag{A-14}$$

where $\alpha(x)$ can be derived easily from device noise characteristic and the noiseless

steady-state waveform.

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